Solid State Lighting Technol

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Solid State Lighting Reliability

Components to Systems

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Preface

Solid state lighting (SSL) is recognized as the second revolution in the history of lighting. The primary reason is the annual global energy bill saving of €300 billion and a reduction of 1,000 MT of CO_2 emission. As such, the SSL industry is expected to exceed €80 billion by 2020, which will in turn create new employment opportunities and revenues. A second reason is the promise of a long useful lifetime, with claims up to 80,000 h. As with any products, the consistency and reliability of SSL systems need to be ensured before they can be adopted in any applications. To add to the complexity, there is also a need to ensure that the cost of this technology needs to be comparable or even lower than the current technology. Although SSL systems with low reliability requirements have already been developed, they can only be used in applications that operate in modest environments or in noncritical applications. For demanding applications in terms of environmental conditions, such as automotive application, or where strict consistency is needed, such as healthcare applications and horticulture applications, the conventional lighting sources are currently still preferred until the reliability of SSL is proven in these applications. Therefore, the knowledge of reliability is crucial for the business success of SSL, but it is also a very scientific challenge. In principle, all components (LEDs, optics, drive electronics, controls, and thermal design) as well as the integrated system must live equally long and be highly efficient in order to fully utilize the product lifetime, compete with conventional light sources, and save energy.

It is currently not possible to qualify the SSL lifetime (10 years and beyond) before these products are available in the commercial market. This is a rather new challenge, since typical consumer electronics devices are expected to function for only 2–3 years. Predicting the reliability of traditional electronics devices is already very challenging due to their multidisciplinary issues, as well as their strong dependence on materials, design, manufacturing, and application. Predicting SSL reliability will be even more challenging since they are comprised of several levels and length scales of different failure modes. The tendency towards system integration, via advanced luminaries, System-in-Package approaches, and even heterogeneous 3D integrations poses an additional challenge on SSL reliability.

A functional SSL system comprises different functional subsystems working in close collaboration. These subsystems include the optics, drive electronics, controls, and thermal design. Hence, there is also a need to address the interaction between the different subsystems. Furthermore, an added challenge for system reliability is that accelerated testing condition for one subsystem is often too harsh for another subsystem. Alternatively, even the highest acceleration rate possible for one subsystem may be too low to be of any use for yet another subsystem. Hence, new techniques and methodologies are needed to accurately predict the system-level reliability of SSL systems. This would require advanced reliability testing methods, since today's available standards are mainly providing the probability at which LEDs may fail within a certain amount of time.

Today, no open literature that covers the reliability aspects for SSL exists, ranging from the Light Emitting Diode (LED) to the total luminiare of a system of luminaries. This book will provide the state-of-the-art knowledge and information on the reliability of SSL systems. It aims to be a reference book for SSL reliability from the performance of the (sub-) components to the total system. The reliability of LEDs and all other components (optics, drive electronics, controls, and thermal design) as well as the integrated system of an SSL luminiare will be covered. Various failure modes in SSL luminiare will be discussed. Different reliability testing and luminiare reliability testing performance will be introduced. The content has an optimal balance between theoretical knowledge and industrial applications, written by the leading experts with both profound theoretical achievement and rich industrial experience. Parts of the contents are firsthand results from research and development projects.

This book is part of a series on Solid State Lighting, edited by Prof. G.Q. Zhang. The series will systematically cover all key issues of solid state lighting technologies and applications.

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Delft, The Netherlands G.Q. Zhang

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Chapter 1
Quality and Reliability in Solid-State Lighting

T. de Groot, T. Vos, R.J.M.J. Vogels, and W.D. van Driel

Abstract Quality is the totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied needs. By this definition, quality is fuzzy but the needs are quantified by so-called critical to quality parameters (CTQs). Reliability is the probability that a system will perform its intended function under stated conditions for a specified period of time without failures. By this definition, reliability is a measure as function of time and, thus, a quantity. Reliability is often said to be the "quality over time," but this in not correct. Reliability has its own measures, so-called critical to reliability parameters (CTR), that can have a relation to the CTQs. This chapter gives a brief history of quality and reliability, their interaction and the impact for the change within lighting into the solid-state era.

1.1 Brief History in Quality

Quality and reliability both have a long history [1, 2]. No individual can claim "I invented quality" or "I invented reliability." Such simplistic hero worship has no basis in fact. Archeological sites, ancient cities and modern museums provide convincing evidence that "invention" of quality and reliability has been a continuing process over the millennia. There are inventions of several crucial techniques and/or methods such as the control chart (Shewhart), the Pareto principle (Juran), Weibull functions (Weibull) and the cause-and-effect fish bone diagram (Ishikawa). The application of such techniques in a successful manner better defines quality and reliability.

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The quality movement can trace its roots back to medieval Europe, where craftsmen began organizing into unions called guilds in the late thirteenth century. These guilds followed a so-called craftsmanship model. The real need for quality and quality control did not occur until the start of the industrial revolution. It started in Great Britain in the mid-1750s and grew into the Industrial Revolution in the early 1800s. Here, quality had an emphasis on product inspection. Following this revolution, in the early twentieth century, manufacturers began to include quality processes in quality practices. After the United States entered World War II, quality became a critical component of the war effort: bullets had to work consistently in all kind of rifles. Initially every bullet was inspected; later on the military began to use sampling techniques (using Walter Shewhart's statistical process control techniques). After World War II, Japan and the United States were the main players in quality control and moved from an inspection mode to a mode to improve all organizational processes that could influence the quality of the product. Industrial sectors such as automobiles and electronics were developing so fast that total quality management (TQM) became a must. Quality has moved beyond the manufacturing sector into such areas as service, health care, education, and government. Many organizations and industries use TQM with great success and the quality toolbox is filled with numerous techniques and methods, such as the following [2]:

- The ISO 9000 standards with sector-specific versions of quality management standards, developed for such industries as automotive (QS-9000), aerospace (AS9000) and telecommunications (TL 9000 and ISO/TS 16949,) and for environmental management (ISO 14000).
- Six sigma methodology developed by Motorola to improve its business processes by minimizing defects.
- Lean manufacturing.
- 8D (discipline) approach.
- Fault tree analysis.
- Failure Modes and Effects Analysis (FMEA).
- Pugh matrix.
- And many, many more.

The following definition of quality is used:

> Quality: The totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied needs.

1.2 Brief History in Reliability

The word reliability originates far sooner than most would guess [3, 4]. In 1816, Coleridge [5] used it in one of his poems obviously not having the same meaning to as we nowadays do so. He more used the word from a psychological perspective where reliability refers to the inconsistency of a measure. A test is consisted reliable

if we get the same result repeatedly. The history of reliability as we know it now goes back to the 1950s, when electronics played a major role for the first time. During the 1950s, there was great concern within the US military where half of the vacuum tubes were estimated to be down at any given time. In these days, many meetings and ad hoc groups were created to cope with the problems. In 1952, as an initiative between the department of defense and the American electronics industry [6], a study group was initiated under the name Advisory Group on the Reliability of Electronic Equipment (AGREE). This group recommended the following three items for the creation of reliable systems:

1. The need to develop better parts.
2. Establishing quantitative reliability requirements for parts.
3. Collecting field data on actual part failures to determine their root cause.

It may seem strange today but at that time there was considerable resistance to recognizing the stochastic nature of the time to failure, and hence reliability. With the basics ready, Shewhart and Weibull [7] already published their techniques, statistics as a tool for making measurements would become inseparable with the development of reliability concepts. During this period, 1950–1960s, several working groups and conferences were held to discuss the reliability topic; examples are the IEEE Reliability Conference, the Reliability Society, Rome Air Development Center (RADC), and the already-mentioned AGREE committee. Recommendations included running formal demonstration tests with statistical confidence and running longer and harsher environmental tests that included temperature and vibration. All led to the well-known Military Standards, such as MIL781 and MIL217 [8]. In this decade, reliability was driven by the demand from the military industry.

From the 1960s onwards to the 1970s, the complexity of electronic equipment began to increase significantly, and new demands were placed on reliability. Semiconductors came into more common use as small portable transistor radios appeared. This decade brought a heightened interest in system-level reliability and safety of complex engineering systems, such as nuclear power plants. In order to do so, people began to use the Weibull function and the further developed Weibull analysis methods and applications.

During the decade of the 1970s, reliability had expanded into a number of new areas; examples are the use of Failure Mode and Effect Analysis (FMEA), risk management through the use of reliability statistics, system safety and software assurance. For the latter one, the first rudimentary models originate from this period in time [9]. System safety was introduced by the railway industry, driven by the need for timely arrivals of its travelers.

The largest changes in reliability development occurred in the 1980s. Televisions had become all semiconductors, automobiles rapidly increased their use, and communication systems began to adopt electronic switches. Standards became worldwide accepted and implemented. During this decade, the failure rate of many components dropped by a factor of 10. Thus, by the decade end, dedicated reliability programs could be purchased for performing FMEA, reliability

predictions, block diagrams, and Weibull analysis. It was also the decade in which the people at home were confronted with a disaster that had a clear reliability nature: the challenger disaster, which occurred on January 28, 1986. This disaster caused people to reevaluate how to estimate risks.

By the 1990s and beyond, the pace of IC development ramped following the well-known Moore's law (number of transistors doubled every 18 months). It quickly became clear that high volume produced components often exceeded the reliability demands that came from the military specifications. Many of these military specifications became obsolete and best commercial practices were often adopted. Most self-respected industries developed their own reliability standards, examples are the JEDEC Standards for semiconductors [10] and the Automotive Standard Q100 and Q101.

The turn of the decade started with a well-known software reliability problem: Y2K. The Year 2000 problem (also known as the Y2K problem, the Millennium bug, the Y2K bug, or simply Y2K) was a problem some questioned whether the relative absence of computer failures was the result of the preparation undertaken or whether the significance of the problem had been overstated. We will never know, but it brought reliability failures and the cost of them closer to the consumer. Product development times decreased to periods below 12 months. This meant that reliability tools and tasks must be more closely tied to the development process itself.

Nowadays, products with high failure rates are logged on the Web leading to bad reputation for a company. In many ways, reliability is part of everyday life and part of consumer expectations. The word reliability is extensively used by the general public and the technical community, as illustrated by the following: there are over 3,000 published books whose title or keywords contain the word reliability; the Web of Science lists some 10,000 technical papers with "reliability" as a keyword (since 1973); and the popular search engine Google lists over 12 million occurrences of "reliability" on the World Wide Web.

The following definition of reliability is used:

> Reliability: The probability that a system will perform its intended function under stated conditions for a specified period of time without failures.

1.3 Note on Reliability Prediction

The term reliability-prediction is historically used to denote the process of applying mathematical models and data for the purpose of estimating field-reliability of a system before empirical data are available [11]. These predictions are used to evaluate design feasibility, compare design alternatives, identify potential failure areas, trade-off system design factors, and track reliability improvement. Reliability predictions are used successfully as a reliability engineering tool for at least five decades. But it is only one element of a well-structured reliability program.

There are basically two competing methods to predict reliability: (1) empirically based models or (2) physics-of-failure(POF)-based models [12]. Much of the literature on the topic of reliability prediction is centered on the debate which one the reliability discipline should focus on for the quantification of reliability.

Empirically based models have the following advantages:

- They reflect actual field failure rates and defect densities.
- They can be a good indicator of field reliability.

But the following disadvantages:

- They are difficult to keep up-to-date.
- They are difficult to collect good-quality field data.
- They are difficult to distinguish cause and effect.

PoF models have the following advantages:

- They model the specific failure mechanisms.
- They are valuable for predicting end of life for known failure mechanisms.

But they have the following disadvantages:

- They cannot be used to estimate field reliability.
- They can be highly complex and costly to apply.
- They cannot be used to model defect-driven failure.
- They are not practical for assessing an entire system.

Nowadays, most companies use a combination of the two methods: where failure mechanisms are well known PoF is used, where field data is available empirical models are used. Clearly, the purpose of a reliability prediction must be understood before a prediction methodology is chosen.

1.4 Linking Quality to Reliability

Reliability is often said to be the "quality over time," but this is not correct. Reliability has its own measures, so-called critical to reliability parameters (CTR), that can have a relation to the critical to quality parameters (CTQs). The link between those two parameters is hidden within two available measures:

- The number of product recalls.
- The Cost of nonquality (CoNQ).

A product recall is a request to return to the maker a batch or an entire production run of a product, usually due to the discovery of safety issues. The recall is an effort to limit liability for corporate negligence (which can cause costly legal penalties) and to improve or avoid damage to publicity. Recalls are costly to a company because they often entail replacing the recalled product or paying for damage caused by use, although possibly less costly than consequential costs caused by damage to

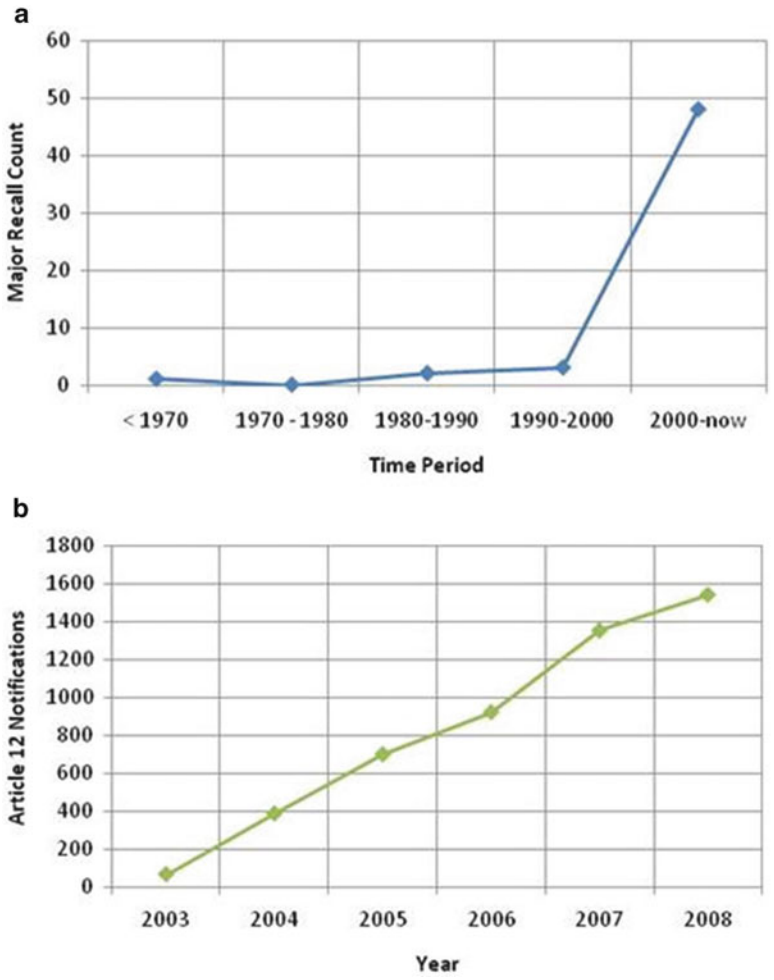


Fig. 1.1 Number of recalls as function of time with (**a**) major ones (>1 M$ costs) reported by recall.gov and (**b**) article 12 notifications (serious risk) by Rapex

brand name and reduced trust in the manufacturer. In the USA, the best source for recalls is recall.gov, in Europe it is Rapex [13]. Both sources are reporting a dramatic increase over time, see Fig. 1.1. Recall.gov presents an exponential increasing number of major ones in the period since 2000. Rapex presents a linear increasing number of notifications under article 12 which are notifications of measures ordered by the national authorities, or actions taken "voluntarily" by producers or distributors in relation to products presenting a serious risk.

The first major recall occurred in the USA in 1959 when General Motors Cadillac's car suffered from a steering linkage (pitman arm) that failed on many cars while making a 90° turn at 10–15 mph (24 km/h). It turned out to originate

Table 1.1 Cost of nonquality for a list of US-based multinationals in 2010 [15]

Company	Claims paid in 2010 (in M USD)	CoNQ (% of sales)
Boeing Co.	$141	0.40
Apple Inc.	$1,151	1.60
Harley-Davidson Inc.	$37	0.90
Cisco Systems Inc.	$471	1.30
Ford Motor Co.	$1,522	1.30
Microsoft Corp.	$82	0.50
IBM Corp.	$407	2.26
Dell Inc.	$1,146	2.31
General Motors Co.	$3,204	2.40
Hewlett-Packard Co.	$2,689	3.20
Lexmark International	$94	8.80

from a reliability issue; the arms were made of metal somewhat softer than that usually employed to withstand the stresses of low-speed turns. The most famous recall occurred worldwide in 2006, when all large notebook manufacturers had to recall their computer batteries. Over seven million batteries were recalled, after a number of instances where the batteries overheated or caught fire. The root cause turned out that a short-circuit failure becomes apparent as the batteries age and perform repetitive charging cycles, a clear example of reliability. One of the most recent recalls concerns DePuy's hip aid systems after finding that more people than expected suffered pain which required additional surgery. Over 93,000 units were sold and implanted but excessive wear out revealed a 13 % failure rate after only 5 years. Total cost of the recall is estimated to be $922 Million. Again an example of reliability.

CoNQ, also denoted by cost of poor quality (COPQ) or poor quality costs (PQC), is defined as costs that would disappear if systems, processes, and products were perfect. The term was popularized by IBM quality expert H. James Harrington [14]. The CoNQ has several origins, being yield loss during manufacturing, scrapping costs of parts, costs for rework in manufacturing, repair and/or recall cost and product liability costs. Table 1.1 lists the CoNQ% for a selected number of USA-based multinationals in 2010. It in total represents an amount of 11B$ which is spend by these multinationals on CoNQ for only the repair and/or recall part. On average the CoNQ of this list is 2.3 %, with clear outliers as low as 0.4 % and as high as 8.8 %. Note that 0 % does not occur and there is actually no enterprise or company that reaches a number below 0.4 % [13].

It is not straightforward to retrieve that part of the CoNQ that is related to the loss and/or lack of reliability. Repair and/or replacement of products may well be due to the fact that the product did not perform its intended function within the warrantee period. But manufacturing errors and scrapping parts are not related to reliability. A rough estimate reveals that approximately 40 % of the CoNQ are purely reliability related [16]. Off course this differs from industry to industry and strongly depends on the technology used.



Fig. 1.2 Linking quality to reliability: how long should your product last?

From a quality perspective, reliability involves two important dimensions beyond quality; they are time and stress. With respect to time, a product has to live (up to expectations) for 1, 2, 5, and perhaps 20 years in the hands of the customer. With respect to stress, the product must also function despite "life-threatening" stresses applied to it, such as temperature, vibration, shock, voltage transients, humidity and several other environments. Reliability techniques and practices thus introduce stress factors to accelerate the (un) known failure mechanisms. If one wants to link quality to reliability, all comes back to the basic question: how long should your product last? (Fig. 1.2).

1.5 A New Era in Lighting

Human civilization revolves around artificial light. Since its earliest incarnation as firelight to its most recent as electric light, artificial light is at the core of our existence. It has freed us from the temporal and spatial constraints of daylight by

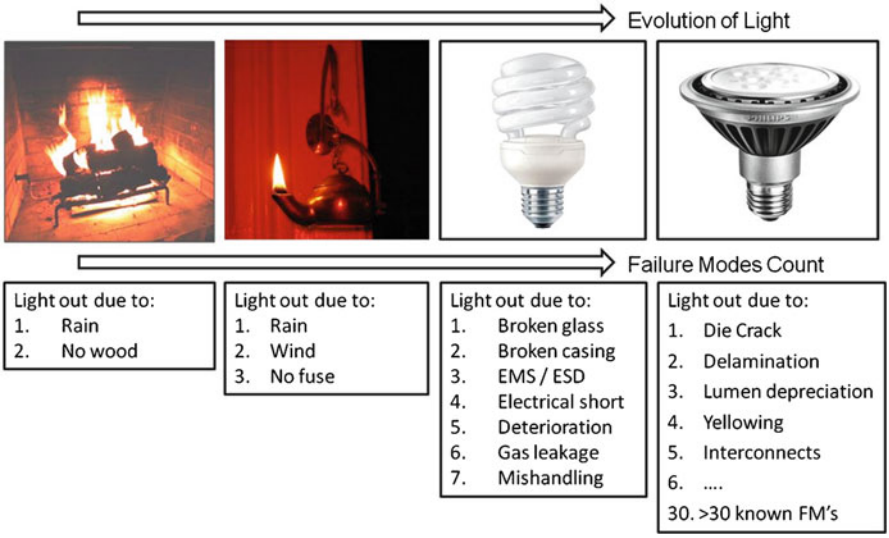


Fig. 1.3 With the evolution of light, the number of failure modes increased

allowing us to function equally well night and day, indoors and outdoors. It evolved from open fire, candles, carbon arc lamp, incandescent lamp, fluorescent lamp to what is now at our doorstep: solid-state lighting (SSL). SSL refers to a type of lighting that uses semiconductor light-emitting diodes (LEDs), organic or polymer light-emitting diodes (OLED/PLED) as sources of illumination rather than electrical filaments, plasma (used in arc lamps such as fluorescent lamps), or gas. SSL applications are now at the doorstep of massive market entry into our offices and homes. This penetration is mainly due to the promise of an increased reliability with an energy saving opportunity: a low cost reliable solution. But there is a catch to it.

Firstly, SSL is semiconductor based and it brings new processes and materials into a commercial business as old as 150 years. Quality enters a new domain with processes that used to be unknown. CTQs need to be redefined to cover the behavior of the SSL devices. For example, SSL performance strongly relies to its lumen depreciation in which the light source gradually but slowly degrades over time. The lighting industry is still struggling with this physical behavior of the new light source and no worldwide agreements and/or standards for lumen depreciation currently exist.

Secondly, new processes and materials will always introduce a series of new and unknown failure modes. In this particular case, the ones that are known from semiconductors are directly imported into the lighting products. Semiconductor failure modes are well described, but their relation to the quality of light is not known. Figure 1.3 visualize the failure mode increase effect due to the evolution of the light sources. The use of SSL has at least four-folded the number of failure modes that can occur in the lighting system. Experiences with these new modes need to be built using accelerated tests like HALT, MEOST and other techniques.

Thirdly, traditionally, luminaires are known to be everlasting and the light source is the limiting factor. This is covered by the luminaire design in which the light source could be easily interchanged. With the introduction of SSL it is no longer the light source that is the limiting factor for the product life. Other parts in the system, electronics, luminaires, connectors, taken an equally part in the field call rate of the product. In other words: there is a clear shift in the reliability budget for SSL applications. For the lighting industry, the next level of reliability assessment is beyond product reliability: system reliability is going to be important.

Fourthly, the promising lifetime numbers of 50.000 and higher burning hours are great, but how does one cover that? It needs accelerated test conditions both on product and component level which is a totally new approach for the lighting industry. The lighting industry is moving from offering a disposable product into a business that is selling cars: high reliability up to 10 years of service. Reliability is an important aspect of SSL applications but as a result of the strong customization, reliability estimations for these products start practically from scratch. It further needs close cooperations with customers to create clear and sound demands for the lifetimes of these applications.

Finally, the lighting industry does not have the installed reliability testing base that is needed to cover the promised lifetimes. Even more, there are no test standards available with appropriate pass/fail criteria for the (key) components and/or SSL products. Relationships with material and component supplier need to be tightened, as is the case in the automotive industry, in order to share the responsibility for the product quality and reliability.

In other words, a huge mindset change is needed in both quality and reliability to make the marked introduction of SSL application a big success. The handbook of quality needs to be rewritten and new reliability practices to be invented.

1.6 Final Remarks

Quality and reliability are not new, they exist for at least 6–8 decades. It is also not new for the lighting industry, in fact many lighting companies are using Six Sigma methodologies to design and manufacture their light sources and/or luminaires. With the introduction of semiconductors-based SSL devices, the challenge is to embed known-good practices from industries such as semiconductors, automotive, military, and aerospace into the veins of the lighting designers.

References

1. Juran JM (1995) A history of managing for quality. ASQ Quality Press, 600 N. Plankinton Ave, Milwaukee, WI 53203, USA. ISBN 0-87389-341-7
2. Tague NR (2005) The quality toolbox, 2nd edn. ASQ Quality Press, 600 N. Plankinton Ave, Milwaukee, WI 53203, USA. ISBN 0-87389-639-4

3. McLinn J (2011) A short history of reliability. J Reliab Inform 22:8–15
4. Saleh JH, Marais K (2006) Highlights from the early (and pre-) history of reliability engineering. Reliab Eng Syst Saf 91:249–256
5. Coleridge ST (1983) Biographia literaria. In: Engell J, Bate WJ (eds) The collected works of Samuel Taylor Coleridge. Princeton University Press, Princeton, NJ
6. Coppola A (1984) Reliability engineering of electronic equipment: a historical perspective. IEEE Trans Reliab R-33(1):29–35
7. Weibull W (1951) A statistical distribution function of wide applicability. ASME J Appl Mech 18(3):293–297
8. Mil standards are available at: http://www.dsp.dla.mil/
9. Moranda PB (1975) Prediction of software reliability during debugging. In: Proceedings of annual reliability and maintainability symposium, IEEE, New York, pp 327–332
10. Jeded standards are available at http://www.jedec.org/
11. Denson W (1998) The history of reliability prediction. IEEE Trans Reliab 47(3-SP):321–328
12. Calce: Center for Advanced Life Cycle Engineering. http://www.calce.umd.edu/
13. Listed recall information on the worldwide internet: http://www.recalls.gov/ and http://ec.europa.eu/consumers/dyna/rapex/rapex_archives_en.cfm
14. Harrington HJ (1987) Poor-quality cost. ASQ Quality Press, 600 N. Plankinton Ave, Milwaukee, WI 53203, USA. ISBN 9780824777432
15. Warrantee Week (2011) Warranty claims & accruals in financial statements, 16 Sept 2011. http://www.warrantyweek.com/
16. Schiffauerova A, Thomson V (2006) A review of research on cost of quality models and best practices. Int J Qual Reliab Manage 23(4):647–669

Chapter 2
Solid-State Lighting Technology in a Nutshell

C.A. Yuan, C.N. Han, H.M. Liu, and W.D. van Driel

Abstract Solid-state lighting (SSL) is the most promising energy saving solution for future lighting applications. SSL is digital and multi-scaled in nature: SSL is based on the semiconductor-based LED and its packaging technology. The LED module can be obtained by cooperation of electronic devices. By integrating the hardware and software, the luminaire and further lighting system can be achieved. This chapter will describe the key elements of SSL technology as the fundamental information towards SSL reliability.

2.1 Introduction

Light technologies are substitutes for sunlight in the 425–675 nm spectral regions where sunlight is most concentrated and to which the human eye has evolved to be most sensitive.

Three major light sources have much different principles:

- Incandescence lamp: The tungsten filament is heated by electric current until it glows and emits light.
- Fluorescent lamp: Mercury atoms are excited by an electric arc and emit UV radiation, and such radiation will strike the phosphor coating inside the glass tube, where the UV light will be converted into visible light.

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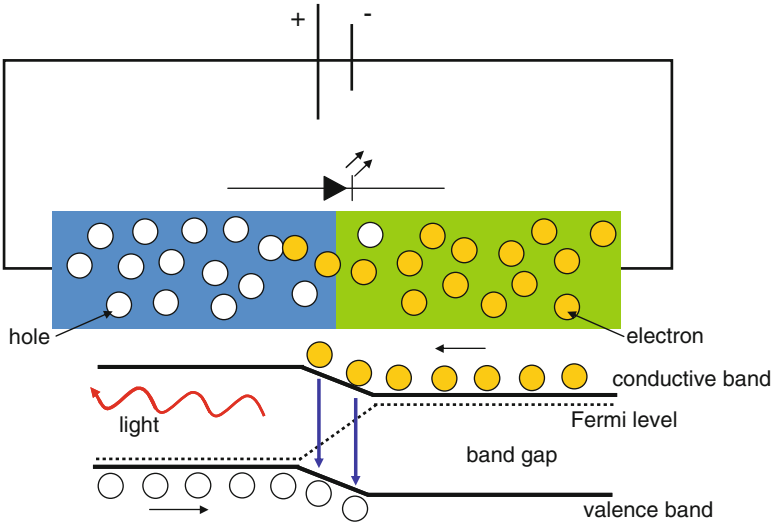


Fig. 2.1 Working principle of an LED

- Solid-state lighting: LED is a semiconductor diode, where the materials are doped with impurities to create p–n junction (as illustrated in Fig. 2.1). When the LED is powered, electrons flow from n-side (cathode) to p-side (anode). (electrons and holes) flow into the function and form electrodes. When an electron meets a hole, it falls into a lower energy level and releases energy in the form of photons [1]. The specific wavelength emitted by LED depends upon the band gap structure (or materials).

Because the light from SSL is narrowband, and can be concentrated in the visible portion of the spectrum, it has, like fluorescence, much higher light-emission efficiency than incandescence. Unlike in fluorescence technology, the wavelength of the narrowband emission can be tailored relatively easily. Hence, this technology is potentially even more efficient than fluorescence.

Lighting is going through a radical transformation, driven by various societal, economical, and environmental needs and rapid progress of solid-state lighting (SSL) and system-related technologies. The value chain of SSL is illustrated in Fig. 2.2 [2]. SSL begins with semiconductor-based LED technology and its packaging. The multiple LED assembly is obtained to be the basic assembly unit for the LED module and luminaire. The combination of electronics is required to proper drive the lighting function. The SSL-based lighting systems can be achieved by combination of hardware and software.

Three qualitative measurements are usually applied to define the quality of LED lighting:

1. Lighting efficiency, as knows as efficacy, enables the comparison of the efficiency of different types of lighting technology. Efficacy is usually defined by



Fig. 2.2 SSL value chain

Table 2.1 Efficacy, CRI and lifetime of common light sources [3]

Light source	Efficacy (lm/W)	CRI	Lifetime (h)
Incandescent (120 V)	14.4	~100	1,000
Compact fluorescent	51	80	10,000
High-pressure mercury	34	50	24,000
High-pressure sodium	108	22	24,000
LED	130–220	>80	50,000

lumens/watt (lm/W), and light source with higher efficacy refers to high energy efficiency. The luminous intensity of an LED is approximately proportional to the amount of current supplied to the device. The design/process limitation provides the upper boundary on both input current and light intensity.

2. Color rendering index (CRI), is another measurement of the lighting quality. CRI is a quantitative measure of the ability of a light source to reproduce the colors of various objects faithfully in comparison with an ideal or natural light source.
3. Lifetime is a reliability parameter of the light source. It represents the working time of such light source within the lighting specification.

Table 2.1 presents examples of the overall efficacy for common light source.

In the following chapter, the process at each SSL value chain, such as LED chips, LED packages, multi-LED assembles, LED modules, luminaires, and large SSL systems, will be presented.

2.2 Level 0: LED Chips

2.2.1 Overview

In recent years, high-brightness LEDs have attracted much attention as light sources for various applications, such as LCD backlighting, camera flash light, indoor lighting, and all kinds of outdoor signs. LEDs are semiconductor devices that emit incoherent narrow-spectrum light when electrically biased in the forward direction. The color of the emitted light depends on the chemical composition of the semiconducting material used and can be near-ultraviolet, visible, or infrared. Progress in the development of new materials for LEDs has continued to since the first red light emitting gallium arsenide phosphate (GaAsP) devices were introduced in low volumes in the early 1960s and in high volumes later in the decade. The materials first developed were p–n homojunction diodes in $GaAs_{1-x}P_x$ and zinc-oxygen-doped GaP for red-spectrum devices; nitrogen-doped $GaAs_{1-x}P_x$ for red, orange, and yellow devices; and nitrogen-doped GaP for yellow-green devices. A milestone was reached in the mid-1980s with the development and introduction of aluminum gallium arsenide (AlGaAs) LEDs, which used a direct band-gap material system and a highly efficient double heterostructure (DH) active region. In 1990, Hewlett-Packard Company and Toshiba Corporation independently developed and introduced a new family of LEDs based on the quaternary alloy material system: AlGaInP.

The luminous efficiency of the different materials of LEDs versus wavelength is shown in Fig. 2.3. The figure indicates that low-power and low-cost LEDs, such as

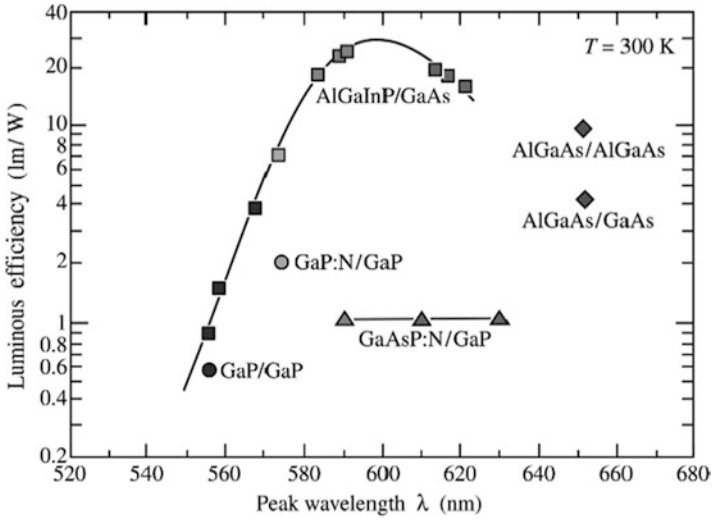


Fig. 2.3 Overview of luminous efficiency of visible LEDs made from phosphide, arsenide, and nitride material system (adopted from United Epitaxy Corp., 1999; updated 2000)

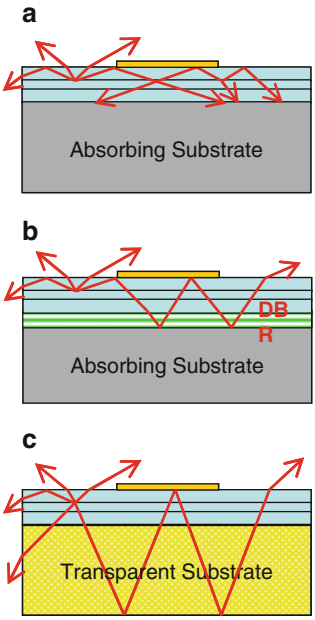


Fig. 2.4 Schematic cross-section view of different type of AlGaInP LEDs: (**a**) absorbing substrate (AS); (**b**) absorbing substrate (AS) with DBR; (**c**) transparent substrate (TS)

GaAsP and GaP:N LEDs, have much lower luminous efficiency. These LEDs are not suitable for high-brightness applications because of their inherently lower quantum efficiency. The GaAsP LEDs are mismatched to the GaAs substrate and therefore have a low internal efficiency. The GaP:N LEDs also have low efficiency because of the nitrogen-impurity-assisted nature of the radiative transition. However, AlGaInP LEDs have high luminous efficiency suited to the visible spectrum from the 570 nm (yellow) to 650 nm (orange). Hence, AlGaInP LEDs are an excellent choice for high luminous efficiency devices in the long-wavelength part of the visible spectrum. New record light-efficiency levels were achieved for this spectral regime, and as a consequence, new applications for LEDs are in the process of being developed.

2.2.2 Long Wavelength LED Technology: AlGaInP System

Today, the quaternary alloy AlGaInP material system is the primary material system used for high-brightness LEDs emitting in the long-wavelength part of the visible spectrum [4–6]. The AlGaInP epitaxial layer can be lattice matched to GaAs and is grown by MOCVD/MOVPE [7]. It has been introduced to yield substantial improvement in the performance in the red-orange and amber spectral regions and potentially in the green. Conventional AlGaInP LEDs are shown in Fig. 2.4a. Nevertheless, the portion of the light emitted from the active layer towards the substrate is completely absorbed by the GaAs absorbing substrate.

Therefore, the external quantum efficiency of this kind of conventional AlGaInP LED is small. The thermal conductivity of GaAs is only 44 W/m K. The low thermal conductivity of the GaAs substrate is not sufficient to dissipate the heat generated when the LED device is driven in high current.

The substrate absorption problem can be minimized by growing a distributed Bragg reflector (DBR) between the LED epitaxial layer and the absorbing GaAs substrate, as shown in Fig. 2.4b. However, the maximum reflectivity of the DBR layer used in AlGaInP LED is only about 80%, and its reflectivity also depends on the reflection angle. The DBR layer can only reflect the light near the normal incidence. For the oblique angles of radiated light, the DBR layer becomes transparent, and light will be absorbed by the GaAs substrate [8–11]. Hence, a more significant improvement in extraction efficiency is to replace GaAs with GaP transparent substrate through the wafer bonding process after epitaxial lattice matched growth. Thus, in Fig. 2.4c, this new class of AlGaInP LEDs called transparent-substrate (TS) LEDs is compared with the absorbing-substrate (AS) LED on GaAs-wafers. Figure 2.4 shows the comparison with the three types of AlGaInP LEDs.

Despite the improvements in extraction efficiency, the use of LEDs in high input power applications remains limited because of the low thermal conductivity of the substrate. To achieve higher light output performance, it is necessary to drive the LED at a higher current and to use a substrate with high thermal conductivity to efficiently dissipate heat from active layer. Many companies fabricated AlGaInP LEDs on Si-wafers using a metal combination of Au and AuBe for bonding. Despite the intermediate dielectric layer, the LEDs benefited from the good thermal properties of silicon, which has 3.2 times higher thermal conductivity than GaAs, thus providing a good heat dissipating ability. The increased thermal conductivity decreases joule heating and increases the quantum efficiency of the LEDs. Researchers successfully replaced GaAs with Cu substrate. This Cu-substrate-bonded LED device can be operated in a much higher injection forward current and high luminous intensity, several times higher than those used in traditional AS LEDs. The transparent conducting ITO and reflective layer between the epitaxial layer and the substrate to enhance the light extraction efficiency were also added. The luminous intensity of this design was 1.46 times greater than that of the conventional LED in the normal direction, and the output power (at 350 mA) increased by approximately 40% as compared with that of the conventional LED. Today, as the development of AlGaInP LEDs progresses, the most effective design to improve its external quantum heat dissipation ability is to combine the reflective structure with a high thermal conductive substrate through the metal bonding technique. However, because of the different CTEs and the intrinsic stress between different materials in the LED device structure, the crack problem may occur either during the removal etching process of the GaAs substrate or the annealing process after the GaAs removal.

The high-brightness LED structure was designed and fabricated by Epistar Corporation. The structural diagram of the LED is shown as Fig. 2.5. The multilayer film-substrate structure, which includes a number of staked films, such as an epitaxial layer of LED, SiO_2 isolation structure, ITO layer, silver (Ag) mirror layer, and eutectic bonding metal of gold/indium materials ($AuIn_2$), was in the range of

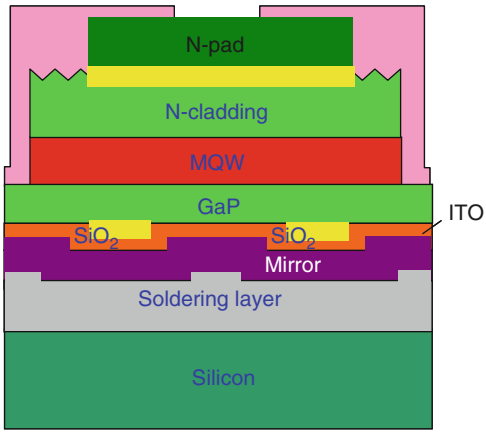


Fig. 2.5 The structural diagram of high-brightness AlGaInP LED

several micrometers to hundreds of angstrom. In addition, the GaAs substrate was replaced with a silicon substrate through the eutectic metal bonding technique. The detailed dimensions of each component will be introduced in the next chapter. The LED structures were grown on 3-in. GaAs wafers through low-pressure metalorganic chemical vapor deposition (MOCVD), with an average fabricated temperature of 750°C. The LED structure consisted of an n-GaAs buffer layer, n-InGaP etching stop layer, n-GaAs ohmic contact layer, AlInP n-cladding layer, undoped AlGaInP MQW active region, AlInP p-cladding layer, and a p-GaP window layer. The PECVD SiO_2 structure was fabricated at 200°C and patterned by an etching process. The ITO layer was placed on the AlGaInP LED to act as a current-spreading layer and was fabricated by an electron beam gun (E-Gun) evaporation system at 330°C. The Ag layer was deposited on the ITO layer to act as a mirror layer at 50°C. Then, the first bonding metals of Ti/Pt/Au/In were deposited at 80°C. The second bonding metals of Ti/Pt/Au were deposited on the host Si substrate [10], which served as a heat sink substrate. The thermal conductivity of the Si substrate was 124 W/m K, which is much higher than the value of GaAs base (44 W/m K).

2.2.3 Blue LED Technology: InGaN/GaN System

Starting early in the twentieth century, there were several reports of light emission from materials due to applied electric fields, and a phenomenon termed "electroluminescence" (EL). Due to that the materials properties were poorly controlled, and the emission processes were not well understood. For example, the first report in 1923 of blue EL was based on light emission from particles of SiC which had been manufactured as sandpaper grit, and which contained "unintentionally" p–n junctions. By the late 1960s, SiC had been extensively

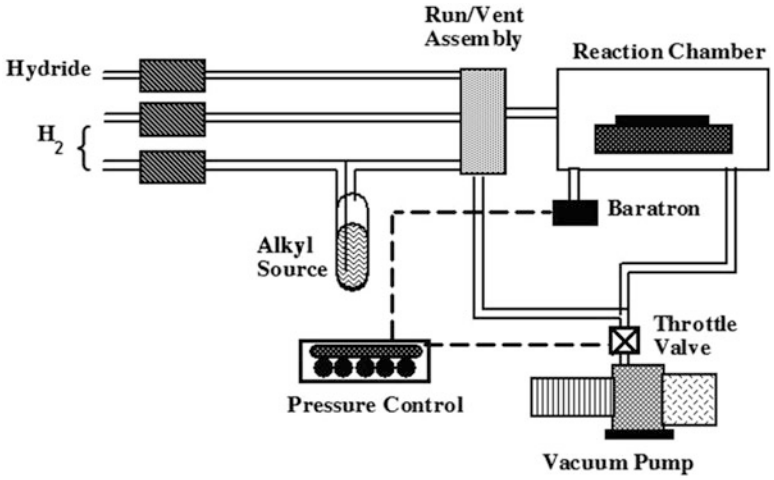


Fig. 2.6 Schematic diagram of MOCVD system

studied in order to enhance the efficiency. However, it was never more than about 0.005% due to SiC naturally being an indirect band gap material. The best efficiency of SiC LEDs till now is only 0.03% emitted at 470 nm.

The high brightness blue LED is actually implemented by InGaN/GaN material system. Studies of GaN material can be traced back into 1930s and 1940s. In the late 1960s, researchers attempt to grow GaN film from halide vapor phase epitaxy (HVPE) approach and obtained single GaN film on heterogeneous substrate (e.g., sapphire). However, all the GaN film grown at early 1960s were naturally n-type without intentionally doping, and it was a great challenge to implement p-type GaN film, because the lack of p–n junctions in Group III nitrides (and their poor crystal growth quality) stalls InGaN/GaN system research for many decades, until two major breakthroughs have been achieved:

- At 1989, Professor Isamu Akasaki shows a breakthrough on Mg-doped GaN sample to solve the p-type doping dilemma by electron-beam to annealing, and he demonstrated the true p–n conducting material [11, 12].
- At 1995, Professor Shuji Nakamura demonstrates the first high power blue LED with an efficiency exceeding 5% [14–16].

These two great achievements are widely credited with re-igniting the III–V nitride system. In the following paragraph, we are going to discuss the key aspects on the blue LED technology, including:

- Key LED chip manufacturing principles: Including MOCVD principle/equipment and buffer layer design.
- Key LED technology: Including the epitaxy process and chip forming technologies.

2.2.4 Epitaxy Growth: MOCVD Equipment

Combining the merit of the capability of volume production as well as adequately precise growth control, MOCVD system (as shown in Fig. 2.6) dominates almost all the field of commercial III–V compound epitaxy. MOCVE applies metal-organic compounds such as trimethyl gallium (TMGa) or trimethyl aluminum (TMAl) as precursors for the material in thin films. The precursors are transported via a carrier gas to a heated zone within a growth chamber. Thin films are produced when the precursors react or dissociate with another compound. The optical and electrical property of the resulting LED is directly related to the composition of the deposited materials and doping within the epilayers with specific elemental materials.

Theoretically, MOCVD is a nonequilibrium growth technique that relies on vapor transport of the precursors and subsequent reactions of Group III alkyls and Group V hydrides in a heated zone. The basic MOCVD reaction describing the GaN deposition process is:

$$\mathrm{Ga(CH_3)_{3(V)}} + \mathrm{NH_{3(V)}} \rightarrow \mathrm{GaN_{(S)}} + 3\mathrm{CH_{4(V)}}. \tag{2.1}$$

However, the detail of the reaction is not fully understood, and the intermediate reactions are much complex. Further research is needed to understand the fundamentals of this crystal growth process.

Various researchers employ both atmospheric-pressure and low-pressure MOCVD reactors in the growth of GaN. In Japan, the majority utilizes atmospheric pressure reactors because of the high partial pressures of ammonia; on the contrary, the low-pressure system occupies an overwhelming portion in the other countries.

MOCVD reactor designs for GaN growth must overcome problems presented by high growth temperatures, pre-reactions, flows, and film nonuniformity. Typically, very high temperature level is required during the GaN growth, because of the high bond-strength of the N–H bond in ammonia precursors. Hence, the thermodynamic ammonia will be pre-reacted with Group III metalorganic compounds in order to form nonvolatile adducts. These contribute to the current challenges for researchers to design and scale-up of III–V nitride deposition systems. Much research activity is needed in the scale-up and understanding of the mechanism of gallium nitride growth by MOCVD.

2.2.5 Epitaxy Growth: Buffer Layer

Due to that there is no high-quality and low-cost GaN bulk single crystal, all technological development of GaN-based devices relies on heteroepitaxy. There are two main substrates commercially available for GaN film growth, 6H–SiC and sapphire. Because of intellectual property (IP) limitation (IP of growing-semiconductor-device-on-SiC is exclusive licensed to Cree by NCSU), most of LED chip companies adopt c-sapphire (0 0 0 1) as growing template.

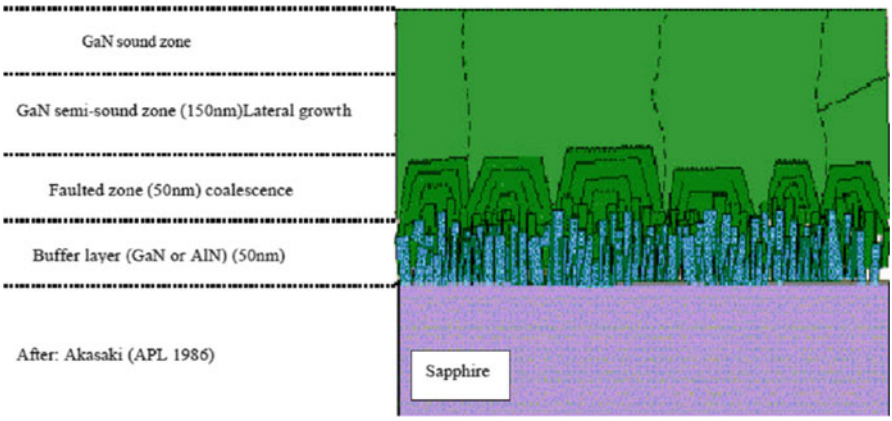


Fig. 2.7 The final structure of buffer layer

The crystallography of the c-sapphire surface is complex and can be terminated by different chemistries. Annealing this surface in flowing H_2 within the deposition system between 1,000 and 1,100°C is a commonly employed cleaning procedure to form a relatively stable Al-terminated surface prior to grow the buffer layer.

Due to that sapphire and GaN have different lattice constant, a special growth technique termed multistep pre-growth processes has been developed to overcome the lattice mismatch and to obtain better process quality. Multistep pre-growth processes involve either sapphire pretreatments or using buffer layers. Major process breakthroughs, e.g., two-step AlN treatment by Prof. Akasaki [13] and low temperature GaN (LT-GaN) by Prof. Nakamura (Fig. 2.7), has been achieved to provide a good nucleation surface and thus solved many problems in hetero-epitaxial MOCVD growth on sapphire.

In more detail on AlN buffer layer process: the sapphire is annealed under flowing NH_3 at temperature larger than 800°C. Nitrogen-containing species from the decomposed NH_3 react with Al atoms on the substrate to form a very thin AlN layer which lowers the lattice mismatch with subsequently grown Ill-nitride films relative to that with sapphire and modifies the surface energy of the substrate.

Nakamura adopted the same idea but not AlN. By atmospheric-pressure MOCVD, he obtained the same beneficial effects of an AlN buffer layer by using GaN low-temperature layer, which starts with a low temperature thin GaN deposition, followed by a high temperature growth to complete the GaN buffer.

2.2.6 Start-of-the-Art of Blue LED Process (1): Epitaxy

Before growing the LED structure, normally 2–6 μm undoped GaN (u-GaN) are deposited, prior to n-type GaN at the temperature around 1,000°C. The purpose of

u-GaN is mainly to reduce the threading dislocation propagating from buffer layer in favor of bettering the quality of LED structure.

On top of the u-GaN, we grow n-type GaN, active layer, and p-type GaN, respectively:

– n-type GaN: Doping silicon is the most popular way to form n-type GaN. Moreover, most process will grow a pre-strain layer before active layer to pre-compensate the strain between n-type GaN and active layer. The growing temperature of n-type GaN is typically equal or slightly higher than that of u-GaN.
– Active layer: The choice for active layer used to be double heterojunction (DH) structure. Because of improvement of efficiency, precise wavelength control and narrower full width at half maximum (FWHM) in wavelength, multi-quantum well (MQW) structure seems to be a widely acceptable choice over the world. The growing temperature of InGaN/GaN MQW must be lower enough in order to successfully introduce indium into the film to emit the desired wavelength.
– p-Type GaN: A long-standing problem was the failure to achieve p-type doping in GaN materials. So far, magnesium is only dopant that is capable of producing p-type GaN. Before 1993, it was very difficult to obtain p-type GaN. Prof. Akasaki showed that a solution existed: He discovered that the low-level electron beam irradiation in an electron microscope could form p-type GaN. However, it was Nakamura who fully solved the problem of p-type doping: He found that all previous GaN researchers had annealed their samples in ammonia (NH_3). Ammonia dissociates above ~500°C, releasing atomic hydrogen, which passivates the acceptors. Therefore, Nakamura switched to annealing in a clean nitrogen (N_2) atmosphere and thereby invented a reliable method to achieve high-quality p-type GaN materials.

Due to a lattice mismatch between the InGaN well layer and the GaN barrier layer of MQWs, a polarization field in the active region, causes inadequate confinement of electrons in the active region, which causes electron overflow to the p-type region and results in an efficiency droop. Growing the electron blocking layer (EBL) between p-type and MQWs is a proven method to improve the efficiency of LEDs, by effectively confining electrons in the MQW region.

The following chart in Fig. 2.8 is the typical flow of LED epitaxy process.

2.2.7 Start-of-the-Art of Blue LED Process (2): Chip Forming

After GaN epitaxy, the following GaN LED process is relatively straightforward, including frontend (mesa forming, TCL, Pad forming, and passivation) and backend (grinding, dicing, and binning) chip forming process:

- Frontend process:
  - Mesa forming: Because sapphire substrate is nonconductive, we have to define the mesa area in order to expose n-type GaN.

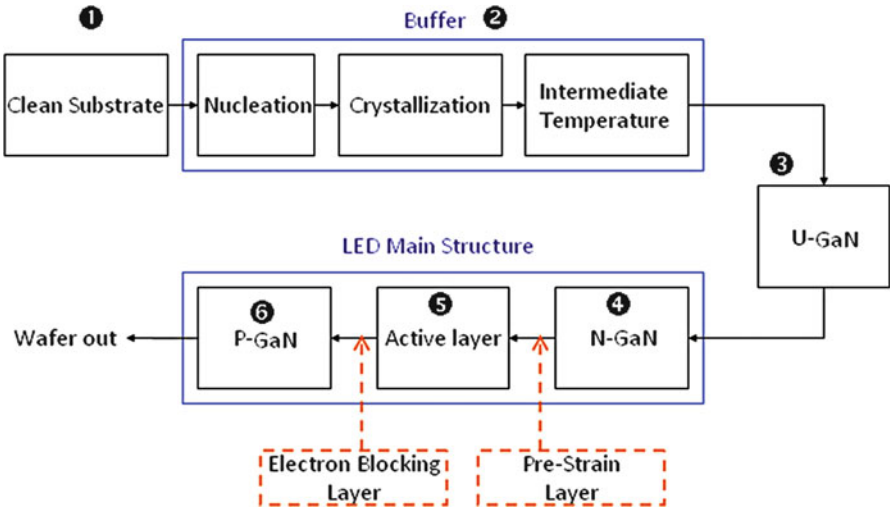


Fig. 2.8 Major epitaxy process flow of blue LED

- Transparent conductive layer (TCL) forming: Normally indium-tin-oxide (ITO) is deposited onto p-type GaN by E-gun or sputtering. Since the hole mobility of p-type GaN nowadays is still a issue, as a result, the use of TCL is to improve the current spreading [17] and thus electroluminescence.
- Pad forming: For providing the current path, properly-chosen metals are deposited onto p- and n-type GaN as p- and n-Pad. The selection rule for metals is that it has to make p- and n-contact be ohmic, to be oxidize free and to be able to well bond with the external connecting wires.
- Passivation: For better reliability, passivation, such as SiO_2 or SiN_x, are deposited to prevent LED from the moisture.
  The frontend process is the illustration of the paragraph above as Fig. 2.9.

- Backend process: The main purpose of the back end of the line (BEOL) is to separate LED chips into individual ones.
  - Grinding: The original sapphire substrate is too thick to scribe; therefore, we have ground the wafer first.
  - Dicing: Scribe-and-break is a prevalent method for individualizing the burgeoning GaN LEDs by virtue of high throughput, low cost, ease of use, process tolerance, and high yields. The wafer is experiencing melting and ablation so as to create thermal crack that is precursor to the following breaking process. Commercially, it is either front-scribe-and-back-break or back-scribe-and-front-break, depending on the process design.
  - Binning and sorting: Statistically, most of the process variations behave the normal distribution, so do the final products. In order to make good-quality commitment to the customers, it is imperative to separate bad ones from good

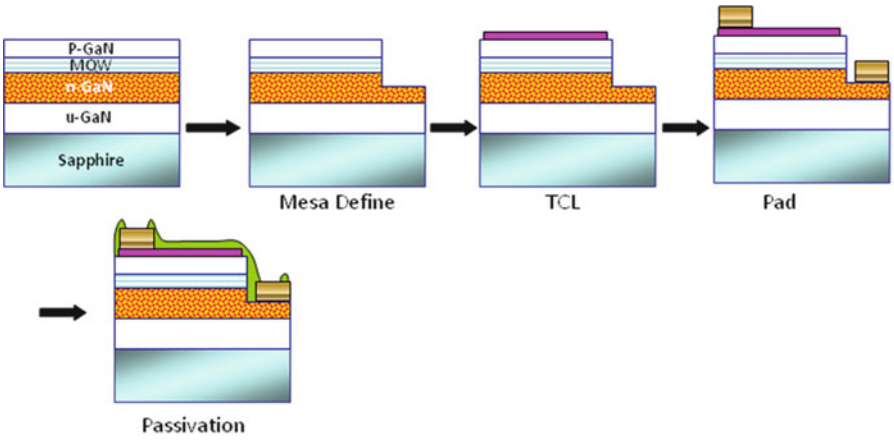


Fig. 2.9 Schematic diagram of blue LED chip process

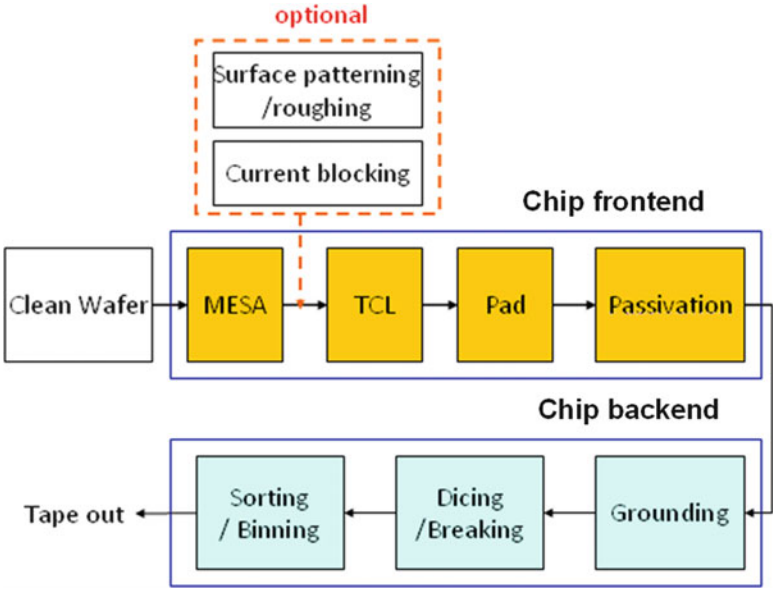


Fig. 2.10 The typical flow of complete LED chip process

ones! And, why binning? It is not only for us to make corresponding price by the grade of the products, but also it is easier for customers to use due to the small variation of the-same-bin product.

The total frontend/backend process is summarized in Fig. 2.10.

2.3 Level 1: LED Packaging

2.3.1 Overview

LED packaging is responsible for the electrical connection, mechanical protection/integrity and heat dissipation of LED chip. Depend upon the LED chip specification and application field, the design concept/structure of the LED packaging varies. In the following paragraph, the concept of the conventional LED packaging, high-brightness LED packaging, and wafer-level chip integration technology will be described.

2.3.2 Conventional LED Packaging

A conventional LED package includes electrical lead, wire, die attach and encapsulant. The most divergence of LED package and IC package is should consider the light extraction from LED package. The LED chip is surrounded by transparent encapsulant and electrical connection via the wire. The LED chip in the conventional package is operating beyond 120 mA (or called low-power chip) and usually using the surface mount technology. There are many types in conventional packing and mostly known as "5 mm lamp" or "SMD5630" as shown in Fig. 2.11. In convention package, it has two different surface shapes, one is hemisphere and the other is planar-surface. The light through the hemisphere is like the Lambertian surface and planar-surface has wider far field angle than hemisphere shape. It has



Fig. 2.11 The different types of LED package

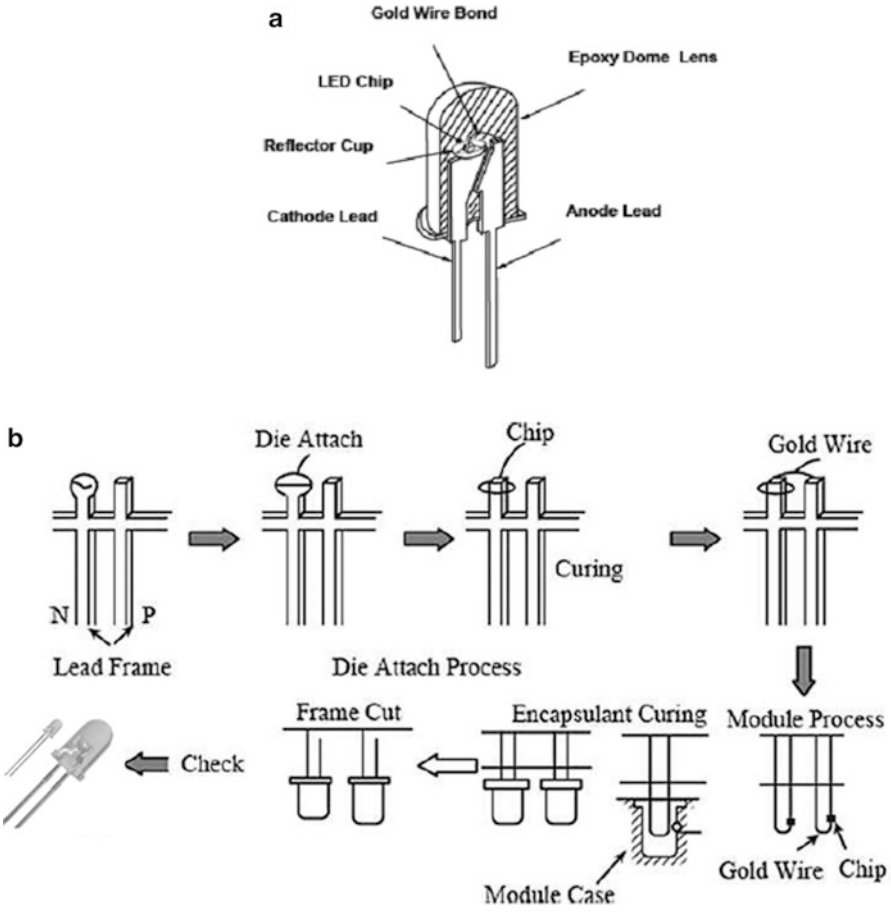


Fig. 2.12 The (**a**) structure and (**b**) packaging process flow of conventional LED packaging

highly reflective metal (like silver) deposit on the contact surface which between chip bottom surface and package top surface. Functions of encapsulant are not only providing protection against humidity and chemicals damage but play the role of a lens in the package.

The process of the conventional LED packaging includes die bonding, interconnect forming, encapsulation/phosphor curing and frame cutting, as illustrated in Fig. 2.12. A pre-reformed leadframe, which comprised of multiple N/P legs are provided, and the LED chip are mounted on to one leg. Interconnect, e.g., gold wire and aluminum wire is applied to connect chip to two legs. Following, the leadframe are sent to the encapsulation process to form the dorm shape transparent protection polymer.

These low-power LEDs are widely used in the application of indicators, signals, backlighting, with the price in the range of 0.1–0.2 $/part.

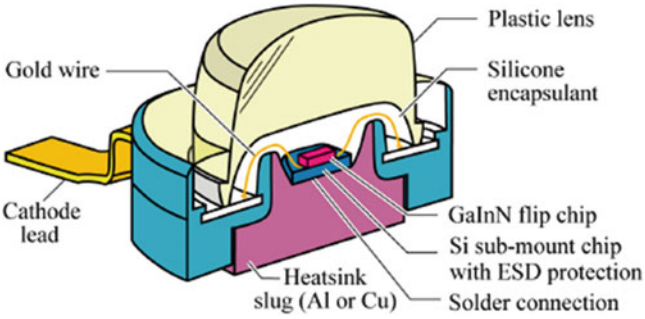


Fig. 2.13 Schematic diagram of high power LED packaging

2.3.3 High Brightness LED Packaging

High brightness LED (HB-LED) packaging, or called high power LED packaging, use operation current of more than 350 mA and generate more than 130 lu/W light output. High current/power usually induces higher temperature at the LED chip, and the LED light efficiency will dramatically decrease when the LED temperature increase. Hence, the thermal dissipation is much severer than the conventional LED packaging, where new packaging concept is needed.

HB-LED packaging will apply advanced thermal management solution for heat dissipation. Refer to Fig. 2.13 as an example, the chip is first mounted on Si-based submount and large heat sink (slug), and connected to one side of the die with an Au/Al wire bond. The other can be connected to the lead with another wire bond, or directly through the bottom of the die through the die attachment. After wire bonding interconnection, the chip is encapsulated with silicone. In a white LED, the phosphor material is suspended in the silicon. Finally, the entire component is molded into an epoxy casing that provides directionality to the light and further protection to the die and leads.

The process flow of HB-LED can be shown in Fig. 2.14.

- Dicing: A two-steps dicing technology is widely used in the LED packaging manufacturing, including:
  - The GaN scribing step must be carried out with high precision. To have good performance, the diodes must have very straight and smooth edges. This step can be done by laser or diamond techniques.
  - The cutting of the substrate requires less precision and aims to separate the diodes. Diamond saws as well as scribe (by diamond or laser) and break techniques are normally used.
- Die bonding
  - Good precision of the die bonding will ensure the optical center of the LED packaging.

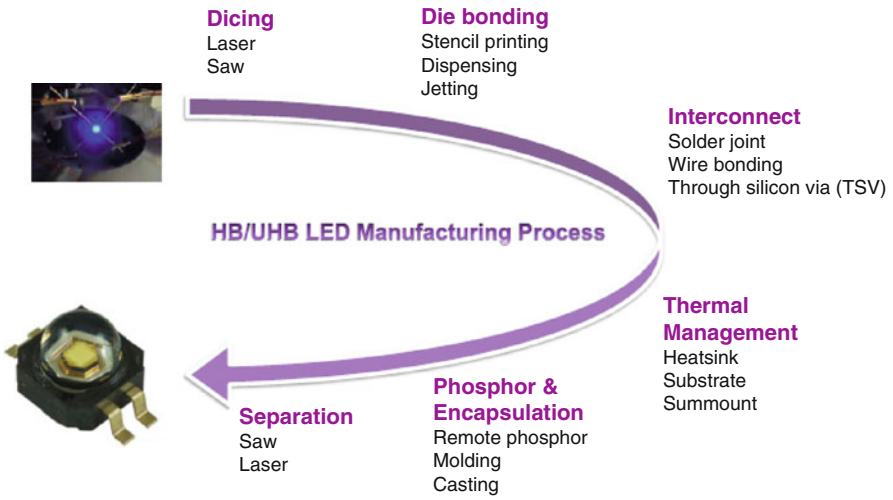


Fig. 2.14 Packaging process flow of HB-LED packaging

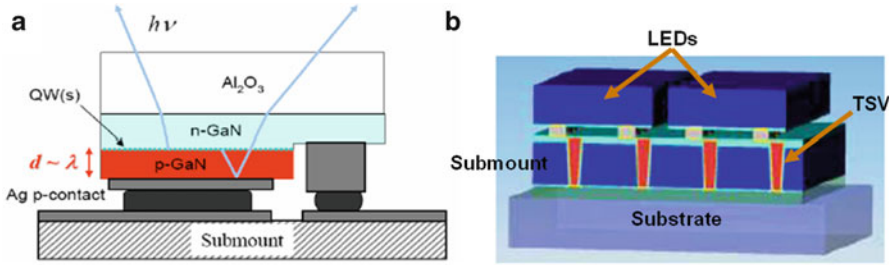


Fig. 2.15 Advanced interconnect technology for HB-LED: (**a**) flip chip and (**b**) TSV

- Good uniformity of die bonding process determines the thermal performance of the HB-LED packaging.
- Currently, conductive polymer and solder paste is widely used.

- Interconnect: The HB-LED interconnect is subject to high current, and the reliable interconnect technology is required.
  - Wire bonding: Traditional Au/Al wire bonding technology is also applied for HB-LED, with the guarantee of high/stable current flow. New wire bonding technology, such as ribbon wire bonding, is developing.
  - Flip chip: As illustrated in Fig. 2.15a, the LED based on the transparent sapphire can be flip-chiped [18] by the solder-based interconnect.
  - Through silicon via (TSV): Forming the TSV in the silicon submount, and mount the LED chip onto it. High thermal conductivity of silicon material (submount) is expected to improve the packaging thermal performance, as illustrated in Fig. 2.15b.

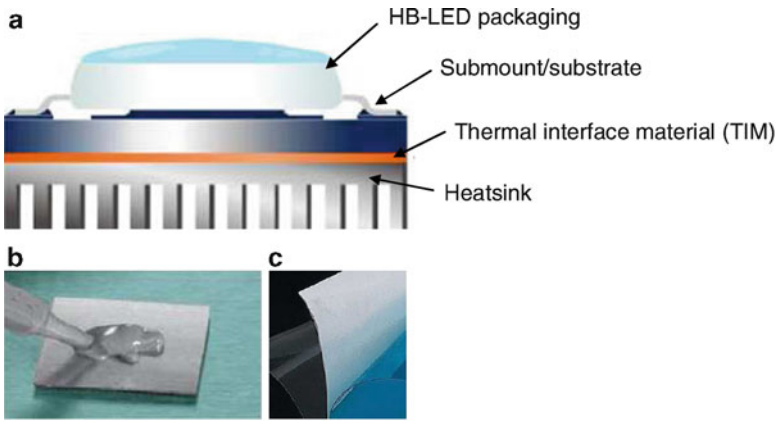


Fig. 2.16 Thermal interface material: (**a**) illustration of the TIM, (**b**) thermal grease, and (**c**) thermal film

- Thermal management: There are several aspects to further improve the thermal performance of HB-LED packaging:
  - Submount and substrate: Thermal substrate materials (e.g., metal core PCB) provide primary heat spreading, heat transfer to the heat sink, electrical connection to the driver, and mechanical mounting. Thermal enhanced materials, such as metal core PCB (MCPCB), ceramic substrate, and TSV for thermal dissipation, are used.
  - Thermal interface material (TIM): Thermal interface materials (e.g., film or thermal grease) improve heat dissipation and electrical isolation [19], as illustrated in Fig. 2.16b.
  - Heat sink: Heat sinks dissipate heat to the ambient environment.
- Phosphor, encapsulation and lens
  - Phosphor is widely used for the white lighting generation from blue LED. YAG:Ce^{2+} and YAG:Eu^{2+} are the mostly used material.
  - Silicon-based encapsulation and lens are widely applied, due to high thermal resistance, photo-thermal stability, less degradation.

2.3.4 Wafer-Level Chip Integration (WLCI) Technology

In contrast with conventional wire bonding packaging, a new wafer-level process has been developed so that it is able to electrically connect each chip without applying wire bonding. Borrowing the concept from IC/packaging industry [10, 20–21], a process called "Wafer Level Chip Integration (WLCI)" technology has been developed to construct hybrid integration of various chips on a substrate.

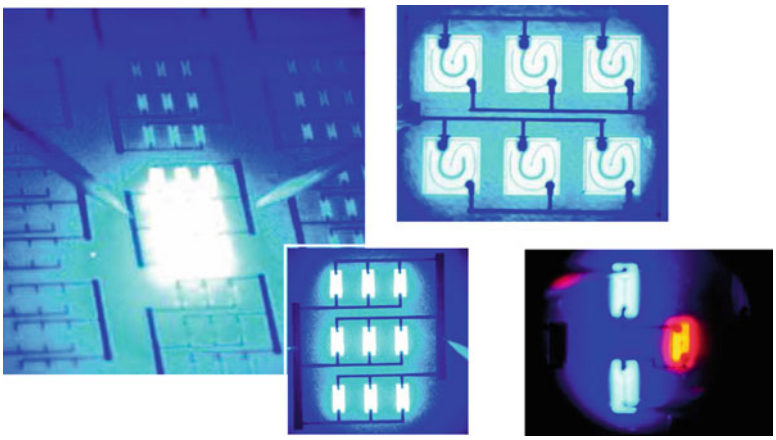


Fig. 2.17 Picture of various multiple chip integration by WLCI technology (Epistar provide)

The chip process of WLCI technology is based on the normal LED chip process with three extra steps:

(a) The LED chips are placed on a substrate. There is not much restriction on the arrangement rule except for the placement accuracy. The accuracy is to be controlled to a degree of 15 μm or less to improve the process yield. Chips used in this platform can be a combination of electronics and optics chips with variety of functions.
(b) The empty space between LED chips is filled with filling material to provide a smooth surface for the following metal interconnection. The filling material is supposed to be transparent in the range of emission spectrum of the designated LED chips for not reducing the light output.
(c) The predetermined electrical connections between chips are through photolithography and thin-film deposition instead of wires. With this technology, it becomes possible to do heterogeneous chip interconnection in wafer form.

Figure 2.17 shows three examples of combining multiple chips to achieve different application by WLCI technology.

2.4 Level 2: Multi-LED Assembles

The LED packages has a relatively small dimension (roughly $4 \times 5\text{mm}^2$ to $10 \times 10\,\text{mm}^2$), which shows a gap towards the lighting application, such as retrofit bulb and luminaire. A transfer layer, multi-LED assembles, is presented to fulfill such gap and enhance the thermal performance of SSL application (Fig. 2.18). In this section, mechanical consideration of the multi-LED assembles and the white light generation will be described.

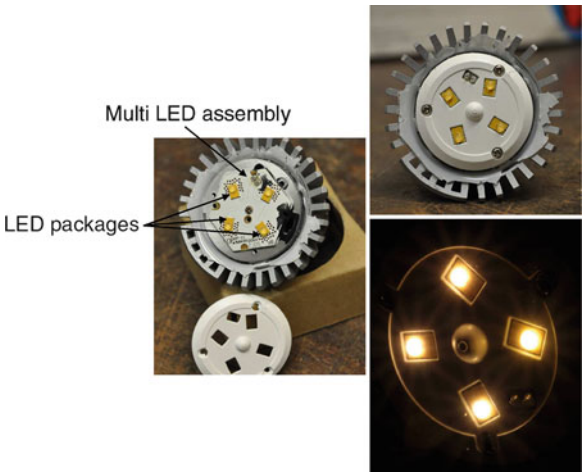


Fig. 2.18 Multi-LED assembly in the retrofit application (Source: Philips)

2.4.1 Mechanical Considerations

The LED packages are assembled onto the large PCB by the solder or epoxy glue/adhesive. The bonding process can be achieved by the solder reflow or epoxy curing.

However, these bonding processes cause sever luminaire reliability risk. Take solder bonding as an example, the LED packages can stand the lead-free solder SnAgCu melding temperature of roughly 220°C. But in reality, the maximum reflow temperature of 40–50°C above the melting temperature. High reflow temperature will induce the LED packaging epoxy degradation and/or delamination initialization/propagation. On the other hand, due to the high coefficient of thermal expansion (CTE) mismatch between the PCB and LED packages, the reliability of such solder/adhesive will dominate the overall luminaire reliability.

In order to reduce costs for LEDs, a logical step is to integrate multi-LEDs onto PCB directly, and skip the LED package level as much as possible. Then different processing steps can be omitted and less (expensive) material will be used. Using multiple LED dies per product will increase the lumen output per product. However, it will pose other challenges to the system. The two most important ones are (1) proper thermal management to get rid of all the heat and (2) directing/shaping the light spot (Fig. 2.19).

2.4.2 White Light LED

Challenges of white light emitting by LED technology are presented, because only a particular wave length of light can be generated by single LED. To emit white light with acceptable CRI, the LED manufacturer commonly uses three approaches: wavelength conversion, color mixing, and homoepitaxial ZnSe:

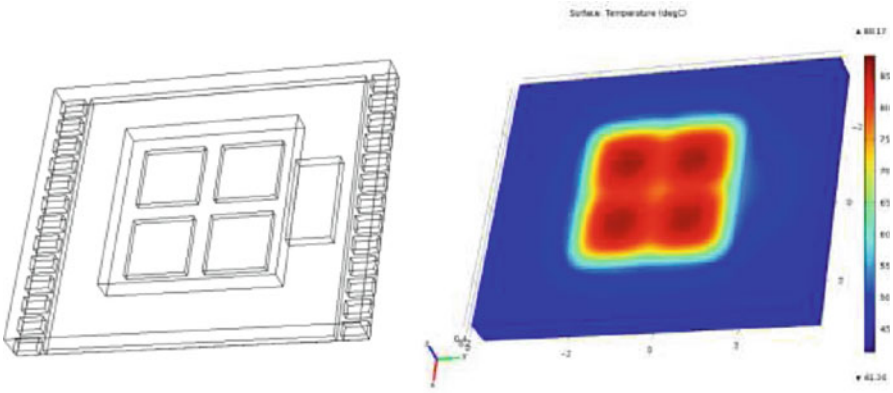


Fig. 2.19 Concept of a four die LED with integrated driver package (*left*), and thermal simulation result (*right*)

1. Wavelength conversion: It involves converting all or a part of LED's emission into visible wavelengths that are perceived as white light:
   (a) Blue LED and YAG-based phosphor: The YAG-based phosphor is excited by the blue LED, and results in the appearance of white light. This method is most widely applied in the SSL industry, due to the most efficient and low cost. However, the material of yellow phosphor usually contains of rare earth, and the material scarcity concern maintains and substitution possibility is exploring.
   (b) Ultraviolet LED with RGB phosphor: Similar to previous application, the light from ultraviolet LED is completely converted by the RGB phosphor.
   (c) Blue LED and quantum dots: Quantum dots (QDs) are extremely small semiconductors crystals (between 2 and 10 nm). These quantum dots are 33 or 34 pairs of cadmium or selenium on top of the LED. Hence the quantum dots are excited by the LED and generated the white light. The excited wavelength from the QDs depends upon the particle size [22, 23].
   (d) Color mixing: Another method is to mix fundamental light sources and generate the white light. Color mixing can be implemented by two LEDs (blue and yellow), three LEDs (blue, green, and red), or four LEDs (red, blue, green, and yellow). Because of no phosphor, there is no loss of energy during the conversion process; as a result, color mixing is more efficient than wavelength conversion.
2. Homoepitaxial ZnSe: The blue LED is placed on to a homoepitaxial ZnSe, and the blue light is generated by the blue LED and yellow light from the ZnSe substrate. From the literature [24], this technology can generate white light with color temperature of 3,400 K and CRI of 68 (Fig. 2.20).

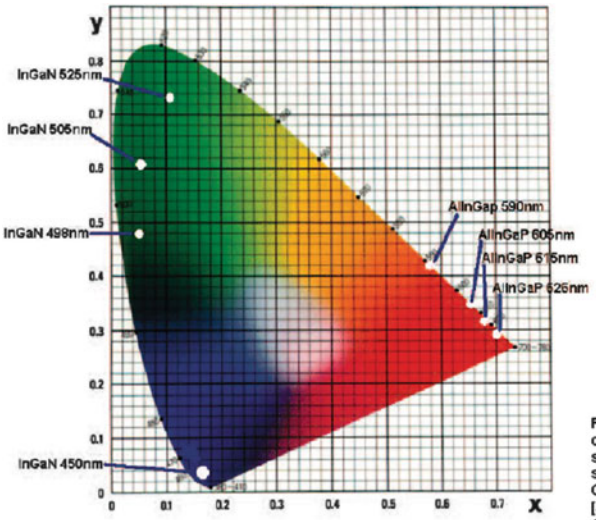


Figure 5. Chromaticity coordinates of typical single-wavelength LEDs shown on a standard CIE chromaticity diagram [adapted from *Schubert and Miller*, 1999].

Fig. 2.20 Color mixing for white LED

2.5 Level 3: LED Modules

LED requires constant current with DC power. The SSL electronic driver is used for converting AC power into DC, or from one DC level into higher/lower DC. These LED electronics are expected to maintain the constant current and control of LED, performing several of electrical protection to LED, such as overvoltage, overload, and over-temperature shutdown. On top of the level 2: multi-LED assembles, the electronics of SSL is presented and integrated.

Conventional SSL devices include three major parts: optical part, LED electrical driver, and interconnections between the latter two parts (Fig. 2.21). In each SSL system all these three parts exists, and they are necessary to make the system functional, however, with respect to the application they can be simpler or more complex. The electrical driver of SSL system prepares the required power for driving optical part. The primary and fundamental task of the SSL driver is to provide electrical power requirements for optical part of the system. There are lots of other functionalities can be defined and implemented in SSL driver. Dimming and color-changing capabilities are two examples of SSL system extra functionalities which already can be found in commercial products. Various driver architecture is applied for different applications, such as Buck (for output voltage is smaller than input one), Boost (for output voltage is smaller than input one), flyback, and transformer-isolated converters (for main to LED lamp application).

Smart SSL—able to sense, describe the environment, and help to decide—will contribute to more than 70% of lighting energy saving. However, less components/

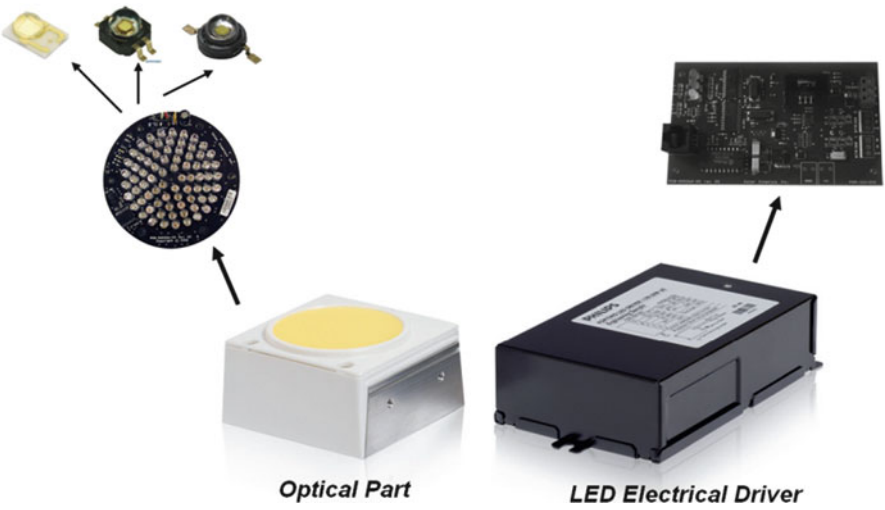


Fig. 2.21 Different parts of a general SSL system. Optical part is the light source of the system and includes LEDs. LED electrical driver (SSL driver) is the interface of the SSL optical part and the input power of the system. SSL driver also can be more than just a power converter and includes the controller and memory. These two parts of the system are interconnected to each other (Source: Philips Lighting)

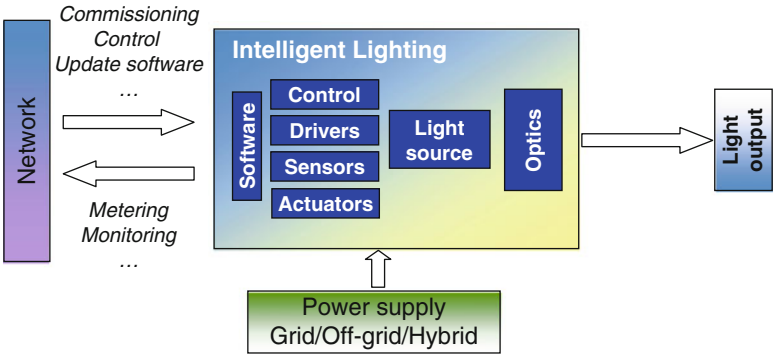


Fig. 2.22 Illustration of intelligent lighting architecture

systems integration results in a high price, large size, and less market acceptance of SSL products and in a nonoptimal energy-saving solution. As SSL is digital in nature, it has inherited excellent advantages to combine the lighting function with other functions (sensing, communication, control, etc.) to create smart and multi-function systems. Figure 2.22 shows the architecture of future SSL concept, where the controller/driver, sensor, communication units are presented.

2.6 Level 4: Luminaires

As the development of the SSL technology, two types of luminaires are developed to accelerate the market acceptance:

1. Retrofit bulb/lamps
   Following the conventional usage of the light bulb, SSL industries create the LED base light bulb to replace the conventional incandescent and fluorescent light bulbs to enhance the market penetration of the LED technology. Figure 2.23 shows an example of retrofit bulb, which has the same fixture design as conventional light bulb and customers can direct replace their bulb without changing the fixture or the luminaire.
2. Beyond retrofit
   The lifetime of the LED chip is expected to be more than 50,000 h, which is close to the luminaire. Further cost reduction concepts of directly integrating the LEDs into luminaires are presented by the beyond retrofit luminaires. Figure 2.24 shows a low-cost consumer luminaire, where the LED and driver electronics are integrated.

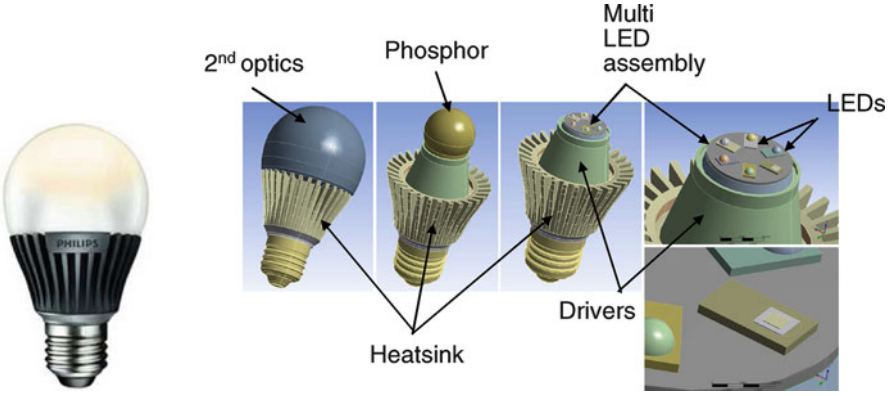


Fig. 2.23 An example of retrofit bulb (Source: Philips and European CSSL project)

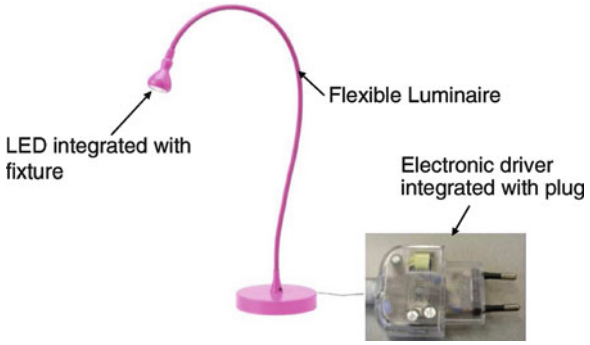


Fig. 2.24 Beyond retrofit: SSL consumer luminaire (Source: IKEA)

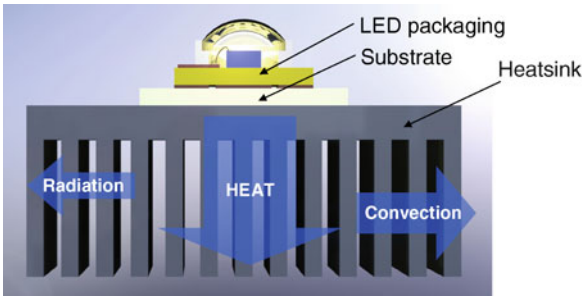


Fig. 2.25 Schematic diagram of thermal path of LEDs

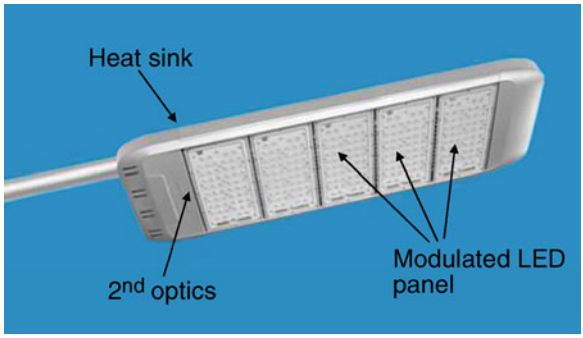


Fig. 2.26 Beyond retrofit: Street light (Source: Lampearl)

High power LED now is used from 500 mW to as much as 10 W in a single package and it is expected to apply even more power in the future. The chip heat fluxes are expected to be in excess of 70 W/cm^2 by the end of this decade, and about 100 W/cm^2 by 2018 [25], which has very high intensity of power. The application of conventional thermal packaging technology results in poor thermal performance to such chip designed LEDs with high temperature hot spot. Advanced thermal materials and novel thermal solutions which are already successfully applied on microelectronic packages have high potential to be used on LED module (Fig. 2.25).

The thermal management is one of the design key issues of luminaire, especially for the high power SSL application. Figure 2.26 shows an example of LED-based street lighting, where the heat sink is located at the opposite side of LED, and the heat sink covers almost all illumination area [26].

The design of the SSL luminaire is alike a designing of the mini compact system. Figure 2.27 demonstrated a luminaire design, where the key functional elements, such as LED, thermal management, optics, controller and driver. As increasing the SSL functionalities, the design challenge of the SSL luminaire is expected.

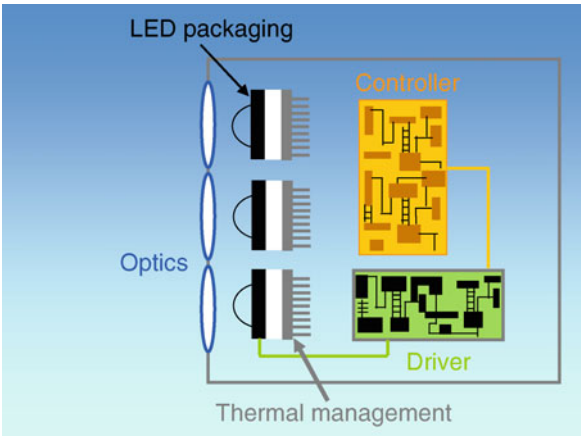


Fig. 2.27 Functional architecture of SSL luminaire

2.7 Level 5: Lighting Systems

Lighting systems is a complex system, which is a system composed of interconnected parts that as a whole exhibit one or more properties (behavior among the possible properties) not obvious from the properties of the individual parts. Lighting system comprises of multiple luminaires and/or types of luminaire, smart sensors, communication, control scheme, and data mining and data management. Examples, such as street lighting, building lighting, city lighting, are given (Fig. 2.28).

Various challenges of complex lighting system are foreseen:

(a) The interactions: Between different disciplines (software, electronics, optics, mechanics, and thermal) and component/subsystem (sensors, communication, ventilation, heating, and air-conditioner).
(b) Long lifetime: Lighting system is expected to be much longer than the components. A building is expected to be 50 years and a bridge is about more than 100 year. The corresponding lighting system will be expected to be functional as long as the objects stand. However, the advanced lighting system should be able to adapt by itself for the different user requirement and component/subsystem replacement.
(c) Complex supplier ownership: Due to the size of the large system, it will be too difficult for a single supplier to cover all components. Hence, it is a scientific/engineering challenge to communication with each supplier at different levels, where a feasible standard is required.
(d) Easy to maintenance.

In summary, a sustainable lighting system lifecycle is proposed in Fig. 2.29.



Fig. 2.28 SSL lighting systems: (**a**) Netherlands Pavilion at 2010 Shanghai world expo, (**b**) Guangdong Olympic Sports Center (Source: Lampearl)

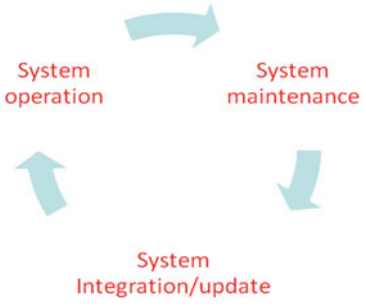


Fig. 2.29 Sustainable lighting system

References

1. LED (2005) The American heritage science dictionary. Houghton Mifflin Company. Via http://dictionary.reference.com/browse/led and http://www.thefreedictionary.com/LED. Accessed 22nd Jun 2011
2. Zhang GQ (2010) Shaping the new technology landscape of lighting. In: Proceedings of green lighting forum, Shanghai, China, Apr 2010
3. Zukauskas A, Shur MS, Gaska R (2002) Introduction to solid-state lighting. J. Wiley, New York, NY
4. Streubel K, Linder N, Wirth R, Jaeger A (2002) High brightness AlGaInP light-emitting diodes. IEEE J Select Top Quant Electron 8(2):321–332
5. Kish F, Fletcher R (1997) AlGaInP light-emitting diodes. In: Stringfellow GB, Craford MG (eds) Semiconductors and semi-metals, high brightness light emitting diodes, vol 48. Academic Press, San Diego, CA, pp 149–220
6. Morrison AP, Lambkin JD, Poel CJ, Valster A (2000) Electron transport across bulk (AlGa) InP barriers determined from the *I–V* characteristics of n-i-n diodes measured between 60 and 310 K. IEEE J Quant Electron 36:1293–1298
7. Pliskin WA, Gdula RA, Materials, S.P. Keller, T.S. Moss (1981) Properties and Preparation Handbook on Semiconductors, Vol 3. North Holland Publishing Co, Amsterdam
8. Pursiainen O, Linder N, Jaeger A, Oberschmid R, Streubel K (2001) Identification of aging mechanisms in the optical and electrical characteristics of light-emitting diodes. Appl Phys Lett 79:2895–2897
9. Chang SJ, Chang CS, Su YK, Chang PT, Wu YR, Huang KH, Chen TP (1997) Chirped GaAs-AlAs distributed Bragg reflectors for high brightness yellow-green light-emitting diodes. IEEE Photonics Technol Lett 9(2):182–184
10. Horng RH, Wuu DS, Wei SC, Tseng CY, Huang MF, Chang KH, Liu PH, Lin KC (1999) AlGaInP light-emitting diodes with mirror substrates fabricated by wafer bonding. Appl Phys Lett 75:3054–3057
11. Sugawara H, Itaya K, Hatakoshi G (2009) Characteristics of a distributed Bragg reflector for the visible-light spectral region using InGaAlP and GaAs: comparison of transparent- and loss-type structures. J Appl Phys 74(5):3189–3193
12. Amano H, Kito M, Hiramatsu K, Akasaki I (1989) P-type conduction in Mg-doped GaN treated with low-energy electron beam irradiation (LEEBI). Jpn J Appl Phys 28:L2112–L2114
13. Akasaki I, Amano H, Koide Y, Hiramatsu K, Sawaki N (1989) Effects of ain buffer layer on crystallographic structure and on electrical and optical properties of GaN and Ga1–xAlxN ($0 < x$ 0.4) films grown on sapphire substrate by MOVPE. J Cryst Growth 98(1–2):209–219
14. Nakamura S, Senoh M, Iwasa N, Nagahama S (1995) High-brightness InGaN blue, green and yellow lighting-emitting diodes with quantum well structures. Jpn J Appl Phys 34(7A): L797–L799
15. Nakamura S, Senoh M, Iwasa N, Nagahama S (1995) High-power InGaN single-quantum-well-structure blue and violet light-emitting diodes. Appl Phys Lett 67(13):114359–114362
16. Nakamura S, Fasol G (1997) The blue laser diode: GaN based light emitters and lasers. Springer, Berlin
17. Yamada M, Mitani T, Narukawa Y, Shioji S, Niki I, Sonobe S, Deguchi K, Sano M, Mukai T (2002) InGaN based near-ultraviolet and blue-light-emitting diodes with high external quantum efficiency using a patterned sapphire substrate and a Mesh Electrode. Jpn J Appl Phys 41: L1431–L1433
18. Krames MR, Shchekin OB, Mueller-Mach R, Mueller GO, Zhou L, Harbers G, Craford MG (2007) Status and future of high-power light-emitting diodes for solid-state lighting. J Display Technol 3(2):160–175
19. Zhang K, Xiao G, Wong CK, Gu H, Yuen M, Chan PCH, Xu B (2005) Study on thermal interface material with carbon nanotubes and carbon black in high-brightness LED packaging

with flip-chip. In: Proceedings of 55th electronic components and technology conference, Lake Buena Vista, FL, USA, pp 60–65
20. International Technology Roadmap for Semiconductors, 2009 edition and 2010 update, http://www.itrs.net/
21. Baron J (2010) 3D integration spurs momentum in embedded and fan-out wafer-level package technologies. 3D Packaging, issue 15, pp 1–4
22. Mićić OI, Cheong HM, Fu H, Zunger A, Sprague JR, Mascarenhas A, Nozik AJ (1997) Size-dependent spectroscopy of InP quantum dots. J Phys Chem B 101(25):4904–4912
23. Shipway AN, Katz E, Willner I (2000) Nanoparticles arrays on surface for electronic, optical, and sensor applications. Chem Phys Chem 1:18–52
24. Katayama K, Matsubara H, Nakanishi F, Nakamura T, Doi H, Saegusa A, Mitsui T, Matsuoka T, Irikura M, Takebe T, Nishine S, Shirakawa T (2000) ZnSe-based white LEDs. J Cryst Growth 214–125:1064–1070
25. Arik M, Weaver S (2004) Chip scale thermal management of high brightness LED pack-ages. In: Proceedings of 4th international conference on Solid State Lighitng, SPIE proceedings series, Bellingham, WA, vol 5530, pp 214–223
26. Arika M, Beckerb C, Weaverb S, Petroskic J (2004) Thermal management of LEDs: package to system, In: Proceedings of 3rd international conference on solid state lighting, Proc. of SPIE, Bellingham, WA, vol 5187, pp 64–75

Chapter 3
Failure Mechanisms and Reliability Issues in LEDs

M.G. Pecht and Moon-Hwan Chang

Abstract The construction of LEDs is somewhat similar to microelectronics, but there are unique functional requirements, materials, and interfaces in LEDs that make their failure modes and mechanisms different. This chapter presents a definite, comprehensive and up-to-date guide to industry and academic research on LED failure mechanisms and reliability. It will help readers focus resources in an effective manner to assess and improve LED reliability for various current and future applications. In this review, we focus on the reliability of LEDs at the die and package levels. The reliability information provided by the LED manufacturers is not at a mature enough stage to be useful for the users of LEDs. This chapter provides groundwork for understanding of the reliability issues of LEDs. First, we present introduction about LED reliability and Physics of Failure (PoF) approach. We then categorize LED failures into 13 different groups related to semiconductor, interconnect, and package reliability issues. We close by identifying relationship between failure causes and associated mechanisms, issues in thermal standardization on LED reliability, critical areas of investigation, and development in LED technology and reliability.

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3.1 Introduction

Light emitting diodes (LEDs) are a solid-state lighting source increasingly being used in display backlighting, communications, medical services, signage, and general illumination [1–6]. LEDs offer design flexibility, from zero-dimensional lighting (dot-scale lighting) to three-dimensional lighting (color dimming using combination of colors), with one-dimensional lighting (line-scale lighting) and two-dimensional lighting (local dimming, i.e., area-scale lighting) in between. LEDs have small exterior outline dimensions, often <10 mm $\times$ 10 mm. LEDs, when designed in properly, offer high energy efficiency that results in lower power consumption (energy saving) with low voltage (generally <4 V) and low current operation (usually <700 mA). LEDs can have longer life—up to 50,000 h—with better thermal management than conventional lighting sources (e.g., fluorescent lamps and incandescent lamps). LEDs provide higher performance, such as ultrahigh-speed response time (microsecond level on–off switching), a wider range of controllable color temperatures (4,500–12,000 K), a wider operating temperature range (-20 to 85°C), and no low-temperature startup problems. In addition, LEDs have better impact resistance compared to traditional lighting due to no glass tubes to break. LEDs are also eco-friendly products, with low UV radiation (higher safety) and no mercury. LEDs that have a single color are over ten times more efficient than incandescent lamps. White LEDs are more than twice as efficient as incandescent lamps [3].

LEDs range from a narrow spectral band emitting a single color light, such as red, yellow, green, and blue, to white, to a distribution of luminous intensity and various types and shapes depending on color mixing and package design. A recent trend of LEDs to produce white light involves using blue LEDs with phosphors. White light is a mixture of all visible wavelengths, as shown in Fig. 3.1. Along with the prominent blue color (peak wavelength range 455–490 nm), there are a lot of other wavelengths such as green (515–570 nm), yellow (570–600 nm), and red (625–720 nm) that constitute white light in Fig. 3.1. Every LED color is represented by unique x–y coordinates, as shown in Fig. 3.2. Red is on the far right, green is on the top left, and blue is on the bottom left. The CIE chromaticity coordinates of x, y, and z are a ratio of the red, green, and blue stimulation of light compared to the total amount of the red, green, and blue stimulation. By definition, the sum of the RGB values ($x + y + z$) is equal to 1. The white area of the chromaticity diagram can be expanded, and boundaries are added to create each color ranges. The color temperatures and the Planckian locus (black body curve) show how they relate to the chromaticity coordinates [7]. Color temperature of a white light is the temperature of an ideal Planckian black-body radiator that radiates light of comparable hue to that light source. Thus, the color temperature of a white light of thermal radiation from ideal black body radiator is defined as equal to its surface temperature in Kelvin. When the black body radiator is heated to high temperatures, the heated black body emits the color starting from red, orange, yellow, white, and to the bluish white. The Planckian locus starts out in the red, then moves through the orange and yellow, and

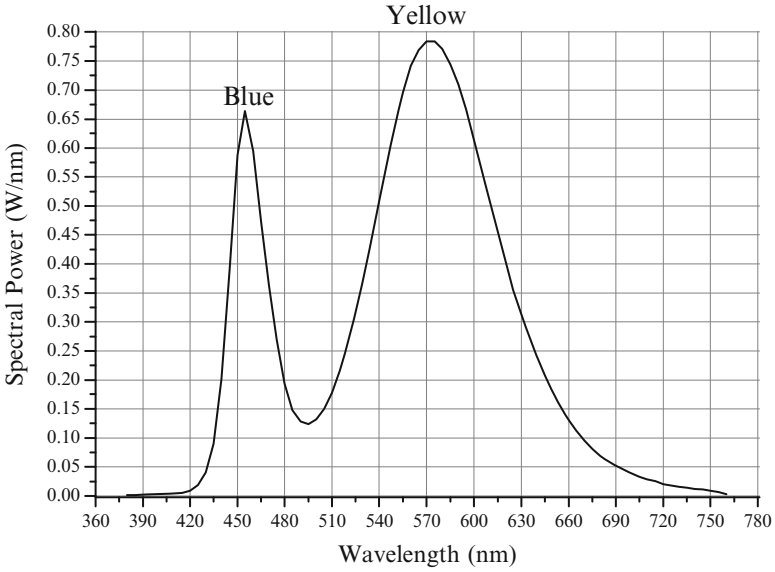


Fig. 3.1 Spectral power distribution—white LED

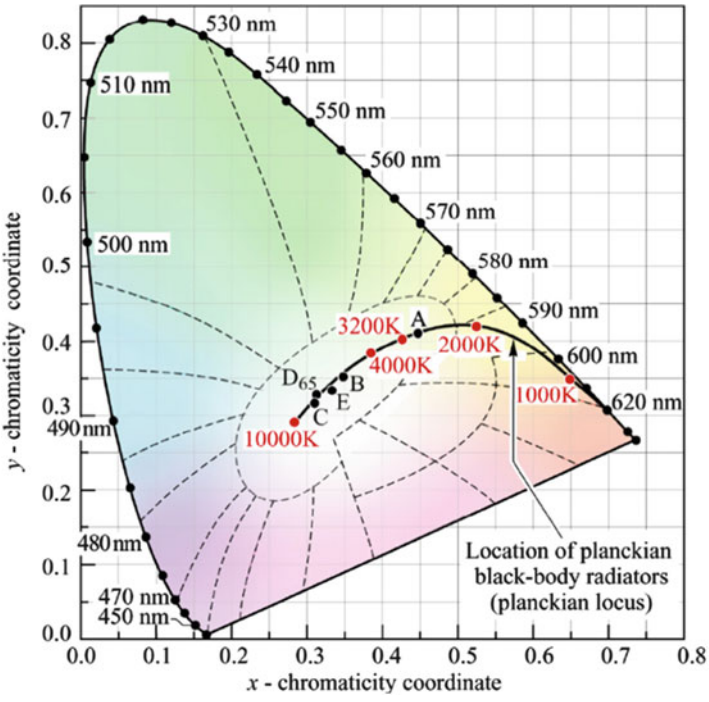


Fig. 3.2 CIE 1931 chromaticity diagram [8] (© Cambridge University Press), reprinted with permission

Table 3.1 Application areas of LEDs

Application area	Application examples
LCD backlight	Mobile phone Camera Portable media player (PMP) Notebook Monitor TV
Displays	Electric score boards Outdoor billboards Signage lighting
Transportation equipment lighting	Vehicle/train lighting Ship/airplane lighting
General lighting	Indoor lighting Outdoor lighting Special lighting

finally to the white region. The color temperature of light source is regarded as the temperature of a Planckian black-body radiator that has the same chromaticity coordinates. As the temperature of the black body increases, the chromaticity location moves from the red wavelength range toward the center of the diagram in Fig. 3.2.

In LED applications, color change should be considered because LED degradation not only results in reduced light output but also in color changes. LED modules are composed of many LEDs. This means that if some number of LEDs experience color changes, it will be recognized by users. Even though all LEDs degrade at the same rate LED modules need to maintain their initial color, especially for indoor lighting applications and backlight applications.

Due to their versatility, LED application areas include LCD backlights, displays, transportation equipment lighting, and general lighting, as shown in Table 3.1. LEDs are used as a light source for LCD backlights including mobile phone, camera, portable media player (PMP), notebook, monitor, and TV. Display areas include LED electric score boards, outdoor billboards, and signage lighting, such as LED strips and lighting bars. Examples of transportation equipment lighting areas are vehicle/train lighting (e.g., meter backlight, tail and brake lights) [9] and ship/airplane lighting (e.g., flight error lighting and searchlights). General lighting applications are divided into indoor lighting (e.g., LED lighting bulbs, desk lighting, and surface lighting) [10, 11], outdoor lighting (e.g., decorative lighting, street/bridge lighting, and stadium lighting), and special lighting (e.g., elevator lighting and appliance lighting) [12, 13]. The use of LEDs in general lighting has increased, initiating from street lighting at public areas and moving onto commercial/business lighting and consumer level.

The history of LED development can be divided into three generations with distinct advancements of new fabrication technology and equipment, new phosphor materials, and advancement of heat dissipation packaging technologies. LED has been being brighter and color variance has been being more flexible.

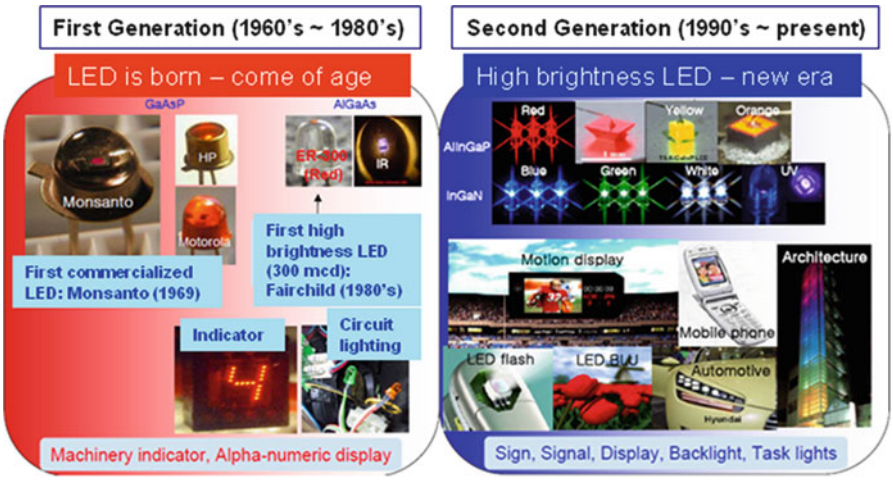


Fig. 3.3 LED development history (© Korea Photonics Technology Institute), reprinted with permission

And also light efficiency and light efficacy have been getting improved. The first commercialized LED was produced in the late 1960s. This first generation of LEDs lasted from the 1960s until the 1980s. In this period, major application areas were machinery status indicators and alpha-numeric displays shown in Fig. 3.3. The first commercially successful high-brightness LED (300 mcd) was developed by Fairchild Co. Ltd. in the 1980s. Candela (cd) unit is defined that a monochromatic light source emitting an optical power of 1/683 W at 555 nm into the solid angle of 1 steradian has a luminous intensity of 1 candela (cd). In the second generation, from the 1990s to the present, high-brightness LEDs became very popular in the world LED market. The main application areas for the second generation include motion displays, LED flashes, LED BLU, mobile phones, automotive LED lighting, and architecture.

The third generation is now arriving in the market. These LEDs have been developed for substantial savings in electrical energy consumption and reduction in environmental pollution. Future LED application areas are expected to include general lighting, lighting communication [14], medical/environmental fields, and critical applications in system controls. Some examples are portable LED projectors, large-size LED backlighting displays, LED general lighting, visible light communication, purifiers, and biomedical sensors as shown in Fig. 3.4. Moore's Law predicts the doubling of the number of Si transistors in a chip every 18–24 months. Similarly, for LEDs, luminous output (luminous flux, measured in lm) appears to follow Haitz's Law, which states that LED flux per package has doubled every 18–24 months for more than 30 years [2]. This trend in the technological advancement of LEDs is based on industry-driven R&D efforts targeting high-efficiency, low-cost technology solutions that can successfully provide an energy saving alternative to the recent applications of LEDs.

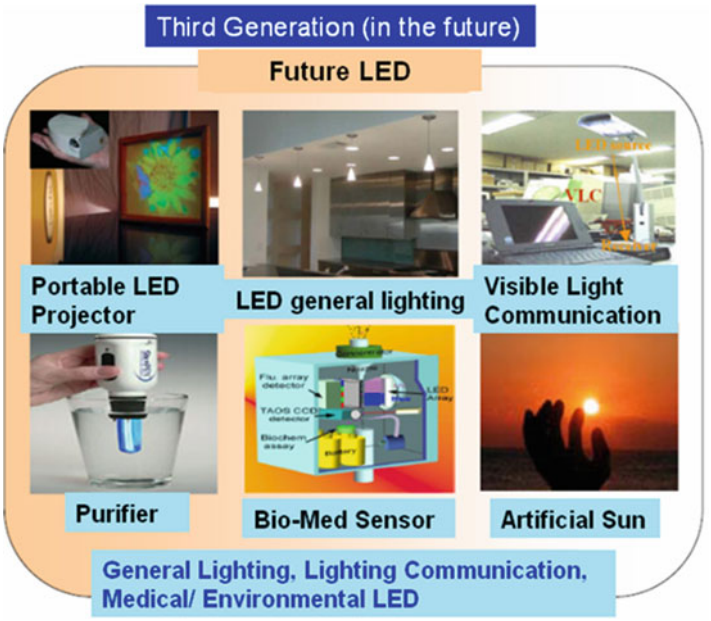


Fig. 3.4 Future LED applications (© Korea Photonics Technology Institute), reprinted with permission

LED dies are composed of a p-junction, a quantum well (active layer) or multiple-quantum wells, and an n-junction. LEDs emit light due to the injection electroluminescence effect in compound semiconductor structures. When a p–n junction is biased in the forward direction, electrons in the n-junction have sufficient energy to move across the boundary layer into the p-junction, and holes are injected from the p-junction across the active layer into the n-junction. The active region of an ideal LED emits one photon for every electron injected. Each charged quantum particle (electron) produces one light quantum particle (photon). Thus, an ideal active region of an LED has a quantum efficiency of unity. The internal quantum efficiency is defined as the number of photons emitted from an active region per second divided by the number of electrons injected into the LED per second. The light extraction efficiency is defined as the number of photons emitted into free space per second divided by the number of photons emitted from the active region per second [8, 15]. Thus, the external quantum efficiency is the ratio between number of photons emitted into free space per second and number of electrons injected into LED per second. Higher external quantum efficiency results in higher light output for the same amount of input.

The LED supply chain starts from an LED chip and progresses to an LED package, an LED module, and then to a system shown in Fig. 3.5. LED production starts from a bare wafer such as sapphire, GaN, SiC, Si, or GaAs. Many thin epilayers are grown on the bare wafer. Different colors of LEDs can be made by using different types of epiwafers. The types of epiwafer are InGaN/AlGaN for

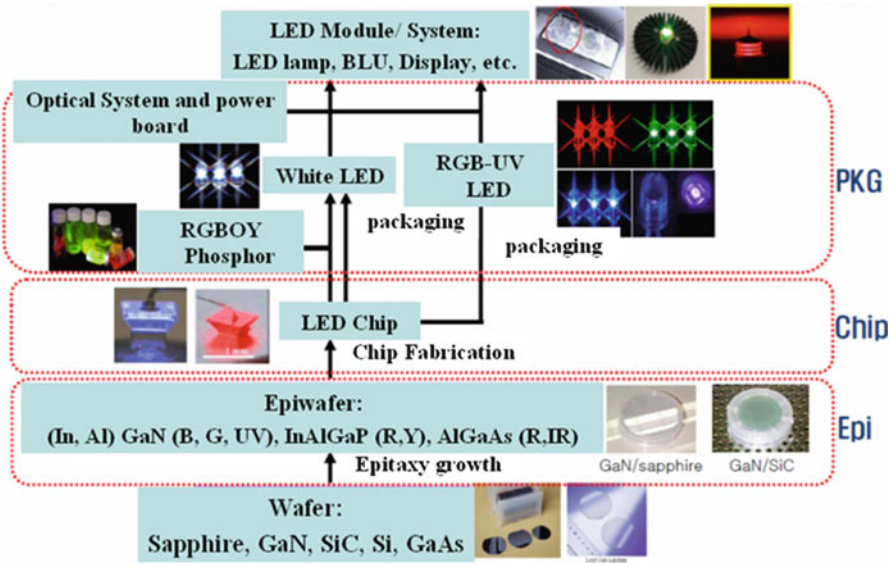


Fig. 3.5 LED supply chain (© Korea Photonics Technology Institute), reprinted with permission

producing blue, green, and UV-range light; InAlGaP for producing red and yellow light; and AlGaAs for producing red or infrared-range light. The LED chip fabrication process involves attaching electric contact pads on an epiwafer and cutting the epiwafer into LED dies that are then packaged.

LEDs are classified into two types: white LEDs and RGB LEDs. White LED packages can use red/green/blue/orange/yellow phosphors with blue LED chips to produce white light. The phosphors comprise activators mixed with impurities at a proper position on the host lattice. The activators determine the energy level related to the light emission process, thereby determining the color of the light emitted. The color is determined by an energy gap between the ground and excitation states of the activators in a crystal structure. RGB LED packages represent red LED package, green LED package, blue LED package, and LED package with multi-dies in a single package producing white light using a combination of red, green, and blue LED dies.

A cross-sectional side view of white LEDs is shown in Fig. 3.6. An LED package mounted on a printed circuit board is composed of housing, encapsulant, die, bond wire, die attach, lead frame, metal heat slug, and solder joint. The housing is a body for supporting and protecting the entire structure of an LED device. The housing is usually formed of materials such as polyphthalamide (PPA) or liquid crystal polymer (LCP). The encapsulant positioned over the housing is a resin material for the LED package in the shape of a dome. The typical material types for the resin are epoxy or silicon. The die is compound semiconductor. The lead frame is used to apply external power to the LED die. The die attach is used to mechanically and thermally connect the chip onto the lead frame. Typical types of die attaches are Ag paste and epoxy paste. Phosphors dispersed in the encapsulant are used to emit the white light excited by absorbing a portion of the light from the LED dies.

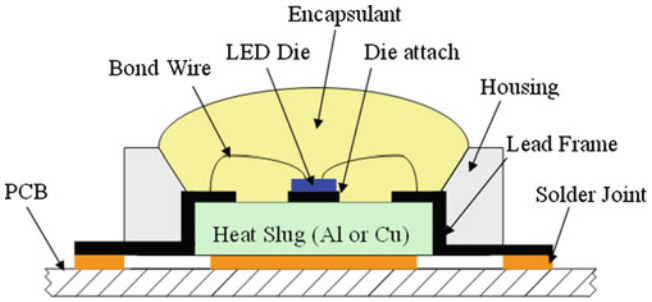


Fig. 3.6 LED package assembled with printed circuit board (PCB)

LED types are placed in the following major categories depending on LED electrical power: low power LEDs are under 1 W of power (currents typically near 20 mA), medium power LEDs (high brightness LEDs) dissipate between 1 and 3 W power (currents typically in the 30 mA/75 mA/150 mA range), and high power LEDs (ultrahigh brightness LEDs) have more than 3 W electrical power (currents typically in 350 mA/750 mA/1,000 mA range). The LEDs vary because of the LED current–voltage curves vary between the materials.

The LED industry, despite exciting innovations driven by technological advances and ecological/energy-saving concerns, still faces challenges in attracting widespread consumption. One issue of concern is price and another is lack of information regarding reliability. The required number of LEDs for general lighting applications is a matter of concern where both of these issues converge. It may take from tens to sometimes thousands of LEDs to replace one conventional lamp because the emission of a single LED covers a limited area. If one single LED fails, the final product is sometimes treated as a failure. For example, the failure of LEDs in an LCD display is very critical even when only a single LED package experiences changes in optical properties [16]. Failures of an LED or LEDs appear as a dark spot, dark area, or rainbow area.

The LED die is a semiconductor, and the nature of manufacturing of LED packages is similar to that of microelectronics. But there are unique functional requirements, materials, and interfaces in LEDs resulting in different failure modes and mechanisms. The major causes of failures can be divided into die-related, interconnect-related, and package-related. The die-related failures include severe light output degradation and burned/broken metallization on the die. The interconnect failures of LED packages are electrical overstress-induced bond wire fracture/wire ball bond fatigue, electrical contact metallurgical interdiffusion, and electrostatic discharge, which leads to catastrophic failures of LEDs. Package-related failure mechanisms include carbonization of the encapsulant, encapsulant yellowing, delamination, lens cracking, phosphor thermal quenching, and solder joint fatigue that result in an optical degradation, color change, an electrical open/short, and severe discoloration of the encapsulant. In this chapter, the focus is on the failure sites, modes, and mechanisms at these three levels.

Cost is another barrier that confronts the LED industry in seeking to expand market share in general lightings. The current cost of LEDs ranges from $0.40 to $4 per package depending on their applications. In the recent past, LEDs were often too expensive for most lighting applications. Even though the sale price of LEDs is decreasing fast, it is still much higher than the price of conventional light sources. According to a study, the life cycle cost of LED lighting systems is less than for incandescent lamp systems [17]. The total cost of a lighting system includes the cost of electricity, cost of replacement, and the initial purchase price. Since the lifecycle savings are not guaranteed at the time of lighting systems selection, higher initial costs are still an obstacle to the acceptance of LED lighting. Manufacturing cost and selling price reduction while maintaining the reliability level is key to increasing market share. According to a study by Samsung, the selling price of a white LED lighting system needs to decrease by 50% in order to strengthen LED's competitiveness with fluorescent lamp systems over a 4- to 5-year period [17].

3.2 LED Reliability

End-product manufacturers that use LEDs expect the LED industry to guarantee the lifetime of LEDs in their usage conditions. Such lifetime information would allow LED designers to deliver the best combination of purchase price, lighting performance, and cost of ownership for the life of the products. One barrier to the acceptance of LEDs in traditional applications is the relatively sparse information available on their reliability. There are many areas in need of improvement and study regarding LEDs, including the internal quantum efficiency of the active region, light-extraction technology, current-flow design, the minimization of resistive losses, electrostatic discharge stability, increased luminous flux per LED package, and purchase cost [4]. Another barrier is the lack of globally accepted thermal standards because all commercial properties of an LED-based system, such as light output, color, and lifetime, are functions of the junction temperature. More details can be found in Sect. 3.6.

It is rare for an LED to fail completely. The life can also vary from 3 months to as high as 50,000–70,000 h based on application and construction [18]. LED lifetime is measured by lumen maintenance, which is how the intensity of emitted light tends to diminish over time. The Alliance for Solid-State Illumination Systems and Technologies (ASSIST) defines LED lifetime based on the time to 50% (L50: for the display industry approach) or 70% (L70: for the lighting industry approach) of light output degradation at room temperature, as shown in Fig. 3.7 [19]. The accelerated temperature life test is used as a substitute for the room temperature operating life test to quickly forecast LED lifetime. Prediction of LED lifetime varies with the method of interpreting the results of the accelerated tests [20–22].

LED manufacturers usually perform tests in the product development cycle during the design and development phases. Typical qualification tests of LEDs are categorized into operating life tests and environmental tests by using industrial

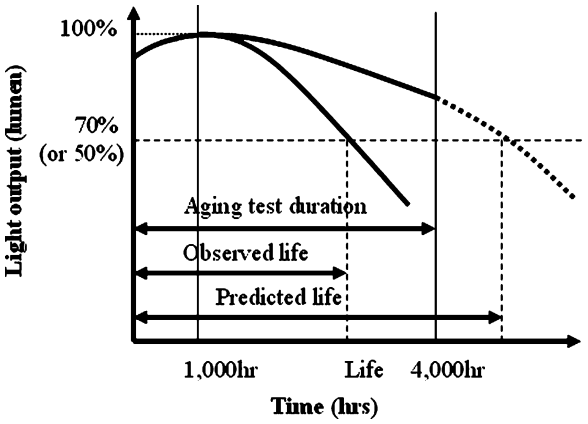


Fig. 3.7 Lifetime estimation based on LED life test

standards such as JEDEC or JEITA [23, 24]. Operation life tests are performed by applying electrical power loads to LEDs adding the Joule heating to the internal part of LEDs. On the other hand, environmental tests are conducted with nonoperating life tests. Tests will vary depending on the manufacturer. Generally, operating life tests for LEDs are the room temperature test, the high temperature test, the low temperature test, the wet/high temperature test, the temperature humidity cycle test, and the on/off test. Environmental tests of LEDs include the reflow soldering test, the thermal shock test, the temperature cycle test, the moisture resistance cyclic test, the high temperature storage test, the temperature humidity storage test, the low temperature storage test, the vibration test, and the electrostatic discharge test. Even combinations of these kinds of loading conditions are used. The acceptance criteria are pass or fail.

Environmental tests check the light output at the initial test condition and the final test condition. Other parameters are sometimes collected, such as chromaticity coordinate values (x and y) and reverse current when the lumen measurement is conducted at each data readout time. In many cases, the proper failure criteria of these other parameters are not defined to demonstrate how these collected data are correlated with the data of the light output degradation measurements.

The LED system manufacturers are interested in estimating the expected duration of LEDs, since customers want the manufacturers to guarantee a certain level of LED lifetime in the usage conditions of the product and the manufacturers want to estimate the life cycle cost of LED systems. To achieve this, they usually perform accelerated life tests at high temperatures while monitoring the light output. Modeling of acceleration factors (AF) is generally used to predict the long-term lifetime of LED packages at specific usage conditions [20, 25]. A lifetime estimate is generally made using the Arrhenius model. Activation energy is sensitive to the test load condition, types of materials, and mechanical design of LED packages. This estimate of LED lifetime includes uncertainties such as exponential extrapolation of lifetime, assumption of activation energy, and possible failure mechanism shift between test and usage conditions, and all other failure causes except temperature.

One method for predicting the lifetime of LEDs is the use of an accelerated test approach where the estimated lifetime in the accelerated life tests is multiplied by an acceleration factor as follows: measurement of the light output of samples at each test readout time, functional curve fitting of time-dependent degradation at test conditions, acceleration factor calculation, and lifetime prediction at the usage condition by using the acceleration factor multiplied by the lifetime of the test conditions. The conventional acceleration factor model reflects the junction temperature difference between the operating conditions and test conditions, as shown in (3.1).

$$AF_{\text{temp}} = \exp\left[\left(\frac{E_a}{k}\right)\left(\frac{1}{T_u} - \frac{1}{T_a}\right)\right], \tag{3.1}$$

where E_a is the activation energy (eV), T_u is the junction temperature at usage conditions, T_a is the junction temperature at accelerated conditions, and k is the Boltzmann constant (8.6×10^{-5} eV/K).

The optical performance of an LED package is dependent on temperature. The junction temperatures in the active layers (quantum well structures) between the p–n junctions of the chip affect optical characteristics such as color and dominant wavelength. Direct measurement of the junction temperature is difficult, and the estimation of the junction temperature is derived from the LED case temperature or lead temperature. The luminous efficiency becomes low as the luminous flux emitted from an LED package decreases and the junction temperature increases. The junction temperature is dependent on the operating conditions (the forward current and the forward voltage) and operating environment. Light output measurement does not isolate the failure mechanisms of LEDs because all failures affect light degradation. This current method may provide some figure of merit of comparison of life expectancy of different LEDs but it does not provide information on reliability. This method also does not help with remaining useful life estimation during operation.

Each LED lighting system manufacturer may use additional tests based on empirical development histories, applying previous product information to product development. The simple functional plotting in test conditions can be affected by the value of the activation energy of the Arrhenius model. This empirical curve plotting sometimes results in unclear data trending of LED lifetime even in the test conditions, since the functional curve fitting is very sensitive in terms of the number of samples and test duration [26–28]. There is a need to develop a more advanced life qualification tool that is able to predict the lifetime of a lighting system during the design, development, and early production phases using analytical tools, simulation, and prototype testing [29–36]. These techniques must be properly utilized in order to achieve improved reliability, increased power capability, and physical miniaturization [37–41].

LED lighting systems are needed to keep the light output and color of an LED constant through the lifetime of the LED by adjusting the amount of current when

necessary. LED manufacturers usually specify a maximum current at each ambient temperature. Therefore, thermal feedback can be set to obtain maximum current at a specific temperature. A major issue in high power LED applications involves thermal cooling of the systems. Currently, multiple temperature sensors, microprocessors, and/or amplifiers are utilized to reduce average LED current along a given maximum current vs. ambient temperature profile.

The LED circuit design on the printed circuit boards also needs to be controlled to maintain electrical and optical stabilities of LEDs [31, 42–46]. Systems for driving LEDs are generally composed of AC–DC power supplies, a DC–DC converter, intelligent controllers, an LED driver, and an LED board to maintain the light output and color of LEDs [47, 48]. For the lighting system design, one must take into account the following: availability for saving space on and cost of the PCB by integrating components, the level of flexibility to add features and adapt to last minute changes, and compatibility for interfacing different types of sensors with current design. In the case of outdoor and indoor lighting applications, an intelligent controller may not be required because the color change is not as critical as the LED display backlighting systems. Input is used to power up the intelligent regulator. An intelligent controller enables binning/temperature compensation, color temperature control, and color control of the lighting system via the color sensor and temperature sensor. The intelligent controller includes programmable digital blocks and analog blocks. These blocks are interfaced with external sensors for collecting censored/amplified data and filtering the data out to perform feedback input. LED drivers generate constant current to light up each LED string. LED driver circuits are composed of current sense amplifiers (feedback elements), hysteretic controllers (control function), internal n-channel MOSFETs (switches), gate drivers for driving external n-channel MOSFETS, n-bit hardware PWMs/PrlSMs/DMMs (modulation), hardware comparators (protection and monitoring), hardware DACs (protection and monitoring), a switching regulator, and a dedicated port of IOs to connect to power peripherals and GPIO functionality [47]. The intelligent controller and LED driver can be embedded into one circuit board for cost savings, smaller PCB size, and intelligent lighting design for tunable white light and color-mixed light operations.

The ways to drive the current to light up LEDs are divided into pulsed width modulation (PWM) dimming and analog dimming (amplitude dimming) [49]. Analog dimming involves changing the constant current through the LED by adjusting the sense voltage. Analog dimming does not generate additional switching noise in the LED lighting system and has higher efficacy as current levels decrease. The dominant wavelength varies with LED current due to band filling and quantum-confined Stark effect (QCSE), so some color shift is to be expected when using analog dimming. On the other hand, PWM dimming sets a desired LED current and can turn the LED on and off at speeds faster than the human eye can detect. The color of LEDs can be controlled by using PWM dimming if the junction temperature is controlled since the dominant wavelength changes due to the junction temperature. The input supply needs to be filtered properly to accommodate high input current transients. The efficiency of PWM dimming is lower than that of the analog dimming [49]. PWM dimming technology is categorized into enable dimming, series

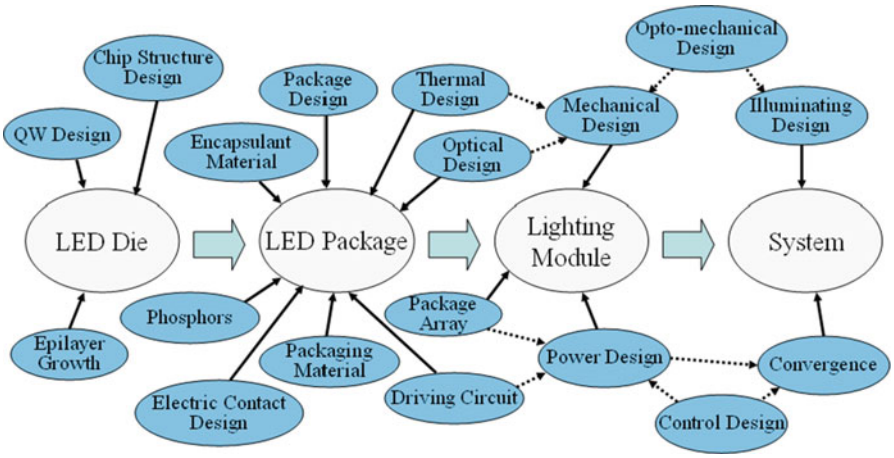


Fig. 3.8 LED core technology

dimming, and shunt dimming. Enable dimming produces PWM current by turning on and off the current; enable dimming is easy to implement, but typically shows slow current transitions. Series dimming uses the series field effect transistor (FET) to generate PWM current with fair current transition. Output voltage can overshoot when using series dimming. Shunt dimming utilizes shunt FET to make the PWM signal with superfast current transitions. The drawback of shunt dimming is that power is dissipated in the shunt FET. If it is necessary to drive different types of LEDs having different forward voltages, multi-boost or buck current mode control is used due to the benefit of independent multiple power stages. PWM dimming control is good for driving uniform LEDs with the same color and forward voltages [48].

LED core technology in terms of structural and reliability analysis is shown in Fig. 3.8. To develop final LED product (e.g., system), manufacturers are required to consider each levels in Fig. 3.8 (composed of LED die, LED package, LED module, and system) because market share power is based on optimal thermal dissipation, high external quantum efficiency, high electrical power conversion efficiency, enhanced performance, low cost, advanced opto-mechanical design (minimizing rainbow or glare effects), and high reliability.

LED package reliability is predominantly important to improve LED lighting system reliability since all other parts including mechanical parts, power, and electric circuit can be repaired or replaced by scheduled maintenance before the system experiences failure. Once LED package or LED module encounter failures, this means that LED system needs to take unscheduled maintenance which causes end users high cost to replacement. Many of LED failure modes and mechanisms are related to thermal, electrical, and humidity stress. This chapter will review LED failures with failure sites of LEDs and those stresses.

3.3 Physics of Failure

3.3.1 Reliability and PoF Approach

Reliability is the ability of a product to properly function within specified performance limits for a specified period of time under the life cycle application conditions. A product must function within certain tolerances in order to be reliable within specified performance limits. A product has a useful life during which it is expected to function within the tolerances. Time can be measured in time, miles, cycles, or any sequence or sequencing index for a specified period. A product's reliability depends on its operational and environmental life cycle conditions under the life cycle application conditions. When a product fails, there are costs to the manufacturer due to loss of mission, service, or capacity; costs due to repair or replacement; indirect costs such as increase in insurance; and costs incurred by personal injury. Time-to-market can increase. This can be significant if failures occur after production. Warranty costs can increase. Significant numbers of failures can initiate a recall. Market share can decrease. Failures can stain the reputation of a company and deter new customers. Claims for damage caused by product failure can increase. Failures of even simple products can cause hardships.

IEEE Reliability Program Standard—1,332 presents the relationship between the supplier and customer, in terms of reliability objectives. The standard identifies three reliability objectives as shown in Fig. 3.9.

A. The supplier, working with the customer, shall determine and understand the customer's requirements and product needs, so that a comprehensive design specification can be generated.
B. The supplier shall structure and follow a series of engineering activities such that the resulting product satisfies the customer's requirements and product needs with regard to product reliability.

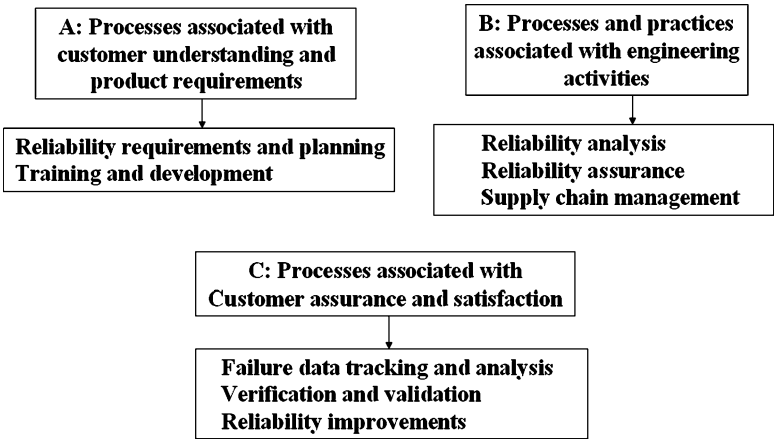


Fig. 3.9 Key reliability activities (processes)

C. The supplier shall include activities that assure the customer that the reliability requirements and product needs have been satisfied.

Key reliability activities include the following:

- Eligibility requirements and planning (plan and allocate).
- Training and development (learn and disseminate knowledge).
- Reliability analysis (assess risk).
- Reliability assurance (demonstrate).
- Supply chain management (identify and foster).
- Failure data tracking and analysis (track, analysis, and report).
- Verification and validation (prove).
- Reliability improvements (anticipate and adapt).

There are many reasons to assess reliability including:

- Increase customer confidence.
- Compare reliability requirements with state-of-the-art feasibility.
- Identify and rank potential failures and problems.
- Conduct design and development trade-offs or compare competing design and manufacturing processes.
- Reduce the time needed to gather data for risk assessment.
- Tailor tests for root cause analysis and corrective actions.
- Determine risk mitigation actions.
- Forecast warranty and life cycle costs.
- Assess logistics support parameters (e.g., provision spare parts).
- Conduct safety analysis.
- Address certification and regulatory concerns.

There are different perspectives regarding the characterization of reliability. These are Bathtub model approach and Physics of Failure (PoF) approach. Bathtub model approach utilizes system-level approach, black box approach, and top-down approach. PoF approach uses bottom-top approach. Reliability is characterized by probability of survival at any time t in a give life cycle in Bathtub model approach. On the contrary, reliability is shown as ability to survive a given life cycle within a given confidence level in PoF approach. Product is reliable when the number of failures during a specified period is at an acceptable level in Bathtub model approach. However, product is reliable if we have confidence that it will not need maintenance for a specified period of time in PoF model. In Bathtub model approach, metric is failure rate, hazard rate, or MTBF (Mean Time Between Failures). In PoF approach, metric is MFOP (Maintenance-Free Operating Period) or FFOP (Failure Free Operating Period) for a given confidence level. Bathtub model approach believes in "random" failures. PoF approach believes in strict causality of failures. Tails of statistical distributions extend from zero time to infinity (e.g., two-parameter Weibull) in Bathtub model. Product knowledge is used to truncate distributions to finite time intervals. Bathtub model is useful for viewing the "forest." PoF model is useful for viewing individual "trees." Bathtub model approach is preferred by reliability

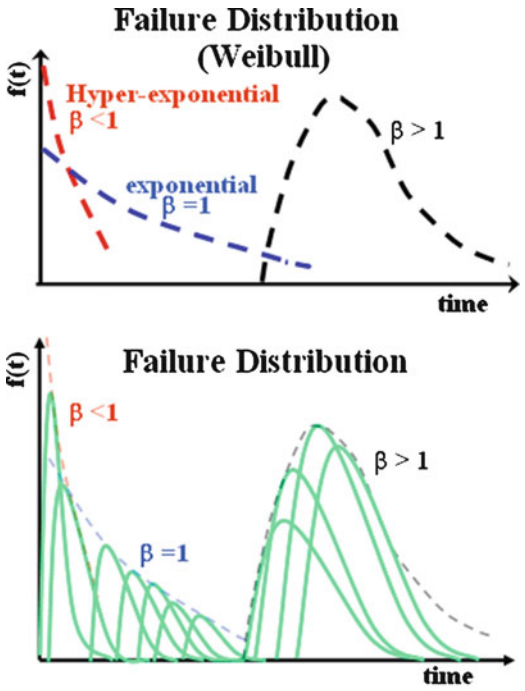


Fig. 3.10 Bathtub model approach vs. PoF perspective

statisticians. PoF approach is preferred by development engineers. Reliability statisticians are interested in tracking system-level failure data for logistical purposes and in determining how the Bathtub curve looks. Causes are infant mortality, random failures, and wear-out failures. PoF reliability engineers and designers want to figure out why the product's Bathtub curve looks the way it does, what the root causes of failures are, and how to reduce failures. Causes of PoF approach are wear-out and random overstress of defective samples and nominal samples. This concept is described in Fig. 3.10.

PoF is an approach to aid in the design, manufacture, and application of a product by assessing possible failure mechanisms due to expected life cycle stresses [50]. The PoF approach and design-for-reliability (DfR) methods have been developed by Center for Advanced Life Cycle Engineering (CALCE) [51] with the support of industry, government, and other universities. The approach is based on the identification of potential failure modes, failure mechanisms, and failure sites for product as a function of its life cycle loading conditions. The stress at each failure site is obtained as a function of both the loading conditions and the product geometry and material properties. Damaged models are then used to determine fault generation and propagation. The PoF models can be used to calculate the remaining useful life, but it is necessary to identify the uncertainties in the prognostic approach and assess the impact of these uncertainties on the remaining-life distribution in order to make risk-informed decisions [52]. With uncertainty analysis, a prediction can be expressed as a failure probability.

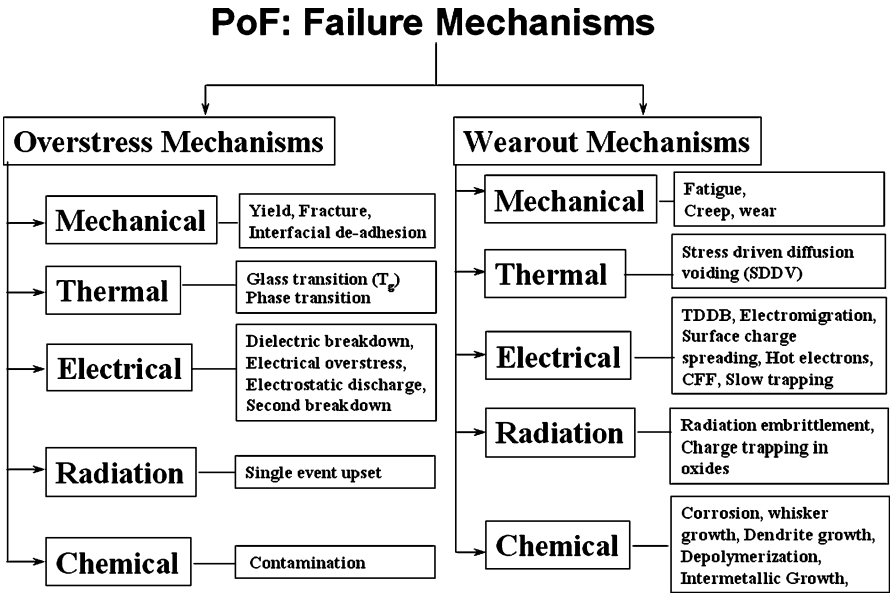


Fig. 3.11 PoF view: Failure mechanisms

PoF is a methodology for building-in reliability based on assessing the impact of hardware configuration and life cycle stresses, the materials at potential failure sites, and root cause failure mechanisms. Based on these analyses, the life cycle is managed to minimize failures. Life cycle management includes activities such as design and qualification; manufacturer, assembly, and quality assurance; supply chain management; stress management and health management; and warranty management, service, and logical support.

Failure of electronic products is caused by one of the four following types of stresses: mechanical, electrical, thermal, or chemical, and it generally results either from the application of a single overstress or by the accumulation of damage over time from lower level stresses [51]. PoF is combined with knowledge about where failure might occur (failure sites), what form it might take (failure modes), how it might initiate the failure (failure causes), and how it might take place (failure mechanisms). In other words, failure modes are effects by which failures are observed to occur; and failure mechanisms are processes by which a specific combination of mechanical, electrical, thermal, or chemical stresses induces failures. Failure mechanisms on PoF view is shown in Fig. 3.11. Radiation was added to main stress factors in Fig. 3.11. The PoF process is described in Fig. 3.12.

PoF-based time-to-failure assessment is following these steps:

- Determine the operating environment.
- Define the assembly design.
- Perform load transformation (stress analysis).
- Assess failure locations and lifetime.

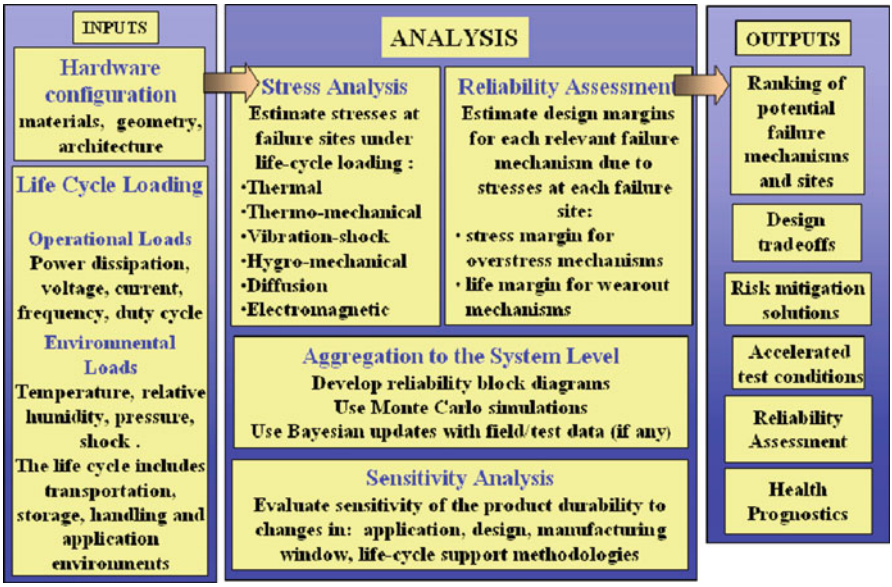


Fig. 3.12 PoF process for building-in reliability

Identification of the life cycle load is the information to develop the design, analysis, and test criteria. The information is related to the following elements:

- Operation
- Manufacturing/assembly
- Rework
- Test
- Storage
- Transportation/handling
- Repair/maintenance

The assembly design is defined by taking account of product layout (CAD files), acquiring bill of materials (BOM), material, geometry, and manufacturing tolerances. Load transformation takes load environment including outside environment and inside environment into account. The load transformation divided into outside environment and inside environment is shown in Fig. 3.13. Failure assessment determines time-to-failure using PoF-based models and depends on the critical failure mechanisms. Examples of failure mechanisms are shown in Fig. 3.14.

Apparent failures that occur during manufacture or field operation of a product that cannot be verified or assigned shown in Fig. 3.15. Failures can be induced by either user-, management-related causes or device-related causes. User can induce failures due to unfamiliarity with equipment, poor maintenance, or fraud. Management-related causes include poor design, poor diagnostic, test procedures or test equipment, poor communications, poor training, or need for compensation or

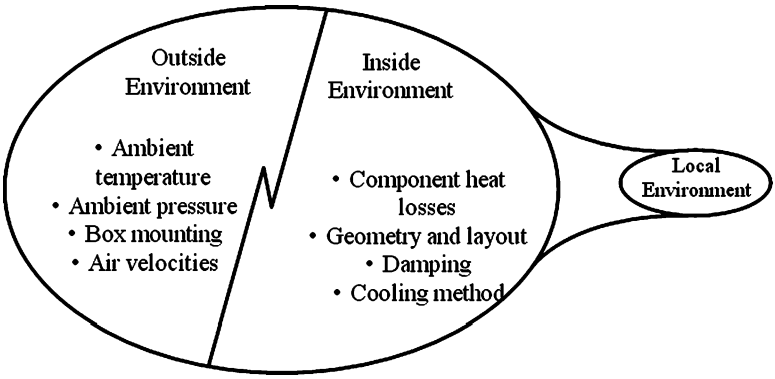


Fig. 3.13 Load transformation

Failure Mechanism	Failure Sites	Relevant Stresses	Sample Model
Fatigue	Die attach, Wire bond/TAB, Solder leads, Bond pads, Traces, Vias/PTHs,	Cyclic Deformations ΔT, ΔH, ΔV)	Nonlinear Power Law (Coffin-Manson)
Corrosion	Metallizations	M, ΔV, T, chemical	Eyring (Howard)
Electromigration	Metallizations	T, J	Eyring (Black)
Conductive Filament Formation	Between Metallizations	M, ∇V	Power Law (Rudra)
Stress Driven Diffusion Voiding	Metal Traces	σ, T	Eyring
Time Dependent Dielectric Breakdown	Dielectric layers	V, T	Arrhenius (Fowler-Nordheim)

D: Cyclic range
∇: gradient
T: Temperature
H: Humidity
V: Voltage
M: Moisture
J: Current
s: Mechanical Stress

Fig. 3.14 Examples of PoF mechanisms and models

fraud. Device-related causes contain early stages of fatigue, worn or fretted connectors, heat-sensitive components, radiation-sensitive components, noisy components, or software.

Potential reliability improvement techniques based on environmental stresses and their effects should be considered when engineers or designers are developing electronic products. Environmental stresses include high temperature, low

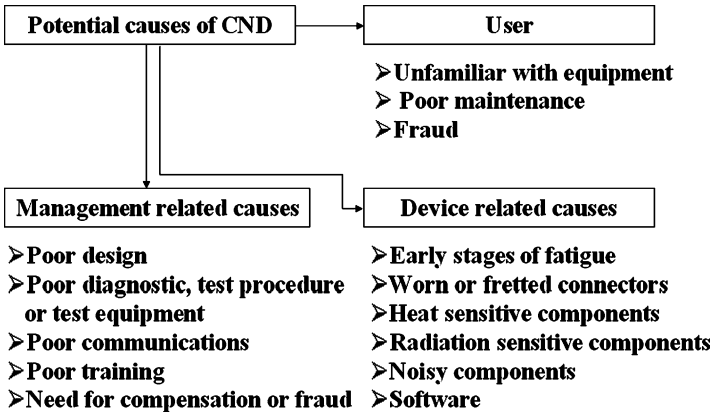


Fig. 3.15 Cannot duplicate (CND) failures

temperature, thermal cycling and shock, shock, vibration, humidity, contaminated atmosphere spray, electromagnetic radiation, nuclear/cosmic radiation, sand and dust, and low pressure (high altitude).

Reliability can be improved under high temperature environmental stress by thermal insulation, heat-withstanding materials, and cooling systems. Effects of high temperature environmental stress are the following:

- Resistance, inductance, capacitance, power, and dielectric constant may be varied.
- Insulation may soften.
- Moving parts may jam due to expansion and finishes may blister.
- Thermal aging, exudation, and other chemical reactions may be enhanced.
- Viscosity may be reduced and evaporation of lubricants can arise and structural overloads may occur due to physical expansions.

Reliability improvement techniques under low temperature environmental stress contain thermal insulation, cold-withstanding materials, and heated environments. The effects of low temperature environmental stress are the following:

- Plastics and rubbers embrittle.
- Electrical constants vary.
- Ice formation occurs when moisture is present.
- Lubricants and gels increase viscosity.
- Finishes may crack.
- Structures may be overloaded due to physical contraction.

Reliability can be improved under thermal cycling and shock environmental stress by thermal insulation and thermal management. The effects of thermal cycling and shock stress are the following:

- Overstress cracks and mechanical failures may be initiated and moved.

- Electrical properties may be permanently altered.
- Crazing, delamination, and rupture in seals may be initiated and moved.

Shock environmental stress can be minimized by considering structural strengthening, reduced inertia, and shock absorbing. The effects of shock stress are the following:

- Overstress cracks and mechanical failures.
- Structural weakening or collapse.

Reliability can be improved under humidity environmental stress by using moisture-resistant materials, dehumidifiers, protective coating, and hermetical sealing. The effects of humidity environmental stress are the following:

- Leakage paths between electrical conductors.
- Oxidation and corrosion.
- Swelling in polymers.
- Loss of humidity causes embrittlement.

Reliability under contaminated atmosphere spray environmental stress can be improved by considering nonmetal covers, use of similar metals in contact, and hermetic sealing. The effects of contaminated atmosphere spray stress are the following:

- Contaminated atmosphere spray can combine with water to provide a good conductor.
- It can lower insulation resistance.
- It can cause galvanic corrosion of metals and accelerate chemical corrosion.

Reliability under electromagnetic radiation can be improved by utilizing techniques such as shielding and radiation hardening. The effects of electromagnetic radiation stress are:

- Spurious and erroneous signals from electrical equipment.
- Spurious and erroneous signals from electronic equipment.

Reliability improvement techniques for nuclear/cosmic radiation is shielding and radiation hardening. The effects of nuclear/cosmic radiation are the following:

- Thermal aging.
- Altered chemical, physical, and electrical properties of materials.
- Gases and secondary radiation.
- Oxidation.
- Soft errors in semiconductors.

Reliability techniques for sand and dust environmental stress can be improved by embedding air-filtering, wear-proof materials, and sealing to electronic products. The effects of sand and dust environmental stress include the following:

- Scratches, abrasion, and erosion.
- Increased friction.

- Contamination of lubricants.
- Clogging of orifices.
- Cracks or chips.
- Contamination of insulation.
- Corona paths.

Reliability under low pressure (high altitude) environmental stress can be improved by strengthening and pressurizing the product, using less-volatile liquids, and improving insulation and heat transfer. The effects of low pressure stress are the following:

- Containers and tanks may overstress or fracture.
- Seals may leak.
- Air bubbles may increase due to lack of cooling medium.
- Insulation may suffer arcing breakdown.
- Ozone may form.
- Outgassing is likely.

3.3.2 Failure Modes, Mechanisms, and Effects Analysis (FMMEA)

FMEA was developed in the early 1960s by NASA and later adopted by US Navy in the 1970s and by the automotive industry in the late 1980s. FMEA provides a system of ranking, or prioritizing, potential failure modes associated with the designing and manufacturing of a new product or a change to an existing product [53]. FMEA does not identify the failure mechanisms that affect the product. Failure Modes, Effects, and Criticality Analysis (FMECA) is an extension of FMEA and was developed to include techniques to assess the probability of occurrence and criticality of potential failure modes [54]. Failure Modes, Mechanisms, and Effects Analysis (FMMEA) is an approach that uses the life cycle profile of a product along with the design information to identify the critical failure mechanisms affecting a product [55]. FMMEA methodology is shown in Fig. 3.16 [56].

In the step "define system and identify elements and functions to be analyzed," the system or product under investigation is divided into logical elements up to a level. For each element, all the associated functions are listed to facilitate failure definition. System breakdown can be either functional (i.e., according to what the system elements do) or geographic/architectural (i.e., according to where the system's elements are). A combination of the two, i.e., functional within the geographic or vice versa, can be used during system breakdown. The lowest level needs to be a geographic location so that a site is identified with every failure mode. The level to which a system can be broken down depends on the level of design to which the assessor is able to obtain part or material information.

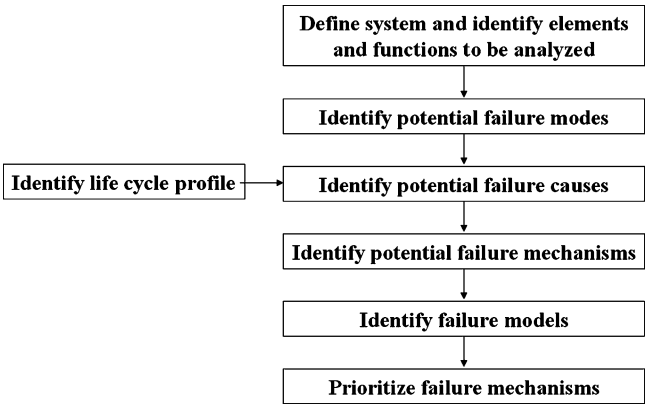


Fig. 3.16 FMMEA methodology

In a step of "identify potential failure modes," a failure mode is the effect by which a failure is observed to occur. Potential failure modes may be identified using modeling analysis, accelerated tests to failure (e.g., HALT), past experience, and engineering judgment. Failure mode identification does not always imply a cause or mechanism. All possible failure modes for each identified element should be listed.

In a step of "identify life cycle profile (LCP)," the phases in a product life cycle include manufacturing/assembly, test, rework, storage, transportation and handling, operation, repair, and maintenance. LCP is a forecast of events and associated environmental and usage conditions a product will experience from manufacturer to end of life. The description of life cycle profile needs to include the occurrences and duration of these conditions. LCPs include conditions such as temperature, humidity, pressure, vibration, shock, chemical environments, radiation, contaminants, current, voltage, power, and the rates of change of these conditions [55].

A failure cause is the specific process, design, and/or environmental condition that initiated the failure, and whose removal will eliminate the failure. In a step of "identify potential failure causes," knowledge of potential failure causes helps identify the failure mechanisms driving the failure modes for a given element. Causes are identified by brainstorming of the FMMEA group. One method of looking for causes is to review the LCP item by item to evaluate whether any of the items there could have caused the failure.

The failure mechanism is a process, not a physical condition or a failure site. Usually, overstress or wear-out can be assigned to a failure mechanism. A quality condition (e.g., void in material) is not a failure mechanism, although it can accelerate the precipitation of a failure. Over heat is not a failure mechanism. Failure of glue is not the mechanism but a failure site. When the failure mechanism is not identified, it is better to record it as unknown or not yet determined rather than making an uninformed decision.

In a step of "identify failure models," failure models quantify the time-to-failure or likelihood of a failure. For overstress mechanisms, failure models typically use

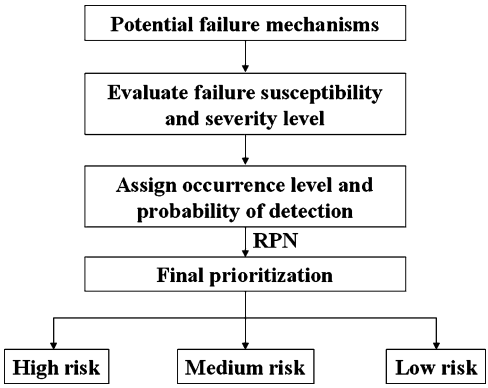


Fig. 3.17 Prioritization of failure mechanisms

stress analysis to estimate whether the product will fail under the given LCP conditions. For wear-out mechanisms, failure models use stress and damage analysis to quantify the damage accumulated in the product. If no failure models are available in the literature, empirical models are often developed from prior field failure data or from the results of accelerated testing [56].

In the life cycle of a product, several failure mechanisms may be activated by different environmental and operational parameters acting at various stress levels, but only a few operational and environmental parameters and failure mechanisms are in general responsible for high-risk failures. The prioritization process determines the high-risk failure mechanisms. Prioritization of failure mechanisms can be performed through constructing risk register and risk matrix. High-risk mechanisms are those with high combinations of occurrence and severity. Failure mechanisms can be prioritized by calculating the risk priority number (RPN) associated with each mechanism as shown in Fig. 3.17. RPN is multiplication of severity, occurrence, and detection. Severity describes the seriousness of the effect of the failure caused by a mechanism. Occurrence describes how frequently a failure mechanism is expected to result in failure. Detection describes the probability of detecting the failure modes associated with the failure mechanism.

FMMEA is utilized in international standards. Determination of failure mechanism as the basis of reliability prediction for a system has been accepted by organizations such as International SEMATECH and JEDEC/EIA [57–62]. Example standards that utilize the concepts include the following: semiconductor device reliability failure models are #00053955A-XFR-SEMATECH [63]; use of condition based reliability evaluation of new semiconductor technologies is #99083810A-XFR-SEMATECH [64]; knowledge-based reliability qualification testing of silicon devices is #00053958A-XFR-SEMATECH [65]; stress-test-driven qualification of and failure mechanisms associated with assembled solid-state surface-mount components is JEP150-JEDEC [59]; and application-specific qualification using knowledge-based test methodology is JESD94-JEDEC [61]. FMMEA-based reliability prediction methods meet the criteria set by IEEE reliability standards.

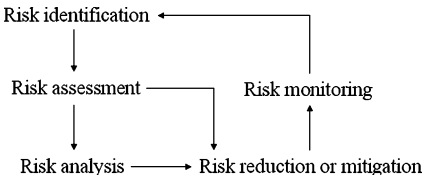


Fig. 3.18 Risk management methodology

3.3.3 Risk Register and Risk Matrix

The term of the risk register has initially been used by Dr. Lindon having discussed ensuring earlier diagnosis during infancy, efficient and regular review, and appropriate management and treatment of babies born with congenital defects in 1961 [66]. The risk register has successfully been applied in many areas such as medical areas and civil engineering areas because the risk register enables team members involved in the project to consciously evaluate and manage the risks as part of the decision-making process [67]. The main benefit of the risk register is that the risk reduction and mitigation plans within the project can be documented [68]. The risk register is generally used as a means of recording and documenting the information generated through the use of project risk management.

The risk management process models were proposed on the bases of the risk register techniques in several ways [67–69]. Department of Defense reported [67] that the risk management process model includes risk identification, risk analysis, risk mitigation planning, risk mitigation plan implementation, and risk tracking. Patterson and Neailey [68] introduced that the risk management methodology is composed of risk identification, risk assessment, risk analysis, risk reduction and/or mitigation, and risk monitoring as shown in Fig. 3.18. Eskesen et al. [69] studied that the risk management strategy is composed of a definition of the risk management responsibilities of the various parties involved (different departments within the owner's organization, consultants, and contractors), a short description of the activities to be carried out at different stages of the project in order to achieve the objectives, a scheme to be used for follow-up on results obtained through the risk management activities by which information about identified hazards accomplished by some form of comprehensive risk register, follow-up initial assumptions regarding the operational phase, and monitoring, audit and review procedures. All of these risk management models repeat the cyclic process initiated at the risk-identification stage to end stage in common with one other.

Williams [70], Carter et al. [71], and Ward [72] presented examples of the type of information or items included in the risk register. Williams [70] reported that the risk register has information with event, impact, actions, and contractual: the event is made up of description of the risk, estimated likelihood of occurrence, and owner of the risks; the impact carries project objectives on which it impacts (e.g., scheduling, cost, and specific specification of performance measure), severity of its impact, and item and groups of activities affected by the risk; the actions add risk reduction actions, contingency plans, and secondary risks; and contractual contain

degree of risk transfers. Carter et al. [71] designed a risk register that includes risk description, risk identification number, activity at risk/work breakdown reference, risk owner reference/work package manager, risk cause ownership reference, risk impact estimate, risk probability estimate, risk exposure as calculated, risk exposed as adjuster (where applicable), risk trigger indicator, and risk mitigation strategy. Ward [72] demonstrated that the risk register is incorporated with risk identifier, title, and description; description of causes and trigger events; description of impacts on cost, time and quality and quantitative assessment of range of impacts where appropriate; nature of any interdependencies with other sources of risk; timing of likely impacts; probability of occurrence; description of feasible responses, including timing required; resource implications of responses; likely effect of responses on the risk; nature of any significant interdependencies with other risks and responses; residual risk after effective response; party bearing the consequences of the risk; and party responsible for managing the risk and implementing responses.

Risk register contains the information on the identified and collected project risks that the project team identifies when estimating and adjusting the activity durations for risks. Here are outcomes of risk reassessments, risk audits, and periodic risk reviews. These outcomes may include identification of new risk events, updates to probability, impact, priority, response plans, ownership, and other elements of the risk register. Outcomes can also include closing risks that are no longer applicable and releasing their associated reserves.

The Risk Register records details of all the risks identified at the beginning and during the life of the project, their grading in likelihood of occurring and seriousness of impact on the project, initial plans for mitigating each high level risk and subsequent results. A wide range of contents for a risk register existed and recommendations are made by the Project Management Institute Body of Knowledge (PMBOK) and PRINCE2 among others. Typically a risk register contains the following:

- A description of the risk.
- The impact should this event actually occur.
- The probability of its occurrence.
- A summary of the planned response should the event occur.
- A summary of the mitigation (the actions taken in advance to reduce the probability and/or impact of the event).
- The risks are often given a ranking with the highest priority risks clearly identified to all involved.

Risk matrix is a table that has several categories of probability, likelihood, or frequency for its columns (or rows) and several categories of severity, impact, or consequences for its columns (or rows, respectively) shown in Table 3.2 [66]. It associates recommended level of risk, urgency, priority, or management action with each row-column pair (that is cell). Risk matrix is a process which users decide if further action is required for reducing and/or mitigating each specified risk.

Table 3.2 Risk matrix

	Consequence criteria				
Likelihood	Insignificant	Considerable	Serious	Severe	Catastrophic
Very high	Low	Medium	High	High	High
High	Low	Medium	High	High	High
Moderate	Low	Low	Medium	High	High
Low	Low	Low	Low	Medium	High
Very low	Low	Low	Low	Low	Medium

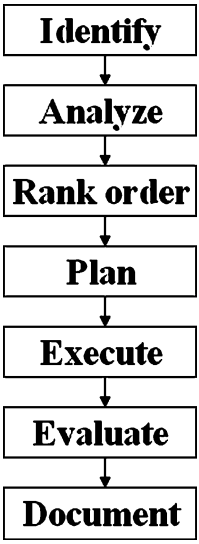


Fig. 3.19 Risk register working process

Risk register and risk matrix, which have been recommended in national and international standards, are popular tools with the use of setting priorities and guide resource allocations. They have spread through many areas of applied risk management consulting and practice, including enterprise risk management (ERM) and corporate governance, highway construction project risk management, airport safety, homeland security and risk assessment of potential threats to office buildings, ranging from hurricanes to terrorist attacks.

The risk register tool combines the different phases of identifying risks, performing qualitative risk analysis, performing quantitative risk analysis, planning risk responses, and monitoring and controlling risks together. Figure 3.19 shows risk register process.

Risk register and risk matrix not only provide a useful tool for managing and reducing the risks identified before and during the project but also serve as the document risk mitigation strategies being pursued in response to the identified risks and their grading in terms of likelihood and seriousness. They provide the Project Sponsor, Steering Committee/Senior Management with a documented

framework from which risk status can be reported; ensure the communication of risk management issues to key stakeholders; provide a mechanism for seeking and acting on feedback to encourage the involvement of the key stakeholders; and also identify the mitigation actions required for implementation of the risk management plan and associated costs.

Performing qualitative risk analysis is the process of prioritizing risks for further analysis or action by assessing and combining their probability of occurrence and impact, while performing quantitative risk analysis is the process of numerically analyzing the effect of identified risks on overall project objectives. The Perform Quantitative Risk Analysis process analyzes the effect of those risk events which may be used to assign a numerical rating to those risks individually or to evaluate the aggregate effect of all risks affecting the project. It also presents a quantitative approach to making decisions in the presence of uncertainty. Three important quantitative elements in risk register are as follows:

(1) Impact/consequence/severity (negligible, marginal, significant, critical, or crisis).
(2) Likelihood/probability/frequency (very unlikely, unlikely, moderately likely, likely, very likely).
(3) Risk level/priority/urgency = probability × consequence (or frequency × severity or likelihood × impact or threat × (vulnerability × consequence), etc.) (low, moderate, or high).

Probability is a way of expressing knowledge or belief that an event will occur or has occurred. If deemed as the relative frequency, probability = relative frequency of occurrence in a long series of similar trials. If deemed as the degree-of-belief probability, probability = degree of belief (objective or subjective) in truth of a hypothesis or the occurrence of an event. The greater the willingness to take action in the face of uncertainty seems, the greater the degree of belief is.

From Bayesian thinking, probabilities are defined directly on the state of nature, which necessitates a prior probability (base rate). Likelihood = weight of evidence.

3.4 Failure Modes and Mechanisms in LEDs

This chapter discusses LED package reliability using a PoF approach to demonstrating the defect-related reliability of LEDs. The failure mechanisms of LEDs are divided into three categories based on the failure sites: semiconductor, interconnect, and package. Semiconductor related failure mechanisms include defect and dislocation generation and movement, die cracking, dopant diffusion, and electromigration. Interconnect-related failure mechanisms are electrical overstress-induced bond wire fracture/wire ball bond fatigue, electrical contact metallurgical interdiffusion, and electrostatic discharge. Package-related failure mechanisms in LEDs include carbonization of the encapsulant, delamination,

encapsulant yellowing, lens cracking, phosphor thermal quenching, and solder joint fatigue. This section discusses 13 different types of failure mechanisms of LEDs based on previously published papers and opinions of experts in the LED industry.

3.4.1 Defect and Dislocation Generation and Movement

The lifetime and performance of LEDs are limited by crystal defect formations in the epitaxial layer structure [73–76] of the die. Crystal defects are mainly generated in contacts and in the active region [77]. Crystal defects result in a reduction in the lifetime [78] of nonequilibrium electron hole pairs and an increase in multi-phonon emissions under high drive currents [79–83]. Multi-phonon emissions result in strong vibration of defect atoms and reduce the energy barrier for defect motions such as migration, creation, or clustering [83].

The failure modes are light output degradation due to nonradiative recombination at defects and shifted electrical parameters due to increased reverse leakage currents. Electrical failure modes known for this failure mechanism include an increase in the reverse leakage current along with optical power degradation, an increase in the -generation-recombination current at low forward bias, an increase in the diode ideality factor, and an increase in parasitic series resistance. For a perfect diode, the ideality factor is unity (1.0). For real diodes, the ideality factor usually assumes values between 1.1 and 1.5. However, values as high as 7.0 have been found for GaN/InGaN diodes [84]. Parasitic series resistance is related to a semiconductor's Ohmic contact degradation on top of the p-layer, and it induces high-current crowding effects that increase the current during the DC aging tests at different current levels [79, 80]. In the case of GaAlAs/GaAs LEDs, even moderate dislocation densities ($\sim 10^4\ \mathrm{cm}^{-2}$) can affect the operating life of LEDs, and the degradation rate related to the dislocation motion is high [85]. On the other hand, the degradation rates of InGaAsP/InP and InGaN LEDs are slow compared to GaAlAs/GaAs LEDs since the defects have no deep trap levels in the band gap and they do not act as nonradiative recombination centers as do GaAlAs/GaAs LEDs [85, 86].

Defects introduced during crystal growth are divided into interface defects and bulk defects [87]. Interface defects include stacking faults, V-shaped dislocations, dislocation clusters, microtwins, inclusions, and misfit dislocations. Bulk defects include defects propagating from the substrate and those generated by local segregation of dopant atoms or native point defects. Structural imperfections due to thermal instability also contribute to defect generation during the crystal growth. Degradation modes of defect generation in LED dies are divided into rapid degradation (random or sudden unpredicted degradation) and gradual degradation (wear-out degradation). Recombination-enhanced dislocation climb and glide are responsible for rapid degradation [88]. One example of gradual degradation is the exits due to the recombination-enhanced point defect reaction in GaAlAs/GaAs-based optical devices. Internal stress due to lattice mismatch also causes gradual degradation [83, 89].

Gradual degradation proceeds as follows: nonradiative recombination occurs in some defects, which causes a point defect reaction and fresh point defect generation. The new defects can also act as nonradiative recombination centers. The generated point defects migrate and condense at some nucleation centers. Defect clusters and/or microloops are formed as byproducts [87]. Chuang et al. stated that four actions are continuously repeated when an electron is captured with the subsequent capture of a hole at a defect site, which causes strong defect vibrations and results in defect generation [83]. The four actions are electron-hole nonradiative recombination at defect sites, the release of band gap energy via multi-phonon emissions, strong vibration at defect sites, and defect diffusion and generation.

Ferenczi reported that gradual performance degradation is mainly concerned with the formation of new nonradiation recombination sites leading to a decrease in the radiative quantum efficiency [90]. If the nonradiative recombination centers form at interfaces, the increased interface density of states leads to erratic switching drawbacks and finally dislocation movement and increased dislocation concentration. This results in mechanical stress fields when dislocation concentration increases greatly.

The dislocation velocity (V_d) of semiconductors is known to depend on applied shear stress (τ) as the driving glide motion and on dislocation mobility (μ) [85, 86]:

$$V_d = \tau\mu, \tag{3.2}$$

$$\mu = \frac{V_0}{\tau_0}\exp\left(\frac{-E_d}{kT}\right), \tag{3.3}$$

where E_d is the activation energy of dislocation motion, T is the temperature, and V_0 and τ_0 are pre-exponential factors. It has been reported that GaN-based LEDs are more reliable than GaAs-based LEDs in high density dislocations [86]. The applied shear stress (τ) is affected by internal misfit strain, thermal strain, and external mechanical strain. Three types of dislocations of GaN-based LEDs are observable by cross-sectional transmission electron microscopy (XTEM) as schematically illustrated in Fig. 3.20 [86]. Type 1 dislocations are wing-shaped 60° or screw dislocations on the basal (0 0 0 1) plane, type 2 dislocations are straight threading edge dislocations existing on $\{1\,\bar{1}\,0\,0\}$ planes, and type 3 are the dislocations staying at buffer layer. Failure analyses for defect and dislocation generation and movement were followed by electrical current voltage (I–V) characteristics and capacitance–voltage (C–V) measurements, deep level transient spectroscopy (DLTS) analyses, and optical device emission measurements made by using the complementary techniques of electroluminescence (EL) and cathodoluminescence (CL) to detect different excitation mechanisms and power regimes as well as efficiency decrease during stress [91].

Threading dislocations form at the interface of the substrate and epitaxial layer. These propagate toward the surface of the epitaxial layer and are often called micropipes because of their open core nature. Threading dislocations form in highest density on sapphire-based GaN LEDs [92, 93].

Pan et al. reported that current-induced thermal effects play a role in the luminescence efficiency of UV LEDs under DC and pulsed injection. The thermal effects

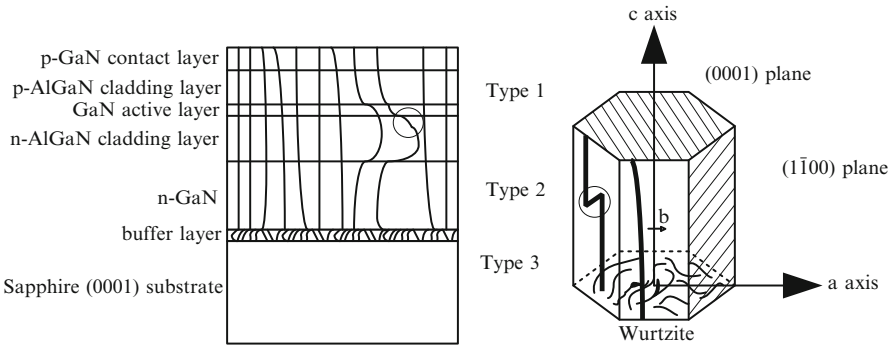


Fig. 3.20 Schematic diagram of types of dislocations in GaN-based LEDs [86] (© American Institute of Physics), reprinted with permission

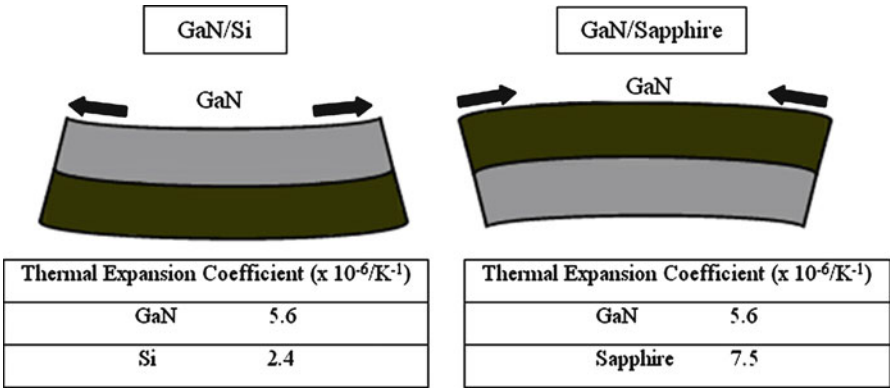
affect the redshifted luminescence wavelength of DC-driven devices. The failure of UV LEDs was found to be due to carrier overflow and nonradiative recombination through threading dislocation [94]. Pavesi et al. reported that failures of structural properties (defects, unintentionally incorporated impurities, and doping) are due to electrothermal stress [95]. Pavesi et al. also discussed the temperature and current dependences of the electrical activity of localized defects and their effects on the electroluminescence efficiency in InGaN-based blue LEDs [96].

Cao et al. investigated electrical and optical degradation of GaN/InGaN single-quantum-well LEDs under high injection current and reverse-bias stress [97]. Gradual changes in light output power–current–voltage characteristics showed the slow formation of point defects, which enhance nonradiative recombination and low-bias carrier tunneling. Cao et al. proposed two different models for defect generation. Defect generation under high forward-current stress results from a thermally assisted and recombination-enhanced process in the InGaN layer. The defect generation under high reverse voltage changes the material, resulting in avalanche breakdown at the boundaries between the space-charge region and preexisting microstructural defects.

Future research on defect and dislocation generation and motion needs improved structural and material design of LED die and internal thermal management handling thermal resistance from junction to the package to reduce formation of crystal defect and dislocation movement caused by high current-induced thermal effect and high ambient temperature.

3.4.2 Die Cracking

Extreme thermal shocks can break the LED die. Due to differences in material properties (such as coefficient of thermal expansion), LED packages can be subjected to mechanical stress when a high drive current is applied (in which causes



Thermal Expansion Coefficient (x $10^{-6}/K^{-1}$)	
GaN	5.6
Si	2.4

Thermal Expansion Coefficient (x $10^{-6}/K^{-1}$)	
GaN	5.6
Sapphire	7.5

Fig. 3.21 Thermal expansion coefficients of GaN/Si and GaN/Sapphire

Joule heating at fast rate) or when high ambient temperature conditions are suddenly applied [15]. The high electrical stress and extreme thermal shock are the causes of die cracking [15, 75, 79]. It is necessary to control die cracking by fine-tuning thermal expansion coefficients between the substrate and epitaxial layers, as shown in Fig. 3.21. The growth of optimal medium layer between the substrate and the epitaxial layer is a key technology to prevent the die cracking [98].

In some cases, the failure mode from die cracking can be electrical degradation and not, as intuitively expected, overstress failure. Barton et al. [98] found that the light output degradation was due, not to a change in contact resistance or the optical transmission of the plastic encapsulation, but due to die cracking. Electron beam-induced voltage (EBIV) analysis showed that the light output degradation was due to a crack propagated through the p-contact and the active layer in the LED die, thus isolating part of the junction area from the p-contact. The sawing and grinding quality of the die has a significant impact on the occurrence of die crack [99, 100]. Initial defects, such as tiny notches or micro-cracks, caused by the sawing and/or the grinding process may act as a starting point for die cracking. Chen et al. reported that the strength of LED dies cut from wafers has to be determined for the needs of the design in order to assure the good reliability of the packages in manufacturing and service [101].

3.4.3 Dopant Diffusion

To produce a high brightness GaN-based LED, an efficient current injection into the LED through the p-GaN layer is usually required. The p-GaN layer needs the improvement of the hole concentration of the p-GaN layer as well as the conductivity in order to decrease the resistivity of the p-type Ohmic contact [102–109]. For the p-type GaN, Mg is used as the acceptor [110] in order to inject the current into LEDs efficiently. Si is generally used in the growth process of GaN as an n-type

dopant. When Mg diffuses into the quantum well during the growth of the p-GaN layer it causes lowering of the internal quantum efficiency of the multiple quantum well (MQW) as the Mg acts as the nonradiative recombination center [111]. The effect of distribution of Mg dopant into the quantum well is called dopant diffusion. The Mg doping profile close to the active region was found to be influenced by segregation as well as by diffusion during growth.

Kohler et al. investigated the influence of the Mg doping profile on the electroluminescence (EL) efficiency of (AlGaIn)N quantum well LEDs grown by low-pressure metal-organic vapor phase epitaxy [111]. They found that high Mg concentrations close to the active region that started at low growth temperatures increased EL efficiency because of improved hole injection. Conversely, high Mg concentrations close to the GaInN QWs increase nonradiative recombination rates. Kwon et al. [112] further reported that the performance of InGaN-GaN MQW ultraviolet LEDs was enhanced by gradient doping of Mg in the p-GaN layer because the gradient doping is able to decrease the Mg diffusion into an MQW active layer. The performance enhancement is also due to the reduction in undesirable carrier transition from the conduction band of the MQW to the acceptor level in the p-GaN:Mg layer. Altieri-Weimar et al. stated that the amount of magnesium (in the active layer for p-doping) and tellurium doping (in the n-doped layers for n-doping), as well as of the amount of oxygen incorporation, influence red-orange AlGaInP LED degradation [113]. The authors also reported that high stress aging temperatures over 85°C can accelerate the Te doped AlGaInP LED degradation.

During life tests, failure modes caused by dopant diffusion acting as nonradiative recombination center include the following: an increase in series resistance and/or forward voltage, which is accompanied by increased current crowding effects; an increase in the tunneling effect of forward diode current and reverse current; and degradation of optical intensity. The general failure mode is decreased light output. Instabilities in the p-type GaN layers as well as the growth of nonradiative recombination centers degrade emitted optical power. The primary causes of light degradation are current density, temperature, and current distribution affecting the increase in series resistance [95, 114–116].

3.4.4 Electromigration

Electromigration is electrically induced movement of the metal atoms in the electrical contact to the surface of the LED die due to momentum exchange with electrons. Inadequately designed LEDs may develop areas of lower and higher thermal resistance (and temperature) within the substrate due to defects, electromigration, or incomplete soldering. This leads to current crowding, causing thermal runaway, which results in severely increasing temperature in the package [92] and thus reducing the life of LEDs.

Electromigration causes contact migration between the electrical contact and surface of LED die, which leads to a short circuit. The driving force is either high

drive current or excessive current density. In sources with electrodes, degradation of the LED is due to the metal diffusing towards the inner region [82, 117]. During operation the metal will diffuse from the p-contact across the junction, creating spikes along with the direction of current flow. Electromigration of contact metals was along crystalline defects or defect tubes.

Kim et al. [118] showed the growth of a dot spot on the electrode surface due to electromigration, which consequently resulted in short circuit failure under various stress conditions. Their results showed the increase of forward and reverse leakage current after electrical stress, which was evidence of contact electromigration. Haque et al. [119] reported that materials selection having chemical compatibility should be considered to mitigate electromigration failures. Barton et al. [120] found that electromigration of contact metals in GaN-based blue LEDs was along crystalline defects or defect tubes. A degradation study by Barton et al. [121] on an InGaN green LED under high electrical stress found that the degradation was fast (about 1 s) when the pulsed current amplitude was increased above 6 A and 100 ns pulse width at a repetition rate of 1 kHz with a visible discharge between the p- and n-type electrodes. This led to the creation of shorts in the surface plane of the diode resulting in damage to metal contacts.

Proper thermal management and innovative package designs are required to solve electromigration. Thermal conductivities of interface materials, which constitute a large portion of the thermal resistance should be improved to prevent electromigration because contact resistances of the interface materials can affect mainly the overall thermal resistance. In addition, low thermal conductivity control at high ambient temperature must be taken into account in the design process.

3.4.5 Electrical Overstress-Induced Bond Wire Fracture/Wire Ball Bond Fatigue

Wire bonding is the most common method for connecting the pads on a chip to those on the LED packages. When LED packages are exposed to high forward currents or high peak transient currents, the bond wire can behave as a fuse [15]. Electrical overstress usually causes bond wire fracture, where the wire is instantly broken above the wire ball. This can cause catastrophic failure [122]. The severity of electrical overstress-induced bond wire fracture is related to the amplitude and duration of the electrical transients and the diameter of the bond (usually gold) wire [15]. Very long pulse duration of electrical transients and high DC forward current also result in thermomechanical stress-related failures. Long-term exposure to a high humidity environment can also result in bond wire fracture. When the quantity of absorbed water molecules within the epoxy encapsulant is of sufficient density to chemically attack the top electric contact on the LED die, the wire bond on the chip breaks the connection [123].

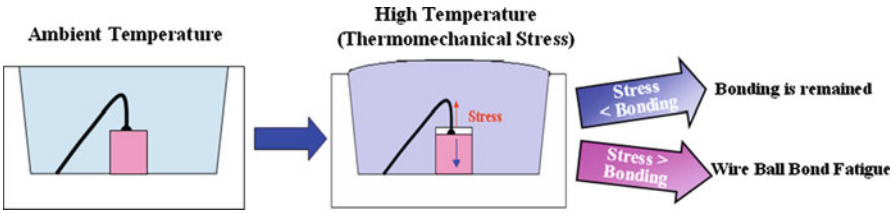


Fig. 3.22 Wire ball bond fatigue

Wire ball bond fatigue by thermomechanical stress is a type of wear-out failure mechanism. Repetitive, high-magnitude thermal cycles can lead to rapid failure. The thermal expansion of the encapsulant pulls the wire bond from the surface of the die [75, 92, 124]. Wire ball bond fatigue takes place when thermomechanical stress drives the repetition of thermal expansion and contraction of the expanding materials depicted in Fig. 3.22. A wire ball open occurs when the thermomechanical stress is higher than the wire ball bonding force. At elevated temperatures, the level of the thermal expansion coefficient and the Young's modulus of the encapsulant, as well as the hardness of the die, affects wire ball bond fatigue. The mismatch of coefficients of thermal expansion (CTEs) causes the wire bond and chip to generate a significant thermomechanical stress in the bonding zone. This results in fatigue crack propagation during thermal cycling. The reliability of such a joint varies with bond wire length and loop height [125].

Bonding process should be optimized by controlling wire type, pad metallization, and device configurations. Accurate bonding tests have to be performed by varying bonding parameters such as clamping force, power, and time matching bond pull strength to extract optimum bonding conditions. The chip damage under the bonding strength condition should also be minimized.

3.4.6 Electrical Contact Metallurgical Interdiffusion

Electrical contact metallurgical interdiffusion is caused by thermally activated metal–metal and metal–semiconductor interdiffusion [126, 127]. A schematic diagram of structure of an AlGaN/InGaN/AlGaN LED is illustrated in Fig. 3.23. Electrical contact metallurgical interdiffusion differs from electromigration in the sense that electrical contact degrades due to out-diffusion and in-diffusion of the electrical contact. On the other hand, electromigration is due to crystalline defects or defect tubes forming in the metal and where metal atoms accumulate. Continuous metallurgical interdiffusion involved with electrical contact degradation results in alloying and intermixing of the contact metals.

For example, in AuGe/Ni contact, nonstoichiometric regions are formed when Ga diffuses outward through the AuGe into the Au layer, while Au diffuses inward, forming high resistive alloying, which causes the contact resistance to increase [128].

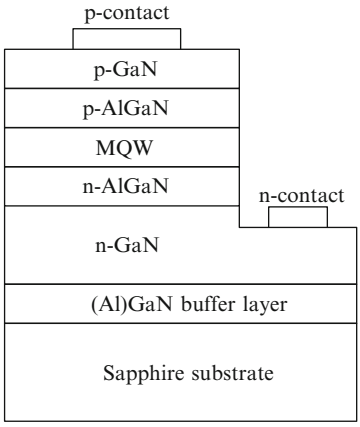


Fig. 3.23 Structure of GaN-based LED die

The failure modes of the electrical contact metallurgical interdiffusion of LED packages are light output degradation, an increase in parasitic series resistance, and short circuits of LEDs. The driving forces of failures are high drive current and high temperature increase.

Meneghesso et al. [79] stated that the long-term reliability of GaN/InGaN under DC-aged testing showed semi-transparent Ohmic contact degradation on top of the p-layer, which resulted in an increase in the parasitic series resistance and light output degradation. The increase in the parasitic series resistance induces increasingly harsh current crowding effects as the current increases during the tests. The values of the parasitic series were evaluated from the current–voltage curves. At high voltages under extreme DC-aging tests, an increase in the parasitic series resistance was found [81]. An electrothermal degradation study on InGaN LEDs by Pavesi et al. [95] also showed that LEDs electrically stressed at 100 mA without a heat sink experienced a decrease in light output up to 70%, after 500 h, with an increase in the series resistance and forward voltage as well as with the current crowding effects observed by emission microscopy. Meneghini et al. [129] analyzed the degradation of p-GaN contacts degraded under high-temperature storage at 250°C. High temperature storage induced a voltage increase and the nonlinearity of the electrical characteristics around zero voltage in *I–V* curves.

3.4.7 Electrostatic Discharge

Electrostatic discharge (ESD) is a type of failure mechanism resulting in rapid open circuit failure in LEDs (such as GaN-based diodes) with sapphire substrates, which are commonly used in blue, green, and white LEDs. The forward biased pulse (1 ns to 1 μs) usually passes through the LED without damage, but a reverse biased

pulse causes electrostatic discharge. Breakdown voltage and reverse saturation current are affected by contact material, thickness, defects in the substrate, and contamination [75, 123].

One possible solution is a correctly rated zener diode reverse biased in parallel with the LED [75, 130]. This device allows voltage spikes to pass through the circuit in both directions without damage to the LED. Another solution involving incorporating an internal GaN Schottky diode into the LED chips improves ESD characteristics of nitride-based LEDs [131, 132]. Inverse-parallel shunt GaN ESD diodes also improve the ESD reliability of GaN-based LEDs [133]. SiC substrates, GaN substrates, and Si substrates with high thermal resistance can also improve ESD robustness.

A sapphire substrate is electrically insulated. The p- and n-contacts are generally positioned on the same side. GaN/InGaN devices are easily damaged by electrostatic discharge and power dissipation because the sapphire substrate has low thermal resistance with the insulation effect [134, 136, 137]. Su et al. showed that an LED with a 1,040°C-grown p-cap layer endures ESD pulses up to 3.5 kV [134]. Their experiments demonstrated that ESD performances of LEDs are sensitive to V-shaped defects and bonding pad design. The forming of V-shaped pits on the p-GaN top layer is also related to the surface termination of threading dislocations [135]. These V-shaped pits cause a leakage path, which leads to worse electrostatic discharge (ESD) characteristics. The results of Tsai et al. [135] demonstrated that GaN-based LEDs with a high-temperature-grown p-GaN layer can withstand a negative electrostatic discharge voltage of up to 7 kV. Zhang et al. [136] reported that the fabricated flip-chip light-emitting diodes (FCLEDs) tolerated 10 kV ESD shock by embedding Zener diodes connected in parallel with the LED die. SiC substrate improved ESD robustness by reducing lattice mismatch in reverse bias conditions [137]. A modulation-doped $Al_{0.12}Ga_{0.88}N$/GaN superlattice improved ESD reliability in nitride-based LEDs by spreading pulse current when LEDs suffered from ESD [138].

3.4.8 Carbonization of the Encapsulant

Carbonization of the plastic encapsulation material on the diode surface under electrical overstress resulting in Joule heating or high ambient temperatures leads to the formation of a conductive path across the LED and subsequently to the destruction of the diode itself. Carbonization of the encapsulant decreases the encapsulant's insulation resistance, significantly inhibiting its ability to provide electrical insulation between adjacent bondwires and leads [139]. The loss in insulation resistance of the plastic combined with latch-up of the device at temperatures above threshold temperature (such as 200°C of high ambient temperature for plastic-encapsulated microcircuits) can initiate a thermal runaway process leading to carbonization of the encapsulant. In this process, fusing of the bondwires at high current causes the current to be shunted through the plastic, leading to Joule

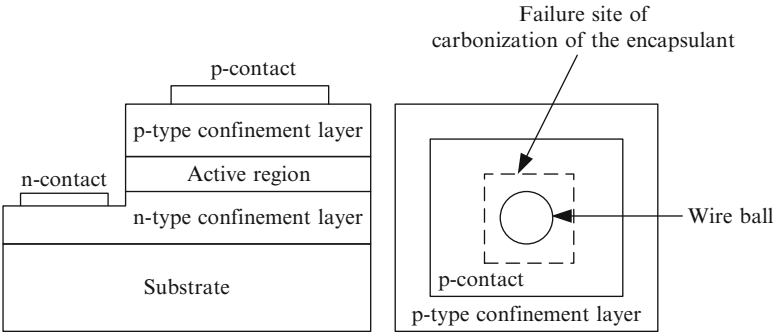


Fig. 3.24 Conceptual image of damaged area for carbonization of the encapsulant

heating of the plastic. This Joule heating further decreases the insulation resistance and can eventually result in carbonization of the encapsulant [140]. The failure mode of carbonization of the encapsulant is light output degradation. The failure site is shown in Fig. 3.24.

Failure analysis results for the degradation of single-quantum-well InGaN LEDs under high electrical stress indicate that the degradation process begins with carbonization of the plastic encapsulation material on the diode surface [126]. Meneghesso et al. reported that plastic carbonization was present along the bond wire, suggesting power or temperature-related encapsulant degradation, which could contribute to optical power degradation [141]. In the degradation process, the encapsulant packaging material burns and leaves a conductive carbon film on the die [142–144]. Several black spots detected on the p-contact layer of the LED die were burned plastic areas generated when the junction below them went into a nonconstant breakdown under high pulsed electrical stress. Continued stress started to create the conductive layer, forming a short circuit across the LED die. Further application of electrical stress caused catastrophic package failure.

Accurate fine-tuning of absolute maximum ratings of electrical current and ambient temperature for usage conditions as well as thermal management are required to avoid unexpected higher loads resulting in carbonization of the encapsulant.

3.4.9 Delamination

Repeated cycle stresses can cause material layers of LED packages to separate, causing significant loss of mechanical toughness. This causes delamination. Delamination can either occur between the die and silicone encapsulant [15], between the encapsulant and packaging lead frame [145], or between the LED die and die attach [146, 147], as shown in Fig. 3.25.

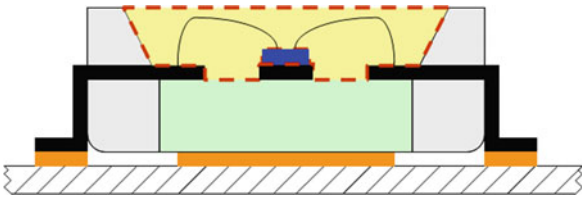


Fig. 3.25 Possible delamination areas of LEDs caused by repeated cycle stresses

The failure mode of delamination is decreased light output. When delamination occurs in thermal path, thermal resistance of the delamination layer is increased. The increased thermal resistance leads to increased junction temperature, which also affects many other failure mechanisms and ultimately reduces the life of LED packages. Delamination may also cause a permanent reduction in light output. Failure causes are thermomechanical stresses, moisture absorption, and/or interface contamination [5, 121, 144, 145, 148, 149]. Interface contamination during the LED package manufacturing process can result in poor adhesion of interfaces, which can initiate delamination.

LED packages are usually molded with polymer plastic materials. Mismatching coefficients of moisture expansion (CMEs) induce hygro-mechanical stress in LED packages and cause the LED packages to swell after absorbing moisture. Different levels of swelling occur between polymeric and non-polymeric materials as well as among the polymeric materials. This differential swelling induces hygroscopic stress in the package, thus adding thermal stress at high reflow temperatures inducing delamination [150]. The moisture presence in packages can reduce interfacial adhesion strength up to 40–60% and lead to delamination [144, 148]. The mismatching coefficients of thermal expansion (CTEs) in LED packages also induce thermal stress during the reflow soldering process. A high temperature gradient can cause delamination between the LED die and the encapsulant, which forms a thin chip–air–silicone interface inside the LED package [144].

Kim et al. reported that the die attach quality of Au/Sn eutectic bonding with low thermal resistance was better than that of Ag paste and solder paste, which have a higher thermal resistance [147]. Die attach discontinuities result in locally increased temperatures within a package [151]. Rencz et al. analyzed and detected die attach discontinuities by structure function evaluation, which is a useful method for measuring partial thermal resistance values. The highest increase in the *R*th value was detected when the voids were centrally located in the package [152]. Structure functions provide a map of the cumulative thermal capacitances of the heat flow path with respect to the thermal resistance from the junction to the ambient. The maximum value of the stress appears at the corner of the chip and die attachment. This stress led to interface delamination between the die and die attach. In most cases, the delamination begins from the corners (where the highest stress occurs) and then expands to other areas [153]. The combined effect of shear and peel stress on the delamination of an adhesive layer is experimentally known by the following relationship:

$$\left(\frac{\tau}{\sigma_{\mathrm{f}}}\right)^2 + \left(\frac{\sigma}{\sigma_{\mathrm{f}}}\right)^2 = 1, \tag{3.4}$$

where τ and σ are the shear and the peel stresses, respectively, at the interface, and σ_f is the combined failure stress for the interface [146].

Thermal transient measurements are usually performed to analyze the thermal behavior of delamination in LED packages [147, 148, 154–157]. From the derivative of the structure function, the differential structure is represented as a function of the cumulative thermal resistance [158]. In both of these functions, the local peaks and valleys indicate reaching new materials or changing surface areas in the heat flow path. A peak usually indicates the middle of a new region [147]. Thermal resistance increases with the degree of delamination. Bad bonding between the chip and other parts in LED packages can increase thermal resistance by as much as 14 times compared to a good bonding scheme across the chip surface area [159]. In the manufacturing process, a CTE mismatch between the bonding solder and bonded parts during temperature cycling causes delamination between the bonded surfaces. The curing of epoxy resins involves the repetition of shrinkage and the development of internal stress, which may also cause delamination [125].

Scanning acoustic tomography is a technique that is frequently used to detect delaminated areas in electronic packages. Driel et al. [160, 161] performed scanning acoustic microscope measurements to examine the occurrence of delamination in cavity-down TBGA package and exposed pad packages. In this technique, a sound wave is transferred through a device and any reflection (two-way) or time-delay (one-way) in the signal indicates a gap between two materials.

Nano-sized silica fillers around 25–50 nm are sometimes incorporated into encapsulant materials to minimize CTE mismatch and transmission loss as well as increase thermal conductivity [162]. Hu et al. presented thermal and mechanical analyses of high power LEDs with ceramic packages [153]. The advantages of ceramic packages replacing the plastic molds include high thermal conductivity, excellent heat endurance, the ability to withstand hazardous environments, flexibility for small and thin structures, enhanced reflectivity due to advanced surface-finishing technology, less CTE mismatch with the die, and high moisture resistance [163, 164]. Ceramic packages reduce thermal resistances from the junction to the ambient. As a result, ceramic packages lower delamination between interface layers in LED packages.

Proper selection of materials of LED package components with similar CTEs and CMEs is required to release thermomechanical stress and hygromechanical stress. Low CTE and modulus encapsulants, excellent adhesion, and CTE matching materials between the bonded surfaces are possible solutions for delamination. Also, thermal management from the die to the underlying leads of LED package should be improved by using large metal heat slug in the center of the bottom of LED packages or metal core printed circuit board (MCPCB) to perform more effective conduction path.

3.4.10 Encapsulant Yellowing

LEDs are encapsulated to prevent mechanical and thermal stress shock and humidity-induced corrosion. Transparent epoxy resins are generally used as an LED encapsulant. However, epoxy resins have two disadvantages as LED encapsulants.

One is that cured epoxy resins are usually hard and brittle owing to rigid cross-linked networks. The other disadvantage is that epoxy resins degrade under exposure to radiation and high temperatures, resulting in chain scission (which results in radical formation) and discoloration (due to the formation of thermo-oxidative cross-links). This is called encapsulant yellowing. Modification with silicone materials has been considered an efficient method to increase the toughness and thermal stability of transparent epoxy encapsulant resin. However, silicone compound as an LED encapsulant can have flaws, such as lower glass transition temperature (T_g), larger CTE, and poor adhesion to housing. Li et al. found that siloxane-modified LED transparent encapsulant is one possible way to improve the thermal mechanical properties, as the multifunctionality of siloxane compounds raises the cross-link density [165]. The increase of the cross-link density means that siloxane compounds improve the bond energy of the polymer chains to mitigate the chain scission.

The failure modes of encapsulant yellowing are decreased light output due to decreased encapsulant transparency and discoloration of the encapsulant. The basic cause is prolonged exposure to short wavelength emission (blue/UV radiation), which causes photodegradation, excessive junction temperature, and the presence of phosphor.

Photodegradation of polymer materials usually takes place under the following conditions: (1) by increasing the molecular mobility of the polymer molecule, which is made possible by raising the temperature above T_g and (2) the introduction of chromophores as an additive or an abnormal bond into the molecule, both of which have absorption maxima in a region where the matrix polymer has no absorption band [166]. Photodegradation depends on exposure time and the amount of radiation. Thus, even long-term exposure to visible light can cause polymer and epoxy materials to be degraded [166, 167]. Down [168] reported that light-induced yellowing was grouped with four distinct types of yellowing curves: linear, autocatalytic (where the amount and rate of yellowing increase with time), auto-retardant (where yellowing proceeds at a decreasing rate), and initial bleaching followed by a linear increase in yellowing. It is well known that many epoxies can turn yellow when subjected to prolonged exposure to ultraviolet (UV) light as well as levels of blue light, since band-to-band recombination in the GaN system can produce ultraviolet radiation [141]. Discoloration results in a reduction in the transparency of the encapsulant and causes a decrease in LED light output [169]. Further, it has been demonstrated that degradation and the associated yellowing increases exponentially with exposure energy (amount of the light illuminating the encapsulant).

The thermal effects associated with excessive junction temperature also plays a role in encapsulant yellowing [169, 170]. Narendran et al. [167] reported that the degradation rate of 5 mm epoxy-encapsulated YAG:Ce low-power white LEDs was mainly affected by junction heat and the amount of short wavelength emissions. It was shown that the thermal effect has greater influence on yellowing than does short-wavelength radiation. Furthermore, they demonstrated that a portion of the light circulated between the phosphor layer and the reflector cup and increased temperature, potentially causing epoxy yellowing. Yanagisawa and Kogima [78] also found that yellowing is not significantly affected by a high humidity test

environment. Baillot et al. stated that silicone coating degradation inside the encapsulant was observed at high temperature accelerated life test condition (30 mA/85°C/1,500 h) [171]. Barton and Osinski [172] also suggested that yellowing is related to a combination of ambient temperature and LED self-heating. Their results indicated that a temperature of around 150°C was sufficient to change the transparency of the epoxy, causing the attenuation of the light output of LEDs.

Down [173] carried out natural dark aging on various commercially available epoxy resin adhesives that were cured at room temperature in order to discuss resistance to thermal yellowing. The extent of yellowing was monitored by measuring the absorption of the wavelengths at 380 and 600 nm, as shown in (3.5). Yellowing curves are plots of average A_t (degree of yellowing) with time (t). According to Beer's law, the absorbance is directly proportional to the thickness of the sample being measured. The results were analyzed by using the following criteria during the yellowing acceptability evaluation test: epoxy samples with an absorbance of <0.1 mm were always perceived as acceptable in color, samples with absorbance greater than 0.25 mm were unacceptable in color, and uncertainty in color acceptability existed from 0.1 to 0.25 mm. In practical terms, the discoloring started visibly where the yellowing curve intersects 0.1 until it reaches 0.25. However, it was considered tolerably yellow from 0.1 to 0.25, which meant it was still acceptable.

$$A_t = [A(380\,\text{nm})_t - A(600\,\text{nm})_t] \times \frac{0.1\,\text{mm}}{F}, \tag{3.5}$$

where A_t is degree of yellowing observed at a specific time t and F is the average film thickness of each sample.

Although phosphor is a necessary component for producing white light, the presence of phosphor causes a decrease in reliability [170]. The phosphor is embedded inside an epoxy resin that surrounds the LED die. The phosphor converts some portion of the short wavelength light from the blue LED, and the combined blue light with the down-converted light produces the desired white light. When the phosphor is in direct contact with the die, as is the case for a phosphor-converted light emitting diode (pcLED), 60% of the phosphor emission is absorbed directly backward toward the chip. When the phosphor is not in contact with the die but away from the die, the loss is mainly from absorption by reflective surfaces and from light being trapped inside the diffused phosphor [174]. A package with lower concentration and higher phosphor thickness has a higher luminous efficacy (measured in units of lumens per watt of optical power) because the light extraction efficiency is lower with low phosphor concentrations [175]. Much research has been conducted relating different spatial phosphor distributions to reliability. Arik et al. [176] used finite element analysis to show that localized heating of the phosphor particles occurs during wavelength conversion because of low quantum efficiency. The authors reported that as little as 3 mW heat generation on a 20 μm diameter spherical phosphor particle can lead to excessive temperatures sufficient to degrade light output.

Thus, it is necessary to consider both photonics and thermal aspects to investigate how phosphor particles affect the encapsulant yellowing. The inclusion of phosphor into an LED package must be considered based on particle size, concentration, geometry, carrier medium, and refractive index matched with the encapsulant material [174, 175]. The geometry of the pcLED is usually divided into three classes: dispersed, remote, and local. A scattered photon extraction pcLED, which is a remote-type pcLED, is 61% more efficient than a conventional pcLED because the phosphor layer is separated from the die and backward-emitted rays are extracted from the sides of the optic structure inside the diffuse reflector cup of the package [174, 177]. Trapping by total internal reflection (TIR) and quantum conversion (QC) loss causes optical losses inside the phosphor layer. Kim et al. used remote phosphor distribution with a diffuse reflector cup to enhance light extraction efficiency [178]. Luo et al. [179] minimized the optical losses by utilizing a diffuse reflector cup, a remote-type phosphor layer, and a hemispherical encapsulant shape. Further, Allen and Steckl [174] found that the enhanced light extraction by internal reflection (ELiXIR) pcLED decreased the phosphor conversion loss by only 1%. This is a nearly ideal blue-to-white conversion obtained by internal reflection leading phosphor emissions away from the surface. This process utilizes a reflector material having high reflectivity and remotely located phosphors with a unity of quantum efficiency, a homogeneous refractive index to attenuate scattering, and a refractive index matching the encapsulant material to annihilate the total internal reflection. Li et al. reported that having fewer ZnO nanoparticles as particle fillers in a transparent epoxy matrix increases the high-visible light transparency and high-UV light shielding efficiency necessary for UV-WLEDs [180]. As can be seen in the works discussed above, enhancing light extraction efficiency was achieved by photonics and thermal consideration of the presence of phosphors in LED encapsulants.

Packaging material solutions are needed for further researches on encapsulant yellowing. UV transparent or silicone-based encapsulant will prevent photodegradation of encapsulants caused by UV radiation. Modified epoxy resins or silicone-based encapsulant and low thermal resistance substrate are useful to minimize thermal degradation of encapsulants induced by high junction temperature between LED die and leads. High refractive index encapsulant, efficient encapsulant and cup design, high phosphor quantum efficiency will solve refractive index mismatch between LED die and the encapsulant to improve light extraction efficiency.

3.4.11 Lens Cracking

The encapsulant and lens materials of LEDs are generally required to contain the characteristics of high transparency, high refractive index, chemical stability, high temperature stability, and hermeticity to enhance the extraction of light into free space as well as reliability performance [181]. High power LEDs use a plastic lens as well as an encapsulant, as shown in Fig. 3.26 [181]. Since standard silicone

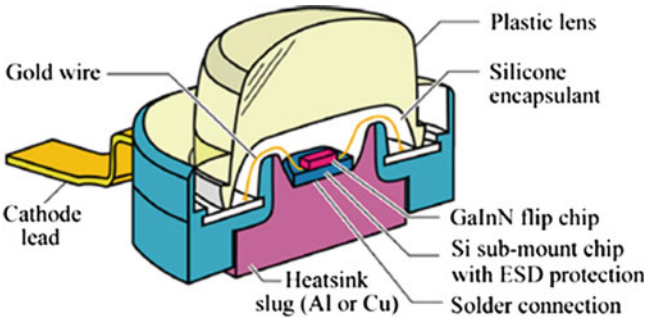


Fig. 3.26 Cross-sectional view of high power LED package [181] (© Cambridge University Press), reprinted with permission

retains mechanical softness in its cured state, the silicone encapsulant is enclosed in a plastic cover that serves as a lens to give mechanical protection. The plastic lenses also serve to increase the amount of light emitted from the LEDs into free space. The failure mode of lens degradation is a number of small hairline cracks that decrease light output due to increased internal reflection of LEDs. The degradation appears due to thermomechanical stresses, hygromechanical stresses, and poor board assembly processing.

Lens cracking depends on the material properties of plastics. All encapsulants and lenses in LEDs are based on polymers such as epoxy resins, silicone polymers, and polymethylmethacrylate (PMMA) [1, 3, 14, 122, 181]. Hsu et al. [182] found a number of cracks introduced from thermal expansion in the center of the lens surface and on the inside of the polymer encapsulation when high power LED samples with three different lens shapes were aged at 80, 100, and 120°C under a constant voltage of 3.2 V. They used LEDs with hemispherical, cylindrical, and elliptical shapes. The hemispherical lens LEDs had longer lives than the cylindrical- and elliptical-shaped plastic lenses due to a more uniform thermal dissipation along the thermal path from the LED chip to the lens. It was also reported that long-term exposure to high condensing moisture caused cloudiness of the epoxy lenses in a plastic LED lamp due to hygromechanical stresses [123]. Lumileds also reported that extreme thermal shock can crack an epoxy lens, since temperature variations in LEDs induce mechanical stress [15]. Poor PC board assembly processing causing cracked plastic domes were revealed during an electrical test when trying to bend lamps into position after soldering. The bending stresses in the lead frames were transmitted to the encapsulating epoxy, causing the epoxy to crack [123].

Further research should be focused on selection of lens materials and efficient lens/cup design to minimize the thermomechanical stress and the hygromechanical stress. There is a need to improve a quality control by reliability evaluation and acceleration life tests to avoid lens cracking.

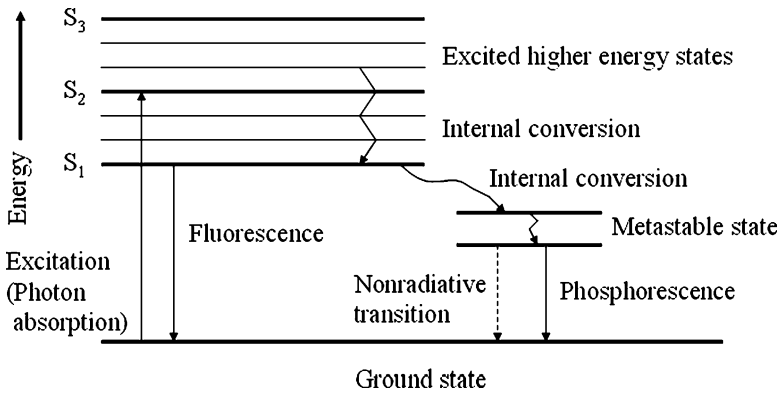


Fig. 3.27 Fluorescence vs. phosphorescence

3.4.12 Phosphor Thermal Quenching

Phosphor thermal quenching decreases light output with the increase of the nonradiative transition probability due to thermally driven phosphorescence decay. Phosphor thermal quenching means that the efficiency of the phosphor is degraded when temperature rises. White LEDs are usually phosphor-converted LEDs (pcLEDs) that utilize short wavelengths emitting from LED dies to excite phosphors (luminescent materials) spread over the inside of the encapsulant. Phosphors emit light with longer wavelengths and then mix with the remains of the diode light to produce the desired white color. Phosphorescence has a longer emission pathway (longer excited state lifetime) than fluorescence, as shown in Fig. 3.27. Phosphorescence decay is temperature dependent, while fluorescence decay is independent of temperature.

It is generally required that phosphors for white LEDs have low thermal quenching by a small Stokes shift to avoid changes in the chromaticity and brightness of white LEDs [183]. The types of white LEDs are class D (daylight), class N (neutral white), class W (white), class WW (warm white), and class L (incandescent light bulb). Phosphors used in white LEDs are generally divided into sulfides, aluminates, nitrides, and silicates. The phosphors used in LEDs are generally required to have the following characteristics: high absorption of UV or blue light; high conversion efficiency; high resistance to chemicals, oxygen, carbon dioxide, and moisture; low thermal quenching; small and uniform particle size (5–20 μm); and appropriate emission colors [184]. Most oxide-based phosphors have low absorption in the visible-light range, which means that they cannot be coupled with blue LEDs. Sulfide-based phosphors are thermally unstable and very sensitive to moisture, and they degrade significantly under ambient conditions without a protective coating layer. Xie and Hirosaki further assert that silicon-based oxynitride phosphors and nitride-based phosphors have a broad excitation band extending from the ultraviolet to the visible-light range and also the ability to strongly absorb blue-to-green light [184].

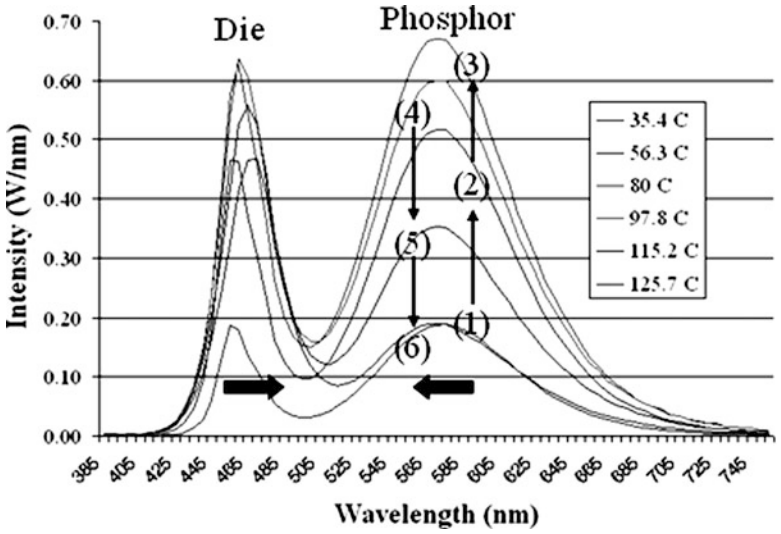


Fig. 3.28 Spectra change with temperature rise

Failure modes resulting from phosphor thermal quenching include a decrease in light output, color shift, and the broadening of full width at half maximum (FWHM). The driving forces are high drive current and excessive junction temperature, which are attributed to increases in temperature of the inside of the package [121].

With increasing temperature, the nonradiative transition probability increases due to thermal activation and the release of the luminescent center through the crossing point between the excited state and the ground state [185]. This quenches the luminescence. Jia et al. demonstrated that a blue shift and spectral broadening with increasing temperature indicate temperature-dependent electron–phonon interaction [186]. The temperature dependency of phosphor thermal quenching is described in Fig. 3.28. Light output degradation begins to occur after lead temperature of 80°C (3.3) for high power LEDs. Upon heating, the broadening of FWHM is caused by the phosphor thermal quenching (3.4)–(3.6). A slight blue shift of the emission band is observed for phosphors as the temperature increases. The shift of die peak wavelength to a lower energy is due to the junction temperature dependence of the energy bandgap shrinkage. The thermal quenching process was caused by either a multiple phonon relaxation process or a thermal ionization of doped material as a part of a trapping mechanism that produced long persistent phosphors. Less lattice phonon energy is favored for reducing a thermal quenching process. For persistent phosphors, activators are supposed to be ionized by one photon to produce trapped electrons. The electrons need thermal energy to be ionized when the electronic excited state is below the conduction band. This process is called thermal ionization, and it requires the electron energy level to be close to the host conduction band. When thermal ionization processes exist, thermal quenching is more severe because a large number of electrons are trapped. This cause light output degradation and color change.

Xie et al. [187] used the Arrhenius equation to fit thermal quenching data in order to understand the temperature dependence of photoluminescence and determine the activation energy for thermal quenching:

$$I(T) = \frac{I_o}{1 + c \times \exp\left(\frac{-E}{kT}\right)}, \tag{3.6}$$

where I_o is the initial intensity, I(T) is the intensity at a given temperature T, c is a constant, E is the activation energy for thermal quenching, and k is Boltzmann's constant. They found the most appropriate value of the activation energy, E, to be 0.23 eV for α-sialon:Yb^{2+} and 0.20 eV for $Sr_2Si_5N_8$:Eu^{2+}.

Research for improving reliability and design of LED packages has been conducted to minimize quantum conversion loss caused by phosphor thermal quenching. Current research is focused on solving phosphor thermal quenching related to enhance quantum conversion efficiency for long-term reliability by utilizing and on developing new phosphor materials generating white lights mixed with colors of LED dies.

One-pcLEDs have been commercially available using a blue LED and yttrium aluminum garnet doped with Ce^{3+} (YAG:Ce^{3+}) to produce white light by combining blue LEDs with yellow-emitting phosphors [188, 189]. The conventional YAG:Ce^{3+} white LED has a low color rendering index (CRI) both because it lacks a red component and because it faces problems of high thermal quenching and narrow visible range [190]. Better light quality was shown to be obtained by using a combination of a Ce^{3+} doped garnet phosphor with a red emitter [191, 192]. Two-pcLEDs using a combination of red and green phosphors with blue LEDs were studied [192]. The two phosphors absorbed the blue light from the InGaN chip and converted it into green and red light, and then white light was produced by color mixing. Three-pcLEDs using a combination of red, green, and blue phosphors with UV LEDs were demonstrated by Mueller and Mueller-Mach [193]. Color mixing of red, green, and blue phosphors improved the color rendering and produced a wide range of color temperatures. Critical key values judging the quality of white light produced by pcLEDs are known as the color rendering index (CRI) and the correlated color temperature (CCT) [194]. CRI $>$ 80 is regarded as good; in the 1970s it was regarded as plain or acceptable [192, 194].

Mueller-Mach et al. [194] presented a 2-pcLED based on phosphors of Sr_2SiN_8:Eu^{2+} (nitridosilicates, red) and $SrSi_2O_2N_2$:Eu^{2+} (oxonitridosilicates, green) excited by blue InGaN/GaN LEDs. These showed a wide range of CCT and good CRI with a low thermal quenching. Uheda et al. [195] found that red phosphor, $CaAlSiN_3$:Eu^{2+}, is more efficient than La_2O_2S:Eu^{3+} or $Ca_2Si_5N_8$:Eu^{2+} under 460 and 405 nm excitation and is chemically stable as well, so that it produces high efficient red-emitting phosphors excited by blue or violet LEDs. Xie et al. reported that Eu^{2+}-activated Li-α-SiAlON is a good greenish yellow phosphor for pcLEDs [185, 187]. Jia et al. [186] showed that phosphors of $SrMgSi_2O_6$ and $Sr_2MgSi_2O_7$ doped with Eu^{2+} blue emission were enhanced by codoping trivalent rare earth ions, such as Nd^{3+}. Li et al. [196] showed that the red emitting $Sr_2Si_5N_8$:Eu^{2+} has a quantum

efficiency of 75–80% and a very low thermal quenching up to 150°C. Xie et al. [197] found that (oxy)nitride phosphors in the system of M–Si–Al–O–N showed high conversion efficiency of blue light, suitable emission colors, and little thermal quenching. Xie et al. further reported that a synthetic route to $Sr_2Si_5N_8:Eu^{2+}$-based red nitridosilicate phosphors showed orange-red emission and high quantum efficiency with very low thermal quenching [198]. Zeng et al. [199] demonstrated that $Ba_5SiO_4Cl_6:Eu^{2+}$ phosphors under 405 nm excitation exhibit an intense blue emission with a peak wavelength at 440 nm more than 220% compared to conventional $BaMgAl_{10}O_{17}:Eu^{2+}$.

Further research on phosphor thermal quenching is required to enhance and to maintain light extraction efficiency by optimizing material, size, concentration, and geometry of phosphor particle to minimize temperature rise of the inside of LED packages as well as by thermal design improvement of LED packages and boards to dissipate internal heat of LED packages through boards to outer environment.

3.4.13 Solder Joint Fatigue

LED packages are usually bonded to a ceramic (AlO), metal (MCPCB), or organic (FR4) PCB using a solder. The solder may fatigue and may lift-off and/or degrade. Failure modes and their mitigation of solder joint fatigue are associated with degradation of electrical connections (solder joints) as well as degradation of LEDs with time. Degradation of electrical connections increases forward voltage. Thermomechanical fatigue is not a major issue of chip-on-board packaged LEDs where the chip is directly wirebonded to circuit board [200]. In case of the chip-on-board package, the critical factor for long-term reliability is degradation of LED itself and not that of the board level interconnects. On the other hand, in a rigid SMT submount (typically ceramic, LCP, or PMMA) type package, the solder interconnects go through stress reversals due to the CTE mismatch between LED package and circuit board [201] resulting in thermomechanical fatigue of the solder joint. Therefore, critical factors for long-term reliability for submount packages include thermomechanical fatigue of solder joints as well as LED degradation.

The failure mechanism could be fatigue due to deformation in response to applied mechanical stresses, cyclic creep and stress relaxation, fracture of brittle intermetallic compounds, or combinations thereof [202]. During temperature changes, shear is the primary stress on solder joints. As a result, the surfaces of solder joints slide relative to one another during thermal cycling, producing electrical transients that are typically of short duration [203]. Failure causes of solder joint fatigue of LEDs are CTE mismatch between package and circuit board, the geometry of the package (i.e., length scale over which stress is transmitted), solder joint material and thickness, temperature swings and dwell time, modulus and thickness of circuit dielectric, and thermal resistance of the dielectric [200, 204]. Chang et al. [204] stated that interconnect reliability between high power LED packages and aluminum metal core printed circuit board depends on the magnitude

of the temperature swing, dwell time, electrical power of LED packages, and board design (with or without the active cooling device). The obtained simulation results showed that high temperature swing resulted in shorter cycles to failure. Longer dwell times reduced reliability. Higher electrical power of LEDs accelerate interconnect failures on solder joints. The active cooling device improves the cycles to failure and makes them longer than passive cooling methods [204]. In most cases of high power LEDs, the metal heat slug located in the center of the LED package provides a mechanical connection and a thermal path to the PCB. The total effective solder joint area increases and cyclic temperature excursion decreases due to the solder joint.

The reliability of solder interconnects is influenced by environmental loads, solder material properties, and the intermetallics formed within the solder and the metal surfaces where the solder is bonded [205, 206]. Osterman and Pecht demonstrated that the Coffin-Manson fatigue life relationship is a good model for estimating fatigue life of slider interconnects early in the design process [207]. The Engelmaier interconnect fatigue life model was developed as an improvement upon inelastic strain range-based Coffin-Manson model. The Engelmaier model provides a first-order estimate of cycles to failure for solder interconnects under power and thermal cycles. However, the Engelmaier model does not consider the local CTE and possible variations such as thermal cycle temperature ranges and different stress levels that a solder joint experience. Also, the Engelmaier model does not take into account any elastic deformation and are mainly applicable to the ceramic interconnect boards [208]. Intermetallic compounds are formed while metal component terminals, board pad finishes, and base board metals react. The growth of intermetallic compounds causes solder to become brittle and results in solder joint failure [206].

LED packages, particularly high power LED packages, are nonstandard compared with other semiconductor and passive parts. For example, the metal heat slug located in the center of the high power LED package under evaluation provided a mechanical connection and a thermal path to the aluminum MCPCB. Chang et al. [204] reported that the total effective solder joint area increased and cyclic temperature excursion decreased due to this solder joint. There are many versions of heat sink materials and shapes for which simulation tools and techniques are not well developed [209].

3.5 Relationship Between the Failure Causes and Associated Mechanisms

Based on the findings from Sect. 3.4, the causes of LED failure can be categorized as extrinsic and intrinsic causes. For example, prolonged exposure to UV, high current, poor assembly, and moisture ingress can be categorized as extrinsic causes of LED failure [148, 210–216]. To avoid extrinsic failures, it is necessary to

exercise control of environmental conditions and fine tune the manufacturing/assembly process, which are achievable goals. However, improving reliability by overcoming intrinsic causes is more challenging, as it requires a complete understanding of the root causes of failures and associated failure mechanisms and as a result hard to overcome. Hence, it is necessary to understand the causes of failure, failure modes, and associated failure mechanism(s). Based on exhaustive literature review and research performed by CALCE, this chapter lays foundation for such understanding. For example, delamination is one of the dominant mechanisms responsible for the failure of LEDs. One type of delamination involves detachment of encapsulant from the LED package. As mentioned earlier, the reduction in light output forms the failure criteria and not catastrophic failure, unlike other electronic components. As can be seen in Table 3.3, there can be two effects on a device—thermomechanical stress and hygromechanical stress—that are responsible for initiating delamination, which can result in reduced light output over a period of time. Table 3.3 summarizes the relationships between various failure sites and the associated causes, effects on devices, failure modes, and failure mechanisms. However, new research and further field experience with LEDs confirming is necessary to continue to update the interrelationships shown in the table.

3.6 Challenges in LED Reliability Achievement Due to Lack of Thermal Standardization

When a higher drive current is applied to LEDs, there is increased light output but that typically comes with increased heat generation. The light output can change as a result of the operating conditions, temperature in particular [217–223] which is impacted by heat generation and depends on the methods of dispersion of the heat. For example, light output decreases with a temperature rise in the LEDs, since the quantum efficiency decreases at higher temperature that contributes to more nonradiation recombination events in LEDs [224]. Temperature increase is also related to forward voltage drop due to the decrease of the bandgap energy of the active region of LEDs and also due to the decrease in series resistance occurring at high temperatures. The resistance decrease is due to higher acceptor activation occurring at elevated temperatures as well as the resulting higher conductivity of the p-type layer and active layers. In addition to the quantum efficiency drop, the colors of LEDs also change with increased temperature. In particular, phosphor-converted LEDs with blue InGaN and yellow phosphors experience light output degradation, which causes shifts of blue peak wavelength and the peak energy of the phosphors when the temperature of the LEDs increases. The shifts of the blue peak wavelength toward longer wavelengths having lower energy (i.e., redshifting) are due to the junction temperature dependence of the energy gap shrinkage and quantum confined Stark effect, a process which reduces energy of bound states in a quantum well under an applied electric field [225]. On the contrary, the shifts of the

Table 3.3 Failure sites, causes, effects, modes, and mechanisms of LEDs

Failure site	Failure cause	Effect on device	Failure mode	Failure mechanism
Semiconductor (die)	High current-induced Joule heating	Thermomechanical stress	Lumen degradation, increase in reverse leakage current, increase in parasitic series resistance	Defect and dislocation generation and movement
	High current-induced Joule heating High ambient temperature Poor sawing and grinding process	Thermomechanical stress	Lumen degradation	Die cracking
	Poor fabrication process of p–n junction High current-induced Joule heating High ambient temperature	Thermal stress	Lumen degradation, increase in series resistance and/or forward current	Dopant diffusion
	High drive current or high current density	Electrical overstress	No light, short circuit	Electromigration
Interconnects (bond wire, ball, and attachment)	High drive current/high peak transient current	Electrical overstress	No light, open circuit	Electrical overstress-induced bond wire fracture
	Thermal cycling induced deformation Mismatch in material properties (CTEs, Young's modulus, etc.)	Thermomechanical stress	No light, open circuit	Wire ball bond fatigue
	Moisture ingress	Hygromechanical stress		
	High drive current or high pulsed/transient current High temperature increase	Electrical overstress Thermal stress	Lumen degradation, increase in parasitic series resistance, short circuit	Electrical contact metallurgical interdiffusion
	Poor material properties (e.g., poor thermal conductivity of substrate)	Thermal resistance increase	No light, open circuit	Electrostatic discharge
	High voltage (reverse biased pulse)	Electrical overstress		

(continued)

Table 3.3 (continued)

Failure site	Failure cause	Effect on device	Failure mode	Failure mechanism
Package (encapsulant, lens, lead frame, and case)	High current-induced Joule heating High ambient temperature	Electrical overstress	Lumen degradation	Carbonization of the encapsulant
	Mismatch in material properties (CTEs and CMEs) Interface contamination	Thermomechanical stress	Lumen degradation	Delamination
	Moisture ingress	Hygromechanical stress		
	Prolonged exposure to UV	Photodegradation	Lumen degradation, color change, discoloration of the encapsulant	Encapsulant yellowing
	High drive current induced Joule heating High ambient temperature Presence of phosphor	Thermal stress		
	High ambient temperature Poor thermal design	Thermomechanical stress	Lumen degradation	Lens cracking
	Moisture ingress	Hygromechanical stress		
	High current-induced Joule heating High ambient temperature	Thermal stress	Lumen degradation, broadening of spectrum (color change)	Phosphor thermal quenching
	Mismatch in material properties/ thermal cycling-induced high temperature gradient	Mechanical stress Cyclic creep and stress relaxation Fracture of brittle intermetallic compounds	Lumen degradation, forward voltage increase	Solder joint fatigue

blue peak wavelength toward shorter wavelengths having higher energy (i.e., blue shifting) are due to band filling, a process which results from the injection of holes via tunneling into an empty impurity band and vacant valence band [226]. The peak energy shifts of the phosphors are due to phosphor thermal quenching. To sum up, many important reliability-related features of LEDs are functions of temperature.

As an example, the long-term stability and lifetime of LEDs are typically judged on the basis of measured light output. The measured light output mostly depends on the junction temperature. Hence, the correctness of light output measurements is dependent on the temperature stability of the light output measurement setup and by the accuracy of the temperature measurement is complicated, and there are associated uncertainties with prediction of the junction temperature because there are only indirect ways of measuring and converting temperatures from reference points to the junction temperature. Long-term stability analyses of LEDs need to demonstrate that the thermal conditions of the LEDs have not changed during the entire aging/testing process in order to enable correct correlation between light output characteristics and $R\text{th}_{\text{J-A}}$ (thermal resistance between LED junction to ambient). Little information has been published about how the light output measurements in reliability studies are performed, but it is suspected that the current $R\text{th}_{\text{J-A}}$ of the LEDs during aging test measurements is often uncontrolled and changes over time. As a consequence, some of the reported light output variations could be attributed to $R\text{th}_{\text{J-A}}$ variations of the test setup. One way to prevent this is to eliminate the potential changes in $R\text{th}_{\text{J-A}}$ by ensuring that all light output characteristics are presented as a function of the real junction temperature. The only way that the reliability data provided by different vendors can be assured is by standardizing all relevant measurements and definitions.

Besides the standardization of reliability-related tests, an important source of information for a designer is the published data in the data sheets, especially thermal data such as junction-to-ambient and junction-to-case thermal resistances. The designer needs these data to ensure that the maximum allowable temperatures prescribed by the vendors are not exceeded. It is necessary for these data to be standardized, because lower thermal resistance is a major selection criterion. Lasance and Poppe [227–230] and Poppe et al. [231] discuss the need for more sophisticated thermal characterization and standardization of LEDs and LED-based products. The reason is that progress in these fields has not kept pace with the exponential growth in applications. This situation is becoming a serious problem for leading manufacturers who are focusing on a sustainable business for the future and are willing to publish reliable thermal data. Unfortunately, due to the lack of globally accepted standards, manufacturers can publish whatever they want. The lack of standards also becomes a problem for the experienced user because the thermal data that are published are often of limited use in practice when accuracy is at stake, and accuracy is needed for estimation of expected performance and lifetime. Remarkably, the situation is not much different from the one that the IC-world was facing almost 20 years ago [231–236]. Around 1990 it became clear that thermal characterization of IC packages was problematic. Manufacturers all over the world were using different standards. Even within a single manufacturer,

intolerable differences showed up. To solve the thermal characterization problems, manufacturers must publish thermal data in such a way that the end user can use this data. End users are responsible for the specifications of the thermal environment to which the LEDs are exposed. Provided that the manufacturers want to cooperate, it would be easy to apply the standard protocols used by IC business.

In addition to standardization itself and suggestions for improved test setups, Poppe and Lasance discussed [227–230] the role of thermal characterization, the definition of thermal resistance, the different goals of manufacturers and system designers, the similarities and differences between LED and IC thermal characterization, the drawbacks of the current thermal data in data sheets, and an overview of the questions that an LED thermal standardization body should address.

3.7 Conclusions

The conventional way to predict the lifetime of LEDs employs the Arrhenius model to extrapolate test results at high temperature to expected operating temperatures. The Arrhenius model as given in (3.1) is not adequate to represent the failures of LEDs. Light output degradation is the major failure mode of LEDs, and it results from hygromechanical and electrical stresses in addition to thermal stresses. A more realistic method of LED lifetime estimation needs to reflect total consideration of temperature, the level of forward current, relative humidity, mechanical stress, and materials. The coverage of this chapter will help both develop reliable product design for industry and provide researchers guidelines for addressing issues related to LED reliability.

Thermomechanical stress, electrical overstress, and hygromechanical stress are the most dominant failure causes of LEDs. The literature available on the testing of LEDs shows that extensive accelerated tests have been performed not only for academic interest but also by agencies dealing in commercial aspects of LEDs. Reliability tests have been used to claim that the typical life of LEDs can be expected to range from 3,000 h for LEDs operating in harsh environments (in terms of high current, high temperature, and high humidity) to 50,000 h in benign environments. For example, LEDs running with the absolute maximum rating of current at high temperature over 85°C and high humidity over 85% might have the worst lifetime among different usage conditions. The higher estimate for LED life is in benign conditions below room temperature and below typical current operation. The overall reliability of LED packages is related to interconnect failures, semiconductor failures, and package failures. Interconnect failures are responsible for broken bond wire/lifted ball, electrical metallurgical interdiffusion, and electrostatic discharge. LED semiconductor failures are manifested as die cracking, defect and dislocation generation and movement, dopant diffusion, and electromigration. Package failures involve mechanical interaction with LED chips, die adhesives, heat slugs, lead frames, and encapsulants. The failure mechanisms responsible for

package failures include carbonization of the encapsulant, delamination, encapsulant yellowing, phosphor thermal quenching, and lens degradation.

Based on our research, we found several design issues on which there is a consensus among researchers. Examples are following: (1) it is necessary to control die cracking by fine-tuning thermal expansion coefficients between the substrate and epitaxial layers. The growth of optimal medium layer between the substrate and the epitaxial layer is a key technology to prevent the die cracking; (2) ESD resistance can be improved by a correctly rated zener diode reverse biased in parallel with the LED and by incorporation of an internal GaN Schottky diode into the nitride-based LEDs. Inverse-parallel shunt GaN ESD diodes also improve the ESD reliability of GaN-based LEDs; and (3) it is imperative that all vendors use globally accepted thermal standards to determine junction temperature to enable a fair comparison between different products, including agreed upon definitions of power and thermal resistance.

We identified the following areas of research and development to ensure that the demand for high reliability and high performance LEDs can be met by the industry while meeting the Green promises. An improved understanding of the root causes responsible for failures in LEDs with respect to improving material properties and fabrication technology must be developed. To address manufacturing processes, a deeper understanding of various process variables and associated environments critical for LED quality must form part of LED reliability research.

1. Future research on defect and dislocation generation and motion needs improved structural and material design of LED die and internal thermal management handling thermal resistance from junction to the package to reduce formation of crystal defect and dislocation movement caused by high current-induced thermal effect and high ambient temperature.
2. Proper thermal management and innovative package designs are required to solve electromigration. Thermal conductivities of interface materials, which constitute a large portion of the thermal resistance should be improved to prevent electromigration because contact resistances of the interface materials can affect mainly the overall thermal resistance. In addition, low thermal conductivity control at high ambient temperature must be taken into account in the design process.
3. Bonding process should be optimized by controlling wire type, pad metallization, and device configurations. Targeted bonding tests have to be performed by varying bonding parameters such as clamping force, power, and time matching bond pull strength to extract optimum bonding conditions. The chip damage under the bonding strength condition should also be minimized.
4. There is a need to the development of new materials of LED package components with similar CTEs and CMEs to release thermomechanical stress and hygromechanical stress. Low CTE and modulus encapsulants, excellent adhesion, and CTE matching materials between the bonded surfaces are possible solutions for delamination. Also, thermal management from the die to the underlying leads of LED package should be improved by using large metal

heat slug in the center of the bottom of LED packages or metal core printed circuit board (MCPCB) to perform more effective conduction path.

5. Packaging material solutions are needed for further researches on encapsulant yellowing. UV transparent or silicone-based encapsulant will prevent photodegradation of encapsulants caused by UV radiation. Modified epoxy resins or silicone-based encapsulant and low thermal resistance substrate are useful to minimize thermal degradation of encapsulants induced by high junction temperature between LED die and leads. High refractive index encapsulant, efficient encapsulant and cup design, and high phosphor quantum efficiency will solve refractive index mismatch between LED die and the encapsulant to improve light extraction efficiency.
6. Further research should be focused on selection of lens materials and efficient lens/cup design to minimize the thermomechanical stress and the hygromechanical stress. There is a need to improve a quality control by reliability evaluation and acceleration life tests to avoid lens cracking.
7. Further research on phosphor thermal quenching is required to enhance and to maintain light extraction efficiency by optimizing material, size, concentration, and geometry of phosphor particle to minimize temperature rise of the inside of LED packages as well as by thermal design improvement of LED packages and boards to dissipate internal heat of LED packages through boards to outer environment.
8. Further research is required to investigate (numerical) lifetime prediction methods for the observed failure modes. The majority of LED packages and systems are not well understood. Numerical prediction techniques will better facilitate our understanding of them. To achieve the goal of the remaining useful life estimate in operation, prognostic and health management (PHM) techniques are necessary. In situ monitoring can explain how the maintenance of each test parameter changes in real-time without increasing the time and the number of test operators.
9. Failure analysis of LEDs has been performed through conventional microelectronics failure analysis approaches and off-line analysis techniques. There is a need to develop advanced failure analysis techniques for LEDs. This includes, for example, nondestructive analyses of semiconductor, interconnect, and package failures of LEDs and in-line (event) detection methods for lumen degradation.

Cooperation between thermal, electrical, and optical standards bodies and professional societies is required to arrive at globally accepted thermal standards to measure junction and reference temperatures to ensure a fair comparison of published performance and reliability data. Since the end user needs total reliability of the final products, reliability research of LED packages has to be expanded to the reliability study of the complete LED-based system, including the luminaires and electronics. Failure mechanisms to cause catastrophic failure (i.e., die cracking, electromigration, electrical overstress-induced-bond wire fracture, wire ball bond fatigue, electrostatic discharge, and carbonization of the encapsulant) as well as degradation mechanisms (defect and dislocation generation and movement, dopant

diffusion, electrical contact metallurgical interdiffusion, delamination, encapsulant yellowing, lens cracking, phosphor thermal quenching, and solder joint fatigue) should be considered for system-level life prediction that can accommodate long-term regional operating conditions.

If the industry keeps its focus only on performance improvement and offering new functionality, the promise of LEDs may die with low level of adaptation. Even when prices come down and LEDs penetrate consumer markets like home light bulb or flashlights, customers would like a safe and durable product. Large-scale municipal, business, and industrial applications need to have promise of long life but also need to give the users ability to know the remaining life.

There is a need to acquire knowledge of LED's life cycle loading conditions, geometry, and material properties to identify potential failure mechanisms and estimate its remaining useful life. The PoF approach considers qualification as an integral part of design and development and involves identifying root causes of failure and developing qualification tests that focus on those particular issues. PHM-based-qualification combined with the PoF qualification process can enhance the evaluation of LED reliability in its actual life cycle conditions to assess degradation, to detect early failures of LEDs, to estimate the lifetime of LEDs, and to mitigate LED-based-product risks. Determination of aging test conditions better designed with PHM-based qualification enables more representation of the final usage conditions of the LEDs.

References

1. Krames MR, Shchekin OB, Mueller-Mach R, Mueller GO, Zhou L, Harbers G, Craford MG (2007) Status and future of high-power light-emitting diodes for solid-state lighting. J Display Technol 3(2):160–175
2. Steigerwald DA, Bhat JC, Collins D, Fletcher RM, Holcomb MO, Ludowise MJ, Martin PS, Rudaz SL (2002) Illumination with solid state lighting technology. IEEE J Select Top Quant Electron 2:310–320
3. Steranka FM, Bhat J, Collins D, Cook L, Craford MG, Fletcher R, Gardner N, Grillot P, Goetz W, Keuper M, Khare R, Kim A, Krames M, Harbers G, Ludowise M, Martin PS, Misra M, Mueller G, Mueller-Mach R, Rudaz S, Shen YC, Steigerwald D, Stockman S, Subramanya S, Trottier T, Wierer JJ (2002) High power LEDs—technology status and market applications. Phys Stat Sol (a) 194:380–388
4. Schubert EF, Kim JK, Luo H, Xi J-Q (2006) Solid-state lighting—a benevolent technology. Rep Prog Phys 69:3069–3099
5. Aoyama Y, Yachi T (2008) An LED module array system designed for streetlight use. In: IEEE Energy 2030 Conference, Energy 2008, Atlanta, GA, pp 1–5
6. Vittori R, Scaburri A (2009) New solid state technologies and light emission diodes as a mean of control and lighting source applicable to explosion proof equipment, with the scope to reduce maintenance, to limit the risk of bad maintenance and to expand the plants' life. In: PCIC Europe, 2009 Conference Record, Europe, pp 193–198
7. King M (2010) Characteristics of high brightness LEDs. In: Electronic design online conference series, session 5, 22 Jun 2010, pp 1–16

8. Schubert EF (2006) Light-emitting diodes, 2nd edn. Cambridge University Press, Cambridge, pp 308–309 (Chapter 18)
9. Huang M-S, Hung C-C, Fang Y-C, Lai W-C, Chen Y-L (2010) Optical design and optimization of light emitting diode automotive head light with digital micromirror device light emitting diode. Optik Int J Light Electron Opt 1–9, vol 121, issue 10, pp. 942–952
10. Lee SWR, Lau CH, Chan SP, Ma KY, NG MH, NG YW, LEE KH, Lo JCC (2006) Development and prototyping of a HB-LED array module for indoor solid state lighting. In: High density microsystem design and packaging and component failure analysis, HDP'06 Conference, Shanghai, China, pp 141–145
11. Peon R, Doluweera G, Platonova I, Irvine-Halliday D, Irvine-Halliday G (2005) Solid state lighting for the developing world—the only solution. Opt Photon Proc SPIE 5941:109–123***
12. Pinto RA, Cosetin MR, da Silva MF, Denardin GW, Fraytag J, Campos A, do Prado RN (2009) Compact emergency lamp using power LEDs. In: Industrial electronics, IECON'09. 35th annual conference of IEEE, Porto, Portugal, pp 3494–3499
13. Shibata S-I, Oyabu T, Kimura H (2009) Bioelectric potential characteristic of pothos under light emitting diode. In: ICCAS-SICE, Fukuoka, Japan, pp 4663–4668
14. Wipiejewski T, Moriarty T, Hung V, Doyle P, Duggan G, Barrow D, McGarvey B, O'Gorman M, Calvert T, Maute M, Gerhardt V, Lambkin JD (2008) Gigabits in the home with plugless Plastic Optical Fiber (POF) interconnects. In: 2nd Electronics system-integration technology conference, 2008 (ESTC 2008), Greenwich, London, UK, pp 1263–1266
15. Lumileds P (2006) Luxeon reliability. Reliability Datasheet RD25
16. Chang YN, Hung CC, Tung SC (2009) Auto mixed light for RGB LED backlight module. In: Industrial electronics, 2009, ISIE 2009, IEEE international symposium, Lisbon, Portugal, pp 864–869
17. Chang SW (2008) LED lighting: high efficiency and environmental benefit, vol 206. Samsung Economic Research Institute Economic Focus, Seoul, South Korea, pp 1–10
18. Narendran N, Deng L, Pysar RM, Gu Y, Yu H (2004) Performance characteristics of high-power light-emitting diodes. In: Third international conference on solid state lighting, proceedings of SPIE, Troy, New York, vol 5187, issue 267, pp 267–275
19. IES (Illuminating Engineering Society) (2008) Standard IES LM-80-08, approved method: measuring lumen maintenance of LED light sources, New York, NY
20. Deshayes Y, Bechou L, Verdier F, Danto Y (2005) Long-term reliability prediction of 935 nm LEDs using failure laws and low acceleration factor ageing tests. Qual Reliab Eng Int 21:571–594
21. Trevisanello L, Meneghini M, Mura G, Vanzi M, Pavesi M, Meneghesso G, Zanoni E (2008) Accelerated life test of high brightness light emitting diodes. IEEE Trans Device Mater Reliab 8(2):304–311
22. Deshayes Y, Bord I, Barreau G, Aiche M, Moretto PH, Bechou L, Roehrig AC, Ousten Y (2008) Selective activation of failure mechanisms in packaged double-heterostructure light emitting diodes using controlled neutron energy irradiation. Microelectron Reliab 48:1354–1360
23. Cree (2009) Cree Xlamp XR family LED reliability. CLD-AP06 Rev. 7. Cree, Inc., pp 1–5
24. Nichia (2009) Specifications for Nichia chip type white LED model: NCSW119T-H3", Nichia STS-DA1-0990A. Nichia Corporation
25. Jeong J-S, Jung J-K, Park S-D (2008) Reliability improvement of InGaN LED backlight module by accelerated life test (ALT) and screen policy of potential leakage LED. Microelectron Reliab 48:1216–1220
26. Polavarapu I, Okogbaa G (2005) An interval estimate of mean-time-to-failure for a product with reciprocal Weibull degradation failure rate. In: Proceedings: Annual reliability and maintainability symposium, 2005, Alexandria, Virginia, pp 261–265
27. Peng C-Y, Tseng S-T (2009) Mis-specification analysis of linear degradation models. IEEE Trans Reliab 58(3):444–455

28. Vazquez M, Nunez N, Nogueira E, Borreguero A (2010) Degradation of AlInGaP red LEDs under drive current and temperature accelerated life tests. Microelectron Reliab 50:1559–1562
29. Lasance CJM (2003) Recent progress in compact thermal models. In: 19th IEEE SEMI-THERM symposium, San Jose, California, pp 290–299
30. Hwang N (2008) Failure analysis matrix of light emitting diodes for general lighting applications. In: Physical and failure analysis of integrated circuits, 2008. IPFA 2008. 15th international symposium, Singapore, pp 1–4
31. Hu Q, Zane R (2009) LED drive circuit with series input connected converter cells operating in continuous conduction mode. In: Applied power electronics conference and exposition, 2009. APEC 2009. 24th annual IEEE, Washington, DC, pp 1511–1517
32. Christensen A, Graham S (2009) Thermal effects in packaging high power light emitting diode arrays. Appl Therm Eng 29:364–371
33. Li Q, Kececioglu DB (2006) Design of an optimal plan for an accelerated degradation test: a case study. Int J Qual Reliab Manage 23(4):426–440
34. Nogueira E, Vazquez M, Nunez N (2009) Evaluation of AlGaInP LEDs reliability based on accelerated tests. Microelectron Reliab 49:1240–1243
35. Kang J-M, Kim J-W, Choi J-H, Kim D-H, Kwon H-K (2009) Life-time estimation of high-power blue light-emitting diode chips. Microelectron Reliab 49:1231–1235
36. Cheng T, Luo X, Huang S, Liu S (2010) Thermal analysis and optimization of multiple LED packaging based on a general analytical solution. Int J Therm Sci 49:196–201
37. Molnar G, Nagy G, Szucs Z (Sept 2008) A novel procedure and device to allow comprehensive characterization of power LEDs over a wide range of temperature. In: TERMINIC 2008, Rome, Italy, pp 89–92
38. Szekely V, Somlay G, Szabo PG, Rencz M (Sept 2008) Design of a static TIM tester. In: THERMINIC 2008, Rome, Italy, pp 132–136
39. Linderman R, Brunschwiler T, Smith B, Michel B (Sept 2007) High-performance thermal interface technology overviews. In: 13th international workshop on THERMINIC 2007, Budapest, Hungary, pp 129–134
40. Horng R-H, Hsiao H-Y, Chiang C-C, Wuu D-S, Tsai Y-L, Lin H-I (2009) Novel device design for high-power InGaN/Sapphire LEDs using copper heat spreader with reflector. IEEE J Select Top Quant Electron 15(4):1281
41. Yu JH, Oepts W, Konijn H (2008) PC board thermal management of high power LEDs. In: Semiconductor thermal measurement and management symposium, 2008. Semi-Therm 2008. 24th annual IEEE, San Jose, California, pp 63–67
42. Chang H, Lai Y-S (2007) Novel AC driver and protection circuits with dimming control for light emitting diodes. In: Industry applications conference, 2007. 42nd IAS annual meeting. Conference record of the 2007 IEEE, New Orleans, Louisiana, pp 696–700
43. Cassanelli G, Mura G, Fantini F, Vanzi M (2008) Failure analysis of high power white LEDs. In: Microelectronics, 2008. MIEL 2008. 26th international conference, Nis, Serbia, pp 255–257
44. Doshi M, Zane R (2008) Reconfigurable and fault tolerant digital phase shifted modulator for luminance control of LED light sources. In: IEEE power electronics specialists conference PESC 2008, Rhodes, Greece, pp 4185–4191
45. Hu Q, Zane R (2009) LED drive circuit with series input connected converter cells operating in continuous conduction mode. In: 24th annual IEEE applied power electronics conference and exposition 2009, Washington, DC, pp 1511–1517
46. Patterson J, Zane R (2008) Series input modular architecture for driving multiple LEDs. In: IEEE power electronics specialists conference 2008, Rhodes, Greece, pp 2650–2656
47. Subramanian K (2010) LED color-temperature control. In: Electronic design online conference series, session 2, 22nd Jun 2010, pp 1–19
48. Ice C (2010) Digitally controlled LED lighting systems. In: Electronic design online conference series, session 3, 22nd Jun 2010, pp 1–28

49. Denicholas J (2010) Using analog semiconductor technologies in solid state lighting applications. In: Electronic design online conference series, session 4, 22nd Jun 2010, pp 1–46
50. Bauernschub R, Lall P (1994) A PoF approach to addressing defect-related reliability. In: IEEE/CPMT international manufacturing technology symposium, Austin, Texas, pp 38–49
51. Pecht M, Dasgupta A (1995) Physics-of-Failure: an approach to reliable product development. J Inst Environ Sci 38:30–34
52. Pecht MG (2008) Prognostics and health management of electronics. Wiley, Hoboken, NJ (Chapter 1)
53. Bowles JB (2003) Fundamentals of failure modes and effects analysis. In: Tutorial notes annual reliability and maintainability symposium, Tampa Bay, Florida
54. MIL-STD-1629A: procedures for performing a failure mode, effects, and criticality analysis, military standard, Nov 1974
55. Mathew S, Das D, Rossenberger R, Pecht M (2008) Failure mechanisms based prognostics. In: 2008 international conference on prognostics and health management, Denver, Colorado, pp 1–6
56. Ganesan S, Eveloy V, Das D, Pecht M (2005) Identification and utilization of failure mechanisms to enhance FMEA and FMECA. In: Proceedings of the IEEE workshop on accelerated stress testing & reliability (ASTR), Austin, Texas, 2–5 Oct 2005
57. JESD659-A: failure-mechanism-driven reliability monitoring, EIA/JEDEC standard, Sept 1999
58. JEP143A: solid-state reliability assessment and qualification methodologies, JEDEC Publication, May 2004
59. JEP150: stress-test-driven qualification of and failure mechanisms associated with assembled solid state surface-mount components, JEDEC Publication, May 2005
60. JESD74: early life failure rate calculation procedure for electronic components, JEDEC Standard, Apr 2000
61. JESD94: application specific qualification using knowledge based test methodology, JEDEC Standard, Jan 2004
62. JESD91A: method for developing acceleration models for electronic component failure mechanisms, JEDEC Standard, Aug 2003
63. SEMATECH, #00053955A-XFR: semiconductor device reliability failure models, SEMATECH Publication, May 2000
64. SEMATECH, #99083810A-XFR: use condition based reliability evaluation of new semiconductor technologies, SEMATECH Publication, Aug 1999
65. SEMATECH, #00053958A-XFR: knowledge-based reliability qualification testing of silicon devices, SEMATECH Publication, May 2000
66. Lindon RL (1961) Risk register. Cereb Palsy Bull 3(5):481–487
67. Department of Defense (2006) Office of the under secretary of defense for acquisition technology and logistics. In: Risk management guide for DOD acquisition, 6th edn. (Version 1.0). OUSD(AT&L) Systems and Software Engineering/Enterprise Development, Washington, DC, pp 1–34
68. Patterson FD, Neailey K (2002) A risk register database system to aid the management of project risk. Int J Project Manage 20:365–374
69. Eskesen SD, Tengborg P, Kampmann J, Veicherts TH (2004) Guidelines for tunnelling risk management: international tunnelling association, Working Group No. 2. Tunnell Underground Space Technol 19:217–237
70. Williams TM (1994) Using a risk register to integrate risk management in project definition. Int J Project Manage 12:17–22
71. Carter R, Hancock T, Morin JM, Robins N (1995) Introducing RIKSKMAN methodology, 1st edn. NNC Blackwell Ltd., UK
72. Ward S (1999) Assessing and managing important risks. Int J Project Manage 17:331–336
73. Yanagisawa T (1998) The degradation of GaAlAs red light-emitting diodes under continuous and low-speed pulse operations. Microelectron Reliab 38:1627–1630

74. Hoang T, LeMinh P, Holleman J, Schmitz J (2005) The effect of dislocation loops on the light emission of silicon LEDs. In: 35th European solid-state device research conference 2005, Grenoble, France, pp 359–362
75. Lu G, Yang S, Huang Y (2009) Analysis on failure modes and mechanisms of LED. In: Reliability, maintainability and safety, 2009. ICRMS 2009. 8th international conference, Chengdu, China, pp 1237–1241
76. Tharian J (2007) Degradation and failure mode analysis of III–V nitride devices. In: Physical and failure analysis of integrated circuits, 2007. IPFA 2007. 14th international symposium, Bangalore, India, pp 284–287
77. Uddin A, Wei AC, Andersson TG (2005) Study of degradation mechanism of blue light emitting diodes. Thin Solid Films 483:378–381
78. Yanagisawa T, Kojima T (2005) Long-term accelerated current operation of white light-emitting diodes. J Lumin 114:39–42
79. Meneghesso G, Levada S, Zanoni E, Podda S, Mura G, Vanzi M, Cavallini A, Castaldini A, Du S, Eliashevich I (2002) Failure modes and mechanisms of DC-aged GaN LEDs. Phys Stat Sol (a) 194(2):389–392
80. Meneghesso G, Levada S, Pierobon R, Rampazzo F, Zanoni E, Cavallini A, Castaldini A, Scamarcio G, Du S, Eliashevich I (2002) Degradation mechanisms of GaN-based LEDs after accelerated DC current aging. In: International electron devices meeting, 2002. IEDM 02 Digest, San Francisco, California, pp 103–106
81. Pavesi M, Rossi F, Zanoni E (2006) Effects of extreme DC-ageing and electron-beam irradiation in InGaN/AlGaN/GaN light-emitting diodes. Semicond Sci Technol 21:138–143
82. Ott M (1996) Capabilities and reliability of LEDs and laser diodes. In: What's new in electronics, 20(6):1–7
83. Chuang S, Ishibashi A, Kijima S, Nakayama N, Ukita M, Taniguchi S (1997) Kinetic model for degradation of light-emitting diodes. IEEE J Quant Electron 33(6):970–979
84. Shah JM, Li Y-L, Gessmann T, Schubert EF (2003) Experimental analysis and theoretical model for anomalously high ideal factors ($n \gg 2.0$) in AlGaN/GaN p–n junction diodes. J Appl Phys 94(4):2627–2630
85. Sugiura L (1997) Comparison of degradation caused by dislocation motion in compound semiconductor light-emitting devices. Appl Phys Lett 70(10):1317–1319
86. Sugiura L (1997) Dislocation motion in GaN light-emitting devices and its effect on device lifetime. J Appl Phys 81(4):1633–1638
87. Ueda O (1999) Reliability issues in III–V compound semiconductor devices: optical devices and GaAs-based HBTs. Microelectron Reliab 39:1839–1855
88. Fukuda M (1988) Laser and LED reliability update. J Lightwave Technol 6(10):1488–1495
89. Wang WK, Wuu DS, Lin SH, Huang SY, Wen KS, Horng RH (2008) Growth and characterization of InGaN-based light-emitting diodes on patterned sapphire substrates. J Phys Chem Solids 69:714–718
90. Ferenczi G (1982) Reliability of LED's; are the accelerated ageing tests reliable? Electrocomponent Sci Technol 9:239–242
91. Rossi F, Pavesi M, Meneghini M, Salviati G, Manfredi M, Meneghesso G, Castaldini A, Cavallini A, Rigutti L, Stress U, Zehnder U, Zanoni E (2006) Influence of short-term low current DC aging on the electrical and optical properties of InGaN blue light-emitting diodes. J Appl Phys 99:053104-1–053104-7
92. Arnold J (2004) When the light go out: LED failure mode and mechanisms. DfR Solutions, College Park, MD, pp 1–4
93. Khan A, Hwang S, Lowder J (2009) Reliability issues in AlGaN based deep ultraviolet light emitting diodes. In: IEEE 47th annual international reliability physics symposium, Montreal, pp 89–93
94. Pan C, Lee C, Liu J, Chen G, Chyi J (2004) Luminescence efficiency of InGaN multiple-quantum-well ultraviolet light-emitting diodes. Appl Phys Lett 84(25):5249–5251
95. Pavesi M, Manfredi M, Salviati G, Armani N, Rossi F, Meneghesso G, Levada S, Zanoni E, Du S, Eliashevich I (2004) Optical evidence of an electrothermal degradation of InGaN-based light-emitting diodes during electrical stress. Appl Phys Lett 84(17):3403–3405

96. Pavesi M, Manfredi M, Rossi F, Meneghini M, Zanoni E, Zehnder U, Strauss U (2006) Temperature dependence of the electrical activity of localized defects in InGaN-based light emitting diodes. Appl Phys Lett 89:041917-1–041917-3
97. Cao XA, Sandvik PM, LeBoeuf SF, Arthur SD (2003) Defect generation in InGaN/GaN light-emitting diodes under forward and reverse electrical stresses. Microelectron Reliab 43:1987–1991
98. Barton DL, Osinski M, Perlin P, Helms CJ, Berg NH (1997) Life tests and failure mechanisms of GaN/AlGaN/InGaN light emitting diodes. In: Reliability physics symposium, IEEE 35th annual proceedings, Denver, Colorado, pp 276–281
99. Wu JD, Huang CY, Liao CC (2003) Fracture strength characterization and failure analysis of silicon dies. Microelectron Reliab 43:269–277
100. Iksan H, Lin K-L, Hsieh J (2001) Fracture analysis on die crack failure. In: IMAPS, Taiwan, 2001, pp 35–43
101. Chen CH, Tsai MY, Tang JY, Tsai WL, Chen TJ (2007) Determination of LED die strength. In: Electronic materials and packaging, 2007. EMAP 2007. International conference, Daejeon, South Korea, pp 1–6
102. Nakamura S, Mukai T, Senoh M, Iwasa N (1992) Thermal annealing effects on p-type Mg-doped GaN films. Jpn J Appl Phys 31:L139–L142
103. Hull BA, Mohney SE, Venugopalan HS, Ramer JC (2000) Influence of oxygen on the activation of p-type GaN. Appl Phys Lett 76:2271–2273
104. Brandt O, Yang H, Kostial H, Ploog KH (1996) High P-type conductivity in cubic GaN/GaAs (113)A by using Be as the acceptor and O as the codopant. Appl Phys Lett 69:2707–2709
105. Kim KS, Han MS, Yang GM, Youn CJ, Lee HJ, Cho HK, Lee JY (2000) Codoping characteristics of Zn with Mg in GaN. Appl Phys Lett 77:1123–1125
106. Zhang X, Chua S-J, Li P, Chong K-B, Wang W (2000) Improved Mg-doped GaN films grown over a multilayered buffer. Appl Phys Lett 73:1772–1774
107. Kim D-J, Kim H-M, Han M-G, Moon Y-T, Lee S, Park S-J (2003) Effects of KrF (248 nm) excimer laser irradiation on electrical and optical properties of GaN:Mg. J Vac Sci Technol B 21:641–644
108. Jang J-S, Park S-J, Seong T-Y (2000) Metallization scheme for highly low-resistance, transparent, and thermally stable Ohmic contacts to P-GaN. Appl Phys Lett 76:2898–2900
109. Khanna R, Stafford L, Voss LF, Pearton SJ, Wang HT, Anderson T, Hung S-C, Ren F (2008) Aging and stability of GaN high electron mobility transistors and light-emitting diodes with TiB2- and Ir-based contacts. IEEE Trans Device Mater Reliab 8(2):272–276
110. Zhu Q-S, Nagai H, Kawaguchi Y, Hiramatsu K, Sawaki N (2000) Effect of thermal annealing on hole trap levels in Mg-doped GaN grown by metalorganic vapor phase epitaxy. J Vac Sci Technol A: Vac Surf Films 18(1):261–267
111. Kohler K, Stephan T, Perona A, Wiegert J, Maier M, Kunzer M, Wagner J (2005) Control of the Mg doping profile in III-N light-emitting diodes and its effect on the electroluminescence efficiency. J Appl Phys 97:104914-1–104914-4
112. Kwon M-K, Park I-K, Kim J-Y, Kim J-O, Kim B, Park S-J (2007) Gradient doping of Mg in p-type GaN for high efficiency InGaN-GaN ultraviolet light-emitting diode. IEEE Photon Technol Lett 19(23):1880–1882
113. Altieri-Weimar P, Jaeger A, Lutz T, Stauss P, Streubel K, Thonke K, Sauer R (2008) Influence of doping on the reliability of AlGaInP LEDs. J Mater Sci: Mater Electron 19: S338–S341
114. Meneghesso G, Levada S, Zanoni E (2004) Failure mechanisms of GaN-based LEDs related with instabilities in doping profile and deep levels. In: IEEE 42nd annual international reliability physics symposium, Phoenix, Arizona, pp 474–478
115. Kozodoy P, DenBaars SP, Mishra UK (2000) Depletion region effects in Mg-doped GaN. J Appl Phys 87(2):770–775
116. Meneghini M, Trevisanello L-R, Levada S, Meneghesso G, Tamiazzo G, Zanoni E, Zahner T, Zehnder U, Härle V, Strauβ U (2005) Failure mechanisms of gallium nitride LEDs related with passivation. In: Electron devices meeting, 2005. IEDM Technical Digest. IEEE International, Washington, DC, pp 1009–1012

117. Hwang N, Naidu PSR, Trigg A (2003) Failure analysis of plastic packaged optocoupler light emitting diodes. In: Electronics packaging technology, 2003, 5th conference (EPTC 2003), Singapore, pp 346–349
118. Kim H, Yang H, Huh C, Kim S-W, Park S-J, Hwang H (2000) Electromigration-induced failure of GaN multi-quantum well light emitting diode. Electron Lett 36:908–910
119. Haque S, Steigerwald D, Rudaz S, Steward B, Bhat J, Collins D, Wall F, Subramanya S, Elpedes C, Elizondo P, Martin PS (2003) Packaging challenges of high power LEDs for solid state lighting. In: IMAPS, Boston, MA, pp 1–5
120. Barton DL, Zeller J, Phillips BS, Chiu P-C, Askar S, Lee D-S, Osinski M, Malloy KJ (1995) Degradation of blue AlGaN/InGaN/GaN LEDs subjected to high current pulses. In: Reliability physics symposium, 1995. 33rd annual proceedings, IEEE international, Las Vegas, Nevada, pp 191–199
121. Barton DL, Osinski M, Perlin P, Eliseev PG, Lee J (1999) Single-quantum well InGaN green light emitting diode degradation under high electrical stress. Microelectron Reliab 39:1219–1227
122. Song BM, Han B (2008) Reliability guidelines of high power LED. In: 2008 CALCE EPS Consortium Report, project no. C08-26, pp 1–11
123. Hewlett Packard (1997) Reliability of precision optical performance AlInGaP LED lamps in traffic signals and variable message sings. Application Brief I-004
124. Wu F, Zhao W, Yang S, Zhang C (2009) Failure modes and failure analysis of white LEDs. In: Electronic measurement & instruments, 2009. ICEMI'09. 9th international conference, Beijing, China, pp 4-978–4-981
125. Shammas NYA (2003) Present problems of power module packaging technology. Microelectron Reliab 43:519–527
126. Damann M, Leuther A, Benkhelifa F, Feltgen T, Jantz W (2003) Reliability and degradation mechanism of AlGaAs/InGaAs and InAlAs/InGaAs HEMTs. Phys Stat Sol (a) 195(1):81–86
127. Meneghesso G, Crosato C, Garat F, Martines G, Paccagnella A, Zanoni E (1998) Failure mechanisms of Schottky gate contact degradation and deep traps creations in AlGaAs/InGaAs PM-HEMTs submitted to accelerated life tests. Microelectron Reliab 38:1227–1232
128. Mizuishi K, Kurano H, Sato H, Kodera H (1979) Degradation mechanisms of GaAs MESFETs. IEEE Trans Electron Devices ED-26(7):1008–1014
129. Meneghini M, Trevisanello L-R, Zehnder U, Meneghesso G, Zanoni E (2007) Reversible degradation of Ohmic contacts on p-GaN for application in high-brightness LEDs. IEEE Trans Electron Devices 54(12):3245–3251
130. Jacob P, Kunz A, Nicoletti G (2006) Reliability and wearout characterisation of LEDs. Microelectron Reliab 46:1711–1714
131. Chang SJ, Chen CH, Su YK, Sheu JK, Lai WC, Tsai JM, Liu CH, Chen SC (2003) Improved ESD protection by combining InGaN-GaN MQW LEDs with GaN Schottky diodes. IEEE Electron Device Lett 24(3):129–131
132. O'Mahony D, Zimmerman W, Steffen S, Hilgarth J, Maaskant P, Ginige R, Lewis L, Lambert B, Corbett B (2009) Free-standing gallium nitride Schottky diode characteristics and stability in a high-temperature environment. Semicond Sci Technol 24:1–8
133. Shei S-C, Sheu J-K, Shen C-F (2007) Improved reliability and ESD characteristics of flip-chip GaN-based LEDs with internal inverse-parallel protection diodes. IEEE Electron Device Lett 28(5):346–349
134. Su YK, Chang SJ, Wei SC, Chen S-M, Li W-L (2005) ESD engineering of nitride-based LEDs. IEEE Trans Device Mater Reliab 5(2):277–281
135. Tsai CM, Sheu JK, Wang PT, Lai WC, Shei SC, Chang SJ, Kuo CH, Kuo CW, Su YK (2006) High efficiency and improved ESD characteristics of GaN-based LEDs with naturally textured surface grown by MOCVD. IEEE Photon Technol Lett 18(11):1213–1215
136. Zhang J-M, Zou D-S, Xu C, Zhu Y-X, Liang T, Da X-L, Shen G-D (2007) High power and high reliability GaN/InGaN flip-chip light-emitting diodes. Chin Phys 16(4):1135–1139

137. Meneghesso G, Chini A, Maschietto A, Zanoni E, Malberti P, Ciappa M (2001) Electrostatic discharge and electrical overstress on GaN/InGaN light emitting diodes. In: Electrical overstress/electrostatic discharge symposium, Portland, Oregon, pp 247–252
138. Wen TC, Chang SJ, Su YK, Wu LW, Kuo CH, Hsu YP, Lai WC, Sheu JK (2003) Improved ESD reliability by using a modulation doped $Al_{0.12}Ga_{0.88}N$/GaN superlattice in nitride-based LED. In: Semiconductor device research symposium, 2003 international, Washington, DC, pp 77–78
139. McCluskey P, Mensah K, O'Connor C, Lilie F, Gallo A, Pink J (1999) Reliability of commercial plastic encapsulated microelectronics at temperatures from 125°C to 300°C. In: Proceedings of the third European conference on high temperature electronics, Proc. HITEN 1999, Oxford, UK, pp 155–162
140. McCluskey P, Mensah K, O'Connor C, Gallo A (2000) Reliable use of commercial technology in high temperature environments. Microelectron Reliab 40:1671–1678
141. Meneghesso G, Leveda S, Zanoni E, Scamarcio G, Mura G, Podda S, Vanzi M, Du S, Eliashevich I (2003) Reliability of visible GaN LEDs in plastic package. Microelectron Reliab 43:1737–1742
142. Meneghini M, Trevisanello L, Sanna C, Mura G, Vanzi M, Meneghesso G, Zanoni E (2007) High temperature electro-optical degradation of InGaN/GaN HBLEDs. Microelectron Reliab 47:1625–1629
143. Wu F, Wu Y, An B, Wu F (2006) Analysis of dark stain on chip surface of high-power LED. In: Electronic packaging technology, 2006. ICEPT'06. 7th international conference, Shanghai, China, pp 1–4
144. Zhou L, An B, Wu Y, liu S (2009) Analysis of delamination and darkening in high power LED packaging. In: Physical and failure analysis of integrated circuits, 2009. IPFA 2009. 16th IEEE international symposium on the digital object, Suzhou, China, pp 656–660
145. Luo X, Wu B, Liu S (2010) Effects of moist environments on LED module reliability. IEEE Trans Device Mater Reliab 10(2):182–186
146. Gladkov A, Bar-Cohen A (1999) Parametric dependence of fatigue of electronic adhesives. IEEE Trans Components Packag Technol 22:200–208
147. Kim H-H, Choi S-H, Shin S-H, Lee Y-K, Choi S-M, Yi S (2008) Thermal transient characteristics of die attach in high power LED PKG. Microelectron Reliab 48:445–454
148. Hu J, Yang L, Shin MW (2007) Mechanisms and thermal effect of delamination in light-emitting diode packages. Microelectron J 38:157–163
149. Mura G, Cassanelli G, Fantini F, Vanzi M (2008) Sulfur-contamination of high power white LED. Microelectron Reliab 48:1208–1211
150. Wong EH, Chan KC, Rajoo R, Lim TB (2002) The mechanics and impact of hygroscopic swelling of polymeric materials in electronic packaging. ASME J Electron Packag 124 (2):122–126
151. Wang L, Feng S, Guo C, Zhang G (2009) Analysis of degradation of GaN-based light-emitting diodes. In: Physical and failure analysis of integrated circuits, 2009. IPFA 2009. 16th IEEE international symposium, Suzhou, China, pp 472–475
152. Rencz M, Szekely V, Morelli A, Villa C (2002) Determining partial resistances with transient measurements, and using the method to detect die attach discontinuities. In: Semiconductor thermal measurement, 2002. Eighteenth annual IEEE symposium, San Jose, California, pp 15–20
153. Hu J, Yang L, Shin MW (2008) Thermal and mechanical analysis of high-power LEDs with ceramic packages. IEEE Trans Device Mater Reliab 8(2):297–303
154. Rencz M, Szekely V (2004) Structure function evaluation of stacked dies. In: Semiconductor thermal measurement and management symposium, 2004. Twentieth annual IEEE, San Jose, California, pp 50–54
155. Hu J, Yang L, Shin MW (2008) Electrical, optical, and thermal degradation of high power GaN/InGaN light-emitting diodes. J Phys D: Appl Phys 41:1–4
156. Molnar G, Nagy G, Szücs Z (2008) A novel procedure and device to allow comprehensive characterization of power LEDs over a wide range of temperature. In: THERMINIC 2008, Rome, Italy, pp 89–92

157. Tan L, Li J, Wang K, Liu S (2009) Effects of defects on the thermal and optical performance of high-brightness light-emitting diodes. IEEE Trans Electron Packag Manuf 32(4):233–240
158. Yu JH, Farkas G, Vader QV (Sept 2005) Transient thermal analysis of power LEDs at package & board level. In: THERMINIC 2005, Belgirate, Italy, pp 244–248
159. Arik M, Weaver S (2005) Effect of chip and bonding defects on the junction temperatures of high-brightness light-emitting diodes. Opt Eng 44(11):11305-1–11305-8
160. Driel WDV, Wisse G, Chang AYL, Jassen JHJ, Fan X, Zhang KGO, Ernst LJ (2004) Influence of material combinations on delamination failures in a cavity-down TBGA package. IEEE Trans Components Packag Technol 27(4):651–658
161. Driel WDV, Gils MAJV, Fan X, Zhang GQ, Ernst LJ (2008) Driving mechanisms of delamination related reliability problems in exposed pad packages. IEEE Trans Components Packag Technol 31(2):260–268
162. Lin Y, Tran N, Zhou Y, He Y, Shi F (2006) Materials challenges and solutions for the packaging of high power LEDs. In: 2006 international microsystems, packaging, assembly conference, IMPACT 2006, Taiwan, pp 1–4
163. Noor YM, Tam SC, Lim LEN, Jana S (1994) A review of the Nd:YAG laser marking of plastic and ceramic IC packages. J Mater Process Technol 42(1):95–133
164. Vandevelde B, Degryse D, Beyne E, Roose E, Corlatan D, Swaelen G, Willems G, Christiaens F, Bell A, Vandepitte D, Baelmans M (2003) Modified micro-macro thermo-mechanical modeling of ceramic ball grid array packages. Microelectron Reliab 43(2): 307–318
165. Li H-T, Hsu C-W, Chen K-C (2007) The study of thermal properties and thermal resistant behaviors of siloxane-modified LED transparent encapsulant. In: International microsystems, packaging, assembly and circuits technology, 2007. IMPACT 2007, Taipei, Taiwan, pp 246–249
166. Torikai A, Hasegawa H (1999) Accelerated photodegradation of poly(vinyl chloride). Polym Degrad Stab 63:441–445
167. Narendran N, Gu Y, Freyssinier JP, Yu H, Deng L (2004) Solid-state lighting: failure analysis of white LEDs. J Cryst Growth 268:449–456
168. Down JL (1986) The yellowing of epoxy resin adhesives: report on high-intensity light aging. Stud Conserv 31:159–170
169. Zhang Q, Mu X, Wang K, Gan Z, Luo X, Liu S (2008) Dynamic mechanical properties of the transient silicone resin for high power LED packaging. In: International conference electronic packaging technology & high density packaging, 2008. ICEPT-HDP 2008, Shanghai, China, pp 1–4
170. Meneghini M, Trevisanello L-R, Meneghesso G, Zanoni E (2008) A review on the reliability of GaN-based LEDs. IEEE Trans Device Mater Reliab 8(2):323–331
171. Baillot R, Deshayes Y, Bechou L, Buffeteau T, Pianet I, Armand C, Voillot F, Sorieul S, Ousten Y (2010) Effects of silicone coating degradation on GaN MQW LEDs performances using physical and chemical analysis. Microelectron Reliab 50:1568–1573
172. Barton DL, Osinski M (1998) Degradation mechanisms in GaN/AlGaN/InGaN LEDs and LDs. In: Proceedings of the 10th conference on semiconducting and insulating materials (SIMC-X), Berkeley, California, pp 259–262
173. Down JL (1984) The yellowing of epoxy resin adhesives: report on natural dark aging. Stud Conserv 29(2):63–76
174. Allen SC, Steckl AJ (2008) A nearly ideal phosphor-converted white light-emitting diode. Appl Phys Lett 92:143309-1–143309-3
175. Tran NT, Shi FG (2007) Simulation and experimental studies of phosphor concentration and thickness for phosphor-based white light-emitting diodes. In: International microsystems, packaging, assembly and circuits technology, 2007, IMPACT, Taipei, Taiwan, pp 255–257
176. Arik M, Weaver S, Becker CA, Hsing M, Srivastava A (2003) Effects of localized heat generations due to the color conversion in phosphor conversion in phosphor particles and layers of high brightness light emitting diodes. In: International electronic packaging technical conference and exhibition, ASME, Maui, Hawaii, pp 1–9

177. Narendran N, Gu Y, Freyssinier-Nova JP, Zhu Y (2005) Extracting phosphor-scattered photons to improve white LED efficiency. Phys Stat Sol (a) 202(6):R60–R62
178. Kim JK, Luo H, Schubert EF, Cho J, Sone C, Park Y (2005) Strongly enhanced phosphor efficiency in GaInN white light-emitting diodes using remote phosphor configuration and diffuse reflector cup. Jpn J Appl Phys 44(21):L649–L651
179. Luo H, Kim JK, Schubert EF, Cho J, Sone C, Park Y (2005) Analysis of high-power packages for phosphor-based white-light-emitting diodes. Appl Phys Lett 86:243505-1–243505-3
180. Li Y-Q, Fu S-Y, Mai Y-W (2006) Preparation and characterization of transparent ZnO/epoxy nanocomposites with high-UV shielding efficiency. Polymer 47:2127–2132
181. Schubert EF (2006) Light-emitting diodes, 2nd edn. Cambridge University Press, Cambridge, pp 192–193 (Chapter 11)
182. Hsu Y-C, Lin Y-K, Chen M-H, Tsai C-C, Kuang J-H, Huang S-B, Hu H-L, Su Y, Cheng W-H (2008) Failure mechanisms associated with lens shape of high-power LED modules in aging test. IEEE Trans Electron Devices 55(2):689–694
183. Arik M, Setlur A, Weaver S, Haitko D, Petroski J (2007) Chip to system levels thermal needs and alternative thermal technologies for high brightness LEDs. J Electron Packag 129:328–338
184. Xie R-J, Hirosaki N (2007) Silicon-based oxynitride and nitride phosphors for white LEDs—a review. Sci Technol Adv Mater 8:588–600
185. Xie R-J, Hirosaki N, Kimura N, Sakuma K, Mitomo M (2007) 2-Phosphor-converted white light-emitting diodes using oxynitride/nitride phosphors. Appl Phys Lett 90:191101-1–191101-3
186. Jia D, Jia W, Jia Y (2007) Long persistent alkali-earth silicate phosphors doped with Eu2+, ND3+. J Appl Phys 101:023520-1–023520-6
187. Xie R-J, Hirosaki N, Mitomo M, Takahashi K, Sakuma K (2006) Highly efficient white-light-emitting diodes fabricated with short-wavelength yellow oxynitride phosphors. Appl Phys Lett 88:101104-1–101104-3
188. Nakamura S (1997) Present performance of InGaN-based blue/green/yellow LEDs. Proc SPIE 3002(26):26–35
189. Tsai C-C, Wang J, Chen M-H, Hsu Y-C, Lin Y-J, Lee C-W, Huang S-B, Hu H-L, Cheng W-H (2009) Investigation of Ce:YAG doping effect on thermal aging for high-power phosphor-converted white-light-emitting diodes. IEEE Trans Device Mater Reliab 9(3):367–371
190. Tang Y-S, Hu S-F, Lin CC, Bagkar NC, Liu R-S (2007) Thermally stable luminescence of $KSrPO_4$:Eu2+ phosphor for white light UV light-emitting diodes. Appl Phys Lett 90: 151108-1–151108-3
191. Mueller-Mach R, Mueller GO, Krames MR (2003) Phosphor materials and combinations for illumination grade white pcLED. Proc SPIE 5187:115–122
192. Mueller-Mach R, Mueller GO, Krames MR, Trottier T (2002) High-power phosphor-converted light-emitting diodes based on III-nitrides. IEEE J Select Top Quant Electron 8 (2):339–345
193. Mueller GO, Mueller-Mach R (2000) White-light-emitting diodes for illumination. Proc SPIE 3938(30):30–41
194. Mueller-Mach R, Mueller G, Krames MR, Hoppe HA, Stadler F, Schnick W, Juestel T, Schmidt P (2005) Highly efficient all-nitride phosphors-converted white light emitting diode. Phys Stat Sol (a) 202(9):1727–1732
195. Uheda T, Hirosaki N, Yamamoto Y, Naito A, Nakajima T, Yamamoto H (2006) Luminescence properties of a red phosphor, CaAlSiN3:Eu2+, for white light-emitting diodes. Electrochem Solid-State Lett 9(4):H22–H25
196. Li YQ, van Steen JEJ, van Krevel JWH, Botty G, Delsing ACA, Disalvo FJ, de With G, Hintzen HT (2006) Luminescence properties of red-emitting $M_2Si_5N_8:Eu^{2+}$ (M = Ca, Sr, Ba) LED conversion phosphors. J Alloys Compd 417:273–279
197. Xie R-J, Hirosaki N, Sakuma K, Kimura N (2008) White light-emitting diodes (LEDs) using (oxy)nitride phosphors. J Phys D: Appl Phys 41:144013-1–144013-5

198. Xie R-J, Hirosaki N, Suehiro T, Xu F-F, Mitomo M (2006) A simple, efficient synthetic route to $Sr_2Si_5N_8:Eu^{2+}$ based red phosphors for white light-emitting diodes. Chem Mater 18 (23):5578–5583
199. Zeng Q, Tanno H, Egoshi K, Tanamachi N, Zhang S (2006) $Ba_5SiO_4Cl_6:Eu^{2+}$: an intense blue emission phosphor under vacuum ultraviolet and near-ultraviolet excitation. Appl Phys Lett 88:051906-1–051906-3
200. Misra S, Kolbe J (2010) Reliability of thermal management substrates for LEDs. In: Electronic design online conference series, session 1, 22nd Jun 2010, pp 1–27
201. Hong E, Narendran N (2004) A method for projecting useful life of LED lighting systems. In: Third international conference on solid state lighting, proceedings of SPIE 5187, pp 93–99
202. Qi H, Vichare NM, Azarian MH, Pecht M (2008) Analysis of solder joint failure criteria and measurement techniques in the qualification of electronic products. IEEE Trans Components Packag Technol 31(2):469–477
203. IPC-SM-785 (1992) Guidelines for accelerated reliability testing of surface mounting solder attachments. Institute for Interconnecting and Packaging Electronic Circuits, Northbrook, IL
204. Chang M-H, Das D, Lee SW, Pecht M (2010) Concerns with interconnect reliability assessment of high power light emitting diodes (LEDs). In: SMTA China south technical conference 2010, Shenzhen, China, 31st Aug–2nd Sept 2010, pp 63–69
205. Choubey A, Yu H, Osterman M, Pecht M, Yun F, Yonghong L, Ming X (2008) Intermetallics characterization of lead-free solder joints under isothermal aging. J Electron Mater 37(8): 1130–1138
206. Li GY, Chen BL (2003) Formation and growth kinetics of interfacial intermetallics in Pb-free solder joint. IEEE Trans Components Packag Technol 26:651–658
207. Osterman M, Pecht M (2007) Strain range fatigue life assessment of lead-free solder interconnects subject to temperature cycle loading. Solder Surf Mount Technol 19(2):12–17
208. Chauhan P, Osterman M, Pecht M (2009) Critical review of the Engelmaier model for solder joint creep fatigue reliability. IEEE Trans Components Packag Technol 32(3):693–700
209. George E, Das D, Osterman M, Pecht M, Otte C (2009) Physics of failure based virtual testing of communications hardware. In: ASME international mechanical engineering congress and exposition (IMECE2009), Buena Vista, FL, USA, 13–19 Nov 2009, pp 12181-1–12181-8
210. Ralston JM, Mann JW (1979) Temperature and current dependence of degradation in red-emitting GaP LED's. J Appl Phys 50:3630–3637
211. Bergh AA (1971) Bulk degradation of GaP Red LEDs. IEEE Trans Electron Devices 18(3): 166–170
212. Meneghini M, Podda S, Morelli A, Pintus R, Trevisanello L, Meneghesso G, Vanzi M, Zanoni E (2006) High brightness GaN LEDs degradation during DC and pulsed stress. Microelectron Reliab 46:1720–1724
213. Tan CM, Eric Chen BK, Foo YY, Chan RY, Xu G, Liu YJ (2008) Humidity effect on the degradation of packaged ultra-bright white LEDs. In: 2008 10th electronics packaging technology conference, Singapore, pp 1–6
214. Tan CM, Chen BKE, Xu G, Liu Y (2009) Analysis of humidity effects on the degradation of high-power white LEDs. Microelectron Reliab 49:1226–1230
215. Narendran N, Gu Y (2005) Life of LED-based white light sources. IEEE/OSA J Display Technol 1(1):167–171
216. Trevisanello L, Zuani FD, Meneghini M, Trivellin N, Zanoni E, Meneghesso G (2009) Thermally activated degradation and package instabilities of low flux LEDs. In: 2009 I.E. international reliability physics symposium, Montreal, Canada, pp 98–103
217. Bar-Cohen A, Kraus AD (1998) Advances in thermal modeling of electronic components and systems, vol 4. ASME Press, New York, NY
218. Gao S, Hong J, Shin S, Lee Y, Choi S, Yi S (2008) Design optimization on the heat transfer and mechanical reliability of high brightness light emitting diodes (HBLED) package. In: 58th electronic components and technology conference, 2008. ECTC 2008, Lake Buena Vista, Florida, pp 798–803

219. Jayasinghe L, Gu Y, Narendran N (2006) Characterization of thermal resistance coefficient of high-power LEDs. In: 6th international conference on solid state lighting, proceedings of SPIE, pp 1–10
220. Gu Y, Narendran N (2004) A non-contact method for determining junction temperature of phosphor-converted white LEDs. In: Third international conference on solid state lighting, proceedings of SPIE 5187, pp 107–114
221. Sanawiratne J, Zhao W, Detchprohm T, Chatterjee A, Li Y, Zhu M, Xia Y, Plawsky JL (2008) Junction temperature analysis in green light emitting diode dies on sapphire and GaN substrates. Phys Stat Sol (c) 5(6):2247–2249
222. Chhajed S, Xi Y, Li Y-L, Gessmann Th, Schubert EF (2005) Influence of junction temperature on chromaticity and color-rendering properties of trichromatic white-light sources based on light-emitting diodes. J Appl Phys 97:054506-1–054506-8
223. Chen ZZ, Liu P, Qi SL, Lin L, Pan HP, Qin ZX, Yu TJ, He ZK, Zhang GY (2007) Junction temperature and reliability of high-power flip-chip light emitting diodes. Mater Sci Semicond Process 10:206–210
224. Liu J, Tam WS, Wong H, Filip V (2009) Temperature-dependent light-emitting characteristics of InGaN/GaN diodes. Microelectron Reliab 49:38–41
225. Peng L-H, Chuang C-W, Lou L-H (1999) Piezoelectric effects in the optical properties of strained InGaN quantum wells. Appl Phys Lett 74(6):795–797
226. Casey HC Jr, Muth J, Krishnankutty S, Zavada JM (1996) Dominance of tunneling current and band filling in InGaN/AlGaN double heterostructure blue light-emitting diodes. Appl Phys Lett 68(20):2867–2869
227. Lasance CJM, Poppe A (2009) Challenges in LED thermal characterisation. In: 10th international conference on thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems, EuroSimE 2009, Delft, pp 1–11
228. Poppe A, Lasance CJM (2009) On the standardization of thermal characterization of LEDs. In: 25th IEEE SEMI-THERM symposium, San Jose, California, pp 1–8
229. Poppe A, Lasance CJM (2008) On the standardisation of thermal characterisation of LEDs. Part II: Problem definition and potential solutions. In: THERMINIC 2008, Rome, Italy, pp 213–219
230. Poppe A, Lasance CJM (2009) Hot topic for LEDs: standardization issues of thermal characterization. In: Light and lighting conference with special emphasis on LEDs and solid state lighting, May 2009, Budapest, Hungary, CIE, pp 1–4
231. Poppe A, Molnár G, Temesvölgyi T (2010) Temperature dependent thermal resistance in power LED assemblies and a way to cope with it. In: 26th IEEE SEMI-THERM symposium, Santa Clara, California, pp 1–6
232. Lasance CJM (2003) Thermally driven reliability issues in microelectronic systems: status-quo and challenges. Microelectron Reliab 43:1969–1974
233. Joshi Y, Azar K, Blackburn D, Lasance CJM, Mahajan R, Rantala J (2003) How well can we assess thermally driven reliability issues in electronic systems today? Summary of panel held at the Therminic 2002. Microelectron J 34:1195–1201
234. Lasance CJM (2008) Ten years of boundary-condition-independent compact thermal modeling of electronic parts: a review. Heat Transf Eng 29:149–168
235. Lasance CJM (2002) The conceivable accuracy of experimental and numerical thermal analyzes of electronic systems'. In: IEEE Trans Comp Packag Technol, 25:366–382
236. Lasance CJM (2001) The European project PROFIT: prediction of temperature gradients influencing the quality of electronic products. In: Proceedings of the 17th SEMI-THERM, San Jose, California, pp 120–125

Chapter 4
Failure Modes and Failure Analysis

J.F.J.M. Caers and X.J. Zhao

Abstract Reliability is related to all levels of an application, from component or device level to system or environment level. Even though all these levels are linked and interact with each other, they are described separately in this chapter. For each level of the system, the dominant failure modes are summarized, and where possible related models describing the degradation are discussed. The chapter is illustrated with pictures of failure modes and an overview of appropriate failure analysis techniques is given. The approach is from an industrial point of view, rather than from academic point of view. Both catastrophic failures and degradation modes resulting in a decreasing light output are discussed. Amongst catastrophic failures, die cracking, electrical opens, electrical shorts, delamination, damage from ESD at the different levels, and driver failures are addressed. Phenomena causing decreasing lumen output are amongst others all mechanisms that affect the recombination of holes and electrons in the active area of the LED, degradation of the lens and of the encapsulant, yellowing of the lens and of the encapsulant, outgassing and deposition, increase of the contact resistance, and degradation of the phosphors. For most failure and degradation mechanisms, a good temperature control is a key. A major challenge is that the time to generate data to predict lumen depreciation is of the same order of magnitude as the life cycle of a LED.

Abbreviations

T_j	Junction temperature
L70	Time to reach 70% of the initial lumen output
EOS	Electrical overstress
ESD	Electrostatic discharge

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TVS	Transient voltage suppression diode
LEE	Light extraction efficiency
CTE	Coefficient of thermal expansion
CME	Coefficient of moisture expansion
IMC	Intermetallic compound
MCPCB	Metal-core printed circuit board
C-SAM	C-mode scanning acoustic microscope
EDX	Energy dispersive X-ray analysis
SAC	Tin silver copper solder alloy (Sn–Ag–Cu)
AuSn	Eutectic gold tin solder composition (AuSn)
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
TST	Thermal shock testing
TCT	Thermal cyclic testing
ESR	Electron spin resonance
pcLED	Phosphor converted LED
HAZ	Heat affected zone
GGI	Gold to gold interconnect
AF	Acceleration factor
FIT	Failures in 10^9 device hours
HTOL	High temperature operating life test
MM	Machine model (ESD)
CDM	Charged device model (ESD)
HBM	Human body model (ESD)
MD	Misfit dislocations
TD	Threaded dislocations
AFM	Atomic force microscope
RI	Refractive index
UBM	Under bump metallization
VOC	Volatile organic compounds
NCA	Nonconductive adhesive
TIM	Thermal interface materials
ECM	Electrochemical migration
FT-IR	Fourier-transform infra red analysis
FWHM	Full-width half-maximum

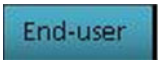
4.1 Introduction

Reliability is related to all levels of an application, from component or device level to system or environment level. All these levels are linked and interact with each other as is shown schematically in Table 4.1: each product is part of a platform and affects all underlying platforms and products. Table 4.2 gives an example of the different levels for a LED-based lighting system: level 0 is the bare LED die, level 6

Table 4.1 System levels for reliability

Product	Platform
Electronic part/component	Electronic assembly
Electronic assembly	Submodule
Submodule	System
System	Environment

Table 4.2 Levels for a LED-based lighting system

	Level 0	Die
	Level 1	Packaged LED
	Level 2	LEDs on board
	Level 3	Module: LED(s) + driver/optics/thermal
	Level 4	Luminaire—Module: L3 + housing/sec.optics
	Level 5	Lighting system including controls
	Level 6	End-user solution

is the end-user solution. Even level 0 in fact can consist of different parts, such as an epitaxial layer deposited onto a carrier substrate. In this chapter, for each product level, different possible failure modes and failure mechanisms and related analysis techniques are discussed.

The interaction between the levels is demonstrated in Fig. 4.1. In this example, encapsulation of a wire bonded LED component (level 1/level 2) results in delamination of the die attach and lifting of the ball bond (level 1). These types of failures are discussed in more detail in the following paragraphs.

A typical build-up of a high-power sapphire based LED package is shown in Fig. 4.2 [1, 2]. The active layers are grown onto a sapphire or SiC submount and

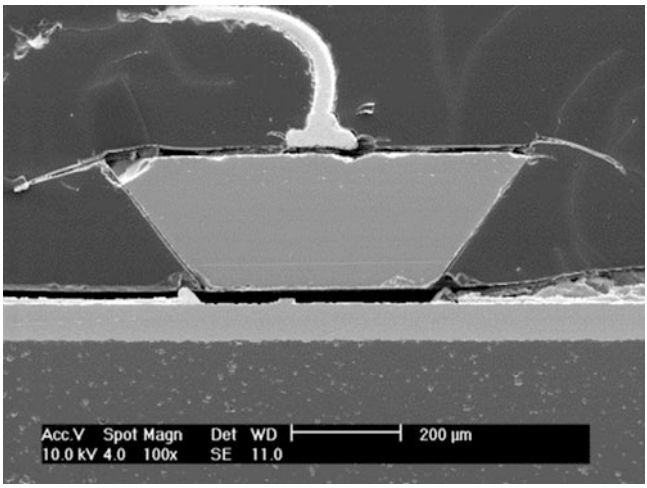


Fig. 4.1 High stresses from encapsulation of the LED results in level 1 defects

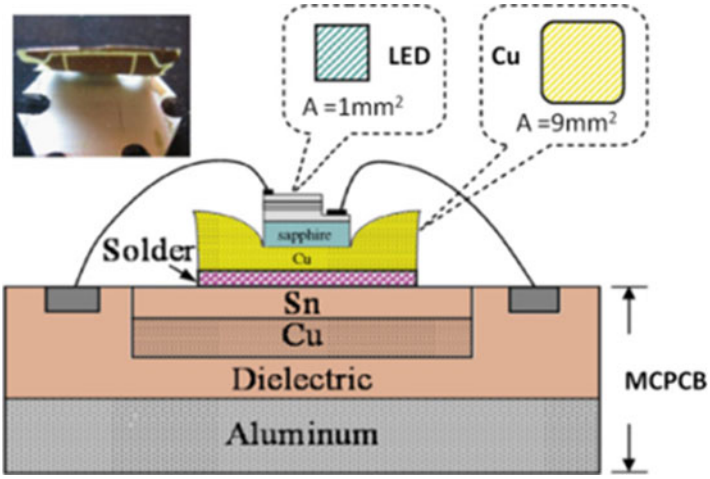


Fig. 4.2 Typical build-up of a high-power sapphire based LED

form together the LED level 1 package. A Cu-slug is used as heat spreader and ensures a good thermal contact between the device and the substrate, typically FR-4 with open or filled via's, direct bonded Cu on AlN or Al_2O_3, or a metal-clad PCB (MCPCB), see Fig. 4.3.

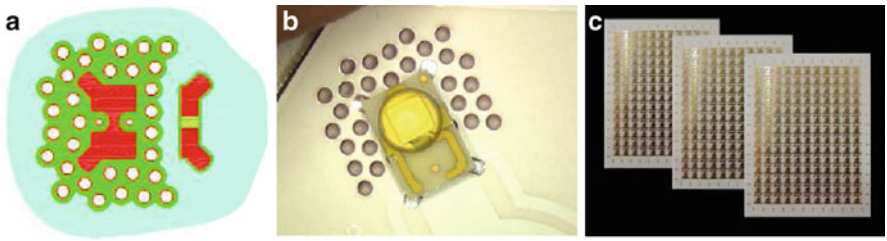


Fig. 4.3 Different level 2 substrates used for high-power LED assembly. (**a**) FR-4 with via's—proposed footprint design for Luxeon REBEL. (**b**) MCPCB. (**c**) Direct bonded copper

4.2 Failure Modes and Failure Analysis

4.2.1 Level 0: Die Level Failure Modes

Different from other electronic components, LEDs most of the time do not fail catastrophically. Apart from catastrophic LED failures, mostly a gradual decrease in lumen output is observed. Therefore, a common criterion for the life time of the LED is the so-called L70; this is the time half the product population falls below 70% of the initial light output. ASSIST, the Alliance for Solid-State Illumination Systems and Technologies, supports this definition for the life time for lighting applications.

4.2.1.1 Catastrophic LED Failures

LED catastrophic failure rates can be modeled using the same general principles as silicon-based semiconductors. Failure rate vs. operating time can be determined for several different stress conditions (i.e. different combinations of junction temperature, T_j, and forward current, I_f). The temperature has a very strong effect on catastrophic failure rates; drive current has a weak effect on catastrophic failure rates.

Catastrophic LED failures can manifest themselves as an open or as a short. Flip-chip LED configuration will in principle fail as a short; broken wires or lifted ball bonds are common failure modes resulting in an open.

For catastrophic failures, we distinguish between intrinsic failures and wear-out failures. The difference is that for intrinsic failures, failure occurs randomly and the failure rate is constant. The important parameter is the total amount of burning hours, meaning number of devices times number of burning hours; the number of devices and the burning time are exchangeable. If we represent the failure rate of a product over its life cycle schematically in the so called bathtub curve, the intrinsic failure rate is related to the flat part in the bath tub curve. In terms of Weibull

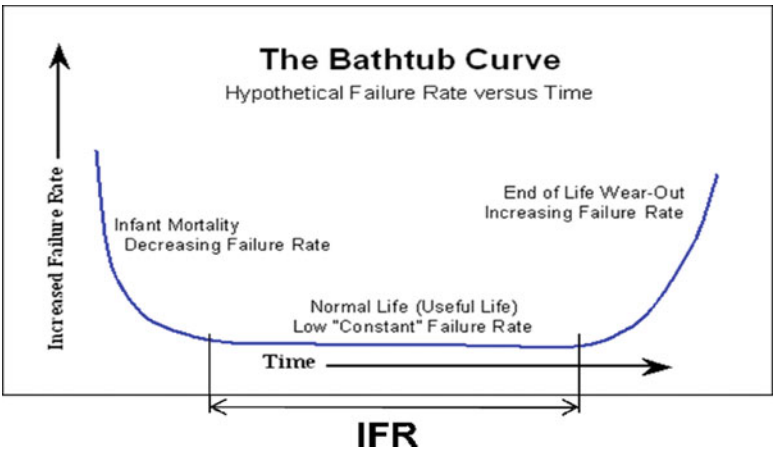


Fig. 4.4 Idealized failure rate over the product life cycle

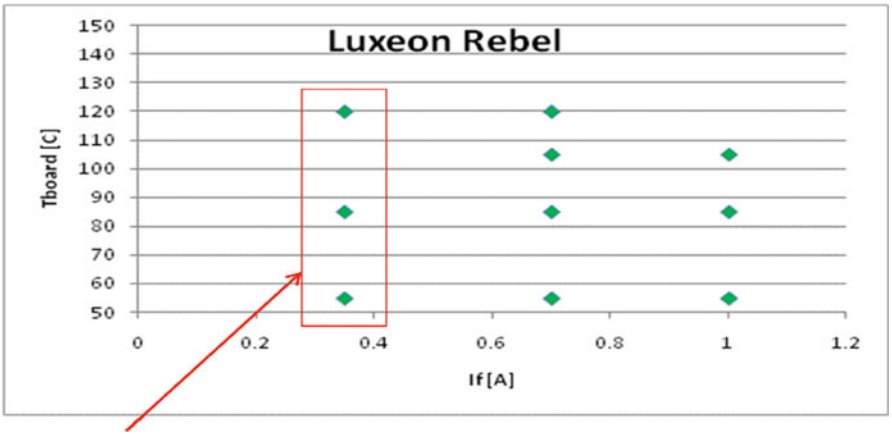


Fig. 4.5 Typical HTOL test scheme for HB LEDs

cumulative failure distribution, the intrinsic failure rate corresponds with a shape factor, β, equaling 1. For wear-out failures, the failure rate is increasing over time (see Fig. 4.4), the Weibull shape factor $\beta > 1$. For both intrinsic and wear-out failures, the failure rate is depending on the forward current and on the junction temperature.

LM-80 data can be used to estimate the intrinsic failure rate. Lumileds published extensive LM-80 data for the Luxeon Rebel [3]. According to LM-80, HTOL tests have to be done at least at three board temperature levels. The Lumileds test scheme is much more extensive and is shown in Fig. 4.5; the conditions required by LM-80

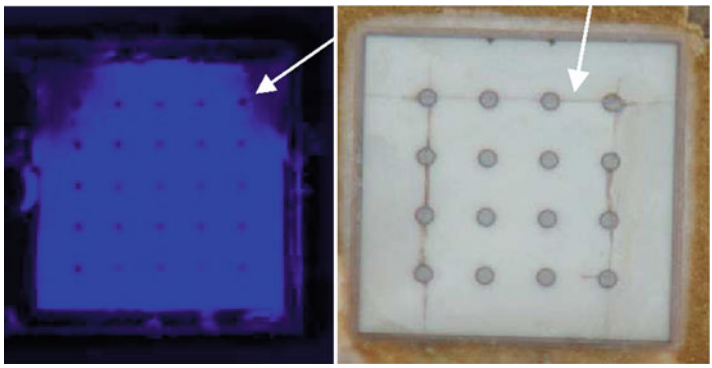


Fig. 4.6 Cracking of LED die

standard are highlighted. The intrinsic failure rate, IFR is expressed in FIT, the number of failures per 10^9 device hours:

$$\mathrm{IFR} = n_c(n)^* 10^9 / (N^* t^* \mathrm{AF}), \tag{4.1}$$

with n, observed total number of failures during the test, excluding early failures; $n_c(n)$, corrected number of failures (using a 60% CL interval with Poisson statistics); $n_c(n) = 0.916$ if no failures observed; N, numbers of units tested; t, test time; AF, acceleration factor; $\mathrm{AF} = \mathrm{AF}(I_f) \times \mathrm{AF}(T)$.

For typical semiconductor devices IFR ≈ 0.5 FIT for logic and ≈3 FIT for microcontrollers, rated at 55°C [4]. With the minimal data set from required LM-80 test and a sample size of 80 per test condition and 6,000 test hours per series, a FIT rate at 55°C lower than 80 FIT cannot be demonstrated. For the calculation, a conservative value for the activation energy is assumed: 0.5 eV. For comparison: for semiconductor degradation, typically the activation energy of 0.7 eV is considered [4].

Examples of catastrophic failure are cracking of the thin epilayer, mechanical or thermal damage from level 1 to level 4 processing, electrical overstress (EOS), and corrosion.

Cracking of the die or of the substrate can be induced by thermal shocks causing temperature gradients and thermomechanical stresses from mismatches in CTE. Additional stresses to the die can be generated from L1 and L2. Similarly, high driving current can cause rapid temperature increase from Joule heating and as a result high thermal gradients. Examples of die cracking or cracking of the epilayer are shown in Fig. 4.6. Dicing quality of LED and substrate can highly affect the risk of cracking. An example of damage from dicing is given in Fig. 4.7 [5]. Higher damage at the component edge increases the risk of cracking. For silicon, the effect of flaw size on the strength is illustrated in Fig. 4.8 [6].

Today, no standard has been agreed to determine the limits for catastrophic failures in terms of junction temperature, T_j and forward current, I_f. Typically,

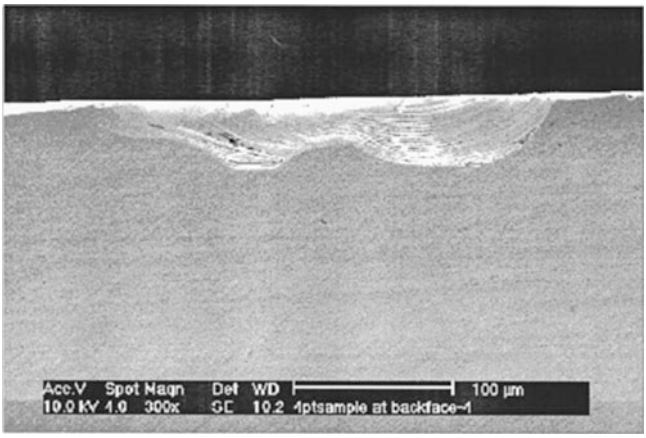


Fig. 4.7 A large edge defect caused by dicing

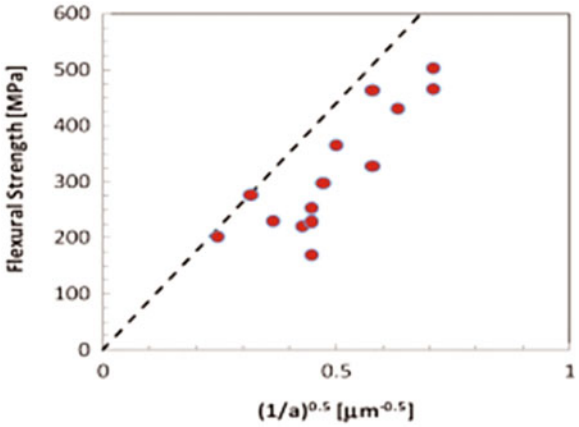


Fig. 4.8 Effect of flaw size on the strength of Si

highly accelerated operating life tests are performed under conditions outside the recommended operating conditions and outside the maximum ratings (see Fig. 4.9) to build life models.

ESD damage is an example of a transient EOS. Electrostatic discharge (ESD) occurs when objects, including people, furniture, machines, integrated circuits or electrical cables, become charged and discharged [7]. The EOS family includes also lightning and electromagnetic pulses. Electrostatic charging brings objects to surprisingly high potentials of many thousands of volts in ordinary home or office environments. ESD produces currents which can have rise times less than a nanosecond, peak currents of dozens of Amps and durations that can last from tens to hundreds of nanoseconds. ESD precautions are important during whole

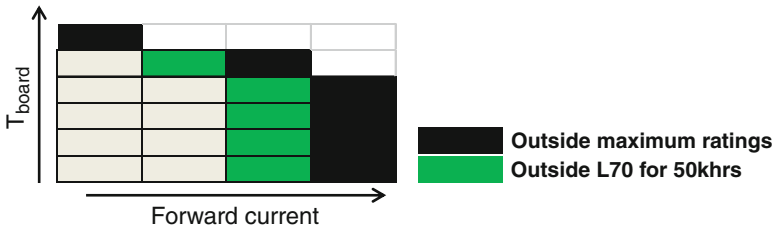


Fig. 4.9 Test cells to build models for catastrophic failures

Table 4.3 Measured static charge developed on people under normal working conditions

Condition	Average reading volts
Person walking across linoleum floor	5,000
Person walking across carpet	15,000
Person working at bench	800
Circuit packs as bubble plastic cover removed	20,000
Circuit packs as packed foam box	11,000
Circuit packs (packaged) as returned for repair	6,000



Fig. 4.10 Static charge of 9.43 kV measured on kapton tape

product process from devices making to system assembly. The prevention methods could be the use of antistatic coatings to the materials or the use of air ionizers to neutralize charges. The damage due to human handling can be reduced by the proper use of wrist straps for grounding the accumulated charges and shielded bags for carrying the individual LEDs components. Table 4.3 shows some measurements of static charge developed on people and materials under normal work conditions [8]. Figure 4.10 illustrates that the static charge on a kapton tape can be as high as

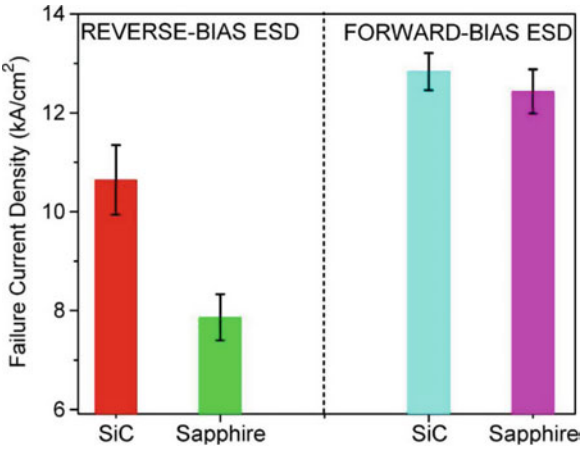


Fig. 4.11 Failure current density of blue LEDs grown on SiC and sapphire substrate submitted to forward and reverse-bias TLP testing

10 kV. To demonstrate the possible impact, the following situation can be considered: with a charge of only 2,000 V, the human body stores approximately 0.2 mJ of energy. At discharge, this energy is dissipated in the body resistance and in the device resistance. When this energy is released with time constants of nanoseconds, an average power of up to several kilowatts is provided. Such short bursts of power in many cases are sufficient to melt small volumes of Si or GaAs and create small explosions that crater the die surface. Unless ESD robustness is included during design, these current levels can damage electrical components and upset or damage electrical systems from cell phones to computers. ESD may cause immediate failure of the semiconductor junction, a permanent shift of its parameters, or latent damage causing increased rate of degradation and hence early failures. Recent reports have indicated that advanced LED structures—in particular those with high indium content—can be particularly susceptible to ESD events. For most of the LED devices, the robustness to reverse bias is lower than with respect to forward bias (see Fig. 4.11). A reverse biased pulse in nanoseconds may cause ESD damage while a forwarded biased pulse in such a time can pass through LED device without damage. Early LED devices were characterized by high defect densities, resulting in low ESD robustness with failure threshold even below 500 V [9]. A measurable leakage current at reverse bias can indicate ESD damage.

Si-devices often have protection circuits incorporated at their inputs. For LEDs, assembly Zener diodes in a reverse biased circuit parallel with the LED circuit would help reducing the risk of ESD damage. This allows the discharge voltage to flow through both directions of the circuit without damage to the device. Selecting high thermal resistance substrates can also improve the ESD robustness, such as SiC substrates, GaN substrates or Si substrates. Because SiC has a better lattice matching with GaN than sapphire substrates, GaN LEDs grown on SiC have in general a better ESD robustness than on sapphire.

Also TVS diodes can be used to protect LEDs against ESD impact. *T*ransient *V*oltage *S*uppress diodes are solid state pn junction devices, specially designed to

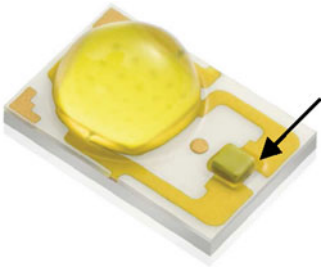


Fig. 4.12 Luxeon Rebel LED with in parallel a protection diode to transient voltages

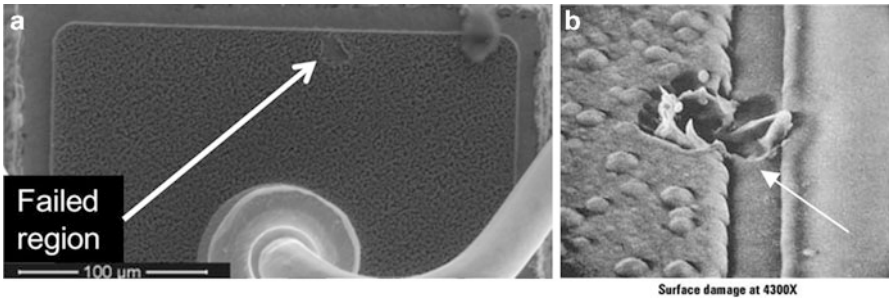


Fig. 4.13 ESD catastrophic damage (SEM)

protect sensitive semiconductors from damaging effects of transient voltages. An example of a LED with in parallel a protection diode is shown in Fig. 4.12 [10]. In this example, the ESD protection is added in level 1. Figure 4.13 shows typical ESD damage as can be observed by SEM. In Fig. 4.13a, ESD caused catastrophic damage from junction shortening on an InGaN-based LED. The position of the failed region is indicated by a label [11, 12].

ESD tests are aimed to ensure that electrical components and systems can survive the ESD stresses that they may encounter. Systems are tested for use in non-ESD controlled environments e.g. according to IEC 61000-4-23. There are three principal sources of charge which can give rise to damaging ESD events [8]: (1) a charged person touches a device and discharges the stored charge to or through the device to ground. (2) The device itself acting as one plate of a capacitor can store charge. Upon contact with an effective ground the discharge pulse can create damage. And (3) an electrostatic field is always associated with charged objects. Under particular circumstances, a device inserted in this field can have a potential induced across an oxide that creates breakdown. Based on the reproduction of typical discharge pulses to which the device may be exposed during manufacturing or handling, several standard ESD stress models have been developed. Most widely used are the human body model (HBM), machine model (MM), and charged device model (CDM). The human-body model (HBM) is the most commonly used model for characterizing the susceptibility of an electronic device to damage from

Table 4.4 ESDS component sensitivity classification—human body model

Mil-STD-1686 classes of ESDS parts	Per ANSI/ESD STM5.1
HBM ESD class (voltage range)	Human body model (HBM)
1: >0–1,999 V	1A: 250 to <500
	1B: 500 to <1,000
	1C: 1,000 to <2,000
2: 2,000–3,999 V	2: 2,000 to <4,000
3: 4,000–15,999 V	3A: 4,000 to <8,000
	3B: > or =8,000

electrostatic discharge (ESD). The model is a simulation of the discharge which might occur when a human touches an electronic device. The HBM definition most widely used is the test model defined in the United States military standard, MIL-STD-883, Method 3015.8, Electrostatic Discharge Sensitivity Classification. This method establishes a simplified equivalent electrical circuit and the necessary test procedures required to model an HBM ESD event. In the HBM model, the human body is modeled as a 100–250 pF capacitor, which is discharged on the device through a 1.0–2.0 kΩ resistance and a switch. The ESD robustness is defined as the maximum voltage a device can withstand before ESD failure. Table 4.4 gives the ESD classification for the three models, compared with ESD STM5.1. While HBM can be an excellent predictor of the ESD robustness of an electronic device, by means of this method no information on the physical mechanism responsible for failure and on the electrical behavior of LEDs at high current/voltage levels can be extrapolated. In 1985, T. Maloney and N. Khurana introduced the transmission line pulse (TLP) as a way to study integrated circuit technologies and circuit behavior in the current and time domain of ESD events [13]. By the TLP method it is possible to generate ESD-like pulses with increasing voltage amplitude. The length of the pulses depends on the length of the transmission line used for the tests. The TLP method has the unique advantage of permitting accurate control and measurement of the characteristics of the devices at extremely high current levels. For this reason, the TLP method is adopted in many research laboratories to study the effect of ESD on the electrical characteristics of electronic devices. Commercial 100 ns TLP systems produce current pulses from 1 mA up to 10 A or 20 A into a short. Most TLP systems can also measure DC leakage after each pulse, allowing the system to detect damage to the sample (Tables 4.5 and 4.6).

Corrosion can result in opens or shorts on die level. It can be the result of e.g. poor protection of the devices from L3 to L5 in outdoor applications. Figure 4.14 illustrates how moisture can get access to the die surface. Figure 4.14 shows delamination of the dome giving free access for the moisture to the die surface. Mostly, it is not so obvious. Dye and pry can be used to demonstrate the leakage path as is shown in Fig. 4.14b. Here, the sample has been immersed in a (red) ink. The ink has a very low viscosity and can wick through very small cracks. After baking, the ink at the outer surface can be wiped off. In case of a silicone protection layer as in Fig. 4.14b, this layer can be peeled off and the leakage path is decorated

Table 4.5 ESDS component sensitivity classification—machine model

Mil-STD-1686 classes of ESDS parts	Per ANSI/ESD STM5.1
MM ESD class (voltage range)	Machine model (MM)
M1: 0–100 V	M1: <100 V
M2: 101–200 V	M2: 100 to <200 V
M3: 201–400 V	M3: 200 to <400 V
M4: 401–800 V	M4: > or =400 V
M5: >800 V	

Table 4.6 ESDS component sensitivity classification—charge device model

Mil-STD-1686 classes of ESDS parts	Per ANSI/ESD STM5.1
CDM ESD Class (Voltage Range)	Charge device model (CDM)
C1: 0–124 V	C1: <150 V
C2: 125–249 V	C2: 150 to <250 V
C3: 250–499 V	C3: 250 to <500 V
C4: 500–999 V	C4: 500 to <1,000 V
C5: 1,000–1,499 V	C5: 1,000 to <1,500 V
C6: 1,500–2,999 V	C6: 1,500 to <2,000 V
C7: ≥3,000 V	C7: ≥2,000 V

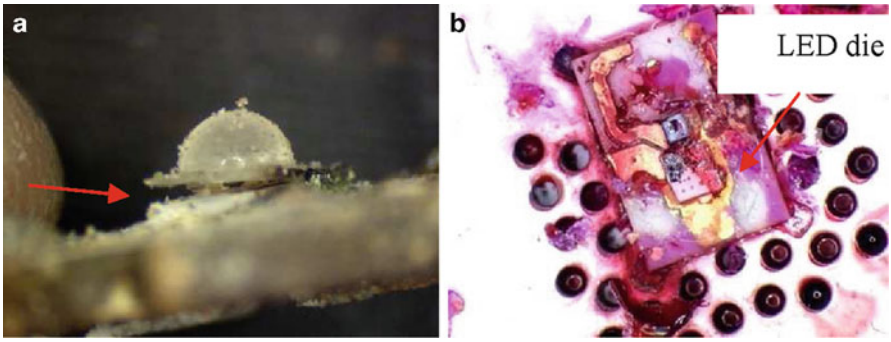


Fig. 4.14 Leakage paths for moisture: (**a**) delamination visible with optical microscopy, (**b**) decoration using dye and pry

with the red ink. In this example, the die is partly covered with ink. Also the narrow gap between the connection lines is filled with ink.

4.2.1.2 Lumen Depreciation

Each level can contribute to lumen depreciation of the system, e.g. yellowing of the optical and encapsulation materials, degradation of the phosphor conversion, etc. In this paragraph the focus is on possible die-level effects causing lumen depreciation. The effect of the other materials is described in the next paragraphs.

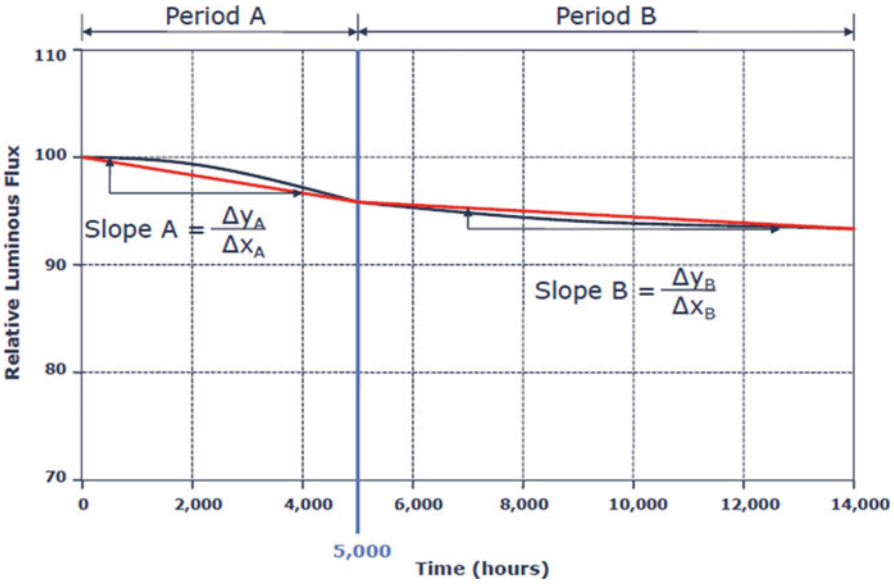


Fig. 4.15 Linear model for lumen depreciation according to Cree

Different from catastrophic failures, for lumen depreciation we notice a strong I_f dependence and weak T-dependence. Several empirical models have been used to describe the lumen depreciation over time. Cree published a linear model, distinguishing between the time period before and after 5,000 h. This is schematically shown in Fig. 4.15 [14].

The most widely accepted model for lumen depreciation over time is approximated by [15]:

$$\frac{L}{L_0} = e^{-\alpha t}, \tag{4.2}$$

with L, lumen output,

$$\alpha = f(T_j, I_f).$$

Figure 4.16 shows the lumen depreciation according to (4.1) for different values of α. For current technologies, $\alpha \approx 10^{-6}$. What this means for the expected life time of e.g. 30.000 h is illustrated in Table 4.7.

To fill in the need of a standard procedure to estimate the decrease of lumen output over time, recently, a guideline has been worked out: TM-21. It provides recommendations for projecting long term lumen maintenance of LED packages using data obtained when testing them per LM-80 [16]. An example of the long-term lumen maintenance and extrapolation to L70 is shown in Fig. 4.17 [15]. Typically, data of lumen output between 1,000 and 6,000 h are used to estimate L70. Extrapolation is only allowed to a maximum of six times the test time.

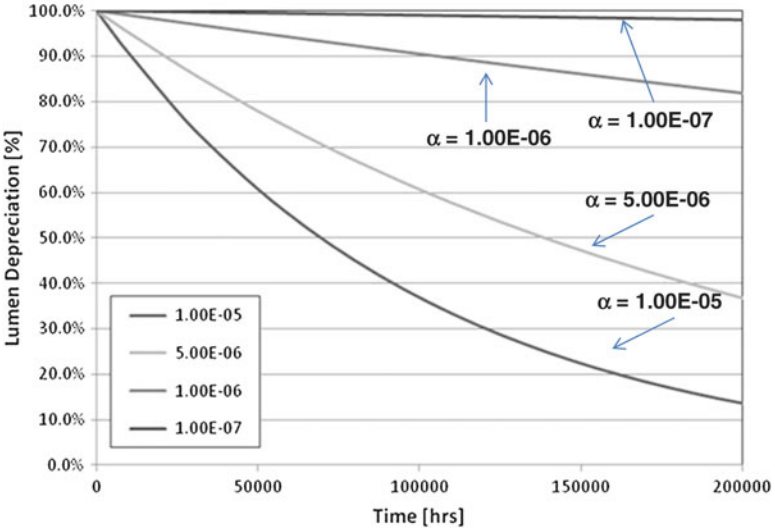


Fig. 4.16 Lumen depreciation according to (4.1) for varying α

Table 4.7 Calculated lumen depreciation according to (4.2)

Lumen depreciation at 30,000 h (%)	α
3	1.00E−06
6	2.00E−06
10	3.50E−06
30	1.20E−05

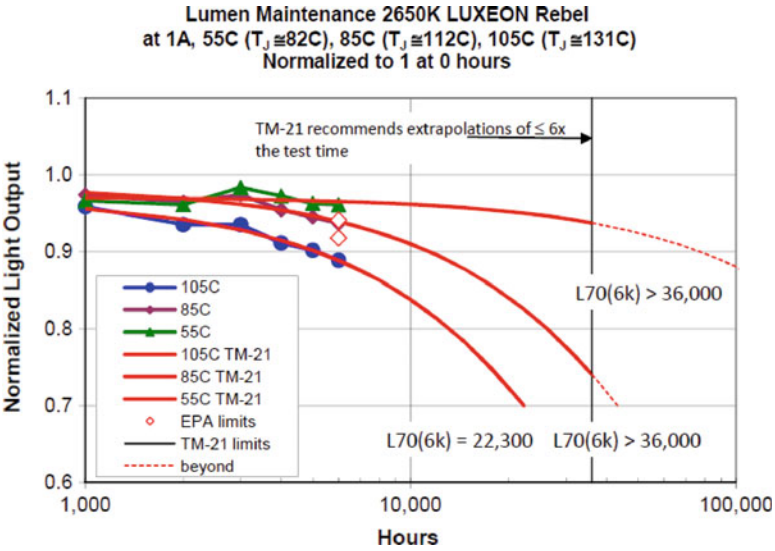


Fig. 4.17 Long-term lumen maintenance data and L70 extrapolation

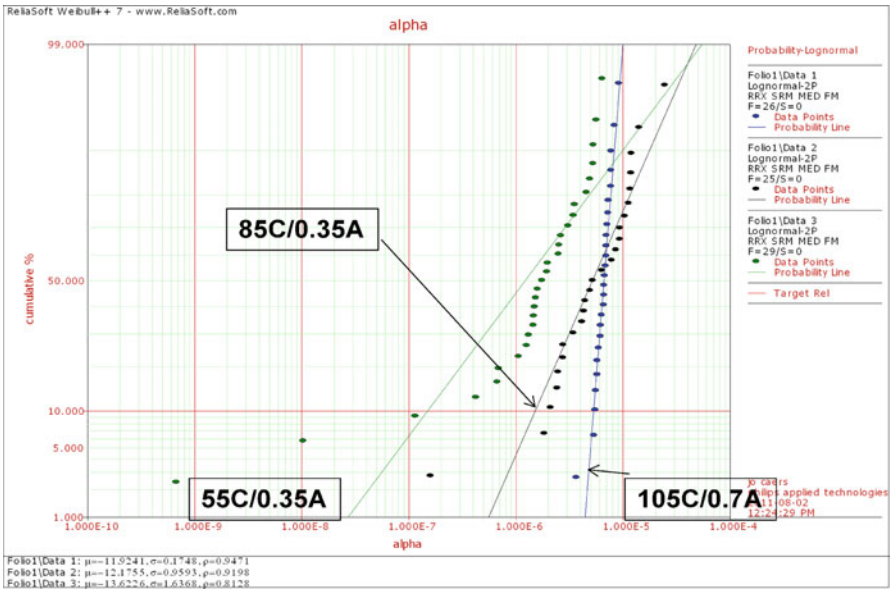


Fig. 4.18 Cumulative distributions of calculated α for Luxeon Rebel taken from LM-80 data

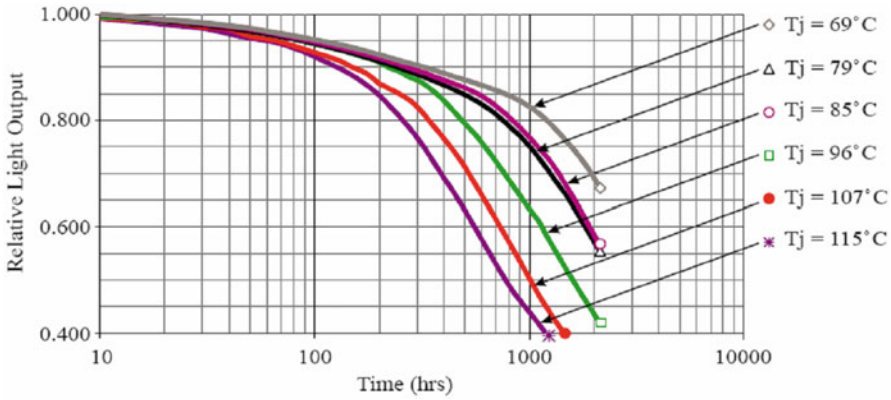


Fig. 4.19 Light output variation as a function of T_j for white LEDs

LM-80 data are only available for limited number of products. Major challenge is that the required test time is around 8 months, which is also more or less the life cycle of current LED products. This means that by the time that the data become available, next generation is already available or even the product has become already obsolete. Extensive LM-80 data have been published for Luxeon Rebel [17]. These include estimations for the exponent, α, of (4.2). Figure 4.18 shows cumulative distributions for three test conditions. A lognormal distribution is assumed. From Fig. 4.19, on average 3% lumen depreciation is to be expected after 30 kh for Luxeon Rebel for 55°C board temperature and $I_f = 0.35$ A.

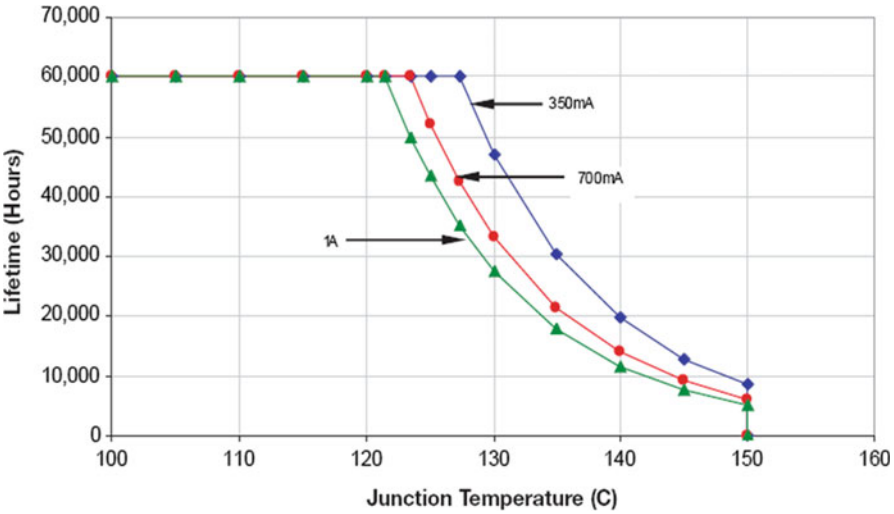


Fig. 4.20 Expected L70 lifetimes for InGaN Luxeon Rebel

An example of the effect of the junction temperature on the lumen output decrease is shown in Fig. 4.19 [18]. For the LED type used in Fig. 4.19, increasing T_j from 69 to 115°C decreases L70 by a factor of 5. For InGaN Luxeon Rebel, the dependence of the life time on I_f is illustrated in Fig. 4.20. The life time is defined as B10/L70, the time that maximum 10% of the LEDs reach 70% of the initial lumen output. Increasing I_f from 0.35 to 1 A decreases the life time by a factor 1.5–2.

Lumen depreciation can have several causes. Any mechanism that affects the recombination of holes and electrons in the active area of the LED will result into a die-level decreased light output. We distinguish between intrinsic and extrinsic failure mechanisms. Intrinsic failure mechanisms are a.o. dislocation and defect creation, movement of these defects, dopant diffusion, electromigration and current crowding from uneven current distribution. External failure mechanisms include electrical contact interdiffusion and degradation of Ohmic contacts, and electromigration at the die surfaces.

Intrinsic Semiconductor Failure Mechanisms

Formation and movement of defects and dislocations. Nucleation and growth of dislocations is a known mechanism for degradation of the active region, where the radiative recombination occurs. This requires a presence of an existing defect in the crystal and is accelerated by heat, high current density, and emitted light. Gallium arsenide and aluminum gallium arsenide are more susceptible to this mechanism than gallium arsenide phosphide and indium phosphide. Due to different properties of the active regions, gallium nitride and indium gallium nitride are virtually insensitive to this

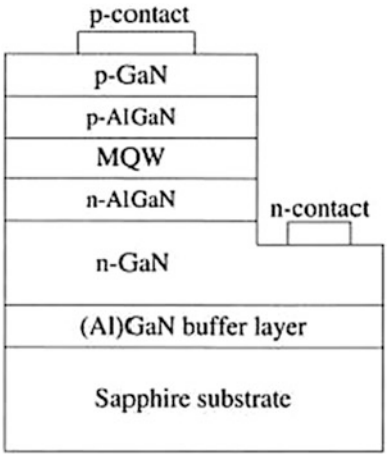


Fig. 4.21 Structure of GaN LED

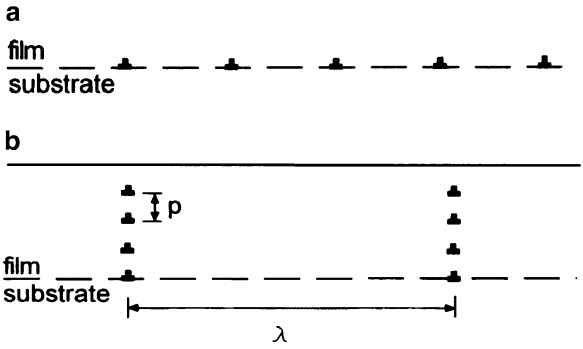


Fig. 4.22 Physical micromechanisms for relaxation of misfit stresses: (**a**) formation of a misfit dislocation row and (**b**) formation of a misfit dislocation walls

kind of defect. Dislocations in heteroepitaxial thin films can be divided into two types: misfit and threaded dislocations respectively. Misfit dislocations lie in the epitaxial interface and accommodate the lattice mismatch between the film and substrate [19, 20]. In order to minimize mismatch dislocations, special care needs to be taken to the structure of the LED die. An example is given in Fig. 4.21. In the example, a buffer layer is inserted for this purpose between the sapphire substrate and the active layers.

Threaded dislocations lie within the film and run from the interface to the film surface [21] and were originally explained on the basis of dislocation "copying" wherein dislocations in the substrate were duplicated into the deposit when they were overgrown. Threaded dislocations or dislocation walls can also be a way to relax misfit stresses as is shown in Fig. 4.22. In Fig. 4.22b λ and p are the spacings between the walls and between the dislocations in a wall, respectively. The convergence of two island films during epitaxial growth leads to the transformation of their contact-edge surfaces (being crystallographically misoriented) into an interface, a low-angle grain boundary. At the same time, any low-angle boundary in a crystal is represented as a wall of dislocations. In the situation discussed, a low-angle boundary in the film resulting from the convergence of two island films is

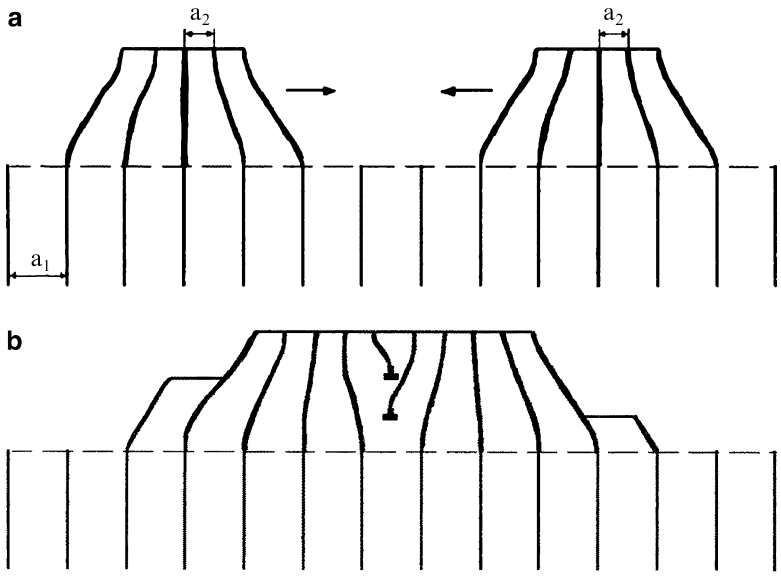


Fig. 4.23 Convergence of island films during deposition (**a**) island films migrate towards each other. (**b**) Island films converge, whereupon a MD wall (a low-angle boundary) is formed

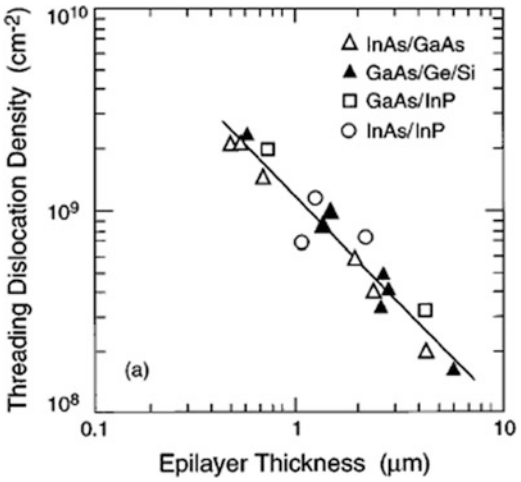


Fig. 4.24 Decay of the threaded dislocation density for high dislocation densities for a range of systems [28]

naturally interpreted as a wall of misfit dislocations [22]. The mechanism is schematically shown in Fig. 4.23. The threading dislocation density typically decreases with increasing epilayer thickness [23] (see Fig. 4.24). The result of threaded dislocations can be an electrical short between *n* and *p* area [24].

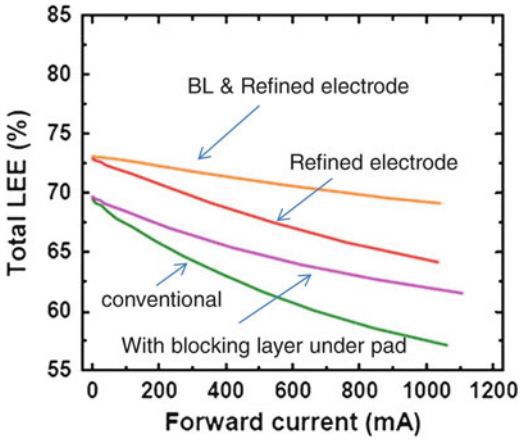


Fig. 4.25 Total LEE as a function of forward current computed for LEDs of various designs

Electromigration caused by high current density can move atoms out of the active regions, leading to emergence of dislocations and point defects, acting as nonradiative recombination centers and producing heat instead of light.

Ionizing radiation can lead to the creation of defects as well, which leads to issues with radiation hardening of circuits containing LEDs (e.g., in optoisolators).

Thermal runaway. Non-homogeneities in the substrate, causing localized loss of thermal conductivity, can cause thermal runaway where heat causes damage which causes more heat, etc. Most common defects are delamination between die and heatspreader or heatsink, voids caused by outgassing from die-attach material, evaporation of volatile elements in solder flux, poor L1 processing, or by electromigration effects resulting in phase segregation and voiding. Kirkendall voiding can be another cause for temperature increase.

Current crowding, which is a non-homogenous distribution of the current density over the junction. This is design related. Current crowding may lead to creation of localized hot spots, which poses risk of thermal runaway [25, 26]. Figure 4.25 illustrates the possible effect of LED designs on the light extraction efficiency (LEE) [25].

Reverse bias. Although the LED is based on a diode junction and is nominally a rectifier, the reverse-breakdown mode for some types can occur at very low voltages and essentially any excess reverse bias causes immediate degradation, and may lead to vastly accelerated failure. 5 V is a typical, "maximum reverse bias voltage" figure for ordinary LEDs; some special types may have lower limits. See also ESD damage in part "catastrophic failures."

Segregation of impurities and dopants. Typical dopants are Mg and Si; dopants can act as non-radiative recombination centers. High temperature can accelerate the degradation. This again results in a decreased light output.

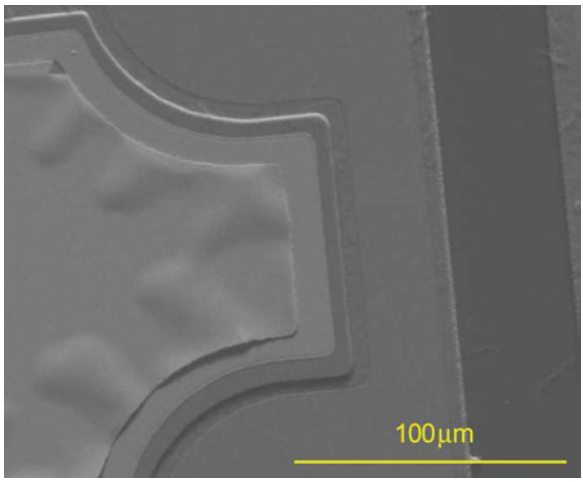


Fig. 4.26 Partial detachment of an Ohmic contact detected as a consequence of stress at high current levels

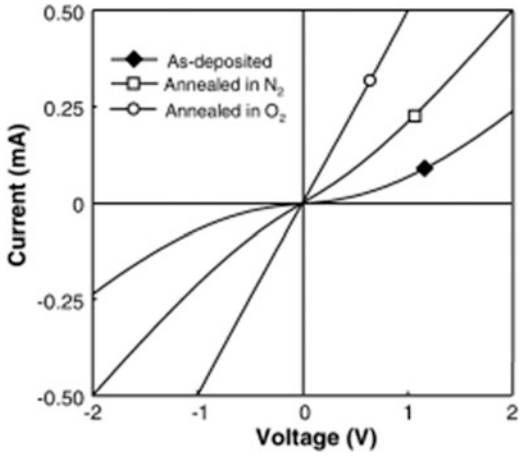


Fig. 4.27 *I–V* characteristics of Ru/Ni (50 A/50 A) contacts on p-type GaN. Annealing was carried out at 500°C for 1 min

Extrinsic Failure Mechanisms

Contact degradation. High driving current levels at high temperature can result in a strong decrease in the optical power at an early stage of the LED life, related to the additional parasitic series resistance from degradation of the Ohmic contact. Figure 4.26 shows an example of visible deterioration of the contact metal at high current levels. In this example, partial detachment of the contact metal is observed [27–30]. Figure 4.27 shows the direct effect of deterioration of the Ru/Ni contacts on p-type GaN on the *I*/*V* characteristic of the LED after annealing at 500°C [31].

Short circuits. Mechanical stresses, high currents, and a corrosive environment can lead to formation of corrosion products or whiskers, causing short circuits along the component surface. With decreasing thickness of the dice and decreasing component size, this risk becomes more obvious.

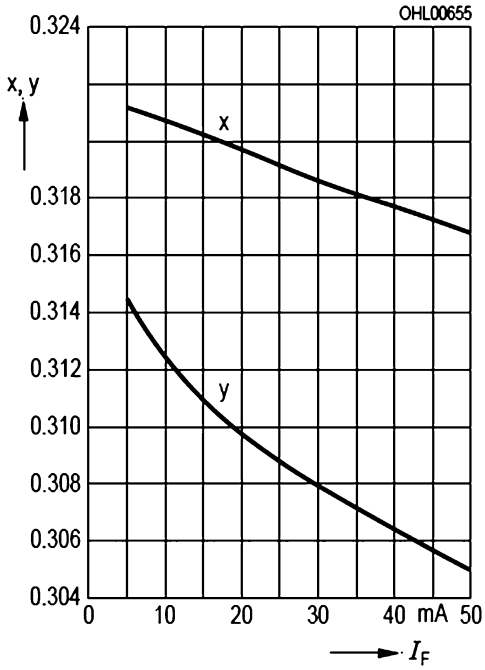


Fig. 4.28 Chromaticity coordinate vs. forward current for InGaN-based LEDs

Metal diffusion caused by high electrical currents or voltages at elevated temperatures can move metal atoms from the electrodes into the active region. Some materials, notably indium tin oxide and silver, are subject to electromigration which causes leakage current and non radiative recombination along the chip edges [32]. A way to mitigate these electromigration effects is using a barrier layer. This is typically done with GaN/InGaN diodes.

Color shift. Not only LEDs show color shift: metal halide lamps are notorious for color shift, incandescent bulbs color shift color when dimmed, linear fluorescent lamps may not color shift "much" however, improper maintenance practices can cause obvious luminaire color shift over time. The mechanism for intrinsic color shift of LEDs is not properly understood yet. External factors as changes in forward current cause shift in color as is illustrated in Fig. 4.28 [33]. This can be driver dependent, especially if more LEDs are in parallel.

Joule heating. This effect is known as droop and effectively limits the light output of a given LED, raising heating more than light output. Degradation from Joule heating is typical for high current use conditions; degradation from Joule heating is much faster than from electromigration [34] (see Fig. 4.29).

The current dependant time to failure, t_f, for both degradation mechanisms can be expressed by (4.3):

$$t_f = \frac{C}{I^n}, \tag{4.3}$$

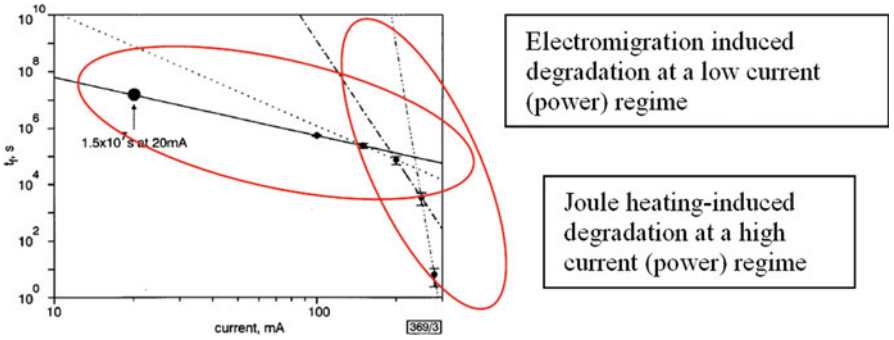


Fig. 4.29 LED degradation as function of forward current

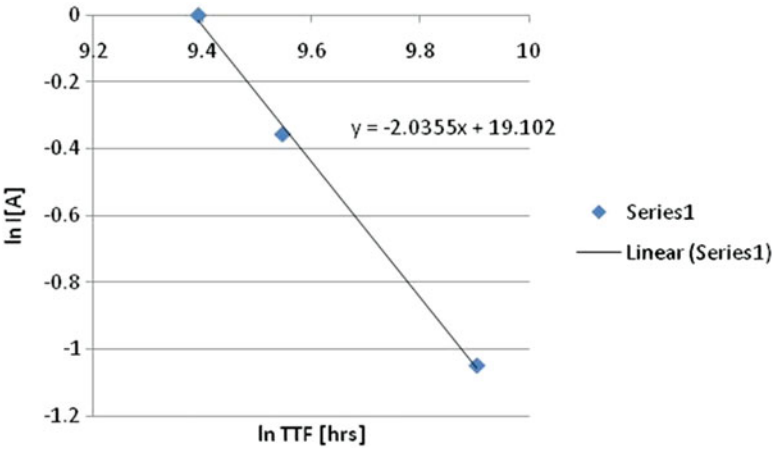


Fig. 4.30 Life time for InGaN Luxeon Rebel vs. forward current (based on data taken from Fig. 4.29)

with t_f, time to failure; C constant; I current; n, exponent, $n \approx 2$ for electromigration degradation and $n > 2$ for Joule heating.

From Fig. 4.30, data can be taken to estimate the exponent n in (4.2) for InAgN Luxeon Rebel [17]. The result is shown from the trend line in Fig. 4.31.

From Fig. 4.30, the exponent in (4.2) is close to 2, indicating most likely Joule heating as degradation mechanism is not happening under these conditions of T_j and I_f. Comparison between catastrophic failures and lumen depreciation is given in Fig. 4.31. From this, lumen depreciation is expected to be the dominant failure mechanism for LEDs rather than catastrophic failures [15].

4.2.1.3 Methods of Level 0 Failure (Degradation) Analysis

Many degradation modes give rise to the same "symptoms" of the device. To find out the exact cause of failure of a device, many analytical observational procedures

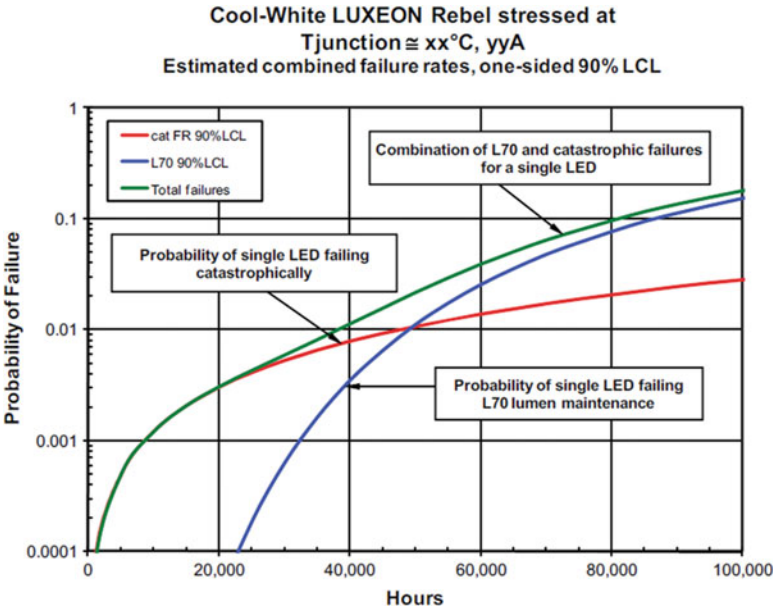


Fig. 4.31 Combined lumen maintenance and catastrophic failure model

have been developed. Often the root cause can only be found by combining several failure analysis techniques. Monitoring the *thermal characteristics* of a device is a good way to monitor the degradation of the device. Ways to measure temperature change in the device are to: watch the wavelength of emitted light, monitor the junction voltage, and to measure the difference in threshold voltage in pulsed and DC operation.

Optical microscopy is another way to monitor a device for characteristics related to failure. Optical microscopy methods measure the light emitted from electro- and photoluminescence and have a resolution of 0.25 μm.

Scanning electron microscopes (SEM) use an electron beam to observe the characteristics of a device. They can glean a lot of information from the device because the electron beam from the SEM induces many reactions in the optical device including Auger, backscattered, and secondary electron emission, X-ray emission, cathode luminescence, and induced current. Misfit dislocations can be revealed using *transmission electron microscopy* (TEM). Figure 4.32 shows an example of threading dislocations as observed with TEM.

Electrical methods can be used to monitor degradation: shift of *I–V* curve, measure the minimal current for light-on, leakage current at forward and reverse bias. As an example, Fig. 4.33 shows the result of a HTOL test performed as a step stress test at constant temperature of 100°C. The LED devices are held under a bias forward current for 1 day; after that, the minimal current for light-on was measured and the HTOL is continued for another day at a higher forward current level. Figure 4.33

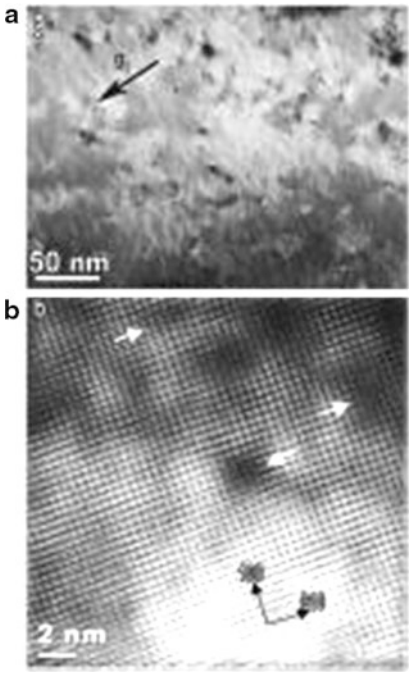


Fig. 4.32 TEM images from plan-view specimens of the 300 nm film: (**a**) bright field image of the TD distribution obtained with g5100; (**b**) HRTEM image with TD cores indicated by *arrows*

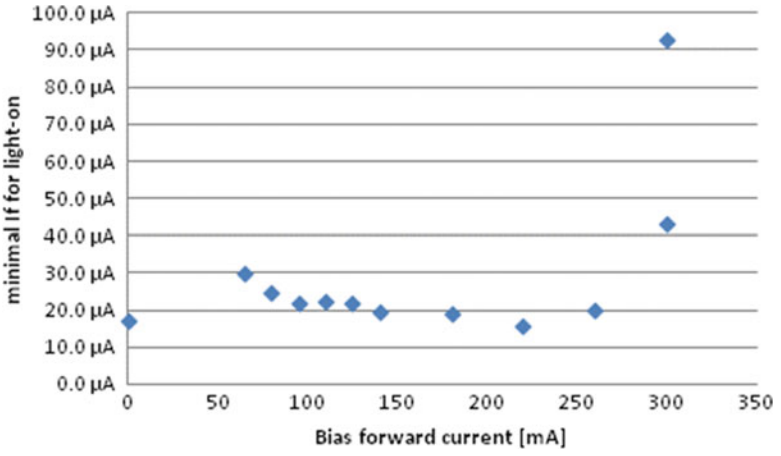


Fig. 4.33 Degradation of LED during HTOL in step stress mode

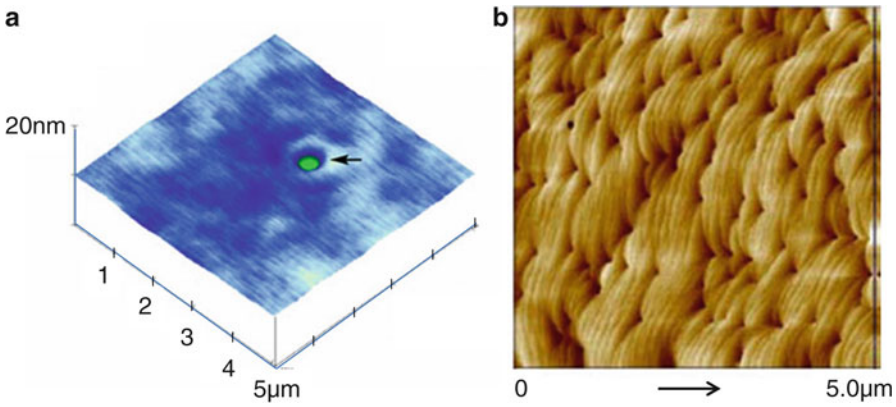


Fig. 4.34 LED defects observations using AFM. (**a**) Threaded dislocations in strained Si and (**b**) GaN surface parameters dislocation/defect/stacking faults

shows that from biasing at 300 mA onwards, the forward current for light-on starts to increase, indicating the start of degradation of the LED.

Surface metrology, e.g. using atomic force microscopy (AFM) can reveal nanometer scale surface roughness, e.g. from threading dislocations or threading disks and stacking faults as is illustrated in Fig. 4.34 [35, 36].

4.2.2 Failure Modes and Mechanism in Level 1

Increasing the electrical power density for the highest lumen output is one main approach to realize high power LEDs. Due to the increasing electrical power, the junction temperature of LEDS keeps increasing further which will further cause variable failures in the device level and thus decrease the lifetime of LEDs. This has been well discussed in previous section. Proper design of LED packaging and/or systems can somehow help cooling the junction and thus is very important to assure LED system reliability [37]. However, the packaging has its own weakness and variable failures will appear during applications following the degradation of the packaging materials or interaction with the LED device. It is often recognized that many critical failures in the LED systems locate in the packaging level, also addressed as level 1 in this chapter. Typical package failures which are well indentified in industry are discussed in this section.

4.2.2.1 Lens/Encapsulant Degradation

LED modules used in consumer applications are usually encapsulated with optically transparent encapsulant materials such as epoxy resin, silicone resin and so on. The shaped encapsulant materials around the LED chips provide a lever arm

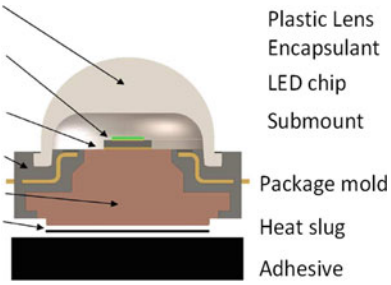


Fig. 4.35 Typical LED packages used in solid-state lighting applications LUXEON K2

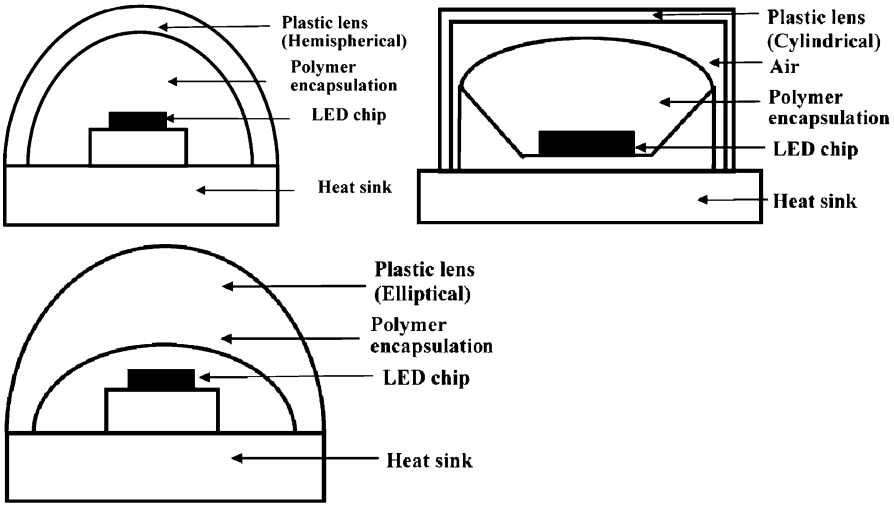


Fig. 4.36 Three shapes of LED lens: hemispherical; cylindrical; an elliptical shaped lens

for increasing light extraction. High power LEDs use a plastic lens as well as an encapsulant, as shown in Fig. 4.35 [17]. The encapsulant, used to protect the LED chip, is usually made with soft silicone in order to have low stress load from packaging and field use. The plastic lens is usually made with relatively hard materials to provide mechanical protection, and also serve as path for transferring the optics and heat to outside. The degradation of the encapsulant/lens often occurring during high temperatures operations is a typical reliability issue in LED applications. Main failure mode is decreased light output due to increased internal reflection at the lens/air interface during aging.

Thermomechanical stress is a factor of the lens degradation. Lens degradation occurs during high temperatures operations in a form of numerous hairline cracks. Thermal mechanical stress, hydro mechanical stress or poor processing are claimed to be the cause of this type of failures. The speed of lens degradation depends very much on the shape of the lens configurations. Three shapes of lens have been studied [38], see Fig. 4.36. It turns out that hemispherical-shaped lens can give a

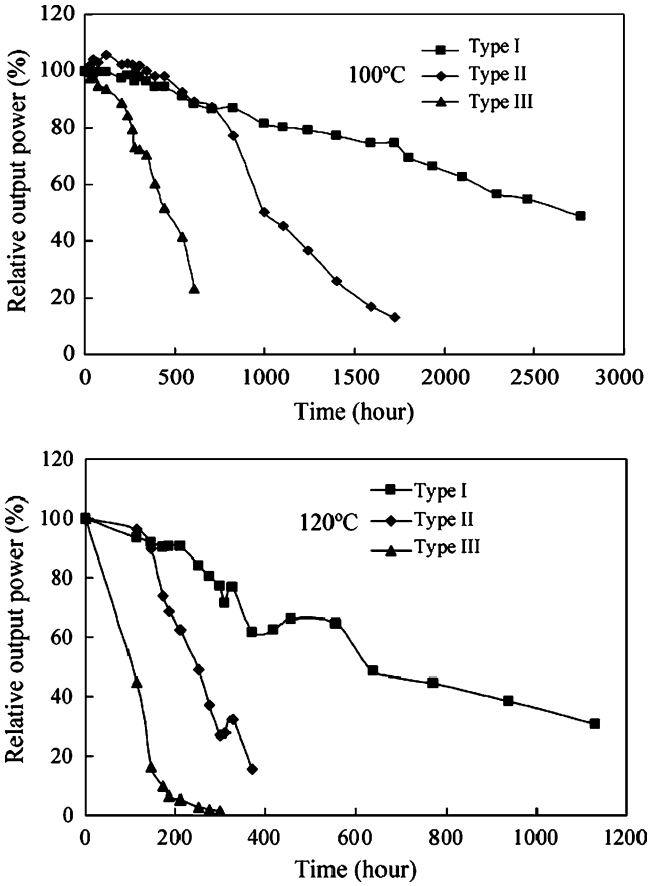


Fig. 4.37 Comparison of life time of different lens configuration

better thermal dissipation than cylindrical and elliptical shaped lens and thus exhibited a better lifetime. Figure 4.37 shows the relative light output and lifetime of each LED with different shaped lens during thermal aging at 100 and 120°C.

High humidity environment is another factor of LED lens/encapsulant degradation. At higher temperature and humidity, the hydrolysis of chains broken due to long term moisture absorption would be accelerated at higher temperature. This will cause the cloudiness and discoloration as the concentration of absorbed moisture within the lamp epoxy encapsulant reaches a high value and decreases the intensity of the lights. The unstable ester groups in the epoxy help the degradation.

Material properties of the encapsulant are also important factor to affect LED lens/encapsulant degradation. For low power applications with power <0.4 W, epoxy resin is normally used as an encapsulant/lens material because of its overall properties and cost advantage. Variable epoxy resins can give a large difference of thermal and molecular mobility under thermal and environmental loads and give



Fig. 4.38 Typical encapsulant yellowing in cycloolefin lens

different optical reliability. Normally bisphenol-A (Bis-A) epoxy resin is more thermally stable than cycloaliphatic epoxy resins because of the phenyl groups in the main chains, but the latter has better resistance to UV yellowing which is discussed later. High power LEDs use a soft silicone gel as the encapsulant because of its high transparency in the UV-visible region, controlled refractive index (RI), stable thermo-mechanical properties, and tunable hardness from soft gels to hard resins. But silicone suffers from issues, such as poor physical properties, poor moisture resistance, dust abstracting, and the need for outer layer protection.

4.2.2.2 Lens/Encapsulant Yellowing

When lens/encapsulants are exposed to radiation or high temperature for certain time, the molecular mobility will be increased which often leads to the scission of the polymer chain bonds via hydrolysis and the formation of thermo-oxidative cross-links and the epoxy resins will become yellow as shown in Fig. 4.38. The lens/encapsulant yellowing/discoloration are some of the critical failures in LED systems, especially for ultraviolet LEDs and outdoor applications. The failure mode of encapsulant yellowing is a decreased light output due to decreased encapsulant transparency and discoloration of the encapsulant. Epoxy resins are more sensitive than silicone to UV lights and high temperature operational environments and thus be more susceptible to yellowing.

The lens/encapsulants yellowing are probably due to (1) prolonged exposure to blue/UV radiation, (2) excessive LED junction temperature, (3) presence of phosphor, or (4) contact with metal silver with Cu impurities.

UV light is a factor of encapsulant yellowing. Down [39] tested the resistance of various room-temperature-cured epoxy resin adhesives to yellowing under high-intensity lights. It is found that light-induced yellowing is usually a nonlinear function of time. Four distinct types of yellowing curves were proposed depending

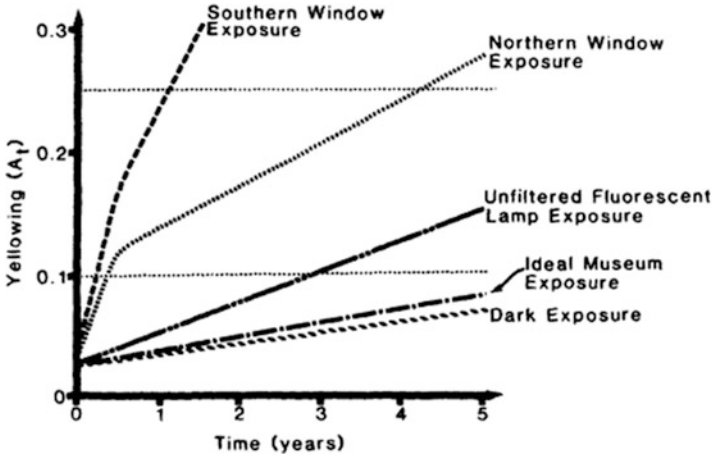


Fig. 4.39 Degree of yellowing of same epoxy material exposed to variable light intensities

on the amount and rate of yellowing to the light exposure time of variable epoxies: linear, autocatalytic (at an increasing rate), autoretard (at a decreasing rate), and initial bleaching, followed by a linear increase in yellowing.

Figure 4.39 shows the degree of yellowing of same epoxy material placed in different locations of the same building, to simulate the four levels of representative light intensities that might be found in a museum [5, 39]. These are (1) safe illumination from incandescent or filtered fluorescent sources such as an ideal museum environment; (2) high illumination from average unfiltered fluorescent source such as in a display case; (3) high illumination from unfiltered daylight, e.g. near a north window; and (4) direct sunlight, e.g. near a south window. It is demonstrated that the intensity of light exposure dictates the service life expectancy of any studied epoxy resin. Under low intensity irradiation, such as in an ideal museum environment, service life expectancy did not differ significantly from estimates made under natural dark aging. The average percent reduction in life expectancy on exposure to ideal museum conditions was about 10%. For the second, third and fourth representative lighting conditions, the average percent reductions in service life expectancy compared to natural dark aging were considerably higher-approximately 30, 60 and 75% respectively.

In addition, the extent of yellowing was monitored by measuring the absorbance of the wavelengths at 380 and 600 nm on variable available commercial epoxies, as described in (4.4) The absorbance values of A_t is proposed as 0.1 and 0.25 respectively for "slightly yellow" and "strongly yellow." Estimated service life expectancy for a thin film of 0.1 mm on many epoxy formulations can be seen in [39].

$$A_t = [A(380\,\text{nm})_t - A(600\,\text{nm})_t] \times \frac{0.1\,\text{mm}}{F}, \tag{4.4}$$

where: A_t, degree of yellowing; A, absorbance; T, time; F, average film thickness for each sample.

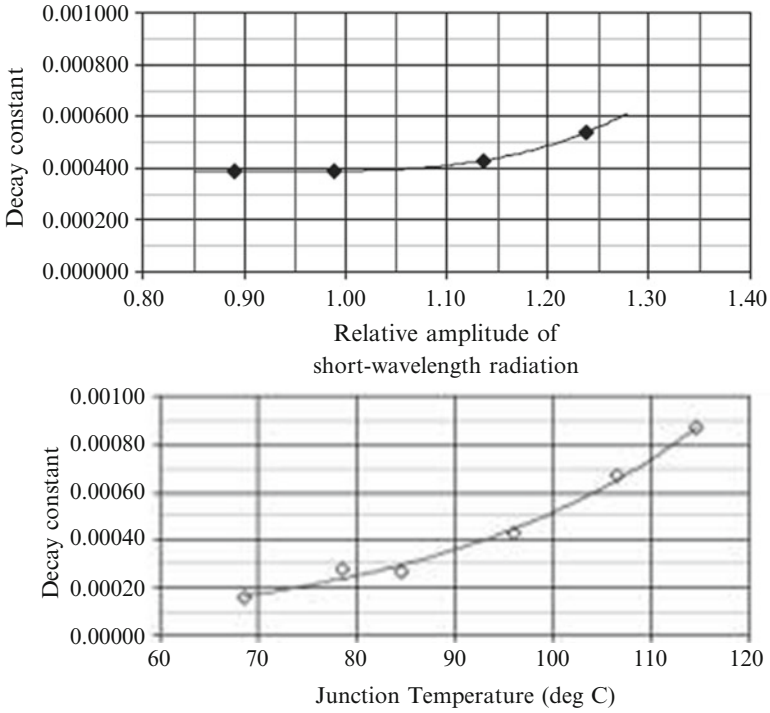


Fig. 4.40 Degradation rate of epoxy encapsulant as a function of short-wavelength and junction temperature, with: decay constant as a function of short-wavelength (*top*), decay constant as a function of junction temperature (*bottom*)

Excessive junction temperature is another factor of encapsulant yellowing. Temperatures of approximately 150°C were sufficient to alter the encapsulant transparency by pure thermal effects [40]. Many studies have claimed that thermal stress and prolonged light exposure would intensively accelerate the epoxy encapsulant yellowing [39, 41–44]. Experiments on 5 mm type white LEDs was carried out by Narendran [34] to see the effect of junction temperature and short-wavelength radiation on the degradation rate of epoxy encapsulants respectively. The results showed that the degradation rate depends on both the junction temperature and the amplitude of short-wavelength radiation. However, the temperature effect was much greater than the short-wavelength amplitude effect.

The effect of junction temperature and short wavelength on the decay constant can be seen in Fig. 4.40 (top and bottom).

Presence of phosphor accelerates yellowing of the encapsulants. White LEDs are usually phosphor-converted LEDs (pcLEDs) by utilizing a blue LED chip partially converted by the phosphor to obtain white emission [45]. Traditionally, the phosphor is dispersed within an epoxy resin that surrounds the LED die, Fig. 4.41a. Because the diffuse phosphor directs 60% of total white light emission back to the LED chip where high loss occurs, this configuration is least efficient. Later, a scattered photon

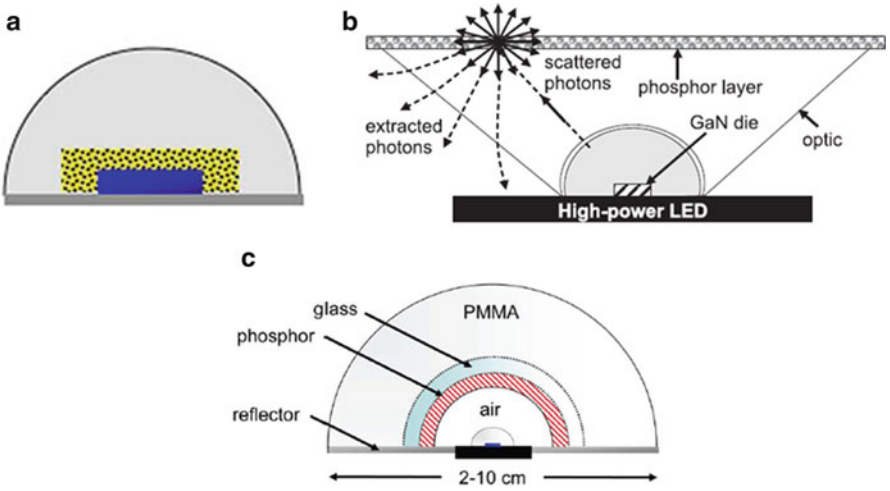


Fig. 4.41 Schematics of several pcLED packages: (**a**) conventional pcLEDs; (**b**) scattered photon extraction remote phosphor; (**c**) ELiXIR: remote hemispherical shell semitransparent phosphor with internal reflector

extraction pcLED is introduced by placing the phosphor away from the die. The backscattered photons can be extracted from the sides of the optic and the efficacy can be significantly increased. However, quite some losses still occur inside the phosphor layer due to quantum conversion loss and trapping by total internal reflection. The efficiency of pcLED was further upgraded with enhanced light extraction by internal reflection (ELiXIR), Fig. 4.41c [46]. The ELiXIR utilizes a semitransparent rather than diffuse phosphor layer that is separated from the chip by an air gap. It was claimed that the internal reflection at the phosphor/air interface redirects much of the backward phosphor emission away from the die and reflective surfaces without loss [46]. And the semi-transparency of the phosphor layer allows light to pass without deflection and escape the device more easily than diffuse phosphor layers.

Although phosphor is necessary to convert the blue light to white light, its existence increases localized heating and increases the speed of encapsulant yellowing. Narendran [34] carried out some functional tests with two operating currents 40 and 60 mA separately on three types of LED arrays: blue LEDs, blue LEDs with remote phosphor, and white LEDs (local dispersed phosphor). The test results show that the blue-plus-phosphor LEDs degraded at a rate slightly higher than the blue LEDs, and the LEDs with the phosphor layer away from the die degrades at a lower rate than white LEDs (see Fig. 4.42). And the degradations are mainly linked to the epoxy yellowing.

The yellowing of encapsulants may happen when the silicon resin comes in contact with silver metal including Cu impurities under heating. Hirotaka [47] carried out damp heat aging test on silicone resin (methylphenyl silicone) while the silicone resins are kept touching a silver plate and a ceramic glass respectively. After 1,000 h aging, the yellowing of the silicone resin touching the silver plate is

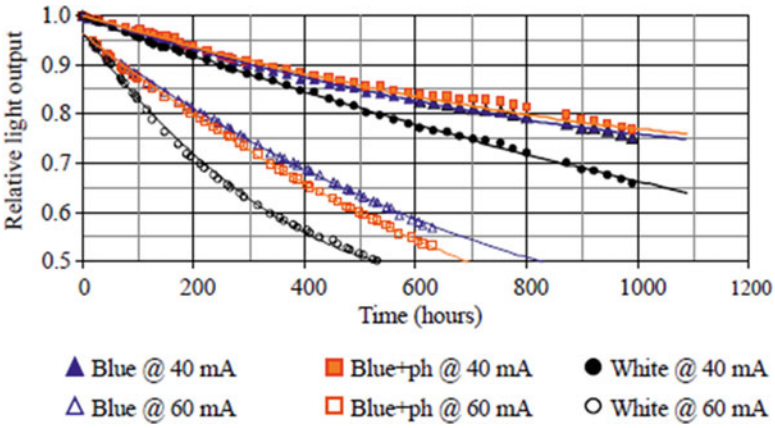


Fig. 4.42 Lumen depreciations for three LED arrays with/without phosphors

highly visible while no discoloration was found at least visually on the silicone resin on slide glass subjected to the same test. ESR analysis on the samples before and after thermal test showed that there were changes in the valence of the transition metal ions in the discolored silicone resin (Fig. 4.43) and the transition metal ions were identified to be Cu^{2+}. In addition, FT-IR analysis indicates the generation of the −OH bonding of an organic acid (carboxylic acid) in the discolored samples. Therefore, it is speculated that the reason of the discoloration is that the heat activates a minute amount of copper impurities in the silver, and then the carbonization of broken-down phenyl radicals and the bonding of released phenyl radicals with additives cause the conjugated system to shift toward long wavelengths.

4.2.2.3 Delamination

In the micro-electronics industry, delamination is a key trigger of many observed reliability issues: for example, the die-lift-downbond stitch breaks associated with die pad delamination and passivation cracks related to interface delamination between chip and molding compound. Delamination is mainly driven by the mismatch between the different material properties, such as CTE (coefficient of thermal expansion), CME (coefficient of moisture expansion or hygro-swelling), vapor pressure induced expansion, and degradation of the interfacial strength due to moisture absorption [48, 49]. Among them, the effect of hygroscopic mismatch strains is often ignored in the reliability valuations. However, when materials like epoxy or silicone are involved, the hygroscopic mismatch strains can be comparable to, if not higher than, thermal mismatch strains [50].

In LED packages, the possible locations of delamination in level 1 are between the chip or phosphor layer and lens/encapsulant, chip and phosphor layer, chip and die attach layer, die attach layer and submount. Figure 4.44 shows several typical delamination observed in level one of LED packages.

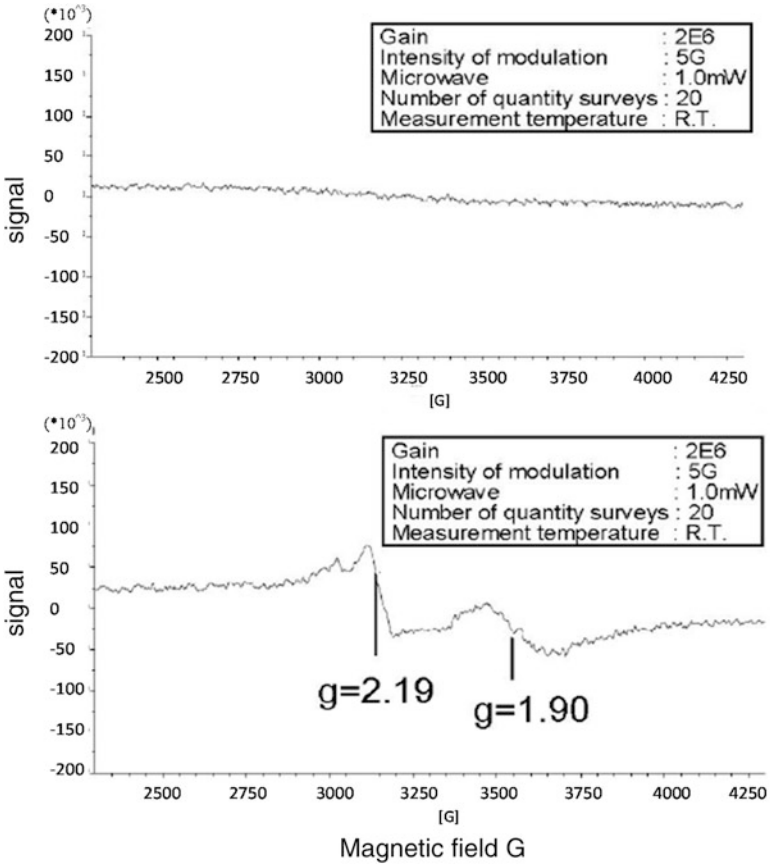


Fig. 4.43 ESR spectrum comparison (broad range) between and after thermal aging test

When delamination happen in the optical path of LEDs, e.g., between the chip and the phosphor, and between the chip and lens/encapsulant, light output will be reduced or LED color will be shifted and local accumulated heats will reduce the LED life time further. When delamination occurs in the thermal interconnect, the thermal resistance will be increased, and thus the junction temperature will be increased. Finally, the lifetime of LEDs will be decreased too. The significant increases are found, however, only after the delamination are more than 60% of the interconnect area, see Fig. 4.45. In most cases, partly delamination would not cause catastrophic failures. But when wire bonding is involved as the electrical interconnect of the LED chips to outer world, delamination between the chip and lens/encapsulant could pull the wire up, fatal failure like shifted wire bonds would be caused, see Fig. 4.46, especially when relatively hard silicone/epoxy are used as the lens/encapsulant materials.

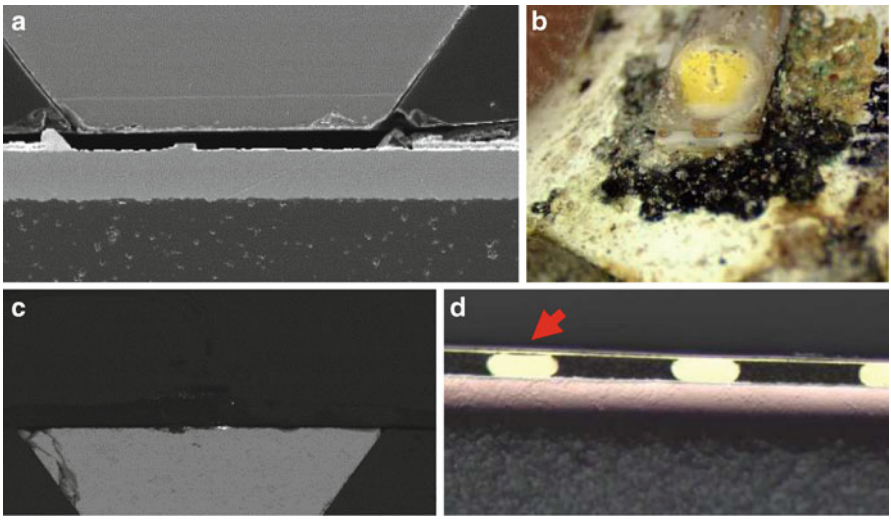


Fig. 4.44 Typical delamination in LED packages. (**a**) Delam between die vs. submount, (**b**) Delam between lens and submount after accelerated salt spray + humidity test, (**c**) Delam between die coating and die, (**d**) Delam between die and die attach interconnect

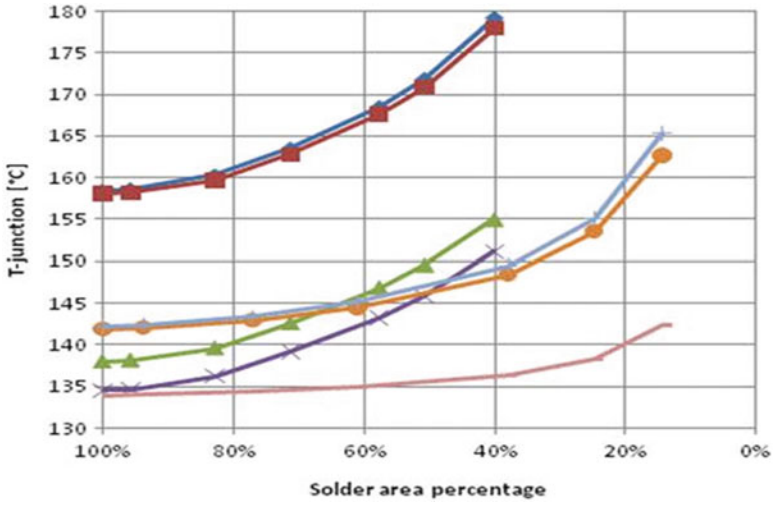


Fig. 4.45 Effect of interconnect area % on the T_junction for different configurations

Thermo-mechanical and hydro-mechanical stress is mostly the main cause of delamination. It is a key to minimize the delamination risk by considering compatible materials in thermal expansion and hygro-swelling in the design phase, especially for high temperature and outdoor applications. In addition, the interface

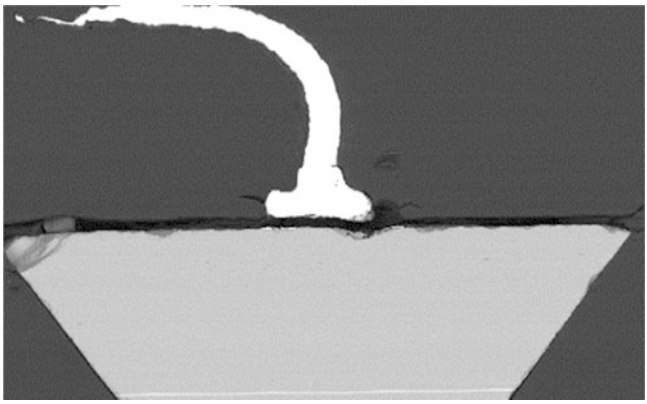


Fig. 4.46 Wire joints pulled off by silicone

strength of adjacent materials highly affect on the delamination too. The risk of delamination in a new packaging can be assessed by combining finite element simulation and characterization of the interfacial strength or toughness [51–53]. Regarding the characterization, a few techniques which have been used in the microelectronics industry can be well explored [53]: (1) button shear/tensile test; (2) dual or double cantilever beam test; (3) wedge test; (4) modified ball-on-ring test (or blister test); and (5) 4-point bending with pre-notch crack.

4.2.2.4 Failures in Die Attach in Level 1

In normal LED packages, the LED chip is assembled on a submount or LED carrier with a die attach material in between. Promising die attach in LED package should have high thermal conductivity to provide effective cooling path so that the junction temperature can be controlled in a healthy level to assure intensified optical power. In addition, the die attach should be robust enough to resist the stress due to CTE mismatch between the LED and the submount. In current LED products, eutectic AuSn is well used as die attach technology in many products because of its superior thermal conductivity and resistance to creep than other die attaches, e.g., Sn based solder paste and Ag paste. In addition, eutectic AuSn (gold/tin) alloy provides high joint strength and high resistance to corrosion. AuSn alloy is also compatible with precious metals. However, the process of AuSn assembly is very critical due to the fact that multiple phases could be formed by dissolving Au from the component/substrate finish into the solder during assembly. Often, many efforts are needed to optimize the process to assure a good quality in the die attach layer. Sometimes, the potential assembly problem is not visible, but as a potential risk to reliability later. As it is typically a fluxless process with preform, local poor wetting of the assembled component to the AuSn die attach is one of the risks which will cause low interface strength and lead to the interface delamination later, see Fig. 4.47. A non-homogeneous microstructures is another risk which makes the

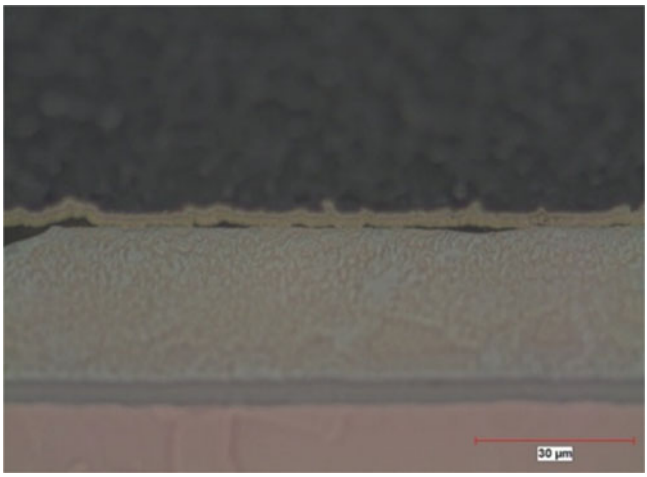


Fig. 4.47 Local poor wetting of AuSn interconnects

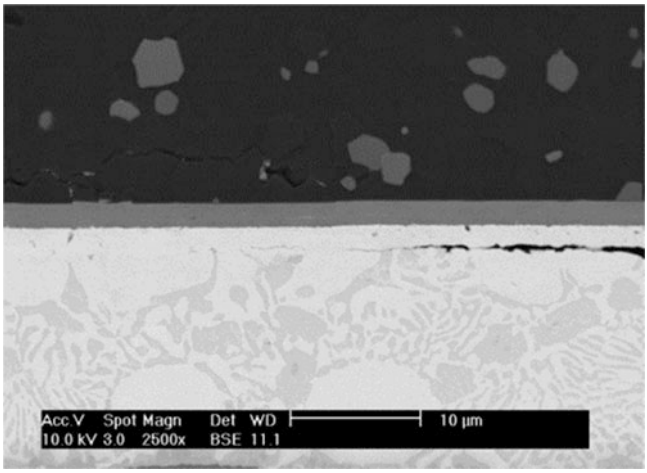


Fig. 4.48 Non-eutecticAu/Sn microstructure

mechanical strength lower than the normal level. And the crack can be easily formed along those large grains boundary, see Fig. 4.48. Sometimes, large voids are observed: see Fig. 4.49.

In addition, the soldering temperature of eutectic AuSn is much higher than conventional Pb-free solders, and thus, the assembly introduces a lot of residual stress to the assembled component and substrate. This may result failures like die cracks, delamination in the component plating layers, or crack/delamination in the substrate, see Fig. 4.49. Even in a good quality product, the fatigue damage in the die attach under cyclic thermal loads may happen after certain cycles of use



Fig. 4.49 Void in AuSn interconnect

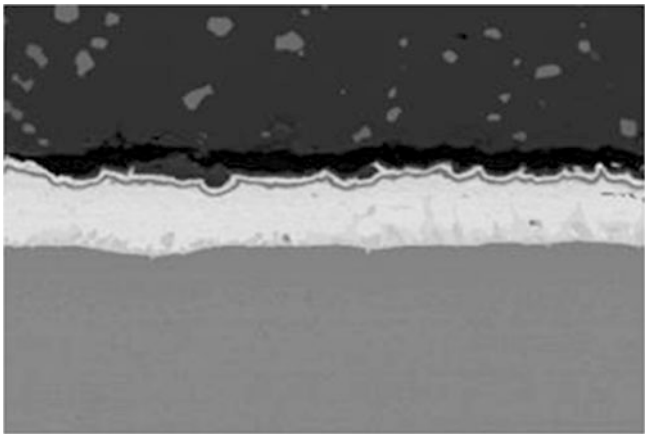


Fig. 4.50 Delamination along the component plating interface

in the applications, especially for high power LEDs. Global thermal expansion mismatch between the component and the substrate, and also the local mismatch between the die attach material and the component or the substrate, the fatigue crack will start in the corner of the highly stressed interface. The crack often propagates along the intermetallic layer Fig. 4.50.

4.2.2.5 Wire Bonding Failure

Wire bonding is one of widely used methods to connect electrically the LED chips to the submount. Typical wire bonding process is to form a ball bond on the LED chips by applying ultrasonic energy, pressure and heat, which is followed by forming a stitch bond on the plating layer of the LEDs submount. Typical failures in wire bonding are wire broken, chipping out under the wire bond, or wire ball

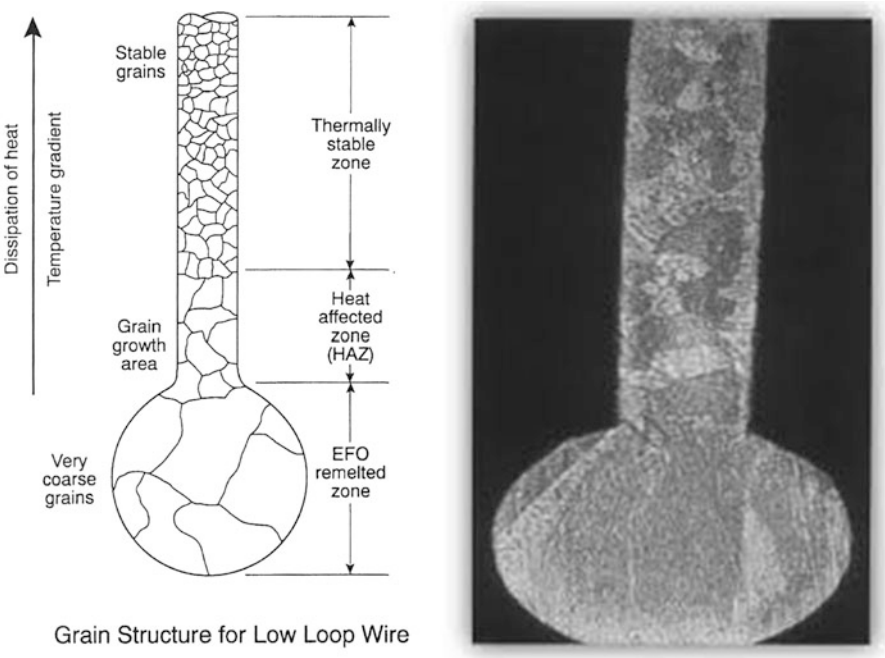


Fig. 4.51 The grain structure for an Au bonding wire after ball formation, showing the heat affected zone

bond fatigue. Most wire bond failures are catastrophic. Gold wires for ball bonding are made in the annealed condition. During ball formation, the part above the ball addressed as the wire neck or heat affected zone (HAZ) becomes annealed and thus would be much weaker than other zones of the wire, especially for low loop wires. In Fig. 4.51, the HAZ is the weakest part of the wire [54]. The wires usually break in this zone under a pulling stress (Fig. 4.52). In LED package, the pulling stress often comes from the thermal expansion mismatch between the encapsulants and the LEDs chip (Fig. 4.52) [55].

When the wire is subjected to a repetitive pulling or bending, such as following the expanding and shrinkage of the encapsulant, even though that stress is lower than the wire's fracture strength, the wire may break after certain cycles as a result of fatigue fracture, see Fig. 4.53 shows S–N curves (stress/strain vs. the number of cycles to failure) for most bonding wires are available. Figure 4.53 shows a typical S–N curve of Au bondwire with a diameter of 32 μm [54]. For improving the wire fatigue performance, in addition to design thermal compatible materials of the encapsulant and the LEDs chip, to optimize the wire loop can benefit a lot. A simple rule for this is to make the ratio of wire loop height to the space of two bonds as high as possible. Figure 4.54 shows that effect on bond pull force of increasing the loop height while the bond spacing is constant.

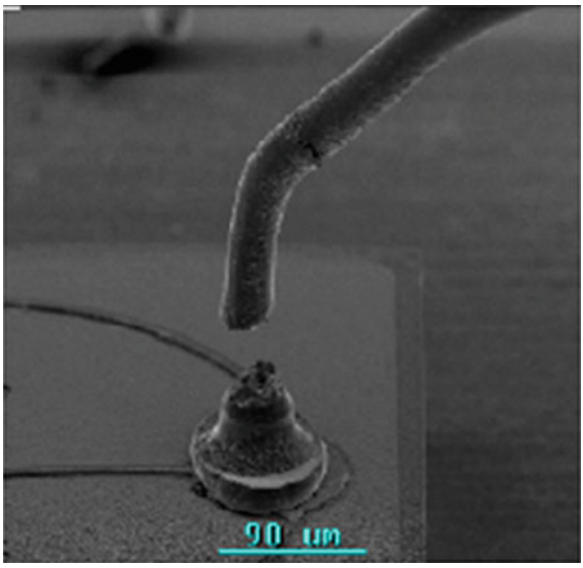


Fig. 4.52 Wire broken in one LED packages after half year usage

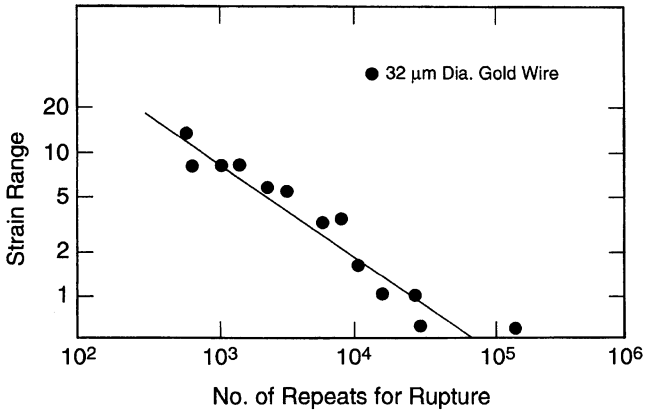


Fig. 4.53 S–N curve for 32 µm Au bonding wire

When the current stress or temperature exceeds the maximum recommended values or gets close to that for long periods of operation, thick intermetallic layer between the wire and the bond pad can be formed. The layer is very brittle and cracks can be easily formed in this area to make the contact open or partly open. This type of failure can be simulated and assessed by accelerating high temperature storage test. Figure 4.55 shows gold-ball bond fracture after 3 weeks storage at 175°C. These

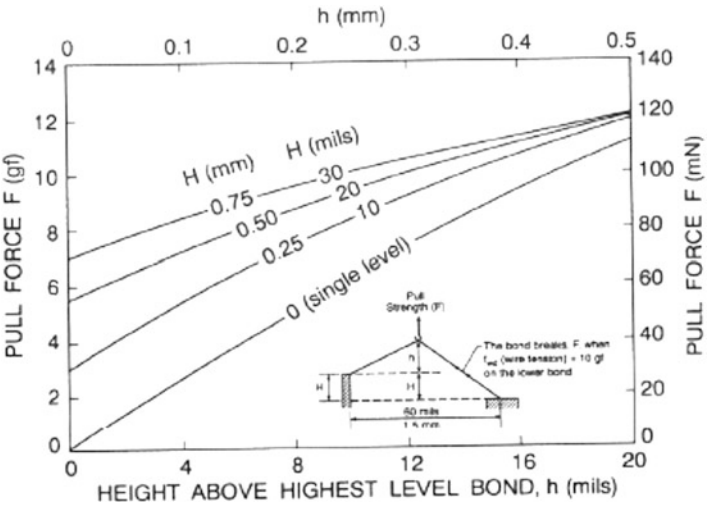


Fig. 4.54 Calculated bond pull force with various loop heights and bondpad heights, pulled in the center of the loop

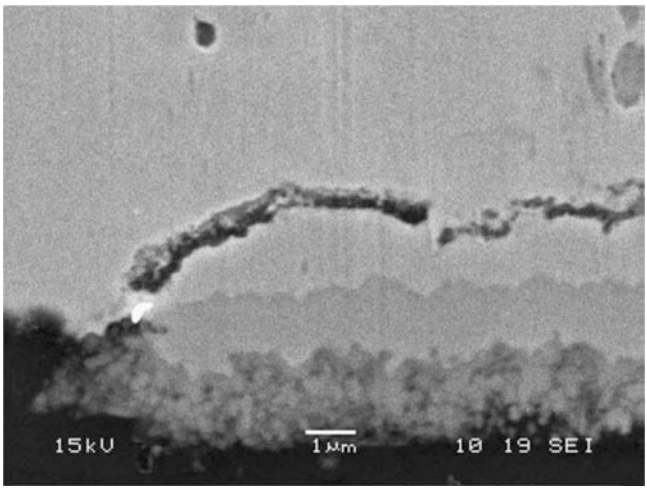


Fig. 4.55 SEM image of gold-ball bond fracture after 3 weeks storage at 175°C

phenomena can also be seen in LED package when high current stress is applied for a long period of operation, the bonding contact area evaporates as an effect of excessive heating. Sputtering is visible in the scanning-electron-microscope image of the contact area [56], see Fig. 4.56.

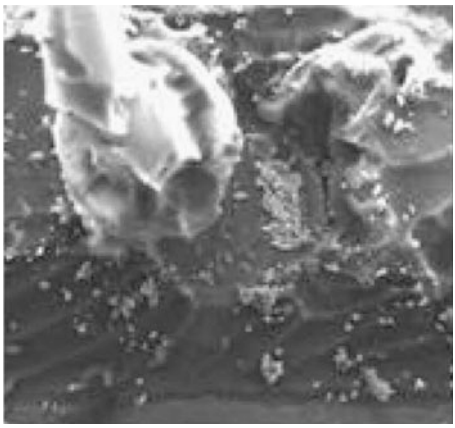


Fig. 4.56 Detail of the contact area is enlarged

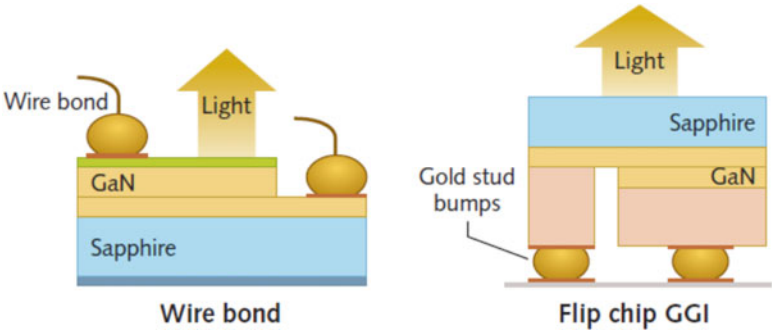


Fig. 4.57 LED constructions: (*left*) with wire bonding; (right) with GGI

4.2.2.6 GGI Failures

Gold to gold interconnection (GGI) flip chip bonding technology has been developed to connect the driving IC to integrated circuit suspension in the areas of semiconductor assembly. In typical GGI process, the Au bumps and Au bond pads in the substrate are joined together by heat and ultrasonic power under a pressure head. As a general interconnect technology, the advantages of GGI include: high interconnect strength, thermal conductivity, and low electrical resistance superior to a solder joint produced by conventional flip chip methods; fast process development path by joint development of the available stud bump and flip chip die attach process; gold stud bumping on a wafer by using traditional wire bond technology with no need for a UBM or redistribution layer; and a lower cost of ownership and lead free process.

In LED markets, traditional wire bond processes to connect the LEDs chip to drivers is being modified to the flip chip GGI attachment method, see Fig. 4.57.

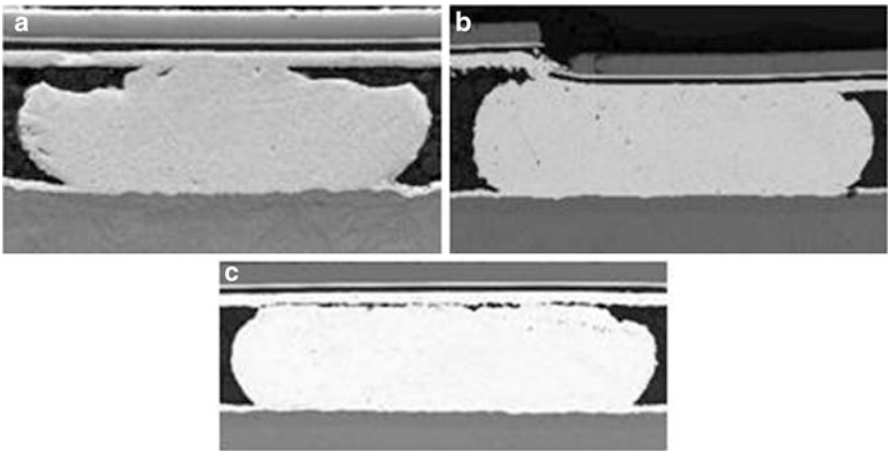


Fig. 4.58 Failures in GGI interconnects. (**a**) Improperly formed GGI. (**b**) Cracks in the LED chip. (**c**) Bonding failures due to contamination

By doing this, the light output can be largely improved because of several advantages: (1) the wire bond which blocks the light output is eliminated; (2) light can be projected out through the transparent carrier, e.g. sapphire to enhance light emission; and (3) higher power can be applied because the inherently thin metal current spreading layers is replaced by the flip chip contacts. In addition, from reliability point of view, the risk of failure induced in wire bonding is well reduced, including the electrical overstress induced bond wire fracture, wire ball bond fatigue, and wire broken due to cyclic encapsulant shrinkage or delamination from the die in application.

The failures in GGI are highly related to the process control. If the ultrasonic time of the thermosonic bonding is not long enough or the bonding pressure is not high enough, the Au bumps/pads may not be softened enough to deform properly in the processing. And then, the Au bump only partly contacts with the Au pad, see Fig. 4.58a. Fractures would happen in such a GGI due to the poor resulting shear strength. However, if the bonding pressure or ultrasonic energy is too high, damage to the device from bonding may be caused, see Fig. 4.58b. If the ultrasonic power is not well optimized and the surface of the bumps is contaminated, delamination may happen directly after the bonding, see Fig. 4.58c.

In addition, the bonding temperature, the coplanarity and alignment of Au bumps/pads are important factors to determine the GGI failures too. When the chuck temperature during thermosonic bonding is too low, the Au bumps/pads will be less plastically deformed and the bonding areas could be not big enough to give strong bonding strength. Fractures may happen later. However, if the bonding temperature is too high, the substrate may suffer from large warpage before bonding which will affect on the bonding strength too. GGI fractures will cause the contact resistance to increase which will lead to light output degradation directly. Indirectly, the junction temperature will be increased and LEDs life time will be shortened.

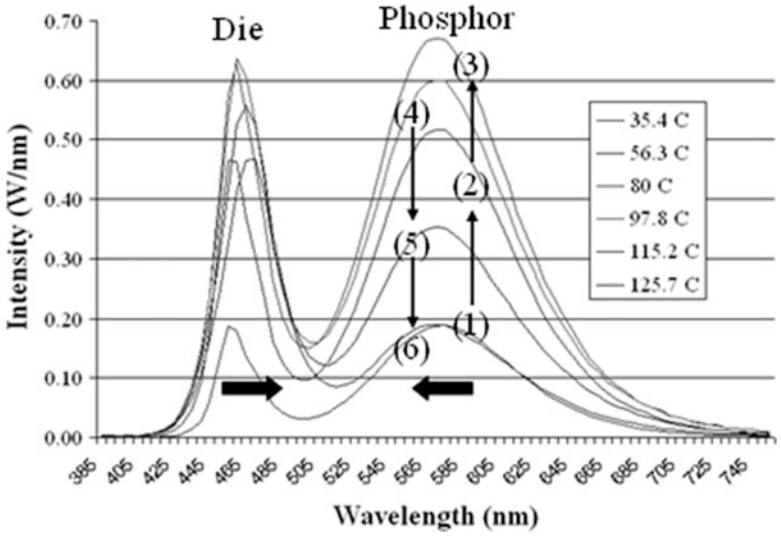


Fig. 4.59 Shift of phosphor spectra with the increasing temperature

4.2.2.7 Phosphor Thermal Quenching

In phosphor converted LEDs, part of blue light emitted by LEDs chip is converted to yellow light by phosphor which will mix with the other part of blue light to emit white light to outside. The quality of the white light highly depends on the converting efficiency of the yellowing emitting phosphors. During the converting process, the phosphor layer will produce heat due to Stoke's shift energy loss [57, 58], which will decrease the phosphor conversancy. Phosphor thermal quenching means that the efficiency of the phosphor is degraded when the temperature rises. Generally, it is required that phosphors for white LEDs have low thermal quenching to maintain long consistency in the chromaticity and brightness of white LEDs. However, it is very difficult to avoid phosphor thermal quenching, especially in a long life period. Phosphor thermal quenching will lead to typical failure modes of LEDs package like color shift or reduced light output. The driving forces are high drive current and excessive junction temperature, which are attributed to relatively poor thermal design in the packaging. With increasing temperature, the nonradioactive transition probability by thermal activation and release of the luminescent center through the crossing point between the excited state and the ground state increases, which quenches the luminescence. The electron–phonon interaction is enhanced at high temperature as a result of increased population density of phonon, which broadens FWHM [59]. Figure 4.59 shows the shift of phosphor spectra with the increasing temperature.

The most convenient way to study the degradation of the package/phosphors system is to carry out thermal stress tests by submitting the LEDs to high

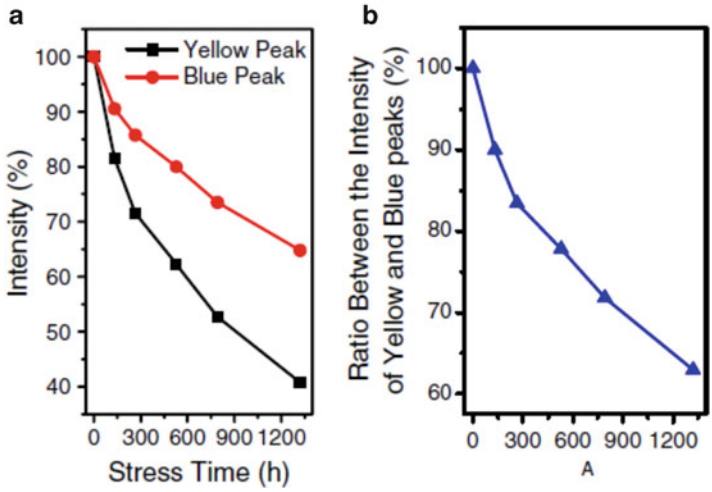


Fig. 4.60 Different intensity of blue and yellow luminescence of a white LED under stress at 140 °C, no bias

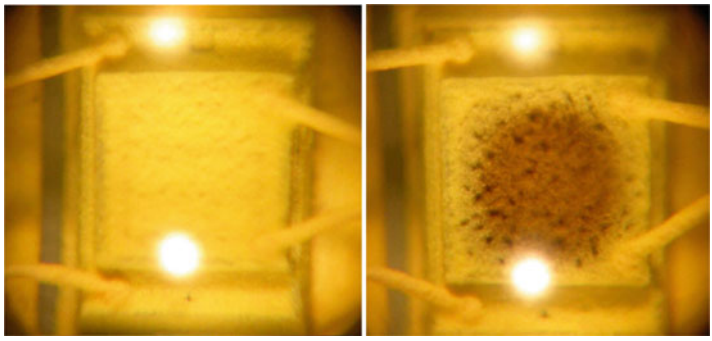


Fig. 4.61 Micrograph of two white LEDs; *left*: untreated sample; *right*: after stress at 100 A cm^{-2}, 120°C

temperatures without any applied bias, because phosphors and package usually degrade under a range of temperatures between 100 and 200°C while the LED chips are quite stable within this temperature range [60]. In this way, the degradation is supposed to happen in the packaging and the phosphor. Meneghesso et al. [60] reported a spectral power distribution (SPD) of a white LED submitted to stress at 140°C with no bias. Besides the overall optical power decrease, stress induced a significant decrease in the intensity of the phosphor-related luminescence with respect to the main blue emission peak, see Fig. 4.60. It is also stated that the degradation modes can take place as well as devices are submitted to stress at moderate current levels with junction temperatures greater than 100–120°C. A significant browning of the phosphorous layer in the proximity of the center of the emitting area are found in LED devices stressed at 100 mA with a temperature of 100°C, see Fig. 4.61. This

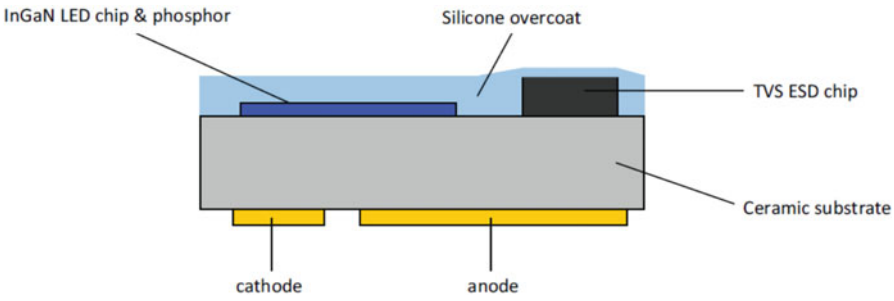


Fig. 4.62 Luxeon type C packages (schematically)

study indicates that high LED junction temperature under operation can result in a significant quenching of device luminescence and in the modification of the spectral properties of the LED.

The temperature dependant phosphor thermal quenching is described by fitting the Arrhenius equation [61]:

$$I(T) = \frac{I_0}{1 + c\ \exp\left(\frac{-E}{kT}\right)}, \tag{4.5}$$

where I_0 is the initial intensity, $I(T)$ is the intensity at a given temperature T, c is a constant, E is the activation energy for thermal quenching, and k is Boltzmann's constant. Xie [61] gives typical activity energy activation energy E of 0.23 and 0.2 eV for two proposed green _sialon:Yb2+ and red Sr2Si5N8:Eu2+ oxynitride/nitride phosphors.

4.2.2.8 Yellowing of the Die

When blue LED chip is stressed with certain current level for certain time, its surface becomes yellow. This phenomenon is addressed as yellowing of the die. Yellowing of the die is typical failures recognized for LEDs with silicone overcoat or encapsulant. The failure mode is decreased light output or color shift due to the yellowing surface of LED chip (Figs. 4.62 [10] and 4.63).

As we have discussed previously, most LED packages consist of an encapsulant/lens layer as the optical extractor. In current LED packages, most of them are with encapsulants of silicone. Silicone is gas permeable. Oxygen and volatile organic compound (VOC) gas molecules can diffuse into the layer. VOCs and chemicals may react with silicone and produce discoloration and surface damage which may affect the total light output or change the white color point. Heat and enclosed environment are two necessary conditions for the reaction to occur. In an enclosed environment, the VOCs diffuse into the silicone and may remain in the silicone dome. Under heat and "blue" light, the VOCs inside the dome may partially be oxidized and create a

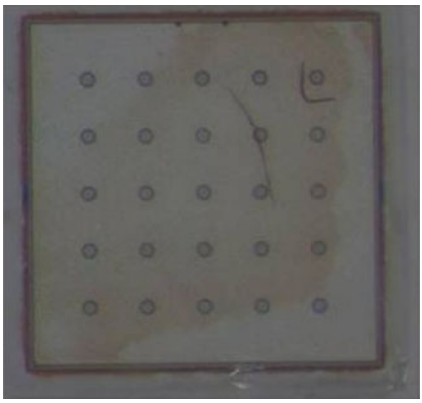


Fig. 4.63 Yellowing is visible on top of LED chip in LED packaging with silicone overcoat after stressing at certain current overnight

silicone discoloration particularly on the surface of the LED where the flux energy is the highest. In the open environment, the VOC has a chance to evaporate out the silicone and leave away. The VOCs may originate from adhesives; solder fluxes, conformal coating material, potting material and perhaps the type of ink printing used on the PCB. Once recognized chemical is rosin based flux with main component of abietic acid which can react with silicone to produce the yellowing of die. Since the yellowing of the die is very difficult to reproduced, simulation test and prediction is very difficult. Therefore, precautions should be paid to avoid incompatible chemicals to existing in the neighborhood of silicone, for example, the flux residue. In addition, rewards can be given by design the LED package in an open environment to assure certain air flow about the encapsulants.

4.2.3 Failure Modes and Mechanism in Level 2

LED packages are usually connected to a metal heat slug which provides a mechanical connection, thermal and/or electrical path from LED devices to drivers. This level of connection is addressed as level 2 interconnect previously. Two typical level 2 interconnects of LED packages are shown in Fig. 4.64: interconnects by using conventional assembly technologies, e.g. SMT, and mechanical connection by using clamps combined with thermal grease between the LED packages and heat slug.

In high power LED packages, thermal problem is still a bottleneck to limit the stability, reliability, and lifetime of LEDs. Effective thermal design with low thermal resistance from the LED junction to ambient is critical to improve the performance of LEDs. The choice of level 2 interconnects including the heat slugs play a significant role to determine the thermal resistance of whole LED system. The interconnect needs to have not only a good thermal conductivity, but also prolonged thermal stability and fatigue resistance. It is often seen that the level 2

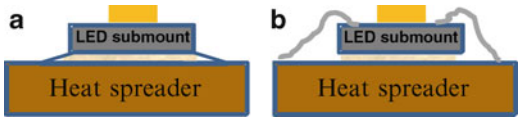


Fig. 4.64 Typical level 2 interconnects in LED packages: (**a**) interconnects by using conventional assembly technologies, e.g. SMT, (**b**) thermal grease with mechanical clamps

interconnect itself gives an even weaker thermal resistance and thus lower lifetime than the LED device. Therefore, it is essential to pursue a reliable level 2 interconnect in order to assure the reliability of whole LED system.

Generally, the main assembly technologies in LED level 2 interconnects are surface mounted soldering interconnects; adhesive interconnects with highly filled particles like silver filled epoxies, and mechanical clamping with a thermal interface material. Each assembly has its own degradation mode and failure mechanism which are discussed in the following section.

4.2.3.1 Solder Interconnect Fatigue Fracture

Using conventional SMT assemblies in level 2 interconnects of LED packages is very attractive because of the wide accessibility and maturity of the process, especially when traditional Pb_free solder: SAC(Sn–Ag–Cu) based solder alloys are used. However, solder interconnect fatigue is often a dominant failure mechanism in LED applications from two interactive aspects. One is the relatively high temperatures of LED in application which would drive the solder creep strongly: the higher the temperature, the higher the solder creep rate. The other one is global CTE mismatch between the LED submount and the heat slug which is normally made of ceramic and MCPCB respectively, which would apply high mechanical stress in the solder interconnects when temperature changes. The stress will increase the solder creep rate further, and the creep will cause the stress relaxation. As a result, the solder will experience deformation in response to applied mechanical stresses, cyclic creep and stress relaxation during cyclic power on/off [62–65]. This will lead to solder fatigue fractures, see Fig. 4.65.

Solder fatigue is a typical wear out failure. The fatigue fracture could cause the degradation of electrical connections, thermal resistance increase, as well as the degradation of the LEDs with time. Solder fatigue depend on solder material properties, especially the creep resistance; material compatibility, e.g. CTE; geometries such as the interconnect thickness, the size of the submount and interconnect shapen/array design. For high power LED applications, the creep resistance of solder interconnect could be a primary factor to the final life time of the products. The creep rate of tin–silver–copper-based solder alloys are reviewed and compared with high-lead solder which is typical solder material for high

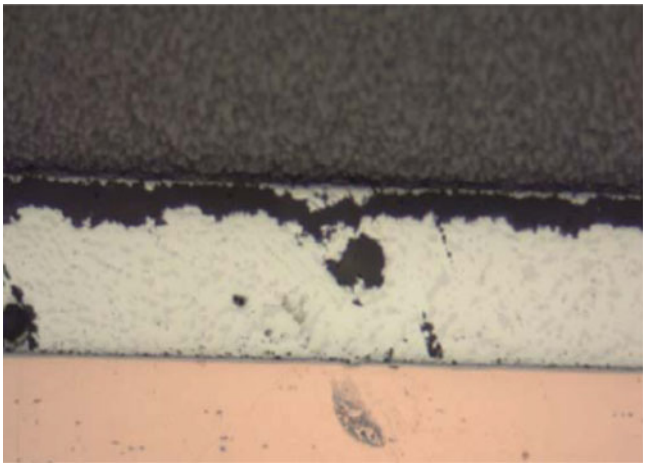


Fig. 4.65 Typical solder fracture due to creep-fatigue under thermal cyclic load environment: (cross-section)

temperature applications like automotive. The summary is given at room temperature 20°C and a high temperature 150°C, see Fig. 4.66. It can be seen that all SAC alloys give much higher creep rate than high-Pb solder. Innolot(SAC+) was claimed to have a better creep resistance than other SAC alloys at high temperature, which can be seen in the summary at high temperature. However, its resistance to creep is still far away from high-Pb solder alloy. Eutectic AuSn solder has much higher creep resistance than SAC based solder and it is expected to be most robust Pb_free interconnect material to resist creep fatigue. But it has its own weakness, especially from processing point of view which has been discussed in previous section.

Choosing CTE compatible materials as the LED submount and the heat slug would help reducing the mechanical stress and thus decrease well the risk of the solder fatigue fracture within targeted life time. For example, if the submount is made of ceramic, choosing MCPCB with Cu base metal would give less stress than with Al base metal. In addition, optimizing the geometry, e.g. the interconnect thickness will help increase the fatigue life time largely: the higher the thickness, the more relaxed stress from global CTE mismatch. It is estimated that the solder fatigue life can be at least two times higher if the thickness can be doubled. Above all, trying to use small LED component/submount and to optimize the solder interconnect shape would be rewarded by increased solder fatigue life too.

The best approach to estimate field product reliability is to extrapolate test failure times to field conditions using acceleration transforms, given the task to evaluate the reliability of Pb-free assemblies in the field application in the absence of field data. Several life prediction and acceleration factor (AF) models for thermal cycling of Pb-free solder interconnects are available [66–69]. Some are strain-based models that follow a Coffin-Manson type of fatigue law, for example, the

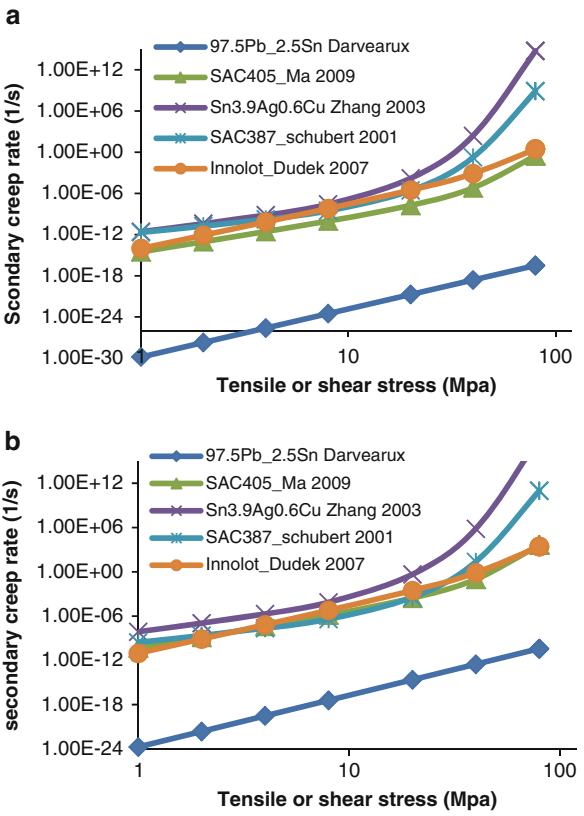


Fig. 4.66 Secondary creep strain rate vs. tensile stress for different SACxx alloys at room temperature and at 150°C. (**a**) Temperature = 20°C. (**b**) Temperature = 150°C

Engelmaier models. Some are strain energy density based in which cycles to failure go as the inverse of strain energy density per cycle as per Morrow's type of fatigue laws. The strain energy density is derived from stress/strain hysteresis loops that are obtained by finite element modeling. Jean-Paul Clech's life model is a typical strain energy based model and some additional factors, e.g. the hot and cold dwell times, are well considered in the model development [66]. Jean-Paul Clech's life mode based on Norris-Landzberg for SAC105/305/405:

$$\mathrm{AF} = \left(\frac{\Delta T_1}{\Delta T_2}\right)^2 \left[\frac{1 - c \cdot \Delta T_1^{-1}\left(t_{\mathrm{cold},1}^{-0.19275} \cdot \mathrm{e}^{705.5/T_{\mathrm{min},1}} + t_{\mathrm{hot},1}^{-0.19275} \cdot \mathrm{e}^{705/T_{\mathrm{max},1}}\right)}{1 - c \cdot \Delta T_2^{-1}\left(t_{\mathrm{cold},2}^{-0.19275} \cdot \mathrm{e}^{705.5/T_{\mathrm{min},2}} + t_{\mathrm{hot},2}^{-0.19275} \cdot \mathrm{e}^{705.5/T_{\mathrm{max},2}}\right)}\right]. \quad (4.6)$$

Engelmaier's life model based on Coffin-Manson law for SAC305/405:

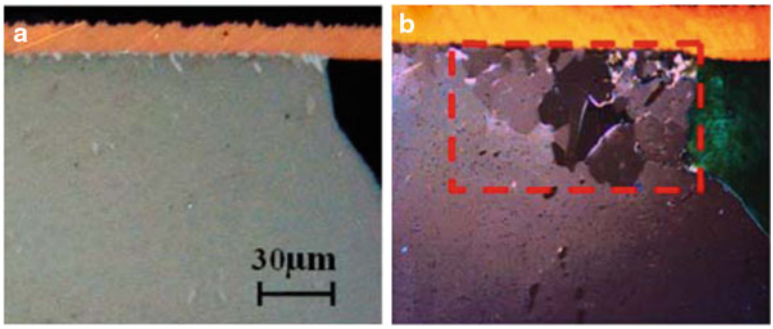


Fig. 4.67 Observed solder interconnection microstructure changes with increasing number of thermal cycles. (**a**) After 500 cycles. (**b**) After 1,500 cycles

$$N_{\mathrm{f}}\,50\,\% = \frac{1}{2}\left[\frac{0.480}{\Delta\gamma_{\max}}\right]^{m}$$
$$\frac{1}{m} = 0.39 + 9.3 \times 10^{-4} \cdot T_{\mathrm{SJ}} - 1.93 \times 10^{-2} \ln\left(1 + \frac{100}{t_{\mathrm{D}}}\right), \tag{4.7}$$

TSJ, mean solder joint temperature; tD, half cycle dwell time.

It has been noticed that the microstructure of the bulk solder changes a lot associated with recrystallization and grain growth under cyclic thermal loading conditions [70]. Figure 4.67 shows the grain structures of SAC based solder after processing and 7,000 cycles of thermal loads. The recrystallized regions are in the area where the solder joint experiences the highest thermal-mechanical loads as indicated by the dashed rectangles. These recrystallized microstructures provide continuous networks of grain boundaries through solder interconnections, and, consequently, they offer favorable paths for cracks to propagate intergranularly. The mechanical properties of solder would be significantly affected by the recrystallization and grain growth. However, the effect has not been included in any of available life models yet. Many challenges are in searching an efficient way to characterize the changing mechanical properties of bulk solder in line with the changed solid microstructure, and then, to incorporate the changing properties into commercial soft ware to predict the critical to reliability parameter.

Another critical failure mechanism of solder interconnect is the fracture along the IMC (intermetallic compound) layer due to the decreased strength in IMC under prolonged high temperature load, see Fig. 4.68.

During soldering process, the liquid solder reacts with the metallization layer of component or substrate to form certain IMC layer. For example, Cu6Sn5 is one typical IMC formed between Cu metallization and SAC based solder. If the product experiences multifle soldering process, or used in high temperature conditions, the IMC layer will grow and become more and more brittle. This will cause reduced mechanical strength in the IMC layer. Figure 4.69 gives a test result of decreased pull strength corresponding to increased IMC thickness on solder interconnects of LED modules.

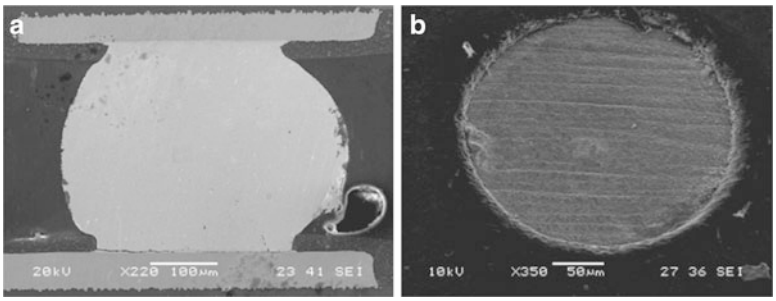


Fig. 4.68 Typical IMC fractrue/crack in SAC based solder interconnect. (**a**) Side view of the IMC cracks, (**b**) top view to the fracture surface after removing the solder and component

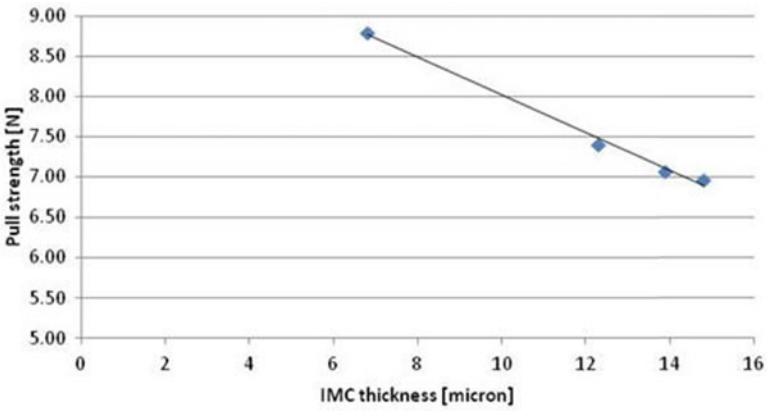


Fig. 4.69 Pull strength vs. copper/tin IMC thickness in SAC solder to copper interconnect of LED packages

The growth of these intermetallic layers can be modeled using parabolic growth kinetics [71]:

$$w = w_0 + D\sqrt{t}, \tag{4.8}$$

where: w, thickness of the intermetallic layer; w_0, initial thickness of the intermetallic layer after assembly; D, diffusion coefficient; t, time.

4.2.3.2 Fractures Related to Adhesive Interconnect

For level 2 interconnect, most of the time, thermal performance is the key factor. This can be achieved by using highly filled epoxy or polyimide adhesives or glass,

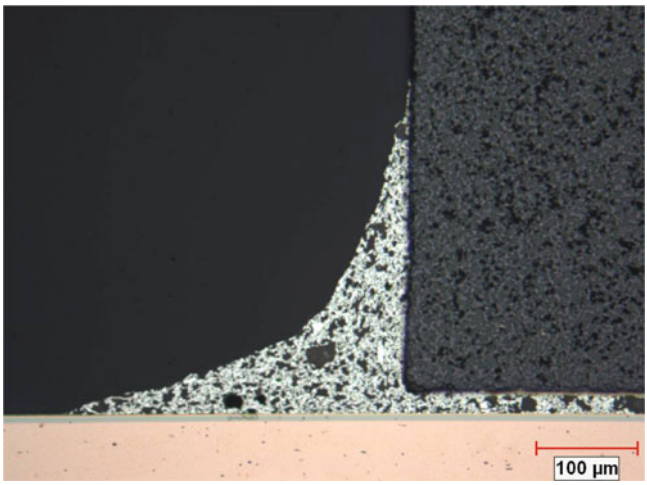


Fig. 4.70 Cross-section of a Ag-filled adhesive interconnects

in addition to SAC based solder alloy. Mostly Ag is used as conductive particles (see Fig. 4.70), for good thermal properties, and providing electrical insulation. AlN particles are also used.

Adhesive has many advantages over solder as level 2 interconnects and thus has been studied in LED applications:

- The processing temperature is considerably lower than soldering.
- The processing is flexible and simple and therefore the cost can be low.
- Packaging size and thickness can be reduced comparing with solder attachment.
- It is more compatible with environment.

However, there are some technical challenges to overcome such as relatively poor thermal cycling performance, unstable contact resistance under extremely humid condition, low electrical conductivity, low impact strength, and low self-alignment capability. The failures modes of adhesive interconnect are decreased thermal and/or electrical resistance due to several failure mechanisms: adhesive cracking; filler motion; formation of oxides; formation of inter-metallic compounds; and Ag migration. Accelerated thermal cyclic tests have been done on several potential adhesives as the level 2 interconnects for typical LED applications. Tested samples are dummy ceramic components assembled on Cu heat slug with adhesive in between. The finish under the component is NiAu. After certain cycles, two typical fractures appeared in some tested samples depending on the choice of adhesive. One fracture with adhesive A is along the interface between the component plating layer and the adhesive, addressed as adhesion failure, see Fig. 4.71a. The other fracture with adhesive B is inside the adhesive layer itself, addressed as cohesion failure, see Fig. 4.71b. The driver of the fractures is the thermal stress in the adhesive layer generated by a huge temperature difference

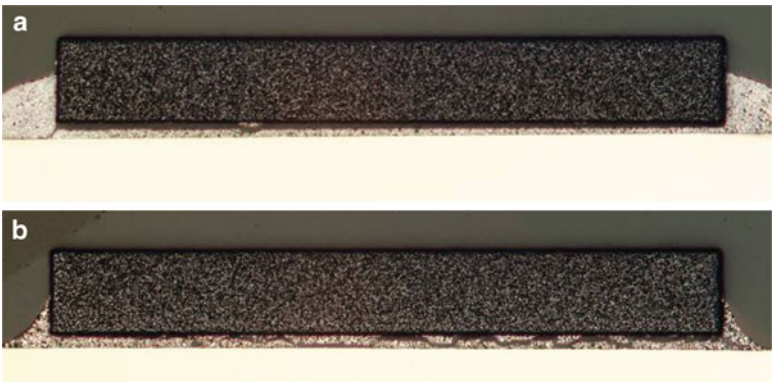


Fig. 4.71 Typical fractures of two different adhesive out of thermal cyclic tests. (**a**) Fractures due to interfacial delamination. (**b**) Fractures due to the adhesive cohesion degradation

during the thermal cyclic test. When the interfacial adhesion strength between the component and the adhesive degrades to a level beyond the driving stress, fractures happened along the interface. When the cohesion strength, which is mainly the bonding strength between various molecules in the adhesive, degrades faster than the interfacial adhesion strength, the cohesion fracture will happen.

Regarding the interfacial delamination, another important driver is the humidity. As adhesives are made of polymers, moisture absorption by the polymeric resin remains as one of the principal contributors to adhesive interconnect failure mechanisms. It has been revealed that absorbed moisture may cause degradation of the adhesive strength as a result of the hydrolysis of the polymer chains [72, 73]. Above that, the mismatch in coefficient of moisture expansion (CME) between adhesive and the connected component and substrates/heat slug induces a hygroscopic swelling stress. Finally, hygroscopic swelling assisted by loss of adhesion strength upon moisture absorption is responsible for the moisture-induced failures in adhesive interconnect. The failure modes are partly or total loss of thermal/electrical contact due to the interfacial delamination. Accelerating test combined with advanced material characterization and finite element modeling can be well used to evaluate the adhesion degradation of typical adhesive interconnect. Related studies including many test data can be found in literature. But there is almost no available information on degradation and life models for adhesive driven by moisture ingression. As a result, it is very hard to say what a particular test result means for the actual life. Caers et al. [74] showed that the resistance increase of NCA (non conductive adhesive) interconnects in a humid environment follows a square root of time function both for steady state humidity conditions as for cyclic humidity test condition. For cyclic humidity, an acceleration transform was proposed as shown in Fig. 4.72.

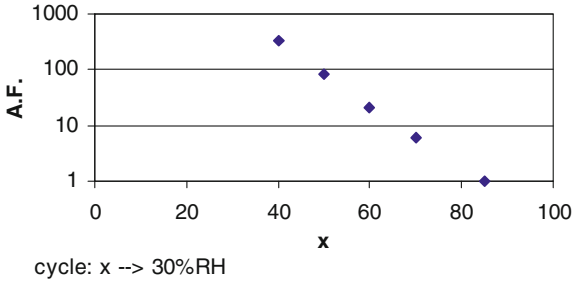


Fig. 4.72 Acceleration transform for NCA in cyclic humidity environment

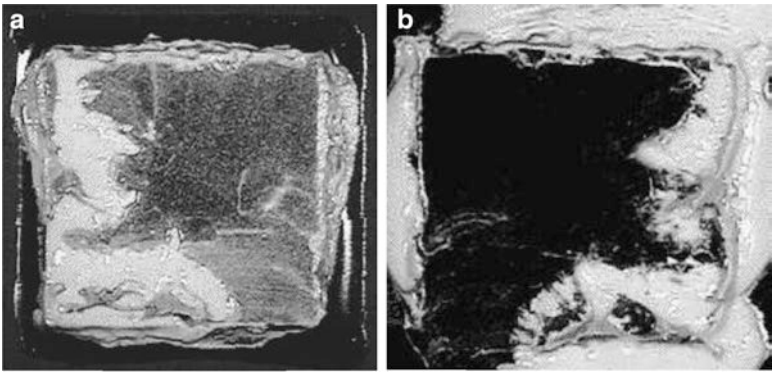


Fig. 4.73 Observed grease pump-out after 6,000 power cycles. (**a**) View to the component side, (**b**) view to the heat spreader

The life time is normalized to 85% RH as maximal humidity content and the lower relative humidity level is 30%. From the graph, the increase in life time for lower max. relative humidity levels than 85% can be read.

4.2.3.3 Thermal Grease Degradation

A possibility to get around the problems of level 2 interconnects related to mismatches in CTE between LED packages and heat slug is using a clamp in combination with a thermal interface material, see Fig. 4.73. For thermal interface materials (TIM) we can distinguish greases, gels and phase change materials [75–79]. Thermal greases are typically silicone based. To enhance thermal conductivity, the silicone matrix is loaded with particles, typically AlN or ZnO. This results in thermal conductivity in the range of 0.3–1.1 K cm^2 W^{-1}. The ideal TIM would have the following characteristics: high thermal conductivity; easily deformed by small contact pressure to contact all uneven areas of both mating surfaces, including surface pores, eliminating *R* contact; minimal thickness; no

leakage out of the interface; maintaining performance indefinitely; non-toxic; and manufacturing friendly.

In reality, many manufacturing and technical challenges are being faced to apply thermal grease. Firstly, thermal grease is very sticky and messy materials so that it is not easy to such as the difficulty in manufacturing due to the stickiness and messy of thermal grease. If the assembled heat slug needs to be replaced, cleaning the grease from the interface has to be done. Excess grease applied that flows out of joint must be removed to prevent contamination and possible electrical shorts. Among all issues, the most critical one is the pumping out. As shown in Fig. 4.73, thermal grease is required to fill the gap between the LED submount and the heat slug in order to reduce the thermal contact resistance. Often, the LED submount experience certain level warpage due to the coefficient-of-thermal-expansion (CTE) mismatch between the LED chip and the submount. Since the CTE of the submount, e.g. Cu, can be much higher than that of the LED chip, this warpage is typically convex after the package assembly process. Since the heat slug is kept in intimate contact with the submount, the expected TIM thickness change is in the same order as the submount warpage change. Under this scenario, every time the LED packages is heated up and cooled down from repeated power on/off, thermal greases can be gradually squeezed out. The thermal grease pumping out can cause significant thermal performance degradation over time. Figure 4.73a, b shows the typical grease pump-out patterns of thermal grease in one flip chip samples after 6,000 power cycles test. In the region where grease pump-out is observed, majority of thermal grease has been squeezed out with some silicone oil remaining [80].

Grease degradation rates are a strong function of operating temperature and number of thermal cycles. To avoid the pumping out, it is very important to choose a TIM which is thermally stable within under targeted temperature and pressure in the application. In addition, the design of the clamp, ensuring good contact during the entire expected life time of the product is critical. Although power cycle test is a direct method to examine thermal grease reliability, it is a time consuming process due to its long heating and cooling times.

4.2.3.4 Electrical Shorts

IEC 61347-1 [81] and UL840 [82] provide guidelines for electrical clearance and creepage distances. The difference between clearance and creepage is that electrical clearances are considered through air spacing; creepage distances (creepages) are spacings over the surface. There are some discrepancies between both documents: IEC 61347-1 advises a minimal creepage distance of 0.5 mm from a peak voltage lower than 125 V. Following this guideline, small form factor WL-CSP LEDs would not be possible. UL 840 accepts creepage distances as low as 80 μm. UL 840 discriminates between different material groups and degrees of pollution. The material groups are related to the comparative tracking index performance level category values, CTI, of insulating materials. Pollution degrees are based on the

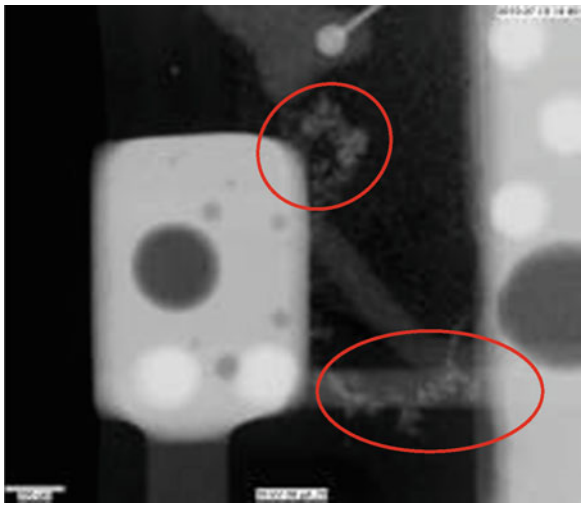


Fig. 4.74 Dendrite formation in level 2 LED interconnect

presence of contaminants and possibility of condensation or moisture at the creepage distance. The lowest pollution degree, degree 1, stands for no pollution or only dry, nonconductive pollution. The pollution has no influence. Pollution degree 1 can be achieved by the encapsulation or hermetic sealing of the product. The highest pollution degree, degree 4, relates to pollution that generates persistent conductivity through conductive dust or rain and snow.

The guidelines from IEC 61347-1 and UL840 are based on safety aspects and do not take time effects into account. Hence failure modes as electrochemical migration (ECM) are not covered. Figure 4.74 gives an example of a failure from Sn-dendrite formation in a design in line with the guidelines for creepage distance. With decreasing component size, ECM becomes more and more a concern.

Dendrites are tree-like growths that tend to be extremely fragile. Once the dendrite growth has bridged the gap between the cathode and anode, a short circuit is created. Because of the small cross-sectional area of the dendrite, the current density can become very high and generate enough heat to burn the dendrite bridge. This can lead to intermittent failures, making the root cause failure and failure site difficult to detect. However, if the dendrite bridge is large enough it can cause total failure of the system. In general, dendrites grow from the cathode to the anode. The cathode is considered the negative conductor (also described as the power conductor). The anode is considered the positive conductor. An example of Cu-dendrite formation is given in Fig. 4.75. The root cause here is poor quality plating of the board finish and cracks in the solder resist layer, filled with Cu/Ni-particles. These decrease the effective creepage distance.

A phenomenon similar to dendrite formation is conductive anodic filament formation, CAF. CAF is a conductive copper-containing salt created electrochemically, that grows from the anode to the cathode subsurface along the interface. It can also grow from the anode on one layer to a cathode on another or as is often the case

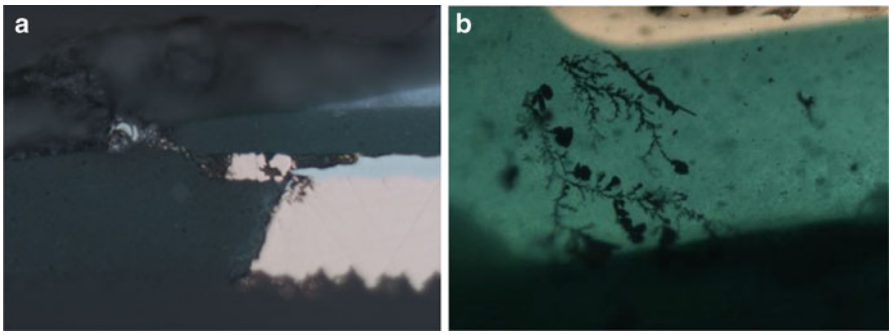


Fig. 4.75 Crack in solder resists of PCB with Cu/Ni-particles (cross-section) (**a**) and Cu-dendrites on PCB as a result (top view) (**b**)

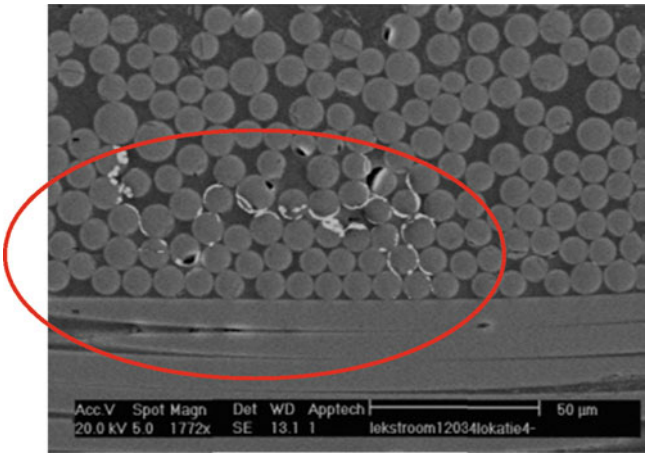


Fig. 4.76 CAF formation along the glass fibers inside the PCB (cross-section, SEM)

along the glass fibers between via's or even through hollow glass fibers [83]. With the introduction of Pb-free soldering and of high-Tg PCBs, in combination with high density PCBs, the risk for CAF has increased considerably. An example is shown in Fig. 4.76. It is a cross-section through the glass fibers of a PCB; between the fibers, the Cu-salts can be seen.

Parameters that affect ECM are: the voltage gradient, temperature, relative humidity, and contamination. Several models describing dendrite growth have been published in literature. These models, however, are not consistent and most of them do not take into account all the expected drivers. J.J.P. Gagne derived an empirical model for Ag-migration [84]

$$t_{50} = PV^{\gamma} \exp\left[\frac{E_a}{KT}\right], \tag{4.9}$$

with t_{50}, median time to failure; V, voltage gradient; P, constant; γ, constant exponent; E_a activation energy for Ag-migration; k Boltzmann constant.

It should be remarked that (4.10) does not include a moisture related term. Other models are a.o. Howard model for dendrite growth [85]

$$\mathrm{TTF} = \frac{wlhndF}{MV} \times \frac{r}{t}, \tag{4.10}$$

where TTF, time to failure; w, conductor width; l, conductor length; h, conductor thickness; n, valence of conductor; d, density of conductor; F, Faraday's constant; M, atomic weight of conductor; V, voltage bias; r, resistivity of electrolyte; t, electrolyte thickness.

In (4.11), there is no temperature term or relative humidity term, Rudra model for dendrite growth [86]

$$\mathrm{TTF} = \frac{af(1,000\,L_{\mathrm{eff}})^n}{V^m(M - M_t)} \quad M > M_t, \tag{4.11}$$

with TTF, time to failure; a, filament formation acceleration factor; f, multilayer correction factor; L_{eff}, effective length between the conductors ($L_{\mathrm{eff}} = kL$); k, shape factor; V, bias voltage; M, percentage moisture content; M_t, threshold percentage moisture content.

Turbini model for CAF [87]:

$$\mathrm{MTTF} = c.\exp\left(\frac{E_a}{kT}\right) + d\left(\frac{L^4}{V^2}\right), \tag{4.12}$$

with MTTF, median time to failure; E_a, activation energy; k, Boltzmann constant; L, spacing; V, bias voltage.

Also (4.12) does not contain a relative humidity related factor. According to the models, a higher voltage gradient results in a higher risk for ECM. However, some sources report an "optimal" voltage gradient of 25 V/mm [88]. Jachim [89] states there is a critical voltage bias range outside which surface ECM will not occur. The lower end of this range is 2 V, due to the need of the bias to be higher than the electrochemical deposition potential of the metal. The upper limit is about 100 V because above this voltage the failure mechanism changes from surface ECM to other migration failures. For moisture, from the model of Rudra, we can expect a threshold in moisture below which ECM will not occur. This critical moisture level can be expressed as a number of monolayers of water on the substrate. Zamanzadeh et al. [90] reports this layer of water to be approximately 20 monolayers thick. Also the temperature effect is not clear. According to most models, the ECM risk is expected to grow with increasing temperature. But, sometimes it turns out that low temperature (e.g. 40°C) is more stringent for easily volatilized residues such as low residue fluxes, than higher temperature (e.g. 85°C). The role of contaminants is even more complex [91]. Contaminants can lower the relative humidity needed for water to adsorb to the PCB. Contamination may also increase the electrical conductivity and change the pH of the electrolytic solution, thus decreasing the amount

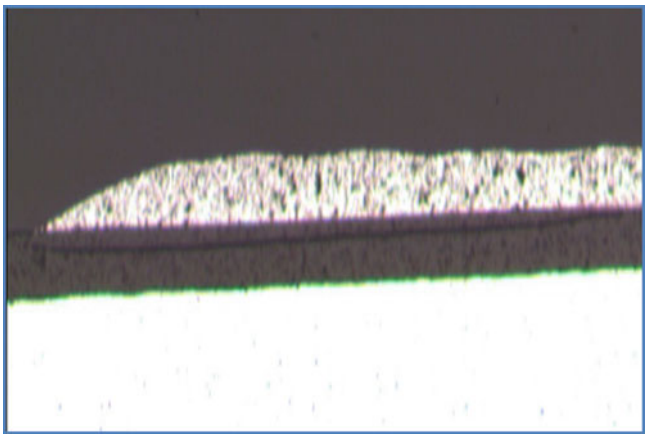


Fig. 4.77 Crack in the dielectric layer of MCPCB

of time it takes for ions to migrate through the solution. Studies have shown that halide ions, primarily chlorine and bromine ions tend to be the most harmful contaminants. As chloride contamination increases, the failure mechanism tends to shift from ECM to uniform corrosion. Lower chloride contamination levels may be a greater risk for ECM and as the contamination levels increase, the risk of uniform corrosion becomes higher. The occurrence of ECM at lower contamination levels may be due to the lower concentration of metal in solution. At higher contamination levels, the concentration of electrochemically active species overcomes the electrochemical corrosion resistance and uniform corrosion occurs. An important source for contamination is flux residues. Summarizing, there is a clear need for a deeper understanding and controlling of all factors governing ECM in order to come to proper design rules for ECM.

4.2.3.5 Other Failure Modes in Level 2

The primary heat transfer process for the LED is conduction, that mainly has to take part throughout the backside of the package, through the level 2 interconnect and the heat slug to outside. With the increasing power density in current LEDs, the traditional substrate materials like FR4 cannot meet the cooling requirement any more. New developed materials like MCPCB (metal core printed circuit boards), with printed circuit attached on metal made of Al or Cu to improve the heat transfer path, and are often used in current LED modules. Although MCPCB can give better performance than FR4, its relatively high CTE, e.g. MCPCB with Al metal, makes it more incompatible with the LED submount like ceramic. Thus, relatively high stress impact is built in the solder layer and also to the dielectric layer of MCPCB. One typical failures identified due to the high stress is the dielectric layer cracking or chipping, see Fig. 4.77.

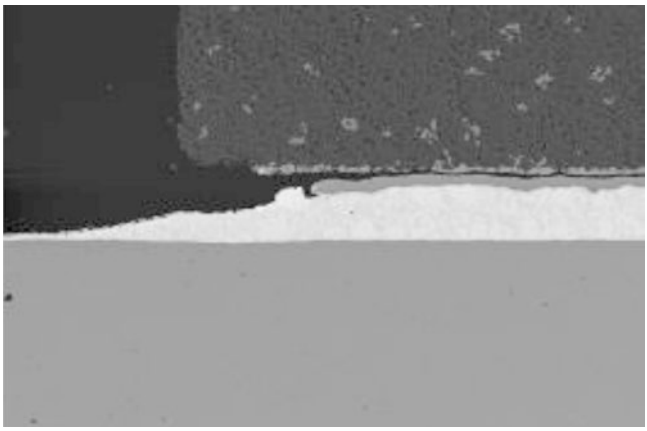


Fig. 4.78 Delamination between the metallization layer and the ceramic submount after thermal cyclic test

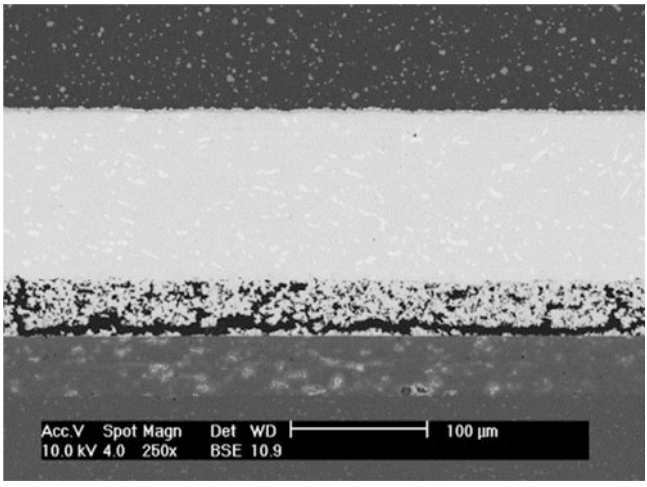


Fig. 4.79 Delamination/fatigue of the Ag-pad above the MCPCB in LED packages after thermal cyclic tests

When the stress induced by the thermal cyclic test is extremely high, the metallization layer under the submount or above the substrate may crack or delaminations too, see Figs. 4.78 and 4.79.

Another failure out of thermal cyclic test on MCPCB is the Ag pad buckling, see Fig. 4.80. Main driver behind is the compressive stress that Ag experiences under

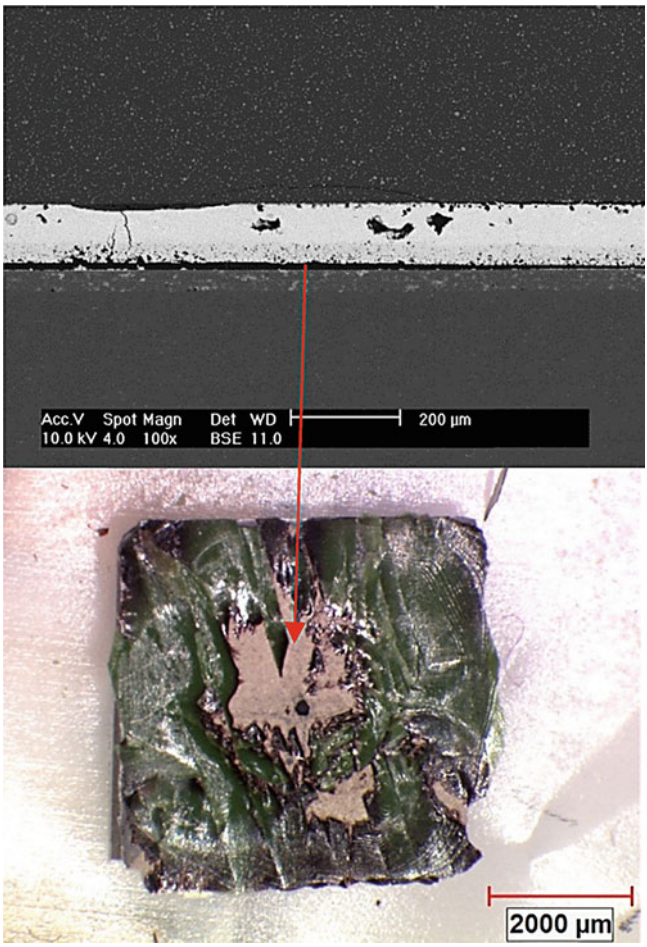


Fig. 4.80 Buckling of Ag pad above the MCPCB in LED packages after thermal cyclic tests

the cooling of thermal cyclic test because it has different scale of shrinkage from the MCPCB. In addition, the relatively poor interface strength between the Ag pad and the dielectric layer is also a factor to such a failure.

4.2.4 Level 3: Module Failure Modes

Level 3 LED modules consist of an assembly of one or more LEDs, together with optics, a heatsink or heatspreader if necessary and the driver. Some examples of level 3 modules are shown in Fig. 4.81.



Fig. 4.81 Example of a level 3 LED module

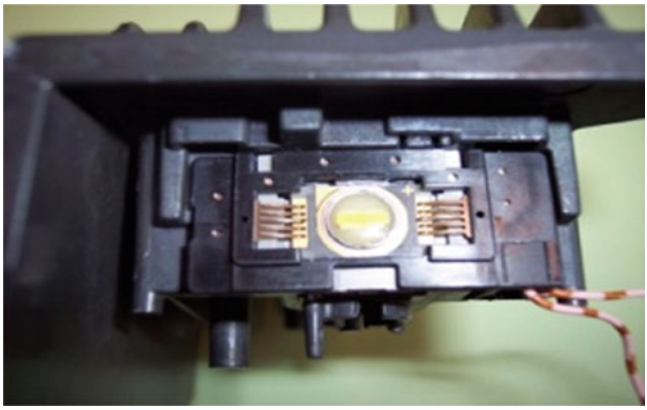


Fig. 4.82 LED module on a heatsink for automotive application

Typical level 3 failure modes are casing cracks, driver failures, optic degradation (browning, cracks, and reflection change), ESD failures and delamination.

Delamination. An example of a module for automotive application is shown in Fig. 4.82. The module is fixed to a die cast heatsink. A thermal interface material (TIM) is used between the module and the heatsink for good thermal contact and hence a good heat transfer. Delamination over time is one possible degradation mode of the module. Delamination will result in an increase of the LED junction temperature and a shorter LED life time. Chiu [92] proposed a powerful method to evaluate the robustness of thermal interfaces using TIMs. Figure 4.83 shows the proposed set-up where the power cycle is replaced by a much faster cyclic mechanical load at a controlled temperature level (b) in comparison with the conventional set-up using power on/off (a). An accelerated mechanical testing technique was developed utilizing a universal testing machine to simulate the squeezing action on the TIM. In this example, a flip-chip package is surface mounted on a FR-4 test board. The embedded heater and temperature sensors on the flip-chip thermal test die are routed through the FR-4 board to the edge connector, so that the test die can be powered up by an external DC power supply, and the die temperature can be monitored by the temperature sensors. The FR-4 test board is held by a fixture,

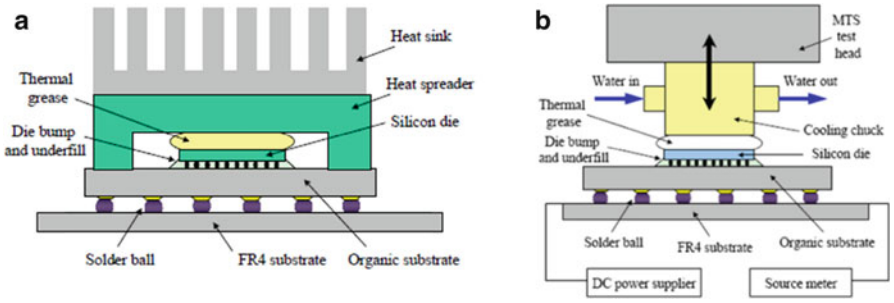


Fig. 4.83 Schematics of set-ups to evaluate the robustness of TIMs—conventional power cycle (**a**) and cyclic mechanical loading at controlled T-level (**b**)

Table 4.8 Typical use classes for consumer electronics

Class	Mode of operation	Operating time/year	Useful life	Total NBR switching cycles
A	Continuous	8,760 h, abs. maximum	90 kh	20
B	Normal	3,000 h, typ. maximum	30 kh	16,000
C	Incidental	300 h, typ. maximum (max. 10 min continuous)	3 kh	16,000

while a cooling chuck (with chilled water circulating through it) is attached to the tensile tester head. The displacement simulates the actual die warpage change from the room temperature to the maximum device operation temperature. The cycling frequency was set to 60 cycles per minute so that a 2,500-cycle test can be completed within 1 h. The chilled water temperature and flow rate through the cooling chuck was adjusted to get the desired die temperature. See also level 1 for more detail on TIM interface degradation.

Power supply failure. Often the power supply will fail long before the lifetime of the LEDs is exceeded. Compared with conventional consumer electronics, there are several additional challenges for LED drivers: (1) the required extra-long life, (2) several applications have a build-in driver, with driver at the top of the bulb and (3) use of electrolytic capacitors.

The required extra-life time for LED drives is not exceptional. To illustrate this, some typical consumer electronics use specifications are summarized in Table 4.8. Hence, major challenge here is not the life time as such, but to keep the temperature under control as most degradation mechanisms are temperature dependent.

If the driver is mounted on top of the LED engine, the driver electronics see an additional heat load and hence need special attention. An example of a build-in driver is shown in Fig. 4.84.

Electrolytic capacitors are sensitive to temperature (Fig. 4.85). The wear out of electrolytic capacitors is due to vaporization of electrolyte that leads to a drift in the

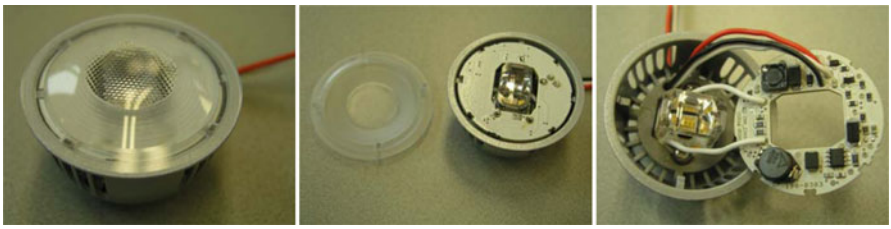


Fig. 4.84 Osram CoinLight with build-in driver PCB



Fig. 4.85 LED driver with electrolytic capacitors

main electrical parameters of the capacitor. One of the primary parameters is the equivalent series resistance (ESR). The ESR of the capacitor is the sum of the resistance due to aluminum oxide, electrolyte, spacer, and electrodes (foil, tabbing, leads, and Ohmic contacts). The health of the capacitor is often measured by the ESR value. Over the operating period, the capacitor degrades i.e. its capacitance decreases and ESR increases. Depending upon the percentage increase in the ESR values we can evaluate the healthiness of the capacitor.

A model for degradation of electrolytic capacitors according to Lahyani [93] is given in (4.13):

$$\frac{1}{\mathrm{ESR}_t} = \frac{1}{\mathrm{ESR}_0}\left(1 - k\,.\,t\,.\exp\left(\frac{-4,700}{T+273}\right)\right), \tag{4.13}$$

with ESR_t, the ESR value at time "t"; T, the temperature at which the capacitor operates; t, the operating time; ESR_0, initial ESR value at $t = 0$; k, constant which depends on the design and the construction of the capacitor.

This corresponds with activation energy for T-dependence of the capacitor life time, $E_\mathrm{a} \approx 0.4$ eV.

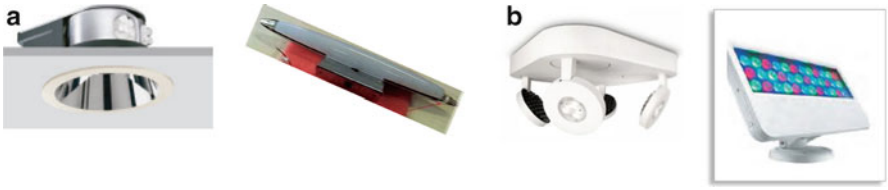


Fig. 4.86 Examples of level 4 luminaries for indoor (**a**) and outdoor (**b**)

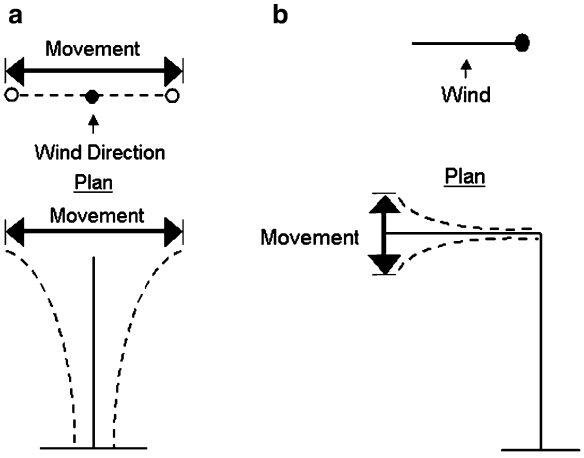


Fig. 4.87 Wind effects: (**a**) vortex shedding and (**b**) galloping

4.2.5 Level 4: Luminary Failure Modes

Level 4 modules consist of a level 3 module together with secondary optics and housing. Some examples for indoor and for outdoor applications are shown in Fig. 4.86.

Typical failure modes for level 4 are fractures of the housing, moisture related failures, and outgassing and yellowing related degradation and failures.

Fractures of the housing can occur from long time exposure to sunlight and humidity and for outdoor applications from mechanical shock and vibration loading (e.g. from the wind or from heavy traffic). Corrosion can enhance the risk for cracking of metal parts. Wind loading is typical for outdoor applications. Two possible effects of wind loading are vortex shedding and galloping as is schematically shown in Fig. 4.87 [94, 95]. For both, the movement is perpendicular to the wind direction. Vortex shedding can result in resonant oscillations of a pole in a plane normal to the direction of wind flow. The winds that are dangerous for vortex shedding are steady winds in the velocity range 5–15 m/s. Unlike vortex shedding, galloping occurs on asymmetric members (i.e., those with signs, signals,

Table 4.9 Most frequently used IP codes [96]

Code	
IP22	Protected against insertion of fingers and will not be damaged or become unsafe during a specified test in which it is exposed to vertically or nearly vertically dripping water. IP22 or 2X are typical minimum requirements for the design of electrical accessories for indoor use
IP44	Water splashing against the enclosure from any direction shall have no harmful effect
IP55	Dust protected, water jets shall have no harmful effect
IP64	Dust tight, splashing water shall have no harmful effect
IP65	Dust tight, water jets shall have no harmful effect
IP67	Dust tight, immersion up to 1 m, 30 min
IP68	Dust tight, immersion beyond 1 m

or other attachments) rather than circular members. Therefore, it is the mast arms rather than the poles that are susceptible to galloping. It is believed that a large portion of the vibration and fatigue problems that has been investigated for cantilevered sign and illumination and signal support structures were caused by galloping.

The movement of the pole and the mast arms are transferred to the luminaries. For outdoor applications, these effects have to be taken into account.

Moisture related failures are related to corrosion due to water ingression, condensation and poor plating quality. To avoid water ingression, the luminary should be designed according to the proper IP code for the particular application. The IP code (*I*ngress *P*rotection *R*ating) classifies use conditions. The IP code consists of two digits [96]. The first digit indicates the level of protection that the enclosure provides against access to hazardous parts such as electrical conductors, moving parts and the ingress of solid foreign objects. The second digit indicates protection of the equipment inside the enclosure against harmful ingress of water. Most frequently used IP codes are summarized in Table 4.9. Moisture ingression does not only cause level 4 damage, but it can also result in failures from level 0 to level 3, e.g. shorts from electrochemical migration (see level 1 and level 2).

If diffusion is assumed to be Fickian with constant diffusivity and if sorption of water by the seal is governed by Henry's law with constant solubility, the moisture ingress can be approximated by a power law (4.15) [97, 98]. The driver for moisture ingress is the relative humidity gradient between inside and outside:

$$\Delta RH = A \cdot \mathrm{e}^{-t/h}. \tag{4.14}$$

Typical metal materials used for luminary housings are die-cast zamak and aluminum or steel. To protect these materials against corrosion, different types of coatings are used e.g. Cu + Ni + Cr finish, and Ni + Cu + varnish finish. Some examples of corrosion observed for inadequate quality luminary finish are shown in Fig. 4.88. Corrosion and blathering can be observed. For a good quality finish, the layer thickness has to be well controlled and sharp edges are to be avoided.



Fig. 4.88 Corrosion and blathering of the finish layer on luminaries for indoor applications

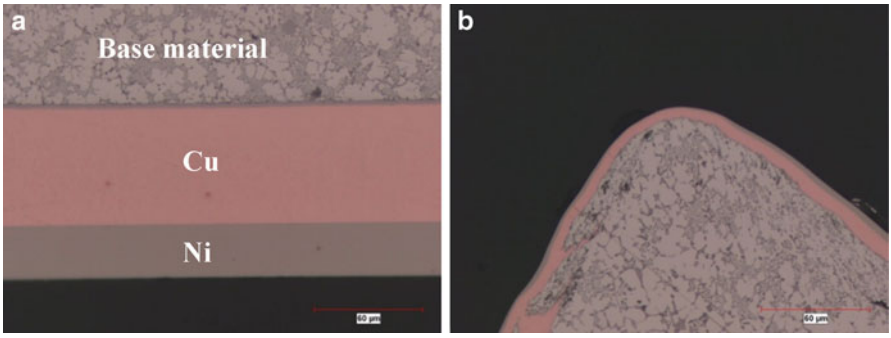


Fig. 4.89 Difference in thickness of finish layer between (**a**) "bulk" and (**b**) "edge"

Figure 4.89 shows a cross-section of housing with a Cu + Ni finish, illustrating that at the sharp edge, both the Cu-layer and the Ni-layer have become very thin; it should be remarked that the pictures in Fig. 4.89 have been taken from the same part and with the same magnification.

Guidelines to evaluate the corrosion resistance of metal luminaries are given in IEC 60598-1 [99]. Ferrous materials e.g., are immersed in a solution of ammonium chloride and water, and then the parts are placed in a box containing air saturated with moisture. After drying the parts shall show no signs of rust.

Connector corrosion is another typical degradation mechanism from moisture ingress. Corrosion is a chemical-metallurgical reaction that reduces the energy level of a discrete system composed of a metal, an oxidizer, moisture or some other chemical, and corrosion products. The oxide or salt corrosion products become like the ore from which the metal was made. Corrosion products have greater volume than the base metal, so on electrical connector contacts the corrosion products push the contacts apart reducing the number of current contact "asperities" (the mountains or "protuberances" on the surface of the metal contacts) and as a result increasing the contact resistance.

Deposition of outgassing material on the optics and y*ellowing* of exit windows from exposure to temperature, humidity and UV are other possible level 4 degradation and failure mechanisms. These phenomena are similar to what is described in level 1 yellowing. Weathering and light exposure are important causes of damage to coatings, plastics, inks and other organic materials. This damage includes loss of gloss, fading, yellowing, cracking, peeling, embrittlement, loss of tensile strength and delamination. Accelerated weathering and light stability testers are widely used for research and development, quality control and material certification. These testers provide fast and reproducible results. The most frequently used accelerated weathering testers are the fluorescent UV accelerated weathering tester (according to ASTM G 154) and the xenon arc test chamber (according to ASTM G 155) [100]. Most weathering damage is caused by three factors: light, high temperature and moisture. Any one of these factors may cause deterioration. Together, they often work synergistically to cause more damage than any one factor alone. Spectral sensitivity varies from material to material. For durable materials, like most coatings and plastics, short-wave UV is the cause of most polymer degradation. However, for less-durable materials, such as some pigments and dyes, longer-wave UV and even visible light can cause significant damage.

The destructive effects of light exposure are typically accelerated when temperature is increased. Although temperature does not affect the primary photochemical reaction, it does affect secondary reactions involving the by-products of the primary photon/electron collision. A laboratory weathering test should provide a means to elevate the temperature to produce acceleration.

Dew, rain and high humidity are the main causes of moisture damage. Research shows that objects remain wet outdoors for a surprisingly long time each day (8–12 h daily, on average). Studies have shown that condensation, in the form of dew, is responsible for most outdoor wetness. Dew is more damaging than rain because it remains on the material for a long time, allowing significant moisture absorption. Both types of testers provide the possibility to heat the samples and to apply moisture environment.

The spectra of a fluorescent UV lamp and xenon arc testers are different. As a result, the application area is slightly different. Xenon arc testers are considered the best simulation of full-spectrum sunlight because they produce energy in the UV, visible and infrared regions. A comparison is given in Table 4.10.

4.2.6 Level 5: Lighting System Failure Modes

Going 1 more level up to level 5, leads to a very wide diversity of products. Therefore, only a list is given of some typical failure modes that can be observed at this level, without going into details: software failures in intelligent drivers, electrical compatibility issues like electromagnetic compatibility (EMC) and electromagnetic interference (EMI), acoustic failures, installation and commissioning issues like flammability, etc.

Table 4.10 General guidelines for selection of weathering simulation equipment

QUV Fluorescent tester	Xenon arc tester
The QUV is better in the short-wave UV	A xenon arc tester is better match with sunlight in the long-wave UV and visible spectrum
The QUV with UVA-340 lamps provides the best available simulation of sunlight in the critical short-wave UV region. Short-wave UV typically causes polymer degradation such as gloss loss, strength loss, yellowing, cracking, crazing, embrittlement	Long-wave UV and even visible light can cause fade and color change in pigments and dyes. Where color change is the issue, xenon arc testers are recommended
QUV fluorescent UV lamps are spectrally stable	Xenon lamps are inherently less spectrally stable than fluorescent UV lamps
The QUV is better at simulating the effects of outdoor moisture. The QUV's condensation system (100% RH) is aggressive and realistic. This type of deeply penetrating moisture may cause damage such as blistering in paints	Xenon arc testers are better for controlling humidity. This can be an important feature for humidity-sensitive materials. High humidity can cause color shift and uneven dye concentrations

References

1. Horng R-H et al (2011) Failure modes and effects analysis for high-power GaN-based light-emitting diodes package technology. Microelectron Reliab 52:818–821. doi:10.1016/j.microrel.2011.02.021
2. Krames MR et al (2007) Status and future of high-power light-emitting diodes for solid-state lighting. J Display Technol 3(2):160–175
3. DR04. Luxeon Rebel IES LM-80 Test Report
4. http://ics.nxp.com/quality/ifr/
5. Cotterell B, Chen Z, Han J-B, Tan N-X (2003) The strength of the silicon die in flip-chip assemblies. J Electron Packag 125:115
6. Dugnani R, Wu M (2009) Fracture mechanisms for silicon dice. In: Proceedings of the 35th ISTFA, San Jose, CA, pp 309–313
7. Amerasekera A, Duvvury C (2002) ESD in silicon integrated circuits, 2nd edn. Wiley, Baffins Lane
8. Unger BA (1983) Electrostatic discharge failures of semiconductor devices. In: IEEE/PROC, IRPS, Las Vegas, NV, USA, pp 193–199
9. Xie R-J, Hirosaki N, Sakuma K, Kimura N (2008) White light-emitting diodes (LEDs) using (oxy)nitride phosphors. J Phys D: Appl Phys 41:1440131–1440135
10. Application Brief AB32 Lumileds, LUXEON® Rebel and LUXEON® Rebel ES, Assembly and Handling information
11. Meneghesso G, Meneghini M, Zanoni E (2010) Recent results on the degradation of white LEDs for lighting. J Phys D: Appl Phys 43:354007
12. https://nepp.nasa.gov/index.cfm/6095
13. Barton DL et al (1999) Degradation mechanisms in GaN/AIGaN/InGaN LEDs and LDs. IEEE 0-7803-4354-9/99/$10.00 0
14. Cree XLamp®. Long-term lumen maintenance. Technical Article CLD-AP28 REV.0
15. Evaluating the lifetime behavior of LED systems—the path to a sustainable luminaire business model. Lumileds White Paper WP15, 10 May 2004

16. Jiao J-Z (2011) TM-21 seeks methods for lumen-maintenance prediction. LEDs Magazine, February 2011, pp 37–39
17. Luxeon Reliability Data, Reliability Datasheet RD07, Lumileds website
18. Uddin A, Wei AC, Anderson TG (2005) Study of degradation mechanism of blue light emitting diodes. Thin Solid Films 483:378–381
19. Ueda O (1999) Reliability issues in III–V compound semiconductor devices: optical devices and GaAs-based HBTs. Microelectron Reliab 39:1839–1855
20. Liu XW, Hopgood AA, Usher BF, Wang H, Braithwaite NStJ (1999) Formation of misfit dislocations during growth of InxGa1 – xAs/GaAs strained-layer heterostructures. Semicond Sci Technol 14:1154–1160
21. Misirlioglu IB, Vasiliev AL, Aindow M, Alpay SP (2004) AlpayFigures threading dislocation generation in epitaxial (Ba, Sr)TiO_3 films grown on (001) $LaAlO_3$ by pulsed laser deposition. Appl Phys Lett 84(10):1742–1744
22. Ovid'ko IA (1999) Misfit dislocation walls in solid films. J Phys: Condens Matter 11:6521–6527
23. Speck JS, Brewer MA, Beltzb G, Romanovc AE, Pompe W (1996) Scaling laws for the reduction of threading dislocation densities in homogeneous buffer layers. J Appl Phys 80(7):3808–3816
24. Arnold J (2004) When the lights go out: LED failure modes and mechanisms, White paper. DfR Solutions, College Park, MD, USA
25. Bogdanov MV, Bulashevich KA, Khokhlev OV, Evstratov IY, Ramm MS, Karpov SY (2010) Current crowding effect on light extraction efficiency of thin-film LEDs. Phys Stat Sol (c) 7(7–8):2124–2126
26. Wang P, Wei W, Cao B, Gan Z, Liu S (2010) Simulation of current spreading for GaN-based light-emitting diodes. Opt Laser Technol 42:737–740
27. Meneghini M, Tazzoli A, Mura G, Meneghesso G, Zanoni E (2010) A review on the physical mechanisms that limit the reliability of GaN-based LEDs. IEEE Trans Electron Devices 57(1):108–118
28. Meneghesso G et al (2002) Failure modes and mechanisms of DC-aged GaN LEDs. Phys Stat Sol (a) 194(2):389–392
29. Meneghini M et al (2008) Reliability of deep-UV light-emitting diodes. IEEE Trans Device Mater Reliab 8(2):248
30. Meneghini M et al (2008) A review on the reliability of GaN-based LEDs. IEEE Trans Device Mater Reliab 8(2):323
31. Jang HW, Kim JK, Kim SY, Yu HK, Lee J-L (2004) Ohmic contacts for high power LEDs. Phys Stat Sol (a) 201(12):2831–2836
32. Kim H, Yang H, Huh C, Kim S-W, Park S-J, Hwang H (2000) Electromigration-induced failure of GaN multi-quantum well light emitting diode. Electron Lett 36(10):908–910
33. Behaviour of InGaN LEDs in parallel circuits. Application Note, 17 May 2002, Opto Semiconductors
34. Narendran N, Gu Y, Freyssinier JP, Yu H, Deng L (2004) Solid-state lighting: failure analysis of white LEDs. J Cryst Growth 268:449–456
35. Application Note 409, Evans analytical group detection of threaded dislocations in strained Si using AFM 7th May 2007, Version 3.0
36. Novak M, Feinstein A. Bruker's nano surfaces solutions provide complete LED surface metrology capability, Bruker website
37. Lin Y-C et al (2006) Materials challenges and solutions for the packaging of high power LED. In: International microsystems, packaging, assembly conference, Taiwan
38. Hsu Y-C et al (2008) Failure mechanisms associated with lens shape of high-power LED modules in aging test. IEEE Trans Electron Devices 55(2):689–694
39. Down JL (1986) The yellowing of epoxy resin adhesives: report on high-intensity light aging. Stud Conserv 1:159–170

40. Arik M, Setlur A, Weaver S, Haitko D, Petroski J (2007) Chip to system levels thermal needs and alternative thermal technologies for high brightness LEDS. J Electron Packag 129:328–338
41. Torikai A et al (1999) Accelerated photodegradation of poly(vinyl chloride). Polym Degrad Stab 63:441–445
42. Torikai A et al (1990) Photodegradation of polyethylene: factors affecting photostability. J Appl Polym Sci 40:1637–1646
43. Torikai A et al (1993) Photodegradation of polymer materials containing flame-cut agents. J Appl Polym Sci 50:2185–2190
44. Bera D et al (2010) Optimization of the yellow phosphor concentration and layer thickness for down-conversion of blue to white light. J Display Technol 6(12):645–651
45. Luo H et al (2005) Analysis of high-power packages for phosphor-based white-light—mitting diodes. Appl Phys Lett 86:243505
46. Allen SC et al (2007) ELiXIR—solid-state luminaire with enhanced light extraction by internal reflection. J Display Technol 3(2):155
47. Sonoki H et al (2007) Study on deterioration mechanism and acceleration tests for optical transparent materials. In: IEEE polytronic conference, Warsaw, Poland, pp 189–192
48. Hu J, Yang L, Shin MW (2007) Mechanism and thermal effect of delamination in light-emitting diode packages. Microelectr J 38(2):157–163
49. Hu J et al (2006) Thermal and mechanical analysis of delamination in GaN-based light-emitting diode packages. J Cryst Growth 288:157–161
50. Wong EH, Chan KC, Rajoo R, Lim TB (2002) The mechanics and impact of hygroscopic swelling of polymeric materials in electronic packaging. ASME J Electron Pack 124:122–126
51. Driel WDV, van Gils MAJ, Fan X, Zhang GQ, Ernst LJ (2008) Driving mechanisms of delamination related reliability problems in exposed pad packages. IEEE Trans Compon Pack Technol 31:260–268
52. Driel WDV, Wisse G, Chang AYL, Jassen JHJ, Fan X, Zhang KGO et al (2004) Influence of material combinations on delamination failures in a cavity-down TBGA package. IEEE Trans Compononents Packag Technol 27:651–658
53. Driel WDV et al (2005) Prediction of delamination related IC & packaging reliability problems. Microelectron Reliab 45:1633–1638
54. Harman G (1997) Wire bonding in microelectronics materials, processes, reliability, and yield, 2nd edn. McGraw-Hill, New York, NY
55. Oldervoll F et al (2004) Wire-bond failure mechanisms in plastic encapsulated microcircuits and ceramic hybrids at high temperatures. Microelectron Reliab 44:1009–1015
56. Buso S (2008) Performance degradation of high-brightness light emitting diodes under DC and pulsed bias. IEEE Trans Device Mater Reliab 8(2):312–322
57. Arik M, Weaver S, Becker CA, Hsing M, Srivastava A (2003) Effects of localized heat generations due to the color conversion in phosphor particles and layers of high brightness light emitting diodes. In: International electronic packaging technical conference and exhibition, Maui, Hawaii
58. Chhajed S et al (2005) Influence of junction temperature on chromaticity and color-rendering properties of trichromatic white-light sources based on light-emitting diodes. J Appl Phys 97:011306
59. Xie R-J, Hirosaki N, Kimura N, Sakuma K, Mitomo M (2007) 2-Phosphor-converted white light-emitting diodes using oxynitride/nitride phosphors. Appl Phys Lett 90:1911011–1911013
60. Meneghesso G et al (2010) Recent results on the degradation of white LEDs for lighting. J Phys D: Appl Phys 43:354007 (11 pp)
61. Xie R-J et al (2007) Silicon-based oxynitride and nitride phosphors for white LEDs—a review. Sci Technol Adv Mater 8:588–600
62. Dudek R et al (2007) Low-cycle fatigue of Ag-based solders dependent on alloying composition and thermal cycle conditions. In: 57th ECTC, Reno, NV, pp 14–21

63. Hannach T et al (2009) Creep in microelectronic solder joints: finite element simulations versus semi-analytical methods. Appl Mech 79(6–7):605–617
64. Ma H (2009) Constitutive models of creep for lead-free solders. J Mater Sci
65. Darveaux R et al (1992) IEEE Trans Component Hybrids Manuf Technol 15(6):1013
66. Clech J-P (2009) Lead-free solder joint reliability: acceleration factors. In: SMTAI, San Diego, CA, USA
67. Schubert A et al (2003) Fatigue life models for SnAgCu and SnPb solder joints evaluated by experiments and simulation. In: Proceedings of the ECTC 2003, May 2003, New Orleans, Louisiana, pp 603–610
68. Engelmaier W (2008) Creep fatigue model for SAC405/305 solder joint reliability estimation—a proposal. Global SMT & Packaging, December, pp 46–48
69. Vasudevan V et al (2008) An acceleration model for lead-free (SAC) solder joint reliability under thermal cycling. In: Proceedings of the 58th, ECTC, May 2008, pp 139–145
70. LI J et al (2010) Multiscale simulation of microstructural changes in solder interconnections during thermal cycling. J Electron Mater 39(1)
71. Klein Wassink RJ (1989) Soldering in electronics, 2nd edn. Electrochemical Publications, Port Erin, Isle of Man, British Isles
72. Liu J, Lai Z, Kristiansen H, Khoo C (1998) Overview of conductive adhesive joining technology in electronics packaging applications. In: Proceedings of the 3rd IEEE international conference on adhesive joining and coating technology in electronics manufacturing, pp 1–18
73. Lefebvre DR, Takahashi KM, Muller AJ, Raju VR (1991) Degradation of epoxy coatings in humid environment: The critical relative humidity for adhesion loss. J Adhesive Sci Technol 5:201–227
74. Caers JFJ et al (2004) Towards a predictive behavior of non-conductive adhesive interconnects. In: Proceedings of the 54th ECTC conference, June 2004, Las Vegas, NV, pp 106–112
75. Lasance C (2003) The urgent need for widely accepted test methods for thermal interface materials. In: Proceedings SEMITHERM XIX, March 2003, San Jose, CA, pp 123–128
76. Viswanath R et al (2002) Thermal performance challenges from silicon to systems. Intel Technol J Q3(2):16
77. Gowda A et al (2005) Reliability testing of silicone-based thermal grease. In: Proceedings of SEMITHERM XXI, March 2005, San Jose, CA, pp 64–71
78. Laird Technologies. T-grease 2500 reliability testing report, Laird website
79. Samson E et al (2005) Interface material selection and a thermal management technique in second-generation platforms built on Intel® Centrino™ Mobile Technology. Intel Tech J (1):75–86
80. Chiu C-P et al (2001) An accelerated reliability test method to predict thermal grease pump-out in flip-chip applications. In: Electronic components and technology conference
81. IEC 61347-1, Lamp controlgear—Part 1. General and safety requirements
82. UL 840 (2007) Insulation coordination including clearances and creepage distances for electrical equipment
83. Rogers K, Van Den Driessche P, Hillman C, Pecht M (1999) Do you know that your laminates may contain hollow fibers? Printed Circuit Fabric 22(4):34–38
84. Gagne JJP (1982) Silver migration model for Ag–Au–Pd conductors. IEEE Trans Components Hybrids Manuf Technol CHMT-5(4):402–407
85. Howard RT (1981) Electrochemical model for corrosion of conductors on ceramic substrates. IEEE Trans CHMT 4(4):520–525
86. Rudra B, Pecht M, Jennings D (1994) Assessing time-to-failure due to conductive filament formation in multi-layer organic laminates. IEEE Trans Components Packag Manuf Tech: Part B 17(3):269–276
87. Turbini LF (2006) Conductive anodic filament (CAF) formation, an historic perspective. Circuit World 32(3):19–24

88. Concoat Systems, Auto-SIR test guidelines, concoat systems website
89. Jachim J, Freeman G, Turbini L (1997) Use of surface insulation resistance and contact angle measurements to characterize the interactions of three water soluble flexes with FR-4 substrates. IEEE CPMT: Part B 20(4)
90. Zamanzadeh M, Meilink SL, Warren GW, Wynblatt P, Yan B (1990) Electrochemical examination of dendritic growth on electronic devices in HCl electrolytes. Corrosion 46 (8):665–671
91. Bumiller E, Hillman C. A review of models for time-to-failure due to metallic migration mechanisms, White Paper. DfR Solutions
92. Chiu C-P, Chandran B, Mello M, Kelley K (2001) An accelerated reliability test method to predict thermal grease pump-out in flip-chip applications. In: Proceedings of the 51st ECTC, 29 May–1 Jun 2001, Orlando, FL
93. Lahyani A, Venet P, Grellet G, Viverge PJ (1998) Failure prediction of electrolytic capacitors during operation of a switchmode power supply. IEEE Trans Power Electron 13:1199–1207
94. Guidelines for the installation, inspection, maintenance and repair of structural supports for highway signs, luminaries, and traffic signals, US department of Transportation, Report No. FHWA NHI 05-036, March 2005
95. Medina MM (2006) Development of design specifications, details and design criteria for traffic light poles, Department of Transportation, Kansas, Report No. K-TRAN: KU-98-6, September 2006
96. Ingress Protection Rating Code according to international standard IEC 60529-2004
97. Pinnes EL (1979) Time constants for moisture diffusion through a permeable barrier into an airspace. Polym Eng Sci 19(7):525–529
98. Goswami A, Han B (2006) On ultra-fine leak detection of hermetic wafer level packages. In: 56th ECTC, San Diego, CA, pp 126–564
99. IEC 60598-1, Luminaires—Part 1. General requirements and tests
100. Grossman DM (2006) The right choice—UV fluorescent testing or xenon arc testing? Paint and Coatings Industry Magazine, March

Chapter 5
Degradation Mechanisms in LED Packages

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Abstract Lumen depreciation is one of the major failure modes in light-emitting diode (LED) systems. It originated from the degradation of the different components within the package, being the LED device or chip, the driver, and the optical materials (including phosphorous layer). This chapter describes the state of the art of the degradation mechanism for these components and how they contribute to the lumen depreciation of the LED package as a whole.

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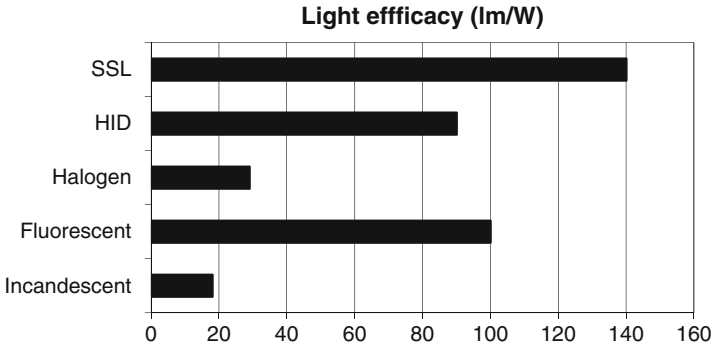


Fig. 5.1 Lighting technology and its efficacy

5.1 Introduction

According to International Energy Agency's estimation, lighting application accounts for about 17.5% of world's total electricity usage in 2006 [1]. However, current artificial lighting technology, with the exception of Light-Emitting Diodes (LEDs), is extremely inefficient (Fig. 5.1).

LED is based on semiconductor materials and processes technology. Tremendous growth in the application of LED in lamps and luminaries both in quantities as well as application has been achieved [2–5] since the invention of the first blue emitting LEDs in 1993 [6] and the introduction of the first commercially available white emitting GaN LED in 1997 [7]. They are known to have an efficacy of 150 lm/W as compared to only about 15 lm/W for a conventional 60–100 W incandescent light bulb [3, 8]. Furthermore, LED luminaries also claimed to have a life of more than 50,000 h and this exceeds the life of nearly all the other light sources [9–11].

In engineering, reliability is the ability of a system or component to perform its required functions under the stated conditions for a specified period of time. As with any other types of products, a reliability study informs both the customers and producers about life and the performance of the product. Customer uses reliability information to compare between different products whereas this information allows manufacturers to design a more reliable product and formulate a maintenance and logistic plan. Therefore, reliability study for any product is essential.

It is very challenging to understand and predict the reliability of the LED emitter because LED system is a relatively new technology with very little field data. Furthermore, their long lifetime makes testing till the end of its lifetime before the product release into the market an almost impossible task. Other factors such as different constructions and technologies employed by different manufacturers may have different failure mode and mechanism. For example, Philips lighting uses the flip chip whereas Osram uses wire bond technologies [5]. Lastly, SSL has much more complex failure mode naming the catastrophic and light depreciation failure mode as compared to the traditional electronic device. In light depreciation failure mode, the device is counted as failed device when the light intensity goes below certain percentage of initial light intensity [14].

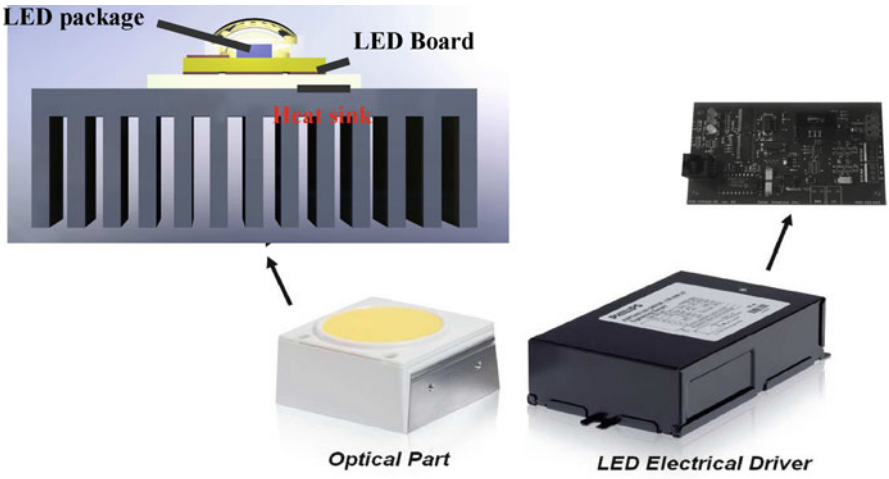


Fig. 5.2 Different parts of a general SSL system. Optical part is the light source of the system and includes LED emitter and thermal solutions whereas SSL driver included power converter and the controller. These two parts of the system are interconnected to each other

Predicting the reliability of SSL systems is even more difficult since a functional SSL system requires close cooperation between different functional subsystems. Each subsystem has unique failure mode and failure mechanisms. These subsystems as shown in Fig. 5.2 include:

1. A semiconductor chip
2. A robust package
3. A lens with optimized light extraction
4. A phosphorous layer
5. A thermal solution

In order to build a reliable product, both fundamental knowledge and industrial practices need to be developed to understand the failure mechanisms in connection with the underlying physics. This chapter attempts to review some of our current understanding on the more common failure mechanisms in SSL. Since SSL system consists of different subsystems as discussed above, the sections in this chapter are divided according to each individual subsystem. This chapter starts with a review of the failure mechanisms of the electrical driver system. Section 5.2 describes a detailed overview on the failure of the LED emitter whereas Sect. 5.3 presents the failure mechanism of packaging.

5.2 Electrical Driver Systems Degradation

As discussed previously, an SSL system is made up of many subsystems including an electrical driver whose primary function is to regulate the input current to the optical subsystems. It has been generally known that one of the weakest subsystems

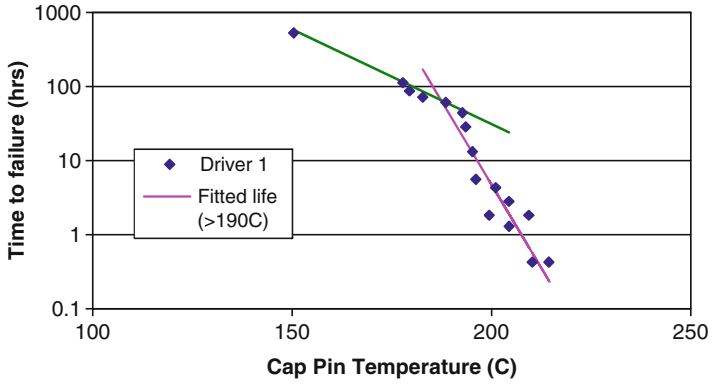


Fig. 5.3 Time to failure with respect to Cap pin temperature of a commercially available driver

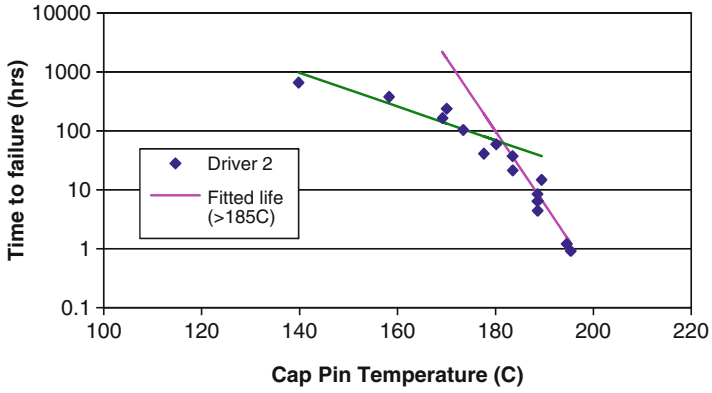


Fig. 5.4 Time to failure with respect to Cap pin temperature of another commercially available driver

of an SSL system is its driver [12]. The failure of electrolytic capacitor is the main failure mode for most of the breakdown in switch mode power supplies [13, 14]. This is especially true at elevated temperature as the failure of the electrolytic capacitor will be accelerated by elevated temperature as shown in Figs. 5.3 and 5.4. A basic rule of thumb for estimating an electrolytic capacitor's life states that decrease by half for every 10°C higher than the rated temperature at which the capacitor operates [15]. Hence, this section focuses on the failure mechanism of an electrolytic capacitor.

An electrolytic capacitor is composed of [16–18] cathode aluminum foil, electrolytic paper, and an aluminum oxide dielectric film on the anode foil surface as shown in Fig. 5.5. The capacitors function is made up between region of the anode and the electrolyte, and between the cathode and the electrolyte. In most cases the capacitor is housed in a cylindrical aluminum container which acts as the negative terminal of the capacitors.

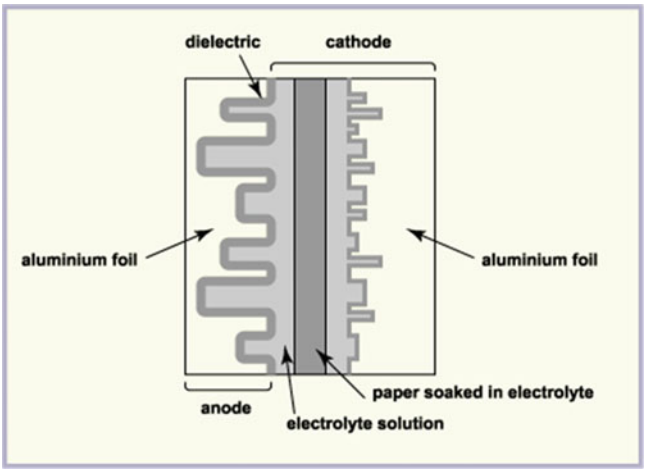


Fig. 5.5 Construction of an electrolytic capacitor

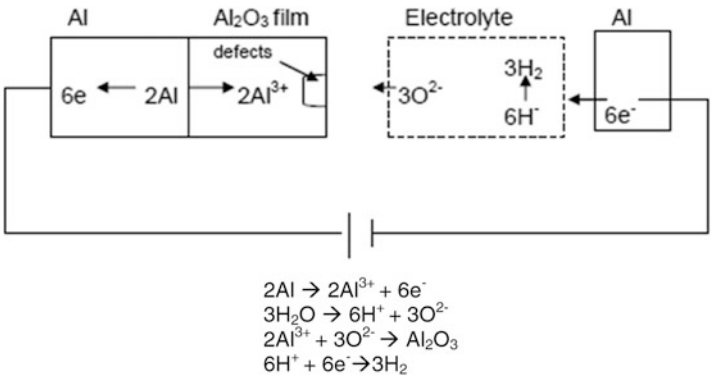


Fig. 5.6 Self-repair mechanisms

The failure mechanism of the electrolytic capacitor at elevated ambient temperature or internal temperature is mainly due to the evaporation and deterioration of electrolyte. Since these capacitors are not hermetically sealed, the electrolyte in these capacitors will evaporate and this will cause a reduction in the capacitance and an increase in ESR. This will in turn cause more heating and deterioration of the electrolyte. This failure mechanism will be more dominant at higher elevated temperature since higher temperature will accelerate the vaporization of electrolyte. This will increase the deterioration rate. Most aluminum electrolytic capacitors have a built-in self-repairing mechanisms as shown in Fig. 5.6. However, this mechanism will induce oxidation of the anode and cause the reduction at the cathode, resulting in the generation of the hydrogen gas.

Under low stressing, the concentration of the hydrogen will not be that critical. However, under the application of harsh environment such as high overvoltage and temperature, the amount of induced defects will increase significantly. This will cause a sudden increase in the generation of hydrogen through these self-repair mechanisms. The induced pressure buildup will then cause failure of the capacitor.

Failures can also be accelerated by cleaning with halogenated solvents during production. When these halogenated materials enter the capacitor, this will corrode the leads or electrode foils and cause the open condition to occur.

In summary, the main failure mechanisms of the electrical driver system are drying up of electrolytic capacitor, pressure buildup due to the generation of hydrogen, and corrosion of the leads or electrode foils.

5.3 Optical Degradation

The optical subsystem of SSL lighting is one of the most important subsystems since only through careful management of emitted light using the optical subsystem can the benefits of SSL lighting be maximized. The optical subsystem includes the light sources which are the semiconductor-based LED emitter/chips, reflectors, phosphor layers, and protective plastic encapsulation. Figure 5.7 shows a schematic of the optical systems.

Over the last few years, several authors have demonstrated that the optical efficiency of the optical subsystem is strongly related to:

1. The degradation of the epoxy such as the yellowing and cracking of the epoxy lens
2. The degradation of the phosphor layer
3. The degradation of the LED chip

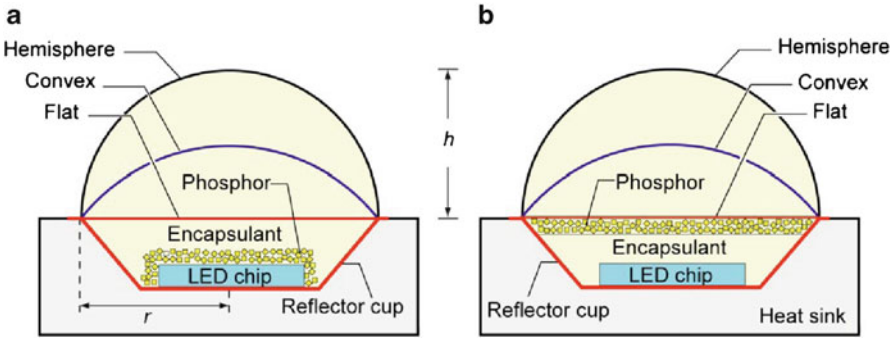


Fig. 5.7 Schematic of the optical systems (hug)

5.4 Epoxy Resin

Epoxy resin is a common material used for the encapsulation of LED. However, most epoxy slowly degrades after extended exposures to light and elevated heat. It will progressively turn more yellow eventually leading to a decrease in its physical properties [19–24]. Yellowing of the epoxy will reduce the light extraction efficiency (as shown in Fig. 5.8) and cause the light color to shift.

Over the past decades, there have been numerous studies of these degradation processes. However, the failure mechanism is highly dependent on the type of epoxy and its loading condition.

The degradation of polysulfone is due to scission of the C–S bonds during oxidation. This will lead to the formation of low-molecular-weight but highly oxidized sulfonic acid which will cause the yellowing of epoxy [21].

Discoloration of bisphenol A polycarbonate is due to Fries photo-transformations, photo-oxidation, and chain scission [25]. Fries photo-transformation is the rearrangement of the phenyl ester due to the absorption of UV radiation [26]. Only photo-oxidation reactions take place under longer wavelength (>300 nm) lights. The chemical changes due to photo-oxidation can be tracked using IR absorbance at 1,713 cm^{-1} since photo-oxidation products, aliphatic acids, ascribed to the absorption band at 1,713 cm^{-1}. The evidence for occurrence of photo-oxidation can be seen in Fig. 5.9 where increasing exposure time resulted in the increase in IR absorption at 1,713 cm^{-1} [27].

The photo-Fries rearrangement involves three basic steps [28]:

1. The formation of two radicals
2. Recombination
3. Hydrogen abstraction

Degradation of the polycarbonate epoxy through Fries photo-transformations involved the direct photoscission of the carbonate bonds of the aromatic chromophores in polycarbonate to form polymeric phenyl salicylates and dihydroxybenzophenone, and mono- or dihydroxybiphenyl and hydroxydiphenyl

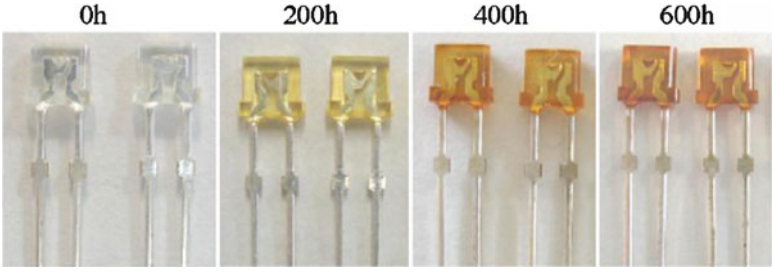


Fig. 5.8 Yellowing of the epoxy encapsulation after thermal storage at 150°C

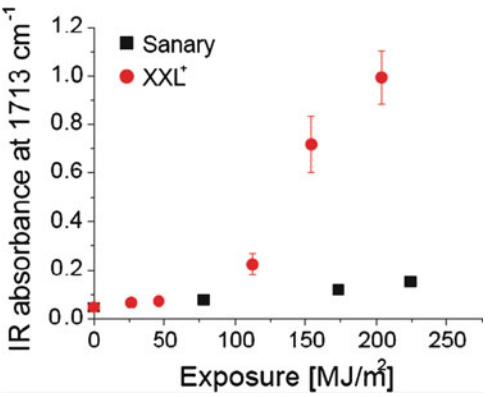


Fig. 5.9 IR absorption at 1,713 cm^{-1} of PC with respect to the exposure for indoor (XXL+) and outdoor (Sanary) condition [25]

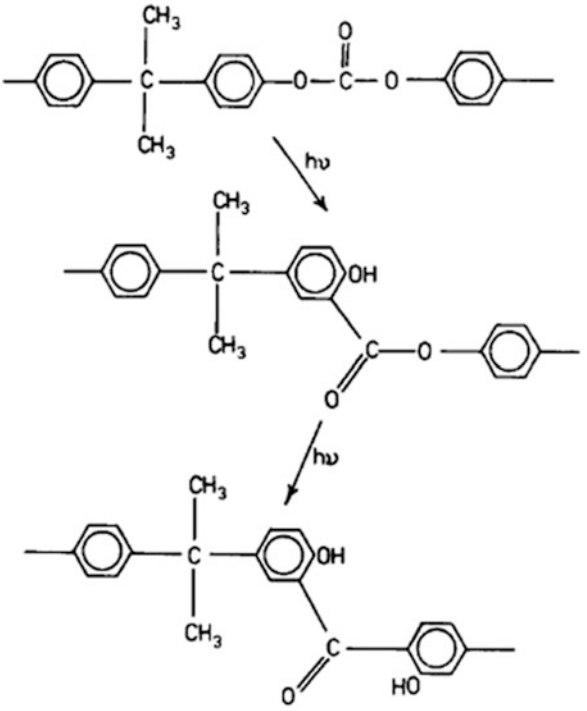


Fig. 5.10 The Fries photo-transformation reaction of Bisphenol A polycarbonate [25]

ether groups [28]. Figure 5.10 shows the Fries photo-transformation reaction of polycarbonate. Photo-oxidation of these photo-Fries reaction product has been found to be the main cause for the photochemical yellowing of the epoxy [29].

The other degradation mechanism involves the scission of the main chain initiated by the abstraction of the hydrogen atoms from the methyl groups. Hydroperoxide intermediates are formed from the photo-oxidation of the gem dimethyl

side chains. Oxidation of the tertiary alcohols and end group ketones formed from these hydroperoxide intermediates and oxidation of the aromatic rings are reported to be responsible for the yellowing of these epoxies [30, 31].

Humidity also has a detrimental effect on the reliability of the polycarbonate. Water modifies the stoichiometry and kinetics of the photochemistry under prolonged exposures. Although the products formed during photo-oxidation and photo-Fries reaction do not react with water, chain scission and formation of these products favor the penetration of water and the liberation of the oligomer and bisphenol A monomers through hydrolysis. These products which have a higher photo-oxidation rate will accelerate the deterioration rate [32].

Another common degradation mechanism of the epoxy encapsulation is the cracking of the epoxy. The shrinkage of the epoxy is due to:

1. Shrinkage after gelation
2. Thermal stresses during cooling due to thermal mismatch
3. Enhanced cross-linking of the epoxy at elevated temperature

The induced stress concentration will not only promote the cracking of the epoxy, but will also deform the metal part and affect the refractive index of the epoxy.

In conclusion, the yellowing of the epoxy resin is mainly due to chain scission, photo-oxidation reaction, and photo-Fries reaction.

5.5 Phosphorous Layer

White light can be formed in several ways. One of the methods is through mixing differently (e.g., red, green, and blue) colored lights [33]. However, this technique requires sophisticated electronic circuits in order to control the blending and diffusion of these different colors. Hence, this method is seldom used to commercially available white light LEDs. The most common method to produce commercial white light LED is to use a gallium nitride (GaN)-based blue LED with cerium-doped yttrium aluminum garnet (Ce^{3+}:YAG) phosphor [8]. The blue LED will generate a blue light that will excite the Ce^{3+}:YAG phosphor and cause it to emit yellow light. The combination of this yellow light from the Ce^{3+}:YAG and the blue light from the LED will result in the white light [34].

One of the failure mechanisms of these LEDs is that the energy is lost during Stokes shift when the phosphor absorbs high-energy blue light and emits low-energy yellow light [35]. This will create localized hot spot. Since the phosphor is always embedded inside an epoxy resin such as silicone, this localized hot spot may promote higher deterioration rate of the silicone such as discoloration of the silicone. In extreme cases, it may also cause cracking of the epoxy.

Another common failure mode is the changes in the light chromatics. This is mainly due to the highly temperature-dependent integral emission intensity from

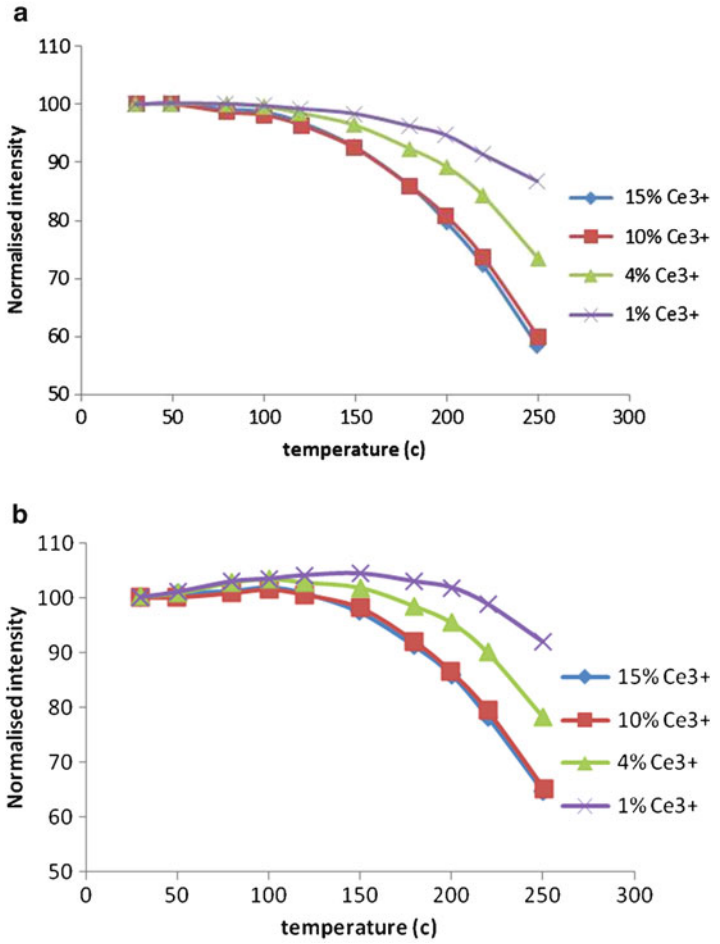


Fig. 5.11 Temperature dependences of the integrated emission intensity of $Y2.93 - xLuxAl_5O_{12}$:Ce0.07 phosphors excited by (a) 460 nm and (b) 340 nm light [36]

the phosphor layer [36]. Figure 5.11 shows the temperature dependences of the integrated emission intensity for YAG:Ce^{3+} phosphors with different Ce^3 concentrations when they are activated by 460 and 340 nm lights. Intensity for all phosphors continuously decreases at a different rate with increasing temperature when they are exposed to 460 and 340 nm light. These relationships are due to typical thermal quenching behaviors. Thermal quenching is a thermal relaxation process that excited the electrons of the activator in such a way that the excited electron and ground states are intermixed. This will cause these electrons to return to the ground state by a non-radiative relaxation process and reducing the luminescent intensity [37].

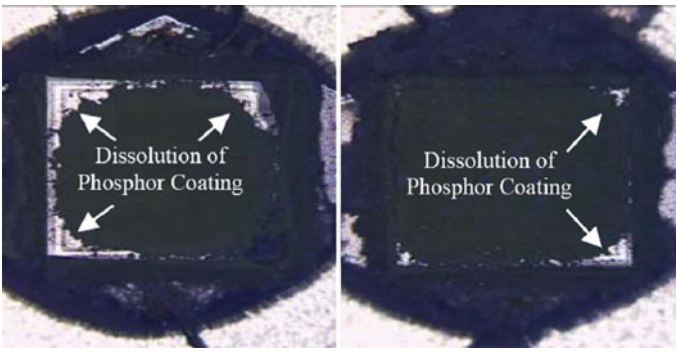


Fig. 5.12 Optical images of the dissolution of the phosphor coating

Since the temperature of the phosphorous layer is highly dependent on the junction temperature and the Stokes shift of the phosphorous layer, any degradation to the emitter will cause the emission intensity to change. This will in turn cause the color chromatics of the LEDs to shift since white light is produced from the combination of the yellow and blue light.

Another degradation mechanism of Y_2SiO_5:Ce phosphorous materials is the chemical change in the phosphor surface through electron-stimulated surface chemical reaction (ESSCR) [38]. This chemical change includes the formation of SiO_2, CeO_2, and CeH_3. Similar degradation can be found in sulfide-based phosphor, ZnS [39].

The dissolution of the phosphor layer in the presence of moisture, as shown in Fig. 5.12, is another common failure mechanism of the optical system. Optical degradation can be caused by the diffusion of Zn activator in the phosphor out of the packaging through the moisture path formed in the presence of humidity [40, 41].

For SSL with high color rendering index, the red-emitting phosphor, CaS:Eu, is sometime added. However, it will react with water to form hydrogen sulfide (H_2S) as shown in (5.1) below:

$$CaS + H_2O \rightarrow CaO + H_2S. \tag{5.1}$$

This H_2S gas will cause the silver in the SSL system to turn black and hence, reduction in the total reflectivity, the total luminance from the LED [42].

A study conducted by Tsai et al. [43] found that the degradation mechanism of the optical system, after a thermal aging at 150°C for 500 h, is the yellowing of the silicone and the mismatch due to the two materials. This includes the reflective index and chemical incompatibility. However, these mechanisms are only dominant for thicker silicone.

In summary, the degradation of phosphorous layer is due to highly temperature-dependent integral emission intensity from the phosphor layer, the chemical change

in the phosphor surface through ESSCR reaction, dissolution of the Zn activator, and blackening of the silver by H_2S gas.

5.6 Light Emitter

Since the light in the SSL system is produced by the semiconductor chip/emitter, it is one of the most important components of SSL lighting system. Over the years, several authors had investigated the failure of the LED emitters and they had found that their optical efficiency can significantly decrease during operation. A number of mechanisms have been identified as follows:

1. The generation of non-radiative centers in the active region of the devices which causes a decrease in the internal quantum efficiency [44–46]
2. The generation of magnesium–hydrogen complexes which causes the decrease in the acceptor concentration at the p-side of the diodes [47–49]
3. Changes in the processes responsible for the injection of the carriers in the active region of the devices (e.g., trap-assisted tunneling) [50]
4. The shortening of the p–n semiconductor junction as a consequence of an ESD event [51]
5. Changes in the local indium concentration in the quantum wells [52–54]

5.6.1 Generation of Non-radiative Centers

Studies conducted by Meneghini et al. [45] show that the degradation of the properties of the active layer of the LEDs can be induced by low-current density stress as shown in Fig. 5.13.

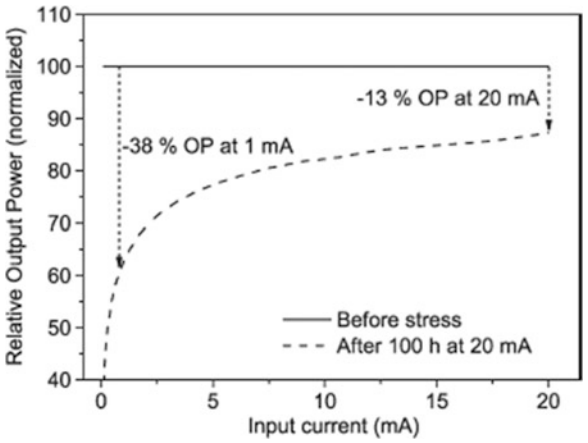


Fig. 5.13 Normalized luminous efficiency (L) – current (I) curves before and after stress at 20-mA dc [45]

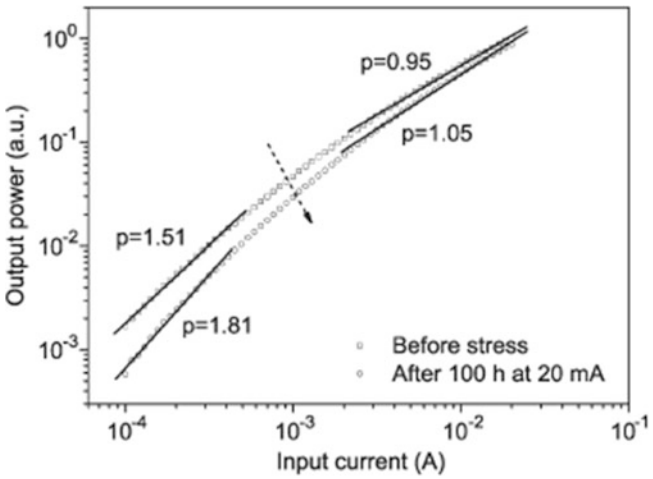


Fig. 5.14 $L - I$ curves before and after stressing with 20-mA dc [55]

This degradation effect is more prominent for low measuring current as shown in Fig. 5.11. Hence, this gives the first hint that their degradation may be related to the generation of non-radiative recombination centers. Using the methodology outlines in [55], the dominating recombination mechanism at each different current level can be further deduced using Fig. 5.14.

Since Auger recombination in wide bandgap is negligible, it can be ignored in the calculation. Hence, under steady-state and charge neutrality conditions, the rate equation can be expressed as

$$\frac{\mathrm{d}n}{\mathrm{d}t} = \frac{J}{qd} - (Bnp + AN_T n) = 0. \tag{5.2}$$

In (5.2)

J is the current density through the active region.
d is the thickness of the active layer thickness.
B is the bimolecular recombination coefficient.
A is the non-radiative recombination coefficient.
N_T is the density of the defects responsible for non-radiative recombination.
n is the concentrations of electrons in the active layer.
p is the concentrations of and holes in the active layer.

Under high injection, (5.2) becomes

$$\frac{J}{qd} = Bn^2 + AN_T n. \tag{5.3}$$

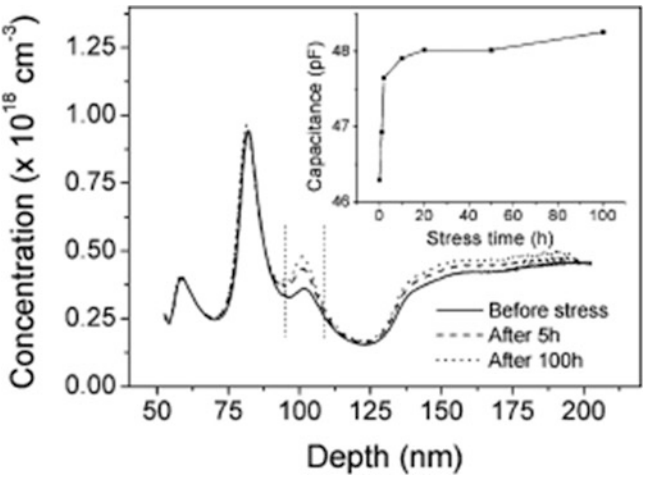


Fig. 5.15 ACD profile of one LED test structure after being stressed by 20 mA dc. *Inset*: Junction capacitance measured at 1 MHz, 1 V during stress [56]

For the radiative recombination to dominate, i.e., $Bn^2 >> AN_T n$, (5.3) simplifies to

$$\frac{J}{qd} \nabla\ Bn^2 = L. \tag{5.4}$$

Hence, (5.4) shows that the slope on the Log (L) vs. Log (I) graphs should be about 1 for this condition to prevail.

For the non-radiative recombination processes to dominate, (5.4) simplifies to

$$\frac{J}{qd} \nabla\ AN_T n. \tag{5.5}$$

Since light intensity is proportional to the square of the injected current, the slope on the Log (L) vs. Log (I) graphs should be about 2. Figure 5.12 shows that slope is about 1.5 at low current levels and about 1 at high current levels. However, the slope of the graph increases after stressing; this indicates an increasing effect of the non-radiative and implies that the degradation is due to the increase in the concentration of the non-radiative center.

C–V measurements have been used to describe the apparent charge distribution (ACD) of the region near the quantum well (QW), and the measurement conducted by Rossi et al. [56] shows an apparent charge increase in the region of the QW (Fig. 5.14). Since Fig. 5.15 also shows that this increase is mostly localized at one peak near 100 nm, the changes should take place mainly near the interface between the active layer and the *n* side of the diode, and in the quantum wells in LED active region [56].

DLTS measurement at this peak shows significant modification of the concentration of a trap state at 170 meV after stressing. This also corresponds to the generation of non-radiative paths. Hence, results from Figs. 5.11, 5.12, 5.13, and 5.14 provide the experimental evidence that the generation of non-radiative recombination centers is one of the failure mechanisms in LED emitter.

Furthermore, since the degradations in Figs. 5.11, 5.12, 5.13, and 5.14 take place at low ambient temperature, this suggests that these non-radiative recombination centers are generated from subthreshold defect generation that is induced by highly accelerated carriers flowing through the active region, as proposed by Manyakhin et al. [46].

5.6.2 Generation of Magnesium–Hydrogen Complexes

Another common degradation mechanism of the LED emitter is the generation of magnesium–hydrogen complexes which can be attributed to the diffusion of hydrogen. Since the precursors SiH_4 and NH_3 are used in the passivation deposition process, this will cause hydrogen to be incorporated into the interface between the p-GaN layers and the passivation [47–49]. This process is mainly aided by the low activation energy of hydrogen diffusion in GaN p–n junctions at the temperature between 250 and 300°C [57, 58]. This hydrogen will then generate bond with the magnesium acceptor at the p side layers to form a metastable Mg–H complex, thus reducing the concentration of the active acceptor [48]. This will then induce an enlargement of the Schottky barrier at the interface and increase the rectifying effect of the device [47].

The evidence for the reduction in the acceptor's concentration can be seen from the *C–V* profiling study conducted by Myers et al. [59]. In their study as shown in Fig. 5.15, 30% reduction of the active Mg concentration can be found after the device is stressed at 100 mA. Further experimental evidence of the formation of metastable $Mg–H_2$ can be observed using infrared vibration spectroscopy (Fig. 5.16). Figure 5.17 shows the $Mg–H_2$ concentration with respect to the electron beam dosage. This concentration is related to the normalized strengths of the IR absorptions [59].

The degradation of the ohmic contact and crowding of the light emission around the pad of the device will also be induced with these degradation mechanisms. Due to the presence of the thick metal layer at the bond-pad region, hydrogen diffusion towards the LED surface will be obstructed near the bond-pad region. This will cause the emission to concentrate near the pad and reduce the overall output power [60]. Furthermore, this concentrated current flow will induce the degradation of the contact layers and partial detachment can occur due to the poor adhesive and the thermal mismatch between the two metals.

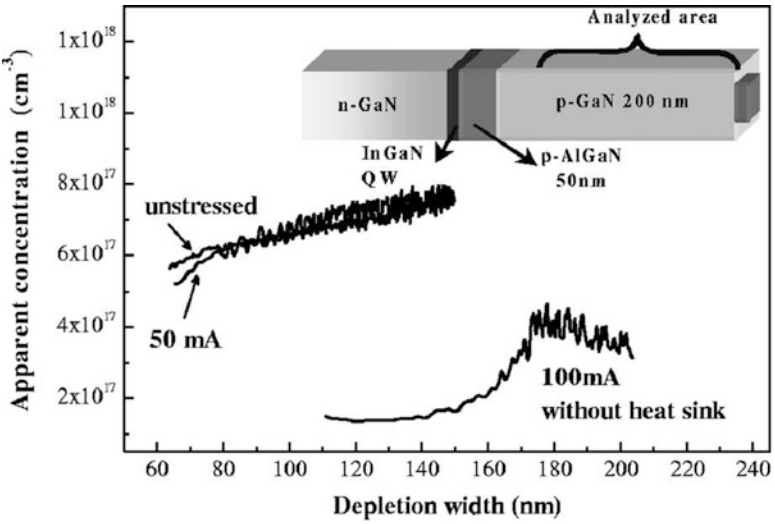


Fig. 5.16 *C–V* measurements for unstressed and stressed devices. The *inset* shows the investigated area [59]

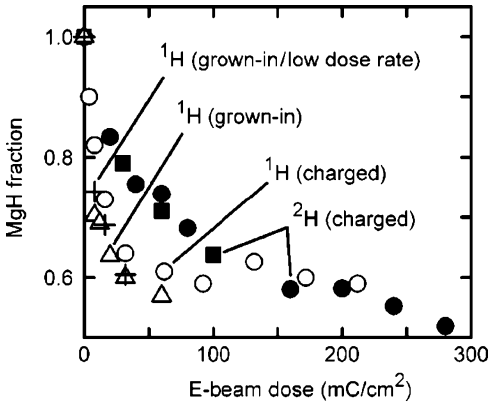


Fig. 5.17 MgH as a function of electron-beam dose. The beam current was 2 mA except for the experiment represented by plus symbols, where the current was 0.4 mA [59]

5.7 ESD Failure

The catastrophic failure of GaN-based LEDs during an ESD event is due to the presence of high defect densities in the device. For example, Figure 5.19 shows SEM pictures of an ESD failure.

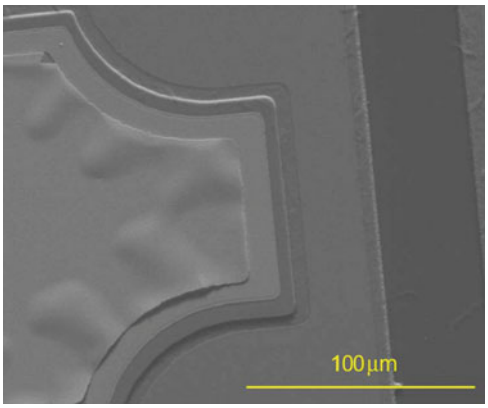


Fig. 5.18 Failure of an ohmic contact detected due to stressing at high current levels [61]

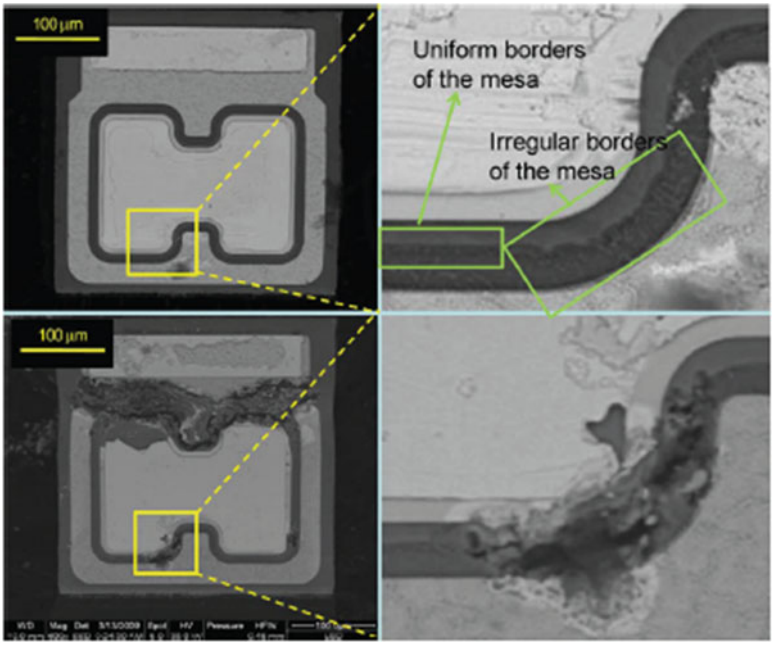


Fig. 5.19 SEM picture of ESD failure of an LED device [61]

Another common cause for the shorting of the P–N junction during an ESD event is the presence of the threading dislocation at the interface of the substrate and epitaxial layer [62]. This dislocation density will then cause an increase in the leakage current. Furthermore, the open core nature of the threading dislocation will facilitate the migration of contract metal resulting in the ohmic resistance between the P and N regions and the subsequent failure of the device.

5.8 Variation of the Local Indium Concentration in the Quantum Wells

Another failure mechanism of the LED emitter is induced by the local indium concentration [52–54]. Pure InN clusters exist within the InGaN layers and are found to be responsible for the light emission in InGaN/GaN MQW structure [52]. However, this emission is highly sensitive to any variation of InN clusters [53].

Interdiffusion of indium and Galium within the InGaN/GaN heterojunctions can occur via vacancy-controlled second-nearest-neighbor hopping. This will result in the intermixing between InGaN quantum wells and GaN barriers and subsequent decrease in the indium concentration. Since a reduction in the indium concentration will result in higher activation energy of Mg acceptors in $In_xGa_{1-x}N$, this will cause a reduction in the hole concentration and hence, a degradation of their optical properties [53].

5.9 Thermal Runaway

Nonhomogeneities in the substrate will result in an area with different thermal and electrical resistance. This will lead to current crowding, which will result in thermal runaway where heat will cause damages that will cause more heating until the eventual failure of the devices. The common cause of their nonhomogeneities are voids caused by electromigration, incomplete soldering, and Kirkendall voiding [62].

5.10 Packaging Degradation

Due to differences in the coefficient of thermal expansion of the materials in a package, the packages will experience significant thermal strains due to the mismatch, which in turn will cause them to fail prematurely [63]. This failure includes epoxies' delamination, fatigue failure for metals, and stability loss for thermal interfaces [63]. One of the common failures is the breakage of the wire bond from the die surface: at elevated temperatures, the forces of the expanding materials can pull the wire bond from the surface of the die due to the differences in the coefficient of thermal expansion of the materials between epoxy encapsulant and the silicone bead [62]. This plastic deformation could result in an electrical open through wire breakage. Another common failure mechanism in LED system due to the thermal mismatch is delamination of the die attach. However, the high strength of the Au/Sn solder may sometime transfer the stress to the device and cause the die to crack.

5.11 Conclusion

This chapter reviews the past research on failure mode and mechanism. A review of the failure mechanisms for the electrical driver system has been performed. Its main failure mechanisms are drying up of electrolytic capacitor, pressure buildup due to the generation of hydrogen, and corrosion of the leads or electrode foils.

Next the optical degradation has been discussed and the failure mechanism includes the degradation of the epoxy such as the yellowing and cracking of the epoxy lens; degradation of the phosphor layer; and the degradation of the LED chip such as the generation of non-radiative centers, generation of magnesium–hydrogen complexes, changes in the processes responsible for the injection of the carriers in the active region of the devices, shortening of the p–n semiconductor junction as a consequence of an ESD event, and changes in the local indium concentration in the quantum wells. Lastly, package failure, due to thermal mismatch, has been reviewed. However, this list is not exhausting since SSL is still a relatively new technology and new failure mechanisms will emerge with insight gained in these technologies.

References

1. International Energy Agency (2006) Light's labours lost—fact sheet. http://www.iea.org/textbase/nppdf/free/2006/light_fact.pdf
2. Alliance for Solid-State Illumination Systems and Technologies (ASSIST) (2007) Recommendations for testing and evaluating luminaires used in directional lighting (cited 2nd Feb 2010). http://www.lrc.rpi.edu/programs/solidstate/assist/pdf/directional3.pdf
3. Mottier P (2009) LEDs for lighting applications. ISTE, Great Britain
4. US Department of Energy (2009) LED applications. http://www.ssl.energy.gov
5. Yole Development Report (2009) HB led & led packaging 2009
6. Nakamura S, Senoh M, Mukai T (1993) P-GaN/N-InGaN/N-GaN double-heterostructure blue-light-emitting diodes. Jap J Appl Phys: Part 2 Lett 32:8
7. Petroski J (2002) Thermal challenges facing new generation Light Emitting Diodes (LEDs) for lighting applications. Solid State Light II 4776:215–222
8. "LED" (2005) The American heritage science dictionary. Houghton Mifflin Company. http://dictionary.reference.com/browse/led and http://www.thefreedictionary.com/LED. Accessed 22 Jun 2011
9. DOE (2009) U.S. LED measurement series: LED luminaire reliability (cited 28 Jan 2010). http://apps1.eere.energy.gov/buildings/publications/pdfs/ssl/luminaire_reliability.pdf
10. Ye H, Zhang G (2011) A review of passive thermal management of LED module. J Semicond 32:014008
11. Philips Lighting. Fortimo LED DLM system. http://www.lighting.philips.co.uk
12. Archenhold G (2009) Driving responsibly, in Mondo arc. Mondiale Publishing Ltd., United Kingdom, pp 93–94
13. Lahyani A et al (1998) Failure prediction of electrolytic capacitors during operation of a switchmode power supply. IEEE Trans Power Electron 13(6):1199–1207
14. Malik R et al (2005) Why do power supplies fail, and what can be done about it. IBM

15. Gasperi ML (1996) Life prediction model for aluminum electrolytic capacitors. Industry Applications Conference, 1996. Thirty-First IAS Annual Meeting, IAS '96, 3:1347–1351
16. Han L, Narendran N (2009) Developing an accelerated life test method for LED drivers. Ninth International conference on solid state lighting, august 3–5 2009, San Diego, Proceeding of SPIE 7422:742209, p 78–86
17. The University of Bolton. Electrolytic capacitors. http://www.ami.ac.uk/courses/topics/0136_ec/index.html
18. Panasonic, Reliability of aluminum electrolytic capacitors, http://industrial.panasonic.com/www-data/pdf/ABA0000/ABA0000TE4.pdf
19. Down JL (1986) The yellowing of epoxy resin adhesives: report on high-intensity light aging. Stud Conserv 31:159–170
20. Down JL (1984) The yellowing of epoxy resin adhesives: report on natural dark aging. Stud Conserv 29(2):63–76
21. Gesner BD, Kelleher PG (1968) Thermal and photo-oxidation of polysulfone. J Appl Polym Sci 12(5):1199–1208
22. Akhavan J et al (2001) Effect of UV and thermal radiation on polyNIMMO. Polymer 42(18):7711–7718
23. Huang JC et al (2004) Comparison of epoxy resins for applications in light-emitting diodes. Adv Polym Technol 23(4):298–306
24. Ollier-Dureault V, Gosse B (1998) Photooxidation of anhydride-cured epoxies: FTIR study of the modifications of the chemical structure. J Appl Polym Sci 70(6):1221–1237
25. Thompson T, Klemchuk P (1993) Light stabilization of bisphenol A polycarbonate. Polymer durability: degradation, stabilization, and lifetime prediction, American Chemical Society, Washington DC, 1996 303–317
26. Anderson J, Reese C (1960) Proceedings of the Chemical Society, London. Photo-induced Fries rearrangements, 217
27. Diepens M (2009) Photodegradation and stability of bisphenol A polycarbonate in weathering conditions. Polymer Degradation and Performance, ACS Symposium Series 1004:287–306
28. Andrady Norma D, Anthony L (1992) Wavelength sensitivity of unstabilized and UV stabilized polycarbonate to solar simulated radiation. Polym Degrad Stab 35:235–247
29. Gupta A, Rembaum A, Moacanin J (1978) Solid state photochemistry of polycarbonates. Macromolecules 11(6):1285–1288
30. Factor A, Ligon WV, May RJ (1987) The role of oxygen in the photoaging of bisphenol A polycarbonate. 2. GC/GC/high-resolution MS analysis of Florida-weathered polycarbonate. Macromolecules 20(10):2461–2468
31. Munro HS, Allaker RS (1985) Wavelength dependence of the surface photo-oxidation of bisphenol A polycarbonate. Polym Degrad Stab 11:349–358
32. Lemaire J et al (1986) Dual photo-chemistries in aliphatic polyamides, bisphenol A polycarbonate and aromatic polyurethanes—a short review. Polym Degrad Stab 15(1):1–13
33. Kameshwar Yadavalli. Solid state lighting. http://www.nd.edu/~gsnider/EE698A/Kameshwar_Light-emitting-diodes.ppt
34. OIDA (2001) Light Emitting Diodes (LEDs) for general illumination. http://lighting.sandia.gov/lightingdocs/JonesEDLEDRoadmap200103.pdf
35. Kawakami Y, Funato M (2008) Light-emitting diode design allows precise control of colors and intensity, 29 April 2008, SPIE Newsroom. doi:10.1117/2.1200804.1109
36. Shao Q et al (2012) Temperature-dependent photoluminescence properties of (Y, Lu)$3Al_5O_{12}$:Ce3+ phosphors for white LEDs applications. J Lumin (in press)
37. Chiang C-C, Tsai M-S, Hon M-H (2008) Luminescent properties of cerium-activated garnet series phosphor: structure and temperature effects. J Electrochem Soc 155(6):B517–B520
38. Coetsee E, Terblans JJ, Swart HC (2007) Degradation of Y_2SiO_5:Ce phosphor powders. J Lumin 126(1):37–42
39. Swart HC, Hillie KT (2000) Degradation of ZnS FED phosphors. Surf Interface Anal 30 (1):383–386

40. Tan CM et al (2008) Humidity effect on the degradation of packaged ultra-bright white LEDs. In: 10th electronics packaging technology conference (EPTC) 2008, Singapore
41. Tan CM et al (2009) Analysis of humidity effects on the degradation of high-power white LEDs. Microelectron Reliab 49(9–11):1226–1230
42. Hyun Ho S, Jae Soo Y (2008) Failure analysis of a phosphor-converted white light-emitting diode due to the CaS:Eu phosphor. Jap J Appl Phys 47(5):3524–3526
43. Tsai CC et al (2009) Investigation of Ce:YAG doping effect on thermal aging for high-power phosphor-converted white-light-emitting diodes. IEEE Trans Device Mater Reliab 9(3):367–371
44. Uddin A, Wei A, Andersson T (2005) Study of degradation mechanism of blue light emitting diodes. Thin Solid Films 483(1–2):378–381
45. Meneghini M et al (2008) A review on the reliability of GaN-based LEDs. IEEE Trans Device Mater Reliab 8(2):323–331
46. Manyakhin F, Kovalev A, Yunovich A (1998) Aging mechanisms of InGaN/AlGaN/GaN light-emitting diodes operating at high currents. MRS Internet J Nitride Semicond Res 3:53
47. Pavesi M et al (2004) Optical evidence of an electrothermal degradation of InGaN-based light-emitting diodes during electrical stress. Appl Phys Lett 84:3403
48. Meneghini M et al (2006) High-temperature failure of GaN LEDs related with passivation. Superlattices Microstruct 40(4–6):405–411
49. Meneghini M et al (2007) Reversible degradation of ohmic contacts on p-GaN for application in high-brightness LEDs. IEEE Trans Electron Devices 54(12):3245–3251
50. Polyakov A et al (2002) Enhanced tunneling in GaN/InGaN multi-quantum-well heterojunction diodes after short-term injection annealing. J Appl Phys 91:5203
51. Meneghesso G et al (2009) Electrostatic discharge and electrical overstress on GaN/InGaN light emitting diodes. IEEE Microelectronics Reliability 39:635–646
52. Youn CJ et al (2003) Influence of various activation temperatures on the optical degradation of Mg doped InGaN/GaN MQW blue LEDs. J Cryst Growth 250(3–4):331–338
53. Chuo CC, Lee CM, Chyi JI (2001) Interdiffusion of In and Ga in InGaN/GaN multiple quantum wells. Appl Phys Lett 78:314
54. Lee W et al (2006) Effect of thermal annealing induced by p-type layer growth on blue and green LED performance. J Cryst Growth 287(2):577–581
55. Grillot PN et al (2006) Sixty thousand hour light output reliability of AlGaInP light emitting diodes. IEEE Trans Device Mater Reliab 6(4):564–574
56. Rossi F et al (2006) Influence of short-term low current dc aging on the electrical and optical properties of InGaN blue light-emitting diodes. J Appl Phys 99:053104
57. Craford M, Steranka F (1994) Light-emitting diodes. Encyclopedia Appl Phys 8:85–514
58. Seager C et al (2002) Drift, diffusion, and trapping of hydrogen in p-type GaN. J Appl Phys 92:7246
59. Polyakov A et al (2003) Hydrogen plasma passivation effects on properties of p-GaN. J Appl Phys 94:3960
60. Myers S et al (2002) Electron-beam dissociation of the MgH complex in p-type GaN. J Appl Phys 92:6630
61. Meneghini M et al (2010) A review on the physical mechanisms that limit the reliability of GaN-based LEDs. IEEE Trans Electron Devices 57:108–118
62. Arnold J (2007) When the lights go out: LED failure modes and mechanisms. http://www.emsnow.com/cnt/files/WhitePapers/DFRLEDFailures.pdf
63. Koh SW (2009) Fatigue modeling of nano-structured chip-to-package interconnections, PhD Thesis, Georgia Institute of Technology, publication number 3364229

Chapter 6
An Introduction to Driver Reliability

S. Tarashioon

Abstract An SSL driver is the interface between the SSL input power, user controls, and the optical part of an SSL device. The reliability of the SSL device is partly defined by the reliability of SSL driver. This text explains about the different issues to study the reliability of an SSL driver. First part is about introducing the different parts and its different application fields. Reliability study is meaningless without having knowledge about the device operational/nonoperational environmental conditions. This information is defined by the SSL driver application field in addition to the device form factor. Thus, the next part is about application field-induced criteria. It is followed by discussion of different common reliability prediction methods and their advantage/disadvantages to apply for SSL drivers. More details of the preferred method, which is based on stress and damage models, are explained.

6.1 Introduction

The electronic control circuitry of a solid-state lighting (SSL) module, as one of the major parts of an SSL module, plays an important role in the reliability of the whole module. Generally, an SSL module consists of three major parts: the optical part, the electronic driving part, and interconnections between the latter two parts. The optical part consists of a number of LEDs usually on a PCB board, and also nonelectrical optical components like lenses and light reflectors. The electronic control circuitry of SSL is the interface between the main power source of the module and the optical part. It can include more advanced controlling functions

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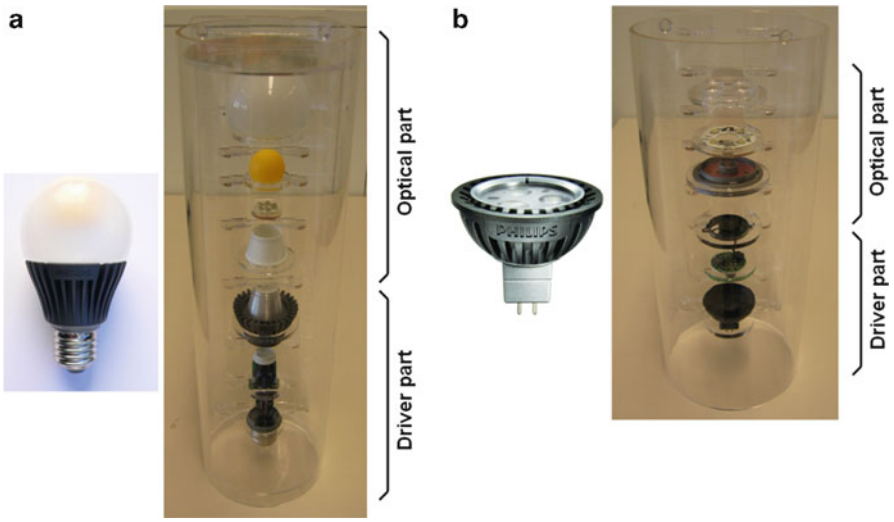


Fig. 6.1 Two examples of Philips SSL devices. In each of the examples *left-side picture* is the device and *right-side picture* is the exploded view of the same device. (**a**) SSL retrofit lamp and (**b**) SSL lamp for halogen lamp sockets

such as sensors and a microcontroller part as well. This SSL electronic control circuitry, for the convenience of use, is called "SSL driver" in this text [1, 2]. In Fig. 6.1 the constructed parts for two examples of SSL devices are shown.

"SSL driver" is a singular term which refers to more than one type of device. It can be as simple as just a transistor and some passive components. It also can be a complex power converter with filters and protections including some sensors and a microcontroller. SSL driver design depends on the application, required light output, and manufacturer demands for size, weight, and cost. This variety makes the discussion of reliability of SSL drivers very broad.

This chapter is a short look at the reliability of SSL drivers [37]. We touch upon the different issues of SSL driver reliability, looking at the different functionalities of SSL drivers in different application fields. Different reliability prediction methods are discussed and what method is preferred for SSL drivers. The discussions give abstract information about different types of SSL drivers, important issues to know before starting a reliability analysis, and what the options are for reliability analysis.

6.2 SSL Driver Functions

Regarding the "ANSI/IESNA RP-16-05 Addendum a" standard, the definition of an SSL module's electronic control circuitry is: "electronic components located between the power source and the LED array designed to limit voltage and current, to dim, to switch, or otherwise control the electrical energy to the LED array."

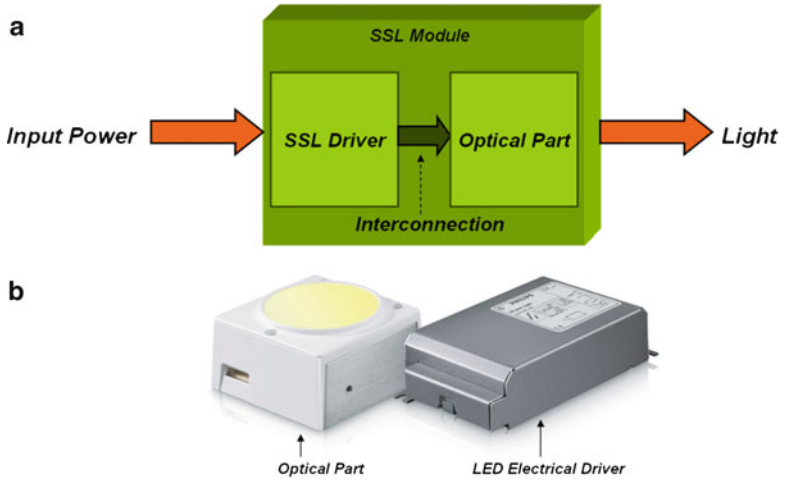


Fig. 6.2 (**a**) An SSL module general block diagram. The three major parts of an SSL module are represented: optical part, SSL driver, and interconnection. (**b**) An example of an SSL device [32, 33]

The circuitry does not include a power source [3]. In other words, an SSL module's electronic control circuitry (in this text called "SSL driver") is the electrical interface to control the electrical energy between the SSL module's optical part and the SSL module's input power source.

The place of the SSL driver in an SSL module block diagram is shown in Fig. 6.2a. The SSL driver input is the input power of the SSL module which is defined by application. For example the input power for retrofit lamp is 220–240 Vac 50 Hz (in European standard) and for halogen lamp is 12 Vac 100 kHz. The SSL driver output is the required power input for the optical part, which is defined by LED type, number of LEDs, and topology of connection of LEDs. The interconnection part (shown in Fig. 6.2a) contains the power lines required for powering up the optical part and also some control signals like dimming functionalities, sensor readout output, etc. Figure 6.2b shows an example of an SSL module for which the optical part and the driver part are separate. Thus we can easily differentiate between the parts of the SSL device. The interconnection between these two parts is a cable which is not shown in this figure.

6.2.1 SSL Driver Basic Functions

Basic functions of an SSL driver can be defined by knowing the basic functionalities of its SSL device. SSL devices are lighting devices and therefore the very basic expected functionalities are to be able to switch the light on and off. The second functionality is dimming capability, which can also be found in conventional lighting technologies. As we have discussed before, the major role

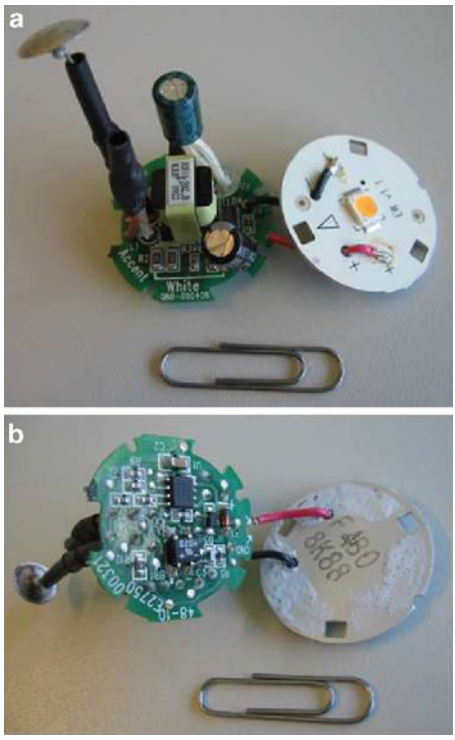


Fig. 6.3 SSL driver and LED board of a commercial retrofit lamp without its external casing. The driver part supports just the basic function to drive the LED part. (**a**) Top part of the boards; the optical part is one high brightness LED. (**b**) Bottom part of the boards

of an SSL driver is to provide the controlling signals and the required power for the optical part. Therefore the basic function of any kind of SSL driver is to provide the proper electrical power for switching a series of LEDs on and off. The dimming function can also be provided by SSL driver either directly or indirectly by having dimming capability by means of an external dimmer [35].

Figure 6.3 shows one example of an SSL device, a retrofit lamp, which provides just the basic function. In the figure, there are its driver and the optical part without the casing or nonelectrical optical elements.

Figure 6.4 shows the major building blocks of an SSL driver with basic functionality. We can categorize the SSL driver based on the type of input electrical power which can be alternative current (AC) or direct current (DC). This distinction changes the input block for the SSL driver. Figure 6.4a illustrates the steps if the input power is AC, and then the first block is an AC to DC converter. As an example for an application with AC input power we can mention retrofit lights. Figure 6.4b illustrates the blocks for when the input power is DC. In that case the first block is to protect the circuit in the occurrence of inverse polarity assembly. Examples of SSL devices with DC input power are automotive applications.

It is worth mentioning that the block diagrams shown in Fig. 6.4 do not show all of the details of functions that exist in an SSL driver. Also, SSL drivers can be even simpler, skipping some of the blocks of the diagram in Fig. 6.4. The simplest driver

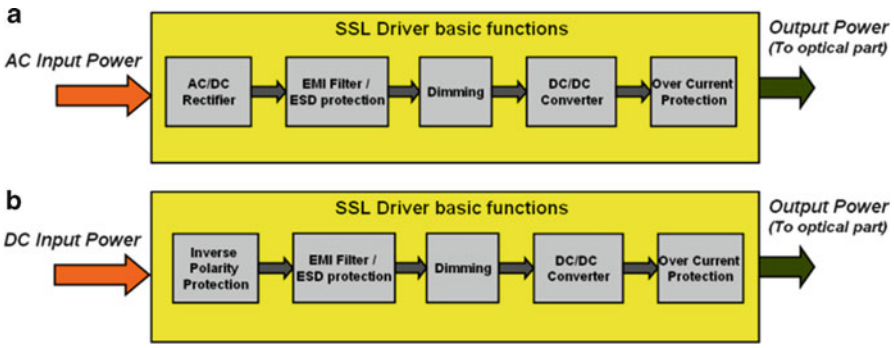


Fig. 6.4 The block diagram of an SSL driver with its basic functions. Regardless of the input block, the rest of SSL driver building blocks are the same. (**a**) When the input power is alternative current (AC) the input block is an AC to DC converter. (**b**) When the input power is direct current (DC) the input block is an inverse polarity protection circuit

for the case of Fig. 6.4a includes only two blocks: AC/DC converter and DC/DC converter. And the simplest configuration for the case of Fig. 6.4b is just a DC/DC converter.

6.2.2 SSL Driver Additional Functions

An SSL device can be more than just a simple lighting device. One existing example is devices equipped with motion sensors for the purpose of energy saving. In the case of not sensing any movement in their field of vision for a specific time period, the lights are turned off. These kinds of devices have some additional functionality other than the basic ones explained in Sect. 6.2.1. Generally, we can categorize the additional functions of SSL drivers into three major categories: processing, monitoring, and communication (Fig. 6.5). In the following paragraphs these three parts are explained with application examples. An example of such an SSL device with these additional functions is shown in Fig. 6.6 in the work by Biano et al. [4].

The monitoring part can be a collection of sensors for monitoring the environmental conditions and also the internal conditions of the SSL device. The sensors for monitoring environmental conditions are mostly implemented to make smart decisions to control the light. One example is the lighting device equipped with a motion sensor which was mentioned in the beginning of this section. Another example can be using a light sensor to measure the ambient light and dim the device light due to this information. This light information can also be used for self-maintenance in a big lighting system [5]. The sensors for monitoring the internal conditions of device can be used for device health monitoring purposes [6, 7]. Another example is the thermal shutdown feature in some LED driver chipsets.

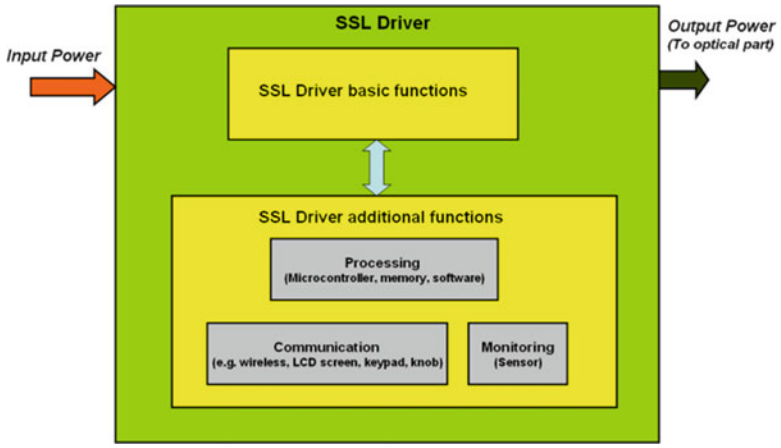


Fig. 6.5 The block of an SSL driver with basic functions and additional functions

The communication part makes the communication possible between individual SSL devices and also between the SSL device and users. The level of communication is different for different users. The capability for dimming the light or changing the light color can be one type of the communication between end user and the SSL device. This can be as simple as a knob or more complex like a remote control. Other kinds of users include the higher level users like system managers and maintenance people. Their communication with devices can be more complicated like receiving the device failure information and data for reprogramming the device. Depending on the type or complexity level of communication between the device and user, the communication part in an SSL driver can be different. It can be just a single wire connected to a key or a screen which shows the health status of the device, or wireless communication for large-scale systems [8].

The processing part is a microprocessor or a microcontroller including the software. This part controls the communication part. It also reads the data from the monitoring part. The processing part controls the light based on the data from monitoring part and communication part. In the mentioned example of a lighting device equipped with a motion sensor, the data from the motion sensor are processed in the processing part and the command for turning off the light is sent.

6.2.3 SSL Driver in Different Application Fields

SSL technology, due to its unique characteristics, gives the opportunity to the designers to use it in a variety of applications. Besides its high efficiency and longer lifetime with respect to conventional lighting, one of the important factors that bring SSL to lots of different application fields is its design flexibility. For SSL technology, design flexibility is about flexibility in light color, light intensity, form factor,

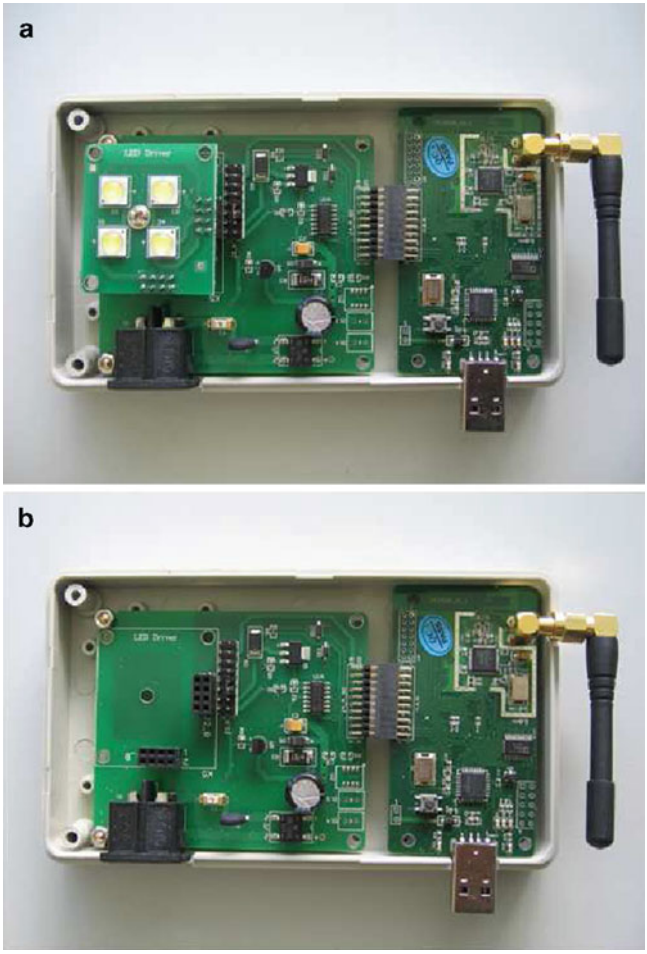


Fig. 6.6 An example of an SSL device with additional functions such as microcontroller, sensors, and wireless communication capability. (**a**) Complete device with optical part and SSL driver and (**b**) just the SSL driver

etc. [1]. There are some examples of application fields for SSL devices as shown in Fig. 6.7: indoor lighting, outdoor/street lighting, and automotive lighting.

Knowing the application field of an SSL device is very essential in all phases of SSL device life cycle: design phase, test, and operational phases. The application field of the device defines the requirements of the design, including the required light output, shape and size of the device, required efficiency with respect to the cost, expected lifetime, etc. In order to define test procedures, we need to know application field conditions [34]. Finally, reliability is meaningless without knowing the conditions that the application field induces and also criteria for performance in that specific application field.



Fig. 6.7 Three examples for different application fields of SSL devices. (**a**) Indoor lighting, (**b**) outdoor street lighting, (**c**) automotive lighting, which in this figure is the headlamp of the car

Figure 6.8 shows the two important aspects of an SSL driver: the technology parameters and application-induced criteria. In this section, we talk about the criteria that different application fields induce. These criteria can be divided into five categories (Fig. 6.8): environmental conditions, user operation profile, performance expectation, cost, and reliability.

Environmental conditions include all the conditions that the surrounding environment forces on the device, referred to as the "mission profile" by some industries. Studying reliability of a device is completely meaningless without knowing these conditions. Referring to Fig. 6.8, there are major categories of environmental conditions: electrical, physical, mechanical, and chemical.

Talking about the environmental conditions for the components of a system refers not only to external environment conditions but also the conditions that the device itself is forcing on its own different parts. One example is in a retrofit lamp; because of its enclosure, the temperature of the SSL driver is not the same as ambient temperature. Another example is an SSL device enclosure which induces

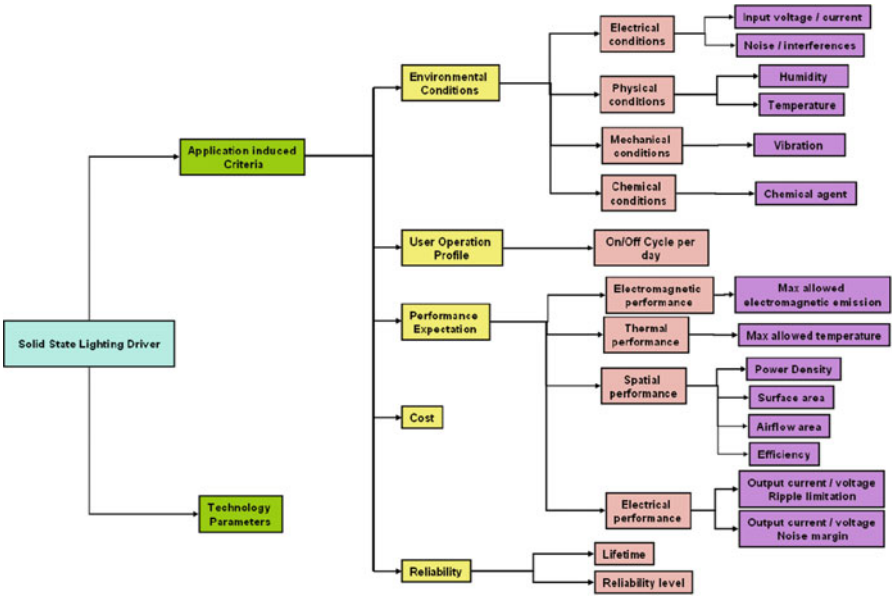


Fig. 6.8 Two important aspects of an SSL driver: the technology parameters and application-induced criteria. In this figure the details related to "application-induced criteria" are shown. In Fig. 6.9 the details of "technology parameters" are explained

mechanical tensile or compressive stresses on the PCB board because of the different thermal expansion coefficients of the case and PCB board.

User operation profile includes all the conditions which are induced on an SSL device because of the way the user handles the device. This includes how many times per day the device is turned on and off, electrostatic discharge (ESD) from user touching the device, etc.

Electrical conditions are input electrical voltage/current, frequency of switching, and any undesirable electrical signals like input voltage surges or additional signals like noises. As an example of an application field with harsh electrical conditions, we can consider SSL devices installed in an industrial environment with lots of electrical motors. In this case the noise level in the environment will be high and it can affect the SSL driver with switching converters.

Mechanical conditions like vibration can be a kind of mechanical stress that devices experience in each application. One of the application fields in which mechanical conditions become critical is the automotive application. SSL devices designed for automotive applications must tolerate a high level of mechanical stress of both vibrations from the engine source and due to driving conditions. For this specific application the standard ISO16750-1 to ISO16750-5 can help to set up suitable tests regarding these conditions [9].

The two most important subcategories of physical conditions are temperature and humidity. High temperature and high level of humidity and also their

combination are the most common failure causes for many electronic circuits. Therefore having enough knowledge about the temperature and humidity of the SSL driver environment condition is very critical. As it has been mentioned before, the conditions are not just the ambient conditions but also what the installation and device enclosure induce on the SSL driver. One of the examples of harsh environment regarding physical conditions is street lighting. In this application the device could be installed in a rainy, hot region and thus experience a high level of humidity and temperature. Also it could be installed in a region near a desert, which can face temperature cycling with very large temperature changes from day to night [10, 11].

Performance expectation differs from one application to another one. One of the parameters that define the performance expectation is safety. For example, for indoor lighting we may tolerate a systemic decrease in the light, but in the automotive headlamp a decrease in the light output decreases the level of visibility of the road for the driver; thus it decreases the level of safety. The level of acceptable light output for some applications is specified [12]. To know the performance expectation for SSL drivers we usually need a translation of the light expectation to a corresponding SSL driver condition [13]. For some of the performance expectation parameters the standards define the accepted levels [36]. For example, the limits for electromagnetic compatibility of the device are defined by classes of FCC. The electrical performance parameters for SSL drivers are the efficiency, output voltage/current level, and ripple in the output [14].

Cost is a driving issue for most of the manufacturing products. In lots of situations decreasing the cost will reduce the performance and reliability. There is always a compromise between different parameters. In some applications like house and office lighting, cost plays a more important role than, for example, in automotive applications. In Fig. 6.8, under reliability category there are two items: lifetime and reliability level. One example of high reliability level is equipping the device with a backup for its critical parts. Having longer lifetime and higher level of reliability seems very desirable. But as we mentioned before, a device is designed based on a compromise of different parameters. One of the parameters which can make the device more expensive, and in some cases bigger, is when we design for a longer lifetime. The application of the device helps decide the compromising point for designing SSL drivers.

It may appear that the criteria induced from an application field should be clear before even starting the design of product. But most of the time this is not the case. Referring to an SSL manufacturing roadmap [15, 16]:

> The lack of driver standards, lack of standard reporting of driver performance, and the lack of availability of high current drivers were all identified as manufacturing roadblocks to luminaire production. This is likely the result of the rapidly evolving performance of LEDs, particularly in terms of their input power requirements, and the variety of luminaire architectures, which all have different incoming power requirements. This results in the problem of most power supplies/drivers being specialized or custom products, which makes them difficult to specify and expensive. This difficulty is compounded by the varied performance reporting of the power supplies/drivers.

Table 6.1 Example of application-induced criteria or as it is called in some industries "mission profile" for internal and external SSL driver for outdoor products

Item		Attribute	Unit	Internal driver	External driver
Physical conditions	Operating ambient temperature	Minimum	°C	25	−20
		Maximum	°C	85	85
		Cycles/24 h	–	1	1
		# of operating	h/day	12	12
		# of operating	h/year	4,000	4,000
	Relative humidity	Minimum	% RH	30%	30%
		Maximum	% RH	60%	95%
Electrical conditions	Electrical stress (mains)	Average voltage	V	230	
		Range	V	110–277 (−6%, +8%)	
		Overvoltage	%	−10%, +10%	
		Interrupts, spikes, surge	–	EN 61000-4-11	
Chemical conditions	Dust	IP-class	–	NA	IP66
User operation conditions	Power scheme	Cycles/day	–	1	
		On/off (mains)	–	On/off (no dimming)	
		Standby	–	No	
		Total operating	h/day	12	

There are lots of cases for SSL applications where the conditions and requirements are not even exactly known to the customers. Further still, knowing the performance and operation conditions for SSL devices and more specifically for SSL drivers can be a challenge. Table 6.1 shows an example of application-induced criteria for internal and external SSL driver for outdoor products. One example of external driver is down light module shown in Fig. 6.2 which faces the same environmental conditions as whole SSL device. Internal driver is actually the built-in driver inside the SSL device; therefore driver environmental conditions are milder than SSL device itself.

As the conclusion for this section, there are a wide range of different application fields for SSL devices and systems. For a reliability study of an SSL driver, it is essential to know what conditions the application field forces on the device. We explained some example fields for which there are already products available in the market. However there are a lot of other application fields like medical applications, agricultural applications, etc. There is a lot of research going on in new applications.

6.3 SSL Driver Technology

There are two important aspects of an SSL driver in regard to a reliability study: application-induced criteria and technology parameters. In the previous section, the application-induced criteria were explained. In this section we focus on technology parameters. The addressed SSL driver in this section is the SSL driver with basic functions.

In Sect. 6.2, different functions that an SSL driver can accomplish were explained. Also explained was that each SSL driver is constructed from many different components: electrical, thermal, and mechanical. The main functionality of each SSL driver is to convert the input power to the required power for the optical part. SSL drivers with basic functions are power electronics in the very low power range (a few Watts). We may also have an SSL system on a very large scale with central control but distributed driver functions. Therefore we never face a single SSL driver with very high power.

For studying any complex system reliability, we always need to break down the system to its constructed elements. Jelena Popovic et al. [17] introduced an approach for studying the level of integration in power electronics to break down a converter to its construction parts according to the functions they perform. This approach is suitable for the reliability study in power electronic, and specifically in our case, for SSL drivers. Studying the reliability of construction parts while considering their functions has a big advantage. The parts which accomplish the same function usually tolerate the same stresses and therefore face the same failure modes.

In Fig. 6.9 two important aspects of an SSL driver are shown with focus on technology parameters. In this figure the methodology of breaking down an SSL driver based on the functionality of construction part is shown.

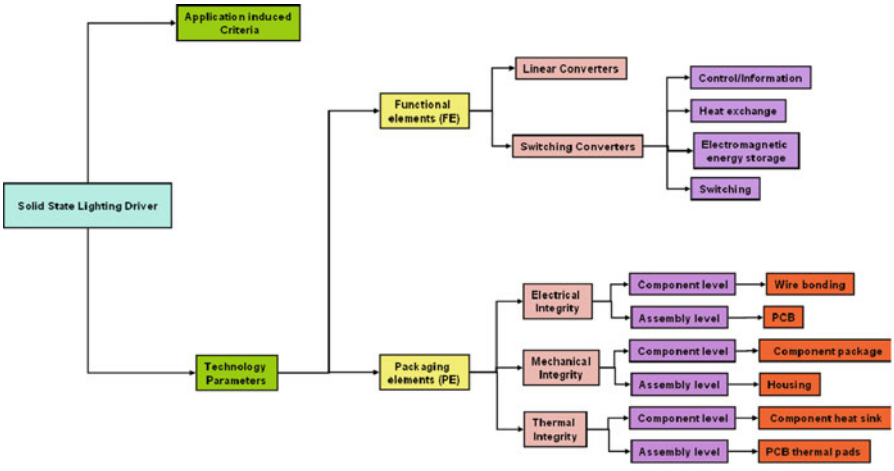


Fig. 6.9 Two important aspects of an SSL driver: the technology parameters and application-induced criteria. In this figure the details related to "technology parameters" are shown. In Fig. 6.8 the details of "application-induced criteria" are explained

Table 6.2 Typical fundamental function elements in SSL drivers

Fundamental function	Functional elements
Switching	Power semiconductor die (MOSFET, diodes)
Control/information	Control semiconductor die (silicon die)
Electromagnetic energy storage	Magnetic core
	Magnetic wire and planar copper conductors
	Metalized foil
	Metalized ceramic layer
Heat exchange	Heat sink
	Heat pipe, fan

6.3.1 Fundamental Function Elements

The main functionality of an SSL driver is embodied in the following functions. It should be mentioned that in this part the additional functions that were discussed in Sect. 6.2.2 have not been taken into account [18]:

- Switching function: Controls the flow of electromagnetic energy through the converter.
- Electromagnetic energy storage function: Provides the continuity of energy when interrupted by the switching function.
- Heat exchange function: Provides the exchange of the heat dissipated in the converter with the environment.
- Control/information function: Enables the required relationship among the previous functions.

These functions will be referred to as "fundamental functions." In Table 6.2, the typical fundamental function elements in SSL drivers are shown.

6.3.2 Packaging Function Elements

In addition to the fundamental functions described above, there are functions necessary to provide the integrity of those fundamental functions of the converter to maintain the functionality. These functions are classified into three categories [17]:

- Functions that provide electrical integrity:
  - Electrical interconnection: Providing electrical path for power and signals.
  - Electrical insulation: Providing integrity of electrical signals.
- Function that provides thermal integrity: Provides heat paths for the dissipated heat from the dissipated part to the heat exchanger in order to ensure that these parts operate in their allowed temperature range.

Table 6.3 Typical packaging elements in SSL drivers

Packaging function		Packaging elements	
Electrical integrity	Interconnection	Component level	Wire bonds
			Semiconductor lead frames
			Bobbins (pins)
			Leads
		Assembly level	Copper tracks
			Via holes
			Copper bus bars
			Pins
	Insulation	Component level	Wire insulation
		Assembly level	Dielectric carrier (PCB dielectric, ceramic)
			Dielectric tapes, adhesives
Mechanical integrity	Mechanical support	Component level	Leads and lead frames
			Bobbin
		Assembly level	Circuit carrier
			Base plate
			Bus bars
	Protection	Component level	Polymer case (molded plastic, epoxy coating)
		Assembly level	Silicone gel
			Metal housing
Thermal integrity		Component level	Cases, lead frames
		Assembly level	Thermally conductive circuit carrier
			Thermal interface materials

- Functions that provide mechanical integrity:
  - Mechanical support: Provides mechanical support, rigidity, and ductility.
  - Environmental protection: Provides protection of the parts and assembly from damaging due to handling and environmental effects, especially moisture.

These functions will be referred to as packaging functions. In Table 6.3, the typical packaging elements in SSL drivers are mentioned.

6.4 SSL Driver Reliability Analysis

The first step for reliability analysis of an SSL driver is knowing about the criteria that the application induces and also the technology that comprises the SSL driver. The next step is to discuss about different methodologies for reliability analysis. We also discuss which methodology is the most suitable for SSL drivers.

6.4.1 Reliability Prediction Methods

There are many different approaches for executing a reliability study. We can divide them into four categories. Reliability prediction methods based on "field data," "test data," "handbooks," and "stress and damage models." In this section, first there is a short explanation about each method and afterwards, a discussion about how each of the methods can be used for the SSL drivers. For more extensive information about different prediction methods, refer to standard IEEE1413.1 2002 [19].

6.4.1.1 Prediction Based on Test Data

Test data are the data which are collected as the result of tests in the manufacturing environment. The value of tests depends on how much the test environment is close to actual environment. Thus reliability tests should be planned very carefully. Generally, there are two types of reliability test data: non-accelerated test data and accelerated test data.

In non-accelerated test data, tests are conducted under nominal load (stress) conditions. These conditions can be of any conditions that the device will face in the real status, like high temperature, humidity, etc. But as the condition in the real operational status is not always completely known, it is sometimes difficult to plan the test, the results of which duplicate the failures found in real-life conditions. During the test procedure, one or more points are monitored. Choosing the test monitoring points depends on different parameters: the best point to show the functionality, the fastest point to detect failure, or the easiest point based on measurement method and instruments.

Accelerated testing is a reliability prediction method performed within a short period of time. The length of test time is usually much shorter than the lifetime of the device in its life-cycle conditions. The goal in accelerated testing is to accelerate the damage accumulation rate for relevant wear-out failure mechanisms. Accelerated tests are not possible without knowing about the major failure causes. Defining the acceleration factor is very essential because if we accelerate the stress too much, the sample may fail due to different failure modes which never happen in the device life-cycle conditions. Some examples of models that can be used to derive acceleration factors are the Coffin–Manson inverse power law model, Rudra's inverse power law model, Peck's model for temperature–humidity, and Kemeny's model for accelerated voltage testing [20, 21].

6.4.1.2 Prediction Based on Field Data

Field data are directly representative of device operation in device life-cycle conditions. The major challenge of prediction based on field data is how to collect the data. Three types of information are required: initial operation time, operating

profile which includes the environmental conditions, and finally failure time for the failed devices. In complex systems with regular maintenance and monitoring, collecting data is easier. But in home appliances we can generally just rely on information from the returned products which is not always the best representation of the whole population of the manufactured and sold devices.

6.4.1.3 Prediction Based on Handbooks

Handbook prediction methods can be used for reliability prediction for electronics and electrical components and systems when the failure mode is standard and previously established. The data in these handbook methods are based on historical data collected from field testing or lab testing, usually from different manufacturers of the components. For system-level reliability calculations, most of the handbook methods assume that the components fail independent from each other.

All handbook prediction methods contain one or more of the following types of prediction [19]:

1. Tables of operating and/or nonoperating constant failure rate values arranged by part type
2. Multiplicative factors for different environmental parameters to calculate the operating or nonoperating constant failure rate
3. Multiplicative factors that are applied to a base operating constant failure rate to obtain nonoperating constant failure rate

There are lots of handbooks and some of them are written for specific application fields. The first one is MIL-HDBK-217 [22] which was published in the 1960s. Examples of some popular and more updated ones are RIAC's 217PLUS, Telcordia RS332, RDF 2000/2003-IEC62380, and FIDES 2009. To choose the proper one for the specific product there are a number of items that can be considered. As an example we can mention age of the handbook, typical products aimed, if it contains the part count/part stress methods, if it contains the multiplicative/additive factors, and if it has any system-level consideration. These items are some examples of the criteria used to choose the most suitable handbook for different cases.

6.4.1.4 Prediction Based on Stress and Damage Model

The objective of a reliability prediction based on a stress and damage model is to assess the time-to-failure and its distribution for a system and its components, evaluating individual failure sites which can be identified and modeled based on the construction of the system and its anticipated life cycle. The stress and damage model approach is based on the understanding of system geometry, material construction, operational requirements, and anticipated operating and environmental conditions [19].

In this approach the failure modes, mechanisms, and failure causes are discussed. The results of the prediction based on physics of failure are valuable

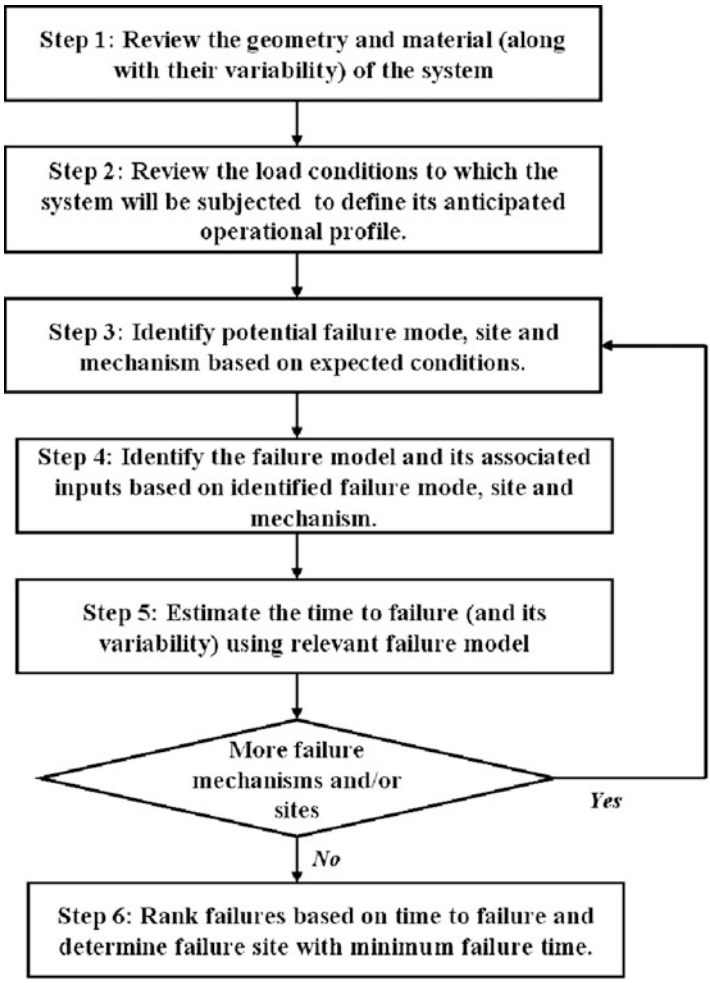


Fig. 6.10 Generic process of estimating the reliability of an electronic system based on stress and damage model

data for improvement in all stages of the device life cycle: design, test, production, storage, handling, installation, operation, and maintenance.

Figure 6.10 is the flowchart of the stress and damage model methodology. Step 1 is reviewing geometry and materials of the constructed parts of the system. It is followed by Step 2, reviewing loads and stresses which are being induced in the system like voltage, temperature, humidity, etc. In Step 3, we identify failure modes that the system can experience, e.g., electrical short circuit or open circuit. The sites of possible failure will be specified. Finally, the mechanisms of the failure are identified like corrosion, fracture, fatigue, etc. A system is a construction of different parts and due to the loading conditions all constructed parts can fail.

Table 6.4 Comparison of reliability prediction methodologies

	Field data	Test data	Stress and damage models	Handbook methods
Are sources of uncertainty in the prediction results identified?	Can be	Can be	Can be	No
Are limitations of the prediction results identified?	Yes	Yes	Yes	Yes
Are failure modes identified?	Can be	Can be	Yes	No
Are failure mechanisms identified?	Can be	Can be	Yes	No
Are confidence levels for the prediction results identified?	Yes	Yes	Yes	No
Does the methodology account for material, geometry, and architectures that comprise the parts?	Can be	Can be	Yes	No
Does methodology allow incorporation of reliability data and experience?	Yes	Yes	Yes	Yes (some)
What probability distributions are supported?	Not limited	Not limited	Not limited	Exponential
Can it provide a reliability prediction for nonoperational conditions?	Yes	Yes	Yes	No (except PRISM)

The complete list of comparison between prediction methodologies can be found in IEEE std 1413.1 [19]

The ones which have higher probability of failing sooner and will lead the system to fail are important to study. In order to distinguish these dominant failures we can use the experiences from similar systems and highly accelerated life test (HALT).

In the flowchart of the stress and damage model in Fig. 6.10, Step 4 connects all information from previous steps together to identify a model for evaluating the time-to-failure for different failure mechanisms. As examples of these we can mention the Arrhenius, Eyring, and Coffin–Manson models. In Step 5 the time-to-failure for the specific failure mechanism, by means of the failure model, is estimated. Steps 2–5 are repeated for all failure mechanisms and failure sites. In the last step, Step 6, based on time-to-failure of different failure mechanisms, we can distinguish the dominant failure mechanism. This information not only gives a good sight about time-to-failure but is also valuable for the designer to improve system reliability.

6.4.2 Comparison of Reliability Prediction Methods for SSL Drivers

In above discussions we introduced four reliability prediction methods. Applying each method for SSL drivers has advantages and disadvantages.

Table 6.4 shows the general comparison between these methods. In the following paragraphs we discuss each method's advantages and disadvantages for SSL

drivers. Finally, we conclude with the most suitable method(s) for SSL driver reliability prediction.

Reliability prediction based on handbooks. Handbook prediction methods are still one of the most commonly used methods to predict the electronic circuits' reliability. For SSL drivers, it is also broadly used by manufacturers and designers. It is because of fast development of SSL devices and lack of enough field information. The other reason is that manufacturers want to introduce their new products very fast to the market and prediction methods based on test data can be very time consuming.

The disadvantage of using handbook methods for SSL drivers is that they do not give identical results for the same product. Sometimes their results are pretty far from each other. This does not give useful feedback information to the designer. If the predicted reliability is not desirable and there is a need for improvement, handbook results cannot be useful. The other disadvantage is that the stress conditions (e.g., temperature or electrical stresses) that we can apply in handbook methods are limited. For example in the Telcordia RS322 handbook [23], the temperature can be defined but it assumes that the temperature during the lifetime of the device is constant. Therefore it is not valid for applications with temperature cycling in their lifetime, like street/road lighting.

We can conclude that, although this method is often applied due to its ease of use, it cannot be the best choice for studying the reliability of SSL drivers.

Reliability prediction based on field data. The advantage of prediction based on field data for SSL drivers is the same for every other kind of product; it is a prediction based on operation in their real life-cycle conditions. SSL is a relatively new technology with a longer lifetime with respect to other lighting technology. The disadvantage of this method for SSL drivers is not having enough field data available for any SSL product. Therefore, because of the lack of enough information at the present time, this is not the best method for reliability prediction for SSL drivers.

Reliability prediction based on test data. Illuminating Engineering Society (IES) [24] has introduced LM-80-08 standard which is an approved method for measuring lumen maintenance of LED light sources. This method covers the measurement of lumen maintenance of inorganic LED-based packages, arrays, and modules [25]. This method is a non-accelerated test method which needs the whole device to be able to run the test: optical part plus the driver. The results show the behavior of the complete device and it is hard to distinguish the role of the SSL driver. The other drawback of this method is that due to very long lifetime of the SSL module and SSL driver, it will take a long time to run the test. For accelerating tests, research is still going on. We need the proper information about the failure causes to be able to accelerate those specific stresses.

Reliability prediction based on stress and damage model. This model, by using the knowledge from the physics of the device, is the best candidate for SSL driver reliability. By setting up a good foundation of the failure models for the device, the information can be used to set up accelerated tests as well. So these two models can

be interrelated with each other. The disadvantage is that still more research needs to be done and at the present time it cannot give a fast answer for the reliability of an SSL driver.

6.5 Failure Analysis of SSL Driver

In the previous section we discussed different reliability analysis methods and the advantages/disadvantages of each method for SSL drivers. The conclusion was that the prediction based on stress and damage model is the best choice we can make. The results from these methods help the prediction method based on test data. Referring to Fig. 6.10, after identifying the technology parameters and load conditions, it is required to identify the potential failure mode, site, and mechanism according to load condition. In Sect. 6.3, it was explained how to break down an SSL device into its constructed parts. In this section some potential failure causes, modes, and mechanisms of these parts are introduced based on existing literature.

6.5.1 Failure Causes, Modes, and Mechanisms

Different stress loads on the SSL driver can be the causes of SSL driver failure. These loads can be thermal, electrical, humidity, mechanical, etc. A "failure mode" is the observed electrical or visual symptom which generally describes the way the failure occurs. Failure modes can range from catastrophic to slight degradation, and they are typically categorized as functional, parametric, or visual. An example of the failure mode in electrical components can be a short circuit or open circuit. "Failure mechanisms" are physical, chemical, or other processes that cause a failure. Different types of failure mechanisms can lead to the same failure mode. As examples of failure mechanisms we can mention electromigration (EM) in interconnections and dielectric breakdown in transistors [26].

After breaking down an SSL driver to its constructed parts, some of their typical failure modes, mechanisms, and causes are introduced. In Table 6.5 there is a list of the fundamental function elements and their potential failures. It is followed by the list of typical failures of packaging elements of an SSL driver in Table 6.6.

6.5.2 The Weakest Links in SSL Driver

The first failures of elements or components which lead the whole device to fail are called the weakest links in the system. In reliability based on stress and damage model (Fig. 6.10), the last step is to rank failures based on time-to-failure and determine failure site with minimum failure time. To define the weakest link in SSL

Table 6.5 Examples of potential failure modes and mechanisms and their causes for fundamental functions in SSL drivers [6, 10, 27]

Fundamental function	Functional elements	Potential failure mode/ failure mechanism	Failure causes
Switching	Power semiconductor die (MOSFER, IGBT, diodes)	Time-dependent dielectric breakdown	Voltage, temperature
Control/ information	Control semiconductor die (Si die)	Fatigue in die attach, fatigue in wire bonding, corrosion in metallization, EM in metallization, TDDB, fatigue in solder leads	Temperature, current density, humidity, voltage cycling, mechanical stress
Electromagnetic energy storage	Magnetic core, magnetic wire and planar, copper conductors, metalized foil, metalized ceramic layer	Wire corrosion, dielectric breakdown, termination break, fracture in ceramic dielectric, internal delaminations or void, silver migration	Voltage, temperature, mechanical stress
Heat exchange	Heat sink, heat pipe, fan, thermal pads, copper planes	Fatigue in bond pads, thermal paths, and traces	Mechanical stress, voltage

driver, the second parameter to study about failures is how much each failure can affect the whole SSL driver reliability. Some failure modes may not affect the device performance and reliability; one example is when there is a small crack in the SSL driver enclosure in an indoor application. Since one of the important enclosure's main functions is to protect the device from moisture, being in an environment with very low level of humidity does not affect the performance and reliability of the device. Nevertheless some elements' failure can be fatal to the device, like failure of the switching function element; there will be no output power for the SSL driver and consequently there will be no light output from the SSL device.

One of the most vulnerable parts of an SSL driver with the switching converter is the energy storage part and switching part. The high-power electrical energy passes these two parts and also they face on an off cycles with a relatively high frequency. Power transistor die electric part can fail due to high temperature and temperature variation. High voltage can be another reason for its failure. Capacitors and inductors as the energy storage components also show high rate of failure. Capacitors, especially electrolytic capacitors, play more important role in device failure [28–31]. The other common source of failures is in interconnections parts. In PCB level due to temperature, humidity, mechanical stress, etc. cracks produced in solder joints and copper pads are delaminated from the PCB. Lots of interconnections in driver play role as heat exchangers as well; thus failure in interconnection part also affects the thermal behavior of the driver.

Table 6.6 Examples of potential failure modes and mechanisms and their causes for packaging functions in SSL drivers [6, 10, 27]

Packaging function		Packaging elements		Potential failure mode/failure mechanism	Failure causes
Electrical integrity	Interconnection	Component level	Wire bonds, semiconductor lead frames, bobbins (pins) leads	Fatigue in wire bonds, fatigue in lead frames, electromigration	Temperature cycling, voltage, humidity
		Assembly level	Copper tracks, via holes, copper bus bars, pins	Delamination and crack in copper tracks, solder joint fatigue/cracking	Voltage, temperature, mechanical stress, temperature cycling, vibration
	Insulation	Component level	Wire insulation	Insulation melted	Temperature
		Assembly level	Dielectric carrier (PCB dielectric, ceramic)	Fracture in dielectric	Temperature, voltage
			Dielectric tapes, adhesives		
Mechanical integrity	Mechanical support	Component level	Leads, lead frames, bobbin	Substrate cracking, underfill cracking	Temperature cycling
		Assembly level	Circuit carrier, base plate, bus bars	Circuit carrier cracking	Mechanical stresses, vibration
	Protection	Component level	Polymer case (molded plastic, epoxy coating)	Package cracking	Temperature cycling, voltage
		Assembly level	Silicone gel, metal housing	Package cracking, void, water penetration	Temperature cycling, mechanical stresses
Thermal integrity		Component level	Cases, lead frames	Case cracking, fatigue in lead frames	Temperature cycling, mechanical stresses
		Assembly level	Thermally conductive circuit carrier	Crack in circuit carrier	Mechanical stresses
			Thermal interface materials		

6.6 Conclusions and Recommendations

Depending on application field, pricing issue, expected reliability level, etc., there is a great variety of SSL drivers. Therefore in this chapter, the goal is to cover the general information for studying the reliability of SSL driver. First, the different structures and technologies in SSL driver were explained. Then we discussed reliability methods and the most proper one for an SSL driver reliability study. The last part provided information about the failure causes, modes, and mechanisms in SSL drivers and also introduced the weakest links regarding the reliability issue.

Among four common reliability prediction methods, handbook methods and reliability based on test data are being used more often than the other methods. Reliability based on field data is not applicable yet because of long lifetime of the SSL and it being a relatively new technology. Method based on stress and damage model is the most attractive one for the case of SSL driver. This method not only can give estimation about lifetime of the driver but also includes valuable information for designer to improve its design regarding reliability issue. The disadvantage of this method is that it is not a fast solution and it takes time to understand and develop a proper model.

References

1. Held G (2008) Introduction to LED technology and applications. Auerbach Publication, Taylor & Francis Group, United States of America
2. Zukauskas A, Shur MS, Caska R (2002) Introduction to solid state lighting. Wiley, New York, NY
3. ANSI/IESNA RP-16-05 Addendum a (2005) Nomenclature and definitions for illuminating engineering, IES standard
4. Biano A, Tarashioon S, van Zeijl HW, Cheng G, Sarro P, Zhang GQ (2010) Compact and cost effective system integration for solid state lighting module. In: Proceedings of 7th China international forum on solid state lighting, October 2010, Shenzhen, China
5. Dong J, van Driel W, Zhang G (2011) Automatic diagnosis and control of distributed solid state lighting systems. Opt Exp 19(7):5784
6. Pecht MG (2008) Prognostics and health management of electronics. Hoboken, New Jersey
7. LED driver for automotive, ASL10XXNTK and ASL10XXPHN series, NXP semiconductor. http://www.nxp.com/#/homepage/cb=[t=p,p=/53426/71502]|pp=[t=pfp,i=71502]
8. Guo C, van Zeijl H, Zhang GQ, Venkatesha Prasad R (2010) An integrated large SSL system with wireless communications. In: Proceedings of 2010 international conference on electronic packaging technology & high density packaging (ICEPT-HDP), Xi'an, China
9. ISO 16750-1 to 5. Road vehicles environmental conditions and electrical testing for electrical and electronic equipment, ISO standards
10. Microelectronics failure analysis, Desk reference, 4th edn. Electronic Device Failure Analysis Society (EDFAS), Switzerland 1999
11. Lasance CJM (2009) Challenges in LED thermal characterization. In: 10th international conference on thermal, mechanical and multiphysics simulation and experiments in micro-electronics and micro systems, EuroSimE 2009

12. ASSIST recommendation, LED life for general lighting: definition of life, vol 1, issue 1, February 2005
13. Mission profile for system components, reliability of power electronics systems, ECPE workshop, Aalborg, Denmark 2011
14. Billings K, Morey T (2011) Switchmode power supply handbook, 3rd edn. Mc Graw Hill, New York, NY
15. US Department of Energy (2009) Solid-state lighting research and development: manufacturing roadmap, September 2009
16. US Department of Energy (DOE) (2009) Solid state lighting manufacturing roadmap, Vancouver, Washington
17. Popovic J et al (2005) An approach to deal with packaging in power electronics. IEEE Trans Power Electron 20(3):550–557
18. van Wyk JD (2000) Power electronics technology at the dawn of a new century-past achievements and future expectations. In: Proceedings of power electronics and motion control conference, vol 1, 15–18 Aug 2000, pp 9–20
19. IEEE std 1413.1-2002. IEEE guide for selecting and using reliability prediction based on IEEE 1413, IEEE standard coordinating committee 37, New York, NY, USA
20. Nelson WB (2004) Accelerated testing, statistical model, test plans and data analysis. Wiley, New York, NY
21. Porter A (2004) Accelerated testing and validation. Elsevier, Amsterdam
22. MIL HDBK217-E (1990) Notice 1, reliability prediction of electronic equipment. Military handbook
23. Telcordia technologies special report, Reliability prediction procedure for electronic equipment, SR332, Issue 1, May 2001, USA
24. Illuminating Engineering Society (IES). http://www.ies.org/
25. IESNA LM-80-08 standard (2008) IES approved method for lumen maintenance of LED light sources
26. Pabbisetty SV et al (2009) Failure mechanisms in integrated circuits. Texas Instruments, Semiconductor Group, Stafford, TX
27. Salemi S et al (2008) Physics of failure handbook of microelectronic systems, reliability information analysis center RiAC, Utica, New York
28. Lahyani A et al (1998) Failure prediction of electrolytic capacitors during operation of a switchmode power supply. IEEE Trans Power Electron 13(6):1199–1207
29. Malik R et al (2005) Why do power supplies fail, and what can be done about it. IBM Corporation, Technical report, Oct 2005
30. Han L, Narendran N (2009) Developing an accelerated life test method for LED drivers, Lighting Research Center, Technical report, Troy, New York
31. Gasperi ML (1996) Life prediction model for aluminum electrolytic capacitors
32. http://www.lighting.philips.com/main/index.wpd
33. http://www.usa.lighting.philips.com/connect/LED_modules/fortimo_DLM.wpd
34. IESNA LM-79-08 standard (2008) IES approved method for the electrical and photometric measurements of solid state lighting products
35. Winder S (2008) Power supplies for LED lighting. Elsevier, Amsterdam
36. US Department of Energy (DOE) (2009) CALiPER Program
37. Archenhold G (2009) Why LED driver reliability will be essential for SSL to succeed, Mondo Magazine. Issue 48, Apr/May 2009

Chapter 7
Highly Accelerated Testing for LED Modules, Drivers, and Systems

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Abstract Highly Accelerated Lifetime Testing (HALT) and Multi-Environment Overstress Testing (MEOST) procedures are used to test the reliability of LED modules, drivers, and systems. HALT and MEOST are very useful test methods to assess the reliability of LED modules, drivers, and systems. However experiences are only recent and hardly any significant feedback from the market is received. For assessment of the driver reliability a main advantage is the structural similarity with many Switch Mode Power Supplies used for other, traditional, lighting applications. For LED module- and system-level constructions, design and materials used often are new. Many different system solutions exist and many will still be developed at an increasing speed. This implies a higher reliability risk for LED modules and systems. In this chapter, we describe our current results of HALT and MEOST procedures for LED modules, drivers, and systems.

7.1 Introduction

The approach of Highly Accelerated Lifetime Testing (HALT) in the electronic industry was first worked out systematically by Mr. G. Hobbs [1], already almost 20 years ago. A HALT is a stress testing methodology for accelerating product reliability during the engineering development process. It is commonly applied to electronic equipment and is performed to identify and thus help resolve design weaknesses in newly developed equipment. Thus it greatly reduces the probability of in-service failures (i.e., it increases the product's reliability). Progressively more severe environmental stresses are applied building to a level significantly beyond what the equipment will see in-service. By this method weaknesses can be

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identified using a small number of samples (sometimes one or two but preferably at least five) in the shortest possible time and at least expense. A second function of HALT testing is that it characterizes the equipment under test, and identifies the equipment's safe operating limits and design margins. Data from a HALT test is therefore used as a basis for the design of an optimal "Highly Accelerated Stress Screening (HASS)" or "ESS" test [2, 3], which is used to screen every piece of production equipment for latent manufacturing defects and defective components. HASS is an extension of HALT, but is applied during production. Individual components, populated printed circuit boards, and whole electronic systems can be subjected to HALT testing. The size of the test sample is governed by many factors including the number of samples available, cost, type of stresses applied, and physical size. For example, component manufacturers can typically test thousands of individual components at one time whereas often it is not economically feasible to write off more than a few items of very expensive equipment because production quantities or the application does not justify the cost. A general principal is that whilst HALT test can and should be conducted at unit level, it is very desirable to conduct it at subassembly and piece-part level as well. Temperature cycling and random vibration, power margining and power cycling are the most common forms of failure acceleration for electronic equipment [4]. HALT does not measure or determine equipment reliability but it does serve to improve the reliability of a product. It is an empirical method used across the industry to identify the limiting failure modes of a product and the stresses at which these failures occur. A significant advantage of accelerated life testing is that it can be conducted during the development phase of a product to weed out design problems and marginal components. Thus a consumer products company can achieve better customer satisfaction because fewer products have to be returned for repair, and can also save money on warranty returns, or an aerospace manufacturer can avoid catastrophic failures in aircraft or space vehicles. Another major advantage is that the design team can be moved on to designing new products rather than becoming occupied with problems in older products. On military design and development programs HALT is conducted before qualification testing. By so doing, significant cost savings can be accrued, because the formal qualification of the equipment and subsequent customer acceptance will proceed more rapidly and at lower cost, and the need for multiple redesigns and repeat testing (regression tests) will be greatly reduced or eliminated. One of the drawbacks of the HALT approach is the focus primarily on temperature and mechanical stresses.

In Philips Lighting HALT testing started about 6 years ago to improve the reliability of electronic drivers for gas discharge lamp headlamps in the automotive industry. The method was transferred to optimize drivers for different types of discharge lamps. This helped in improving the reliability; however, also in many cases field failures could not be reproduced. Also failures occurred which did not occur in the field. The main reason was that in the applied HALT testing stresses have been increased rapidly, resulting in components operated quickly too far outside the specifications.

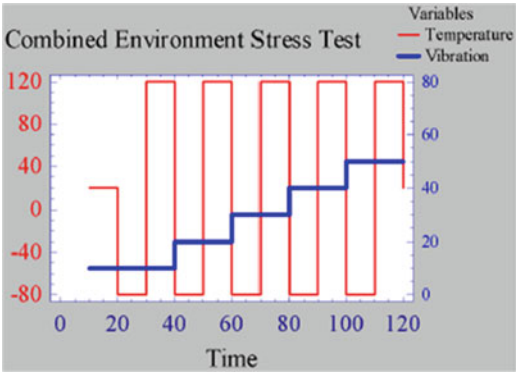


Fig. 7.1 Example stress profiles in an HALT experiment

Improvements of the HALT testing method to deal with nonrepresentative failures in the USA already had been proposed by Mr. Keki Bhote [5, 6]. He named this extension to the HALT method Multi-Environment Overstress Testing (MEOST). The first step is that after having determined the HALT-destruct limits of the single stresses, a combined stress test is executed within the destruct limits of the product under test, while at the same time the testing time is much longer (1). Also it is then important that the product is tested as much as possible in a way which is representative as how it is used in the field (2). The final extension to optimize MEOST is to calibrate the testing profile by reproducing field failures (3). In 2009 we optimized our testing approach by designing an MEOST testing profile which improved coverage of detecting issues from a list of 12 different kinds of field failures from 40 to 70%. The characteristics of this profile are still used continuously when new or derived types of drivers for lamps are tested and since 2 years also for electronic drivers of LED modules. Figures 7.1 and 7.2 show two example stress profiles in a HALT and MEOST experiment, respectively.

Since 2 years we have explored how HALT and MEOST can be used to verify new LED modules, drivers, and systems effectively. For testing of lamp drivers we already developed very effective profiles. Switch Mode Power Supplies (SMPS) for discharge lamps and for LEDs for almost 98% use the same component base. Also they use the same circuit modules and the same assembly and manufacturing methods. Only minor adaptations to the profiles are needed to test drivers for LEDs effectively. More challenging it is to test LED modules and complete LED systems. In this chapter, we present briefly HALT and MEOST test results for three different LED modules and three different LED systems. The focus is on the stressors and the stress levels we use in the tests, and to evaluate and where possible to conclude how HALT and MEOST can be used in the most optimal way. However before doing so, the next paragraph briefly explains the differences between the quantitative Accelerated Lifetime Testing and the qualitative HALT.

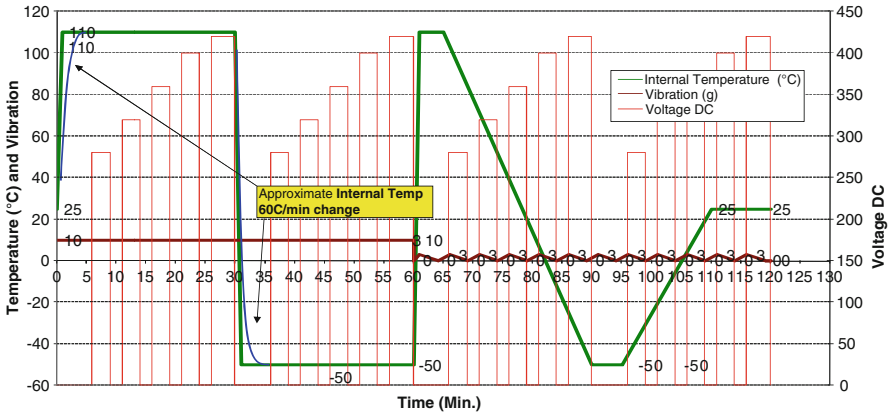


Fig. 7.2 Example of simple stress profiles in an MEOST experiment (thermal, vibration, and voltage input stress on *Y*-axis, time in minutes on *X*-axis). For effective MEOST testing additional realistic and application-specific stress and load variations should be added. The graphical profile presents a 2-h testing. For a full MEOST this profile is repeated for 2 days

7.2 Enthusiasm and Skepticism Concerning HALT and MEOST Testing

Although many specialists in the field of reliability are very enthusiast when it comes to HALT and MEOST, many managers and also project leaders still are skeptical. The most important reason for this is in the naming of HALT. The naming of HALT pretends that the full lifetime of a product can be accelerated to a very short period. The implication is then that by applying the appropriate acceleration factors, the lifetime of the product can be predicted. The advantages of doing so are substantial. However when managers are confronted with the disappointment that again when the product has to be released to the market no proper lifetime prediction is possible, the disappointment is even bigger.

Many failure modes in electronics are temperature driven, and the temperature relation of temperature stress and time to failure can be described by the Arrhenius equation [7]. In Fig. 7.3, the Arrhenius acceleration lines for failure mechanisms with activation energies 0.6, 0.8, and 1.0 eV are projected in an acceleration plot. When for a specific failure mode the activation energy is exactly known, the application lifetime at any stress can be calculated with the Arrhenius acceleration relation when the accelerated lifetime is determined at only one stress level. For example when in the application the stress is 70°C and the test is done at stress 120°C, then the acceleration factor is 30 for activation energy 0.8 eV.

When the failure mode is known, but not the exact activation energy, then by determination of accelerated tests at two stress levels both the acceleration factors and the activation energy can be determined. It is a strong requirement that the failure mechanism is known. In this example we assumed that the Arrhenius

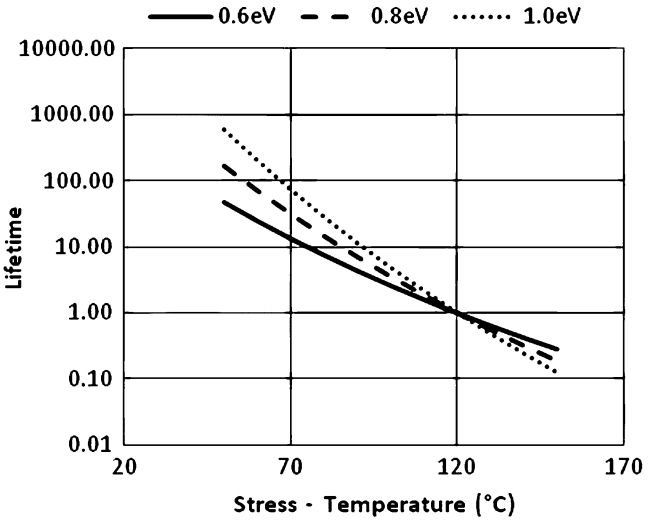


Fig. 7.3 Arrhenius acceleration lines

relation between stress and lifetime, but also power relations or different ones are also common. When the relation between stress and lifetime of the failure mechanism is not known, or when there is interaction between different failure mechanisms, then tests should be done at more than two stress levels. This means the first risk with any acceleration testing is exact knowledge concerning the stress lifetime relation over the total temperature range from application to test. When the failure mechanism is purely temperature driven and an Arrhenius relation can be assumed, then still it should be verified that the activation energy behaves constant over the complete temperature range where it is applied. For all failure mechanisms the condition of a fixed relation is only valid in a certain range. Beyond the maximum stress of this range additional mechanisms come into action, which are always more destructive than within the range. The maximum stress level within a boundary level where a much stronger mechanism comes into action is called the technology limit.

As LED drivers and systems are built of electronic components, it is important to know the technology limits of the used components, modules, subassemblies, products, and systems. In this hierarchy from component to system level, it seems inevitable that the technology limit is highest at the lowest level, so at the component level, while at the system level the margin between technology limit and use condition is smallest. Some data from practical-use components, products, and systems are presented in Table 7.1. The difference between a product and a system is a relative one, and depends on the level from which you are looking at it.

The increase of the destruction rate beyond the technology limit of, e.g., 120°C is shown in Fig. 7.4. When testing is done above the technology limit of 120°C and the accelerated lifetime test results are used to predict the useful life at 70°C use temperature, the useful life can easily be overrated with a factor 5–10.

Table 7.1 Temperature limits of components, modules, and systems

	Technology limit (°C)	
	Common	Special
Components		
Active semiconductor	150	175
Passive semiconductors	130	150
Power resistors	130	150
Electrolytic capacitors	110	135
Film capacitors	110	130
Subproduct or module		
LED module	90	110
Lamp or module driver	80	95
Reflector/housing	80	90
System		
Integrated LED lamp	80	90
LED fixture	80	90

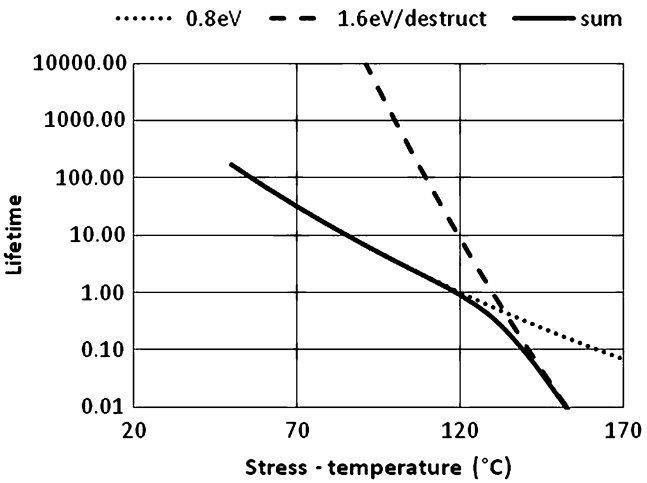


Fig. 7.4 Deviation of the Arrhenius acceleration beyond the technology limit

Figure 7.5 indicates ALT, HALT, and MEOST in the Arrhenius acceleration plot. With HALT testing of electronic products regimes are entered where the failure mechanisms are not simple Arrhenius or power relations anymore. Also products or systems have many more possible interactions between stress factors. At higher temperatures new failure modes can occur which are not present at lower temperature. One example is magnetic saturation of inductors which could occur above 110°C. In electronic drivers this can result in catastrophic peak currents in active components. A second example is very fast degradation of film capacitors above 130°C, due to shrinkage of capacitor foil material. Another cause for an

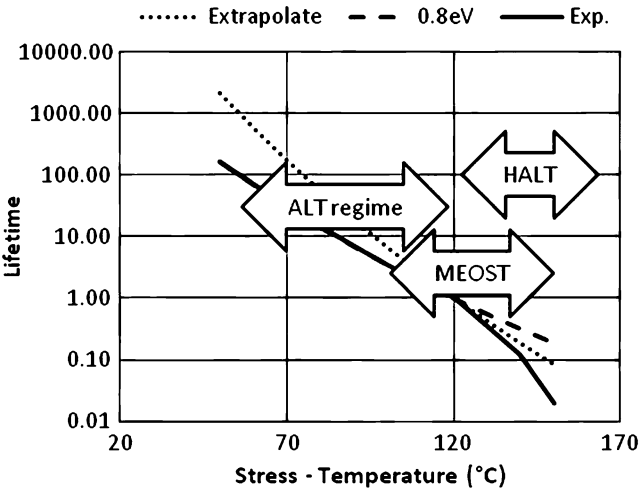


Fig. 7.5 ALT, HALT, and MEOST testing regimes

excessive increase of failure rate is when multiple stressors are acting simultaneously. For example thermal cycling stress combined with vibration stress can have a much higher destructive impact on mechanical connections then each of the single stressors alone.

The difference between ALT and HALT testing lies in the fact that with ALT testing lifetime predictions are possible, while for HALT this is not possible. ALT testing takes long periods, ranging from 6 up to sometimes 48 weeks, while HALT testing typically is done in 1 week. The main purpose of HALT is to reveal design, component, and process weaknesses in a very short time. Most effective is HALT when the weaknesses can be revealed as close as possible to the normal-use conditions. This is especially the focus of MEOST. When an MEOST profile is derived from the HALT destruct limits and the stress profile is optimized to reproduce real-field failures, then the testing profile can be adopted as a calibrated MEOST profile.

7.3 HALT/MEOST for LED Modules

Testing is done on a series of three different LED modules, denoted as LED module A, B, and C. Loading profiles and results are presented in Tables 7.2, 7.3, and 7.4. Module A is a new composite LED module. Module B is an outdoor module. Module C is a module for an office application. For the discussion of the test results please refer to the next section.

Table 7.2 LED module A

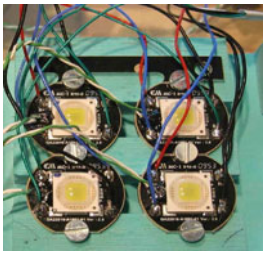
Picture	
Loading profile	HALT Temperature test max 160°C, T-module 195°C MEOST Temperature −50 to 130°C, Grms average 6, Grms peak 15, 44 h
Results	HALT Failure: De-soldering of electrical connections (>230°C!) Grms max 100 No failure Combined test −50 to 150°C and step up to 80 Grms Failure: Loosening of ceramic module from MCPCB MEOST Failure: De-soldering of electrical connections (>230°C!) Failure: Loosening of ceramic module from MC-PCB Failure: LED failures, both red and blue LEDs

Table 7.3 LED module B

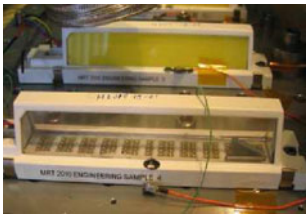
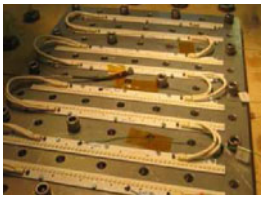
Picture	
Loading profile	HALT Temperature test max 100°C, T-module 150°C Vibration test Combined test −60 to 90°C and step up to 65 Grms
Results	HALT Temperature test: No failure Vibration Failure: Loosening of aluminum part of internal housing construction

Table 7.4 LED module C

Picture	
Loading profile	HALT Temperature test −50 to 200°C, T-module 200°C Vibration test max 50 Grms
Results	HALT Temperature test: No failure Vibration: No failure Combined test: Light flickering starting at 180°C at 30 Grms

7.4 HALT/MEOST for LED Systems

Testing is done on a series of three different LED systems, denoted as LED system D, E, and F. Loading profiles and results are presented in Tables 7.5, 7.6, and 7.7. System D is an indoor system. Module E and F are outdoor systems.

Our test results indicate that high stresses can be applied to LED modules. Well-designed LED modules can be tested far beyond the rated specification limit of active components of 150°C. Most modules tested withstood vibrations level beyond 50 Grms for the short duration of the HALT. Only the LED construction with the highest thermal load showed thermal and mechanical problems in HALT and MEOST (LED module A).

HALT—driver testing sometimes reveals electrical issues at relatively low temperatures, for example in LED system F. This however is not a typical HALT test result. These failures could also have been revealed in a laboratory test on the workbench. In general for electronic drivers which are robust designed HALT—failures start to occur above typical 130°C. Above this temperature film capacitors start to degrade rapidly and normally used magnetic cores of the inductors saturate. For commercial Switch Mode Power Supplies 120–130°C component temperature is the technology limit. Also mechanical weak solder joints, weak component constructions, or weak interconnections can be revealed in MEOST testing in the temperature range below 120°C.

Comparing the modules to the systems, it is clear that at system level additional failures at relatively lower stress levels can occur due to:

– Temperature ratings of materials used (plastics with low melting temperature)
– Weak interconnections, for example the plastic front glass of system A

Table 7.5 LED system D

Picture	
Loading profile	HALT Temperature test max 190°C, T-module 200°C Grms max 50 Combined test −50 to 150°C and step up to 80 Grms
Results	HALT Temperature test: Melting of transparent plastic front cover Vibration: No failure Combined test: No failure

Table 7.6 LED system E

Picture	
Loading profile	HALT Temperature test max 140°C Vibration test max 50 Grms MEOST Temperature −30 to 100°C, Grms max 20, 30 Grms, 44 h
Results	HALT Temperature test Failure: Melting of transparent front covers Failure: Driver A failure, melting of Asphalt potting, and critical component failure (T-component > technology limit) Vibration: No failure MEOST Temperature test Failure: Detachment of plastic front covers (<1 h) Failure: Multiple solder cracks in driver B

Table 7.7 LED system F

Picture	
Loading profile	HALT Temperature limits of test −50 to 170°C Grms max 50
Results	HALT Temperature test Failure: 80°C/under-voltage and voltage transitions No failure for nominal voltages up to 170°C Vibration Failure: Color Cove at 20 Grms—fracture of lead of electrolytic capacitor Combined test: No failure

For most of the failure modes which have been found it is debatable if they would become significant causes for failures in the field. First because in the field stresses are much lower while as already explained it is not possible to predict this from the test results. A number of failures are (far) beyond the technology limit.

However for some other failure modes, it can be shown that the failure mode was caused by a deviation of the derating rules or design rules for the component or the construction. In most cases these deviations can be solved easily and without additional cost, at least when the issue is found early in the project. A condition for effective HALT and MEOST testing is that the execution is done early in the project, as soon as first representative samples are available.

7.5 Conclusions and Recommendations

Based on our 6 years' experience in HALT testing to improve the reliability of electronic drivers, we have investigated the applicability of our approach to LED systems. We have presented a series of HALT and MEOST test results and conclude the following:

- HALT and MEOST are valuable additional reliability testing tools to reveal potential design weaknesses of LED modules, drivers, and systems.
- HALT and MEOST focus mostly on electrical, thermal, and mechanical stresses.

- Testing at system level will reveal first issues at system level which will occur typically at lower stress than testing at module level. This could mask potential issues at module level.
- HALT and MEOST do generally not include stresses as humidity, electrostatic (ESD), chemical, UV, or additional less common stresses.
- From HALT and MEOST test results lifetime of LED modules, drivers, or systems cannot be predicted.

Based on the result, we will continue to explore HALT and MEOST techniques for Solid-State Lighting applications.

Acknowledgments With thanks to contributions, support, and fruitful discussions: Toine Bazelmans, Reliability engineer; Paul van Bakel, Reliability expert; and Bert Vereecken, Quality engineer (all Royal Philips Electronics).

References

1. Hobbs G. Accelerated reliability engineering. ISBN 0-615-12833-5
2. McLean HW. HALT, HASS & HASA explained, accelerated reliability techniques, revised edition. ASQ. ISBN 978-0-87389-766-2
3. Institute of Environmental Sciences and Technology. Management & technical guidelines for the ESS process. IEST-RP-PR001.1, published
4. Dodson B, Schwab H (2006) Accelerated testing: a Practitioners guide to accelerated and reliability testing. ISBN-13: 978-0768006902
5. Bhote KR. World class reliability, ISBN 0-8144-0792-7
6. Bhote KR, Bhote AK. World class quality, ISBN 0-8144-0427-8
7. Arrhenius equation—IUPAC Goldbook definition

Chapter 8
Reliability Engineering for Driver Electronics in Solid-State Lighting Products

Abhijit Dasgupta, Koustav Sinha, and Jaemi Herzberger

Abstract Solid-state lighting (SSL) products offer very high energy efficiencies (approximately 90%) and the possibility of very long lifetimes (on the order of 20,000–100,000 h; or 10–30 years). A complete SSL product is a complex optoelectronic system consisting of many interacting subsystems. Reliability assurance is therefore a complex task and requires an integrated system-level approach. The current state of the art is that the reliability of the light engines has received far more attention from SSL engineers than the driver electronics. This chapter provides an overview of reliability activities in the context of developing reliable driver electronics for SSL products.

8.1 Introduction and Background

A key aspect of the technological promise and economic feasibility of solid-state lighting (SSL) products is that they offer very high energy efficiencies (approximately 90%) and the possibility of very long lifetimes (on the order of 20,000–100,000 h; or 10–30 years) [1]. They are currently quite expensive compared to other competing lighting technologies such as incandescent lighting and compact fluorescent lighting (CFL) technologies, so the affordability equation is predicated partly on incurring low maintenance cost during the long lifetime, thus requiring the SSL product to be highly reliable.

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A complete SSL luminaire product is a complex optoelectronic system consisting of many interacting subsystems such as:

- LED light engine
- Associated optics (reflectors, lenses, etc.)
- Driver electronics
- Thermal management system
- Interconnections and wiring
- Outer case, seals, and system packaging

Reliability assurance is therefore a complex task and requires an integrated system-level approach. Much research has been devoted to identifying the dominant failure mechanisms in the SSL light engine itself, which is composed of LED semiconductor devices and associated packaging and optics. Other chapters in this book are devoted to this topic. The performance of these light engines is usually specified in terms of lumens output and color quality. The ability to sustain it is critical to functionality and hence to reliability. Lifetimes are therefore defined in terms of specified thresholds for lumens depreciation and color shifts.

SSL product designers recognize that one of the key differentiators compared to conventional incandescent lighting products is that the lamp now contains significant amounts of integrated driver electronics, such as power supplies, ballast, dimmers, and smart color controls. Some competing technologies, such as compact fluorescent lamps (CFL), also contain some amount of integrated electronics, but they are typically far less complex than in modern SSL systems and their lifetime expectations are typically far less demanding than in SSL systems.

The current state of the art is that the reliability of the light engines has received far more attention from SSL engineers than the driver electronics, which is typically either a commercial-grade bought-out subsystem or built and assembled from commercial-grade parts. There is significant concern therefore that the driver electronics reliability may not be comparable to that of the light engine and may not be able to meet the very aggressive lifetime targets that have been set for SSL products. The complexity of the driver electronics in modern SSL luminaire systems makes reliability assurance for 10–30 years a difficult challenge, especially in harsh-use conditions such as outdoor lighting environments, automotive headlamps, etc. Therefore, this chapter focuses on the reliability of the driver electronics. Other chapters in this book address the reliability of other subsystems.

Typical commercial-grade electronic parts and assemblies are qualified for far shorter life cycles (2–5 years is common) than the 10–30-year goals of the SSL industry. Consequently, there are no industry standards available today to qualify the driver electronics for SSL applications. The empirical reliability models and accelerated testing models used in commercial reliability standards such as Telcordia specs have seldom been validated for such long-field applications and also result in qualification tests that are too long to allow reasonable product development cycles. The SSL industry realizes that nontraditional solutions are needed based on a proactive, rigorous, and scientific approach. The problem is too vast for individual companies to solve and requires a pan-industry effort across the

entire supply chain. Agencies, such as the Department of Energy in the USA, have only recently initiated such multi-industry efforts to address these reliability concerns.

A systematic Physics of Failure (PoF) approach offers a promising framework for addressing this challenge and is being effectively used in other industry segments that face similar reliability challenges, including military and aerospace systems that use COTS technologies, automobile and rail transportation, medical and health-care systems, telecommunication base stations, information networks, transportation infrastructure (e.g., signaling systems in urban commuting networks), and distributed energy platforms (e.g., small or large solar units or wind turbines that are expensive to access and maintain). This chapter discusses the fundamentals of the PoF approach as it applies to the development and reliability assurance of SSL driver electronics. The application of the PoF approach to electronic products is founded on the conviction that the failure of electronics is governed by fundamental mechanical, electrical, thermal, and chemical processes. For this reason, potential problems in new and existing technologies can be identified and solved before they occur, by understanding the possible dominant failure mechanisms. The PoF approach includes the following critical-to-reliability (CTR) activities:

- Understanding the life cycle loading histories.
- Understanding the hardware architecture and its vulnerabilities to life-cycle loads.
- Setting reliability goals for the system and associated subsystems. This may include benchmarking analysis against competing products.
- Planning and performing engineering activities around product design and manufacturing to meet those goals. This may include:
  - Overall concept and architecture design of the hardware/software.
  - Preliminary failure modes, mechanisms, and effects analyses (FMMEA) to assess the design and process and to identify the potential dominant failure modes.
  - Detailed part design using a combination of PoF simulation (virtual qualification) and testing, to address the expected dominant failure modes. PoF simulations are based on detailed failure models.
  - Detailed planning of the optimal manufacturing process to minimize potential variabilities and defects.
  - Assessment of the variabilities and uncertainties in the model inputs for the failure models.
- Managing the supply chain to ensure that they meet the reliability goals of bought-out and subcontracted subsystems/parts.
- Verifying that reliability goals can be met by nominal products.
- Sustaining reliable product performance throughout the life cycle. This includes:
  - Continuous monitoring of quality (quality is defined here as variability in CTR parameters across a sample lot, and hence, variability in lifetime expectation for that lot).
  - Product support, real-time condition monitoring, and health management.

- Ongoing corrective actions to minimize manufacturing anomalies across the supply chain.
- Ongoing activities to assess the impact of continuous cost-reduction efforts.

This chapter provides an overview of each of these reliability activities listed above, specifically in the context of developing reliable driver electronics for SSL systems. Section 8.2 discusses typical life-cycle environments for SSL products; Sect. 8.3 addresses typical architecture for driver electronics hardware; Sect. 8.4 discusses methods for specifying reliability goals; Sect. 8.5 discusses the dominant failure mechanisms in SSL driver electronics; Sect. 8.6 discusses methodologies for concurrent design of reliable systems; Sect. 8.7 discusses accelerated test methods to verify design margins; Sect. 8.8 discusses methods to audit product quality; Sect. 8.9 discusses ongoing product support technologies such as prognostics and health management to ensure high reliability and high availability; and Sect. 8.10 presents a summary of this chapter.

8.2 Typical Life-Cycle Environments for SSL Products and Driver Electronics

A key activity in reliability assurance is proper quantification of the expected life cycle loading histories that the product must survive. This includes not only details of how the product will be used, but also the "stress" conditions that the product will experience during all phases of product life cycle, including the manufacturing process itself, testing (e.g., stress screens), rework and repair, handling and assembly, packaging and transportation, distribution and storage, deployment/installation, and field repairs. Sometimes it is useful to segregate the life cycle stresses into two different groups: those experienced by the product prior to sale vs. those experienced after sale. The reason is that presale failures are often treated as yield issues while post-sale failures are addressed under warranty policies and carry a much stiffer cost penalty.

The term "stress" is used in this section as a generic term to indicate the effect of all external (environmental) and internal (operational) influences that can cause degradation of the product over its life cycle, e.g., mechanical, thermal, electrical, or chemical degradation. These stresses must be quantified, not only for effective design but also for designing a meaningful reliability test program. Some common sources of life cycle stresses are operational electrical stresses and power dissipation (and on–off cycling), ambient temperature (and cycling), ambient humidity (and cycling), accidental drop of portable products into water, chemical spills, contamination (sand, dust, or chemicals), accidental drop or shock, vibration, button actuation, mechanical handling of portable products, pressure due to changes in altitude, electromagnetic radiation from surrounding equipment, exposure to solar radiation (UV), high-energy cosmic particles during high-altitude applications, etc. Excessive exposure to stresses of these types may have some deleterious effect on

the performance of the product either due to catastrophic overstress failure mechanisms and/or due to wearout (cumulative) degradation mechanisms. For example, high temperature can cause one or more of the following problems:

- Circuit malfunctions by letting electrical parameters like resistance, inductance, etc. vary beyond design tolerances
- Mechanical stresses due to thermal expansion mismatches
- Surface degradation rates due to catalysis of chemical reactions and diffusion of harsh chemicals
- Issues for optical components due to outgassing and subsequent deposition of volatile compounds

The various sources for environmental information include historical data collected from field/customer. Some industry standards (e.g., standards from IPC, ASTM, ISO, ISTA, ETS, IEC, Mil-Hdbk, etc.) offer generic guidelines about different classes of usage stresses, but these are often nonspecific and it is more cost-effective in the long run to obtain more realistic data directly for different usage categories. SSL products are ideally designed to survive in different environments all around the globe both indoors and outdoors, depending on the product type. Outdoor products include street lighting, decorative lighting on building exteriors, and transportation lighting (e.g., cars, trains, ships, airplanes, etc.). The outdoor conditions of course show strong geographic variations and it is important to understand the extremes and ranges which SSL products have to withstand without functional or cosmetic failures. As examples, three different geographic locations are discussed here to provide a good understanding of the diversity of conditions that SSL products must survive (http://www.weatherbase.com, 2011 [2]; http://www.wunderground.com, 2011 [3]).

The first example, Singapore, is a typical tropical region with high but relatively stable temperature, and high humidity that does not change much over the year. The second example is from a hot, dry region (Dubai) but with strong diurnal and seasonal variations in the temperature. So, we can expect failures in Dubai to be predominantly due to mechanisms that are triggered by cyclic loading at high temperatures (e.g., creep–fatigue degradation caused by thermomechanical stresses), while failures in Singapore are likely to be dominated by mechanisms that are triggered by steady temperature and moisture (e.g., corrosion). The third example is from a cold region (Nuuk, Greenland) which has a drastically lower mean temperature and humidity compared to Dubai but experiences large cyclic variations. Thus, failures in Nuuk may have a greater contribution from cyclic stresses in viscoplastic materials (like polymers), which behave in a brittle manner at low temperatures.

Figure 8.1 is a comparison of the average temperatures and average morning humidity, for the year 2010. These typical average values are important for cumulative damage estimates. On the other hand, freak extremes are important for assessing the risks of overstress failures. For example, the global outdoor extreme temperatures range from −30°C at the cold end to 50°C at the hot end.

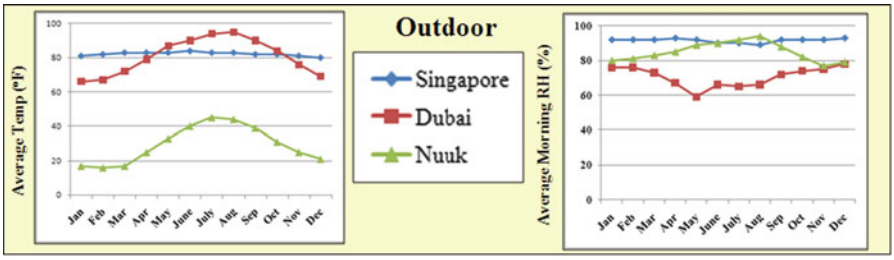


Fig. 8.1 Outdoor temperature and humidity variation for the year 2010

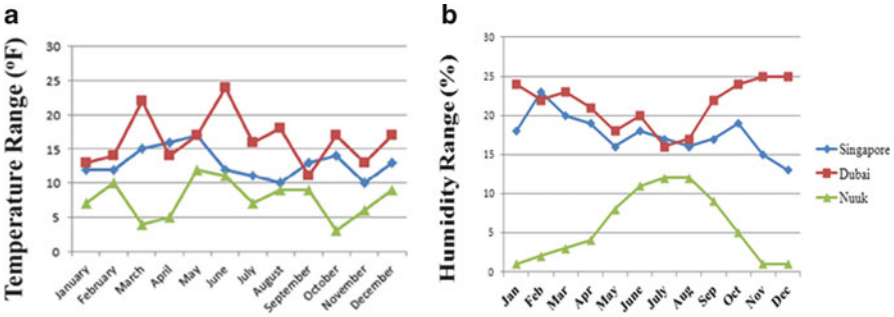


Fig. 8.2 Typical cyclic range of outdoor (**a**) temperature; (**b**) humidity

Average relative humidity is generally high outdoors with occasional precipitation increasing the chances of moisture ingress into outdoor SSL products.

Figure 8.2a, b shows that the cyclic variation of temperature ranges from 3 to 24°F while cyclic variation in humidity ranges from 1 to 25%. Colder regions have smaller ranges of temperature and humidity than their hotter counterparts.

Two-point correlation functions are sometimes used to quantify stresses when multiple stress types act in conjunction. For example, variable temperature histories can be expressed with correlated combinations of the cyclic mean and cyclic range, via cycle counting techniques. One way to represent such two-point distributions is with a box-plot, as shown in Fig. 8.3a. Another example of two-point correlation is between temperature and moisture, for corrosion mechanism, as shown with two-parameter histograms in Fig. 8.3b.

Indoor conditions are significantly more complex and difficult to predict. Temperature and humidity also vary with building material and internal sources of heat and moisture. In richer countries, most commercial buildings and residential buildings use central heating and air-conditioning. So, irrespective of the outdoor conditions, the temperature and humidity are maintained at a more or less constant benign level throughout the year. On the other hand, in less affluent nations, fewer commercial buildings and very few residential buildings can afford controlled

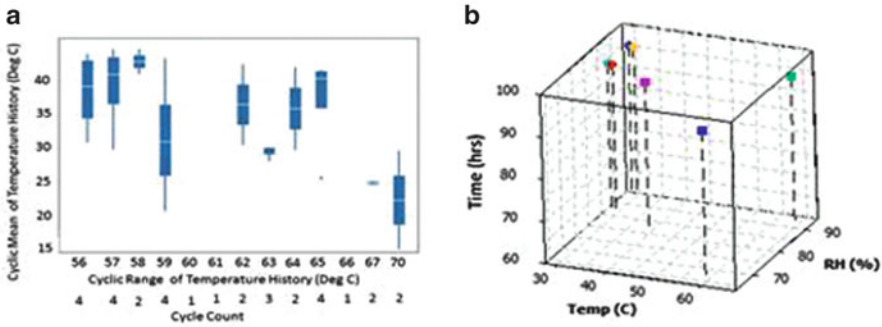


Fig. 8.3 (**a**) Box plot of typical temperature history; (**b**) two-parameter histogram for typical temperature–humidity combination

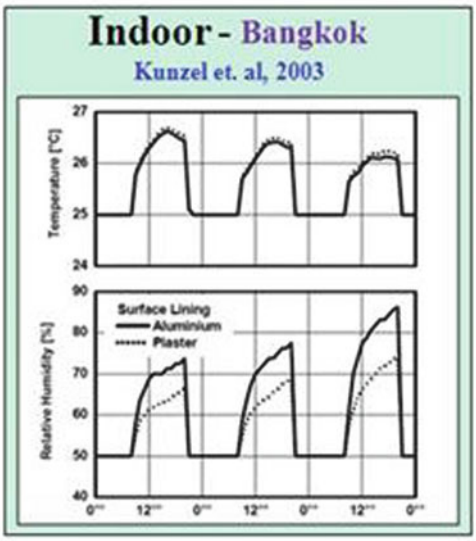


Fig. 8.4 Hourly variations in indoor environments

environments and indoor conditions may track to some extent the outdoor trends. There have been a few attempts to develop models that can take into account these various parameters. Künzel et al. [4] got a good match between model predictions and the measured indoor temperatures, as shown in Fig. 8.4.

In addition, there may be mechanical vibration loads for some applications such as LED automotive headlamps and drop/shock loads for portable applications such as LED flashlights. Random vibration environments can be characterized either in the time domain with range distribution functions obtained with cycle counting techniques, as shown in Fig. 8.5a, or in the frequency domain with power spectral

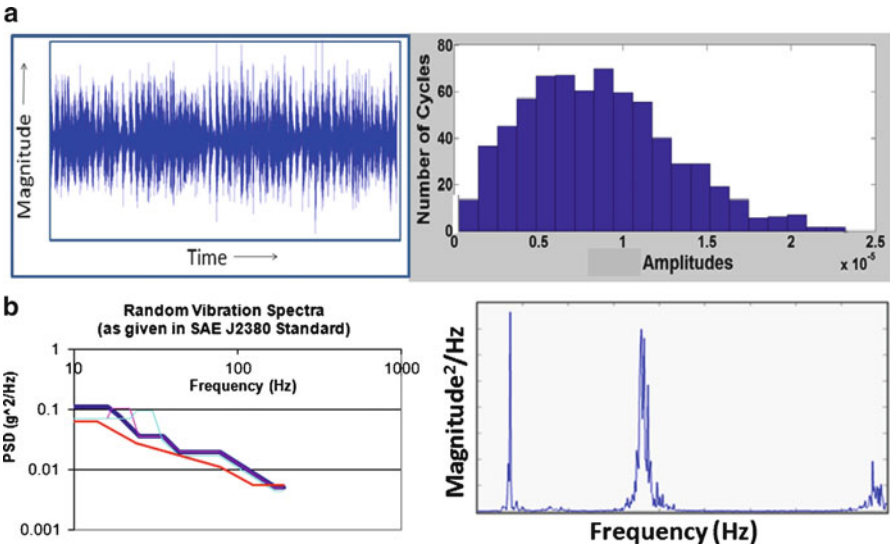


Fig. 8.5 (**a**) Range distribution function (RDF) obtained from time history via cycle counting. (**b**) Power spectral density (PSD) obtained in frequency domain from time history via fast Fourier transform (FFT). Figure on *left* shows a typical excitation PSD as per an SAE standard, while figure on *right* is typical response PSD

density (PSD) distributions, as shown in Fig. 8.5b. Either approach can be used to conduct fatigue durability assessments in order to characterize the reliability under random vibration environments. Figure 8.5b shows a typical input PSD, specified in SAE standards for vibration testing for automotive applications, and a typical response PSD which clearly shows that the test specimen has some dominant resonant frequencies.

Shock/drop environments are often quantified with shock response spectra (SRS), as shown schematically in Fig. 8.6. The SRS plot indicates the severity of the shock, in terms of the response of a hypothetical series of single degree-of-freedom (SDOF) oscillators. The x axis of the SRS plot indicates the natural frequency of these idealized SDOF oscillators. Thus it is a plot of response amplitude of a series of reference SDOF systems vs. the natural frequency of each such SDOF system.

The local environment for the driver electronics depends on the environmental histories discussed above, the usage duty cycle which governs the power cycling parameters, and the luminaire enclosure design which includes thermal management (heat dissipation mechanisms), moisture protection seals (especially for outdoor products), mechanical isolation, and EMI protection. The usage duty cycle can vary significantly depending on the product type, e.g., an indoor replacement LED bulb may have a very different duty cycle than an outdoor LED street lamp.

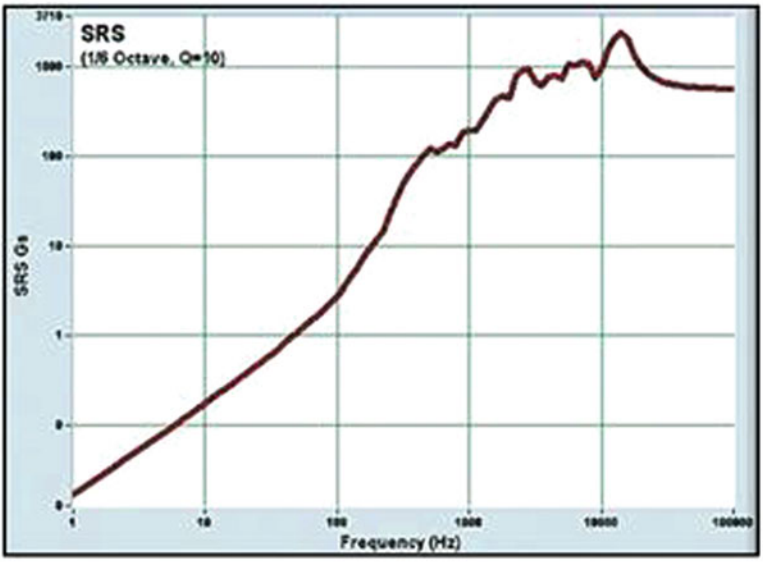


Fig. 8.6 Shock response spectrum (SRS)

8.3 Typical Architectures and Topologies for SSL Driver Electronics

The SSL industry uses a semiconductor-based light engine and complex lighting controls, and has therefore changed from an electrical to electronics-based industry. Unlike fluorescent lighting with simple ballast control, SSL is a power electronics system with more versatile capabilities. Additional circuitry is needed to make the LED light engine useful. As a result, SSL product manufacturers have to also consider the LED electronic driver module. The basic electrical circuit for incandescent and fluorescent light sources has to be replaced with sophisticated solid-state electronic lighting fixtures. The primary function of the driver module is to supply a stable power level over the entire temperature range for the LED in order to maintain a consistent light output. The driver has to convert standard AC input into a controlled DC current or voltage. Since the driver's power dissipation reduces the overall efficiency of the SSL system, drivers must be designed for low power consumption, for the most efficient lighting. The capabilities provided by a typical LED driver module include protection features such as temperature protection, current detection, and power factor correction. The driver also performs several system-level functions, such as interfacing with the AC input line or 0–10 VDC dimmers, as well as other emerging smart controls, such as daylight harvesting, ambient light sensing, and occupancy detection for tailoring the lighting to the needs.

LED driver modules must be designed to balance competing requirements such as efficiency and life expectancy. While there are several off-the-shelf driver modules available to address some of the design requirements, SSL system manufacturers often need customized design solutions to satisfactorily address all of these concerns at the system level. This includes matching the driver module with the interface requirements of the LED module and providing the appropriate thermal management, temperature protection, and electrical surge protection.

The driver module must also be compact enough to be easily integrated into an SSL system, to simplify the entire lighting design process. As in most electronic power systems design, smaller form factors and higher power density are part of the ongoing improvements.

8.4 Typical Reliability Expectations of "Long-Life" Driver Electronics

A system is said to be reliable when there is adequate confidence level that it will perform within specified limits, for a specified period of time, under specified life-cycle conditions. The typical approach for quantifying or specifying reliability consists of specifying confidence bounds on a chosen reliability metric. There are several such metrics that can be used to express how reliable a system is. For a complex SSL system with many subsystems, the reliability goals must be then suitably allocated/distributed among subsystems so that the overall system reliability budget can be met.

Some of the commonly used reliability metrics are:

- Expected time to failure:
  - Mean time to failure (MTTF): MTTF for a selected failure distribution.
  - Failure-free operating period (FFOP): FFOP (typically expressed by the location parameter, γ, when the failure distribution is expressed by a three-parameter Weibull distribution).
  - Maintenance-free operating period (MFOP): MFOP, which is the FFOP for repairable systems.
- Expected cumulative amount of failures over a specified period of time: Defective parts per million (DPPM) units over n years. For a statistically large sample size, this metric can be normalized to provide an estimate of the failure probability ($F(n)$) at the end of n years. This metric is also the value of the cumulative distribution function (CDF) of the failure distribution at the end of n years.
- Probability $R(n)$ that a given unit will survive up to the specified time, n years. For a statistically large sample size, this metric and $F(n)$ (normalized Metric 3 above) add up to unity. In other words, $R(n) = 1 - F(n)$.

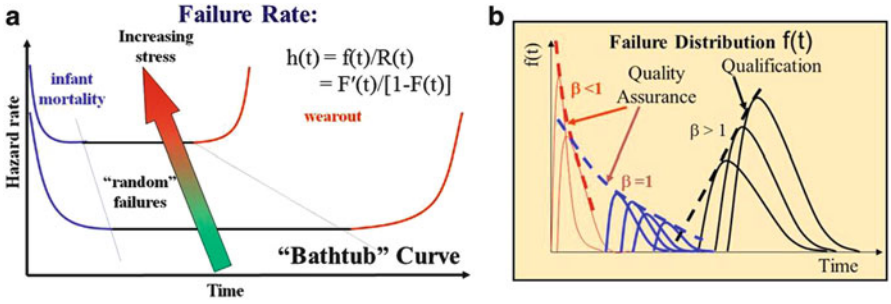


Fig. 8.7 (**a**) Traditional system-level view of the bathtub curve showing the three dominant regions ($h(t)$ is hazard rate, $f(t)$ is failure probability density function, $F(t)$ is cumulative failure distribution, $R(t)$ is reliability function); (**b**) failure probability density functions showing multi-modal Physics of Failure (PoF) perspective of the bathtub curve

- Expected failure rates:
  - Hazard rate, $h(t)$: The hazard rate function ($h(t)$) is the instantaneous ratio of the failure probability density function (PDF) ($f(t)$) to the reliability function ($R(t)$), where $f(t)$ is the instantaneous slope of the CDF ($F(t)$).
  - Mean time between failures, MTBF: This metric assumes a constant hazard rate, and is estimated as the reciprocal of the failure rate. This metric is appropriate only for random failure events that can be expressed by an exponential failure distribution.

The life cycle of a product is often visualized by reliability statisticians in terms of three failure distributions, shown schematically in Fig. 8.7. The graph to the left shows the hazard rate of a product-family, as a function of time in service. The distribution in red, with increasing hazard rate (Weibull distribution with shape factor $\beta > 1$), signifies the expected end-of-life failures of the in-service products. This phase is often termed the "wearout" phase by reliability statisticians. The other two distributions (in blue and black) indicate premature field failures due to gross or minor manufacturing variabilities, and due to accidental, unexpected abuse. The failures early in the life cycle (in blue) typically show a decreasing hazard rate, and is termed the "infant mortality" phase by reliability statisticians (hyperexponential function with Weibull $\beta < 1$). The midlife mortality data (in black) is typically represented at the system level with a constant hazard rate (implying an exponential failure distribution with Weibull $\beta = 1$) and is termed the "random failure" phase by reliability statisticians.

This plot is usually termed the "Bathtub" curve because of its shape and is constructed by collecting all failures in the system into a single data set without regard to the root cause failure mechanisms. Reliability statisticians usually attempt to use field data to quantify these distributions. Of particular interest to the reliability statistician is the expected value of the constant hazard rate during the

"random failure" phase (and its reciprocal, the MTBF), since this is considered to characterize the intrinsic reliability of the product under typical usage. However, this information is of very limited value to the PoF reliability engineer who has to understand the root cause and improve the reliability by reengineering the next-generation product. Also useful is the beginning of the "wearout" phase since this indicates the useful life of the product. The "infant mortality" phase is important for quantifying warrant risks and for understanding gross quality problems.

In the figure on the right, we see the PoF view of this same information. In other words, the failure data is now divided into multiple subpopulations, when the data is segregated by failure mechanisms. Each subpopulation is now shown with a separate PSD (in green), scaled by the size of the subpopulation. This schematic figure is intended to convey the message that many of the premature failures may be due to wearout mechanisms, although at the system level the combination of all the failures may show a decreasing or constant hazard rate. The premature failures are usually due to quality issues. In other words, these are defective subpopulations that contain manufacturing defects/variabilities. Improving the design margins can sometimes improve the quality by increasing the margin of tolerance for manufacturing variabilities. The failure mechanism has to be carefully understood for each premature failure subpopulation, using PoF methods, so that they can be carefully minimized or eliminated.

8.5 The PoF View of Reliability Challenges in Long-Life SSL Driver Electronics

The task of PoF reliability engineers here is to understand the dominant failure mechanisms in SSL driver electronics and to use a science-based, holistic reliability approach to appropriately ruggedize the product. This requires careful teaming with the design engineers, process development and manufacturing engineers, supply chain and procurement engineers, and field-support engineers. The intent of the PoF approach is to be proactive about influencing the design and manufacturing process, to build right the first time, and to minimize reactive (and expensive) Build-Test-Fix iterations. Reliability engineering is a holistic product development function—not just a testing function. It is well understood that it is not possible to "test reliability into a product"; testing can only provide a final verification and confirmation of a robust design/process. Excessive reliance on system-level testing as a reliability tool is very expensive and an untenable strategy when developing very-long-life products like SSL systems, because the time-to-market pressures do not allow sufficient time for extensive empirical verification of product life. Furthermore, design improvements cannot be implemented in a timely or cost-effective manner. The challenge for the PoF engineer is to divide the complex product into individual subsystems and failure sites so that the system reliability challenge

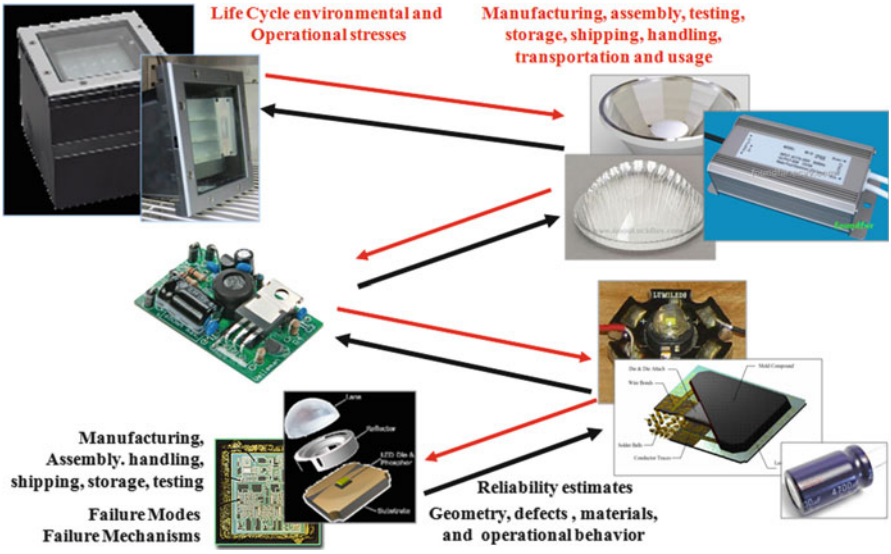


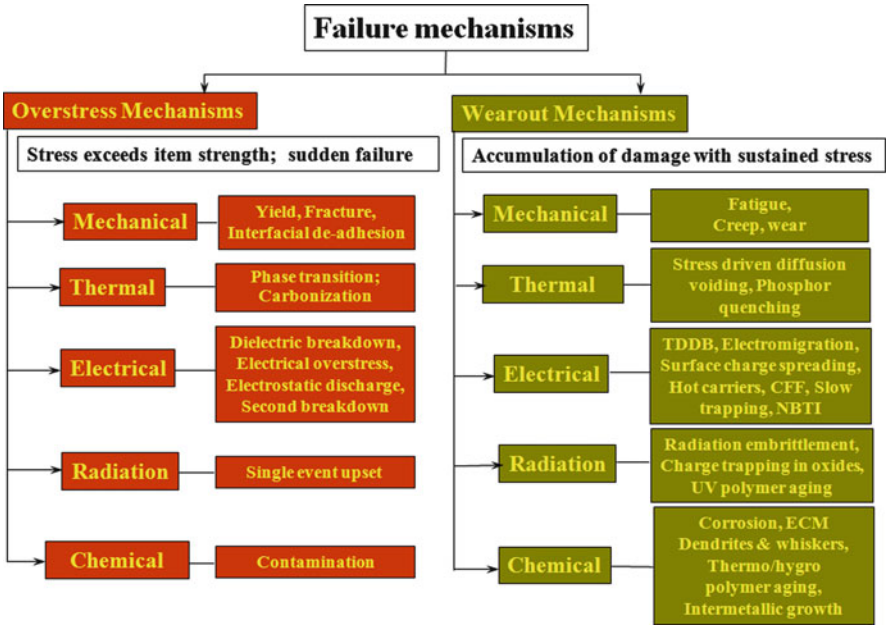
Fig. 8.8 Supply chain for complex SSL product: quality and reliability attributes flow up the chain, life cycle stress profile information flows down the chain

can be de-convolved into a smaller set of subproblems and can be tackled with a divide-and-conquer strategy.

One of the key problems for the SSL reliability engineer is that much of the driver electronics may consist of commercial off-the-shelf (COTS) parts and outsourced subsystems, and contract manufacturing, all of which have important influences on the reliability of the end product. Assuring reliability in such a complex reliability ecosystem requires a very symbiotic relationship with the supply chain, as shown schematically in Fig. 8.8. The reliability team therefore needs to gain skills in collaborating with Tier 1 and Tier 2 suppliers to manage product reliability. The supply chain needs to provide sufficient engineering information needed to quantify the reliability expectation of their supplies. Conversely, the SSL OEMs need to inform the supply chain about the life cycle stress scenarios of the final product and provide them the reliability budget or allocation for their subsystem. Life cycle stress specifications will have to be tailored to each level in this supply chain since (1) the product construction and transmissibilities will attenuate or amplify how the product stresses are transmitted to the electronics enclosure and to internal subsystems and components and (2) low-level components and subsystems in the assembly sequence will see more of the upstream manufacturing process stresses.

The purpose of this section is to describe the methodologies and approaches used in PoF-based reliability programs for SSL products. The remainder of this section discusses dominant failure mechanisms in SSL driver electronics and also discusses how to connect life-cycle stress profiles to the various reliability modeling and

Table 8.1 Dominant overstress and wearout failure mechanisms in SSL systems



testing activities. Details of these PoF processes can be obtained in industry standards such as:

- IEEE-1332 (Standard Reliability Program for the Development and Production of Electronic Systems and Equipment)
- IEEE-1413 (Standard Framework for Reliability Prediction of Hardware) for further guidance
- IEEE-1624 (Standard for Organizational Reliability Capability)

There are many failure mechanisms that are relevant to material systems used in complex systems like SSL products and their electronic driver modules. Table 8.1 provides a listing of the dominant mechanisms, divided into two groups: overstress mechanisms and wearout mechanisms. Overstress mechanisms cause instantaneous catastrophic failure whenever there is a stress exposure that is severe enough to exceed the "strength" of the material. The terms stress and strength are being used in a generic sense for mechanical, thermal, electrical, or chemical types of loads. Wearout mechanisms, on the other hand, cause progressive damage accumulation under lower (but sustained) levels of steady or cyclic stress histories. Ultimate failure occurs when the cumulative damage level exceeds some relevant damage-tolerance capability of the material.

Within each category, the failure mechanisms are further sub-grouped by the dominant type of stress that triggers these mechanisms. For example, mechanical

stresses cause overstress fracture and wearout cyclic fatigue. In many cases, the mechanism is driven by multiple stress types; e.g., temperature, moisture, and ionic chemical contaminants together drive corrosion. In such cases, the mechanism is listed under one of the dominant stress drivers. In addition, sometimes there are interactions between failure mechanisms, such as stress corrosion cracking which is a combination of corrosion and fatigue. Similarly, fretting corrosion is a combination of mechanical wear and corrosion. Furthermore there is also an interaction between wearout and overstress mechanisms, viz. accumulation of wearout damage can lower the ability of a material to withstand overstress events.

The next few subsections provide some examples of failure mechanisms that dominate in passive and active electronic components used in the driver electronics. The failure modes in LED devices are not discussed here since they have been covered elsewhere in this book.

8.5.1 Failure Mechanisms in Passive Components

Passive components such as resistors, capacitors, inductors, transducers, switches, relays, connectors, fuses, and so on outnumber semiconductor devices in most electronic assemblies, and are significant contributors to unreliability. Capacitors (especially electrolytic capacitors) are extensively used in SSL driver electronics and are a known reliability challenge for the long 20,000–50,000 life expectation in SSL products. The failure modes of the main types of passive components are discussed in this section.

8.5.1.1 Resistors

Since a resistor is a dissipative element, the general failure mode for most types of resistor is open circuit. This is not always the case for power wirewound resistors, where an overheating condition can cause the material inside to fuse across adjacent turns of the resistor. As in all components, resistor failures are due to material degradation and can be exacerbated by design errors, incorrect usage, or manufacturing defects. Typical resistor failures can be due to:

- Manufacturing defects such as non-homogeneities of the film composition
- Design or usage errors that cause excessive current flow and parasitic inductance or capacitance at high frequencies
- Excessive thermal and electrical noise
- Environmental and operational stresses such as excessive heat and humidity

The source of resistor failures is generally due to outside environmental factors such as handling damage or external stress. High vibration or shock can also degrade the interface for large mass resistors. Failures seldom occur due to a failure

of the resistive element itself. The only exception to this rule is the thin film resistor styles that are susceptible to electrostatic discharge (ESD) damage.

8.5.1.2 Capacitors

Capacitors are a common circuit element in all electrical and electronic applications, including in SSL drivers. Electrolytic and multilayered ceramic capacitors (MLCCs) are commonly used and both are known sources of manufacturing defects and reliability issues. The following list is a summary of the most common environmental "critical factors" with respect to capacitors. The design engineer must take into consideration his/her own applications and the effects caused by combinations of various environmental factors.

Service life. The service life of a capacitor must be taken into consideration. The service life decreases as the temperature increases.

Capacitance. Capacitance will vary up and down with temperature depending upon the dielectric. This is caused by a change in the dielectric constant and an expansion or shrinking of the dielectric material/electrodes itself. Changes in capacitance can be the result of excessive clamping pressures on nonrigid enclosures.

Insulation resistance. As the temperature of a capacitor is increased the insulation resistance decreases. This is due to increased electron activity. Low insulation resistance can also be the result of moisture trapped in the windings, a result of prolonged exposure to excessive humidity, or moisture trapped during the manufacturing process.

Dissipation factor. The dissipation factor is a complex function involved with the "inefficiency" of the capacitor. It may vary either up or down with increased temperature depending upon the dielectric material.

Dielectric strength. The dielectric strength (dielectric withstanding voltage or "stress" voltage) level decreases as the temperature increases. This is due to the chemical activity of the dielectric material which causes a change in the physical or electrical properties of the capacitor.

The construction and failure modes of two different commonly used types of capacitors are discussed in this section: film/foil capacitors and MLCCs.

(a) Paper/plastic film/foil and electrolytic capacitors

These capacitors are subject to several classic failure modes, including opens, shorts, intermittent opens, or high resistance shorts. In addition to these failures, capacitors may fail due to capacitance drift, instability with temperature, high dissipation factor, or low insulation resistance. Failures can be the result of electrical, mechanical, or environmental overstress, "wearout" due to dielectric degradation during operation, or manufacturing defects.

Electrolytic capacitors are used extensively in driver electronics for SSL products. As shown in Fig. 8.9a, the anode and cathode are constructed of aluminum

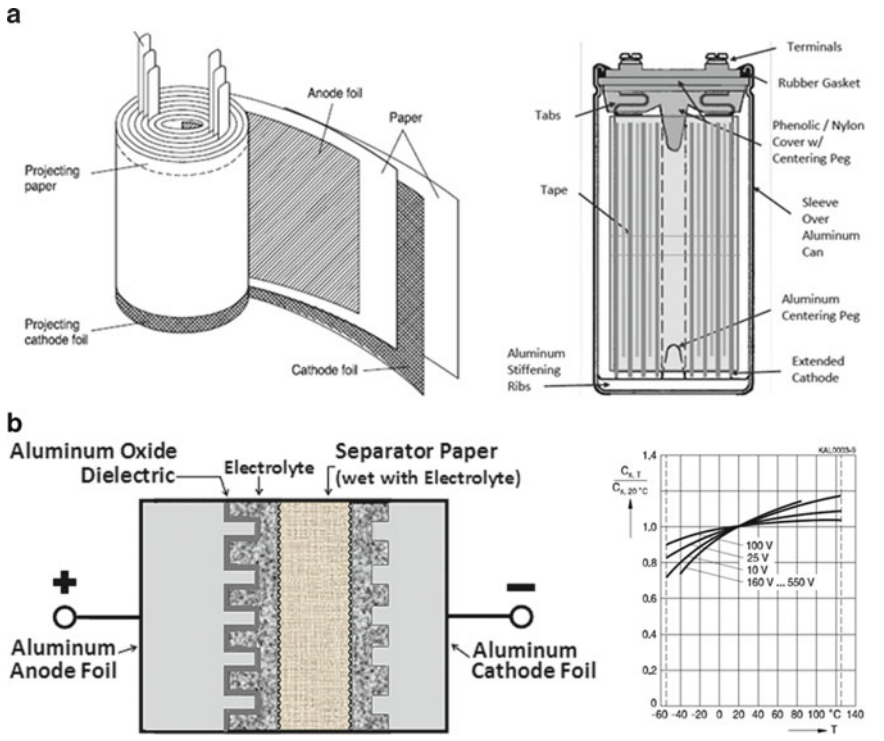


Fig. 8.9 Aluminum electrolytic capacitor: (**a**) schematic of construction. (**b**) Electrode materials and temperature dependence of capacitance

foils (etched to a specified surface roughness, to increase the effective surface area 200–500 times). These foils are separated by a paper dielectric (impregnated with an electrolytic fluid). All three elements are rolled into an aluminum can and sealed with a rubber plug to preserve the electrolyte [5, 48]. Furthermore, as shown in Fig. 8.9b, the capacitance increases as the temperature increases because of a drop in the viscosity of the electrolyte. Electrolytic capacitors have several vulnerabilities to environmental stresses, as discussed below.

Electrolyte evaporation. Over time, the electrolyte slowly evaporates, resulting in a slow increase of the equivalent series resistance (ESR) and a slow decrease of the capacitance [6]. Eventually, the parameters drift out of specification and the capacitor is considered to have failed. For applications with ripple current, the increase of ESR leads to increased internal heating which accelerates the wearout process. The evaporation rate of the electrolyte is one of the life-governing factors for electrolytic capacitors. The corresponding life model is often based on the Arrhenius relation. Thus, equations normally used to extrapolate the rated to operational life values are

$$\frac{L_2}{L_1} = e^{\left[E\left(\frac{T_1 - T_2}{T_2 T_1}\right)\right]}, \tag{8.1}$$

where T_1, T_2 are element temperatures in Kelvin, L_1, L_2 are life at those respective temperatures, and E is the activation energy (normalized by Boltzmann's constant or by the universal gas constant, depending on the units used).

"Short" failure mode (*dielectric breakdown*). The dielectric in the capacitor is subjected to the full potential to which the device is charged and, due to physical sizes of small capacitors, high electrical stresses are common. Dielectric breakdowns may develop after many hours of satisfactory operation. There are numerous causes which could be associated with operational failures. If the device is operating at or below its maximum rated conditions, most dielectric materials gradually deteriorate with time and temperature to the point of eventual failure. Most of the common dielectric materials undergo a slow aging process by which they become brittle and more susceptible to cracking. The higher the temperature, the more the process is accelerated. Chemical or aqueous cleaning may also have an adverse effect on capacitors. Dielectric breakdown may occur as a result of misapplication of high voltage transients (surges). The capacitor may survive many repeated applications of high voltage transients; however, this may cause premature failure.

"Open" failure mode. Opens occur in capacitors usually as a result of overstress in an application. For instance, operation of DC rated capacitors at high AC current levels can cause a localized heating at the end terminations. Continued operation of the capacitor can result in increased end termination resistance, additional heating, and eventual failure. The "open" condition is caused by a separation of the end connection of the capacitor. This condition occurs more often with capacitors of low capacitance and a diameter of <0.25 in. This is why care must be taken when selecting a capacitor for AC applications. Mounting capacitors by the leads in a high vibration environment may also cause an "open" condition. Military specifications require that components weighing more than one-half ounce cannot be mounted only by their leads. The lead wire may fatigue and break at the egress area if a severe resonance is reached. The capacitor body must be fastened into place by use of a clamp or a structural adhesive.

Leakage in seals due to temperature. As the temperature increases, the internal pressure inside the capacitor increases. If the internal pressure becomes great enough, it can cause a breach in the capacitor seal, which can then cause leakage of impregnation fluid or moisture susceptibility.

Leakage in seals due to humidity. The epoxy seals on both epoxy encased and wrap and fill capacitors will withstand short-term exposure to high humidity environments without degradation. These case materials are somewhat porous and through osmosis can cause contaminants to enter the capacitor. The second area of contaminant absorption is the interface between the lead wire and the epoxy seal. Since epoxies cannot bond perfectly to tinned lead wires, there can be a path formed, up the lead wire, into the capacitor section, for contaminant ingress and electrolyte leakage. This can be aggravated by aqueous cleaning of circuit boards.

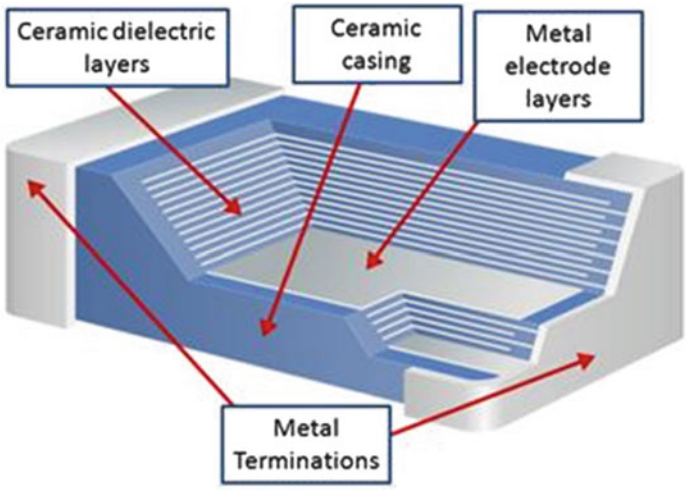


Fig. 8.10 Schematic of multilayer ceramic capacitor [51]

Damage due to barometric pressure. The altitude at which hermetically sealed capacitors are to be operated will control the voltage rating of the capacitor. As the barometric pressure decreases the terminal "arc-over" susceptibility increases. Non-hermetic capacitors can be affected by internal stresses due to pressure changes. This can be in the form of capacitance changes or dielectric arc-overs as well as low IR heat transfer can be also affected by high altitude operation.

Mechanical failures due to vibration, acceleration, and shock. A capacitor can be mechanically destroyed or may malfunction if it is not designed, manufactured, or installed to meet the vibration, shock, or acceleration requirement within a particular application. Movement of the capacitor within the case can cause low IR, shorts, or opens. Fatigue in the leads or mounting brackets can also cause a catastrophic failure.

(b) MLCCs

These are often called "chip capacitors" and come in a wide range of sizes and capacitance values for surface mount applications. They consist of thin metal plates separated by thin ceramic dielectric layers, as shown schematically in Fig. 8.10. The brittle ceramic dielectric makes these components vulnerable to manufacturing microflaws that can result in brittle micro-cracking during the thermal shock experienced in solder reflow processes. Two commonly encountered degradation modes that are often observed are [7] the following:

Punch thru. The presence of defects such as minute air bubbles, thin places in the ceramic layers, or relatively close portions between the internal plate electrodes increases the leakage current which results in self-heating that deteriorates the insulation resistance. If this phenomenon is accelerated under high-temperature

and high-voltage conditions, excess energy accumulates at a particular region. Finally the stored energy abruptly dissipates as destructive energy. This phenomenon is called *punch thru*.

Silver migration. Silver is often used in the metal terminations and electrodes. Silver migration is a failure mode caused when silver moves by electrochemical action from its initial location to some other location on the surface of the insulating material (ceramic). This is caused by the presence of water on the insulating surface and electrical potential and can cause electrical shorts.

8.5.2 Failure Mechanisms in Active Devices

The term "active components" usually refers to semiconductor transistor devices that are capable of controlling, switching, or modifying the electrical energy flow in circuits. Transistors consist of three stations that can be connected to the circuit in which it is contained. These three terminals are the gate, source, and drain. A thin SiO_2 layer exists between the gate and the conducting channel in the transistor. Failures in active components due to device degradation are discussed here. Package degradation is discussed in a subsequent section. Currently, the electronics industry manufactures chips that contain millions of transistors. The ever-increasing industrial need to shrink the size of transistors, in order to increase the number of transistors per chip, emphasizes the crucial need for high-reliability design and manufacturing techniques [8]. This section focuses on the failure modes and mechanisms of such active components.

The three most important wearout failure modes in transistors are hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), and negative bias temperature instability (NBTI) [8]. The following sections summarize each of these mechanisms and their associated lifetime acceleration models.

8.5.2.1 Hot Carrier Degradation

Hot electrons occur when a semiconductor in thermal equilibrium is exposed to a high electrical field. These electrons experience a heightened state of energy, corresponding to effective temperatures of tens of thousands of degrees Kelvin [8]. The substantial increase in kinetic energy of these electrons results in them becoming "hot." Hot carriers can be created due to scattering toward the drain side of an active metal oxide semiconductor field effect transistor (MOSFET) when a high field near this side is generated due to a concentrated voltage drop [8]. Most of the scattering hot carriers surge toward the drain side. However, some of them collect enough energy to create electrons and holes through collisions [8].

A hot carrier with enough accumulated energy can be injected into the oxide layer by surpassing the energy barrier. Once injected, depending on the remaining

energy level of the hot carrier, certain weak atomic bonds in the oxide or at the injection interface may break [8], leading to the permanent alteration of the electrical characteristics of the MOSFET.

At lower temperatures, electrons are less mobile, making electron collisions less likely. This makes it more likely that the hot carriers will have a clear path to be injected into the oxide by one of the three injection mechanisms described below. Therefore, at lower temperature, hot carrier effects are more critical [8]. The temperature acceleration factor for hot carrier degradation is commonly modeled with an Arrhenius relation, as shown below:

$$AF = \exp\left[E_a\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right], \tag{8.2}$$

where T_1 and T_2 are the operating temperatures and E_a is the activation energy. According to the JEDEC standards, the activation energy has a value around -0.1 to -0.2 eV. There are three distinct processes by which hot carriers can be injected into the oxide layer, according to Takeda et al. [9].

Channel hot electron injection. The first injection mode, or channel hot electron (CHE) injection, is the random escape of a hot carrier, also known as a "lucky" electron. This is made possible by an increase in the gate current. Since current is the flow of electrons, this increased gate current supplies many potential hot carriers (electrons with high velocity) to the barrier, thus increasing the possibility of electron trapping. CHE injection occurs when the gate current has reached its maximum value. Low temperatures greatly increase these degradation effects of the oxide [10]. The Lucky Electron Model (LEM) represents the time to failure due to CHE injection:

$$\tau^{-1} = \frac{B}{T_c}\int_0^{T_c} I_D\left(\frac{I_{Sub}}{I_D}\right)^m dt, \tag{8.3}$$

where τ is the device lifetime, T_c is the full cycle time, I_D is the drain current, I_{Sub} is the substrate current, and m is the ratio of the electron energy for impact ionization to the amount of energy needed to surpass the interface barrier. The integral represents the alternating waveform of current encountered as the device is operated [8].

Drain avalanche hot carrier. The second injection mode is drain avalanche hot carrier (DAHC) injection, which has the most degrading effect at room temperature and is due to impact ionization currents in the electrons and holes creating hot carriers. Gate current increases as the gate voltage increases, and reaches a maximum when the gate voltage becomes equivalent to the drain voltage [8]. DAHC injection occurs before the gate current has reached its maximum value. The power law model, proposed by Takeda et al. [9], is more appropriate to describe DAHC due to the impact ionization constraints introduced:

$$\tau \propto \exp\left(\frac{b}{V_{\mathrm{D}}}\right), \tag{8.4}$$

where b is inversely proportional to the threshold voltage and V_{D} is the drain voltage [11].

Secondary generated hot electron. The third injection mode is secondary generated hot electron (SGHE) injection, which occurs due to secondary impact ionization or *bremsstrahlung* radiation. These minority carriers have the most severe effect in very small MOS components [8]. The body effect caused by SGHE injection was examined by Koike and Yonezawa [12] to create a model that incorporated the lifetime of the device based on the degradation caused by the primary and secondary hot electrons. The device lifetime based on the degradation caused by the secondary hot electrons in SGHE injection can be represented as follows:

$$\tau_{e2}\left(\frac{I_{\mathrm{D}}}{W}\right)^2 = (\Delta D_{\mathrm{f}})^{1/n} H_{e2}\left(\frac{I_{\mathrm{Sub}}}{I_{\mathrm{D}}}\right)^{-m_{e2}} \exp\left(\frac{a_{e2}}{|V_{\mathrm{B}}|}\right), \tag{8.5}$$

where τ_{e2} is the device lifetime due to the secondary hot electron effects, W is the channel width, ΔD_{f} is the degradation criteria for lifetime, n is a first impact ionization parameter, and H_{e2}, m_{e2}, and a_{e2} are the secondary impact ionization parameters [8].

Additionally, HCI can also be caused by quantum tunneling of the electrons, such as Fowler–Nordheim or direct tunneling [8] and this is discussed further in the next section on dielectric breakdown. A commonly used wearout model for HCI is [8]

$$\mathrm{MTTF}_{\mathrm{HCI}} = A_{\mathrm{HCD}} \exp\left(\frac{\theta}{V_{\mathrm{ds}}}\right), \tag{8.6}$$

where MTTF stands for mean time to failure, A_{HCD} and θ are constants based on lifetime testing, and V_{ds} is the voltage from the drain to the source. This simple equation is only valid for a small range of voltages near the maximum substrate current.

8.5.2.2 Time-Dependent Dielectric Breakdown

The thin oxide layer in the transistor device can undergo degradation, due to wearout, which is known as TDDB. Wearout occurs over an extended time period and could be the result of operational stresses, such as voltage, or tunneling electrons causing tears in the oxide [8].

Oxide charge mechanisms. TDDB is ultimately caused by the creation of charge states in the oxide under elevated electric fields [8]. These charges can be interfacial

oxide charges, fixed oxide charges, or oxide trapped charges [8]. As the names of the charges imply, these charges can be fixed or trapped electrons or holes, and can be located in the oxide or near the silicon–oxide interface. Vacancies can be produced in the oxide due to oxide rings, and dangling bonds tend to occur near the silicon–oxide interface. Defects such as vacancies and dangling bonds cause interfacial oxide charges. Fixed oxide charges are positive charges located near the oxide interface in vacancies, and are a result of heat treatments. Oxide trapped charges also occur in vacancies and are a result of the fabrication process [8].

Tunneling mechanisms. As was mentioned previously, tunneling of electrons can result in dielectric breakdown. Under the exposure of an elevated electric field, penetration of the electrons can occur through the oxide barrier and into the conduction band. This quantum mechanical process is known as Fowler–Nordheim tunneling [8]. The width and thickness of the oxide layer determine the tunneling process that will dominate. For very thin oxides, <3 nm of wall thickness, direct tunneling is the main mode of current travel. Unlike Fowler–Nordheim tunneling, direct tunneling does not have a direct dependence on the electric field [8].

Dielectric trap generation models. The current models for dielectric breakdown include the anode hole injection (AHI) model, or 1/E model, the thermochemical model, or E-model, and the anode hydrogen release (AHR) model [8].

The 1/E (AHI) model [13] proposes that TDDB is caused by AHI into the oxide. These holes can become trapped, which increases the electric field, hence increasing electron tunneling, according to Fowler–Nordheim tunneling. This process breaks silicon–oxide atomic bonds and leads to dielectric breakdown [8]. The 1/E or AHI model for the time to breakdown (T_{BD}) of the dielectric is shown below:

$$T_{\mathrm{BD}} = \tau_0(T)\exp\left(\frac{G(T)}{\varepsilon_{\mathrm{OX}}}\right), \tag{8.7}$$

where $\varepsilon_{\mathrm{ox}}$ is the electric field strength in the dielectric layer and $\tau_0(T)$ and $G(T)$ are temperature-dependent constants. This model does not address substrate currents that occur at low voltages [8]. A corresponding acceleration factor for accelerated testing is given as

$$AF_{(1/E)}(T_0, \varepsilon_0;\ T_1, \varepsilon_1) = \frac{\tau_0(T_0)}{\tau_0(T_1)}\exp\left(\frac{G(T_0)}{\varepsilon_0} - \frac{G(T_1)}{\varepsilon_1}\right), \tag{8.8}$$

where subscripts 0 and 1 refer to the use and accelerated conditions, respectively.

At low voltages [14], the failure modes are believed to be field driven rather than current driven and propose that the current flowing through the oxide is not actually the primary cause for defects. The E model is based on the theory of dielectric breakdown caused by the decrease in the energy required to break bonds due to interactions between the electric and vacancy dipoles [8]. The time to breakdown based on the E model is

$$T_{BD} = A_0 \exp(-\gamma \varepsilon_{OX}) \exp\left(\frac{E_a}{kT}\right), \tag{8.9}$$

where A_o is a material and process scale factor, γ is a field acceleration parameter, and k is Boltzmann's constant. Due to experimental verification, this model has been widely accepted, except for very thin oxides [8]. The corresponding acceleration factor is

$$AF_{(E)}(T_0, \varepsilon_0;\ T_1, \varepsilon_1) = \exp[-\gamma(\varepsilon_0 - \varepsilon_1)] \exp\left[\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_1}\right)\right], \tag{8.10}$$

where subscripts 0 and 1 refer to the use and accelerated conditions, respectively.

The AHR model deals with tunneling electrons, released from the anode, giving off atomic hydrogen [15]. The atomic hydrogen radicals then interact with and diffuse the oxide, causing degradation [8]. However, there are arguments against the AHR model due to the model not accounting for isotope effects [16].

Wearout models for TDDB. The wearout model for TDDB is

$$\text{MTTF}_{TDDB} = A_{TDDB} A_G \left(\frac{1}{V_{gs}}\right)^{(\alpha - \beta T)} \exp\left(\frac{X}{T} + \frac{Y}{T^2}\right), \tag{8.11}$$

where V_{gs} is the gate voltage, T is the temperature, α, β, and X are fitting parameters, A_{TDDB} is an empirically determined constant, and A_G is the surface area of the gate oxide [8].

The Weibull and lognormal distributions can be used to analyze the accelerated test data, including temperature and voltage acceleration, of dielectric breakdown lifetime [8]. The Weibull distribution has been found to more accurately fit large samples of TDDB failures, and oppositely, the lognormal distribution has been found to more accurately fit smaller sample sizes of TDDB failures [17].

8.5.2.3 Negative Bias Temperature Instability

NBTI occurs under the stress conditions of negative gate voltage and increased temperature. This failure mechanism occurs most severely in PMOS devices [8]. Continuous direct current applied to the PMOS device generates interface traps that result in voltage and current shifts, creating device instability [8]. NBTI effects exponentially heighten as the thickness of the oxide layer decreases. This implies that the density of the interface traps greatly increases as the oxide layer decreases. [8]

NBTI failure mechanisms. NBTI occurs most severely in PMOS devices due to the different oxide charge states interacting with the holes in the PMOS inversion layer. As mentioned previously, these oxide charge states include oxide trapped and fixed electrons or holes, and interface trapped charges. There is incredibly little resistance

to changes in the electrical characteristics of the silicon due to the changing density of these charges. The threshold voltage of the PMOS shifts easily to instability as the interface trapped charge changes [8, 18]. Therefore, the main failure mechanism of NBTI is the generation of the interface trapped charge.

Interface trap charge generation. The reaction–diffusion model [19] describes the low electrical field generation of interface trap charges. This model assumes that the silicon interface is riddled with defects, and that these defects can be triggered by chemical reactions into a state of electrical activity. When the activity state of the defect is altered, bond dissociation occurs, and a fixed charge and interface trap are formed [8].

NBTI models. Voltage instability occurs when the threshold voltage shifts due to the reasons discussed previously. The time to threshold voltage shift can be modeled by a power law model that considers the gate voltage, temperature, and reversible effects of diffusion [8]. This model is shown below:

$$\Delta V_{\mathrm{TH}}(t) = B_1\left[1 - \exp\left(\frac{-t}{\tau_1}\right)\right] + B_2\left[1 - \exp\left(\frac{-t}{\tau_2}\right)\right], \tag{8.12}$$

where B is the number of trivalent silicon bonds, τ is the time constant, and the subscripts 1 and 2 represent forward and reverse reactions, respectively [8].

The wearout model for NBTI is

$$\mathrm{MTTF}_{\mathrm{NBTI}} = A_{\mathrm{NBTI}}\left(\frac{1}{V_{\mathrm{gs}}}\right)^{\gamma} \exp\left(\frac{E_{\mathrm{aNBTI}}}{kT}\right), \tag{8.13}$$

where A_{NBTI} is a process-related constant, γ is the voltage acceleration factor, and E_{aNBTI} is the activation energy [8].

Further details of semiconductor failure mechanisms, models, and model constants can be found elsewhere in the literature.

8.5.3 Packaging Failures in Active Components

The packaging of the active device is often referred to as first-level packaging. This involves several steps, depending on the particular architecture selected. The package may contain a single die or sometimes there may be multiple dies to create a system-in-package (SiP). The dies can be mounted either in-plane on a substrate or vertically in 3D die-stacks. Sometimes multiple packages may be stacked on top of each other to create package-on-package (POP) architectures. Several different architectures are shown in Fig. 8.11 [20].

The specifics of the packaging steps depend on the particular package architecture selected. In general the packaging steps involve:

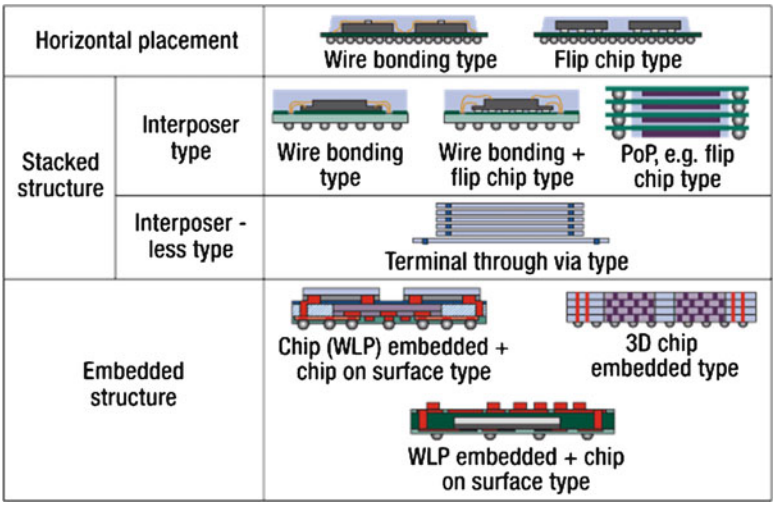


Fig. 8.11 Examples of first-level packaging architectures

- Attachment of one or more dies to interposers/substrates
- Connecting the die electrically to the substrate
- Routing the signal traces on the interposer/substrate
- Providing bond pads or terminals on one surface of the substrate for interconnection to a printed wiring board (PWB)
- Providing a protective covering, such as over-molding with an epoxy molding compound (EMC) in the case of plastic encapsulated microelectronic (PEM) components, or providing a ceramic or metal case in the case of hermetic packages

The die attachment is used to either mount the die on the surface or embed the die within a substrate or an interposer. The attachment layer may serve multiple roles including mechanical mounting, thermal dissipation, and electrical functionality. The die is electrically connected to the interposer/substrate or to other dies in a 3D die-stack, with wire bonds or with flip-chip mounting using solder joints or conductive adhesives. In 3D die-stacks, this may involve the use of through-silicon-vias (TSVs). The substrates or interposers may be multilayered and the routing may include through-thickness plated through holes (PTHs), blind/buried vias, or microvias. The encapsulation consists of molding the component and substrate (or lead-frame) in an EMC, while hermetic packaging involves sealing the component, interconnections, and substrate in a ceramic or metal case and sealing the lid and interconnection ports against moisture ingress. Examples of failure modes commonly encountered at the first-level package are listed below:

- Electromigration failure of the metal traces due to high current densities
- Electrical overstress (EOS) of metal traces due to excessive current densities
- Dielectric breakdown due to ESD

- Fracture of the brittle semiconductor die or the die passivation layer due to stresses transmitted through the package
- Bond pad corrosion due to the presence of moisture and chemical contaminants
- Fatigue delamination in the die attach due to thermomechanical stresses caused by power and temperature cycling
- Fatigue delamination failures at interfaces of the molding compound with die surface, substrate surface, or lead-frames due to thermomechanical stresses caused by power and temperature cycling and/or hygro-mechanical stresses caused by moisture cycling
- Fatigue fracture of wire bonds or bond wires themselves due to thermomechanical stresses caused by power and temperature cycling
- Solder fatigue in the interconnects between the die and interposer/substrate due to thermomechanical stresses caused by power and temperature cycling
- Via fatigue in the substrate/interposer layers due to thermomechanical stresses caused by power and temperature cycling
- Metallization corrosion in the substrate/interposer layers due to the presence of moisture and chemical contaminants
- Bond-pad pull-out under solder joints in the substrate/interposer layers due to mechanical overstress (e.g., in drop/shock loading of portable SSL products, such as handheld flashlights)
- Fatigue delamination failures in multilayered substrates due to thermomechanical stresses caused by power and temperature cycling and/or hygro-mechanical stresses caused by moisture cycling
- Conductive filament formation (CFF) between neighboring metallization elements on the substrate/interposer, in the presence of moisture and high-potential gradients
- Failure of lid seals and lead-seals in the case of hermetic packaging

Detailed discussion of these failure mechanisms and the associated PoF-based reliability models are beyond the scope of this chapter, and can be found in the literature [21, 22]. Some of these failure modes have been discussed in other chapters of this book.

8.5.4 Failure Mechanisms in Printed Wiring Assemblies and Interconnections

Printed wiring assemblies (PWAs) typically contain active and passive components either mounted on the surface of multilayered PWBs or embedded within their layers. This has typically been termed 2nd-level packaging. However, sometimes semiconductor dies are bonded directly onto PWBs, e.g., in chip-on-board technologies, in which case, this can also serve as 1st-level packaging. The failure sites and associated failure modes can be grouped under the PWB substrate,

interconnections, and separable connectors that are used to connect the PWA to wiring harnesses for the next higher level packaging.

8.5.4.1 PWB Substrate

PWBs typically consist of multilayered substrates with dielectric layers separated by copper signal planes or power planes. The surface layer contains the footprints for accommodating surface mount components. The footprint can consist of bond pads surface-mount assemblies or through holes for insertion mount assemblies. The copper signal patterns are produced through suitable plating and etching processes. Architecturally, the PWBs can be quite similar to the organic substrates used for first-level packaging. The PWB substrate layers can be either rigid or flexible. Rigid substrates typically consist of glass-reinforced polymer-matrix composites. The vast majority of PWB glass reinforcement is in the form of woven fabrics. Some low-cost options use randomly oriented distributions of chopped fibers. The surface layer often consists of an unreinforced polymer layer. Flexible substrates usually use unreinforced polymer dielectric layers. Further details can be found in IPC-4101 [23].

The individual signal layers are interconnected through the thickness by vias that are drilled and copper plated. The vias can be through-hole, blind, or buried, depending on whether they go through the entire thickness or through some portion of the thickness. Laser-drilled microvias are often used under component bond pads on the surface layers, to distribute the traces of high-density and high-I/O components to subsurface layers. A typical example of a rigid multilayered PWB construction is shown in Fig. 8.12.

Dominant failure modes associated with the PWB are listed below:

- Opens due to fatigue failures in the copper plating of vias due to thermal expansion mismatches in the thickness direction, during temperature or power cycling [24].
- Shorts due to CFF between metallizations with electrical potential gradients across them. These filaments usually form in the interior of the PWB due to the presence of moisture in hollow-core fibers or along the surfaces of fibers that have debonded from the matrix due to fatigue caused by hygro-thermo-mechanical stresses [25–28].
- Loss of surface insulation resistance (SIR) due to ionic contaminants and electrochemical migration (ECM) mechanisms on the surface of the PWB. Examples include silver dendrite formation in PWBs plated with immersion silver and tin whisker formation in PWBs plated with immersion tin. Dendrite formation usually requires the presence of an electrical bias (in addition to temperature and humidity) but whisker formation does not require the electrical bias [29]. With respect to migration and dendrite formation, the tests used include the silver migration test described in UL 796, Section 23 [30], and the electrochemical

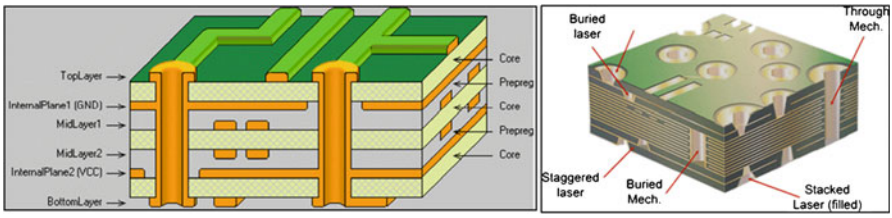


Fig. 8.12 Schematics of multilayered rigid PWB [52, 53]

migration resistance test described in the IPC test method manual, TM-650 2.6.14.1 [31]. More information can be found in IPC-9201A [32].
- General uniform corrosion of PWB metallization due to harsh corrosive chemical contaminants in the ambient environment or in the process chemicals (e.g., flux residues, etc.). This can eventually reduce the overall effective metallization cross-sectional dimensions and electrical functionality [33].
- Copper trace failures under solder bond pads due to cyclic flexural loading or due to repeated drop and shock loads [34].
- PWBs with embedded passive or active components may exhibit additional failure modes discussed earlier in Sects. 8.5.1–8.5.3.

8.5.4.2 Solder Interconnects in Printed Wiring Assemblies

Surface mount components are typically soldered onto bond pads on the surface of the PWB (surface mount assembly) and the leads of insertion mount components are typically soldered into the PTHs in PWBs. Solder joints form the electrical, thermal, as well as mechanical interconnection between the component and the PWB. Sometimes, secondary mechanical and thermal interconnections are also provided in the form of adhesives and thermal interface materials (TIMs). Solder interconnect opens are a known reliability risk in surface mount technology and shorts due to whisker formation are a risk in both insertion mount and surface mount technologies. There is a very vast literature on reliability risks in soldered interconnects, in both lead-based and lead-free technologies [see, for example, 35, 36].

The dominant failure modes for soldered interconnections are:

- Creep–fatigue failures in the solder or in the interfacial intermetallic layers due to cyclic thermomechanical stresses arising during temperature cycling and/or power cycling
- Tin whisker formation
- Metal migration due to thermomigration and electromigration in solder joints that have to carry high current densities at high temperature
- Corrosion due to contaminants such as flux residues

8.5.4.3 Separable Connectors

Most separable connectors are made from copper or copper alloys, with beryllium copper and phosphor bronze being the most common base materials due to their high electrical conductivity. The construction usually includes multiple plating layers on the contact surface. The outermost layer is usually a soft inert material (like gold) to prevent corrosion and also to ensure good contact at microasperities. This outer layer is usually plated on top of a barrier layer (such as nickel) which covers the base metal. Proper functionality requires sufficient contact force across the separable contact terminals (generated with spring forces) to plastically deform surface microsasperities, so that the contact resistance is below the acceptable threshold value.

Due to their very nature, connectors are the most vulnerable points in a circuit. There are reversible failure modes due to accumulation of dust and contaminants. However, the most common wearout failure modes in contact systems are [37, 38] the following:

Corrosion. Corrosion, from either oxidation or galvanic processes, reduces current-carrying capacity and results in intermittent, ultimately permanent failure of the circuit. In harsh environments the major cause of connector failure is galvanic corrosion, in the presence of an electrolyte, usually water. The mating and unmating process can minimize corrosion intermittents by scraping away corrosion products. On the other hand, the mating/unmating process can also hurt by scraping away the surface layer of protective metallization and exposing the underlying base metal to ambient corrosion agents.

Diffusion and migration. Metal migration can occur when metal ions migrate because of electric field, thermal field, mechanical stress field, or combinations. Examples include shorts and arcs due to growth of dendrites and whiskers across neighboring or mating terminals.

Dry oxidation mechanisms. When the copper is heated (e.g., by bad connection), more oxides are formed. These high-resistance oxides continue to increase the heat until the conductor breaks. At temperatures above 88°C (180°F), copper oxidizes in dry air. Copper is oxidized in an ammonium environment and is also affected by sulfur dioxide.

Fretting wear. When dealing with SSL products in automotive applications, separable connectors will have to be deployed in vibration environments. Sustained vibration micromotion can lead to fretting wear of the thin plating layer of soft materials (e.g., gold or tin) that are sometimes used as a protection layer on the surface of the mating conductive surfaces. The soft surface layer serves a dual purpose. It protects the underlying base material from oxidation and maximizes contact surface area by plastic deformation at the microscale surface asperities. Fretting wear therefore leads to degradation due to both of these reasons.

Creep. The contact resistance in separable connectors depends on the normal compressive force at the contact surfaces. The connector design incorporates spring elements, to sustain this contact force throughout the entire life of the connector. If the connectors see sustained application in high-temperature environments, then the spring metals or their housing may experience creep deformation, leading to a slow relaxation of contact forces and a corresponding increase in contact resistance.

Connectors are usually designed and tested as per industry reliability standards, e.g., EIA 364-1000 [39], to assure reliable operation. However, these standards are empirically developed for connectors in general, and are not necessarily based on rigorous physics of failure methods for any particular design or any particular use condition, and hence do not provide application-specific acceleration factors.

8.6 Hierarchical Codesign for Reliable SSL Driver Electronics

The term codesign has been used in this section to imply design of the SSL driver electronics concurrently for both electrical functionality AND reliability, using a combination of simulation and testing approaches. Design for reliability (DfR) is based on the PoF approach discussed throughout this chapter. Since the dominant failure mechanisms in SSL systems (discussed above in Sect. 8.5) can be driven by electrical, mechanical, thermal, or chemical stresses, codesign activities include multi-physics analysis, simulations, and testing. PoF models and analysis are used to ensure sufficient design margins for reliable performance. Design margins imply stress margins for overstress failure mechanisms and life margins for wearout failure mechanisms. The term hierarchical has been used to imply that both top-down analyses (such as Failure Modes, Mechanisms, and Effects Criticality Analysis (FMMEA)) as well as detailed bottom-up analyses (such as detailed PoF assessment) are needed to ensure reliable designs. This section provides a brief overview of both approaches.

8.6.1 Failure Modes, Mechanisms, and Effects Criticality Analysis

The FMEA (Failure Modes and Effects Analysis) methodology is a systematic procedure to recognize and evaluate the potential failure modes of a product and its effects, and to identify actions that could eliminate or reduce the likelihood of the potential failure to occur. The basic FMEA procedure consists of the following steps [40]:

1. Identify elements or functions in the product
2. Identify all element or function failure modes
3. Determine the effect(s) of each failure mode and its severity

4. Determine the cause(s) of each failure mode and its probability of occurrence
5. Identify the current controls in place to prevent or detect the potential failure modes
6. Assess risk, prioritize failures, and assign corrective actions to mitigate the risk
7. Document the process

To achieve the greatest value, FMEA should be conducted before a failure mode has been unknowingly built into the product. For risk assessment, an FMEA uses occurrence and detection probabilities in conjunction with severity criteria to develop a risk priority number (RPN). The RPN is the product of severity, occurrence, and detection. The calculated RPNs are prioritized and corrective actions are taken to mitigate the risk associated with the potential failure. Once corrective actions are implemented, the severity, occurrence, and detection values are reassessed, and a new RPN is calculated. This process continues until the risk level is acceptable.

A limitation of the FMEA procedures is it does not identify the root-cause failure mechanisms (and the associated failure models) in the analysis and reporting process. In the PoF approach, root-cause mechanisms (and PoF failure models) are identified for each possible failure mode, to aid in developing failure-free and reliable designs. Failure mechanisms and their related physical models are also important for planning tests and screens to audit nominal design and manufacturing specifications, as well as the level of defects introduced by excessive variability in manufacturing and material parameters. Without information on failure mechanisms, FMEA may not provide a meaningful input to critical procedures such as virtual qualification, root cause analysis, accelerated test programs, and remaining life assessment.

In PoF-based reliability assessment, failure models of the relevant mechanisms are used to analytically estimate distributions of time-to-failure, to identify potential design weaknesses, and to evaluate competing design options, so that product development cost and time can be minimized. Reliability simulation can only be technically and economically effective if it considers the appropriate failure mechanisms relevant to a particular design and application environment. Addition of this failure mechanism assessment step in the FMEA process leads to Failure Modes, Mechanisms, and Effects Analysis (FMMEA).

FMMEA enhances the value of the FMEA and FMECA methods by identifying high-priority failure mechanisms so that their affects can be mitigated. Models for the failure mechanisms help in the design and development of the product. FMMEA is based on understanding the relationships between product requirements and the physical characteristics of the product (and their variation in the production process), the interactions of product materials with loads (stresses at application conditions), and their influence on the product susceptibility to failure with respect to the use conditions. The steps of the FMMEA process are:

– Define system architecture, and identify elements to be analyzed and their functions
– Identify potential failure modes for given loading conditions

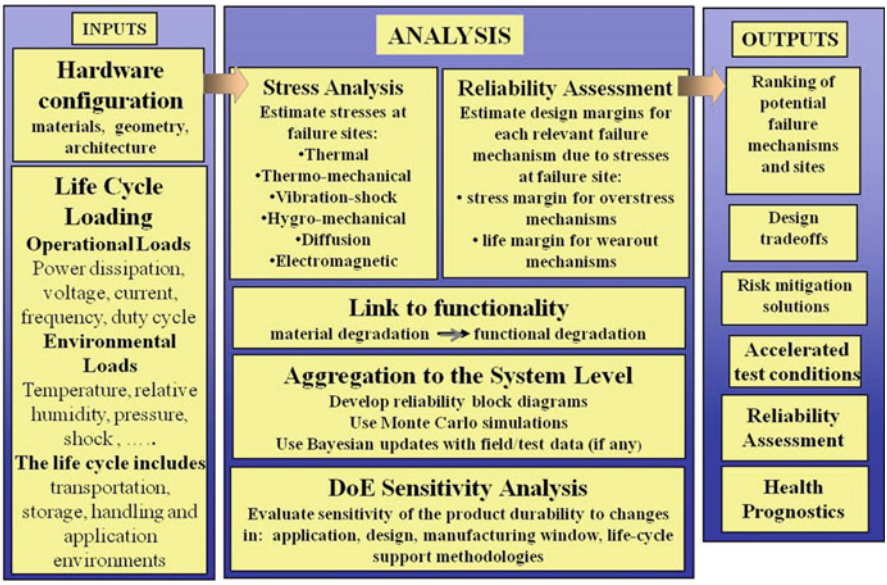


Fig. 8.13 Schematic of the virtual qualification process

- Identify potential failure causes
- Identify potential failure mechanisms
- Identify relevant failure models
- Prioritize failure mechanisms in terms of severity of failures

8.6.2 Virtual Qualification During System Codesign

Virtual qualification (VQ) is a process that requires significantly less time and money than accelerated testing to qualify a part for its life cycle environment. This simulation-based methodology is used to (1) identify and rank the dominant failure mechanisms associated with the part under life cycle loads; (2) conduct design trade-off studies; (3) determine the acceleration factor for a given set of accelerated test parameters; (4) determine the time-to-failure corresponding to the identified failure mechanisms; and (5) determine the remaining useful life for real-time prognostics and health management. As shown in Fig. 8.13, the virtual qualification process comprises two main steps: (1) appropriate stress analysis and (2) damage accumulation assessment.

The stress modeling uses knowledge of the product architecture and life-cycle loading to identify the stress magnitudes at critical failure sites. Examples include analysis of (1) electrical stresses (voltage and current density); (2) thermal stresses (temperature and heat flux); (3) thermomechanical stresses (mechanical

deformations, stress, and strain); (4) chemical stresses (concentrations of moisture and other harsh chemicals that can cause corrosion and metal migration); (5) hygromechanical stresses (mechanical deformations, stress, and strain); (6) mechanical stresses due to quasi-static mechanical loading, vibration, and shock (mechanical deformations, accelerations, stress, and strain); (7) electromagnetic stresses (field intensities that cause EMI); and (8) combined stresses.

The damage models quantify the degradation due to dominant failure mechanisms, in response to the stress histories at the critical failure sites. The output of the damage modeling provides the design margins. This includes stress margins for overstress failure mechanisms and life margins for wearout failure mechanisms. Dominant failure mechanisms in SSL driver electronics are listed in Sect. 8.5 and in Table 8.1.

The stress-degradation models can then be used to conduct parametric sensitivity studies and can be aggregated together to predict reliability at the system level.

8.7 Accelerated Product Qualification Strategies for SSL Driver Electronics

Three main reasons why a product may fail are (1) design deficiencies or flaws; (2) excessive manufacturing variabilities due to quality control problems; and (3) accidental misuse.

While the third reason is not within the direct control of the product developer, the first two can be minimized by careful design practices and manufacturing process controls. The design/process robustness (design margins) can be verified at appropriate steps during product development, using accelerated stress testing (AST), as depicted in the flowchart in Fig. 8.14.

AST is based upon the concept that a product will exhibit the same failure mechanism and mode in a short time under high stress conditions, as it would exhibit in a longer time under actual life cycle stress conditions. Such a stress-life transfer function is shown schematically in Fig. 8.15a. The stresses must be carefully enhanced in accelerated tests because of the possibility of failure mechanism shifting when there are competing failure modes with different stress-life acceleration transforms, as shown schematically in Fig. 8.15b. Accelerated stress tests are used to precipitate failures during product development and verification. Only with the knowledge of the relevant failure mechanisms can one design appropriate tests (e.g., stress levels, physical architecture, and durations) that will precipitate the failures by the same mechanism without resulting in spurious failures. The accelerated test data can be used to estimate times to failure in the field, if the mechanism and stresses that affect both the mechanism and times to failure are known and understood. The following sections give a brief account of the principal steps.

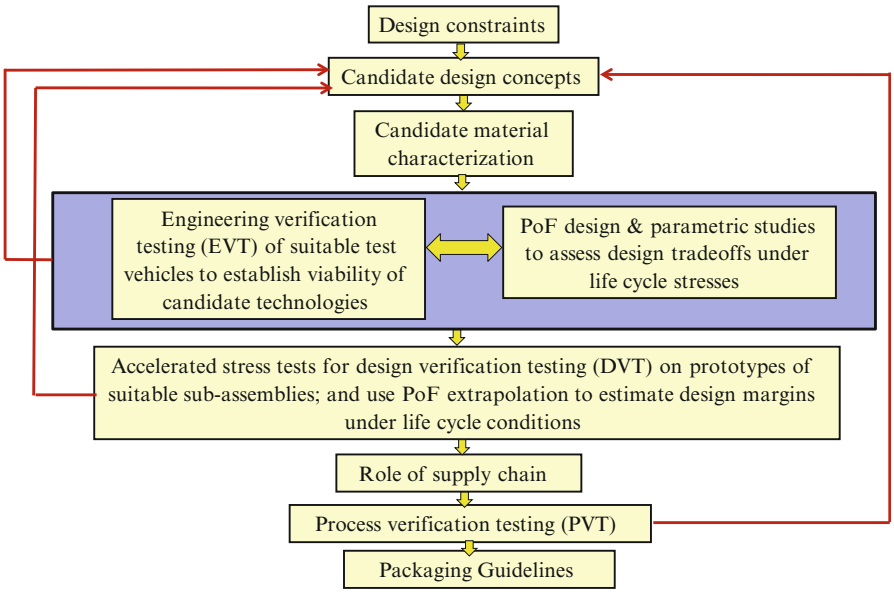


Fig. 8.14 Schematic of product verification process

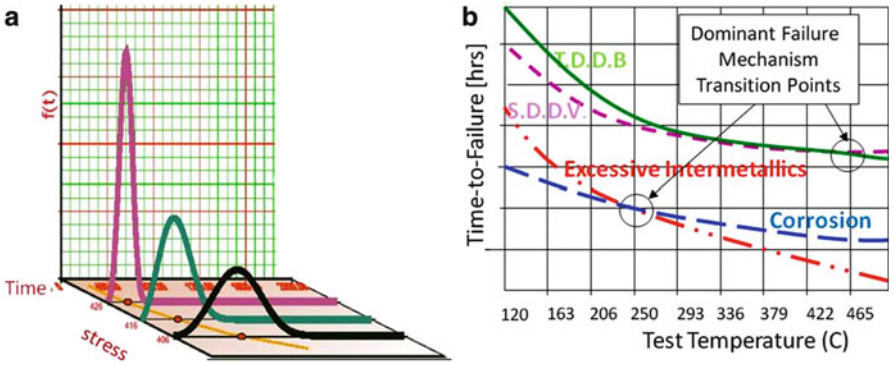


Fig. 8.15 (**a**) Stress-life acceleration transformation for a given failure mechanism in accelerated stress testing; (**b**) transition of failure mechanisms during accelerated stress testing

8.7.1 Engineering Verification Testing

Identifying design problems and solving them as early in the design cycle as possible is key to keeping new product introduction (NPI) within budget and schedule. Too often, product design flaws and performance problems are not detected until late in the product development cycle—when the final product is

ready to ship. The old adage holds true: the cost of correcting errors increases by an order of magnitude (tenfold) from the engineering phase to the production phase, and by another order of magnitude to correct the problem in the field after the product has been launched.

In the prototyping stage, engineers create either actual working samples of the subassemblies that will go into the planned product or test vehicles that deploy the technologies and materials that are going to go into the final product. Engineering Verification Testing (EVT) is conducted on such prototypes to verify that the technologies and constituent design concepts and candidate materials will indeed meet the performance/reliability goals under the expected life cycle conditions. The goal is to use such testing to verify early in the development cycle whether the design is acceptable as is or will need improvements. EVT may include basic functional tests, parametric measurements, specification verification, and also preliminary life testing of the engineering prototypes described above.

8.7.2 Design Verification Testing

When the product design is completed and prototypes are developed, the product is moved to the next phase of the design cycle: design verification and refinement. Engineers verify the ability of the design to meet performance and design requirements and specifications. Design improvements are implemented if necessary. This is accomplished with Design Verification Testing (DVT), which consists of objective, comprehensive testing verifying all product specifications, interface standards, OEM requirements, and diagnostic commands.

DVT is an intensive testing program, typically consisting of five areas of testing:

- Functional testing (including usability)
- Performance testing
- Climatic testing
- Reliability testing
- Compliance testing

8.7.3 Process Verification Testing

Process verification test is the final go/no-go in the product development cycle. It covers the same type of reliability tests in DVT, except on a larger sample base to truly take into account the statistical variability in the production process. Sometimes, it is considered as a subset of the DVT process. Process Verification Testing (PVT) is performed on preproduction or production units and basically it verifies whether the design has been correctly implemented into production.

8.7.4 Steps for Product Verification (EVT/DVT/PVT) with Accelerated Stress Testing

The product verification discussed in the last three sections usually relies on the use of accelerated stress testing guided by PoF simulations. This PoF-guided testing is tailored for individual hardware-specific and user-specific risk tolerance. This is a distinctly different philosophy than specs-based testing. The PoF-based accelerated stress tests can be used in two ways. The first application is to verify the stress margins for expected overstress failure mechanisms, using systematic step-stress testing until the test specimen reaches its destruct limits. The second application is to verify the life margins (durability) for expected wearout failure mechanisms by intentionally using stress levels that are in excess of the levels expected in the field so that degradation rates can be accelerated to some suitable level in the test. The latter is sometimes called accelerated life testing (ALT) or AST and requires quantitative assessment of the acceleration factors using PoF models of the relevant failure models. The acceleration factors are used to extrapolate the ALT results to life cycle stress conditions so that in-service reliability can be assessed. The systematic PoF-based approach for ALT is typically a five-step process, as discussed below.

Virtual qualification. This is a modeling and simulation step in preparation for accelerated testing. As discussed above in Sect. 8.6, the output of this modeling tells us which failure mechanisms pose the greatest reliability risks during the product life cycle. This information is useful to decide which failure mechanisms and modes should be the focus of ALT. This step also tells us what PoF failure models can be used to extrapolate the test results to the life cycle.

Test design. Based on the weakest failure site(s) uncovered in Step 1, a test setup is designed to exercise these failure sites/modes.

Test setup characterization. Once the test setup design is finalized, the test setup and test specimen are experimentally characterized. The goal is to verify that the response of the test specimens agrees with the VQ models and to see whether the test setup is functioning as intended. The measured response is used to verify and calibrate the estimates obtained from the VQ modeling. The second goal of this step is to determine the stress levels for the AST. During this step, a systematic step-stress testing is conducted to find the destruct limits of the product. This process is sometimes termed HALT© in the literature [41]. The stress levels for ALT are then selected to be suitably smaller than the overstress limits of the test vehicle, so that the time to failure in the accelerated stress test is economically viable.

Virtual testing. When Step 3 is complete, the accelerated testing configuration is simulated using the same PoF failure models used for VQ, to assess the time-to-failure in the test. This step, termed virtual testing, provides an estimate of the acceleration factor between the field and test configurations.

AST. The final step is to conduct the accelerated stress test at the load levels determined in Step 3. Time to failure is documented, statistics of the failure data are determined, and failure analysis is conducted to confirm that the root causes are the same as those expected from VQ and VT.

At the end of the AST process, the time to failure in the field is estimated by using the time to failure measured in Step 5 and the acceleration factor estimated in Step 4. This PoF-based approach has been used successfully in the literature to qualify new technologies and electronic products and is preferred to spec-driven qualification tests that do not necessarily account for product-specific and user-specific reliability challenges [42–44].

8.8 Effects of Manufacturing Quality in SSL Driver Electronics

The manufacturing process introduces variabilities that can affect the stress state, damage accumulation rates, and damage endurance of the product. The goal in this step is to use a combination of testing and analysis to assess the extent of variabilities so that their influence on product reliability can be assessed. Key approaches for assessing manufacturing variability include nondestructive evaluation (NDE) methods. Accelerated stress testing is also used in some cases to precipitate latent defects as active failures. This process, termed "stress screening," can be used to screen out defective specimens if the defect distributions are multimodal. PoF methods are useful for designing screens so that the screen does not consume excessive life in "good" specimens. Thus screens can be effective if the defective subpopulations are substantially weaker than the main ("good") population. The stress levels used for stress screening are usually milder than those used for VQ. Once again, the goal is to understand the role of the defects in accelerating the damage accumulation rates, so that the stress screens can be designed and tailored based on PoF principles instead of spec-driven "one-size-fits-all" screening regimens.

The stress screen acts as a quality audit. Sometimes such audits are done on statistically significant sample sizes. The sample size for quality audit testing is estimated to provide statistically significant conclusions regarding the defect distributions in the test vehicles. Stress screens cannot guarantee that all defective specimens can be detected, but are often a viable option to remove gross defects, especially in low-volume complex product lines that include many manual operations. However, as the manufacturing volume increases and the manufacturing process becomes more automated, the cost-effectiveness of stress screening decreases and it is better to invest than in effective statistical process controls. Further information can be obtained from the literature [42, 45].

8.9 Prognostics and Health Management of Driver Electronics to Assure High Availability

Many SSL systems, especially those used in commercial applications, are expected to satisfy very stringent availability and reliability requirements. This is particularly challenging when the life-cycle usage conditions have significant variability and uncertainties, e.g., in outdoor SSL products. One of the methods being explored by SSL manufacturers to assure high availability under high uncertainty is real-time prognostics and health management (PHM). The goal is to generate early warning of impending degradation and failure. The time between the early warning and final system failure is termed the "prognostic distance" or the "remaining useful life (RUL)." The goal of PHM is to maximize RUL so that condition-based maintenance practices can be implemented to maximize availability and cost-effectiveness.

Health and usage monitoring of the driver electronics involves the selection and placement of appropriate sensors into the product or real-time monitoring of (1) life-cycle loads experienced by the system and (2) selected performance parameters that can be used as instantaneous indicators of the system health. The constraints on physical space and interfaces available for data collection and transmission limit the number of sensors that can be integrated into a product. Therefore, a prioritized list of failure mechanisms and the environmental conditions that affect them needs to be established to ensure that the appropriate data is collected and utilized for the remaining life assessment. The data collected from these sensors are post-processed in real time with the help of suitable data-mining algorithms (e.g., using PoF-guided machine learning algorithms) to diagnose early signs of anomalies and health degradation.

The PHM process is sometimes enhanced with the help of "canaries," which are sacrificial sub-elements of the system that are intentionally designed for accelerated degradation (compared to the degradation rate of the functional elements in the system). The use of canaries can add to system complexity and cost and must be balanced against the benefits of higher availability. Therefore suitable algorithms must be used by system designers to assess the return on investment (RoI) of implementing the PHM system. Further details on PHM implementation in electronic systems can be found in the literature [46].

8.10 Summary and Discussions

This chapter has provided a broad overview of the PoF approach for ensuring reliability of SSL products. The failure mechanisms discussed in this chapter are relevant to the driver electronics used in SSL systems. The failure mechanisms specific to the LED light engine are discussed elsewhere in this text.

Ensuring system reliability for SSL driver electronics is a challenging task because of:

- Desired lifetime levels of 50,000 operational hours
- Uncertainties of the actual life-cycle usage stresses, especially in outdoor SSL systems
- Large number of competing multi-physics failure modes and mechanisms
- Lack of design rules for high reliability
- Lack of existing acceleration test methods and/or standards to demonstrate reliability
- Lack of understanding of all the manufacturing variabilities
- Complex and diverse global supply chain

With the ever-increasing pace of new applications of SSL systems, there is an urgent need for industry-wide efforts to address the DfR rules and qualification standards for SSL driver electronics. Preliminary efforts are being initiated around the world, e.g., the Department of Energy in the USA is currently coordinating pan-industry efforts with the help of SSL manufacturers, to explore reliability practices and testing methods to assess the reliability of typical SSL systems.

References

1. Van Driel WD, Li XP, Chen J, Evertz F, Zhang GQ (Jul 2010) Solid state lighting reliability: from components to system. In: Proceedings of the LS12-WLED3 conference, The Netherlands
2. http://www.weatherbase.com (Dec 2011). Last accessed Dec 2011
3. http://www.wunderground.com/history (Dec 2011). Last accessed Dec 2011
4. Künzel HM, Zirkelbach D, Sedlbaue K (Oct 2003) Predicting indoor temperature and humidity conditions including hygrothermal interactions with the building envelope. In: Proceedings of 1st international conference on sustainable energy and green architecture, Building Scientific Research Center (BSRC), King Mongkut's University, Thonburi, Bangkok, pp 8–10
5. Dubilier C (2011) Aluminum electrolytic capacitor application guide. Accessed 6th Sept 2011
6. Gasperi ML (Oct 1996) Life prediction model for aluminum electrolytic capacitors. In: IEEE industry applications conference, vol 3, pp 1347–1351, doi:10.1109/IAS.1996.559241
7. Kobayashi T, Ariyoshi H, Masuda A (1978) Reliability evaluation and failure analysis for multilayer ceramic chip capacitors. IEEE Trans Components Hybrids Manuf Technol 3:316–324. doi:10.1109/TCHMT.1978.1135275
8. White M, Bernstein JB (2008) Microelectronics reliability: Physics-of-Failure based modeling and lifetime evaluation. NASA Technical Report WBS: 939904.01.11.10, JPL Publication, 08-5 2/08
9. Takeda E, Yang CY, Miura-Hamada A (1995) Hot-carrier effects in MOS devices. Academic, New York, NY, pp 49–58 (Chapter 2)
10. Song M, MacWilliams KP, Woo JCS (1997) Comparison of NMOS and PMOS hot carrier effects from 300 to 77 K. IEEE Trans Electron Devices 44:268–276
11. Takeda E, Suzuki N (1983) An empirical model for device degradation due to hot-carrier injection. IEEE Electron Device Lett EDL-4:111–113
12. Koike N, Yonezawa H (2002) A modeling methodology and body effect analysis for hot-carrier reliability simulation of logic circuits. IEICE Trans Electron E85-C:1356–1365

13. Schuegraf KF, Hu C (1994) Hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation. IEEE Trans Electron Devices 41:761–767
14. McPherson JW, Mogul HC (1998) Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films. J Appl Phys 84:1513–1523
15. DiMaria DJ, Stasiak JW (1988) Trap creation in silicon dioxide produced by hot electrons. J Appl Phys 65:2342–2356
16. Wu J, Rosenbaum E, MacDonald B, Li E, Tao J, Tracy B, Fang P (2000) Anode hole injection versus hydrogen release: the mechanism for gate oxide breakdown. In: International reliability physics symposium, San Jose, CA, pp 27–32
17. Wu EY, Abadeer WW, Han L-K, Lo S-H, Hueckel GR (1999) Challenges for accurate reliability projections in the ultrathin oxide regime. In: International reliability physics symposium, pp 57–65
18. Liu C-H, Lee MT, Lin C-Y, Chen J, Loh YT, Liou F-T, Schruefer K, Katsetos AA, Yang Z, Rovedo N, Hook TB, Wann C, Chen TC (2002) Mechanism of threshold voltage shift caused by negative bias temperature instability in deep submicron PMOSFETs. Jpn J Appl Phys 41:2423–2425
19. Jeppson KO, Svensson CM (1977) Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices. J Appl Phys 48:2004–2014
20. iNEMI Roadmap (2009) International electronics manufacturing initiative
21. JEP122F Standard (2010). http://www.inemi.org/sites/default/files/images/rm_keynote.pdf. Failure mechanisms and models for semiconductor devices. Joint Electron Device Engineering Council, Solid State Technology Association, Arlington, VA
22. Pecht M (ed) (1994) Integrated circuit, hybrid, and multichip module package design guidelines: a focus on reliability. Wiley, New York, NY
23. IPC-4101C (2009) Specification for base materials for rigid and multilayer printed boards. Institute for Interconnecting and Packaging Electronic Circuits, Northbrook, IL
24. Yoder D, Bhandarkar S, Dasgupta A (1993) Experimental and analytical investigation of PTH fatigue life in Aramid PWBs. IPC News and Technology Review, Institute for Interconnecting and Packaging Electronic Circuits, Part 1: vol 34, issue 4, pp 23–27 and Part 2: vol 34, issue 5, pp 20–27
25. Lahti J, Delaney R, Hines J (1979) The characteristic wearout process in epoxy-glass printed circuits for high density electronic packaging. In: Proceedings of the 17th annual reliability physics symposium, San Francisco, CA, pp 39–43
26. Rudra B, Pecht M, Jennings D (1994) Assessing time-to-failure due to conductive filament formation in multi-layer organic laminates. IEEE Trans Components Packaging Manuf Tech—Part B 17(3):269–276
27. Shukla A, Dishongh T, Pecht M, Jennings D (1997) Hollow fibers in woven laminates. Printed Circuit Fabric 20(1):30
28. Welsher TL, Mitchell JP, Lando DJ (1980) CAF in composite printed-circuit substrates: characteristics, modeling, and a resistant material. In: Proceedings of the 18th annual reliability physics symposium, Las Vegas, Nevada, p 235
29. Fang T, Mathew S, Osterman M, Pecht M (May 2006) Assessing tin whisker risk in electronic products, vol 20, issue 5. SMT Magazine, PennWell, pp 24–25
30. UL 796 (2001) Test standard for “Printed Wiring Boards”. Underwriter’s Lab, Cames, WA
31. IPC-TM-650 (2003) Test methods manual, conductive anodic filament (CAF) resistance test: *X–Y* axis. Institute for Interconnecting and Packaging Electronic Circuits, Northbrook, IL
32. IPC-9201A (2007) Surface insulation resistance handbook. Institute for Interconnecting and Packaging Electronic Circuits, Northbrook, IL
33. Bumiller E, Pecht M, Hillman C (2004) Electrochemical migration on HASL plated FR-4 printed circuit boards. J Surf Mount Technol 17(2):37–41

34. Farley D, Zhou Y, Askari F, Al-Bassyiouni M, Dasgupta A, Caers JFJ, DeVries JWC (2010) Copper trace fatigue models for mechanical cycling, vibration and shock/drop of high-density PWAs. Microelectron Reliab 50(7):937–947 (Special Issue, Eurosime 2009, MR-S-09-00568)
35. Ganesan S, Pecht M (eds) (2006) Lead-free electronics. Wiley, Hoboken, NJ
36. Shangguan D (ed) (2005) Lead-free solder interconnect reliability. ASM International, Materials Park, OH
37. Mroczkowski RS (1998) Electronic connector handbook—theory and applications. McGraw-Hill, New York, NY
38. Milton Ohring M (1998) Reliability and failure of electronic materials and devices. Academic, San Diego, CA
39. ANSI/EIA-364-1000.01 (Dec 2000) Environmental test methodology for assessing the performance of electrical connectors and sockets used in business office applications. In: ANSI Standard, Electronic Components, Assemblies and Materials Association (EIA)
40. Ganesan S, Eveloy V, Das D, Pecht M (Oct 2005) Identification and utilization of failure mechanisms to enhance FMEA and FMECA. In: Proceedings of the IEEE workshop on accelerated stress testing & reliability (ASTR), Austin, Texas
41. Hobbs G (2005) HALT and HASS, accelerated reliability engineering. Hobbs Engineering Corporation, Westminster, CO
42. Dasgupta A, Pecht M, Evans J, Evans J (eds) (1994) Quality assurance and qualification of electronic packages. Wiley, Hoboken, NJ
43. Upadhyayula K, Dasgupta A (2001) Accelerated stress testing of surface-mount interconnects under combined temperature and vibration loading. In: Chan HA, Englert PJ (eds) Accelerated stress testing handbook for quality products in a global market. IEEE Press/Wiley Blackwell, USA/UK, p 189 (Chapter 12)
44. Upadhyayula K, Dasgupta A (1999) Physics-of-Failure guidelines for accelerated qualification of electronic systems. Int J Qual Reliab Eng 14:433–447 (published in special issue on Accelerated Stress Testing)
45. Dasgupta A, Verma S, Agarwal R (Sept 1992) Towards a QML approach: product validation, process verification and control. In: Proceedings, IEEE/CHMT, 13th international electronics manufacturing technology symposium, Baltimore, MD
46. Pecht M (ed) (2008) Prognostics and health management of electronics. Wiley, Hoboken, NJ
47. Bazu M, Bajenescu T (2011) Failure analysis: a practical guide for manufacturers of electronic components and systems, 1st edn., pp 153–170. doi:10.1002/9781119990093 (Chapter 6)
48. Epcos (Dec 2011). http://www.epcos.com/inf/20/30/db/alu_x/B41112.pdf. General technical information of Al electrolytic capacitors. Accessed 3rd Jun 2011
49. Nadar K (2011). https://de.wikipedia.org/wiki/Keramikkondensator. Accessed 26 Dec 2011
50. Printline PCB Shop (2012) HDI Brocure. http://www.printline.dk/uk/hdi.php. Downloaded Jan 2012
51. University of Bolton (2012). http://www.ami.ac.uk/courses/ami4809_pcd/index.asp. Concepts of PCB design. Online postgraduate courses for the electronics industry, Bolton, UK. http://www.bolton.ac.uk/. Last accessed Jan 2012

Chapter 9
Solder Joint Reliability in Solid-State Lighting Applications

J. Kloosterman, R. Kregting, M. Erinc, and W.D. van Driel

Abstract Lighting is an advancing phenomenon both on the technology and on the market level due to the rapid development of the solid-state lighting technology. The interest in solder joint reliability has increased by the introduction of the so-called high brightness leadless type of packages. Solder joint reliability is one of the main failure modes in these package types, especially when it comes down to lifetimes beyond 20,000 h. Many end customers require lifetime prediction data with respect to board-level reliability. As it is time consuming to determine the endurance performance of each package separately, we have to look for means to reduce test time. A possible method is to actually determine the lifetime of a few products within one product family, and use the obtained results to verify and improve advanced simulation-based prediction models. The improved models will subsequently be used to predict the reliability performance of the entire product family in question. A new and innovative approach to accurately predict the board-level performance of LED packages is proposed.

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9.1 Introduction

Accelerated Life Test (ALT) is a lifetime prediction methodology commonly used by the industry in the past decades. This method, however, is reaching its limitations with the development of products within emerging technologies requiring long-term reliability. New methodologies are required to shorten the time to market, and accurately predict long-term reliability. A new method to predict long-term reliability by extending ALT methods is presented in this chapter. This will be achieved by a novel numerical-experimental approach, substantiated by a fundamental understanding and description of the degradation mechanisms involved. The purpose of ALT is to induce field failure in the laboratory at a much faster rate, by providing a harsher yet representative environment. In such a test the product is expected to fail in the lab, just as it would have failed in the field, but in much less time. Currently, the industrial trend is towards products with high long-term reliability. These products, contradictorily, are expected to be developed in a shorter time to market. For instance, typical lifetime for automotive electronics is 15 years, LEDs 7,000 h to 50,000–100,000 h, and solar panels more than 20 years. The industrial desire is to be able to qualify these products within 6 weeks, and be able to guarantee the long-term reliability. The established 1,000–6,000 h ALT schemes cannot provide the mentioned industrial needs. Therefore, the state-of-the art ALT is not sufficient anymore and extensions or new methodologies need to be developed.

The common industrial practice is to first identify the dominant failure mechanisms, and then perform tests which accelerate that specific degradation mechanism. This approach needs to be well verified in the sense that only the desired failure mechanism is triggered, and others are suppressed. Further, accelerated tests use harsh environments such as high–low temperatures, high humidity, etc. which affect the material's response to time-dependent relaxation or diffusion mechanisms as well as mixed interactions such as time and temperature, temperature and humidity.

The reliability information obtained by ALT is fed into models such as Coffin–Manson and Engelmaier, and used to extrapolate the product reliability. In products that require long-term reliability, the extrapolation extends to 10–20 years, where the errors also extrapolate orders of magnitude (Fig. 9.1). Hence, the accuracy and tolerances become crucial. From a research and development perspective, how to accurately correlate the information obtained from ALT to the application is not yet answered. The main goals of our ALT approach are the following:

- Substantiating long-term reliability predictions on reliability modeling with a physics of failure approach in a generic sense. Utilizing numerical methods based on the underlying physics is a step-up in reliability engineering compared to the, current state-of-the art, semi-phenomenological methods.
- Gaining insight on the correlation between reliability predictions based on ALT performance and field application conditions and developing numerical approaches to close the gap between the two. Such a correlation is not used by the microelectronics industry and a theoretical basis does not exist.

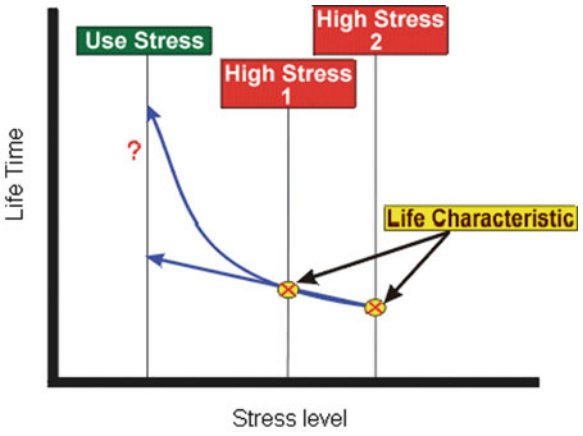


Fig. 9.1 Schematic of stress level vs. lifetime for a hypothetical electronic product

9.2 Solder Joint Reliability: Simulations

9.2.1 Literature Overview

9.2.1.1 Constitutive Creep Modeling

The FE model can incorporate several different constitutive models for the description of solder behavior. The correct description of time-dependent inelastic (or plastic) behavior for elevated stress levels is crucial, since solder fatigue failure occurs mainly through creep deformation as a result of CTE differences in combination with applied thermal processes.

– Power Law/Norton

$$\frac{\mathrm{d}\varepsilon_p}{\mathrm{d}t} = A \cdot \sigma^n. \tag{9.1}$$

This model has the simplest relation between stress and inelastic (creep) strain rate. Only two parameters need to be identified, the pre-exponential A and the stress dependency exponent n. Temperature dependence can be added as follows:

$$\frac{\mathrm{d}\varepsilon_p}{\mathrm{d}t} = A \cdot \sigma^n \cdot \exp\left(-\frac{Q}{RT}\right), \tag{9.2}$$

where Q corresponds to the activation energy, R to the universal gas constant, and T to the temperature. Power law parameters for SnAg and SnAgCu are shown in Table 9.1. These values are taken from [1].

Table 9.1 Power law creep parameters for two types of SAC

Flip chip joints	A (s^{-1})	n	Q (kJ/mol)
$SnAgCu_a$	6E−23	19	84.2
$SnAgCu_b$	1E−12	13	75.2

Table 9.2 Bulk eutectic parameters

A_1 (s^{-1})	n_1	Q_1 (kJ/mol)	A_2 (s^{-1})	n_2	Q_2 (kJ/mol)
1E−4	3	34.6	1E−12	12	61.4

Table 9.3 Material parameters for Garofalo's model

Solder	A	α (1/MPa)	n	Q (J/mol)
Sn–3.9Ag–0.6Cu [3]	1,500	0.19	4	71,300

However, at higher stresses, this relation breaks down and creep accumulation occurs at a higher rate than this model predicts. One way to compensate for this limitation is to split the model into two parts, each having its own pre-exponential A and stress exponent n. One part accounts for the low stress regime and the other for the high stress regime [2]:

$$\frac{\mathrm{d}\varepsilon_p}{\mathrm{d}t} = A_1 \cdot \left(\frac{\sigma}{\sigma_N}\right)^{n_1} \cdot \exp\left(-\frac{Q_1}{RT}\right) + A_2 \cdot \left(\frac{\sigma}{\sigma_N}\right)^{n_{21}} \cdot \exp\left(-\frac{Q_2}{RT}\right), \tag{9.3}$$

with $\sigma_N = 1$ MPa. The double power law has the parameters for bulk eutectic SnAgCu listed in Table 9.2.

– Sinh-Law/Garofalo

Another way to compensate for the higher creep accumulation is to use a sinus hyperbolical function such as Garofalo's, as shown below.

$$\frac{\mathrm{d}\varepsilon_p}{\mathrm{d}t} = A \cdot [\sinh(\alpha\sigma)]^n \cdot \exp\left(-\frac{Q}{RT}\right). \tag{9.4}$$

This relation has been created in order to avoid the power law breakdown at higher stress levels. Model parameters for different solder materials are shown in Table 9.3.

– Anand

The Anand model is the so-called unified viscoplastic constitutive model which is able to describe large isotropic deformations. It has no explicit yield condition and only has 1 state variable s, the deformation resistance. The flow equation is shown below (9.5):

$$\frac{\mathrm{d}\varepsilon_p}{\mathrm{d}t} = A \cdot \exp\left(-\frac{Q}{RT}\right) \cdot \left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}}, \tag{9.5}$$

Table 9.4 Material parameters for Anand's model [4]

Solder	A (s^{-1})	Q (J/mol)	ξ	M	$\hat{s}$ (MPa)	n	h_0 (MPa)	a	s_0 (MPa)
Sn–3Ag–0.5Cu	717.26	50,446	2	0.130	29.0	0.0436	14,560	2.2	2.45

	Parameter	Sn2Ag0.5Cu	Sn4Ag0.5Cu Sn3.4Ag0.8Cu	62Sn36Pb2Ag	Definitions
C1	S_o (MPa)	6.6	1.3	12.41	Initial value of deformation resistance
C2	Q/k (1/K)	8500	9000	9400	Activation energy / Boltzmann's constant
C3	A (1/s)	500	500	4e06	Pre-exponential factor
C4	ξ	4.3	7.1	1.5	Multiplier of stress
C5	m	0.16	0.3	0.303	Strain rate sensitivity of stress
C6	h_o (MPa)	6100	5900	1379	Hardening constant
C7	s^ (MPa)	28.7	39.4	13.79	Coefficient for deformation resistance saturation value
C8	n	0.04	0.03	0.07	Strain rate sensitivity of saturation (deformation resistance) value
C9	a	1.3	1.4	1.3	Strain rate sensitivity of hardening

Fig. 9.2 Anand parameters for different solder materials

with the corresponding evolution equation for s:

$$\frac{\mathrm{d}s}{\mathrm{d}t} = \left[h_0 \cdot \left(1 - \frac{s}{s^*}\right)^a \cdot sign\left(1 - \frac{s}{s^*}\right)\right] \cdot \frac{\mathrm{d}\varepsilon_p}{\mathrm{d}t} \quad \text{with a} > 1, \tag{9.6}$$

in which saturation s^* is

$$s^* = \hat{s} \cdot \left[\frac{1}{A} \cdot \frac{\mathrm{d}\varepsilon_p}{\mathrm{d}t} \cdot \exp\left(\frac{Q}{RT}\right)\right]^n. \tag{9.7}$$

Creep parameters for Sn–3Ag–0.5Cu, Sn–3.5Ag, and Sn–0.7Cu are also provided in [4] and are shown below in Table 9.4. For other solder materials [5] the properties are shown below in Fig. 9.2.

A modified extension of Anand's model is also described in [4], which relates h_0 with the temperature and strain rate. This extends Anand's model with three new material parameters. These are also given for the above-described materials in [4]. Authors in [6] argue that if the high sensitivity of strain rate and temperature of h_0 is neglected, the Anand model cannot predict the response of material with a high strain hardening at low temperature. Therefore h_0 should be estimated as a function

Table 9.5 h_0 Constants for Sn–3.5Ag for (9.2)

a_0	a_1	a_2	a_3	a_4
−90939.8	960.7	−0.956	−3260581.8	24976815.5

Table 9.6 h_0 Constants for (9.3)

Solder	a_h (MPa)	n_1	n_2
Sn–3Ag–0.5Cu	6,728	−0.228	−0.131
Sn–0.7Cu	5,589	0.232	−0.132

of temperature and strain rate. A polynomial expansion relation for h_0 would then look something like (Table 9.5)

$$h_0 = a_0 + a_1 T + a_2 T^2 + a_3 \cdot \dot{\varepsilon}^p + a_4 \cdot (\dot{\varepsilon}^p)^2. \tag{9.8}$$

A similar suggestion was made in [4], although an Arrhenius relation has been used (Table 9.6):

$$h_0 = a_h \left(\frac{\dot{\varepsilon}^p}{A}\right)^{n1} \cdot \left[\exp\left(\frac{Q}{RT}\right)\right]^{n2}. \tag{9.9}$$

9.2.1.2 Fatigue Modeling

Generally, five types of models can be used to predict fatigue lifetime.

– Stress based

Stress-based models typically apply to shock or vibrational fatigue. Therefore, this type of fatigue model is not useful for the current application.

– Plastic strain based

Coffin–Manson, Solomon, Engelmaier, and Miner have proposed fatigue models based on the accumulation of plastic strain. All of the plastic strain-based models require geometry-specific data. This data can be obtained through both experimental or FEA work. Well known is the Coffin–Manson model, which assumes that the total number of cycles to failure is dependent on the plastic strain amplitude, $\Delta\varepsilon_p$; the fatigue ductility coefficient, ε'_f; and the fatigue ductility exponent, c. Since the Coffin–Manson model only describes failure due to plastic strain it is commonly combined with Basquin's equation. This fatigue model accounts for both the elastic and plastic contribution to fatigue failure and is applicable for in case of both low cycle (plastic strain region) and high cycle (elastic strain region) fatigue conditions. This gives the so-called Total Strain equation:

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma'_f}{E}(2N_f)^b + \varepsilon'_f(2N_f)^c. \tag{9.10}$$

The Engelmaier fatigue model relates the total number of cycles to failure to the total shear strain, $\Delta\gamma_t$, as

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma_t}{2\varepsilon'_f}\right]^{\frac{1}{c}}. \tag{9.11}$$

With ε'_f the fatigue ductility coefficient and variable c described as follows:

$$c = -0.442 - 6 \cdot 10^{-4} \cdot \overline{T_s} + 1.74 \cdot 10^{-2} \cdot \ln(1+f), \tag{9.12}$$

in which $\overline{T_s}$ is the mean cyclic solder joint temperature in °C and f is the cyclic frequency in cycles/day. However, the Engelmaier model is based on geometry-dependent isothermal experimental fatigue data. All of the plastic strain-based fatigue models require knowledge of the plastic strain range which is geometry specific.

– Creep strain based

Fatigue models which are based on the accumulation of creep strain during cyclic loading can be separated into two mechanisms, matrix creep and grain boundary creep. The fatigue model by Syed takes both mechanisms into account by introducing an accumulated equivalent creep strain per cycle for both matrix creep and grain boundary creep. These quantities have to be determined by either experiment or simulation. Note that this approach requires a more detailed description of the solder ball deformation on local (grain and matrix) level.

– Energy based

Most fatigue models for solders are energy based. These models predict fatigue failure based on hysteresis or some kind of volume-weighted stress–strain history. The Darveaux fatigue model is the most commonly used energy-based fatigue model, although it incorporates a damage/fracture modeling since the initial crack length and the crack growth due to both primary and secondary creep accumulation per cycle are taken into account (Gustafsson). The primary equations are shown below:

$$\Delta w_{\text{ave}} = \frac{\sum_{i=1}^{\text{Elements}} \Delta W_i \times V_i}{\sum_{i=1}^{\text{Elements}} V_i};\ N_0 = K_1 \Delta W_{\text{ave}}^{K_2};\ \frac{\mathrm{d}a}{\mathrm{d}N} = K_3 \Delta W_{\text{ave}}^{K_4}. \tag{9.13}$$

– Damage based

Damage-based fatigue models use a damage parameter d to determine the amount of cycles until failure. For solders, the critical damage is assumed 0.5. This means that when d reaches $d_f = 0.5$, the solder material has failed. This type of fatigue modeling is also highly dependent on solder geometry. Therefore FE modeling has to be employed in order to use this approach.

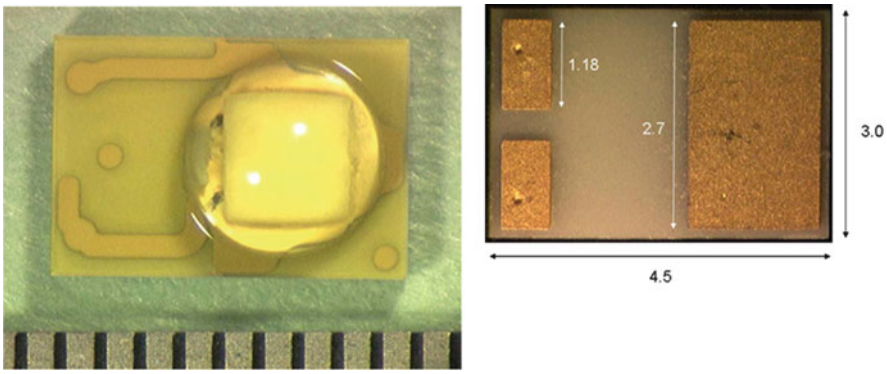


Fig. 9.3 View of the studied LED package. The top view (*left*) shows a scale with 0.5 mm increments, the under view picture (*right*) contains some dimensions (in mm)

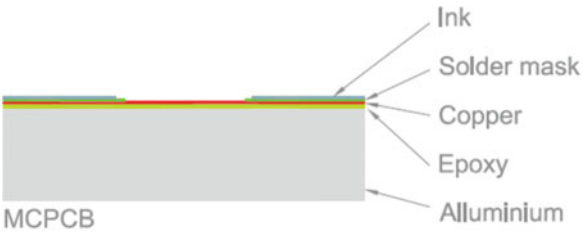


Fig. 9.4 Cross section of MCPCB, which is used in the model study of the LED

9.2.2 Finite Element Model

9.2.2.1 Model Geometry

The model geometry is based on a commercially available LED package [7]. Data concerning the applied materials and the dimensions are mainly derived from data sheets and from measurements on an LED package. Images of the LED package are shown below in Fig. 9.3.

LEDs are normally mounted to printed circuit boards (PCBs). Since thermal management is essential in view of the lifetime of an LED device, the board must apply to certain design rules to ensure a thermal resistance path that is as low as feasible. The manufacturer developed three reference boards, on the basis of standard FR4 boards (with open or capped vias) or a metal core PCB (MCPCB). The described model is based upon the MCPCB, as its geometry is much simpler than the geometry of the other board designs. Figure 9.4 shows a schematic view of the MCPCB.

In the model it is assumed that the LED device is mounted on a square MCPCB, with sides of 15 mm. A schematic cross section of the model is shown in Fig. 9.5.

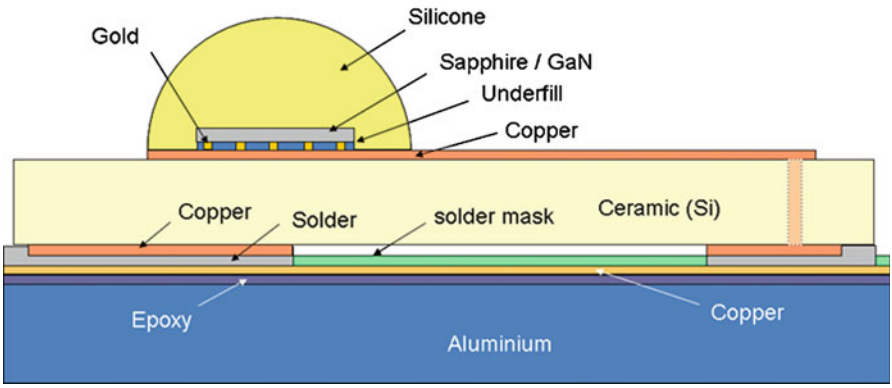


Fig. 9.5 Cross section of the LED model

Table 9.7 Material properties as applied in the FEM model

Material	Application	ε (10^{-6} K^{-1})	ν	E (GPa)	ρ (kg/m^3)	Source
Sapphire	Die substrate	6.5	0.29	345	3,980	8
GaN	Die	5.6	0.35	200	6,150	9
Gold	Gold bumps	14.2	0.44	70	19,300	11
Epoxy (1)	Underfill	75	0.4	3	1,190	5, 7
Copper	Conductive tracks	17	0.35	110	8,700	11
Silicon	Substrate	2.59	0.27	162	2,330	4, 9
Silicone	Lens	220	0.49	0.5	980	6, 10
Aluminium	Core material PCB	23.4	0.33	69	2,700	11
Epoxy (2)	Top layer MCPCB	45	0.49	0.5	980	3
Epoxy (3)	Solder mask	60	0.35	3.1	1,370	10, 12

9.2.2.2 Material Properties

The materials have already been mentioned in the foregoing. Most materials have linear elastic properties in the expected temperature and load range, but for the epoxy resin (viscoelastic) and the solder (elastic–plastic), material behavior is nonlinear. Viscoelastic properties are used to describe the solder mask behavior. The above-described two-step Wiese (power law) model is used to describe the solder creep behavior. The material properties for all other linear elastic assumed materials are shown in Table 9.7 [2].

9.2.2.3 Parametric Modeling

A three-dimensional half package model is generated in order to describe the mechanical behavior in a realistic way. The final model is shown below in Fig. 9.6.

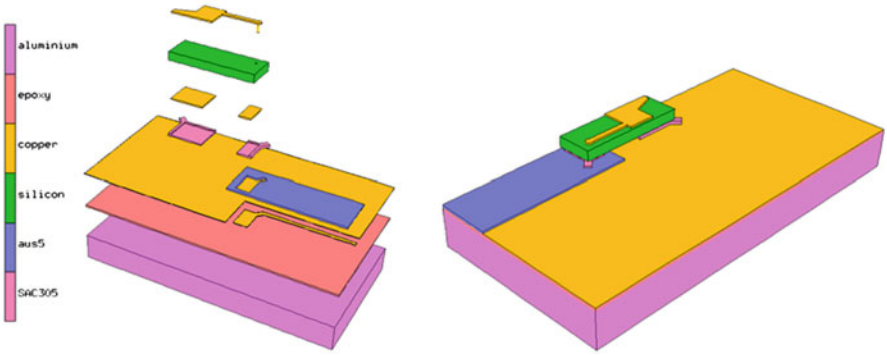


Fig. 9.6 Half LED package model. *Left image* shows exploded view, *right image* shows assembled view

This model consists of all earlier described components, each with its corresponding mechanical behavior. Most material properties are assumed to be temperature dependent; an inelastic creep model is used to describe the solder behavior; and the mechanical behavior of the solder mask is described using a viscoelastic model.

9.2.2.4 Boundary Conditions

The total loadcase consists of two parts. First, the package is cooled down from soldering temperature (216°C) to room temperature (RT, 23°C). The package is assumed to be stress free at soldering temperature. Next, thermal cycling tests (TCTs) between −40 and 125°C are performed. The temperature profile is shown in Fig. 9.7.

9.2.2.5 Weibull Fit of Fatigue Parameters

ALT tests have been conducted, using the −40 to 125°C temperature profile. The failure plot and corresponding Weibull fit are shown below in Fig. 9.8.

The unknown coefficients in Syed's fatigue law can be derived using these results. The Weibull fit shown in Fig. 9.8 can be described using the alpha (characteristic lifetime, i.e., 63.2% failed) and beta (wear out rate). For this configuration and these test conditions, alpha corresponds to 2,207 and beta corresponds to 3.4. This means the product has a characteristic lifetime of 2,207 cycles. The fatigue law coefficients are fit to this number. Since Syed's law, shown below, uses two creep strain mechanisms, two coefficients have to be derived from one experimental data set.

$$N_f = (C_1 \cdot \varepsilon_{cr1} + C_2 \cdot \varepsilon_{cr2})^{-1}, \quad \text{with } C1 = 0.02 \text{ and } C2 = 0.063.$$

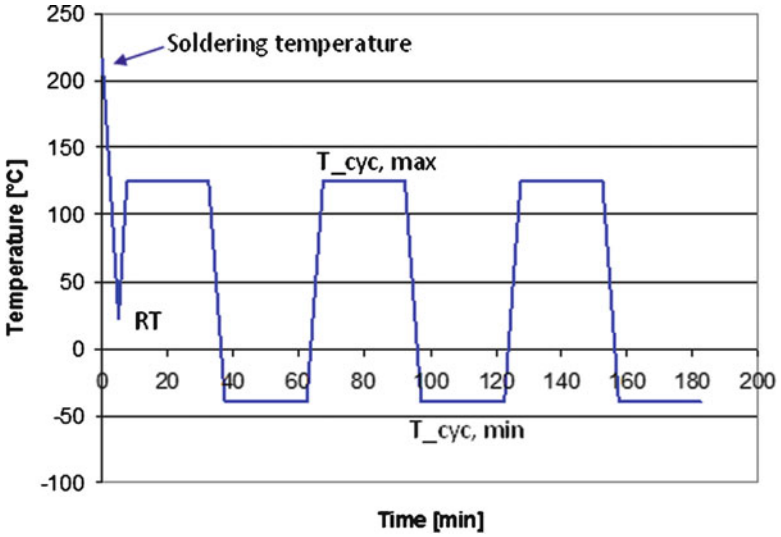


Fig. 9.7 Temperature profile of LED package showing cool down path and three thermal cycles (−40°C:125°C)

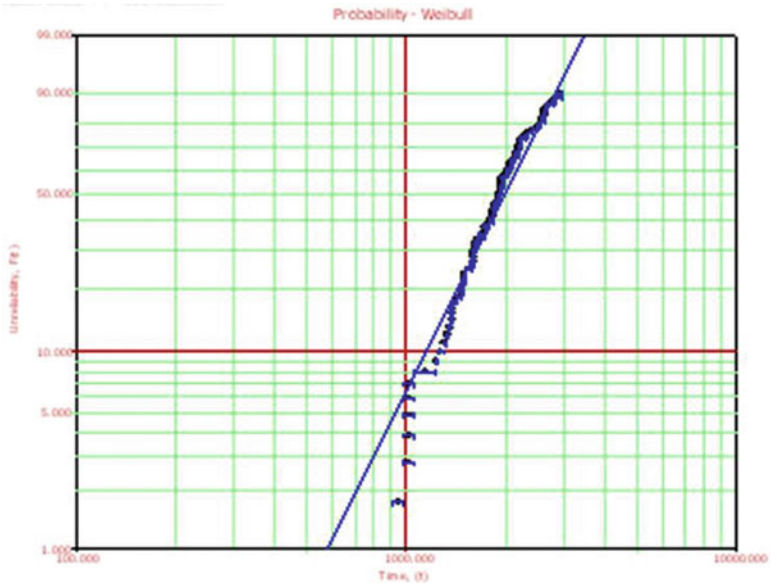


Fig. 9.8 Failure data and corresponding Weibull fit for the ALT measurements

The number of cycles until failure, N_f, is taken 2,165, after the measurements. Applying a temperature profile of 30 min at −40°C and 30 min at 125°C to the numerical model yields a creep strain accumulation per cycle of 0.0024 and 0.0036 for the first and the second creep strain mechanism, respectively. The original fatigue

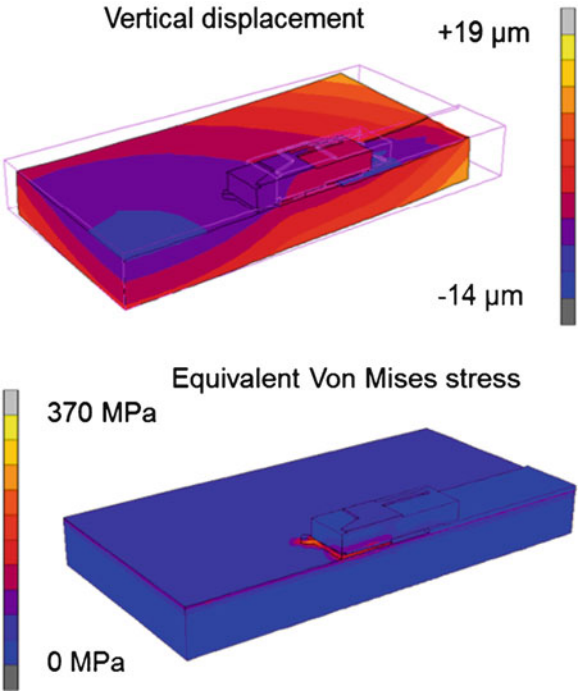


Fig.9.9 Deformations (*top*) and equivalent Von Mises stresses (*bottom*) in LED package after cool down from solder temperature

law was fitted to a ball grid array (BGA) package. The *ratio* $C1/C2$ is 0.317; this is kept constant for the new coefficient fit. Therefore $C1$ and $C2$ are determined to be 0.0347 and 0.109, respectively. Syed fitted fatigue law now becomes

$$N_f = (0.0347 \cdot \varepsilon_{cr1} + 0.109 \cdot \varepsilon_{cr2})^{-1}.$$

This fatigue law is used for further fatigue evaluations and predictions.

9.2.3 Results

9.2.3.1 Thermal Cycling

As a start, the temperature path is prescribed as simply cooling down from soldering temperature (~216°C) to room temperature. Therefore, the structure is assumed to be stress free at soldering temperature, and the gradual stress and inelastic strain buildup will be evaluated during the cooling and the subsequent thermal cycling process. Due to thermal expansion mismatch, thermal strains will be introduced which in turn lead to stresses and creep and plastic strains. Note that only the reference model with nominal dimensions is investigated at this point. Figure 9.9 shows deformations and the equivalent stress distribution on a global level after cool down from soldering temperature.

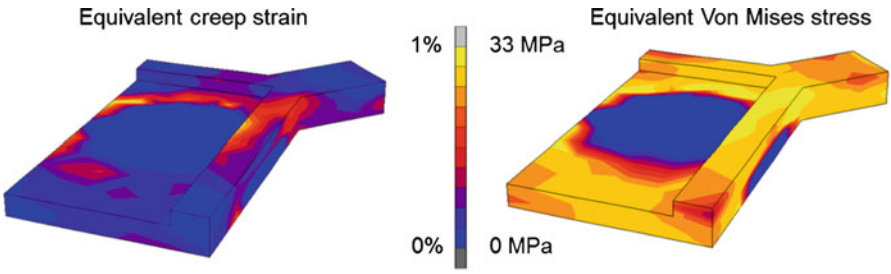


Fig. 9.10 *Left*: Creep strains accumulated in solder joint after cool down. *Right*: Equivalent Von Mises stresses after cool down

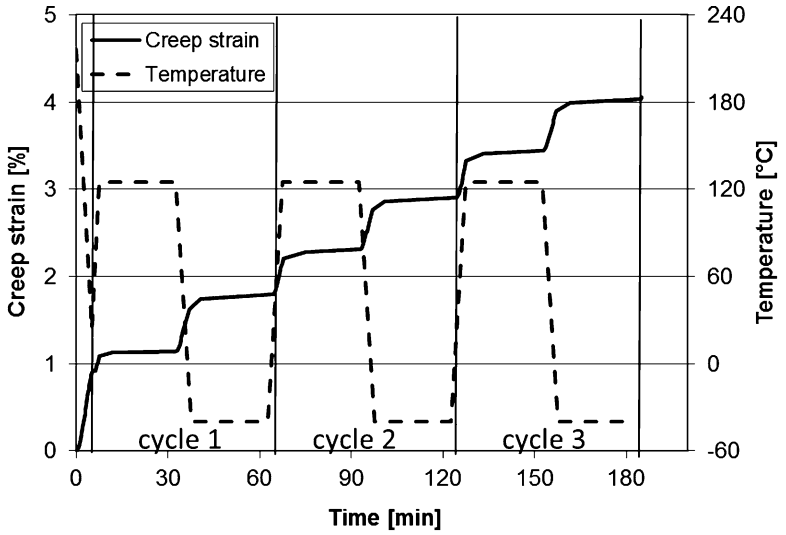


Fig. 9.11 Example of creep strain accumulation in solder joint and temperature load as a function of time

As shown above in Fig. 9.9, thermal loading of the package results in warpage due to CTE differences. The total vertical displacement difference resulting in the "smiling" type warpage is approximately 33 μm. Highest stresses occur in the vicinity of the interface between the substrates, i.e., near the solder joint. This implies that the solder joint region is sensitive to temperature cycles. Corresponding creep strains are shown in Fig. 9.10.

Naturally, the maximum values are found in the corners of the solder material. A more suitable location is shown black encircled in Fig. 9.10 (left image). The corresponding creep strain at this location is approximately 0.9%. The temperature and corresponding creep strain path as a function of time is shown below in Fig. 9.11.

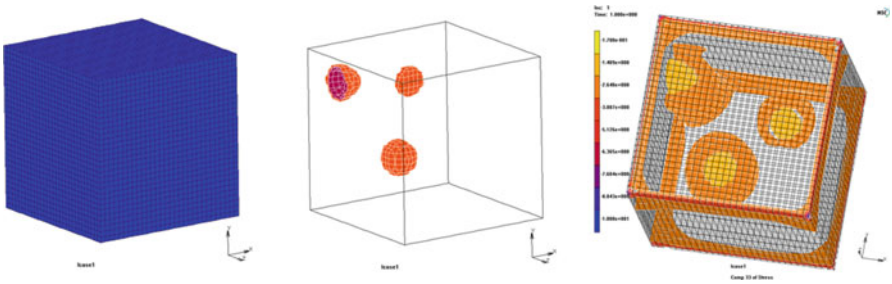


Fig. 9.12 Solid FE model showing void implementation. *Left*: Outer surface of solid FE block. *Middle* and *right*: Three small voids result in a negligible stress increase after loading

The accumulated creep strain per cycle stabilizes after the second cycle, i.e., the creep strain increase during each thermal step does not change significantly after the second cycle. Therefore, the creep strain accumulated during the third thermal cycle will be taken as representative.

9.2.3.2 Parameters Influencing the Solder Joint Reliability

– Ceramic thickness

The thickness of the substrate on which the LED device is located. The thickness is assumed to have a significant influence on the overall deformation during thermal cycles and therefore on the resulting solder creep. This influence is caused by the nonlinear increase of the stiffness due to increase in thickness and the intrinsic stiffness of the material.

– Solder void percentage

The influence of voids in the solder joint on the overall solder lifetime is not yet understood. It is assumed that voids have a negative influence on the solder reliability. Solder voids are implemented in the MscMarc FE model using combination of subroutines *Hooklw.f* and *plotv.f*. Solder material which is located within a prescribed ellipsoid (void) is designated a Young's modulus of 1, thereby effectively removing material. This is illustrated below in Fig. 9.12.

– Standoff

The distance from the PCB to the ceramic substrate is assumed to have a significant influence, since the distance determines the amount of material across which shear stresses have to be averaged. Therefore, a higher standoff is generally recommended with respect to solder joint reliability.

– Solder mask alignment

The LED device is mounted to the PCB by means of soldering. To this end, a solder mask is used to define the exact location where the solder paste must be

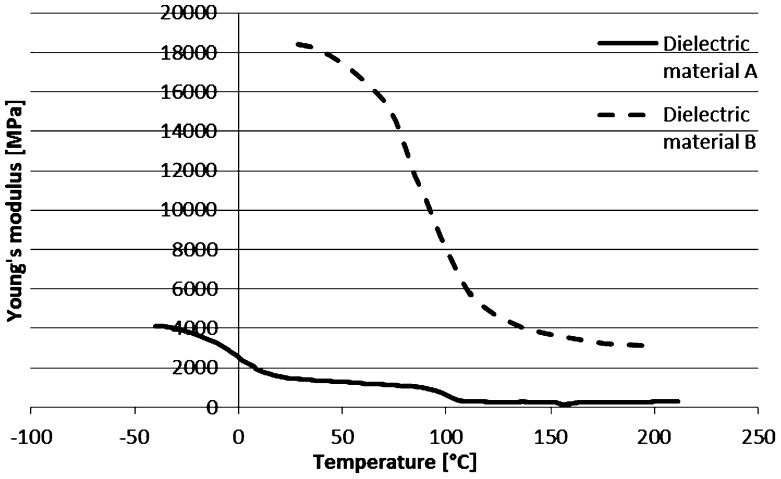


Fig. 9.13 Young's modulus of the dielectric materials as a function of temperature

applied. However, if the mask is not properly positioned then the resulting solder joint can be subjected to significantly higher loads. Misalignment of the solder mask can result in stress concentrations near the edges of the mask.

– Dielectric material

Two significantly different compounds are used as dielectric material (orange material in figure), a stiff variant (B), and a softer one (A). The Young's moduli or both materials as a function of temperature are shown below in Fig. 9.13. It is expected that the mechanical properties of the dielectric can have a significant influence on the resulting load on the solder joints.

9.2.3.3 Design of Experiments

In order to reduce the amount of simulations a Design of Experiments (DoE) approach is used. The DoE approach proposes test matrices which result in a significant reduction of the amount of simulations. For instance, current simulation variable space consists of five factors, which are all variable on two levels. Normally, a full factorial test run would result in 32 simulations. However, using the Design Expert software package, a 12 run Plackett Burman DoE is chosen which is shown below in Table 9.8.

The 12 simulations are performed and the resulting accumulated creep strains are extracted from the results in order to be evaluated. These creep strains are shown in the last column in Table 9.8. An ANOVA analysis is performed on the results and the result is shown below in Table 9.9. The parameter sensitivity results are represented in a bar graph below in Fig. 9.14.

Table 9.8 Placket Burman DoE for solder joint reliability

Run	$t_{ceramic}$ (mm)	Solder void (%)	Standoff (μm)	Solder mask alignment (μm)	Dielectric material	ε_{creep}/cycle (%)
1	0.613	0	92	0	Type B	0.89
2	0.41	0	134	30	Type B	0.579
3	0.613	0	134	0	Type A	0.815
4	0.41	25	134	30	Type A	0.646
5	0.613	25	92	30	Type A	1.14
6	0.41	25	134	0	Type B	0.559
7	0.613	25	134	0	Type B	1.35
8	0.41	25	92	0	Type A	0.552
9	0.613	0	134	30	Type A	0.616
10	0.41	0	92	30	Type B	1.02
11	0.41	0	92	0	Type A	1.28
12	0.613	25	92	30	Type B	0.869

Table 9.9 Parameter sensitivity results

Parameter	Min (−1)	Max (+1)	Coefficient test	Error	Standard coeff = 0	T for H_0 Prob > |t|
$t_{ceramic}$	0.41 mm	0.613 mm	−2.267E−4	1.642E−4	1.38	0.2168
Solder void	0%	25%	8.417E−4	1.642E−4	5.12	0.0022
Standoff	92 μm	134 μm	2.318E−3	1.642E−4	14.12	<0.0001
Solder mask alignment	0 μm	30 μm	−2.700E−4	1.642E−4	−1.64	0.1513
Dielectric material	Type A	Type B	1.037E−3	1.642E−4	6.31	0.0007

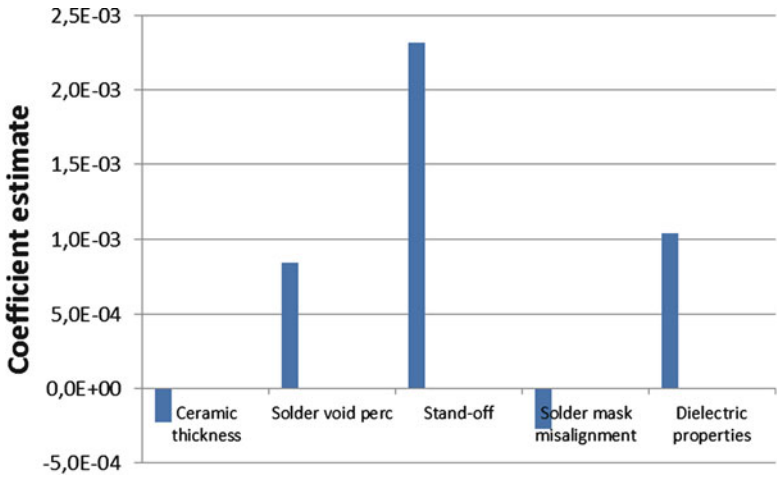


Fig. 9.14 Influence of selected variables on the accumulated creep strain per temperature cycle (−40°C:125°C)

9.3 Solder Joint Reliability Testing

9.3.1 Experimental Setup

A series of board-level experiments are done to further explore the board-level performance of LED packages. The eventual results can be used to calibrate the earlier described simulation approach. The experiments comply with the general JEDEC specifications [8–12]. The variations are listed in Table 9.10. Two type of experiments are executed:

- Using event detecting
- Using manual measurements

For the event detecting method, a data logger and/or event detector is used to perform continuous electrical monitoring. The advantage of such a system is the ability to detect and record small changes in the chain resistance and the ability to capture an intermittent high resistance event. Disadvantages of such a system are false failures due to minor electrical noise in the test apparatus, cabling, and connectors. Therefore, manual verification on failed samples is performed to eliminate false failures due to cabling, connectors, etc., not to verify a failed solder joint itself. For the manual measurements, at sequential times the boards are taken out of the temperature chambers to perform a light-up check. Failures are recorded at these time intervals. After the test, failure analysis is performed to verify the solder fatigue. Weibull plots are used to determine the statistical data. The variations that are under test are the following:

– Package size

Package size and footprints largely influence the board-level performance; thus, a package with a totally different size and footprint layout is put at test.

– Temperature swing

The temperature settings are the main driver for solder fatigue. Instead of the temperature swing −40 to +125°C, a subsequent test is executed with a swing from −20 to +100°C.

– Board type

MCPCB is known for its large coefficient of thermal expansion and high E-modulus, mainly due to the base aluminum. Therefore, a test is executed with LED packages mounted on an FR4 board.

Table 9.10 Test variations

Variation	Test setting
1. Package size	Package size increases with 1.8
2. Temperature swing	Temperature swing −20 to 100°C
3. Board type	FR4 iso MCPCB
4. Solder type	SAC versus SAC+

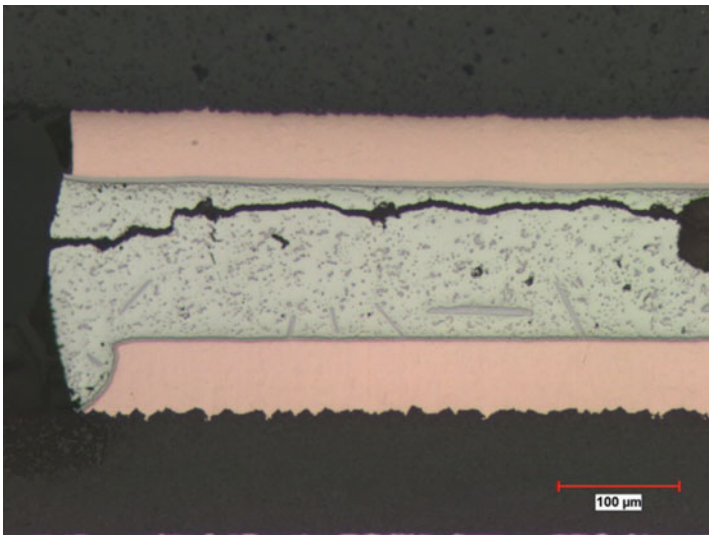


Fig. 9.15 Fatigue crack in the solder, cross section

– Solder type

Many solder types are currently under development to increase the fatigue life of several applications. A test is executed with the so-called SAC+ version.

9.3.2 Experimental Results

The experimental variations are executed until approximately 65% of the packages are failed. A selected number of failures are checked by cross-sectioning the packages through the IOs. Figure 9.15 shows a typical result of such a cross section. The solder cracks found are school examples of fatigue: nicely through the bulk of the material.

Figure 9.16 shows the Weibull curves for the different variations. Table 9.11 compares the *hours to 10% failures* for the different variations. The 10% failure point is seen as representative for acceptable field performance levels.

The results in Table 9.11 and Fig. 9.16 show that:

- The largest positive effect is given by the board type. Changing from a metal core PCB to an FR4 PCB triples the performance of the solder interconnects.
- The largest negative effect is given by the package size. A larger package (read larger distance to the neutral point) significantly reduces the performance. The relationship is quadratic with the package size.
- The smaller temperature swing increases the performance, and the relationship is linear. Dividing the reference swing of 165°C by those for variation 2, being 120°C, gives a factor of 1.38 which is close to the experimental value of 1.36.

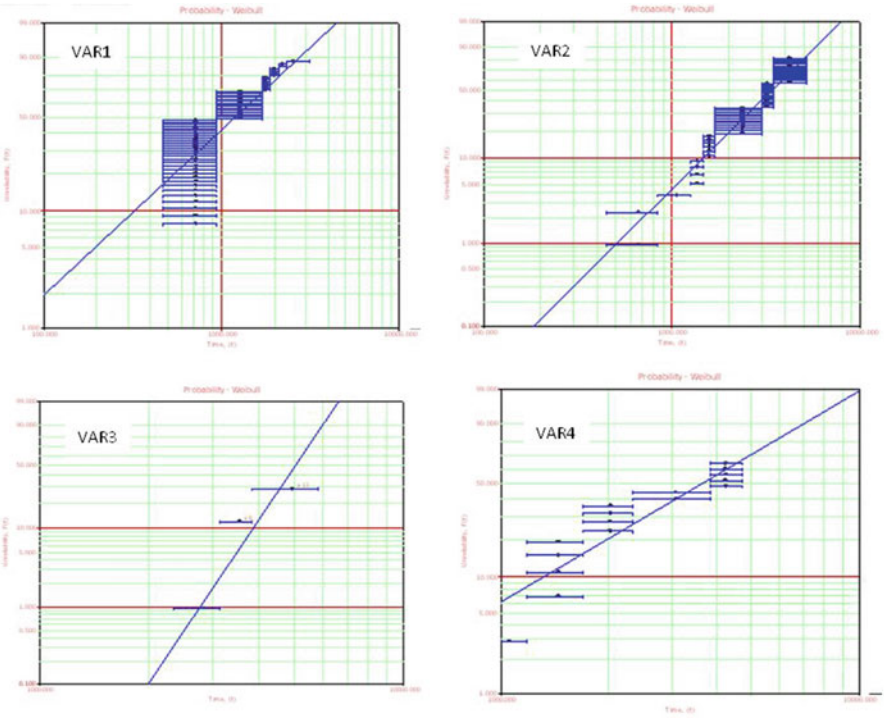


Fig. 9.16 Weibull curves for the different variations

Table 9.11 Comparison of the hours to 10% failure

Variation	10% Failures (h)	Effect
0. Reference	1,100	1.0
1. Package size	300	0.27
2. Temperature swing	1,500	1.36
3. Board type	3,800	3.45
4. Solder type	1,300	1.18

- The effect of the solder type is marginal and results in an 18% increase in interconnect performance which is close to the experimental accuracy.

9.4 Conclusions

Solder joint reliability is a crucial failure mode for SSL applications. This is mainly due to the high lifetime expectations which make the solder joints one of the first to be expected failure modes. In this chapter we have presented an ALT approach to determine the lifetime of solder joints. The approach combines experiments with

FE models and is proven to be very powerful in predicting solder joint behavior. The calibrated model can be used to examine variations in materials, package sizes, footprints, and/or temperature swings.

References

1. Wiese S, Roellig M, Mueller M, Wolter K-J (2008) The effect of downscaling the dimensions of interconnects on their creep properties. Microelectron Reliab 48:843–850
2. Wiese S, Wolter KJ (2004) Microstructure and creep behaviour of eutectic SnAg and SnAgCu solders. Microelectron Reliab 44:1923–1931
3. Zhang Q, Dasgupta A, Haswell P (2004) Partitioned viscoplastic-constitutive properties of the Pb-free Sn–3.9Ag–0.6Cu solder. J Electron Mater 33:1338–1349
4. Ning B, Chen X, Gao H (2009) Simulation of uniaxial tensile properties for lead-free solders with modified Anand model. Mater Des 30:122–128
5. Reinikainen TO (2009) Simulation-enhanced qualification of printed wired board-level reliability in microelectronic. PhD thesis, Helsinki University of Technology
6. Chen X, Chen G, Sakane M (2004) Modified Anand constitutive model for lead-free solder Sn–3.5Ag. In: International Society Conference on Thermal Phenomena, Las Vegas, pp 447–452
7. Luxeon Rebel LED packages: www.philipslumileds.com
8. Jedec JESD22: www.jedec.org
9. Yang X, Nassar S (2005) Constitutive modelling of time-dependent cyclic straining for solder alloy 63Sn-37Pb. Mech Mater 37:801–814
10. Lee WW, Nguyen LT, Selvaduray GS (2000) Solder joint fatigue models: review and applicability to chip scale packages. Microelectron Reliab 40:231–244
11. http://www.boulder.nist.gov/div853/lead_free/part1.html#%201.21.table1.2
12. Syed A (1996) Thermal fatigue reliability enhancement of plastic ball grid array (PBGA) packages. In: Electronic components and technology conference, Orlando, FL, pp 1211–1216

Chapter 10
A Multiscale Approach for Interfacial Delamination in Solid-State Lighting

H. Fan and M.M.F. Yuen

Abstract Interfacial delamination is the root cause for many failure modes in electronic devices. Examples are metal shift, wire stitch failures, and die lift. LED packages suffer from delamination as well, mainly due to the fact that transparent materials are needed to pass the light from the device to the surroundings. Using these kinds of materials has a significant impact on the mismatch of material properties. Any gap in the optical pathway will create reflections and, as such, destroy the functionality of the LED package. Therefore, investigation of interfacial delamination is rather important for LED product design. In this paper, we propose a multiscale approach to study delamination in a bi-material structure, which bridges molecular dynamics method and finite element method using cohesive zone model (CZM). CZM parameters were derived from an interfacial MD model under mechanical loading and were assigned to the cohesive zone element representing the interfacial behavior. Based on the multiscale model, the material behavior at nanoscale was passed onto the continuum model under tensile loading condition.

10.1 Introduction

A light-emitting diode (LED) is now moving not only towards high power and multifunctional application because of its high efficiency, good reliability, long life, variable colors, and low power consumption. Thermal management is one of the

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critical factors for high LED performance. Improper thermal management can result in high junction temperature of LED chips in the lamp, which not only can degrade LED lumen output, but also can result in interfacial delamination between epoxy compound and LED lead. Delamination is one of the main concerns which can destroy the functionality of the LED system. Therefore, investigation of interfacial delamination is rather important for LED product design.

An interface is a more complicated region that separates two non-miscible materials containing chemical bonding, and roughness. So far, it is still rather difficult to describe interface in one model considering all these effects. Traditional numerical method, like finite element method, is not suitable for modeling the chemical effect on the interfacial behavior. Molecular dynamics (MD) simulation is a well-established tool for modeling the material performance at an atomistic level including modulus, adhesion, thermal conductivity, solubility, diffusion, and reactivity [1–8]. However, MD model is only suitable for modeling systems consisting of up to several thousands of atoms. The layout of a real structure always consists of the interfaces at different length scales from several nanometers to several millimeters or larger. It is impossible to build the full model by MD technique due to long calculation times and costly calculations. Multiscale modeling methods is still a challenge because of the different length scales and timescales involved in the models. Several methodologies on how to couple nanoscale models and continuum models for studying material performance of composites have been established, including hand-shaking method [9], coarse-grained molecular dynamics (CGMD) method [10], and virtual internal bond method [11–15]. Hand-shaking method introduces displacement boundary conditions in interfacial region between the MD and FEA regions, where FEA mesh in the coupling region was scaled down to match the lattice of atomic cell. However, it is not easy to implement computational technique in the coupling region due to the higher distortion under large deformation, especially for the amorphous structure.

CGMD method seamlessly couples the MD regions to the continuum region through a statistical coarse graining procedure. However, the application of the multiscale method still suffers from mismatch of timescale occurring at the different length scales. VIB approach proposed by Gao and Klein [10] reproduces the behavior of a hyper-elastic solid, in which there are microstructures consisting of internal cohesive bonds based on the extension of the Cauchy-Born concept. VIB model can model crack nucleation and propagation without any presumed crack path in complex materials. However, VIB incorporates cohesive bonds into a constitutive law for the homogenized material particles. It is suitable for the bulk materials rather than description of atomic interaction along a prescribed interface. Moreover, VIB is based on the simplified atomic potentials without considering bond torsion, bending, and electrostatic force, which is obviously not adequate to model the complicated reality of the material at atomistic scale across the material interface.

Molecular modeling endeavors to simulate the basic origins of material performance in a wide variety of topics including mechanical, chemical, and electrical properties. With proper atomic description relative to the measurement (energy potential, structure, and environmental conditions), the reliable information could

be extracted from MD simulation and adequately represent the material response being measured, such as mechanical modulus for specific low k dielectric spin-on materials [3] and for epoxy resin materials [6]. Therefore, it is possible to propose a hierarchical multiscale method incorporating the information obtained by MD simulations into the continuum model to investigate the constitutive response of bulk composite which contains nanomaterials. The methodology does provide an indication that information of interfacial failure at nanoscale could be transferred to traditional continuum models by cohesive element.

In this chapter, a multiscale approach was proposed to study delamination in a bi-material structure, which bridges molecular dynamics method and finite element method using cohesive zone model (CZM). CZM parameters were derived from an interfacial MD model under mechanical loading and were assigned to the cohesive zone element representing the interfacial behavior. Based on the multiscale model, the material behavior at nanoscale was passed onto the continuum model under tensile loading condition.

10.2 Computational Methodology

The interfacial failure is an adhesion problem which is governed by the interfacial bonding, in particular the molecular bonding across the interface. Except for atoms belonging to bulk materials attached to the interface, interface is covered by some other atoms like oxygen atoms or molecules like water molecules, as well as chemical bonds formed among these interface atoms. Moreover, rough surfaces at the atomic scale represent the nature of the interface, where large gaps exist. Obviously, these dominant factors at atomic scale govern interfacial adhesion rather than bulk material properties of two bonded materials. Kendall [16] also found that the adhesion between surfaces is dominated by a number of factors such as van der Waals force, chemical bonding, and surface roughness. Obviously, without considering all these issues at the interface, continuum model is not enough to simulate interfacial delamination. In spite of long calculation times and costly calculations in MD simulation, MD models can easily and explicitly provide the interfacial behavior of a local area under different mechanical loading conditions considering chemical treatment at the interface, such as bond broking, defect generation, and delamination propagation. Therefore, MD simulation can provide traction force under the applied displacement during interface separation, which is the basis of the cohesion model for interfacial delamination. It is indicated that a multiscale investigation from atomic simulation to continuum simulation could be established for complete understanding of interfacial delamination.

An atomic-based continuum model will be proposed to investigate interfacial delamination in this study, as illustrated in Fig. 10.1. An interfacial MD model will be built to find the constitutive relation of the interface under external mechanical loads. A continuum FEA model is built with cohesive zone elements laid on the interface and the constitutive relations from interfacial MD model are inputs to cohesive elements to simulate interfacial delamination under the mechanical

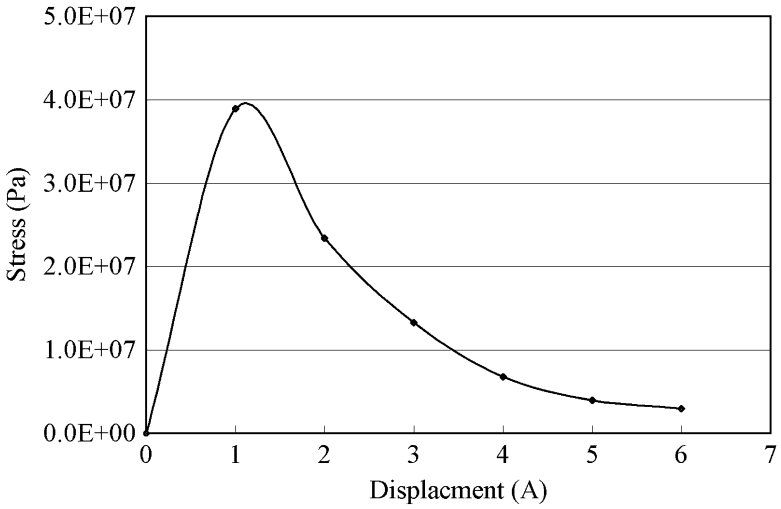


Fig. 10.1 An illustration of the proposed model linking nanoscale and macroscale

loading. The corresponding failure force varying with the applied displacement will be extracted from the model, which can be used to guide experiment for interface material design.

10.3 Interfacial MD Model

From the engineer's standpoint, interface always bears interfacial stresses coming from the bulk bodies bonded to the interface. These stresses are the macroscopic collective behavior of the atomistic bond network and govern the crack nucleation and propagation of the interface. Therefore, it is rather important to derive the constitutive relation of the interface (stress–displacement relation) from MD simulations.

Normally interfacial MD mode is built with a rectangular simulation box in the x and y directions, periodically located in the plane perpendicular to the interface, as shown in Fig. 10.2. A large vacuum space is positioned at the top of the model in order to avoid interaction across the mirror image in the z direction in the calculations. Energy minimization is first performed to find the equilibrated structure of the bi-material system. Then all the atoms except for those two layers of atoms near the interface are held rigid in all simulations. A tensile or shear displacement is applied on the model in single simulation step and the displacement is maintained by the time interval for the relaxation of the system before the same next displacement is applied. Above MD procedure is repeated until interface is completely separated. The atomic configurations and energies of the system for each simulation step are monitored and recorded during the simulations. The simulations are conducted by using Discover module of the Materials Studio

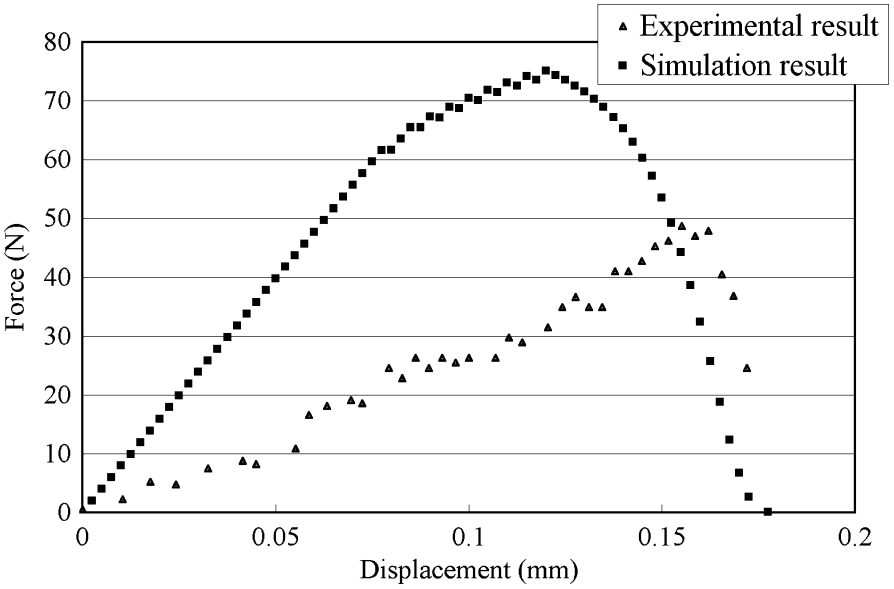


Fig. 10.2 An illustration of interfacial MD model of bi-material system

software (Accelrys Inc.) COMPASS force field that enables accurate prediction of material properties for a broad range of materials under different conditions. The COMPASS force field can accurately be applied on the systems of polymers, metals, and their interfaces.

Normally, atoms in MD simulations are modeled as point masses interacting through potentials, which are usually characterized experimentally. The potential energy of the system provides the forces on each atom, which can be used to determine the acceleration, velocity, and positions of each atom. In the classical molecular dynamics method, the equations of motion for atoms are described by Newton's equations as follows:

$$F_i = m_i \frac{d^2 r_i}{dt^2} F_i = -\nabla_i \Phi \tag{10.1}$$

where F_i, m_i, and r_i are, respectively, the force vector, mass, and position vector of molecule i. Φ is the potential energy function of the system.

When the bi-material system is subjected to external displacement, force will be transferred to the interface by the interaction among atoms whose position and velocity are governed by above potential energy. The corresponding interfacial stresses can be calculated as follows:

$$\sigma_{\alpha,\beta} = \frac{1}{A} \sum_i \left(\sum_j \frac{\partial \Phi}{\partial (r_{ij})} (r_{ij})_\alpha \cdot (r_{ij})_\beta \right) \tag{10.2}$$

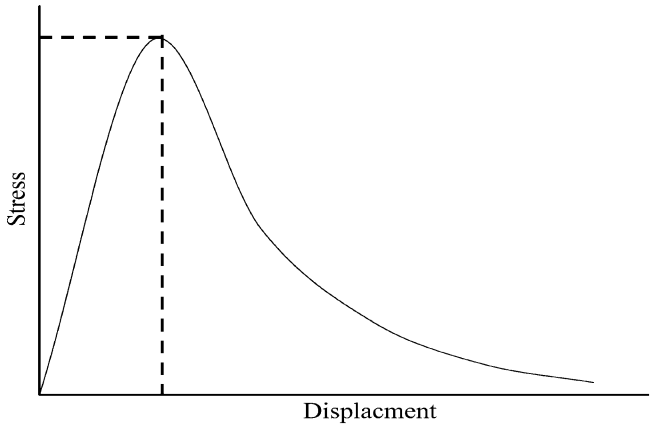


Fig. 10.3 Constitutive relation for the interface

where $\sigma_{\alpha\beta}$ is interfacial component, α and β correspond to the x, y and z directions, and A is the interfacial area.

Stress–displacement relation can be derived from MD simulations, as shown in Fig. 10.3. The relation shows the nonlinear behavior of the interface, increasing stress first and then decreasing stress with the increasing displacement. This is a constitutive cohesive relation of interface, describing the relation of interfacial traction force and opening displacement during delamination propagation. As presented by Shet and Chandra [17], the cohesive curve starts from point, A, where interface starts to separate, reaches point, B, where cohesive crack tip is located, and finally comes to point, C, where interface is completely separated.

CZM is widely used to simulate fracture process in different kinds of composites under different loading conditions [18]. The key of the CZM is the traction–displacement constitutive relation representing interfacial fracture behavior. However, it is still rather difficult to experimentally determine these parameters due to complex interfacial adhesion governed by molecular bonds and roughness. In this proposed method, these key parameters are derived by MD simulations, which avoid some experimental issues.

CZM has been widely used to study fracture process because of avoiding singularity at the crack tip and easy implementation in traditional FEA models. In a CZM, energy is allowed to flow into the fracture process zone for surface separation. Normally cohesive relation is described by cohesive parameters, namely, cohesive strength, $\sigma_{\max}$, separation distance, δ, and cohesive energy, φ, derived by the area under the traction–displacement curve. These cohesive parameters could be obtained from the above constitutive relation derived by MD simulations as shown in Fig. 10.4, which normally constitute CZMs with linear [19], bilinear [20], trapezoidal [21], and exponential shape [22]. The shape of the CZM has some effects on the analysis of interfacial delamination [23]. Bilinear and exponential cohesive models are selected and implemented in commercial codes ANSYS and ABAQUS.

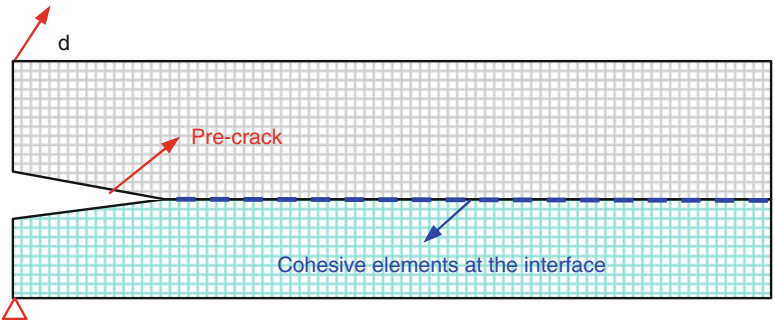


Fig. 10.4 An illustration of multi-scale model of bi-material system

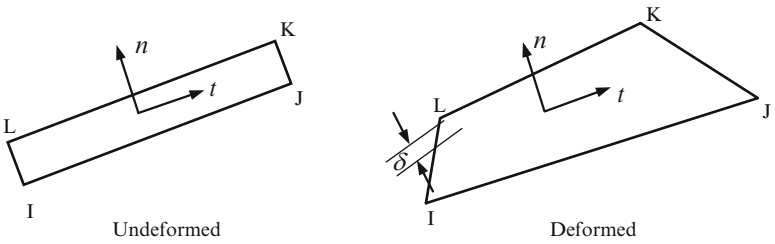


Fig. 10.5 Schematic of undeformed and deformed cohesive element

10.4 Cohesive Zone Model

A multiscale model of a bi-material system was built by using the ANSYS code, as shown in Fig. 10.4, to study the interfacial delamination of the bi-material system under mechanical loading. In this model, both materials are modeled as continuum with homogeneous and elastic properties. Solid element is used to model material 1 and material 2. Cohesive zone elements are laid on the interfaces except for a part of the interface where a pre-crack is made, as shown in Fig. 10.4. Cohesive element is used at the interface to describe the behavior with the selected CZM. Figure 10.5 shows the schematic of planar cohesive element. The initial thickness of the undeformed element is set to zero and the interfacial separation is defined as displacement jump, δ, the difference of the displacement of the adjacent interfacial nodes for deformed element. The relation of nodal force and interfacial separation is governed by the cohesive relation derived by MD simulations. Under external mechanical loads, the system undergoes elastic deformation and total energy is beard by elastic energy and cohesive energy dissipated within the cohesive elements. The cohesive energy goes within the crack tip region to separate the interface. When new free surfaces were created, the traction force and the stiffness of the cohesive zone elements on these free surfaces go to zero, but the displacement

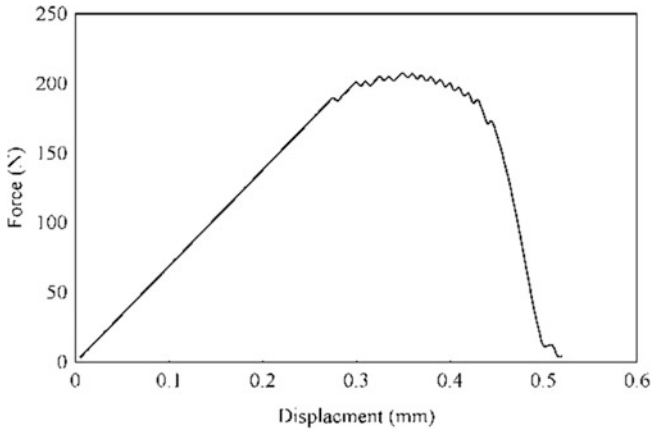


Fig. 10.6 The plot of fracture force and displacement applied on the model

across them is still continuous. That is why CZM can be implemented in FEA model for interface separation without loss of continuity.

With stipulated external displacement applied to the model, the corresponding failure force under the applied displacement is extracted from the multiscale model during interface separation, as shown typically in Fig. 10.6. The maximum fracture force is used to estimate the fracture strength of the interface which characterizes the interfacial material property.

10.5 Case Study

In this study, MD simulations are performed to evaluate adhesion between epoxy-molding compound (EMC) and copper substrate. MD model includes a fragment of EMC and copper atoms. The fully cured epoxy network is composed of diglycidyl ether of bisphenol-A (DGEBA) epoxy and methylene diamine dianilene (MDA) curing agent and the model is same as that presented by Fan et al. [8]. The model did not include solid components such as filler and pigments, which would require large-scale models that are beyond the current MD simulation capability. Based on the same method, the fully cured epoxy network was layered with a cuprous oxide surface cleaved from a crystal structure, corresponding to the (0 0 1) plane. The cured epoxy chains were initially placed on the substrate. A large vacuum spacer was positioned at the top of the epoxy chains in order to avoid interaction across the mirror image in the z direction in the calculations. The MD models were built with a rectangular simulation box 3.53×3.53 nm^2 in the x and y directions, periodic in the plane perpendicular to the EMC–Cu interface. All the copper atoms were held rigid, while all the EMC chains were allowed to move freely in all simulations. Energy minimization was performed to find the equilibrated structure of the

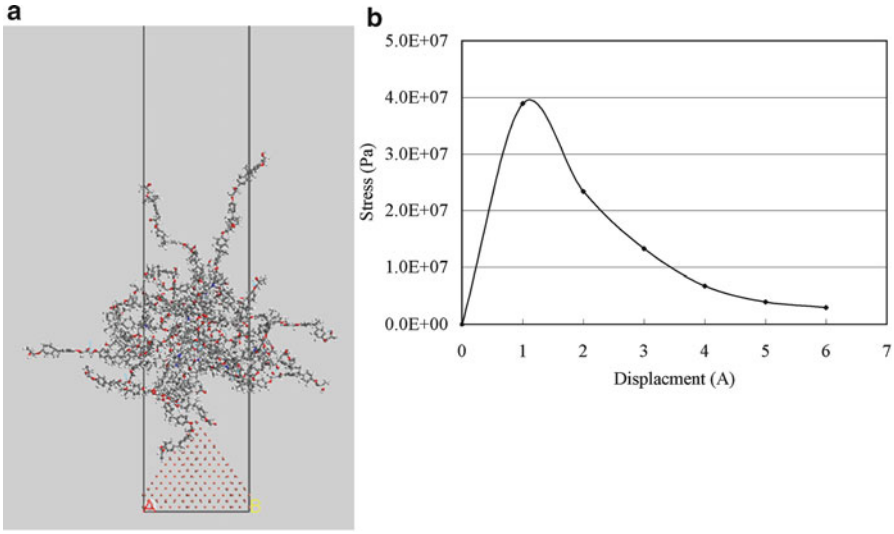


Fig. 10.7 (**a**) MD model of the EMC–Cu system; (**b**) stress–displacement relation for the EMC–Cu system

bi-material system using the ensemble of the constant number of particles, constant volume, and constant temperature (NVT) at 25 °C. Figure 10.7a shows the morphological configuration with the minimum potential energy for the MD model.

Based on the above procedure proposed in Sect. 10.3, the constitutive cohesive relation of the EMC/Cu interface is derived from MD simulations, as shown in Fig. 10.7b. The curve showed the nonlinear behavior of the interface, increasing stress first and then decreasing stress with the increasing displacement. The curve provides the cohesive parameters for cohesive elements.

Tapered double cantilever beam (TDCB) test is carried out to evaluate the tensile adhesion between EMC and copper substrate. In order to study the interfacial delamination of EMC and Cu substrate under mechanical loading, it is necessary to perform finite element analysis to extract some useful information. A more realistic multiscale model of TDCB test is shown in Fig. 10.8a. The mesh was refined at the interface between the EMC and copper to capture the steep stress gradients expected. A pre-crack with a length of 39 mm is made at the interface. Cohesive elements are used at the EMC/Cu interface and the initial thickness of the cohesive elements is set to zero. Both EMC and Cu materials are assumed to be linear elastic, homogeneous, and isotropic. The constitutive relations derived from the interfacial MD model as shown in Fig. 10.8b are assigned to the cohesive zone elements as the description of the atomic interaction between the EMC and copper substrate. The displacements of nodes at the surface of the hole in the bottom block were constrained and tensile displacement was applied on the surface of the top hole.

The tensile force was calculated for the multiscale model under the tensile displacement and plotted against the displacement, as shown in Fig. 10.4. The

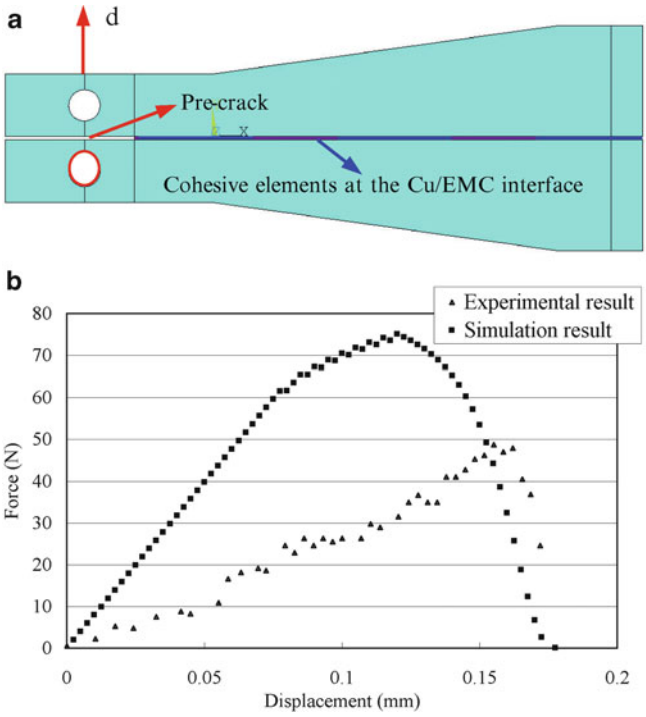


Fig. 10.8 (**a**) The diagram of the TDCB assembled with EMC and copper lead frame; (**b**) force–displacement curve for the EMC–Cu system

tensile force increased with the increased displacement and reached the maximum value where delamination initiated, and then decreased to zero for the remainder of the displacement. The higher maximum tensile force means the higher adhesion between EMC and Cu substrate. Predicted result from TDCB test simulations showed that the adhesion force between EMC- and SAM-treated Cu substrate was higher than that for the control sample. Experimental result is also shown in Fig. 10.8b. It can be seen that the predicted result from simulations was a little bit higher than the experimental result. The difference between the simulation and experimental value can be attributed to more complicated cross-link density of EMC. Moreover, voids or impurity inside the real samples can also degrade the interfacial properties.

10.6 Summary and Discussion

A simple and effective multiscale approach was proposed to study delamination in a bi-material structure, which bridges molecular dynamics method and finite element method using CZM. With proper formulation of the MD model and appropriate use

of boundary conditions, potential functions, and simulation procedure, MD simulation can provide good understanding of delamination at fundamental level, and the parameters of the CZM for delamination propagation.

In contrast to other multiscale methods, the method presented in this study has significant advantages. It avoids the complicated numerical equations to solve the overlapping domain in the method involving coupling of continuum models with molecular models. We also demonstrated a methodology to investigate delamination initiation at the EMC/Cu interface [15], in which the interfacial material properties were derived from atomic force microscopy (AFM) measurements using the Lennard-Jones potential. In that study, we considered only van der Waals force because the adhesion between the EMC and copper was dominated by nonchemical bonding interactions. However, that method is not suitable any more in the above case due to the complicated interfacial bonds between EMC and copper substrate. In this approach, the atomistic behavior is directly transferred from the nanoscale to the continuum scale by the constitutive relation derived from MD simulations; therefore it avoids the suffering from mismatch of timescale occurring at the different length scales. It can also predict the material behavior more accurately than VIB method considering simplified potential energy.

A bifurcation-based multiscale decohesion model was developed by Shen and Chen [24] to investigate delamination between tungsten film and silicon substrate. They conducted MD simulations to obtain decohesion relation of single crystal W block under tensile loading and implemented the model into the material point method (MPM). However, MPM is the method for the size scaling down the continuum level to the atomic level, so size of the model is still within the nanoscale. Moreover, they also argued that the proposed model should be verified by an integrated experimental, analytical, and numerical investigation on the structures with sizes varying from nanoscale to macroscale.

Namilae and Chandra [25] also developed a hierarchical multiscale method to study interfacial shear strength between CNT and its polymer matrix by the CZM parameters. This model had been successfully employed to study the effect of interfacial strength on the elastic properties of the composites. However, they did not provide any experimental evidence for the model that the atomistic behavior of the interface from the MD model was successfully passed on to the continuum model.

Based on the method presented in this study, the atomistic information including deformation, void nucleation, and interfacial debonding were extracted and represented by the constitutive relation. The constitutive relation of the interface of the epoxy resin polymer and Cu substrate was derived from MD simulations under tensile strain and is assigned to the TDCB model to calculate the tensile forces. The predicted results were found to be comparable with those from experimental measurement, which indicates that the proposed approach can be used to study delamination at the interface consisting of nanoscale materials. The approach can be further developed to investigate failures in LED lighting systems.

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References

1. Tanaka G, Goettler LA (2002) Predicting the bonding energy for nylon 6,6/clay nanocomposites by molecular modelling. Polymer 43:541–553
2. Gou J, Minaie B, Wang B, Liang ZY, Zhang C (2004) Computational and experimental study of interfacial bonding of single-walled nanotube reinforced composites. Comput Mater Sci 31 (3–4):225–236
3. Iwamoto N, Moro L, Bedwell B, Apen P (2002) Understanding modulus trends in ultra low k dielectric materials through the use of molecular modeling, proceedings of the 52nd electronic components and technology conference, 28–31 May, San Diego, CA, pp 1318–1322
4. Fan HB, Chan EKL, Wong CKY, Yuen MMF (2006) Investigation of moisture diffusion in electronic packaging by molecular dynamic simulation. J Adhes Sci Technol 20:1937–1947
5. Fan HB, Chan EKL, Wong CKY, Yuen MMF (2007) Molecular dynamic simulation of thermal cycling test in electronic packaging. ASME J Electron Packag 129:35–40
6. Fan HB, Yuen MMF (2007) Material properties of the cross-linked epoxy resin compound predicted by molecular dynamics simulation. Polymer 48:2174–2178
7. Wong CKY, Fan HB, Yuen MMF (2008) Investigation of adhesion properties of Cu-EMC interface by molecular dynamics simulation. IEEE Trans Compon Packag Tech 31:297–308
8. Fan HB, Zhang K, Yuen MMF (2009) The interfacial thermal conductance between a vertical single-wall carbon nanotubes and a silicon substrate. J Appl Phys 106:034307
9. Lidorikis E, Bachlechner ME, Kalia RK, Nakano A, Vashishta P, Voyiadjis J (2001) Coupling length scales for multiscale atomistics-continuum simulations: atomistically induced stress distributions in Si/Si3N4 nanopixels. Phys Rev Lett 87:086104
10. Rudd RE, Broughton JQ (2000) Concurrent coupling of length scales in solid state systems. Phys Status Solidi B 217:251–291
11. Gao H, Klein P (1998) Numerical simulation of crack growth in an isotropic solid with randomized internal cohesive bonds. J Mech Phys Solids 46:187–218
12. Klein P, Gao H (1998) Crack nucleation and growth as strain localization in a virtual-bond continuum. Eng Fract Mech 61:21–48
13. Ji B, Gao H (2004) A study of fracture mechanisms in biological nano-composites via the virtual interbal bond model. Mater Sci Eng A 366:96–103
14. Gao H, Ji B (2003) Modeling fracture in nanomaterials via a virtual internal bond method. Eng Fract Mech 70:1777–1791
15. Fan HB, Wong CKY, Yuen MMF (2006) A multi-scale method to investigate delamination in electronic packaging. J Adhes Sci Technol 20:1061–1078
16. Kendall K (2001) Molecular adhesion and its applications: the sticky universe. Kluwer Academic/Plenum, New York
17. Shet S, Chamdra N (2002) Analysis of energy balance when using cohesive zone model to simulate fracture process. J Eng Mater Tech 124:440–450
18. Xu XP, Needleman A (1994) Numerical simulation of fast crack growth in brittle solids. J Mech Phys Solids 42:1397–1434
19. Camacho GT, Ortiz M (1996) Computational modeling of impact damage in brittle materials. Int J Solids Struct 33:2899–2938
20. Geubelle PH, Baylor J (1998) The impact-induced delamination of laminated composites: a 2D simulation. Compos Part B 29B:589–602
21. Tvergaard V, Hutchinson JW (1992) The relation between crack growth resistance and fracture process parameters in elastic-plastic solids. J Mech Phys Solids 40:1377–1397
22. Needleman A (1990) An analysis of decohesion along an imperfect interface. Int J Fract 42:21–40
23. Alfano G (2006) On the influence of the shape of the interface law on the application of cohesive-zone models. Compos Sci Technol 66:723–730
24. Shen L, Chen Z (2004) An investigation of the effect of interfacial atomic potential on the stress transition in thin films. Model Simulat Mater Sci Eng 12:347–369
25. Namilae S, Chamdra N (2005) Multiscale model to study the effect of interfaces in carbon nanotube-based composites. J Eng Mater Tech 127:222–232

Chapter 11
On the Effect of Microscopic Surface Roughness on Macroscopic Polymer–Metal Adhesion

O. van der Sluis, S.P.M. Noijen, and P.H.M. Timmermans

Abstract Surface roughening is a generally accepted way to enhance adhesion between two dissimilar materials. One of the key mechanisms, besides the obvious increase in surface area, is the transition from adhesive to cohesive failure, i.e., crack kinking. This chapter presents several analysis methods to study this phenomenon. First, a semi-analytical approach is discussed in which the competition between adhesive and cohesive cracking is analyzed by means of the theoretical relation between interface and kinking stress intensity factors. Accordingly, the crack kinking location and kinking angle are readily calculated. Second, transient crack propagation simulations are performed to calculate crack paths at a roughened surface by means of cohesive zone elements. Third, delamination experiments are performed on samples containing well-controlled surface roughness profiles.

11.1 Introduction

Delamination of polymer–metal interfaces is one of the major failure modes occurring in micro- and nano-electronics [1]. Light-emitting devices (LEDs) suffer from delamination as well, mainly due to the fact that transparent materials are needed to pass the light from the device to the surroundings. Using these kinds of materials has a significant impact on the mismatch of material properties. Any gap in the optical pathway will create reflections and, as such, destroy the functionality of the LED package [2]. Figure 11.1 depicts two examples of delamination within LEDs.

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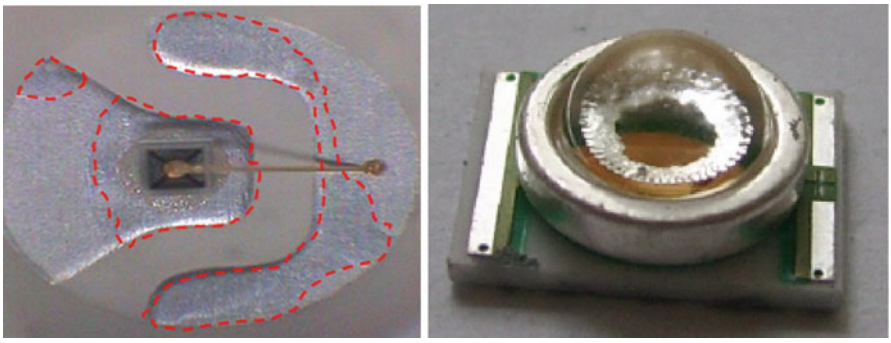


Fig. 11.1 Examples of interfacial delamination in LED packages, with left delamination at the lead frame–epoxy interface [2] and right delamination within the lens system

At the macroscopic scale interface adhesion originates from contributions at different length-scales: (1) chemical interactions such as primary bonds and physical interactions such as secondary bonds at the nanoscale; (2) microscale phenomena due to surface roughness such as crack kinking into the surrounding bulk material, increase in bonding area, plastic dissipation, and fibrillation [3–5]. For polymer–metal interfaces it is known that a major contribution to macroscopic adhesion can be attributed to crack kinking at the roughened interface: the interface crack deflects into the polymer which is driven by the (irregular) geometry of the roughness profile [6]. In fact, the underlying mechanisms include surface increase, mechanical interlocking, and competition between cohesive and adhesive failure around the interface [7–9]. In order to predict the effect of roughness on adhesion it is therefore imperative to take into account the competition between adhesive and cohesive failure in the analysis of the underlying interfacial microstructure.

A semi-analytical approach, based on the pioneering work by He and Hutchinson [10], has been developed in which the competition between adhesive and cohesive cracking is analyzed by means of the theoretical relation between interface and kinking stress intensity factors (SIFs) [11]. The parameters that define this relation, the solution coefficients, are quantified by numerical simulations and formulated in terms of cubic response surface models (RSMs). Accordingly, the crack kinking location and kinking angle are readily calculated for arbitrary material combinations. Next, a numerical approach is applied in which adhesive and cohesive cracking processes are analyzed by transient numerical simulations employing cohesive zone elements. Clearly, the kinking angle and position are direct results of these simulations. To properly deal with the occurrence of limit points during these simulations caused by the brittleness of the interface and bulk materials, a local arc-length solver is employed which is based on the weighted subplane method [12]. In this formulation, the damage in the active cohesive zone elements controls the load in the solution procedure. Finally, experimental analysis is used to study the occurring cracking phenomena in specifically designed bilayer samples containing a well-defined surface roughness.

11.2 The Semi-analytical Approach

This approach is based on the work performed by He and Hutchinson [10, 13, 14] and more recently by Jakobsen et al. [15]. In essence, the method uses the theoretical relation between kinking and interface SIFs for an interface crack of length L between two semi-infinite dissimilar materials 1 and 2, loaded under remote uniform stress σ_{22}^{∞} and σ_{12}^{∞} and normal stress σ_{11} along the interface, and assuming that the kinking crack length a is small with respect to all relevant in-plane length quantities [14]

$$K_I + iK_{II} = cKa^{i\varepsilon} + \overline{d}\,\overline{K}a^{-i\varepsilon} + b\sigma_{11}\sqrt{a}, \tag{11.1}$$

in which (K_I, K_{II}) are the kinking SIFs, K is the complex interface SIF, $(\bar{\cdot})$ denotes complex conjugation, and b, c, d are complex-valued solution coefficients. In [13], tabulated solution coefficients c and d are provided for certain material combinations while [14] includes the parallel normal stress term $b\sigma_{11}$. Upon introducing the kinking crack energy release rate (ERR) into material 2, $G = (K_I^2 + K_{II}^2)(1 - \nu_2^2)/E_2$ and the interface crack ERR $G_0 = (1 - \beta^2)(K_1^2 + K_2^2)/E_*$ with $E_*^{-1} = (\overline{E}_1^{-1} + \overline{E}_2^{-1})/2$ the criterion for crack kinking from an initially delaminated area can be written as [16]

$$G_R \equiv \frac{G}{G_0} > \frac{\Gamma_k}{\Gamma_i(\psi)} \equiv \Gamma_R, \tag{11.2}$$

where Γ_k is the fracture toughness of material 2 and $\Gamma_i(\psi)$ corresponds to the interface toughness, while ψ denotes the mode angle. In [11], the dependency of G_R-values for different mode angles, kinking angles, kinking crack lengths, and Dundurs' parameter values is illustrated. The tabulated solution coefficients of He and Hutchinson [13] are based on numerical solutions of singular integral equations resulting from a basic solution for an edge dislocation in material 2 under the assumption that $L \gg a$. The tables restrict crack kinking predictions to the available tabulated material combinations and kinking angles. In order to generalize the tabulated solution coefficients, it is therefore proposed to derive an analytic expression that renders solution coefficients for any material combination (α, β) and kinking angle ω. A finite element (FE) procedure is employed here to determine the solution coefficients (b, c, d) for any (α, β, ω) combination. To this end, the method proposed by Jakobsen et al. [15] is slightly adapted. Response surface modeling is utilized to derive empirical equations describing the aforementioned dependency. To establish the solution coefficients, the SIFs are calculated for three mode angles which results in the following system of equations [5]:

$$\begin{bmatrix} \Re(c(\omega)) \\ \Im(c(\omega)) \\ \Re(d(\omega)) \\ \Im(d(\omega)) \\ \Re(b(\omega)) \\ \Im(b(\omega)) \end{bmatrix} = \begin{bmatrix} f_1^{\psi_1} & -f_2^{\psi_1} & f_1^{\psi_1} & -f_2^{\psi_1} & f_3^{\psi_1} & 0 \\ f_2^{\psi_1} & f_1^{\psi_1} & -f_2^{\psi_1} & -f_1^{\psi_1} & 0 & f_3^{\psi_1} \\ f_1^{\psi_2} & -f_2^{\psi_2} & f_1^{\psi_2} & -f_2^{\psi_2} & f_3^{\psi_2} & 0 \\ f_2^{\psi_2} & f_1^{\psi_2} & -f_2^{\psi_2} & -f_1^{\psi_2} & 0 & f_3^{\psi_2} \\ f_1^{\psi_3} & -f_2^{\psi_3} & f_1^{\psi_3} & -f_2^{\psi_3} & f_3^{\psi_3} & 0 \\ f_2^{\psi_3} & f_1^{\psi_3} & -f_2^{\psi_3} & -f_1^{\psi_3} & 0 & f_3^{\psi_3} \end{bmatrix}^{-1} \begin{bmatrix} K_I^{\psi_1}(\omega) \\ K_{II}^{\psi_1}(\omega) \\ K_I^{\psi_2}(\omega) \\ K_{II}^{\psi_2}(\omega) \\ K_I^{\psi_3}(\omega) \\ K_{II}^{\psi_3}(\omega) \end{bmatrix}, \tag{11.3}$$

with $f_1^{\psi_i} = K_1^{\psi_i} \cos(\varepsilon \ln a) - K_2^{\psi_i} \sin(\varepsilon \ln a)$, $f_2^{\psi_i} = K_1^{\psi_i} \sin(\varepsilon \ln a) + K_2^{\psi_i} \cos(\varepsilon \ln a)$, and $f_3^{\psi_i} = \sqrt{a}\sigma_{11}^{\psi_i}$. The only requirement for this system to be regular is $\psi_1 \neq \psi_2 \neq \psi_3$ and $\sigma_{11} \neq 0$ for at least one loading condition. In [11], the accuracy and wide range of applicability of this method are proven by means of two benchmark cases: an isolated and a finite interface crack.

FE analysis is required to calculate the SIFs and ERR of an interfacial crack accurately for arbitrary geometries and loading conditions. Consequently, K_I and K_{II} of the kinking crack are calculated by means of (11.1). Performing these calculations analytically for different kinking angles gives G_R as function of ω. By applying the kinking condition (11.2), it is determined if crack kinking occurs and at which angle ω_k. This semi-analytical approach to perform crack kinking analysis by a combination of FE calculations for the interface crack and analytic equations has been generalized by constructing RSMs that make the solution coefficients immediately available as function of α, β, and ω.

As indicated in [16], physically admissible material combinations in plane strain are restricted to $\alpha \in [-1, 1]$ and $(\alpha - 4\beta) \in [-1, 1]$. A design of experiments (DOE) is set up to derive solution coefficients for these material combinations with $\omega = \pm$ [20°, 40°, 60°, 80°, 100°]. For each material combination FE simulations consisting of stress simulations to determine σ_{11}, interface crack SIF calculations, and kinking crack SIF calculations are performed for three loading conditions. Solution coefficients for a total of 1250 α, β, and ω combinations are determined. Cubic RSMs including interaction terms for each solution coefficient for all α, β, and ω are established.

Now that expressions are available that couple the solution coefficients to the material combinations and kinking angle, only the ERR and stress state of an interfacial crack need to be determined numerically to find G_R.

Figure 11.2 shows the resulting G_R values as a function of ω for the case of an isolated interface crack for different material combinations. From these results, it can be concluded that the semi-analytical results reflect the FE values rather well with a maximum error of about 5 %. For Cu/MC and Cu/EP, kinking is most likely to occur at 85° for the used loading conditions. It can thus be concluded that the semi-analytic approach is a very cost-effective method to perform crack kinking analyses at interface cracks. It must be noted, however, that the accuracy by utilizing the RSM is limited to approximately 95 % of FE analysis. In cases that a higher accuracy is required it is recommended to recalculate the solution coefficients of the particular problem. More details can be found in [11].

11.3 The Transient Numerical Approach

In this section the geometrical effect of roughness is analyzed by means of FE simulations in which the interface topology follows from measured roughness profiles and includes transient simulation of adhesive and cohesive failure using cohesive zone elements. Figure 11.3a shows an FE model of a surface profile taken

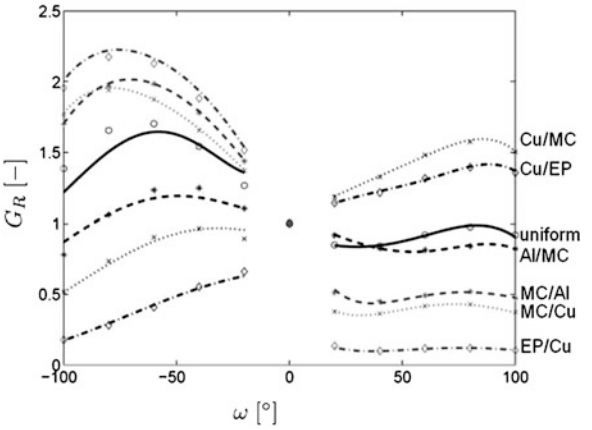


Fig. 11.2 Validation of semi-analytic approach by comparison of FE (*symbols*) and semi-analytic (*lines*) G_R values for different metal–polymer bi-materials and one loading situation

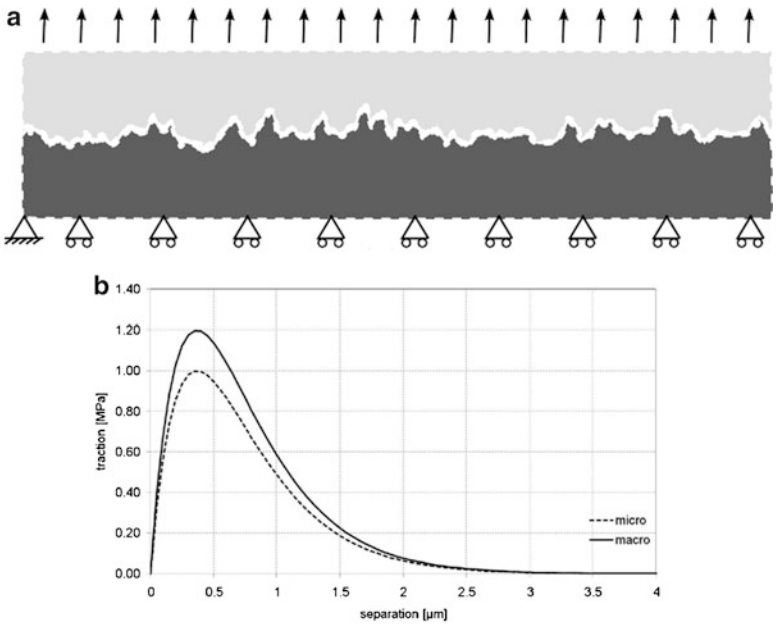


Fig. 11.3 (**a**) 2D microscale plane strain model for a measured surface roughness under mode I loading conditions; (**b**) microscale and macroscale traction–separation curves for a rough interface

from a white light interferometer measurement of a copper lead frame with an accuracy of 0.5 μm, which is well below the typical size of the measured roughness of $R_a = 4.1$ μm. Clearly, surface cavities cannot be detected by this measurement technique.

It appears that the length of the actual profile L is approximately 20 % higher than the length of the straight profile L_0. Now, if the surface is subjected to a vertical tensile force F_y, the macroscopic interface toughness increases by a factor L/L_0 (similar to the Wenzel factor $r = A/A_0$ [17]), assuming that the interface properties at this scale are indeed mode independent and no cavities causing interlocking are present. In the model, mode I loading is prescribed while interface delamination is described by cohesive zone (CZ) elements employing an exponential Smith–Ferrante law [18]. At this analysis scale, the interface properties are only due to chemical and physical interactions which can be found by molecular simulations (e.g., [19]) or by experiments (e.g., [20]). The bottom metal layer is constrained in vertical direction while at the top polymer layer a vertical displacement is prescribed. The macroscale tractions are calculated by summation of the nodal reaction forces at the top edge of the microscale model divided by the width; see Fig. 11.3b. The increase of interface toughness for the rough surface is apparent.

To include bulk fracture into the simulations, cohesive zone elements are dynamically inserted into the bulk mesh (e.g., [21]) during the simulation based on the following criterion:

$$\left[\frac{\sigma_n}{S_n}\right]^{x_n} + \left[\frac{\sigma_t}{S_t}\right]^{x_t} \geq 1, \tag{11.4}$$

if $\sigma_n > 0$. In this equation, σ_n and σ_t are the normal and tangential stresses, respectively. S_n and S_t correspond to the fracture strength values in normal and tangential direction while x_n and x_t are the respective exponents. To avoid numerical issues typical for cohesive zone simulations for brittle fracture processes, a robust local arc-length solver is applied which is based on the weighted-subplane method [12]. Here, the damage in cohesive zone elements controls the load in the solution procedure. To illustrate the impact of the loading conditions on the resulting crack path, normal and peel boundary conditions are prescribed on a small part of the roughness model from Fig. 11.3a. It is remarked that for the purpose of illustration, the kinking location in both simulations is fixed. From the crack path predictions illustrated in Fig. 11.4, the effect of the boundary conditions is evident. Normal loading results in a more or less horizontal crack path including vertical deviations that are clearly caused by the roughness profile. On the other hand, peel loading results in a more vertically directed crack path into the polymer. Obviously, the complete range of mode mixities should be prescribed on this model to arrive at a macroscopic mode-dependent traction-separation law (TSL).

Future work will focus on the effect of different microscopic TSLs, addition of plasticity in the metal, and friction at the interface to arrive at macroscopic interface properties as function of roughness geometry and mode angle.

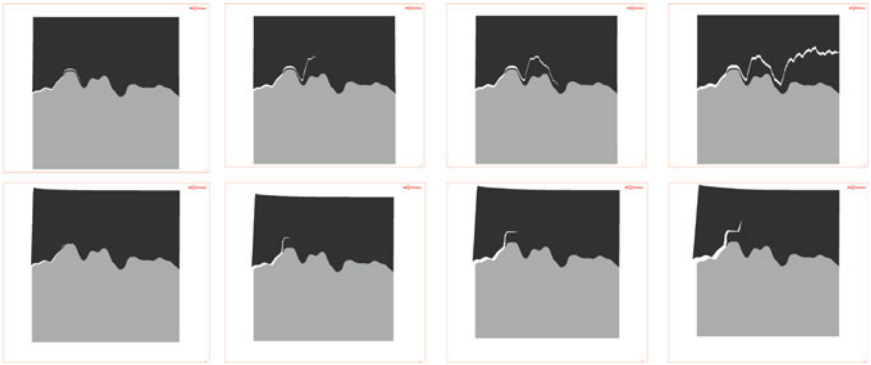


Fig. 11.4 Crack path predictions for normal (*top figures*) and peel (*bottom figures*) loading conditions (deformation scale factor: 10)

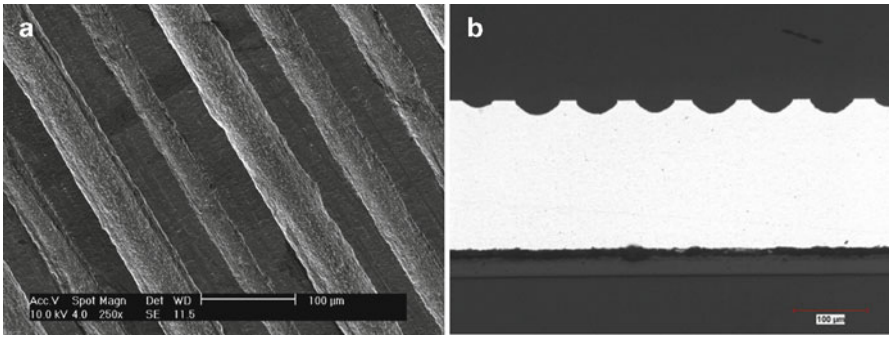


Fig. 11.5 (**a**) Top view and (**b**) cross section of samples containing predefined roughness

11.4 Experimental Validation Procedure

The stochastic nature of roughness prohibits quantitative experimental validation of the numerically determined deterministic crack paths. Alternatively, it is proposed to perform interface delamination experiments on samples containing controlled 2D roughness profiles as illustrated in Fig. 11.5. For this purpose, a 0.2 mm thick copper lead frame was structured with roughness grooves by using a spray etching process combined with a specifically designed mask. In this way, different groove widths and pitches were processed. The structured lead frames were cleaned using a sulfuric acid dip and plasma prior to molding of a 0.5 mm layer of EMC on top of the lead frame. The EMC is molded at 180 °C and 180 bar during 180 s of which 45 s is pressure buildup time. A post-mold cure step at 175 °C during 4 h was performed. The resulting structured bi-material layer was laser cut into strips suitable for 4PB tests with dimensions $50 \times 8 \times 0.7$ mm^3. A pre-notch in the EMC was applied to trigger crack propagation at the interface.

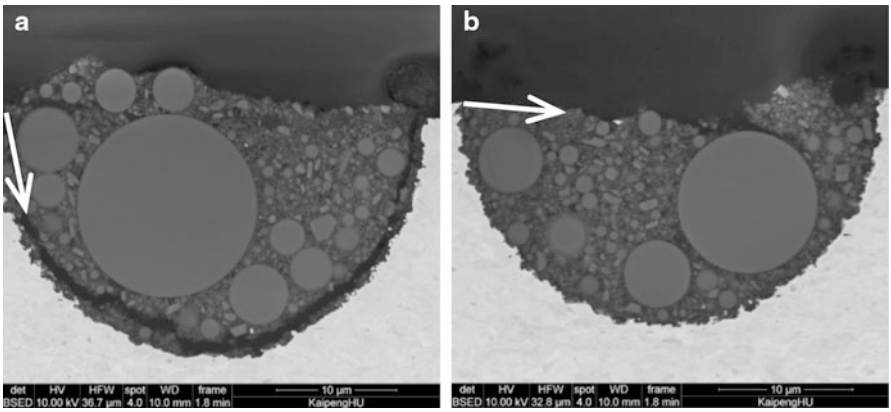


Fig. 11.6 Cross sections illustrating the occurrence of (**a**) adhesive and (**b**) cohesive failure. The *white arrows* indicate the direction of the failure paths

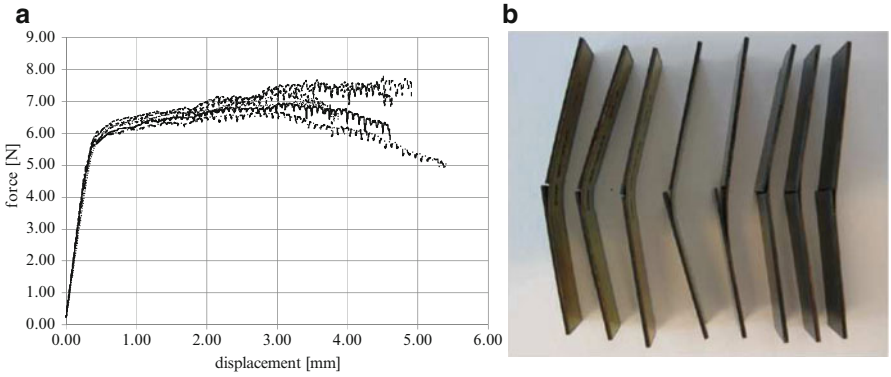


Fig. 11.7 Four-point bending results: (**a**) force–displacement curves and (**b**) deformed samples after testing illustrating the occurrence of plastic deformation

Failure analysis of the delaminated metal and polymer surfaces after four-point bending shows that kinking indeed occurs. In Fig. 11.6, cross sections are shown which confirm that both adhesive (Fig. 11.6a) and cohesive (Fig. 11.6b) failure modes take place during testing as indicated by the arrows in the pictures. It is remarked that these results are preliminary and require more in-depth study.

Figure 11.7a shows several force–displacement curves obtained from the four-point bending experiments. It can be easily observed that the typical 4PB shape is not recovered. Instead, two regions are recognized:

1. Initial stiffness regime due to bending of the sample
2. Delamination regime during which the force remains constant, increases, and/or decreases

The first region is relatively straightforward and is only influenced by the mechanical properties of both materials, the dimensions of the sample and the initial crack geometry. The second part is more complex: the classical solution exhibits a steady-state solution rendering a constant plateau force which can be used as direct measure for the (steady-state) interface toughness [22]. Alternatively, the second part exhibits an increasing and/or decreasing force level during delamination.

From numerical analysis, several mechanisms have been identified that could contribute to the force–displacement curves obtained by four-point bending:

- Increasing mode angle during testing caused by a higher shear stress-to-normal stress ratio [22] which results in an increasing interface toughness, and thus a force increase.
- Decrease of effective span length due to sample sliding over the supports during testing results in a force increase, even without an increasing interface toughness.
- Increasing plastic deformation during testing (as illustrated in Fig. 11.7b) which might result in a force increase.
- Large bending displacements which result in a force decrease even without a decreasing interface toughness: numerical analysis reveals that forces decrease when taking into account large displacements in the simulation. This effect is more pronounced with increasing interface toughness values as in this case, larger displacements are required to achieve actual interface delamination.
- Asymmetric interface crack propagation due to asymmetry of the initial crack with respect to the lead frame grooves could result in a nonsteady-state crack propagation and consequently, in a nonconstant force.

Although it is currently believed that a delicate interplay exists between the above-mentioned phenomena, due to the preliminary character of the presented results, more in-depth study is required to adequately explain the reasons for the difference in increasing and decreasing forces during the four-point bending test.

11.5 Conclusions

In this chapter, a concise overview was presented concerning our ongoing effort to fundamentally understand the mechanisms of polymer–metal interface failure at microscopic scale. The enhancement of adhesion properties due to roughness is considered to be caused by surface increase and deviation of the interface crack into the polymer. This crack kinking was analyzed by means of a semi-analytical approach and by transient numerical calculations. Finally, an experimental validation procedure was discussed to quantitatively validate the numerically predicted crack paths by considering well-defined 2D surface roughness profiles of which first preliminary results were presented. It is remarked that due to the complexity of the

underlying phenomena, more in-depth study is required to arrive at a quantitative prediction of the effect of roughness on macroscopic adhesion properties.

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References

1. Zhang GQ, van Driel WD, Fan XJ (2006) Mechanics of microelectronics. Springer, Berlin
2. Hu JZ, Yang LQ, Hwang WJ, Shin MW (2006) Thermal and mechanical analysis of delamination in GaN-based light-emitting diode packages. J Cryst Growth 288:157–161
3. Buehler MJ (2008) Atomistic modeling of materials failure. Springer, New York, NY
4. Evans AG, Rühle M, Dalgleish BJ, Charalambides PG (1990) The fracture energy of bimaterial interfaces. Mater Sci Eng 126:53–64
5. Van der Sluis O, Hsu YY, Timmermans PHM, Gonzalez M, Hoefnagels JPM (2011) Stretching induced interconnect delamination in stretchable electronic circuits. J Phys D: Appl Phys 44:034008
6. Qu J (2003) Thermomechanical reliability of microelectronic packaging. In: Milne I, Ritchie RO, Karihaloo B (eds) Comprehensive Structural Integrity, Pergamon, Oxford, 219–239, ISBN: 9780080437491
7. Devries KL, Adams DO (2002) Mechanical testing of adhesive joints. In: Dillard DA, Pocius AV (eds) The mechanics of adhesion. Elsevier Science, The Netherlands
8. Yao Q, Qu J (2002) Interfacial versus cohesive failure on polymer–metal interfaces in electronic packaging effects of interface roughness. J Electron Packaging 124:127–134
9. Zavattieri PD, Hector LG Jr, Bower AF (2008) Cohesive zone simulations of crack growth along a rough interface between two elastic–plastic solids. Eng Fracture Mech 75:4309–4332
10. He MY, Hutchinson JW (1989) Kinking of a crack out of an interface. J Appl Mech 111:270–278
11. Noijen SPM, van der Sluis O, Timmermans PHM, Zhang GQ (2012) A semi-analytic method for crack kinking analysis at isotropic bi-material interfaces. Eng Fracture Mech 83:8–25
12. Geers MGD (1999) Enhanced solution control for physically and geometrically non-linear problems. Part I – the subplane control approach. Int J Numer Meth Eng 46:177–204
13. He MY, Hutchinson JW (1989) Kinking of a crack out of an interface: tabulated solution coefficients. Technical report, Harvard University
14. He MY, Bartlett A, Evans AG, Hutchinson JW (1991) Kinking of a crack out of an interface: role of in-plane stress. J Am Ceram Soc 74:767–771
15. Jakobsen J, Andreasen JH, Bozhevolnaya E (2008) Crack kinking of a delamination at an inclined core junction interface in a sandwich beam. Eng Fracture Mech 75:4759–4773
16. Hutchinson JW, Suo Z (1991) Mixed mode cracking in layered materials. Adv Appl Mech 29:63–191
17. Packham DE (2003) Surface energy, surface topography and adhesion. Int J Adhesion Adhesives 23:437–448
18. Van Hal BAE, Peerlings RHJ, Geers MGD, van der Sluis O (2007) Cohesive zone modeling for structural integrity analysis of IC interconnects. Microelectron Reliab 47:1251–1261
19. Yarovsky I (1997) Atomistic simulation of interfaces in materials: theory and applications. Aust J Phys 50:407–424

20. Hölck O, Bauer J, Wittler O, Land K, Michel B, Wunderle B (2011) Experimental contact angle determination and characterisation of interfacial energies by molecular modelling of chip to epoxy interfaces. In: Proceedings of ECTC 2011, Florida
21. Prechtel M, Leiva Ronda P, Janisch R, Hartmaier A, Leugering G, Steinmann P, Stingl M (2011) Simulation of fracture in heterogeneous elastic materials with cohesive zone models. Int J Fracture 168:15–29
22. Charalambides PG, Lund J, Evans AG, McMeeking RM (1989) A test specimen for determining the fracture resistance of bimaterial interfaces. J Appl Mech 56:77–82

Chapter 12
An Introduction to System Reliability for Solid-State Lighting

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Abstract Solid-State Lighting (SSL) applications are slowly but gradually pervading into our daily life. An SSL system is composed of an light-emitting diode (LED) engine with a microelectronic driver(s) in a housing that also supplies the optic design. Knowledge of system-level reliability is crucial for the business success of future SSL systems, and also a very scientific challenge. In practice, a malfunction of the system might be induced by the failure and/or degradation of the subsystems/interfaces. Extra costs, in terms of exceed efforts/designs/parts, have been applied to the system in order to secure the guaranteed reliability performance of SSL system. Most SSL system designs allow few failures of the subsystem/interface during the application period. Hence, a significant cost reduction can be achieved when the system-level reliability is well understood by proper experimental and simulation techniques. This chapter covers the reliability of total SSL systems including the reliability theories and practices for all (sub) components, such as LED engines, drivers, and fixtures.

12.1 Introduction

Solid-State Lighting (SSL) is slowly but gradually pervading into our daily life. At present, light-emitting diode (LED) lighting systems in various shapes are developed and designed for general lighting, advertisement, emergency lighting, and architectural markets. LED-based illumination systems have long surpassed the traditional incandescent light sources in efficiency and reliability and have achieved

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good color rendering. Significant penetration into the general lighting market is mainly due to the costs. Adding to that, recent increases in efficiency (approx. 75%), reliability (approx. 50,000 h) and power density (approx. 100 lm/W) offer higher lumens per Euro. About 15% of the world's total consumed energy is used for artificial lighting. Artificial lighting is extremely inefficient, for example incandescent lamps with about 5% and fluorescent lamps with 20% efficiency. SSL is based on semiconductor materials and processes, and has potential to achieve far higher efficiencies, possibly more than 90%. Long useful lifetimes of 50,000 h (or more) and high efficacy are major benefits of SSL applications. In other words: SSL applications are now at the doorstep of massive market entry into offices and homes.

In engineering, reliability is the ability of a system or a component to perform its required functions under stated conditions for a specified period of time. It is often reported in terms of a probability [1–8]. It is very challenging to understand and predict the reliability of a macro-level system, because reliability is always a multidisciplinary issue, and strongly associated with materials, design, manufacturing process, testing, and application conditions. System reliability, herein, mainly addresses the reliability of all components of the system, and is even more challenging. It needs not only new fundamental theory and methodology, but also different techniques, be it experimental and/or numerical, and engineering practices to deal with the new behavior and characteristics of the total system. Due to the relatively short period of time for technology and industrial development, system reliability is a young scientific playground with limited knowledge, but tremendous opportunities for creativity, innovation, and new business development. This chapter describes system-level prediction methods for SSL applications. The first paragraph discusses the definition of an SSL system, and the second one the principles of system reliability. The fourth paragraph describes the statistical backgrounds for system reliability. Industrial cases are described in the fifth paragraph. The chapter ends with conclusions and recommendations.

12.2 Solid-State Lighting Systems

What is an SSL system? This question needs to be answered before we can go forward in this chapter. The word system originates from the Latin systēma, in turn from Greek σύστημα systēma, and described as "whole compounded of several parts or members, system," and literary means composition [9]. The commonly used description of a system is given as follows [10]:

- System: A set of interacting or interdependent system components forming an integrated whole.

This implicates that two components together already form a system, be it the simplest that one can think off. When the number of components and their interactions



Fig. 12.1 SSL applications, with (**a**) LED package, (**b**) LED retrofit bulb, (**c**) LED puck, (**d**) LED indoor luminiare, (**e**) living house with LED lighting, and (**f**) city of Shanghai with LED street lighting

significantly increase, the so-called large or complex systems are formed. The commonly used description of a large or complex system is given as follows [11]:

- A complex system: A system composed of interconnected parts that as a whole exhibit one or more properties (behavior among the possible properties) not obvious from the properties of the individual parts.

A system's complexity may be of one of the two forms: disorganized complexity and organized complexity [12]. In essence, disorganized complexity is a matter of a very large number of parts, and organized complexity is a matter of the subject system (quite possibly with only a limited number of parts) exhibiting emergent properties. Examples of complex systems include ant colonies, human economies and social structures, climate, nervous systems, cells and living things, including human beings, as well as modern energy or telecommunication infrastructures.

Back to SSL systems, Fig. 12.1 shows different possible SSL applications, ranging from an LED package, an LED retrofit bulb, an LED puck, an LED indoor luminaire, and living house with light and total city that needs to be lighted. Even an LED package can be seen as a system since it is composed of several interacting components, being the LED device of chip: the lens on top and the (ceramic) carrier below. A retrofit bulb adds to that a driver, the housing, and a thermal solution (mostly heat sink). Pucks are another form of the housing in which typically over ten LED packages are mounted. When several pucks are combined, a luminaire is formed. A luminaire may contain a controller. A typical household nowadays consists of over 30–40 light engines: they could be controlled from a central

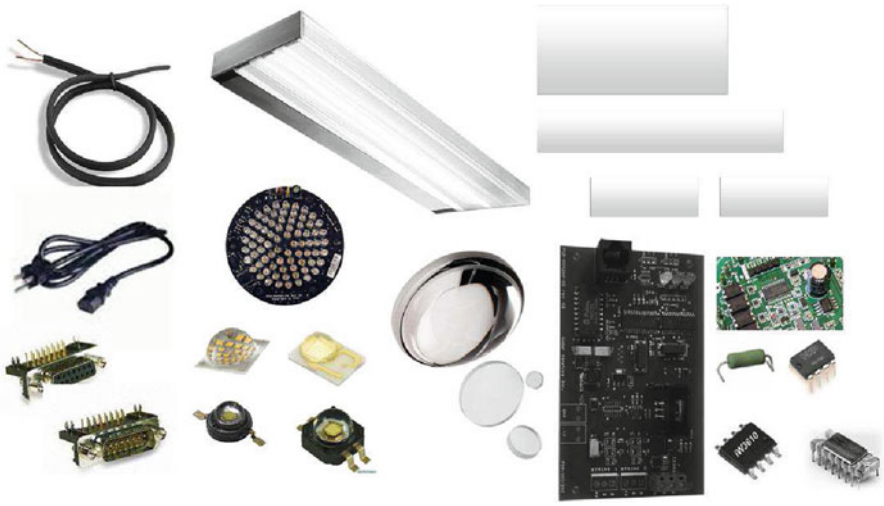


Fig. 12.2 Breakdown of an SSL system into the key components

place. Finally, the city of Shanghai consists of millions of streets and indoor lighting engines. Only the latter one can be seen as a complex or a large system.

As mentioned above a system is composed of components and the question is then raised: What are the components in an SSL system? The breakdown of a typical SSL system is depicted in Fig. 12.2. Key components in an SSL system can be distinguished as being:

1. LED packages
2. Interconnects (solders, thermal interface materials, and substrates)
3. Male/female connectors
4. Electronics
5. Cooling systems
6. Optics (includes remote phosphors, lenses and coating systems, reflectors and reflective and hard coating systems, paints—if present internally)
7. Gaskets, feed troughs, and sealants
8. Fastening systems

12.3 System Reliability

Many textbooks are available that describe reliability principles, ranging from its history (accelerated), testing, system reliability, and reliability predictions to reliability standards [2, 3, 5, 6, 13–21]. It is not the intention to repeat and/or summarize this extensive number of published pages in this paragraph. A very good reference on system reliability is written by Marvin Rausand, 2nd edition in 2004 [14], being part of a larger series on probability and statistics. In this paragraph only the basic principles and those detailed reliability theories that are important for SSL systems are discussed.

12.3.1 Generic Principles

As mentioned before, a system is a collection of components, subsystems, and/or assemblies arranged to a specific design in order to achieve desired functions with acceptable performance and reliability. The types of components, their quantities, their qualities, and the manner in which they are arranged within the system have a direct effect on the system's reliability. Often, the relationship between a system and its components is misunderstood or oversimplified. For example, the following statement is not valid: *all of the components in a system have a 90% reliability at a given time; thus the reliability of the system is 90 % for that time*. Unfortunately, poor understanding of the relationship between a system and its constituent components can result in statements like this being accepted as factual, when in reality they are false. The commonly used description for system reliability is given as follows:

- System reliability: The probability that a system, including all hardware, firmware, and software, will satisfactorily perform the task for which it was designed or intended, for a specified time, and in a specified environment.

  Which is in compliance with the one mentioned in [14]:

- System reliability: The ability of an item to perform a required function, under given environmental and operational conditions and for a stated period of time (ISO 8402).

Here, the term "item" is used to denote any component, subsystem, or system that can be considered as an entity. Using the same analogy the required function may be a single function or a combination of functions that is necessary to provide a specified service. From a system reliability point of the view, the challenge is to master the reliability of all these components. Clearly, each system, whatever the complexity, can just last as long as its lowest life component (see Fig. 12.3 for the implications in SSL). The reliability may be measured in different ways depending on the particular situation; examples are:

– Mean time to failure (MTTF)
– Number of failures per time unit (failure rate or field call rate)
– The probability that the item does not fail in a time interval (0, t] (survival probability)
– The probability that the item is able to function at time t (availability at time t)

If the item is not repaired after failure, the 3rd and 4th situations coincide. For precise mathematically definitions please refer to [14]; it is not the intention to repeat it in this book/chapter.

Whatever the complexity of the system, its reliability is determined by its components and the interaction between them. Figure 12.4 schematically presents this principle: based on the failure mode i in component c its distribution is the input for the system simulator. With the user conditions from the application point of



Fig. 12.3 The challenge in SSL system reliability: cover all levels from the materials to the (sub) components to the (complex) system

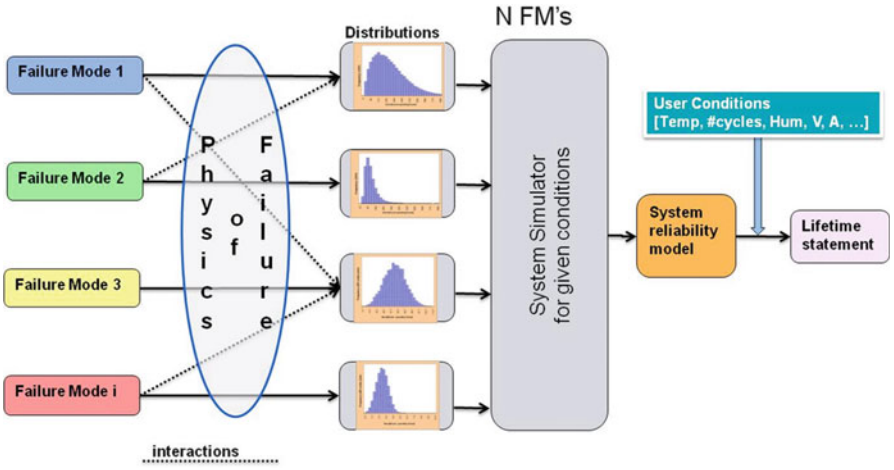


Fig. 12.4 Basic diagram for system reliability

view, one can create a lifetime statement. Investigations into the physics of failure are needed to understand the failure modes (read mechanisms), combined with any sort of testing. Verification testing is needed on a product level. In the next paragraphs, testing and prediction methods are further described.

12.3.2 System Reliability Testing

To cover system reliability one would need to test the reliability performance of both the components and the total system. If the total system is aimed for long lifetimes, which is the case for SSL systems, a common way of tackling this requirement is to expose the device to sufficient overstress to bring the time to failure to an acceptable level. Thereafter one tries to "extrapolate" from the information obtained under overstress to normal-use conditions. Depending on the kind of device in question, the accelerated testing conditions may involve a higher level of temperature, pressure, voltage, load, vibration, and so on than the corresponding levels occurring in normal-use conditions. These variables are called stressors. This approach is called accelerated life testing (ALT) or overstress testing. A very good reference on accelerated testing is written by Nelson [13], 2004 version. However, acceleration on a system level is not without risk. Overstress by simply increasing the loads, for example temperature or electrical power, may drive certain components to new and/or unwanted failure modes that have relevance to the actual field performance. There, acceleration should be taken with precautions. Some generic rules for that are the following:

- Find your system stressors
  - Field studies or application studies are needed to determine the so-called mission profile or user profile of the product.
  - For SSL products, known stressors are temperature, relative humidity, mechanical forces like vibrations and shocks, electricity, and, not to forget, light.
- In principle: A component failure $\neq$ a system failure
  This particularly holds for SSL products since if one LED is broken it does not mean that the total light output on a system level is insufficient.
- Each component in a system exhibits its own failure behavior, and needs to be captured by:
  - Experiments by using at least three accelerated testing conditions
  - Numerical/analytical models that describe the reliability physics or physics of failure [16]
- Interactions between the components need to be captured by:
  - Testing subsystems
  - Testing the total system
  - Accelerating environmental user conditions in a physically correct manner

In most industries, standard tests are used in order to quantify the reliability performance of the (sub) components and systems. Examples are the MIL standards for military and the JEDEC standards for electronics. For SSL applications, LM79

and LM80 are leading [17, 18]; however system reliability is not a well-covered topic yet. There are basically two different reliability test approaches:

– Test-to-pass
  Test-to-pass, demonstration testing, or zero failure acceptance testing is an approach in which a certain number of test cycles is needed without the occurrence of failures. Test-to-pass only provides pass–fail results; the results do not give any information with respect to the reliability as a function of time (or kilometers or cycles). These limitations are addressed by test-to-failure.
– Test-to-failure
  Test-to-failure is an approach in which the tests are continued until at least 65% of the population failed. This approach will give full information on failure modes, but the limitation could be long duration of the test.

For key components in any system, it is advised to follow a test-to-fail approach, preferable using meaningful accelerated tests. For systems, a test-to-pass approach is advised for product release and a test-to-fail approach for product development.

12.3.3 System Reliability Prediction

In (system) reliability one will always have to work with models of the system. In practical situations the analyst will have to derive (stochastic) models of the system at hand, or at least have to choose from several possible models before an analysis can be performed. To be "realistic" the models must describe the essential features of the system, but do not necessarily have to be exact in all details. Always bear in mind that one is working with an idealized, simplified model of the system. Take for example the electronic industry. For electronic devices a wide range of reliability prediction methods is available today [19–29]. Traditional handbook-based reliability prediction methods for electronic products include Mil-Hdbk-217, Telcordia SR-332 (formerly Bellcore), PRISM, FIDES, CNET/RDF (European), and the Chinese GJB-299. These methods rely on analysis of failure data collected from the field and assume that the components of a system have inherent constant failure rates that are derived from the collected data. Reliability calculated using these commonly used methods may vary with factors up to 100 [25]. The root cause for the prediction inaccuracy lies in the fact that many of the first-order effect stressors are not explicitly included in the prediction methods. These stressors include thermal cycling, temperature change rate, mechanical shock, vibration, power on/off, and/or supplier quality difference. In addition these prediction models are not frequently updated with reliability improvement with respect to calendar years and ageing trends. Any one of these stressors neglected could cause a variation in the predicted reliability by several factors. Correctly finding the system stressors is not always easy and some of them or the precise impact of them might be easily overlooked.

Much literature is available on the prediction of system reliability; it is not the intention to summarize or to repeat. In the next chapter more details are described on the application of system reliability prediction technique suitable for SSL products.

Reliability block diagrams are described as a means to represent the logical system architecture and create system reliability models. Possible logical structures are serial, parallel, and/or combinations of these two. In a serial structure with n independent components, the system reliability is calculated as the multiplication of the individuals:

$$R_{\text{total}} = \prod_{i=1}^{n} R_i. \tag{12.1}$$

Consider a series structure of four independent components. At a specified point of time the component reliabilities are $R1 = R2 = 0.99$, $R3 = 0.97$, and $R4 = 0.94$. The system reliability at time t is then equal to $0.99 \times 0.99 \times 0.97 \times 0.94 = 0.89$. In a serial system, the product is at most as reliable as the *least* reliable component.

In a parallel structure with n independent components, the system reliability is calculated as

$$R_{\text{total}} = 1 - \prod_{i=1}^{n} (1 - R_i). \tag{12.2}$$

Consider a parallel structure of four independent components. At a specified point of time the component reliabilities are $R1 = R2 = 0.99$, $R3 = 0.97$, and $R4 = 0.94$. The system reliability at time t is then equal to $1 - (1 - 0.99) \times (1 - 0.99) \times (1 - 0.97) \times (1 - 0.94) = 0.999$. So, parallel systems are in principle more reliable than serial systems.

Most systems, for sure SSL systems, comprise a combination of serial and parallel structures (or components). It will make the structure functions more complex. The complexity increases even more when redundancy is present, when product repair is an option, and/or when interactions play a dominant role (meaning that the assumptions of independency disappear). In such cases it becomes inevitable to use dedicated software to determine the structural diagram of the system and calculate its reliability. In the following, three basic system reliability principles are highlighted.

1. Fault trees
   Fault-tree analysis (FTA) is a deductive methodology to determine the potential causes of failures and to estimate the failure probabilities [30]. FTA addresses system design aspects and potential failures, tracks down system failures deductively, describes system functions and behaviors graphically, focuses on one error at a time, and provides qualitative and quantitative reliability analyses. The purpose of a fault tree is to show the sets of events—particularly the primary failures—that

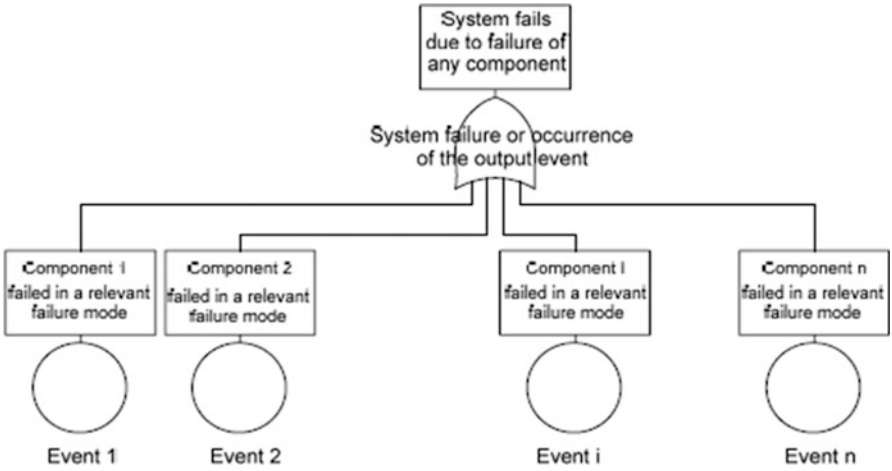


Fig. 12.5 Fault tree example: representation of a serial system [30]

will cause the top event in a system. FTA is often applied to the safety analysis of systems (such as transportation systems, power plants, or any other systems that might require evaluation of safety of their operation). FTA can be also used for availability and maintainability analysis. FTA is used by many industries and therefore it is standardized by the IEC committee [30]. There are basically two FTA techniques available: qualitative and quantitative. In the qualitative approach the probability of events and their contributing factors—input events—or their frequency of occurrence is not addressed. It is largely used in nuclear industry applications and many other instances where the potential causes or faults are sought out, without interest in their likelihood of occurrence. The second approach, adopted by many industries, is largely quantitative, where a detailed FTA models an entire product, process, or system, and the vast majority of the basic events, whether faults or events, has a probability of occurrence determined by analysis or test. In this case, the final result is the probability of occurrence of a top event representing reliability or probability of a fault or a failure. In an FTA, standard symbols to denote the so-called events and gates are used to calculate the failure probability of the system. An example FTA is depicted in Fig. 12.5.

Note that fault trees provide with a static (in time) representation of the reliability of the system. By taking advantage of their graphical notation they also provide with a good description of the logic of the system.

2. Markov Chains

A Markov Chain is a stochastic process that describes transitions in time between a discrete number of states. Markov Chains, named for Andrey Markov, are a mathematical system that undergoes transitions from one state to another, between a finite or countable number of possible states [31]. Markov Chains have many applications as statistical models of real-world processes. Markov Chains describe the failure distribution change by time. Monte Carlo simulations

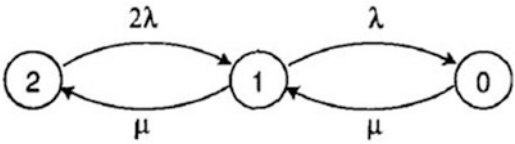


Fig. 12.6 Example state transition diagram for a two-component parallel structure

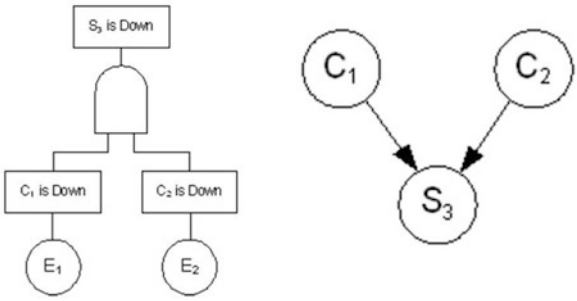


Fig. 12.7 Classical fault tree model for a parallel system (*left*) and the equivalent Bayesian Network (*right*)

often go hand in hand with Markov Chains in order to update the state of the system (read failure probability) at a certain time. The changes of state of the system are called transitions, and the probabilities associated with various state-changes are called transition probabilities. A well-known example of a Markov Chain is the PageRank of a Webpage as used by Google. Figure 12.6 shows an example of a Markov Chain for a system with two components in a parallel structure. The system is fully functioning when the state is 3 and failed when the state is 0. In states 1 and 2 the system is operating with only one component functioning. The transitions are characterized by two parameters:

- The failure rate λ
- The repair rate μ

Theoretically, when the system has n components, and each component has two states (functioning and failed), the system will have at most 2^n different states.

3. Bayesian Networks

Large systems become difficult to model by Markov Chains because they induce a combinatory explosion of states. Fault trees are also difficult to implement to large systems and particularly if the studied system presents redundant failures. In this context, Bayesian Networks (BN) are a very interesting methodology [32–35]. They allow the stochastic modeling of reliability in a compact and graphic form. The graphical form commonly used for BN is the Directed Acyclic Graphs (DAGs) whose nodes represent random variables and arcs represent direct influences between adjacent nodes. An example is presented in Fig. 12.7. Modeling with a BN is realized with a single "V structure" in which the conditional probability table contains the failure propagation mechanisms through the functional architecture of the system. BNs build the relationships between the nodes and calculate the nodal influence by such relationships.

Table 12.1 (Dis-) advantages of three main reliability prediction methodologies

Model	Advantages	Disadvantages
Fault tree	– Discrete – Logic of the system well described	– Static in time – Point estimates
Bayesian Network	– Fast updating – Discrete or continuous – Interval estimates available – Clear causality	– Static in time – No gate representation (logic)
Markov Chain	– Dynamic in time – Limiting probabilities – Computationally more intensive	– Point estimate at every time – Causality not very clear – Difficult to handle large systems

The influences represented by the arc of a Bayesian network can be probabilistic or deterministic.

Table 12.1 lists the advantages and disadvantages of the different prediction methods as explained above. The next paragraph presents application of these methods to SSL systems.

12.4 Case Studies

12.4.1 Basic SSL System

Consider the simplest possible SSL system. It contains three LEDs mounted on a printed circuit board (PCB) and electrically driven by one common driver. The goal is to model the system reliability of such a basic SSL system and predict its lifetime. The system may fail due to:

- LED failure (both catastrophic and depreciation) or
- Solder failure or
- Driver failure

This basic system is used to compare the three prediction methods described in the previous paragraph: Fault Tree, Bayesian Network, and Markov Chains. Figure 12.8 shows the fault tree representation of the problem together with the component failure distribution. The component failure distributions are the results of accelerated test data.

The FT in Fig. 12.8 is turned into a discrete BN using the Netica software [36]. Conditional probability tables are quantified as follows:

- Nodes without parents need probability of failure or no failure (denoted as LEDx_CAT or Lx_C).
- The probability of catastrophic failure is a deterministic node. There will NOT be a catastrophic failure when NONE of the individual LEDs fails.

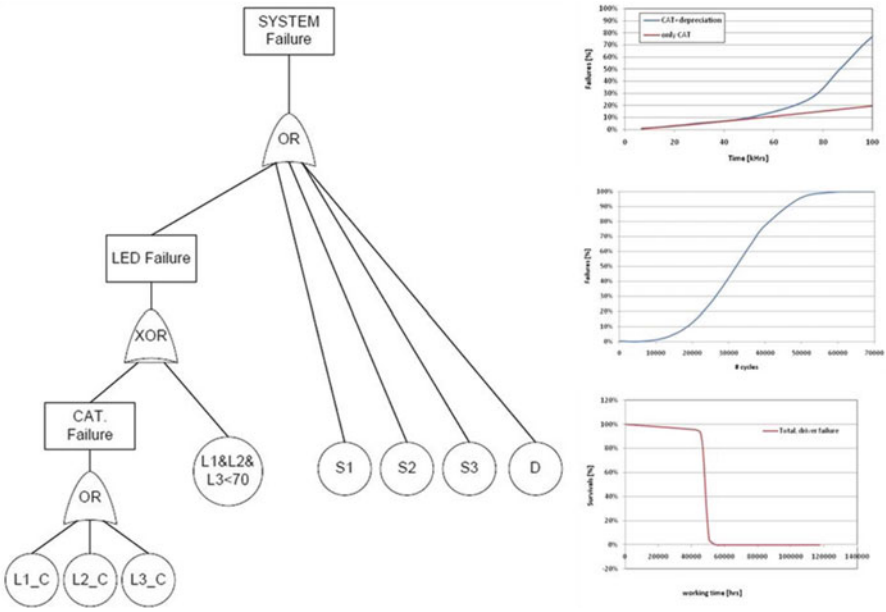


Fig. 12.8 Fault tree representation of the basic SSL system (*left*) and components failure distribution (*right*) with LED catastrophic and lumen failures (*top*), solder fatigue failures (*middle*), and driver failures (*bottom*) as function of time

- The depreciation node (denoted as LED_1_2_3_DEP_70 or L1&L2&&L3 < 70) depends on the catastrophic failure. If there is a catastrophic failure, then there is NO depreciation failure. If there is NO catastrophic failure then the probability of depreciation is computed according to [37, 38].

The discrete BN is depicted in Fig. 12.9. The BN model turned out to be tough: at every time of interest "one instance" of the model with its corresponding failure quantification turned out to be quite user unfriendly.

The estimation of the time-dependent failure rates feeds the Markov Chain model. Its parameters are determined by fitting Weibull distributions, see Table 12.2, onto the component failure data using the least squares theory. The density $f(t)$ and failure rate $r(t)$ for the Weibull distribution are given by

$$\begin{aligned} f(t) &= b \cdot a^{-b} \cdot t^{b-1} \cdot e^{-(t/a)^b} \\ r(t) &= a^{-b} \cdot b \cdot t^{b-1}. \end{aligned} \tag{12.3}$$

The procedure for the Markov Chain calculations is as follows: first estimate the failure rate and then use it in the transition probability matrix and use the matrix exponential to compute the reliability. Notice that the failure rate does not need to come from a Weibull distribution.

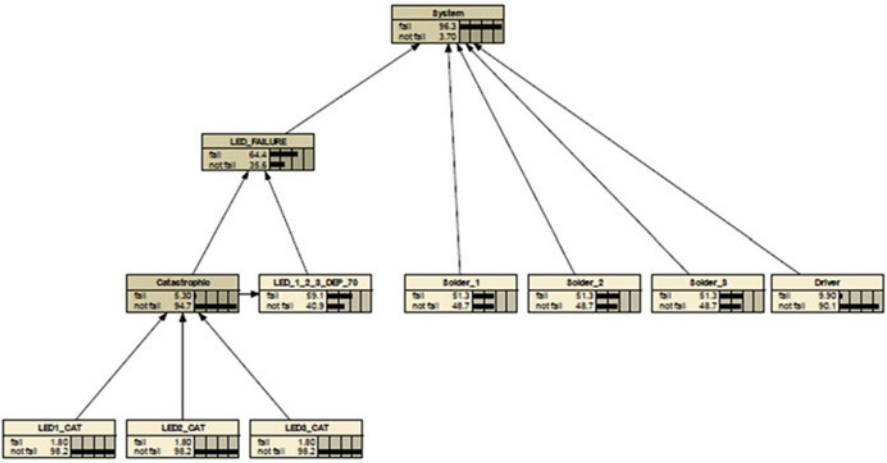


Fig. 12.9 Discrete BN representing the basic SSL system

Table 12.2 Fitted Weibull parameters as input for the Markov Chain model

Component	*a*	*b*
LED		
Catastrophic	1,509	1.5
Depreciation	102	5.3
Solder fatigue	110	3.4
Driver	965	1.0

Figure 12.10 shows the calculated system reliability curves with the different methods compared. All methods are able to produce identical results, which is not a surprise. The simulations show that the failures up to 20 kh are mainly dominated by the LED depreciation and the solder joint fatigue. As time progresses, the solder joint fatigue will dominate the system reliability behavior. Since all the lines overlapped, for the Markov Chain model a 5% repair rate is introduced in order to demonstrate the strengths of MC models.

12.4.2 Indoor Module

We applied the fault tree system approach to an SSL indoor system consisting of 12 LEDs and a simple driver [39–46]. For the LEDs, both the catastrophic and lumen depreciation failure modes are considered. For the driver, the FIT number is determined at an FIT of 1,040 failures in 10^9 operations. The LEDs are soldered onto an FR4 PCB. The system-level prediction is depicted in Fig. 12.11. After

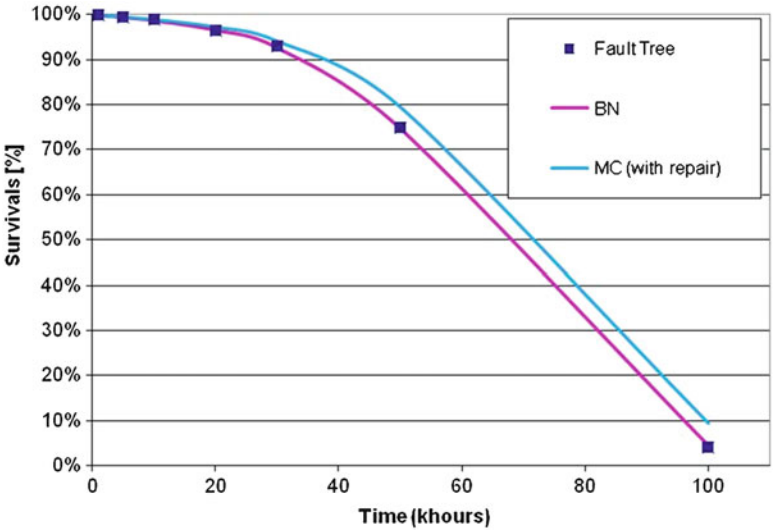


Fig. 12.10 Reliability prediction for the basic system and comparison between the different methods

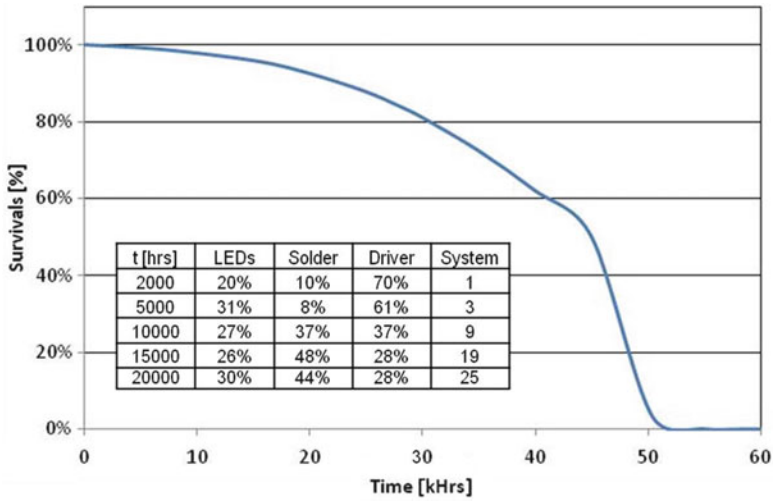


Fig. 12.11 Survivals (%) over time (kh) for a typical indoor SSL system

20,000 h of operating, it revealed that 30% of the failures is accounted by the LEDs, 44% by the solder interconnect, and 28% by the driver. The reliability of this system is driver limited within the first 5,000 h; after that the solder and the LEDs start to take an equal role in the failure performance.

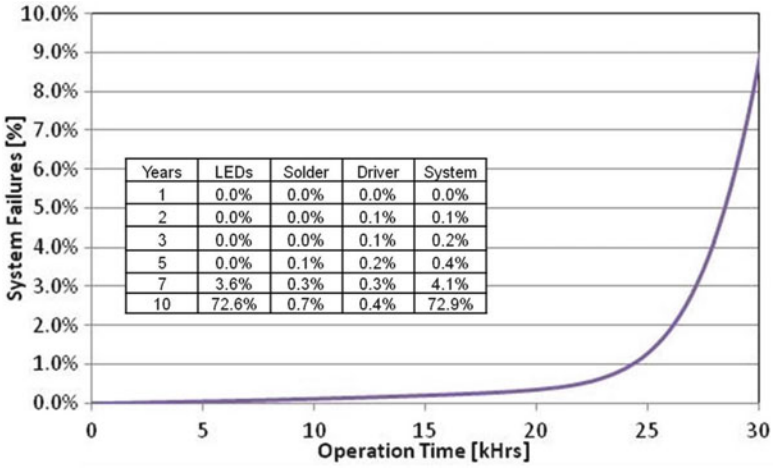


Fig. 12.12 Survivals (%) over time (kh) for a typical outdoor SSL system

12.4.3 Outdoor Luminaire

In this third case, we applied the fault tree system approach to an SSL outdoor system consisting of over 100 LEDs and a dedicated driver [47–51]. For the LEDs, both the catastrophic and lumen deprecation failure modes are considered. For the driver, the reliability performance equals 0.01% failures per 1 kh operations at a case temperature of 70 °C. The LEDs are soldered onto an MCPCB board. The system-level prediction is depicted in Fig. 12.12. After 10 years of operating, it revealed that 72.6% of the failures are accounted by the LEDs, 0.7% by the solder interconnect, and 0.4% by the driver. The reliability of this system is very good with failure rates way below 0.5% up to 5 years of service. After that time, the system mainly fails due to the lumen depreciation of the LED.

12.5 Conclusions and Recommendations

System reliability for SSL applications is a challenging task. This challenge mainly comes from:

- The large amount of unknown failure modes and mechanisms
- The technological gap to physically describe these mechanisms
- No existing acceleration test methods and/or standards
- The requested lifetime levels
- The lack of design for reliability rules

With the current pace of industry application development, there is a direct need to address the (long-term) design for reliability of SSL systems. This chapter presented the currently available reliability methods applicable for SSL systems. The presented case studies clearly show the benefits of such a system approach.

References

1. Nelson WB (1990) Accelerated testing: statistical models, test plans, and data analysis. In: Series in probability and statistics. Wiley, New York, ISBN:0-471-52277-5
2. Tobias P (1994) Applied reliability. Chapman & Hall, London. ISBN 0-442-00469-9
3. Dodson B, Nolan D (2002) Reliability engineering handbook. QA Publishing, LLC, Tucson, AZ. ISBN 0-8247-0364-2
4. Kececioglu Z (2003) Robust engineering design-by-reliability with emphasis on mechanical components and structural reliability. Destech Publications Inc., Lancaster, PA. ISBN 1-932078-07-X
5. Stamatis DH (2003) Failure mode and effect analysis: FMEA from theory to execution. ASQ Quality Press, Milwaukee, WI. ISBN 0-87389-598-3
6. Misra KB (2008) Handbook of performability engineering. Springer, London. ISBN 978-1-84800-130-5
7. http://en.wikipedia.org/wiki/Reliability
8. Zhang GQ, van Roosmalen AJ (2006) Reliability challenges in the nanoelectronics era. J Microelectron Reliab 46:1403–1414
9. Liddell HG, Scott R (1940) A Greek-English Lexicon. Perseus Digital Library
10. Wikipedia: http://en.wikipedia.org/wiki/Complex_system
11. Joslyn C, Rocha L (2000) Towards semiotic agent-based models of socio-technical organizations. In: Proceeding of the AI, simulation and planning in high autonomy systems (AIS 2000) conference, Tucson, Arizona, pp 70–79
12. Weaver W (1948) Science and complexity. Am Scientist 36:536
13. Nelson W (2004) Accelerated testing statistical models, test plans, and data analyses. Wiley, New York, NY. ISBN 0-471-69736-2
14. Rausand M, Hoyland A (2004) System reliability theory: models, statistical methods and applications. Wiley, Hoboken, NJ. ISBN 0-471-47133-X
15. ISO 8402 (1994) Quality management and quality assurance—vocabulary. http://www.iso.org/iso/iso_catalogue/catalogue_ics/catalogue_detail_ics.htm?csnumber=20115
16. Calce: Center for Advanced Life Cycle Engineering. http://www.calce.umd.edu/
17. Illuminating Engineering Society (2008) LM-80-08. Approved method for measuring maintenance of led light sources, p.10, ISBN: 9780879952273
18. Illuminating Engineering Society (2008) LM-79-08. Approved method: electrical and photometric measurements of solid-state lighting products, p.16, ISBN: 978-0-87995-226-6
19. U.S. Department of Defense (1965) MIL-HDBK 217: military handbook for reliability prediction of electronic equipment, Version A. 918
20. Technologies T (2001) Special Report SR-332: reliability prediction procedure for electronic equipment. Telcordia Customer Service, Piscataway, NJ
21. Denson W (1999) A tutorial: PRISM. RAC J 21(3):1–6
22. China Military Standard (1998) GJB299B, Handbook for reliability prediction for electronic device, Bejing, pp 12–39
23. Villemeur A (1992) Reliability, availability, maintainability and safety assessment: methods and techniques. Translated from French Edition by Cartier A, LMC (eds). Wiley, New York
24. Denson W (1998) The history of reliability prediction. IEEE Trans Reliab 47(3-SP):321–328
25. Wong KL (1990) What is wrong with the existing reliability prediction methods? Qual Reliab Eng Int 6(4):251–257

26. Painton L, Campbell J (1995) Genetic algorithms in optimization of system reliability. IEEE Trans Reliab 44(2):172–178
27. Chaudhuri G, Hu K, Afshar N (2001) A new approach to system reliability. IEEE Trans Reliab 50(1):75–84
28. Tian X (University of Arizona Tucson) (2002) Comprehensive review of estimating system-reliability confidence-limits from component-test data. In: Proceedings annual reliability and maintainability symposium, pp 56–60
29. Pecht M (2009) Product reliability, maintainability, and supportability handbook, 2nd edn. CRC Press, Boca Raton, FL 33487–2742. ISBN 978-0-8493-9879-7
30. IEC (1990) IEC 61025: fault tree analysis. IEC, New York
31. Meyn SP, Tweedie RL (2008) Markov chains and stochastic stability, 2nd edn. Cambridge University Press, Cambridge
32. Torres-Toledano J, Sucar L (2004) Bayesian networks for reliability of complex systems. In: Coelho H (ed) Progress in artificial intelligence, IBERAMIA98, Lisbon, Portugal, October 5–9, Springer, pp 195–206
33. Jensen F (1996) An introduction to Bayesian networks. UCL Press, London
34. Bobbio A, Portinale L, Minichino M, Ciancamerla E (2001) Improving the analysis of dependable systems by mapping fault trees into Bayesian networks. Reliab Eng Syst Saf 71 (3):249–260
35. Simon Ch, Weber Ph, Levrat E (2007) Bayesian networks and evidence theory to model complex systems reliability. J Comput 2(1):33–43
36. Netica software available at http://www.norsys.com/
37. LED reliability and lumen maintenance. www.philipslumileds.com
38. Hechfellner R, Landau S (2009) Understanding LED performance, Led Lighting Magazine, pp 45–53
39. US Department of Energy (DOE) (2009) LED applications. www.ssl.energy.gov
40. Alliance for Solid-State Illumination Systems and Technologies (ASSIST Program). http://www.lrc.rpi.edu/programs/solidstate/assist/index.asp
41. Mottier P (2009) LED for lighting application. Wiley, Hoboken, NJ 07030, ISBN 978-1-84821-145-2
42. HB Led & Led Packaging (2009) Yole Development report, 2009. http://www.yole.fr/
43. NF EN 13201-3 standard for photometric performance of public lighting facilities, Europe, pp 69–89
44. LED professional review, July/August edition, 2010, pp 7–11
45. Tarashioon S, Koh SW, van Driel WD, Zhang GQ (2010) High temperature reliability of drivers for solid state lighting. In: Proceedings of the LS12-WLED3 conference, The Netherlands, July 2010
46. Erinc M, Kloosterman J, van Driel WD, Gielen AWJ, Zhang GQ (2010) On solder joint reliability in LEDs by accelerated life testing. In: Proceedings of the LS12-WLED3 conference, The Netherlands, July 2010
47. Led luminaire lifetime: recommendations for testing and reporting, solid state lighting product quality initiative, next generation lighting industry alliance with the U.S. Department of Energy, 2nd edition, june 2011. http://apps1.eere.energy.gov/buildings/publications/pdfs/ssl/led_luminaire-lifetime-guide_june2011.pdf
48. Evertz FE, van Driel WD, Kloosterman J, Vanlier G, Zhang GQ (2010) Towards a system level reliability approach for solid state lighting. In: Proceedings of the LS12-WLED3 conference, The Netherlands, July 2010
49. van Driel WD, Li XP, Chen J, Evertz F, Zhang GQ (2011) Solid state lighting reliability: from components to system. In: Proceedings of the China SSL conference, Shenzhen, China, October 2011
50. van Driel WD, Evertz F, Zhang GQ (2011) Towards a system level reliability approach for solid state lighting. J Light Vis Environ 35(3):267–273
51. FIDES Group (2004) FIDES Guide Issue A: reliability methodology for electronic systems. http://www.fides-reliability.org

Chapter 13
Solid State Lighting System Reliability

M.H. Schuld, B.F. Schriever, and J.W. Bikker

Abstract System level reliability is crucial for the business success of future Solid State Lighting systems. This chapter covers the reliability theories and practices and applies them to solid state lighting products. Both hardware and software reliability theories are addressed. Practical approaches for system reliability are proposed as well.

13.1 Introduction

Knowledge of system level reliability is crucial for the business success of Solid State Lighting (SSL) systems and is also a very scientific challenge. In practice, a malfunction of the system might be induced by the failure and/or degradation of the subsystems and interfaces. Most SSL system designs allow few failures during the application period. Hence, a significant cost reduction can be achieved when the system level reliability is well understood by proper experimental and simulation techniques. This chapter covers the reliability theories and practices. It is organized as follows. A description of SSL systems is provided in Sect. 13.2. In Sect. 13.3 the contributions of components are discussed. In Sect. 13.4 the statistics of system reliability—taking into account hardware, correlations, software, and interactions—is presented. In Sect. 13.5 a practical approach for system assessment is proposed.

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13.2 Solid State Lighting Systems

A system is a set of interacting or interdependent system components forming an integrated whole. This implicates that two components together already form a system. When the number of components and their interactions hugely increase, so-called large or complex systems are formed. System reliability can be defined as the probability that a system, including all hardware, firm-ware, and software, will satisfactorily perform the task for which it was designed or intended, for a specified time and in a specified environment.

Figure 13.1 shows different possible SSL applications, ranging from LED lighting in offices, around living houses to streetlight and a total city that needs to be lighted. Even an LED package can be seen as a system since it is composed of several interacting components, being the LED device; the lens on top and the (ceramic) carrier below. A retrofit bulb adds to that a driver: the housing and a thermal solution (mostly heat sink). Pucks are another form of the housing in which typically over 10 LED packages are mounted. When several pucks are combined, a luminiare is formed. A luminiare may contain a controller. A typical household nowadays consist of over 30–40 light engines, they could be controlled from a central place. Finally, a city of Shanghai consists of millions of street and indoor lighting engines. Only the latter one can be seen as a complex or large system.

13.2.1 What Do We Mean by the Lifetime of a System?

When do we say that a LED system does not function properly? Basically we distinguish two categories:

(a) Catastrophic failures: the device ceases to operate. This type of failures is clear. Specifications are set on the time to (catastrophic) failure.
(b) Degradation failures: the device still functions but does not meet the performance target. This type of failure is less well defined. It is well known that the light output from power LEDs is highest when new, and declines gradually over time. For this reason, it is common to set a specification for the time for which the lumen maintenance is at least 70%. However, LED degradation is not just



Fig. 13.1 SSL applications, with from left to right, an office with bulbs, outdoor luminiares at living house environments, street lighting in Dubai and lighting the city of Shanghai with LEDs

lumens; also the color, light uniformity, and V_f can shift over time. This means that for all the LED-system end product parameters we should set a degradation limit similar to the 70% lumen maintenance degradation limit.

In this way we can define the time until one system fails (the failure time). In case we have more systems of one and the same design, the failure times will not be identical. Traditionally engineers estimate the mean failure time of all systems to be produced of a specific design (the Mean Time To Failure, MTTF in short). However, customers are not interested in the MTTF, they want to know the point in time at which 90% (or 95% or even 99%) of the systems survive. This point in time is called the B10 (B05 and B01 respectively.)

13.3 What Is the Contribution of Each Component?

The survival function of the total system in the field depends on the design, on the components used, on the manufacturing process, and on the use conditions. An insufficient understanding of the factors that determine reliability, can result in either a higher than expected rate of claim against the warranty, or cause a product to be overspecified, potentially increasing the manufacturer's bill of materials unnecessarily.

13.3.1 Model Approach

First consider the survival function as a function of the design and the components used (and exclude the manufacturing process and use conditions). Suppose the individual survival functions of each component are known. Also, the interactions or dependencies between the components may be known. The joint reliability function can be obtained by exact calculation, or by Monte Carlo. One of the purposes of system reliability analysis is to identify the weakness in a system and to quantify the impact of component failures. Several measures of "reliability importance" exist, each expressing the importance from a slightly different point of view. Suppose we want to know the importance of component K for the reliability of the total system. Let $R_S(t)$ denote the survival function of the total system, and let $R_k(t)$ denote the survival function of the individual component K. Well known measures are:

- Birnbaum's Measure
- Criticality Importance
- Reliability Reduction Worth
- Reliability Achievement Worth

13.3.2 Birnbaum's Measure

Birnbaum's measure, see ref. [1] Birnbaum (1969) is defined as

$$I_k^B = \frac{\partial R_S(t)}{\partial R_k(t)}$$

It can be interpreted as the maximum loss in system reliability when component K switches from the condition of perfect functioning to the failed condition. A weakness of Birnbaum's importance measure is that does not depend on the component reliability, $R_K(t)$. Therefore, two components may have a similar Birnbaum metrics, although these current levels of reliability could differ substantially. In practice, the less reliable component is generally a greater concern, and hence is more critical.

13.3.3 Criticality Importance

The Criticality Importance metric includes the component unreliability, $1 - R_K(t)$, whereas the Birnbaum's measure does not. In this way, a less reliable component becomes more critical. The Critically Importance is defined as

$$I_k^{\mathrm{IC}} = \frac{1 - R_k(t)}{1 - R_S(t)} I_k^B(t)$$

It can be interpreted as the probability that component k has caused system failure, when we know that the system is failed at time t.

13.3.4 Reliability Reduction Worth

The Reliability Reduction Worth is an importance metric that reflects the reduction of reliability if component K always failed (i.e., $R_k(t) \equiv 0$ for all t), see ref. [2]. In formula

$$I_k^{\mathrm{RRW}} = \frac{R_S(t)}{R_S(t|R_k(t) \equiv 0)}$$

The numerator in this definition describes the probability that the system will survive time t, and the denominator describes the probability that the system will survive time t when the component K is replaced by an always defect system. It expresses the potential damage caused to the system by component K.

13.3.5 Reliability Achievement Worth

The Reliability Achievement Worth metric describes the increase of reliability if component K is replaced by a perfect system, i.e., $R_k(t) = 1$ for all t

$$I_k^{\mathrm{RAW}} = \frac{R_S(t|R_k(t) \equiv 1)}{R_S(t)}$$

This measure quantifies the maximum possible percentage increase in system reliability generated by component K.

The abbreviations RRW and RAW are also used for Risk Reduction Worth and Risk Achievement Worth. These could also be used in the context of system reliability. The risk is then the unreliability of a system $1 - R(t)$. Although the Risk Reduction Worth should come close to the Reliability Achievement Worth, the definitions are not equal. (Similarly, the Risk Achievement Worth is close, but not equal to the Reliability Reduction Worth).

Risk Achievement Worth (RAW): the increase in system risk if the component K is assumed to be failed at all times. It is expressed in terms of the ratio of the risk of the system with the component K failed to the system risk level.

Risk Reduction Worth (RRW): the decrease in system risk if the component K is assumed to be perfectly reliable. It is expressed in terms of the ratio of the system risk level to the system risk with the component K guaranteed to succeed.

13.3.6 Example: LED String

Consider the following simple design with one driver and four identical LED's in series. The system fails as soon as one of the components fails. Hence dependency between the components has no effect on the system reliability. (Furthermore, solder joints are not expected to fail. Also, light degradation is not considered, i.e., only one catastrophic failure mode).

The survival function of each LED is denoted by $R_L(t)$ and the survival function of the driver by $R_D(t)$. In Sect. 13.4.2.1 it is explained that the survival function of the system can be written as

$$R_S(t) = R_L^4(t)R_D(t)$$

The formulas for the four importance measures for each LED and the Driver are:

$$I_L^B(t) = R_L^3(t)R_D(t),\ I_D^B(t) = R_L^4(t)$$

$$I_L^{\mathrm{IC}}(t) = \frac{1 - R_L(t)}{1 - R_S(t)} R_L^3(t)R_D(t),\ I_D^{\mathrm{IC}}(t) = \frac{1 - R_D(t)}{1 - R_S(t)} R_L^4(t)$$

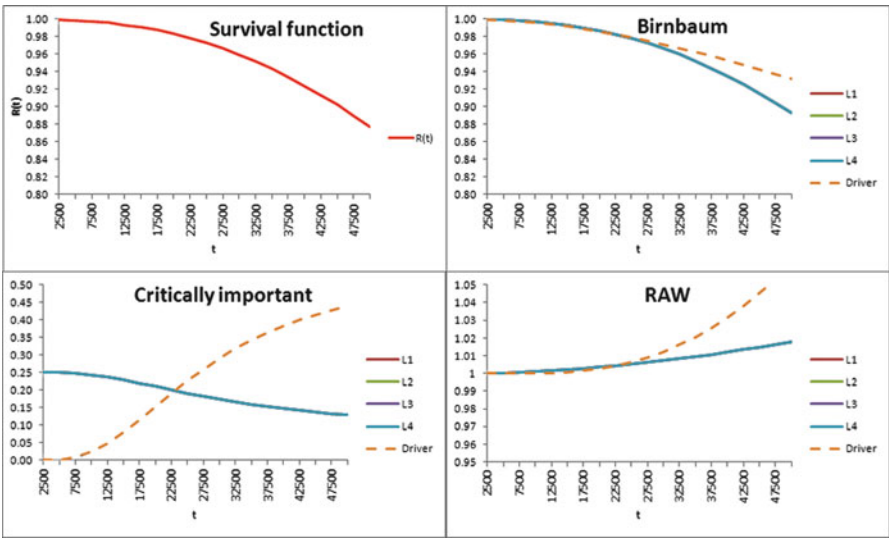


Fig. 13.2 Contributions using a Weibull survival function for the LED and a lognormal function for the driver

$$I_L^{\mathrm{RRW}}(t) = \infty, \qquad I_D^{\mathrm{RRW}}(t) = \infty$$

$$I_L^{\mathrm{RAW}}(t) = 1/R_L(t), \; I_D^{\mathrm{RAW}}(t) = 1/R_D(t)$$

Suppose the LED survival function is determined as a Weibull with scale 500,000 and shape 1.75 and the Driver is LogNormal with location 12 and scale 0.75, then the survival and importance measures are given by the following graphs (Fig. 13.2):

Note that the lines for the four LED's overlap. The importance measures are displayed for one single LED, which means the sensitivities when we change only one LED and keep the other three at the same reliability performance. The graphs show that for the longer life-times the Driver is more important than a LED. The Critically important measure says that when the system fails before $t = 20{,}000$, it is probably not due to the Driver.

13.4 Statistics of System Reliability

13.4.1 Introduction System Reliability (Hardware)

System reliability is about modeling the reliability of a complete system using knowledge of the underlying components. The system-wide reliability depends on

- The system structure of components and failures
- Reliability of the components
- (Environment, stress-factors)

The output of the model is

- Description of the survival time distribution of the system
- Assessment of the sensitivity of the survival time

Often, it is desirable to check the model accuracy by means of a system reliability test.

13.4.2 System Structures

13.4.2.1 Basic Examples of System Structures

A basic way of modeling system structure is by considering the system structure to consist of several components linked together in series or parallel, where failures of components occur independently.

- Examples of simple systems:
  - *Components in series*: the system fails as soon as one of its components fails. Examples are LED strings, a chain, batteries in series.
    For k independent components:

$$R_{\text{system}}(t) = \prod_{i=1}^{k} R_i(t)$$

  - *Components in parallel*: the system fails when all components are failed. Examples are multiple emergency lights in a corridor, headlights and rear lights of a car.
    For k independent components:

$$R_{\text{system}}(t) = 1 - \prod_{i=1}^{k} (1 - R_i(t))$$

  - *An s-out-of-k system structure*: the system fails as soon as $k - s + 1$ components out of the k components failed (= the system did not fail when at least s out of k are still working).
    For k independent and identical components

$$R_{\text{system}}(t) = 1 - \sum_{i=k-s+1}^{k} \frac{k!}{i!(k-i)!} \times (1 - R(t))^i R(t)^{k-i}$$

The reliability function R is easily calculated from the component's reliability functions.

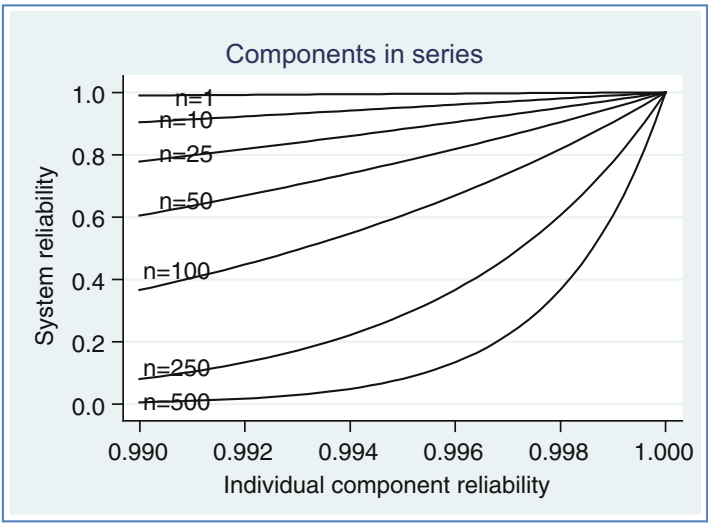


Fig. 13.3 System reliability for components in series

13.4.2.2 Example LED String

Consider a product with $k + 1$ components: k LED's of one and the same type plus one driver. The lifetime of the LED type has a Weibull distribution with scale and shape parameter α, and β. The life time of the driver has a LogNormal distribution with location and scale parameter μ, and σ. The product fails when the first of the $k + 1$ components fails (*in series*). The reliability function of the product equals:

$$R(t) = \Phi\left(\frac{\ln(t) - \mu}{\sigma}\right) \times \exp\left(-\left(\frac{t}{\alpha}\right)^{\beta}\right)^{k}.$$

When the product fails when the driver fails or $k - s + 1$ out of the k LEDS fail, the reliability of the product equals:

$$R(t) = \Phi\left(\frac{\ln(t) - \mu}{\sigma}\right) \times \left(1 - \sum_{i=k-s+1}^{k} \frac{k!}{i!(k-i)!} \times \left(1 - \exp\left(-\left(\frac{t}{\alpha}\right)^{\beta}\right)\right)^{i} \exp\left(-\left(\frac{t}{\alpha}\right)^{\beta}\right)^{k-i}\right)$$

In theory a system consisting of identical components in series is less reliable than the individual components; the reverse is true for components in parallel. This is illustrated in the examples in Figs. 13.3 and 13.4. The figures show how the number of component influences the system reliability. On the horizontal axis is the individual component reliability, i.e., the survival probability for a given time. The vertical axis has the same, for the system. It is assumed that the components fail independently of each other and have the same survival probabilities. The first graph shows an example for components in series, where increasing s (nr of

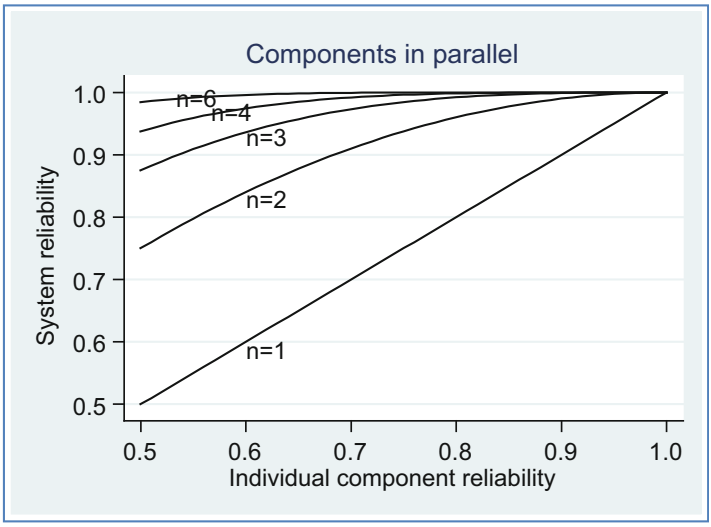


Fig. 13.4 System reliability for components in parallel

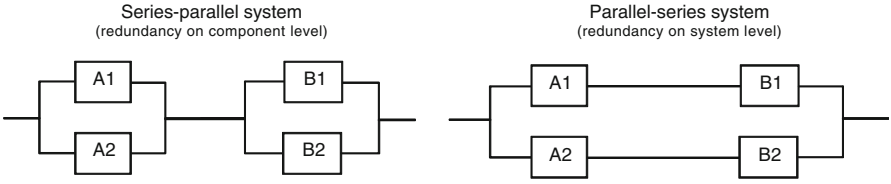


Fig. 13.5 Extensions to the parallel and series constructions, examples

components) results in a less reliable system. The second graph shows components in parallel, where system reliability increases with more components.

The same line of thought and system reliability function can be applied to extensions of the parallel and series set-up, for instance see Fig. 13.5.

In practice, however, the assumption of independence is not completely valid: when in a parallel set-up, LEDs fail the other strings will face a kind of surplus of current ("current hogging") which leads to rapid thermal runaway, which will eventually lead to no light output at all.

13.4.3 Dependency, Interactions Between Components

13.4.3.1 The Problem Statement

Assume that a system consists of two components with identical life time distributions, for example, two identical LEDs. We assume that they are "in series",

so we regard the system as failed as soon as one of the LEDs fails. Suppose that the failures do not occur independently. Possible reasons for this could be

- An underlying mechanism causing both LEDs to wear out with about the same speed. For instance (increasing) current or environmental/junction temperature influence equally the lifetimes of the LEDs.
- Between-batch production spread. It is possible that LEDs of the same batch are more similar than across batches. The system probably gets the LEDs from the same batch when being manufactured. If the first LED has a short life time, the second LED probably has a short life time as well.
- Cause-and-effect between components. Consider a system consisting of LEDs and a cooling system with a fan. If the fan deteriorates (bearing, wear, ...) the cooling is not as good, temperature of the LEDs rise, so the LEDs wear out faster. Low survival times for the fan will have a tendency to coincide with low survival times of LEDs, hence the dependency of survival times.

It turns out that the system reliability depends on the degree of dependency ("correlation") of the reliability of its components. Note that very often independency is assumed. However, the system reliability can be strongly influenced by dependency as is shown in a simple example. Here, the dependency is described by a correlation ρ. In general, describing dependency between survival time distributions is more complex than just the familiar correlation coefficient; see copulas in Sect. 13.4.3.2. Below, the meaning of ρ in this example is explained:

Suppose we have a system consisting of two identical components, with identical failure time distributions. The axes show the survival probability for a given point in time; horizontal: for the individual component, vertical: the system. The different lines belong to different degrees of dependency: $\rho = 0$ (no dependency; often assumed) to $\rho = 1$, complete dependency, the two components fail at exactly the same point in time (and the system can be considered as having one component) (Fig. 13.6).

The construction of dependency in this example gives a taste for the mathematical complexities involved. Each of the individual components has a survival time with an identical log-normal distribution. Then the log-survival times both follow a normal distribution. The bivariate normal distribution has correlation ρ. This means that if you would observe many systems and record the log survival times of component 1 and 2, you would get the following plots (for different values of ρ):

13.4.3.2 Introduction to Copulas

In general, lifetimes of components (as part of a system) are not independent, so it is necessary to consider their joint, multivariate distribution. In recent years, the copula models became increasingly popular for modeling dependencies between random variables based on marginal distributions. They are widely investigated in the financial world. For an extensive description of the theory on copulas we refer to ref. [3].

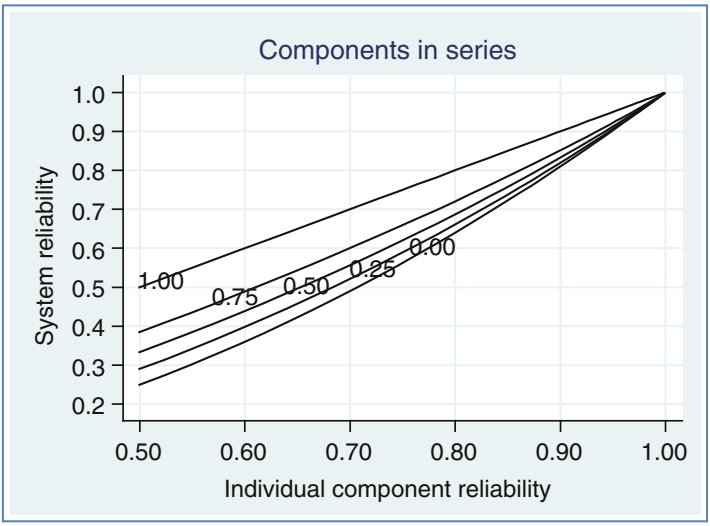


Fig. 13.6 Components: the impact of correlation

The basic idea of a copula can be expressed in terms of information; the mathematical version is called Sklar's theorem:

Joint distribution Information for system reliability	=	**Marginal distributions** Of each component (familiar distributions)	+	**Copula** Dependency structure. Like correlations, but more subtle

The example in subsection 13.4.3.1 actually contains a "Gaussian" copula. Namely, the marginal distributions were given: survival times are log-normal, with log(T) normally distributed with $\mu = 2$, $\sigma = 1/3$. The dependency structure was stated as follows. "Stretch" or rescale the marginal distributions so that they get a normal distribution. In this specific case, this is achieved by taking the logarithm of the survival times, but this could be done for any distribution with a more complicated stretching. Then it was assumed that the resulting multivariate distribution, plotted in Fig. 13.7, is actually bivariate normal with a correlation parameter ρ. This assumption fixes the Copula, and this particular choice is called a Gaussian copula.

It is also possible to stretch the marginal distribution to a uniform distribution on [0,1]. This can always be achieved by the cumulative distribution function:

$F_T(t) = P[T \leq t]$ so F_T gives a transformation from time t to the interval [0,1]. For the Gaussian copula, if we stretch the marginal normal distributions to a uniform distribution, they look like this (Fig. 13.8):

Now we have arrived at the mathematical description of a Copula. *A copula is the joint cumulative distribution function of a vector of uniformly distributed variables:* $C(u_1, \ldots, u_n) \rightarrow [0,1]$. Note that any joint cumulative distribution corresponds to a copula via: $C(u_1, \ldots, u_n) = P[X_1 \leq F_1^{-1}(u_1), \ldots, X_n \leq F_n^{-1}(u_n))]$. Where F_i is the cumulative distribution function of margin i.

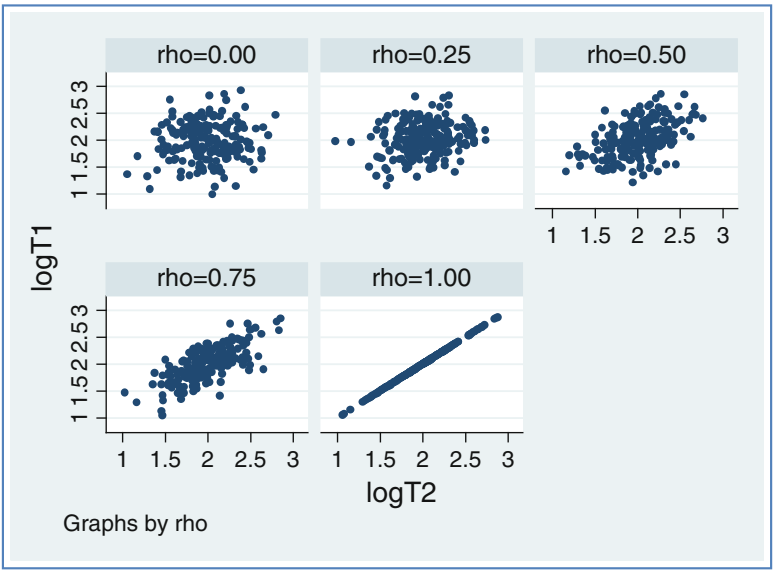


Fig. 13.7 Bivariate normal distributions of the log-survival times of two identical components

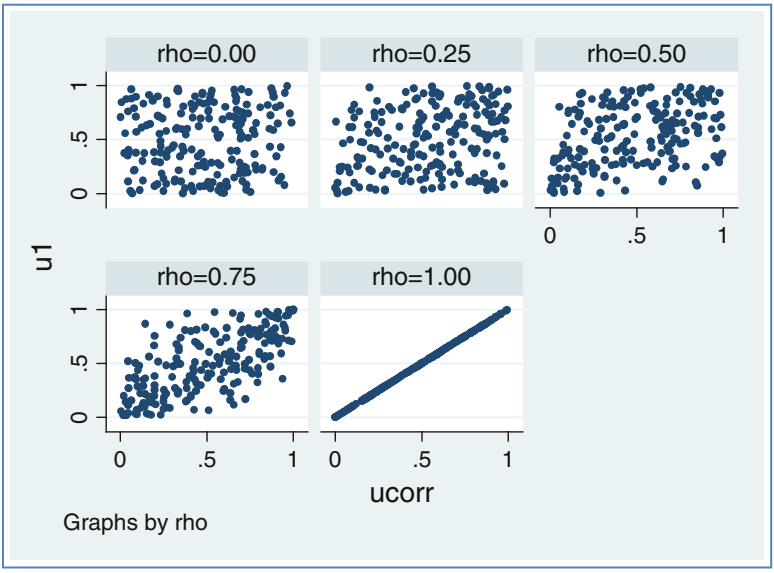


Fig. 13.8 Gaussian Copula with uniform margins

Consider a system of two components in series and failure times T_1, T_2, and T_{system}. Then $R_{\text{system}}(t) = P[T_{\text{system}} > t] = P[T_1 > t, T_2 > t]$. If T_1 and T_2 would be independent, then calculations are easy:

$$R_{\text{system}}(t) = P[T_1 > t, T_2 > t] = P[T_1 > t]P[T_2 > t] = R_{T_1}(t)R_{T_2}(t)$$

However, if T_1 and T_2 are dependent, this formula no longer holds and the output depends on the *joint cumulative distribution function* $F(t_1, t_2) = P(T_1 \leq t_1, T_2 \leq t_2)$. The *marginal cumulative distribution functions* are derived from the multivariate, e.g., for T_1: $F_{T1}(t) = F(t, \infty) = P[T_1 \leq t, T_2 \leq \infty] = P[T_1 \leq t]$. The marginal cumulative distributions belong to the components and would typically have a familiar reliability distribution like Weibull or log-normal. What remains is the choice of a copula to have a complete description for the system.

13.4.3.3 Choice of Copulas

In subsection 13.4.3.1, a description of a Gaussian copula was given mainly to illustrate the idea of copulas, however, there are many more possible choices. In general, it would be very hard to decide on a copula just based on empirical evidence. When investigating system reliability, the choice would probably be made based on practical grounds. We give two main directions:

1. Gaussian and t-copulas
2. Archimedian copulas.

Gaussian and t-copula	Archimedian copula
Easy in simulations	Some easy analytical results
Given by correlation matrix	Given by one parameter (usually)
Easy explanation and "default choice" is a motivation	Analytical tractability is a motivation

In all cases, one or more parameters of a copula need to be established. This may be done from an empirical test where many *systems* are tested until *all* of the components fail, because we need observations of failure times as vectors $(t_1, t_2, \ldots, t_n)$. Such a test may not be possible in all cases.

Alternatively, the copula parameter could be fixed based on some historical value of a comparable product.

Another approach is to build the model for system reliability and study the outcomes as the copula parameter varies. This may give an impression of the sensitivity of the system to dependency, and it may give a bound to how bad the system reliability could be.

If a system test can be done where each system is tested until one of its components fails, still the copula approach may be useful. Namely, if component models are combined with the copula to a system model, the copula parameter could be chosen (calibrated) so that the resulting system reliability predictions match the test results as closely as possible. We refer to Sect. 13.5.2.

13.4.3.4 Modelling with Gaussian and t-Copulas

Starting point is a system with components with known or chosen distributions of survival times. After a copula is chosen, in principle the system reliability can be determined, e.g., by simulation.

The Gaussian and t-copula are similar in the sense that

1. A correlation matrix defines the copula
2. The copula (multivariate distributions) are easily simulated

The difference is that a Gaussian copula has no "tail dependency" and a t-copula has positive tail dependency, see ref. [4]. In words, according to Gaussian copulas, it virtually never happens that two or more components fail very early, or survive very long. According to t-copulas, there is a real chance that extreme survival times (very small or very large) happen to multiple components. The insurance world favors the t-copula for this reason (multiple extreme events may occur) in many applications. In fact, the Gaussian and t-copula belong to the class of *elliptic copulas* whose tail-dependencies are studied, see ref. [5].

Both the Gaussian and t-copula follow the same method to estimate the correlation matrix. The required data would in principle be the survival times of components of a system, where many systems are tested until (almost) *all* of a system's components fail and not just one. On this data, for each pair of components (i,j) the so-called Kendal-tau τ_{ij} is calculated, which is similar to the familiar linear correlation coefficient. The Kendal-tau only depends on ranks of values, and therefore not on the distributions of values. Then the correlation coefficient for the Gaussian or t-copula follows from $\tau_{ij} = 2/\pi * \arcsin(\rho_{ij})$.

Simulation is described briefly here. The correlation matrix C is determined by $C_{ij} = \rho_{ij}$ with ρ_{ij} determined as described above. For the Gaussian copula, we need to draw random vectors from a multivariate Gaussian distribution given the correlation matrix C. This can be done by the following steps. Calculate the Cholesky decomposition (the matrix equivalent of the square root) of the correlation matrix C: find H such that

$$H \cdot H^T = C.$$

The Cholesky decomposition can be determined with a relatively simple algorithm. Then draw randomly a vector z of independent standard normally distributed values, and multiply with H:

$$z = (z_1, \ldots, z_n)^T, z_i \sim \mathcal{N}(0,1)$$

$$y = H \cdot z$$

Now y is a vector of n standard normally distributed values with correlation matrix equal to C. To simulate a t-copula, an extra step is needed. Suppose the

desired t-copula has υ degrees of freedom. Then an extra random variable W needs to be simulated, independent of z, where the distribution of W is determined by

$$\frac{\upsilon}{W} \sim \chi^2_{\upsilon}$$

Taking the y from above, the following vector x has a multivariate t-distribution with υ degrees of freedom and scatter matrix C:

$$x = \sqrt{W} \cdot y$$

This distribution has covariance matrix $\frac{\upsilon}{\upsilon-2}C$; the matrix C is called the dispersion or scatter matrix. For more details on the t-copula, see ref. [6]. For both the Gaussian and t-copula, the inverse marginal distributions are taken on x resp. y to get to a vector of random variables with values on the interval [0,1] and the desired dependency structure.

13.4.3.5 Modeling Dependency Structures with Archimedean Copulas

For an extensive description of the theory on copulas we refer to ref. [5]. In this section, we will focus on a bivariate survival function using an *Archimedean* copula, which can be extended easily to more components.

Suppose that ψ: $[0, \infty] \rightarrow [0,1]$ is a strictly decreasing function such that $\psi(0) = 1$. Then an Archimedean copula may be generated as

$$C(x, y; \rho) = \psi\left(\psi^{-1}(x) + \psi^{-1}(y)\right), x, y \in [0, 1], \tag{13.1}$$

and ρ is the parameter of association. Examples of Archimedean copulas include three families:

1. Frank's copula, generated by

$$\psi^{-1}(x) = -\ln\left[\frac{e^{-\rho x}-1}{e^{-\rho}-1}\right], \text{ with } C_F(x, y; \rho) = \frac{-1}{\rho} ln\left[1 + \frac{(e^{-\rho x}-1)(e^{-\rho y}-1)}{e^{-\rho}-1}\right], \rho \neq 0.$$

2. Clayton's copula, generated by

$$\psi^{-1}(\mathrm{x}) = \frac{1-\mathrm{X}^{\rho}}{\rho \mathrm{X}^{\rho}}, \text{ with } C_c(x, y; \rho) = \left(x^{-\rho} + y^{-\rho} - 1\right)^{-1/\rho}, \rho > 0.$$

3. Gumbel-Hougaard copula, generated by

$$\psi^{-1}(x) = (-\ln(x))^{\rho}, \text{ with } C_{GH}(x, y; \rho) = e^{\left\{-\left[(-\ln(x))^{\rho} + (-\ln(y))^{\rho}\right]^{1/\rho}\right\}}, \rho \geq 1.$$

Archimedean copulas can be used for modeling survival functions with marginal distributions such as Weibull, Exponential, Lognormal, etc. All information concerning dependence is contained in the association parameter ρ. For example

assume a system consisting of two components, Weibull marginal distributions, and Gumbel-Hougaard copula, the joint survival probability equals

$$R(t) = e^{\left\{ -\left[\left(\frac{t}{\lambda_1}\right)^{\rho\beta_1} + \left(\frac{t}{\lambda_2}\right)^{\rho\beta_2} \right]^{1/\rho} \right\}} \tag{13.2}$$

As one can easily conclude, a higher value for ρ will increase the survival probability.

Covariates z—such as design parameters, or use conditions—can be incorporated as follows:

$$\lambda_i(z) = e^{\sum_j \xi_j z_j}, \ \mathrm{i} = 1, 2. \tag{13.3}$$

An extension of (13.2) to the case of $p \geq 3$ components is very straightforward, however a drawback of this model is that association among the components is governed by a single parameter ρ. This is adequate in cases where components are exchangeable and the R_i's are identical, but is an undesirable assumption in many settings. A vector of parameters P is more convenient.

Maximum likelihood estimation can be used to estimate the parameters. The required data would in principle be the survival times of components of a system, where many systems are tested until (almost) *all* of a system's components fail and not just one.

13.4.4 Software Reliability

In general a system consists of two major components: hardware and software. Software reliability is really different from hardware reliability in the sense that that software does not wear out or burn out. The software itself does not fail unless flaws within the software result in a failure in its dependent system. A study has shown that professional programmers average six defects for every 1,000 lines of code written. These defects include memory related errors, memory leaks, language-specific errors, wrong library references, compilation errors, etc. At that rate, a typical SSL system which contains 20,000 lines of code, might have 120 programming errors on average.

Also, predicting a software failure rate is more difficult than estimating a hardware failure rate because:

- Impact of software defects varies: some defects trigger failures with catastrophic results; others produce minor problems, or are automatically recovered by the system.
- Impact of hardware on software.

- Software defects only trigger failures when they are executed: since execution of software components/code is by far nonuniform, there is a large variation in how often particular defects might be executed.

Therefore, an important goal is to certify with high statistical confidence that software components do not have specific undesirable properties. In particular reliability engineers are focussed on two aspects. These are the fault-free period after the last failure observation, and the number of remaining faults in the code.

We give an overview of methods and models.

13.4.4.1 Complexity Metrics and Real-World Experience

Some models, formulated in the 1970s, are based on the complexity of the code, counting the number of lines, operators, operands, IF/WHILE/REPEAT/CASE commands and base predictions of the number of errors on those Examples are Halstead's software metric and McCabe's cyclomatic complexity metric. Another approach, also called curve fitting models, focus on project and software properties and compare it to known earlier software project. Input parameters are for example the release sequence number, environmental factors at the release, the number of modules, inter-release interval, number of days since the first release error, etc.

13.4.4.2 Error Seeding Models

Error seeding models focus at the test phase of a software project. Mill's error seeding model and an extension called Cai's model are based on deliberately introducing bugs into the code before the test phase and keeping track of the proportion of found bugs that were "seeded". Another variant deliberately does not solve bugs when found (the hyper geometric distribution model). These models aim to predict the total number of bugs present in the code. The most important examples are from the 1990s.

13.4.4.3 Failure Rate Models

The large class of failure rate models focus at the test phase of a software project and at the rates at which bugs are found. Many of these models were proposed in the 1970s. The models vary in nature of the failure rates (constant, or changing over time). The failure rates play a role similar to hazard rates known from hardware reliability. Some models take as input the times t_i at which bugs are found; others take the number of bugs found in subsequent time intervals. Some models allow multiple errors found at the same time, or imperfect repairs. All these models have an associated software reliability function $R(t)$, which is a "hazard rate" for the next software failure to occur.

Other extensions are Markov Structure models, which have a wide variety in applied mathematics. They focus on "states" a system may be in, and the transition probabilities between states. For instance, if the states are the number of errors in a piece of software, the possible transitions are the removal of one bug or addition of a bug, both with given probabilities. This way, imperfect debugging can be modelled. Other models take different software modules as states so that the interfaces between modules are modelled. Software safety models have safe and unsafe states.

13.4.4.4 Nonhomogeneous Poisson Process Models

The class of NNHP (nonhomogeneous Poisson Process) models are in fact failure rate models and explicitly model the testing phase of a software project. There are several recent models (1990s, 2000s). They have an analytical framework, where the model is given by a failure rate function describing the process of discovering errors. For instance, a basic model (the Goel-Okumoto model) assumes that the failure rate, or error detection rate, is proportional to the remaining number of errors in the model. There are two important kinds of model extensions.

- S-shaped models assume that the error detection rate increases after a while in the test phase to some maximum and then decrease. The motivation is that many errors are masked by others in the beginning of a test phase, and only become apparent after removal of the first main errors.
- Imperfect debugging models allow that new errors are introduced at repairs, and in fact a general error content function over time.

The Pham-Nordmann-Zhang model (PNZ model, 1999) and the Pham-Zhang model (1997) are examples of model than have both extensions. In that sense, they incorporate many features of earlier models. Section 6.8 of Pham [7] evaluates these and other models on real-life data from software test phases.

13.4.4.5 Bridging the Environments of System Tests and the Field

The nonhomogeneous Poisson process models of 0 give a description of errors occurring in the system test environment. For reliability of systems in the field, the perception of the user is more relevant. As a general approach, certain NHPP models are suitable for modifying the failure rate function for the system test environment using a calibration factor, so that the field failure rate is described. The calibration factor needs to be estimated using previous projects. An extension of this idea is the class of Random Field Environment (RFE) reliability models. These models view the field as uncertain and describe the translation using random variables.

13.4.4.6 Software Reliability Certification

Recently, there have been interesting developments in the area of statistical procedures for supporting software release decisions. These are described in the PhD-thesis of Ramos [8], Chap. 5. The methods focus on a certification criterion, which is motivated from the user point of view, who expects producers to certify that the software is reliable. Such statistical approaches can be found in Currit et al. [9] and Di Bucchianico et al. [10]. Both approaches focus at the test phase in software development where errors are found in a sequence. The first approach focuses at the times between finding errors; similarly, the second focuses on the number of test runs needed to find the next error. Di Bucchianico et al. [10] has a statistical framework with hypothesis testing for deciding how many test runs should be performed in trying to find an error, before concluding with a high confidence that there are no errors left. The amount of testing that needs to be done may vary over the test history; after each found error the counter starts again. The method ensures that the total uncertainty of the procedure is as desired.

Ramos [8] describes in Chap. 5 another approach on certifying software, namely based on the criterion that with high confidence the next software error is not found within a given time interval. Using a Bayesian framework, the procedures are worked out for several models: Jelinski-Moranda, Goel-Okumoto, and Run models. Each of these models is worked out in four cases, depending on the status of the initial number of errors and the error detection rate. Both parameters can be either known and fixed, or random (assuming for example that the initial number of errors is Poisson distributed). Together this gives four combinations. For each of these cases, an expression is given for the time interval in which with high confidence no error would be found if testing would continue.

13.4.5 Interaction Between Hardware and Software

Technical failure modes can be divided into three main groups: hardware failure modes, software failure modes, and the toughest failures to prevent however, are those caused by subtle interactions between hardware and software. Interaction failures, as being malfunctions of the system, may be caused by design faults in the software components which cannot deal with partial failures/disturbances of the hardware. On the other hand, resource leaks, race conditions, and wrongly designed exception codes may lead to interaction failures, such as electrical failures (short-circuiting, too high voltage/current), mechanical failures, and temperature effects (deformation of components). In spite of the progress of hardware/software co-design, hardware and software in an embedded system are usually considered separately in the design process. System failures often involve defects in both.

Software, especially in critical systems, tends to fail where least expected. Often engineers are good at setting up test plans for the main line code of the program, and

these sections usually do run with minor issues only. Software does not "break" but it must be able to deal with "broken" input and conditions, which are often causes for "software failures". The task of dealing with abnormal/anomalous conditions and inputs is handled by the exception code ("unhappy flows") dispersed throughout the program. Anomalous inputs can be due to failed/degraded hardware, material failures (e.g., corrosion), harsh/unexpected environmental conditions and multiple changes in conditions and inputs that are beyond what the hardware is able to deal with.

13.4.5.1 Fault Injection Technique

As the functions of SSL systems get more complex, it gets more difficult to detect faults that cause reliability troubles. Fault Injection Technique (FIT) is a technique that be used to detect those faults: it observes system behaviours by injecting faults into target system so as to detect interaction faults between hardware and software in a system. FIT first simulates behaviours of embedded system to software program from requirement specification. Then hardware faults, after being converted to software faults, are injected into the simulated program. And finally, effective test data are selected to detect faults caused by the interactions between hardware and software. For an extensive description of FIT we refer to refs. [11], and [12].

13.4.5.2 Model Based Assessment

This section discusses briefly an approach to model system reliability taking into account hardware and software failures, as well as hardware–software interaction failures. For such system reliability model assessment the principle of "Markov processes" can be applied.

The term "Markov model", named after the mathematician Andrei Markov, originally referred exclusively to mathematical models in which the future state of a system depends only on its current state, not on its past history. This "memory less" characteristic, called the "Markovian property", implies that all transitions from one state to another occur at constant rates. Much of the practical importance of Markov models for reliability analysis is due to the fact that a large class of real-world devices (such as electronic components) exhibit essentially constant failure rates, and can therefore be effectively represented and analyzed using Markov models. For any given system, a Markov model consists of a list of the possible states of that system, the possible transition paths between those states, and the rate parameters of those transitions.

Hardware–software interactions can be specified into two categories: partial and permanent hardware-related software failures. Figure 13.9 shows a presentation of the system reliability diagram.

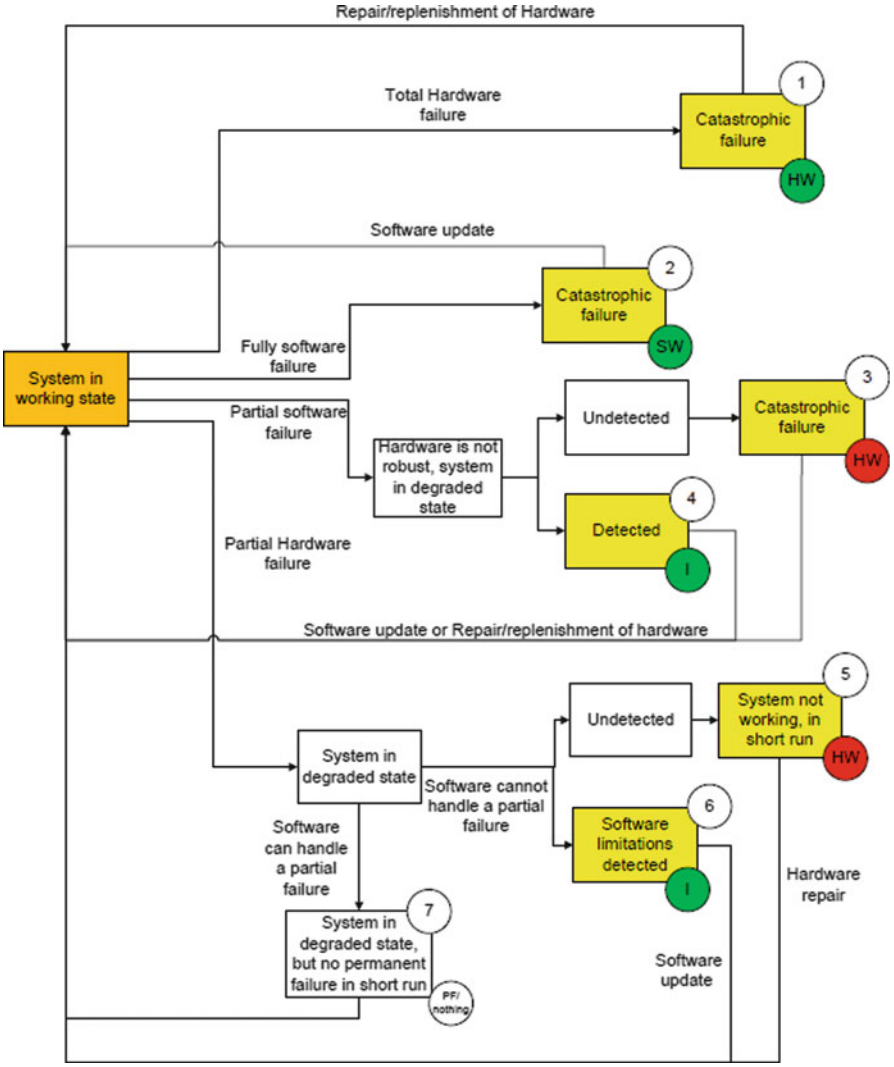


Fig. 13.9 System failure categories, interactions between hardware and software reliability

The reliability of the entire system equals

$$R_{\text{system}}(t) = R_s(t)R_h(t)R_{hs}(t)$$

where

$R_s(t)$ = reliability of software subsystem
$R_h(t)$ = reliability of hardware subsystem
$R_{hs}(t)$ = reliability of hardware–software interaction
$= P\{\text{No permanent failures at time } t\} \times P\{\text{No transient failures at time } t\}.$

Teng et al. [13] used the Markov approach to derive an explicit model to capture hardware–software interaction failures. They illustrated the combined hardware and software modelling approach by applying it to a real telecommunication system. We refer to Teng et al. for more reading. However, that is up to now, within SSL no application of this explicit model based assessment using Markov processes is known to the writers. We are convinced that this approach is very interesting from a development as well as from a business point of view.

13.5 System Reliability: A Practical Approach

13.5.1 Starting Points and Goal

The starting points of our approach are as follows:

1. There's information available on the reliabilities of the components, i.e.
   (a) Test data of the components, or
   (b) The supplier is able to provide the distribution(s)
2. The components are assumed to fail independently (or no real information on dependency)
3. The configuration of the components is known, that is series, or parallel, or a mix.

Goal: evaluation of system reliability, that is

1. Characterize the distribution of the survival time,
2. Derive the confidence intervals of properties like B10, B50, or MTTF,
3. Compare the outcomes with the system test.

13.5.2 Approach for Modeling System Reliability

Suppose the system consists of components in series. For the moment, we assume that they fail *independently* of each other (Section 13.4.3 deals with the extension of dependency). Then the survival probability equals $\hat{R}_{\text{system}}(t) = \prod_i R_i(t)$. In case the system structure is parallel or more complicated, this expression takes on a different form but the principle remains the same. This expression allows one to generate point estimates of B10, B50, or MTTF. What remains is to derive confidence intervals by

1. Bootstrap, in case the original data of the components is available,
2. Monte Carlo on model coefficients; sometimes a supplier is able to provide the covariance matrix of the model coefficients, or
3. Monte Carlo and bootstrap may be combined for the different pieces of information.

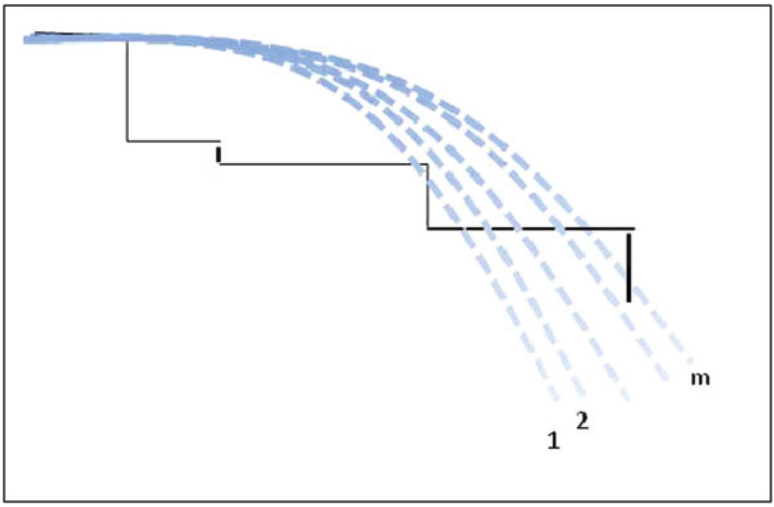


Fig. 13.10 $R_{\text{system}}(t)$ and system results (Kaplan Meier)

Result can be thought of as a (large) series of size m of estimates of possible functions $R_{\text{system}}(t)$. Perform an actual system reliability test, and see if its outcomes fit the estimates of $R_{\text{system}}(t)$, using a Kolmogorov-Smirnov or Log-rank test. Repeat this test m times, and consider the average size of these tests (Fig. 13.10).

A reason that it might not fit is because of the independent failure assumption. One can do two things:

1. Check if the final result changes much if the assumption is not true,
2. Calibrate the system reliability function so that it matches the test results using a Copula model.

Choose a copula family, e.g., an Archimedean or Gaussian copula. This copula is completely determined by its correlation matrix. Choose for example a matrix with all pair wise correlations equal, to ρ. For each ρ, the system reliability $R(t)$ can be evaluated. When $R(t)$ is plot for different ρ's, if possible against the empirical Kaplan-Meier estimates, this may give an impression of the role of dependency and which ρ gives the best fit to the system reliability test.

However, a single parameter ρ for all pair wise dependencies might be too simple. Perhaps there are two types A and B of components, in which case you might assume that all components of the same type have the same pair wise ρ. Then three ρ's would result. It is also thinkable to let the correlation matrix completely free, but the number of parameters increases quite fast with the number of components: e.g., 5 components have 10 pair wise correlations.

The system model could be calibrated to the results of the system test by choosing the best correlation parameters. This can be done via an optimization problem. The optimization problem then looks as follows.

- Objective: a measure of similarity between $R_{\text{systemmodel}}(t, P)$ and $R_{\text{systemtest}}(t)$. For instance, the test statistic from a log rank test; or the sum of squares of differences in R at a set of time points, or a measure of dissimilarity in "the horizontal direction": sum of squared differences of B10, B50, and other percentiles.
- Variables: the vector P. There should be as few different independent entries of the correlation matrix as possible (e.g., 1, 2, 3).
- Constraints:
  - The correlation matrix must be positive definite. This is not trivial, see below.
  - Possibly, an expert can state that some of the dependencies are nonnegative (i.e., $\rho >= 0$).

When varying the vector P, the correlation matrix must be a *correlation* matrix (mathematical term: positive definite). This is similar to the fact that a standard deviation cannot be negative. Intuitively, if survival times of components 1 and 2 have a high dependency, and likewise for components 2 and 3, then components 1 and 3 must also have a high dependency. The check if a given matrix is positive definite is quite technical, and there are several options: via Cholesky decompositions, calculation of eigen values, or via determinants of sub matrices. The last option allows for a closed-form expression to evaluate the constraints, required for many optimization algorithms.

13.6 Conclusions

System reliability is complex and needs fundamental understanding from both a statistical and physical point of view. Statistical methods at hand are described in this chapter; the physical part relates to failure modes and failure mechanics topics that are discussed in the previous chapters. For hardware reliability, theories are at hand and frequently used in several industries. For software reliability, this chapter outlines an approach that can be used to tackle it. Eventually, interactions between the two, denoted as i-ware reliability, will become a challenging task from a statistical point of view.

References

1. Birnbaum ZW (1969) On the importance of different components in a multicomponent system. Multivariate analysis 2. Academic, New York, pp 581–592
2. Levitin G, Podofillini L, Zio E (2003) Generalized importance measures for multistate elements based on performance level restrictions. Reliab Eng Syst Saf 82:63–73
3. Nelsen RB (2006) An introduction to Copulas, 2nd edn. Springer-Verlag, New York
4. Demarta S, McNeil AJ (2005) The t copula and related copulas. Int Stat Rev 73:111–129
5. Alink SHF (2007) Copulas and extreme values. PhD thesis, Radboud University Nijmegen

6. Stefano Demarta e.a. (2005) The t copula and related copulas. http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.71.1228
7. Pham H (2006) System software reliability. Springer-Verlag, London
8. Ramos C (2009) Statistical procedures for certification of software systems. PhD thesis, Eindhoven University of Technology
9. Currit PA, Dyer M, Mills HD (1986) Certifying the reliability of software. IEEE Trans Software Eng 11(12):1411–1423
10. Di Bucchianico A, Groote JF, van Hee KM, Kruidhof R (2008) Statistical certification of software systems. Commun Stat Simul Comput 37(2):346–359
11. Benso A, Prinetto P (2004) Fault injection techniques and tools for embedded systems reliability evaluation. Kluwer Academic Publishers, Dordrecht
12. Durães JA, Madeira HS (2006) Emulation of software faults: a field data study and a practical approach. IEEE Trans Software Eng 32(11):849–867
13. Teng X, Pham H, Jeske D (2006) Reliability modeling of hardware and software interactions, and its applications. IEEE Trans Reliab 55(4):571–577

Chapter 14
Prognostics and Health Management

M.G. Pecht

Abstract There is a need to acquire knowledge of LED's life cycle loading conditions, geometry, and material properties to identify potential failure mechanisms and estimate its remaining useful life. The physics-of-failure (PoF) approach considers qualification as an integral part of design and development and involves identifying root causes of failure and developing qualification tests that focus on those particular issues. PHM-based-qualification combined with the PoF qualification process can enhance the evaluation of LED reliability in its actual life-cycle conditions to assess degradation, to detect early failures of LEDs, to estimate the lifetime of LEDs, and to mitigate LED-based- product risks. Determination of aging test conditions better designed with PHM-based-qualification enables more representation of the final usage conditions of the LEDs.

14.1 Introduction

We introduce prognostics and health management to improve LED reliability and qualification techniques in this section. Prognostics and health management (PHM) is composed of health management and prognostics. Health management is based on health monitoring. Heath monitoring is defined as ability to sense the instantaneous condition of the product. This means in situ performance monitoring. Prognostics are defined as ability to extrapolate forward to predict remaining useful life (RUL). Purpose of developing PHM is to assess the degree of deviation or

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degradation from an expected normal operating condition for electronics. Goals of PHM comprise [1]:

- Providing warning of failures in advance
- Minimizing unscheduled maintenance, extending time duration of maintenance cycle, and maintaining time repair action effectively.
- Reducing life cycle costs of equipment
- Improving qualification and helping design and logistical support of future products

Prognostics need sensing capability to monitor the history of stress exposures throughout the life cycle. Prognostics also need a model-based capability and/or other suitable method to assess life consumed and life remaining. Approaches to prognostics are classified into PoF-based prognostics (quantitative and proactive), data-driven prognostics, and Fusion prognostics combining the advantages of the PoF and data-driven approaches. Data-driven prognostics use statistics and probability for analyzing current and historical data to estimate RUL.

14.2 PoF-Based Prognostics

PoF-based prognostics utilize knowledge of a product's life cycle loading conditions, geometry, material properties, and failure mechanisms to estimate its remaining useful life. PoF utilization in PHM includes the following [2]:

- Virtual life assessment with design data and expected life-cycle conditions
- Identification of critical failure mechanisms (through FMMEA: failure modes, mechanisms, and effects analysis)
- Selection of precursor parameters to monitor
- Development and implementation of canaries
- Calculation of remaining useful life (RUL)

Based on the monitored operational and environmental data, the health status of the electronics product can be assessed. Damage of parts or product can be evaluated by PoF-based physical models to get RUL. PoF-based PHM methodology is summarized in Fig. 14.1.

There is known history of canary birds used in early coal mines to detect the presence of hazard gases. Failure of the canary served as early warning to miners of health hazards. Since canaries are more sensitive to hazardous gases than humans, the death or sickening of the canary was an indication to the miners to get out of the shaft. Canary refers to embedded devices that are used to predict the degradation and provide early warning of impending failure of the host. Canary devices sense stress conditions in the host and degrade faster than the host system so that impending catastrophic failure can be anticipated and preempted before occurrence.

Reliability is the foremost concern for many companies, especially for aerospace, medical, and military industries because the failure of the products during operation can be catastrophic. It is not always safe and economical to conduct regular maintenance. In other words, benefits of canary devices are:

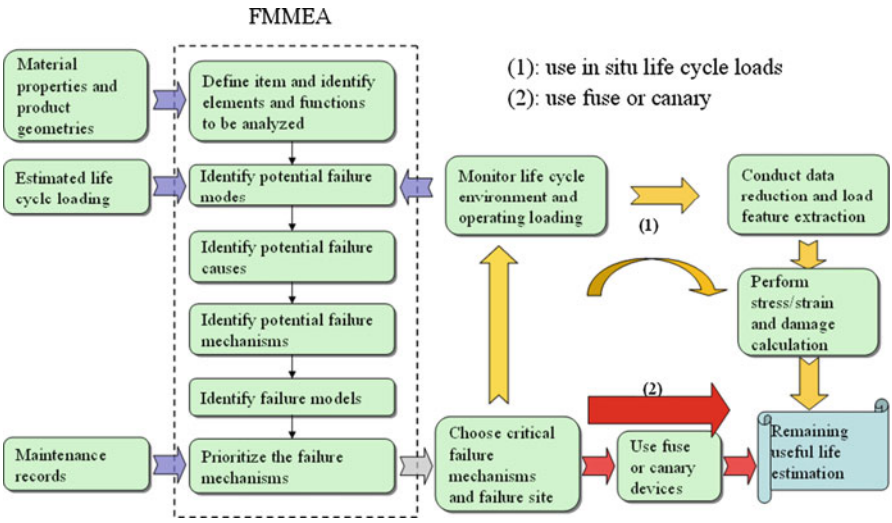


Fig. 14.1 POF-based PHM methodology

- Physical mechanism that directly measures the cumulative environmental exposure indicates that a system may soon fail.
- Canaries store environmental life history of equipment for trouble shooting/repair.
- Canaries provide information on suitable qualification test levels.
- Canaries offer data that can be used to make real time adjustments to other predictive methods such as PoF and empirical approaches.

Types of expandable canaries can be divided into overstress canaries and wear-out canaries. Overstress failure occurs when stress exceeds strength. Overstress failures include dielectric breakdown, electrostatic discharge (ESD), and die fracture. Overstress canaries will be developed for large stress events that can cause latent damage and subsequent premature failure or designed to act as a sacrificial element that eliminates the stress-flow path before the overstress event can damage costly functional elements. Wear-out failure is caused by gradual increase of cumulative damage. Examples of wear-out failure are electromigration, interconnect fatigue, Sn whisker growth, corrosion, and time dependent dielectric breakdown caused by tunneling mechanisms. Wear-out canaries will be developed for accelerated tracking of cumulative damage under life-cycle stresses.

Technically a canary can be any device that wears out faster than the actual product. The approach for controlled error-seeding in canaries includes three-inter-related techniques that will be used individually or synergistically to enhance the damage accumulation rates in the canaries: geometric error-seeding, material error-seeding, and load error-seeding.

- Geometry error-seeding: the canary geometry is designed to increase stress conditions at the failure site beyond the levels experienced in corresponding

functional elements. Canary solder joints can be designed to have lower height than normal ones to attain faster degradation rates. Canaries for electrochemical migration are designed with closer spacing to increase degradation rates.

- Material error-seeding: the composition and microstructure of canary can be tailored to alter material properties. The material properties include dielectric constants, dielectric strength, glass-transition temperature, diffusivity, creep resistance, ductility, and fracture toughness. Preliminary concepts are being explored for tin whisker canaries using compositional gradient libraries deposited on glass substrates.
- Load error-seeding: the canary will be subjected to higher load levels than functional elements. Canaries for conductive filament formation in metal traces will be subjected to higher voltage gradients than normal. Electromigration canaries in solder and die metallization will be subjected to higher current densities than normal. Microvia fatigue canaries will be subjected to higher current swings.

Design steps of expendable canaries include the following:

- Identify the failure mechanisms of host systems.
- Find out what governing parameters or equations (material properties, physical size, usage, and environmental conditions) can affect these failure mechanisms.
- Design canaries with adjusted governing parameters.
- Determine the appropriate equipment for (a) measuring these governing parameters and (b) applying accelerated or real-situ loading stress.
- To conduct experiments and find out the coefficients in governing equations.
- To develop a model which correlates the failure of canaries with that of host systems so that RUL can be quantified based on the health state of canaries.

Sensory canaries are inspired by biological system focusing on self-cognizant systems with in situ canary capabilities to look, listen, smell, and feel for signs of degradation and impending failure. Guidelines of sensory canaries are being developed to make the canary approach generic for both new and legacy information systems.

- Infrared canaries are to look for degradation in microprocessors based on changes in the thermal dissipation
- Impedance spectroscopy and time domain reflectometry are to listen for defects in signal traces and wiring harnesses.
- Acoustic sensors are to listen for delamination and cracking
- MEMS-based chemical canaries are to smell for out-gassing products.
- Piezoelectric or piezoresistive canaries are to touch and feel for sign of delamination.

Conjugate-stress canaries can be developed to provide prognostic assessments based on simultaneous identification of conjugate-stress pairs (e.g., stress & strain; temperature gradient & heat flux; voltage and charge flux density; and magnetic

field and magnetic induction), using novel dual-field detector pair concepts. These canaries provide model-based fusion prognostic assessments of RUL by:

- Providing stress histories for damage accumulation models
- Monitoring intrinsic changes in material properties due to damage (e.g., stiffness, thermal/electrical conductivity, and dielectric constants)
- Monitoring other damage metrics; e.g., hysteretic energy dissipation at failure site

Interconnect canaries built in one same system can be connected together to form a built-in canary network by using wireless or wired network, or optical fiber communication systems. The canary network has advantages over an individual canary because it can cover a much wider area of communication and provide distributed early warnings of failures.

In summary of canaries, PHM is attracting more attention from industry due to the increasing demand for reliable products from both consumers and critical applications such as military, aerospace, and nuclear power plants. As an approach of PHM, canary has an intrinsic capability of providing advance warning of host system failure and prediction of its health state, by accelerating the degradation rates within the canary and providing more information about the actual life cycle stresses at potential failure sites. Canaries should degrade faster than their host systems under the same loading conditions.

14.3 Data-Driven Approaches for PHM

Data-driven techniques (also known as empirical approaches) use historical information to statistically and probabilistically determine anomalies and make predictions about the RUL of systems [3]. Data-driven techniques are needed due to following reasons:

- As systems become increasingly complex, performing PHM efficiently and cost-effectively becomes a challenge.
- Conducting FMMEA may not be cost effective for a complex system.
- The only kinds of information available regarding the system may be performance data.
- Data-driven approaches for PHM are useful for complex systems where the knowledge of the underlying physics of the system are absent and when the health of large multivariate systems is to be assessed.
- DD techniques are capable of intelligently detecting and assessing correlated trends in the system dynamics to estimate the current and future health of the system.

Prognostics include steps of anomaly detection, diagnosis, and prognosis as shown in Fig. 14.2. Anomaly detection process is to know where an anomaly in the system of interest is detected. The goal of anomaly detection is to extract underlying structural information from the data, to define normal structure, and to

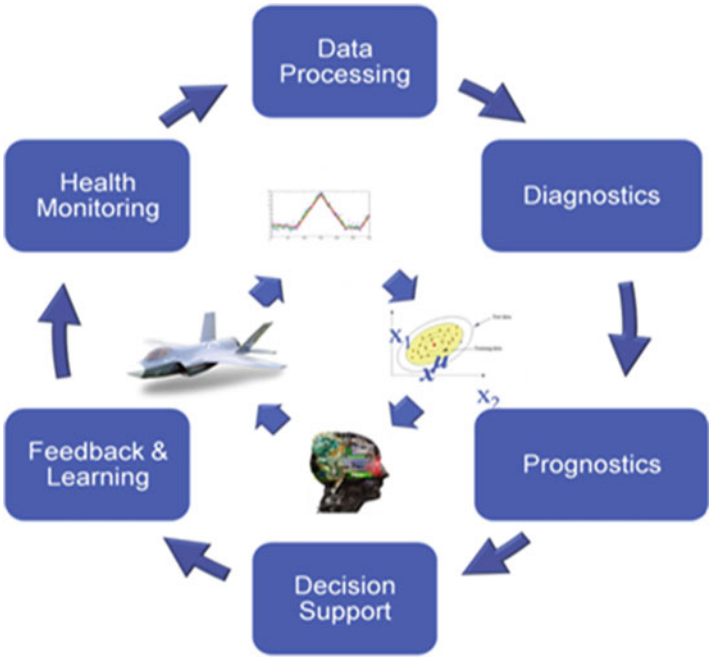


Fig. 14.2 PHM cycle

identify departures from such normal structures [4]. Diagnosis step is useful to recognize where the fault is identified and isolated. Prognosis step predicts a failure. The prediction can be based on a comparison of the current state of the system and the expected normal state, in addition to the continued tendency of the system to deviate from the expected normal state.

Statistical methods are composed of parametric methods and nonparametric methods [5]. Parametric methods assume that the data are drawn from a certain distribution (for example, the Gaussian distribution) and that the parameters (such as the mean and the standard deviation) of the distribution are calculated from the data. Nonparametric methods do not make any assumptions regarding the underlying distribution of data. These methods draw their strength from the data and its inherent features (e.g., Mahalanobis distance).

Machine learning (ML) algorithms recognize patterns in data and make decisions on the state of the system based on the data [6]. General procedures for learning algorithms are shown in Fig. 14.3. Three types of learning algorithms are supervised, semi-supervised, and unsupervised techniques.

The translation from raw data to meaningful information may be achieved by using techniques like classification, clustering, regression, and ranking. ML based on statistical methods is suited for PHM because it is capable of actively learning about the system and its dynamics, faults, and failures. ML techniques can handle the increasing complexity of system information. ML is useful for real time analysis.

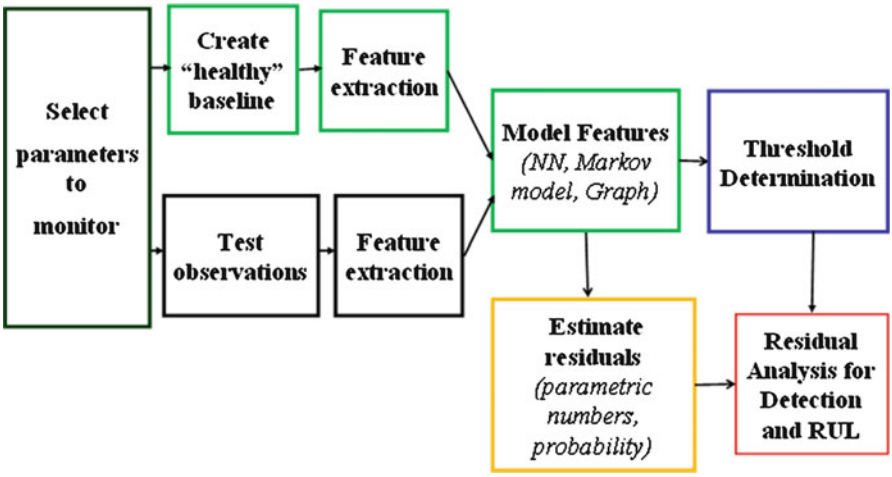


Fig. 14.3 Machine learning algorithms

Prognostic measurements are processed by identification of new nonzero states, change in state probabilities, changes in the amount of time a system can stays in a state, changes in the time and probability to reach a particular state, and time to reach a particular state. The example of data driven prognostics is shown in Fig. 14.4.

Data-driven algorithms used at Center for advanced life cycle engineering (CALCE) for prognostics include [3]:

- Mahalanobis distance clustering
- Principle component analysis (PCA)
- Support vector machine (SVM)
- Sequential probability ratio test (SPRT)
- Gaussian processes (GPs)
- Bayesian support vector machine (BSVM)
- Neural networks (NN)
- Self-organizing map (SOM)
- Particle filtering (PF)

The each algorithms are not be covered by this chapter. Please refer to a book written by Prof. M. G. Pecht, "Prognostics and Health Management of Electronics", published in A John Wiley & Sons, Inc. in 2008.

Anomaly detection is required to perform data-driven PHM techniques shown in Fig. 14.5. Data-driven PHM techniques are performed by following in steps of collection of raw data, feature selection, anomaly detection, diagnostics, and prognostics.

Nature of input data can be classified into categorical data and real-valued data shown in Fig. 14.6. Categorical data is a part of an observed dataset that consists of categorical variables (which are variables assessed on a nominal scale) or for data that has been converted into the form (e.g., grouped data) [4]. Real-valued

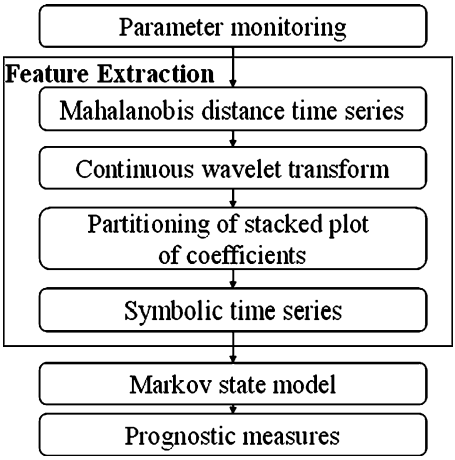


Fig. 14.4 Example of data-driven technique

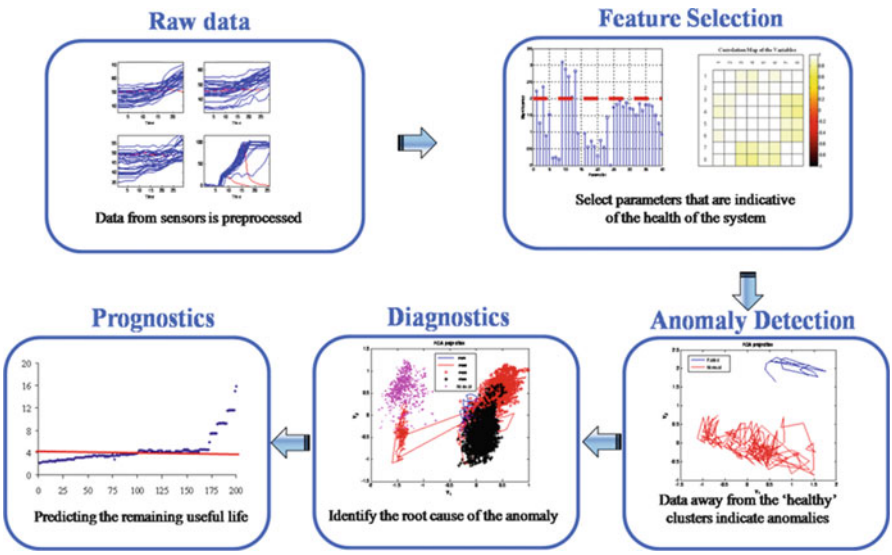


Fig. 14.5 Data-driven PHM flow

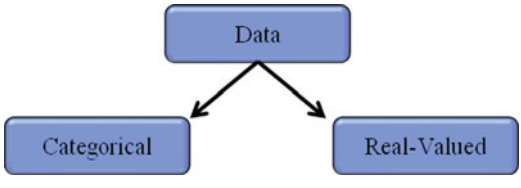


Fig. 14.6 Nature of input data

(continuous) measurements are collected from sensors that measure physical properties such as voltage, current, and speed. They have traditionally been the primary data source for monitoring applications because they allow one to trend subtle changes over time. Categorical data can include error logs, fault messages, and warnings that are either of textual nature or binary flags. Some of the fault messages can be triggered, for example, when real-valued measurements are beyond certain thresholds or more generally when the subsystem behaves outside preset operating parameters. Real-valued data are often prior to their usage to enhance their usefulness in the prognostic applications. Understanding the data needs to acquire following information:

- Meaning of each variable
- Data formatting (software reads correctly)
- Ranges of variables
- Duplications
- Outliers (e.g., errors)
- Graphics and summaries
- Domain knowledge

Data preparation needs:

- Choice of variables
- Choice of scales (continuous/categorical)
- Binning
- Missing values
- Extent/type
- Drop observations or drop variables (replace with dummy)
- Impute (mean, regression, more advanced methods)
- Explanatory vs. predictive
- Creating derived variables

Some preprocessing techniques including outlier removal, noise reduction, and transformation into other domains are used to select features of data. Examples of outlier, filtering, and transformation of domain are shown in Fig. 14.7. Outlier is value far away from most others in a set of data [5] (for example, temperature of 2,000 °C in computer). Anomaly is defined as deviation or departure from the normal order.

Anomaly detection is finding patterns in data that do not conform to expected behavior. Anomalies in data provide significant, and often critical, information in a wide variety of application domains. Examples of applications are [4]:

- Fault detection (spacecraft, airplanes, and laptop computers)
- Fraud detection in credit cards, insurance, or health care
- Medical diagnosis and public safety (disease outbreaks)
- Intrusion detection (cyber security)
- Military surveillance

Types of anomalies can be divided into point anomalies, contextual anomalies, and collective anomalies [4]. Point anomalies are that an individual data instance is

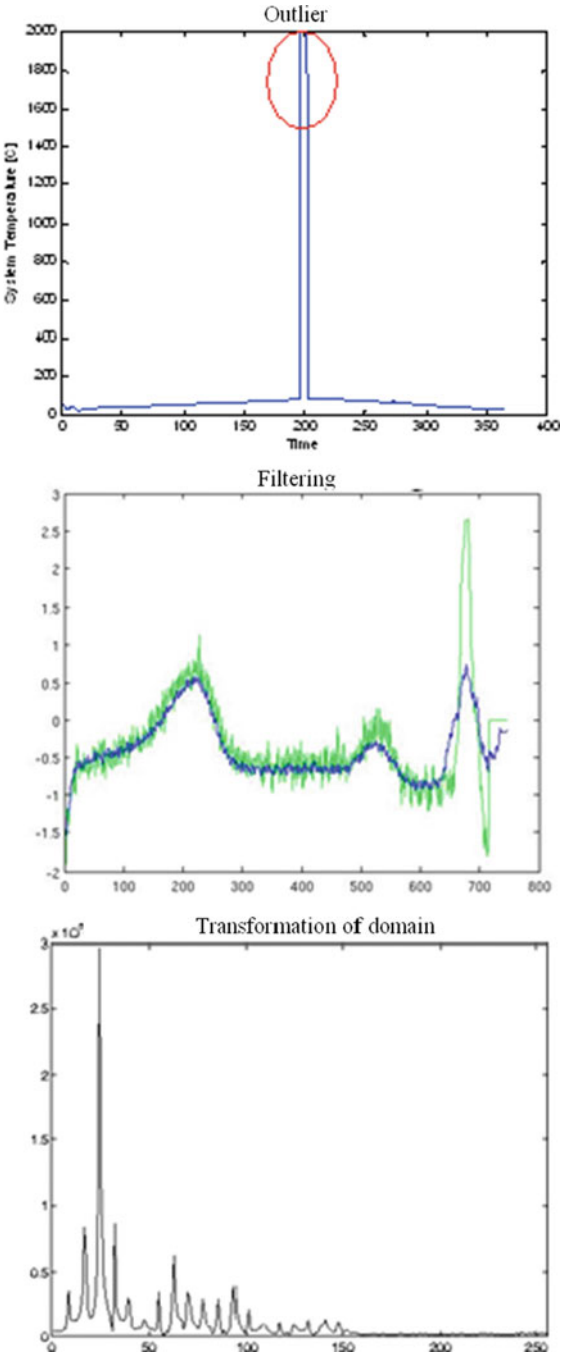


Fig. 14.7 Outlier, filtering and transformation of domain for data preprocessing

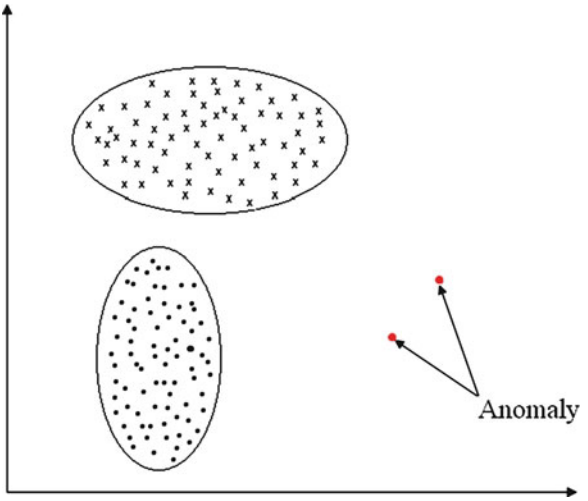


Fig. 14.8 Example of point anomalies

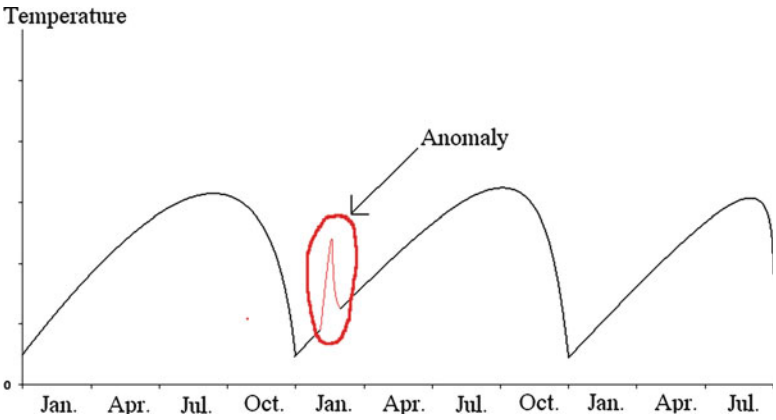


Fig. 14.9 Example of contextual anomalies

anomalous compared to the rest of the data shown in Fig. 14.8. Contextual anomalies are that data instance is anomalous only in a particular context shown in Fig. 14.9. High temperature in the month of January is anomalous although the high temperature in the month of July is not anomalous. Collective anomalies are that collection of related data instances is anomalous in Fig. 14.10. The individual data instances may not be anomalous by themselves.

Machine learning techniques can be divided into supervised, semi-supervised, and unsupervised algorithms [6]. Supervised learning techniques require training data set that has labeled data for normal as well as anomaly classes. Semi-supervised learning techniques can use training data that has labeled instances

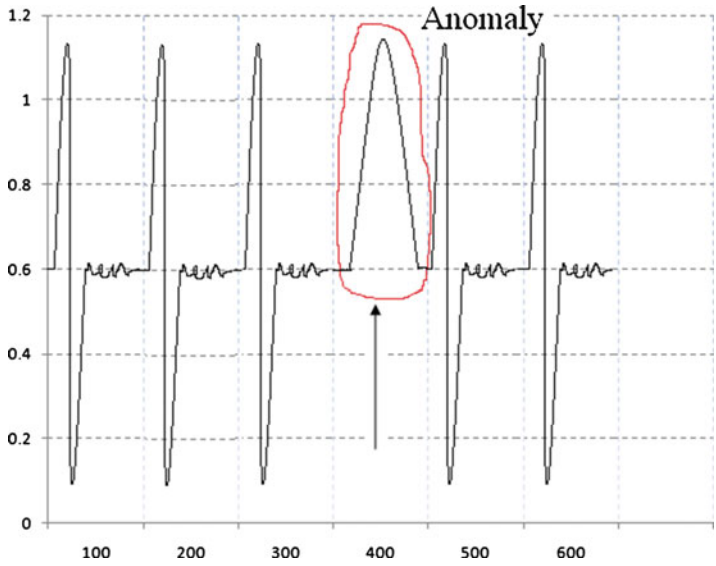


Fig. 14.10 Example of collective anomalies

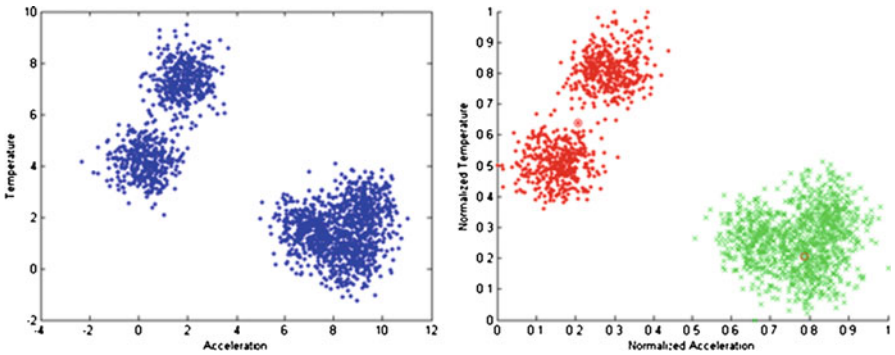


Fig. 14.11 Hypothetical example

only for the normal class. Unsupervised learning techniques may not require training data. They assume that normal instances are more frequent than anomalies. Machine learning techniques can handle the increasing complexity of system information. In other words, machine learning for PHM can actively learn the system and its dynamics, faults, and failures.

Techniques for point anomaly detection include classification based techniques, nearest neighbor, clustering, statistical (e.g., hypothesis test), and spectral techniques [4]. Input data can be collected by building matrix. Columns contain variables and rows contain instances. Example is temperature as a junction of acceleration for some system shown in Fig. 14.11.

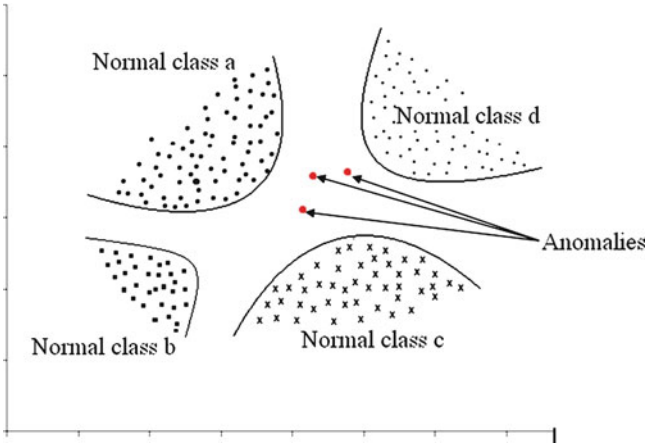


Fig. 14.12 Multi-class anomaly detection

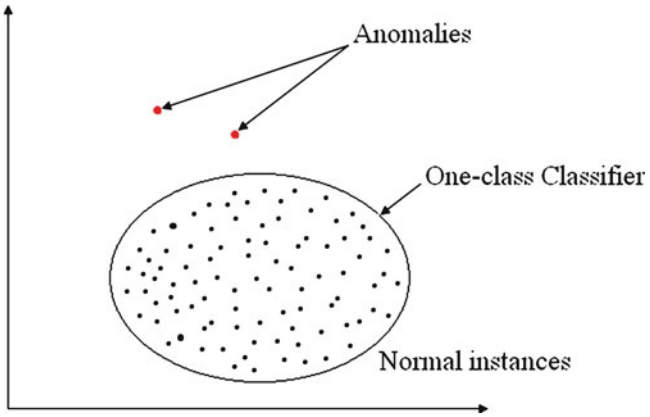


Fig. 14.13 One-class anomaly detection

Classification based anomaly detection build a classification model for normal and anomalous events based on labeled training data, and use it to classify each test instance. Assumption is that a classifier which can distinguish between normal and anomalous class can be learned with a given training set. There are two classification based techniques in terms of training data available.

- Multi-class training is capable of operate in semi-supervised or supervised mode.
- One-class training can operate in semi-supervised or unsupervised mode.

Multi class technique assumes training data contains instances belonging to multiple normal classes. Test data is anomalous if it belongs to none of the normal classes shown in Fig. 14.12. One-class technique assumes all training data belong to only one normal class shown in Fig. 14.13.

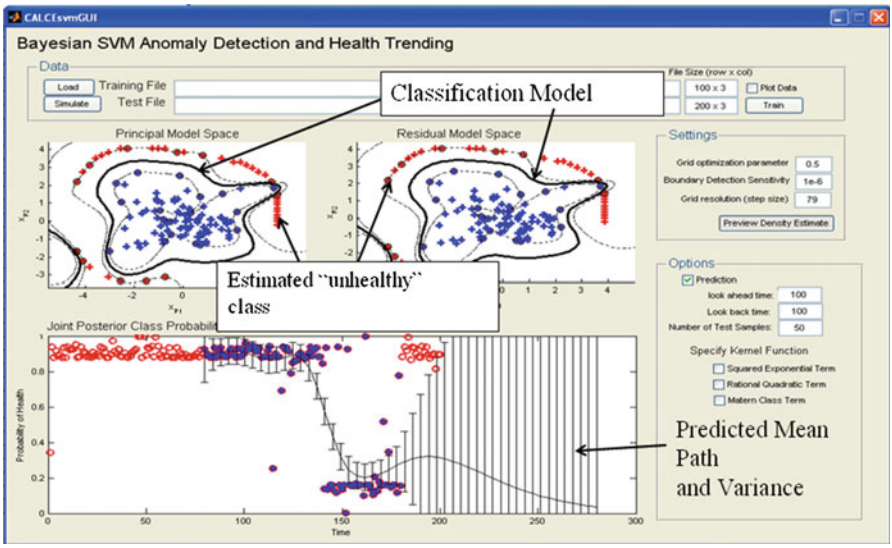


Fig. 14.14 Support vector machines

Algorithms in classification based techniques are neural networks based algorithm, Bayesian networks based algorithm, support vector machines (SVM) algorithm, and rule based algorithm. Example of SVM is shown in Fig. 14.14. Neural networks based algorithm works in both multi-class and one-class settings. Two steps are:

- First, a neural network is trained on the normal training data to learn different classes.
- Second, each test instance is provided as an input and if the networks accept the test input, it is normal.

Bayesian networks based algorithm works in multi-class setting. It estimates the expectancy that the test instance belongs to the normal or anomaly class label. It also assumes independence between the different attributes. SVM creates a boundary around the region containing the training data. SVM determines if the test instance falls within the boundary. SVM declare anomalous if it does not fall within the boundary. Rule based algorithm works in multi-class as well as one-class setting. Two steps of rule based algorithm are:

- Learn rules regarding the normal behavior of a system from training data (e.g., by using decision trees)
- Find the rule that best captures each test instance.

Nearest neighbor based anomaly detection assumes that normal data instances occur in dense neighborhoods, anomalies occur far from their closest neighbors [7]. Concept is shown in Fig. 14.15. Each circle corresponds to a group of nearest neighbor. Nearest neighbor based anomaly detection utilize a distance/similarity measure between data instances. Two-step approach includes:

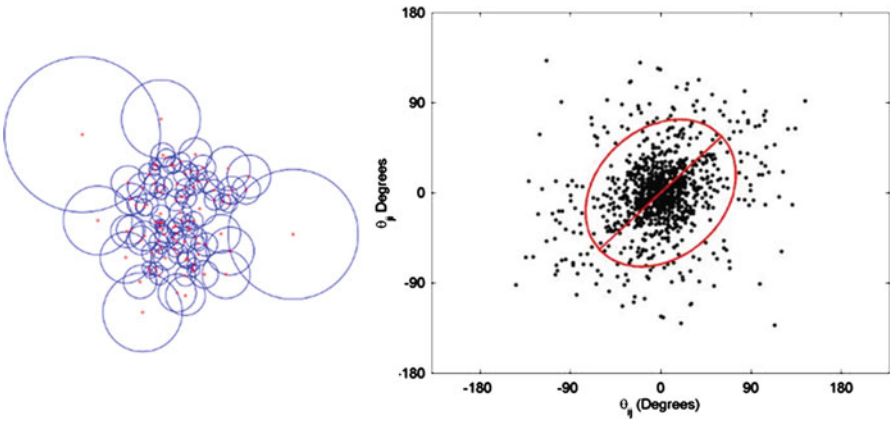


Fig. 14.15 Nearest neighbor

- Compute neighborhood for each data record.
- Analyze the neighborhood to determine whether data is anomaly or not.

This can result in misclassification if normal instances do not have sufficient neighbors or anomalies have close neighbors.

Nearest neighbor based techniques are categorized into Kth nearest neighbor and relative density based technique. In case of kth nearest neighbor technique,

- Distance of test instance to the kth nearest neighbor is calculated.
- To determine if test instance is anomalous, a threshold value is chosen based on experience.

In case of relative density based technique,

- The density of the neighborhood of each data instance is estimated.
- Test instance in a low density neighborhood is declared anomalous, and instance that lies in a dense neighborhood is declared to be normal.

Clustering based anomaly detection technique utilizes primarily an unsupervised or semi-supervised technique to group similar data instances into clusters [4, 7]. Clustering based anomaly detection technique is distinct from the nearest neighbor based technique such that clustering based technique evaluates each instance with respect to the cluster it belongs to while nearest neighbor based technique analyzes each instance with respect to its local neighborhood. Several techniques are effective only when the anomalies do not form significant clusters among themselves. Three categories for detection are used with different assumptions. The assumptions of category 1, category 2, and category 3 are:

- Assumption of category 1: normal data instances belong to a cluster in the data, while anomalies do not.
- Assumption of category 2: normal data instances lie close to the nearest cluster centroid while anomalies are far away.

- Assumption of category 3: normal data instances belong to large and dense clusters, while anomalies either belong to small or sparse clusters.

Statistical methods have an underlying principle such that an anomaly is an observation which is suspected of being partially or wholly irrelevant because it is not generated by the statistical distribution assumed [4, 5]. Assumption is that normal data instances occur in high probability regions of distribution, while anomalies occur in the low probability regions of the distribution. Statistical methods fit a statistical model to the given data (usually for normal behavior) and apply a statistical inference test to determine if the test instance belongs to this model. The confidence interval associated with anomalies can be used as additional information while making a decision. Two categories are:

- Parametric techniques
  - Assumption: normal data is generated by a parametric distribution with parameters φ and probability density function $f(x; \varphi)$, where x is an observation.
  - Parameters are estimated from the given data, and a statistical hypothesis test is used for anomaly detection.
- Nonparametric techniques.
  - The data structure is not defined a priori, but is instead determined from the given data.
  - Typically makes fewer assumptions regarding the data.

Spectral anomaly detection techniques have an assumption such that data can be embedded into a lower dimensional subspace in which normal instances and anomalies appear significantly different. The approach adopted is to determine subspaces wherein the anomalous instances can be easily identified. For example, principle components analysis (PCA) can be used to find the projections along subspaces which will separate the anomalies based on variance. A preprocessing step can be used for existing anomaly detection technique in the transformed space.

Examples of problem settings depending on data set are discussed here. In case of data set 1 shown in Fig. 14.16, normal data are generated from a Gaussian distribution. Anomalies are generated from another Gaussian distribution whose mean is far from the first. Training data set from normal data set is available. In data set 1, all discussed anomaly detection techniques are able to detect the anomalies in this case.

In data set 2 shown in Fig. 14.17, normal data are generated by large number of Gaussian distribution. One-class classification technique fails to detect anomalies. Multi-class classification technique will detect anomalies. Clustering based, nearest neighbor based, and spectral based techniques will also detect these anomalies.

In data set 3 shown in Fig. 14.18, anomalous instances form a tight cluster of significant size at the center. Clustering based and nearest neighbor based techniques will treat these anomalies as normal. Spectral technique will perform better to detect these anomalies.

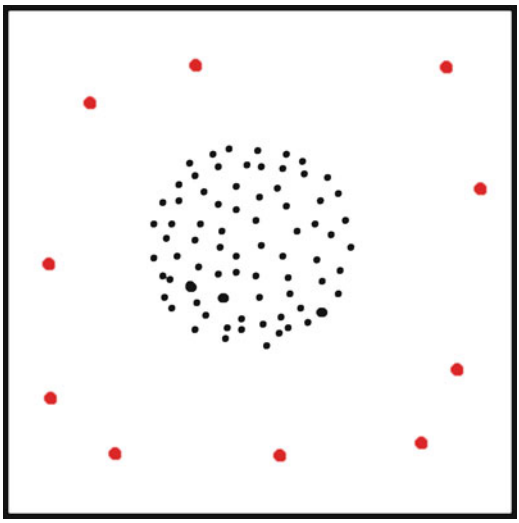


Fig. 14.16 Data set 1

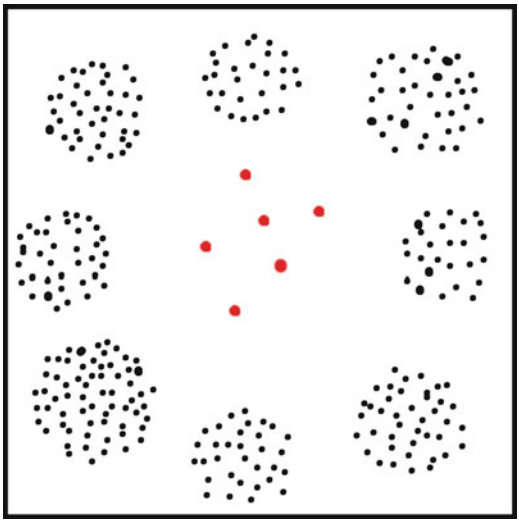


Fig. 14.17 Data set 2

Classification based techniques require labeled training data for both normal and anomaly classes [8]. Nearest neighbor and clustering based techniques suffer when number of dimensions is high. When identifying a good distance measure is difficult, classification based and statistical techniques are better. Statistical techniques are effective with low dimensional data and when the statistical assumptions hold true. Spectral techniques are good only if anomalies are separable from normal states in the projected subspaces.

Previous techniques primarily focus on detecting point anomalies. Contextual anomaly detection works where data instances tend to be similar within a context.

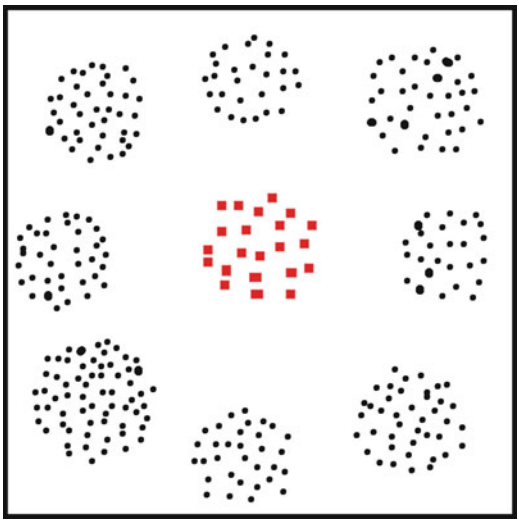


Fig. 14.18 Data set 3

Contextual anomaly detection techniques are able to detect anomalies that might not be detected by point anomaly detection techniques that take global view of the data. It is applicable only when a context can be defined. Two methods of handling contextual anomalies: conversion to point anomaly detection problem and utilization of the structure of the data.

- Conversion to point anomaly problem:
  - Splits data into different contexts or attributes.
  - Uses point anomaly detection techniques on each of the attributes within a context.
- Utilization of structure of the data:
  - Used when data cannot be split into contexts
  - A model is learned from the training data, which can predict the expected behavior with respect to a given context.
  - Anomaly is declared if the expected behavior is significantly different from observed behavior.

Collective anomalies are subset of instances that occur together as a collection [4]. Handling collective anomalies are more challenging than point and contextual anomaly detection. Data is presented as a set of sequences. Primary requirement is the presence of relationship between data instances. Collective anomalies are detected mostly by building models using sequential training data. Sequential anomaly detection detects anomalous sequences or subsequences in a database of sequences. To handle collective anomalies, the sequences are transformed to a finite feature space. Sequences may or may not be of the same length. Sequential rules are generated from a set of normal sequences. The test sequence is compared to the

rules, and anomaly is declared if it contains patterns for which no rules have been generated. For long sequences, one can assume that the normal behavior follows a defined pattern. If a subsequence within the long sequence does not conform to the pattern, it declares anomalous.

Challenges in anomaly detections are:

- It is difficult in defining a normal (healthy) operating region that encompasses every possible normal behavior of the system.
- The boundary between normal and anomalous behavior is often not precise.
- Normal behavior changes with time.
- The definition of an anomaly is application specific (e.g., fluctuations in body temperature).
- Uncertainties make data analysis difficult if there is noise in data.
- Availability of labeled data for training/validation of models used by anomaly detection techniques is usually a major issue.

14.4 Fusion Prognostics

The PoF-based prognostics involve the usage of representative models that allow estimation of damage and degradation in critical components as a function of the life cycle loads. The PoF approach utilizes knowledge of a product's life cycle loading conditions and material properties to identify critical failure mechanisms and estimate RUL. Advantages and limitations of PoF-based prognostics are:

- Advantages:
  - Provide estimate of damage and RUL for given loading conditions and failure modes or mechanisms (in operating and nonoperating state).
  - Identify critical components and parameters to be monitored.
  - Provide information regarding failure modes and mechanisms that are useful for root cause analysis.
- Limitations:
  - Development of models of the degradation process in a complex system may be practically infeasible.
  - System specific knowledge is necessary to create and use the system models which may not always be available.
  - It is hard for PoF models to detect intermittent failures.

The data-driven approach derives features from product performance data using statistical and machine learning techniques to estimate deviations of the product from its healthy state. Advantages and limitations of data-driven prognostics are:

- Advantages:
  - Do not require system specific knowledge (i.e., material properties, geometry, or failure mechanisms).

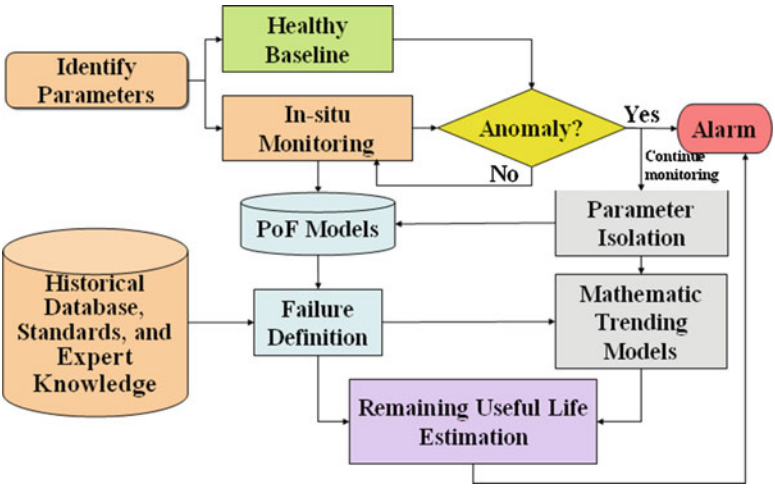


Fig. 14.19 Fusion prognostics approach

  - Can detect intermittent failures.
  - Capable of capturing complex relationships (between subsystems and environment), reduce dimensionality and thus can be used for complex systems.

- Limitations:

  - In some cases, reliable training data is required to create a baseline.
  - Cannot identify failure mechanisms.
  - It is difficult to estimate RUL without complete historical knowledge (run-to-failure data) of system parameters.

The conceptual explanation of fusion prognostics is depicted in Fig. 14.19. For a complex system, high dimensions may be required to monitor what can be monitored. Not all the parameters are related to anomalies or failures of the system. PoF methods can assist the parameter identification. Potential failure modes, causes, mechanisms, and models of a product under an environmental and operational condition can be identified by PoF method (e.g., failure modes, mechanisms, and effects analysis (FMMEA)). The parameters to monitor and the sensing locations can be identified based on the failure mechanisms and models. PoF methods may not identify all the parameters related to anomalies or failures.

Data-driven methods can identify other parameters. Relationship (e.g., correlation or covariance) between parameters and the principle parameters relative to anomalies can be identified by data-driven methods. Anomaly detection can be done by data-driven methods. Features of monitored data can be extracted, for example:

- Statistical characteristics, e.g., range, mean, standard deviation, and histogram
- Similarity measures and distance measure: e.g., Euclidean distance and Mahalanobis distance
- Relationship between parameters: e.g., correlation and covariance
- Residuals: e.g., between actual measurement and the estimation

Mathematical tools can be used to detect the anomalies by analyzing extracted features. Mathematical tools can be sequential probability ratio test (SPRT), PCA, neural networks, and support vector machines (SVM).

Failure can be predicted by PoF models assisted by data-driven methods. Parameters responsible for the anomalies or failures can be isolated by data-driven methods (e.g., PCA). Proper PoF models from a database can be extracted. Failure can be predicted by the extracted model. Failure can be also predicted by data-driven methods. Mathematical tools can conduct the trending or regression based on the features of the isolated parameters. Failure criteria can be obtained from standard, PoF models, historical databases, or expert knowledge. Decision making will be performed if multiple predictions are available. Examples of decision making are choosing conservative one or utilizing methods such as Dempster-Shafer method and fuzzy fusion.

Capability of fusion prognostics are: it aggregates the strengths of PoF and data-driven approaches to improve the capability of PHM for system health assessments and prognostics; it is capable of detecting intermittent failures; and it can provide information about the failure modes and mechanisms occurring in the system which can be used for root cause analysis.

References

1. Pecht MG (2008) Prognostics and health management of electronics, chap. 1. Wiley, Hoboken, NJ, pp 3–4
2. Pecht MG (2008) Prognostics and health management of electronics, chap. 4. Wiley, Hoboken, NJ, pp 73–84
3. Pecht MG (2008) Prognostics and health management of electronics, chap. 3. Wiley, Hoboken, NJ, pp 47–72
4. Chandola V, Banerjee A, Kumar V (2009) Anomaly detection: a survey. ACM Comput Surv 41 (3) Article 15: 15:1–15:58
5. Markou M, Singh S (2003) Novelty detection: a review-part 1: statistical approaches. Signal Process 83:2481–2497
6. Nilsson NJ. Introduction to machine learning. http://ai.stanford.edu/~nilsson/mlbook.html
7. Tran TN, Wehrens R, Buydens LMC (2006) KNN-kernel density-based clustering for high-dimensional multivariate data. Comput Stat Data Anal 51(2):513–525
8. Xu R (2005) Survey of clustering algorithms. IEEE Trans Neural Network 16(3):645–678

Chapter 15
Fault Tolerant Control of Large LED Systems

Jianfei Dong, W.D. van Driel, and G.Q. Zhang

Abstract This chapter describes a system-level design method of automatically diagnosing and compensating LED degradations in large LED systems, also known as solid-state lighting (SSL) systems. A failed LED may significantly reduce the overall illumination level, and destroy the uniform illumination distribution achieved by a nominal system. The main challenge in diagnosing LED degradations lies in the usually unsatisfactory observability in a large LED system, because the LED light output is usually not individually measured. In this chapter, we review a solution which we have recently developed in ref. (Dong et al. Optics Express 19:5772-5784, 2011). This solution tackles the observability problem by assigning pulse width modulated (PWM) drive currents with unique fundamental frequencies to all the individual LEDs. Signal processing methods are applied therein to estimate the individual illumination flux of each LED. Statistical tests are described to diagnose the degradation of LEDs. Duty cycle of the drive current signal to each LED is reoptimized once a fault is detected, in order to compensate the destruction of the uniform illumination pattern by the failed LED. The combined diagnosis and control reconfiguration is known as fault tolerant control (FTC) in control theory literature. In this chapter, we first review the essential technical details of the solution in ref. (Dong et al. Optics Express 19:5772-5784, 2011), and then focus on detailed simulation case studies, which clearly verify the effectiveness of this FTC solution for multiple LED degradations at the same time.

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15.1 Introduction

The recent popularity of solid-state lighting (SSL) systems can be attributed to the great benefits of using LEDs [1], namely high efficiency, controllable emission properties with much greater precision, and the consequent huge environmental benefits. According to the calculations in [1], with an 80 % market penetration of solid-state lighting technology, one half of the electrical energy currently used for lighting in the USA can be saved per year. However, since single LEDs cannot provide sufficient luminous flux alone, they are usually grouped together [2–4]. By distributing the illumination task to each LED in the system, the burden on each individual is significantly reduced. Consequently, the life of each LED can be increased [3]. There is hence an urgent need for system-level design of SSL systems [2] to cope with large LED systems.

Recent research on large LED systems mainly focuses on analyzing the illumination distribution of a group of LEDs [4–7]. An array of LEDs is usually required to achieve a uniform illumination pattern [4, 6, 8]. Obviously, if some LEDs in the array fail, the desirable illumination pattern will be destroyed. Due to the long life time of LEDs, LED failure seems to be a rare event. But, there is still a question to ask, i.e., what if an LED fails any way? This can be due to the gradual degradation of the LED chip, phosphor, and the electrical drive circuit. Besides, LED degradation can also be due to the excessive increase in its junction temperature [2], which could be unexpected. Although one may visually inspect a degraded LED in his/her home and replace it with a new one, it is not as straightforward for the LEDs in an office building or for street lighting. The disturbance to a meeting by the replacement of failed LEDs in the meeting room may be quite annoying. Pedestrians may find failed lamps in street. But it is not up to them to replace these lamps. They have to suffer from darkness, until the lighting system is repaired by the concerned authority. However, automatic diagnostic schemes are still rarely seen in the literature.

To fulfill the need, we have recently developed a scheme of automatically diagnosing LED degradations in [9], based on the general fault diagnosis theories [10, 11]. Briefly speaking, fault diagnosis is a residual generation and evaluation problem. If only a single LED is applied and there is a photosensor measuring its luminous flux, then diagnosing its degradation is relatively easy, since a residual can be readily computed as the difference between the measured and the theoretical luminous flux. However, as long as a group of LEDs are simultaneously implemented, the problem becomes much more complicated. There are usually not as many photosensors as LEDs, because otherwise the cost would be high, and the mounting would be difficult. If there is only one photosensor measuring the entire group of LEDs, then its measurement is a mixture of all the LED outputs. It is not easy to separate these signals. In [9], we tackled this observability problem by the illumination sensing method proposed in [12].

This chapter will start with describing the diagnostic method in [9].We will consider the case where there are less photosensors than LEDs in a SSL system. Separating the light signals is made possible by tagging the drive current signal to

each LED with a distinguishable "identity." In [12], the drive current signal to each LED is assigned with a unique fundamental frequency, which is known as frequency division multiplexing (FDM). As a consequence, it is natural to separate each LED contribution to the overall illumination at the photosensor by a bank of band-pass filters. Based on this "virtual sensing" approach, we will describe a statistical method to diagnose the degradations of LEDs in a SSL system. Once degradations of some LEDs are detected, an automatic reconfiguration of the drive current signals to the LEDs in the system is required to compensate the destroyed uniform illumination pattern. In this reconfiguration, the failed LEDs should be turned off; and the properly working LEDs should be given more duty to compensate the loss of the failed LEDs. To this end, we will review the optimization-based reconfiguration scheme proposed in [9]. We will finally provide more detailed simulation case studies, where we verify the effectiveness of the method to tolerate not only one LED failure, as already reported in [9], but also more LEDs degrading simultaneously.

15.2 LED Model and Illumination Rendering

Generally, fault diagnosis is a residual generation problem. Here, the term, "residual," refers to a fault indicator as the deviation between measurements and model equation based computations [13]. A mathematical model is hence needed to diagnose LED degradations. Such a model describes the relation between the input drive current to a LED and its produced illumination at a target point. A residual generator can hence be schematically illustrated in Fig. 15.1.

The residual generation problem will be further elaborated later in this chapter.

We shall first focus on introducing the LED models to be used in the residual generator.

15.2.1 Single LED Illuminance Model

Lambertian model is widely used in describing the illumination pattern of LEDs [4–6, 14]. The illuminance, i.e., the luminous flux per unit area, at a target point on a

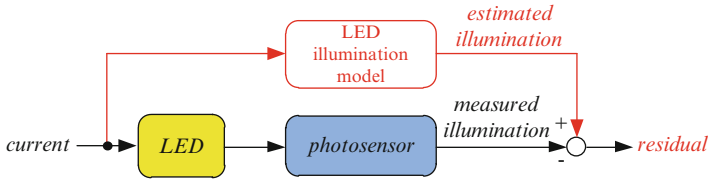


Fig. 15.1 Scheme of diagnosing a single LED

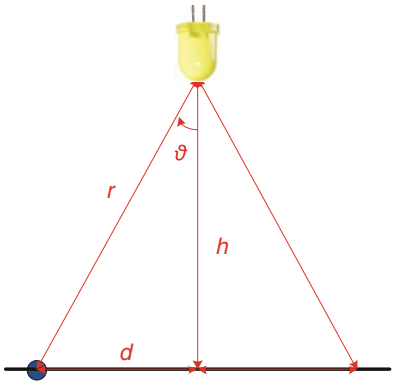


Fig. 15.2 Geometry between an LED and a target. *Circle*: target points

flat surface with a horizontal and vertical distance of respectively d and h from a single LED can be expressed by the following Lambertian model [14],

$$l(d,h) = \frac{(\mu+1)I_0}{2\pi h^2}\left(1+\frac{d^2}{h^2}\right)^{-\frac{\mu+3}{2}}$$

Here, $\ell(d,h)$ denotes the illuminance in the unit of lumen/m^2. ℓ_0 is the total luminous flux (in lumen) produced by the LED. μ (> 0) is the Lambertian mode number, dependent on the view angle at which the illuminance is half of the value at $q = 0$ [5, 14]. The geometry is illustrated in Fig. 15.2.

15.2.2 Rendering by an Array of LEDs

The overall illumination rendered by an array of LEDs, as shown in Fig. 15.3, is a superposition of all the individual Lambertian model outputs.

In order to separate the mixed illuminance at a target point, frequency division multiplexing scheme is applied to pulse width modulated (FDM-PWM) drive current signals in [12]. The FDM-PWM drive current pulses lead to light pulses as illustrated in Fig. 15.4, where f_i is the fundamental frequency of the drive current fed to the i-th LED; $0 < p_i < 1$ is the length of one duty cycle.

To avoid flicker and to ignore the transient response of the LEDs to the drive current, the fundamental frequencies should be chosen within the band 2 kHz $\leq f_i \leq$ 4 kHz,$\forall_i$ [12]. Hence, if p_i/f_i is chosen much greater than the on/off switching frequency of the LEDs, the light pulses generated by an array of L LEDs can be well approximated by a rectangular function; i.e.

$$I_{x,y,h}(t) = \sum_{i=1}^{L}\sum_{n=-\infty}^{\infty} a_{f,i}\cdot \mathrm{rect}\left(t-\frac{n}{f_i}\right) + e(t) \tag{15.1}$$

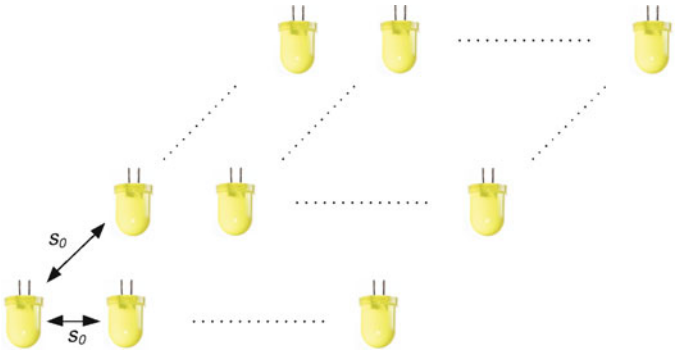


Fig. 15.3 A LED array on a flat surface with equal spacing s_0

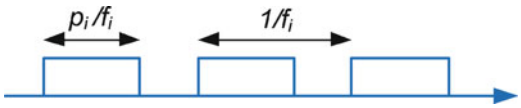


Fig. 15.4 FDM-PWM light pulses

Here, the rectangular window is defined as

$$\text{rect}(t) = \begin{cases} 1, & -1/2 \le t \le 1/2 \\ 0, & \text{otherwise} \end{cases}$$

Besides, $a_{f,i} = \alpha_i \cdot l_i(x, y, h)$ with α_i standing for the gain from the i-th LED to the illumination measured by the photosensor. $l_i(x, y, h)$ is the Lambertian model output of the i-th LED at the position of the photosensor, with (x, y) the coordinates on the target surface, i.e., $d = \sqrt{(x^2 + y^2)}$. The last term $e(t)$ consists of thermal and shot noise in the photosensor circuit, which is usually considered as zero mean white Gaussian in literature [12]. Here, we also assume that there is no ambient light, except the LEDs in the SSL system.

15.3 Illumination Sensing for Measuring Individual LED Outputs

As defined by (15.1), the illumination measured at a target point is a mixture of light pulses with distinguishable frequencies. The task of illumination sensing is therefore to estimate a_i for each individual LED. At each fundamental frequency f_i, a_i can be estimated by

$$\hat{a}_i = \frac{\pi}{\sin(\pi p_i)} \left| \int_0^T I_{x,y,h}(t-\tau) \cdot g(\tau) \cdot e^{-j2\pi f_i \tau} \cdot d\tau \right| \tag{15.2}$$

Here, $g(t)$ represents the impulse response parameters of a filter defined on the support [0,T]. In [12], to achieve unbiased illumination sensing, $g(t)$ is taken as

$$g(t) = \frac{1}{T} \text{rect}\left(\frac{t}{T} - \frac{1}{2}\right)$$

where $T \geq 1$, with $\Delta_f = \frac{f_{\text{upper}} - f_{\text{lower}}}{L}$, where f_{upper}, f_{lower} respectively the upper and lower frequency limit. Note that the estimate, $\hat{a}_i$, is a function of time in this expression, because it is the output from a dynamic filter. Furthermore, due to the measurement noise $e(t)$, the estimation error is upper bounded as [12]

$$\left| a_{f,i}(t) - \hat{a}_{f,i}(t) \right| \leq |v_i(t)| \tag{15.3}$$

where $v_i(t)$ has a variance of (P_e/T), with P_e the double-sided power spectrum density of $e(t)$.

15.4 Diagnosis of LED Degradations

The diagnostic method proposed in [9] is reviewed in this section. We consider the degradation of an LED as the reduction in its efficiency from drive current to its light output. We shall treat the estimated illumination via the method introduced in the previous section as measured signals, and compare them with its theoretical counterparts. The light output from a LED is known to be proportional to the drive current flowing through it at steady state [15, 16]. Besides, the dynamic response of light output to drive current has a first-order behavior with the on-/off-switching time constant of the LED, usually smaller than 1 microsecond. The transient response can hence be neglected. The following equalities hold.

$$l_{0,i} = \eta_i \cdot c_i$$

$$a_i(t) = \eta_i \cdot \alpha_i \cdot c_i(t) \cdot \frac{\mu_i + 1}{2\pi h^2} \cdot \left(1 + \frac{{d_i}^2}{h^2}\right)^{-\frac{\mu_i + 3}{2}} \tag{15.4}$$

Here, c_i is the amplitude of drive current pulses flowing through the i-th LED. η_i is the responsivity coefficient. In addition to the theoretical relation $\ell_{0,i} = \eta_i \cdot c_i$, $\ell_{0,i}$ can also be found by interpolating the current versus luminous flux chart provided on the data sheet of an LED, e.g. [17]. In this case, $\eta_i \cdot c_i$ in (15.4) can be replaced by the interpolated values according to the data sheet. Besides, we shall treat the

nominal values of α_i, η_i, μ_i as known parameters. The theoretical value of $a_i(t)$ can hence be calculated.

The residual can now be written as

$$r(t) = a_i(t) - \hat{a}_i(t)$$

where $\hat{a}_i(t)$ is from the "virtual sensor," i.e., (15.2). The components of $r_i(t)$ include a random noise (denoted by w_i), whose distribution is determined by (15.3), and in the faulty case, a fault signal (denoted by φ_i); i.e.

$$r(t) = \varphi_i(t) + w_i(t)$$

For fault diagnosis, φ_i needs not be to known or modeled. We can now analyze the statistical characteristics of $r_i(t)$ due to the noise term w_i, and develop a fault diagnosis test. In fact, due to (15.3),

$$\frac{[a_i(t) - \hat{a}_i(t)]^2}{P_e/T} \leq \frac{[v_i(t)]^2}{P_e/T}$$

Since $v_i(t)$ is zero mean Gaussian with variance P_e/T, the random variable $(v_i^2(t))/(P_e/\mathrm{T})$ is χ^2 distributed with a DoF of 1 [11], denoted as ${\chi_1}^2$. In other words, the random variable $\zeta_i(t) = ([a_i(t) - \hat{a}_i(t)]^2)/(P_e/T)$ is upper bounded by the ${\chi_1}^2$ distributed variable $\nu_i(t) = (v_i^2(t))/(P_e/T)$. This then leads to a fault diagnosis test in terms of the worst case estimation error; i.e.

$$\zeta_i(t) = \frac{[a_i(t) - \hat{a}_i(t)]^2}{P_e/T} \begin{matrix} \overset{\text{faulty}}{>} \\ < \\ \text{no-fault} \end{matrix} \gamma_\beta \tag{15.5}$$

where γ_β denotes the threshold, determined by a chosen false alarm rate β. Technically, the number and positions of the photosensors shall be determined by the signal-to-noise ratio (SNR) of the luminous flux of the i-th LED $a_i(t)$ to the estimation error $v_i(t)$, as defined in (15.3), i.e., $\mathrm{SNR}_i = \dfrac{{a_i}^2(t)}{P_e/T}$ On the other hand, $a_i(t) = \alpha_i \cdot \ell_i(x,y,h)$ is determined by the solid angle θ , see Fig. 15.2, between the i-th LED and the photosensor and the Lambertian mode number of the LED, i.e., μ_i. For a narrow Lambertian-type LED, μ_i is big, leading to fast decaying luminous flux as the solid angle θ increases. In this case, a photosensor should be placed at small solid angles relative to the LEDs, which is thus limited to monitor the LEDs only in its close neighborhood. Conversely, when μ_i is small, one photosensor is able to effectively monitor more LEDs further away from its neighborhood. The SNR determines the sensitivity of the diagnostic method. In the "worst-case," the sensitivity, or the SNR, should guarantee that the diagnostic algorithm is able to detect the complete failure of a LED. In [9], we have analyzed that this "worst-case" sensitivity can be mathematically expressed as

$$\mathrm{SNR}_i = \frac{{a_i}^2(t)}{P_e/T} > \gamma_\beta \tag{15.6}$$

Since a_i depends on the relative position between the i-th LED and the photosensor, condition (15.6) shall be checked, when determining the positions of the photosensors to ensure that at least the complete failure of all LEDs can be detected.

15.5 Control Reconfiguration Against LED Degradations

The desired performance of a large LED system is the uniformly distributed illumination on a target surface with a certain intensity. If this performance is achieved by the nominal system, then a degraded LED will destroy this uniformity, and especially reduce the illumination around it. Therefore, it is necessary to compensate this degradation by the other nominal LEDs in the system. This can be done by automatically tuning the (average) amplitudes of the drive current fed into these nominal LEDs, once the degradation of an LED is detected. To this end, we describe the optimization-based control reconfiguration scheme of [9] in this section. Due to the rectangular LED light pulses in response to the PWM drive current signals, the average flux of the i-th LED in one period is the total luminous flux produced by the peak current c_i scaled by the on/off switching ratio (i.e., the duty cycle), p_i. At a point (x,y,h) on the target surface, the average illuminance can be written as

$$I_{x,y,h} = \sum_{i=1}^{L} p_i \cdot \eta_i \cdot c_i \cdot \alpha'_i \cdot \frac{\mu_i + 1}{2\pi h^2} \cdot \left(1 + \frac{{d_i}^2}{h^2}\right)^{-\frac{\mu_i + 3}{2}} \tag{15.7}$$

Here, α_i' is the path loss of the free-space optical channel from the i-th LED to the target. Here, $I_{x,y,h}$ quantities the illumination distribution at a target point. Suppose that the i-th LED has degraded. To still maintain a uniform illumination distribution, we intend to compensate the degraded LED with the remaining properly working LEDs. The degraded one will be switched off. We can hence set the duty cycle p_i to zero in (15.7) corresponding to the degraded LED, to turn it off. In [9], we have proposed the following cost function to be optimized.

$$J = \sum_{(x,y)\in \mathbf{TS}} w_{(x,y)} \cdot \left(I_{x,y,h} - R_{x,y,h}\right)^2 + \sum_{i \in \mathbf{I}_{\mathrm{all}} \backslash \mathbf{I}_{\mathrm{fail}}} w_{p_i} \cdot {p_i}^2 \tag{15.8}$$

Here, "**TS**" denotes the target surface. $w(x,y) \geq 0$, $(x,y) \in$ **TS** and $wp_i \geq 0$, $i \in I_{\mathrm{all}} \backslash I_{\mathrm{fail}}$ are weighting coefficients respectively penalizing the tracking errors and duty cycles. The set $I_{\mathrm{all}} = \{1,\ldots,L\}$ collects all the LED indices in the SSL system; while

I_{fail} only contains the indices of the failed LEDs. The set, $I_{\text{all}} \backslash I_{\text{fail}}$, hence refers to all the remaining properly working LEDs in the system. By its definition, the duty cycle p_i has to be limited between 0 and 1. More precisely, in an FDM scheme [12, 18], p_i is required to be within the range, $0.001 \leq p_i \leq 0.97307$. The upper bound is to distinguish the current signals from DC. The cost (15.8), together with these bounds, leads to the following constrained optimization problem.

$$\begin{aligned} &\min_{\{p_i | i \in \mathbf{I}_{\text{all}} \backslash \mathbf{I}_{\text{fail}}\}} J(p_1, \cdots, p_L) \\ s.t. \quad &0.001 \leq p_i \leq 0.97307, i \in \mathbf{I}_{\text{all}} \backslash \mathbf{I}_{\text{fail}} \end{aligned} \tag{15.9}$$

Note that since p_i is linear in $I_{x,y,h}$, J is quadratic and convex. Therefore, (15.9) is a convex optimization problem with global minimum [19].

15.6 Application Case Study

15.6.1 Problem Settings

Consider a 9 × 9 LED array on a 2 m × 2 m flat surface, as shown in Fig. 15.3. Consider the following numerical values: $\mu_i = 50$, $s_0 = 0.25\ m$ and $\ell_{0,i} = 100$ lumens at $c_i = 350$ mA, i.e., $\eta_i = 285.7$ lumen/A, $i = 1,\ldots,81$. This can be realized by a LUXEON Rebel LXM7-PW40 LED [17]. The optical channel gains are set as $\alpha = 1$, $\alpha' = 1$. P_e is chosen as 0.01.

Suppose there is only one photosensor on the target surface, two meters below the LED array. Its position on the surface is (0,0), i.e., the origin fixed at the central LED of the array. We shall use this sensor to estimate a_i, $i = 1,\ldots, 81$. The contribution of each individual LED to the photosensor is illustrated in Fig. 15.5, where the gray levels are calculated as $0.97\ (1 - a_i/a_{\max}\ [1\ 1\ 1])$, $i = 1,\ldots,81$, with $a_{\max} = \max\{a_i | i = 1,\ldots,81\}$. The vector, [1 1 1], represents normalized RGB values. The more visible (the darker) the circles are seen by the readers, the more visible the LEDs are to the photosensor. On the other hand, Fig. 15.6 indicates that all the LEDs contribute to an SNR greater than 17 dB, sufficient for diagnosing degradations. We shall hence only use this photosensor in this chapter.

The frequency spacing of the FDM-PWM drive current signals is therefore $\Delta_f = (f_{\text{upper}} - f_{\text{lower}})/L = 24.7$ Hz. The rectangular filter window is hence chosen to be $T = 0.0405$ s. The initial duty cycles to all the LEDs in the array are chosen as, $p_i = 0.4, \forall i$. The sampling period is set to 10^{-6} s. The illumination signal measured by the photosensor in a time interval of 0.15 s is shown in Fig. 15.7, whose power spectral density is depicted in Fig. 15.8. Obviously, besides the DC component, the signal power is dominating within the frequency band, [10, 15]kHz. On the other hand, the target surface is discretized with a spacing of 0.01 m into a 201 × 201 grid.

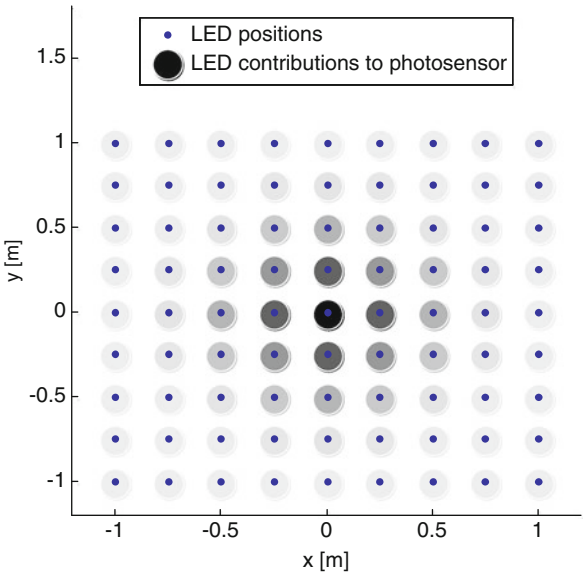


Fig. 15.5 Contributions of the LEDs to the photosensor

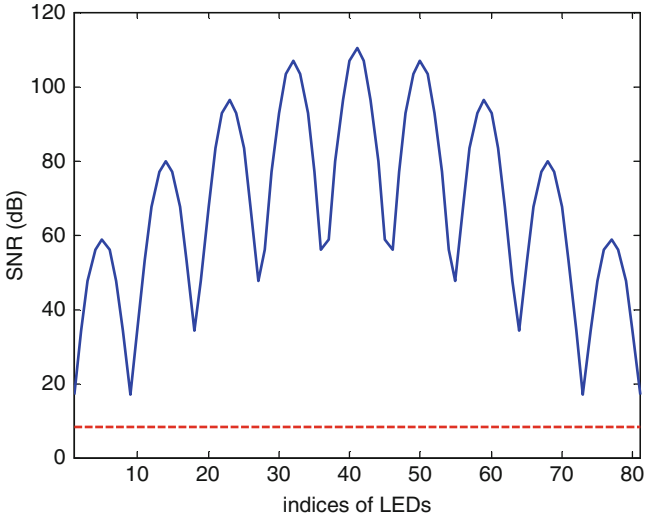


Fig. 15.6 SNRs (*solid*) of the photosensor measurement of each LED, as compared with the detection threshold (*dashed*)

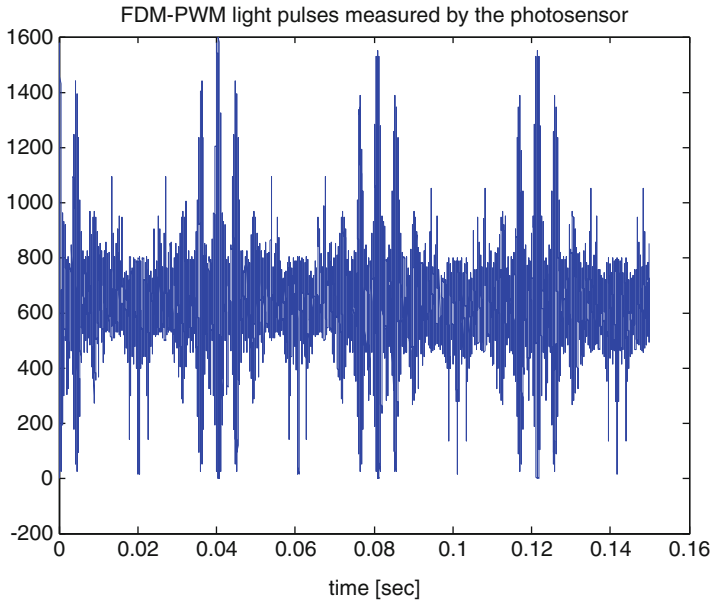


Fig. 15.7 Illumination signal measured by the photosensor

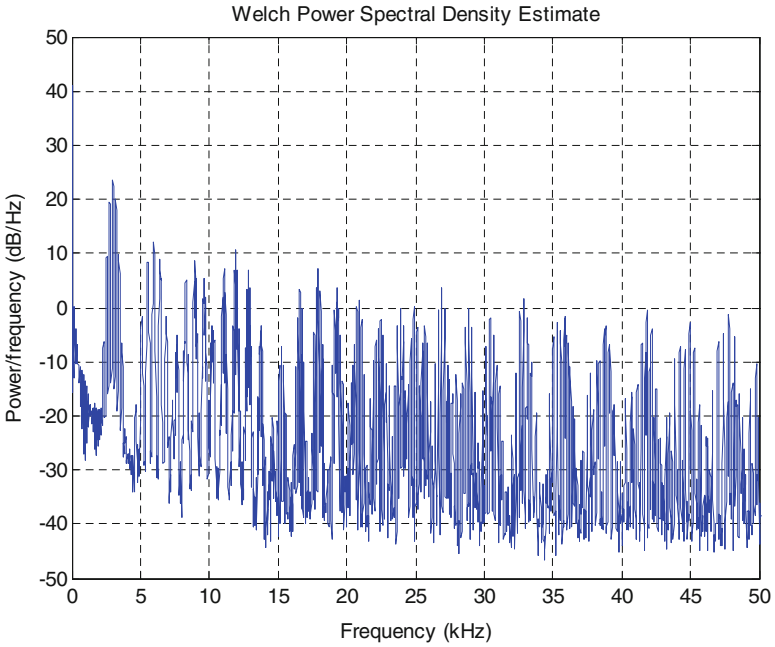


Fig. 15.8 Power spectral density of the signal measured by the photosensor

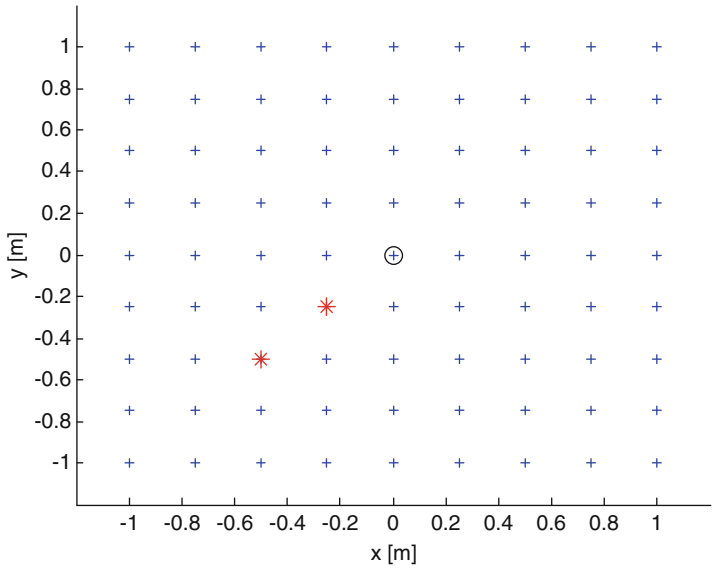


Fig. 15.9 Positions of the failed LEDs in the case study. Pluses: nominal LEDs. Stars: failed LEDs. Circle: photosensor

15.6.2 FTC of Two LED Degradations

Suppose the LEDs have been running for 10^5 h. Consider the two LEDs as shown in Fig. 15.9 failed, with half of their efficiency lost. These degradations are injected into the two LEDs at 0.075 s after 10^5 h. The other LEDs are not changed. With this degradation, the overall illumination pattern is shown in Fig. 15.10. It can be seen that the area adjacent to the projected point of the degraded LED becomes darker. The uniformity of the illuminated surface is destroyed. To automatically diagnose these degradations, we implement the diagnostic scheme described in this chapter. The false alarm rate is chosen as $\beta = 1$ %. The threshold is therefore $\gamma_\beta = 6.6349$, corresponding to an SNR of 8.2 dB. See Fig. 15.6. The total simulation time is 0.15 s.

The test statistics $\zeta_i(t)$ are plotted in Fig. 15.11. The vertical lines in the figure divide the time axis into four intervals, i.e., $I_1 = [0,0.0405]$, $I_2 = [0.0405,0.075]$, $I_3 = [0.075,0.1155]$, $I_4 = [0.1155,0.15]$. This is because the filter window length is $T = 0.0405$ s. In I_1, the filter waits for sufficiently long signal segment to process. There is hence no test statistics can be computed. In I_2, all the LEDs work properly. So the statistics are restrained below the threshold. The two LEDs degrade at 0.075 s. In I_3, all the estimated $\hat{a_i}$ are biased, due to the transient phase of the estimation filter. To see this, note that the filter $g(t)$ is in fact a moving average of the light signals measured during the past 0.0405 s. In I_4, when the filter window is entirely filled with degradation-affected light signals, the estimated a_i, become unbiased again, which result in the statistics below the threshold, only except the two corresponding to the degraded LEDs. Correct alarms are therefore produced by the diagnosis. The detection delay is hence $T = 0.0405$ s.

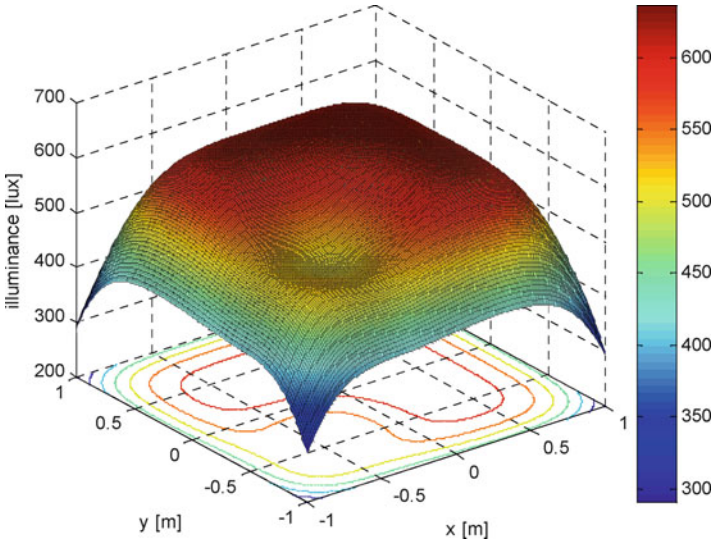


Fig. 15.10 Illumination distribution (lumen/m^2) of the LED array with two degraded LEDs, whose locations are shown in Fig. 15.9

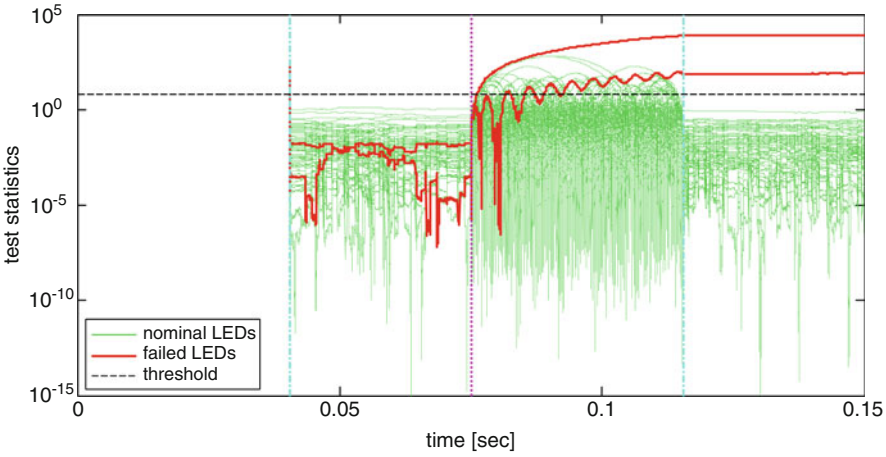


Fig. 15.11 Test statistics for diagnosing LED degradations. *Dotted purple* (*darker*): time instant of the fault onset. *Dash-dotted cyan* (*lighter*): 0.0405 s intervals respectively from the start and from the fault onset

For the optimization-based reconfiguration, we choose the reference $R_{x,y,h}$ to be the same as the original illuminance produced when all the LEDs working properly with $p_i = 0.4$ and $c_i = 350$ mA. The weights are set to $w_{(x,y)} = 10, \forall (x,y) \in \mathbf{TS}$, and $w_p = 1$ for the nominal LEDs. The reconfigured illumination distribution is shown in Fig. 15.12. The variance of the illuminance (in (lumen/m^2)^2) in the range

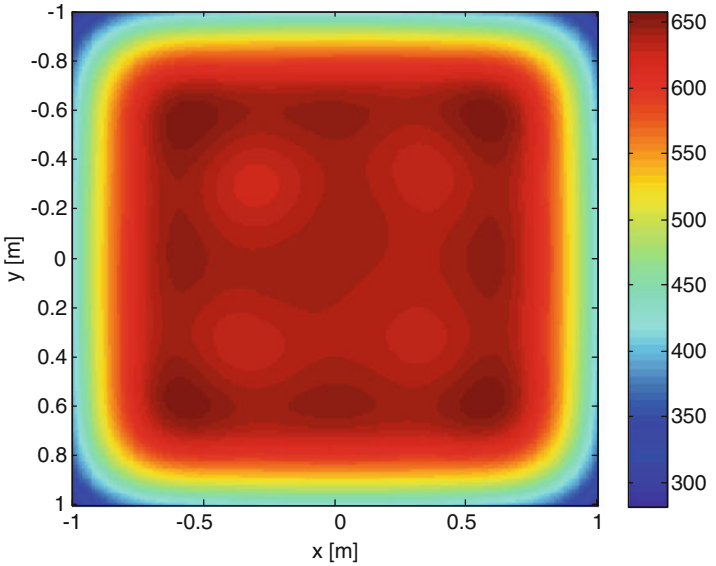


Fig. 15.12 Reconfigured illumination distribution (lumen/m^2) of the LED array with two degraded LEDs

of a 1.6 m $\times$ 1.6 m square on the target surface centered at the origin, defined as (with N_{dp} denoting the number of discretized points on this square surface)

$$\frac{1}{N_{dp}} \sum_{-1 \le x,y \prec 1} \left(I_{x,y,h} - \bar{I}\right)^2, \text{ where } \bar{\mathrm{I}} = \frac{1}{\mathrm{N_{dp}}} \sum_{-1 \le \mathrm{x,y} \prec 1} \mathrm{I_{x,y,h}}$$

is changed from 1,556.6 in the degraded case to 258.6 in the reconfigured case, i.e., 16.6 % of the uncompensated value. Clearly, the degraded pattern is efficiently compensated.

15.6.3 Control Reconfiguration Against Even More LED Degradations

A relevant question to answer now is whether the degradation of more than two LEDs can also be tolerated by the optimization scheme (15.9). We verify this by more simulations. To this end, we randomly choose eight LEDs in the array, as illustrated in Fig. 15.13. The destroyed illumination pattern is shown in Fig. 15.14.

The reconfigured illumination distribution is shown in Fig. 15.15. The variance of the illuminance in the range of a 1.6 m $\times$ 1.6 m square on the target surface centered at the origin, is changed from 1,638 in the degraded case to 333 in the reconfigured case, i.e., 20 % of the uncompensated value. Clearly, the degraded pattern is efficiently compensated.

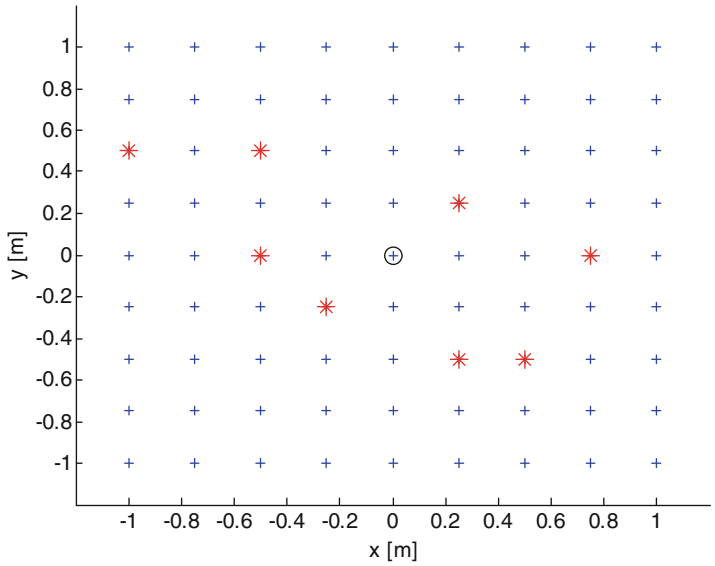


Fig. 15.13 Positions of eight failed LEDs. Pluses: nominal LEDs. Stars: failed LEDs. Circle: photosensor

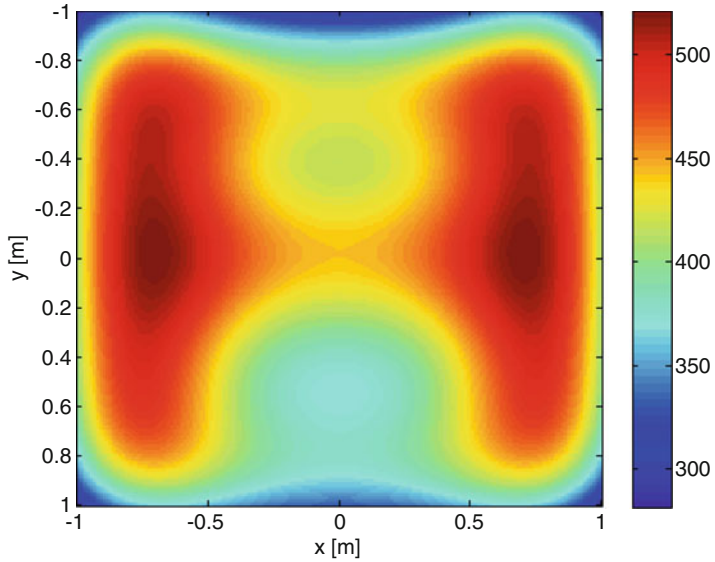


Fig. 15.14 Illumination distribution (lumen/m^2) of the LED array with eight degraded LEDs, whose locations are shown in Fig. 15.13

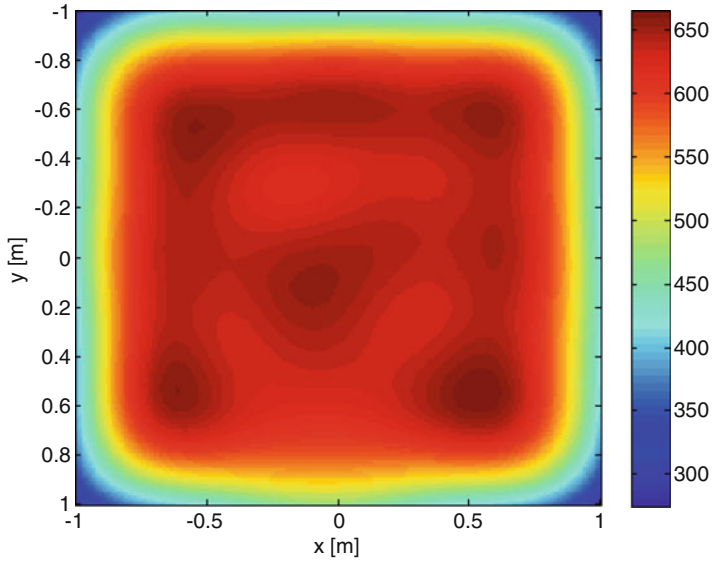


Fig. 15.15 Reconfigured illumination distribution (lumen/m^2) of the LED array with eight degraded LEDs, whose locations are shown in Fig. 15.13

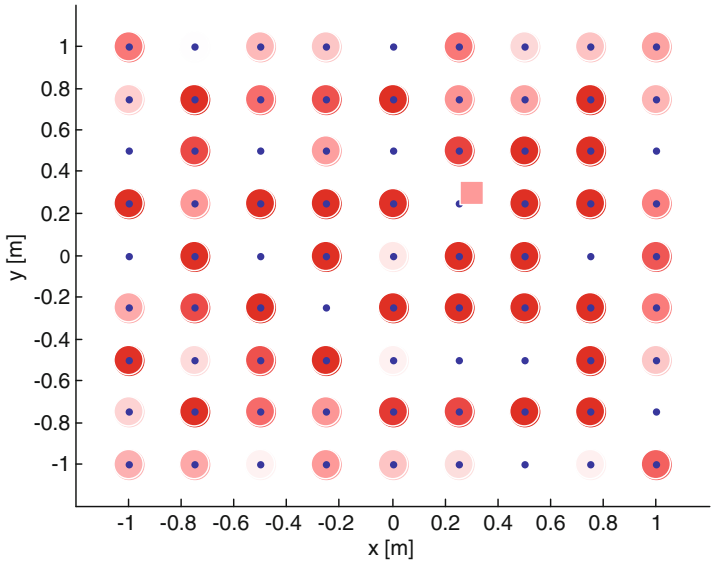


Fig. 15.16 Reconfigured duty cycles of LED currents. *Dots*: positions of the LEDs projected onto the target surface. *Red square*: magnitude of the original duty cycle, $p_i = 0.4, \forall_i$. *Circles* with different levels of red: magnitudes of duty cycles. The darker the circles than the square, the longer their duty cycles than 0.4; and vice versa. The color is calculated as $1 - p_i \cdot [0\ 1\ 1], \forall_i$

It is also interesting to illustrate the reconfigured duty cycles of the nominal LEDs, as in Fig. 15.16. Obviously, the adjacent LEDs to the degraded ones are assigned with longer duty cycles. However, doing so will also increase the illuminance adjacent to them. Consequently, the optimization in turn dims the light of their nearest neighbors, in such a way that the uniformity is maintained as much as possible, as shown in Fig. 15.15. Moreover, all the reconfigured duty cycles are kept below 0.97307.

15.7 Conclusions

In this chapter, we have described a system-level design approach for automatically diagnosing and reconfiguring large LED systems. The diagnosis of the LED condition in the system is made possible by assigning distinguishable fundamental frequencies to the FDM-PWM drive current signals to all the individual LEDs. The fault diagnosis approach and the optimization-based control reconfiguration method, developed in our previous work [9], are briefly reviewed. The complete technical details shall be referred to [9]. This chapter instead focuses on verifying these methods in a 9×9 LED array, where two or even more LEDs may fail at the same time. The simulation case studies are carried out in MatLab, which clearly verifies the effectiveness of the proposed diagnosis and control reconfiguration scheme in handling simultaneous multiple LED degradations.

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References

1. Schubert EF, Kim JK, Luo H, Xi JQ (2006) Solid-state lighting a benevolent technology. Rep Progr Phys 69:3069–3099
2. Ashdown I (2006) Solid-state lighting design requires a system-level approach. SPIE Newsroom. http://newsroom.spie.org/x2235.xml?highlight=x531
3. Narendran N, Maliyagoda N, Bierman A, Pysar RM, Overington M. Characterizing white LEDs for general illumination applications. Proc SPIE, 2000
4. Tsuei CH, Pen JW, Sun WS (2008) Simulating the illuminance and the efficiency of the LED and fluorescent lights used in indoor lighting design. Optics Express 16:18692–18701
5. Moreno I, Contreras U (2007) Color distribution from multicolor LED arrays. Optics Express 15:3607–3618
6. Qin Z, Wang K, Chen F, Luo X, Liu S (2010) Analysis of condition for uniform lighting generated by array of light emitting diodes with large view angle. Optics Express 18:17460–17476
7. Sun CC, Chien WT, Moreno I, Hsieh CC, Lo YC (2009) Analysis of the far-field region of LEDs. Optics Express 17:313918–13927

8. Ding Y, Liu X, Zheng ZR, Gu PF (2008) Freeform LED lens for uniform illumination. Optics Express 16:12958–12966
9. Dong J, van Driel WD, Zhang GQ (2011) Automatic diagnosis and control of distributed solid state lighting systems. Optics Express 19:5772–5784
10. Blanke M, Kinnaert M, Lunze J, Staroswiecki M (2003) Diagnosis and fault-tolerant control. Springer, Heidelberg
11. Gustafsson F (2001) Adaptive filtering and change detection. John Wiley & Sons, Ltd, West Sussex, England
12. Yang H, Bergmans JWM, Schenk T (2009) Illumination sensing in LED lighting systems based on frequency-division multiplexing. IEEE Trans Signal Process 57:4269–4281
13. Isermann R, Ballé R (1997) Trends in the application of model-based fault detection and diagnosis of technical processes. Control Eng Pract 5:709–719
14. Yang H, Bergmans JWM, Schenk T, Linnartz JPMG, Rietman R (2008) An analytical model for the illuminance distribution of a power LED. Optics Express 16:21641–21646
15. Descombes A, Guggenbuhl W (1981) Large signal circuit model for LED's used in optical communication. IEEE Trans Electron Dev 28:395–404
16. Wood D (1994) Optoelectronic semiconductor devices. Prentice Hall
17. Philips Lumileds. LUXEON rebel illumination portfolio—technical datasheet DS63. http://www.philipslumileds.com/pdfs/DS63.pdf
18. IEC 62386. Digital addressable lighting interface. 2007
19. Boyd S, Vandenberghe L (2004) Convex optimization. Cambridge University Press, Cambridge, United Kingdom

Chapter 16
LED Retrofit Lamps Reliability

Xiu Peng Li and Chen Mei

Abstract LED retrofit lamps are claimed as long lifetime, high efficiency, and low power. The failure mechanisms are different from conventional lamps. How to apply the reliability requirement of conventional lamps into LED retrofit lamp becomes important and essential. With reviewing the reliability of conventional lamps and the failure mechanism of LED retrofit lamp, the paper proposes a methodology of reliability definition, analysis, and evaluation.

16.1 Introduction

Solid State Lighting (SSL) is slowly but gradually pervading into our daily life. At present, light-emitting diode (LED) lighting systems in various shapes are developed and designed for general lighting, advertisement, emergency lighting, and architectural markets. LED based illumination systems have preceded the conventional incandescent light sources in efficiency and reliability and have achieved good color rendering. Although lack of significant penetration into the general lighting market is mainly due to the costs, looking at recent increases in efficiency (approx. 75%), reliability (approx. 50,000 h), and power density (approx. 100 lm/W) thereby offering higher lumens per Euro, they are now at the doorstep of massive market entry into offices and homes, Especially the retrofit lamp keeps the same mechanical outline as incandescent lamp so that it could replace the incandescent lamp and install in the existing luminaries.

It can be concluded that an increasing amount of manufacturing companies are moving into this fast growing market of LED retrofit lamps, resulting in a very

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competitive environment. In order to emphasize the strength of LED retrofit lamps, some manufacturers claim 50,000 h or even 100,000 h lifetime without any approved test data, nor do they specify the use conditions. Some manufacturers are using the lifetime information from the LED supplier as the whole lamp lifetime without considering the lifetime of the total system. Therefore, the high failure return rates from field may be caused by the electronic component failure, the color shift, plastic degradation, and many more possible failure modes. In this chapter we review the reliability approaches for conventional lamps and the failure mechanisms of LED retrofit lamp. The chapter proposes a methodology for a reliability definition, analysis, and evaluation for LED retrofit lamps.

16.2 LED Retrofit Lamps

LED has been used in diverse lighting applications with replacing the conventional lighting because of efficient, energy saving, and long lifetime. This also dramatically changes 100-years-old lighting industry. LED lamp follows the same outline specified in IEC 60630 maximum lamp outlines for incandescent lamp and can be easily installed in current luminaries, which is called as LED Retrofit lamp. Retrofit lamp is best candidate to replace incandescent lamps.

Energy star lists lumen requirement of LED retrofit lamp in corresponding to incandescent lamp as Table 16.1. The efficiency of LED retrofit lamps is around 50 lm/W which is rather higher than that of the conventional incandescent lamp (20 lm/W per Table 16.1).

LED retrofit lamps are facing lots of design issues, such as thermal design for heat dissipation from LED and electronic driver, and driver layout with small space, which eventually impact the lamp reliability

To design a reliable LED retrofit lamps, it is necessary to understand how the reliability requirement of incandescent lamps is defined, e.g., failure criteria, user conditions or user profile.

Table 16.1 Lumen output of conventional lamp from Energy Star

Nominal wattage of lamp to be replaced (W)	Minimum initial light output of LED lamp (lm)	Efficiency (lm/W)
25	200	8
35	325	9.3
40	450	11.3
60	800	13.3
75	1,100	14.7
100	1,600	16
125	2,000	16

16.3 Reliability of Incandescent Lamp

Incandescent lamps have more than 100 year's history. The first successful incandescent lamp was invented by Thomas Alva Edison in 1897 by using a carbon filament in a bulb containing a vacuum. The incandescent lamp generates visible light by heating a metal filament wire with electric current to a high temperature. Since that time, the incandescent lamp has been improved by using tungsten filaments and changing the vacuum inside to inert gas filled which could slow down the evaporation process of filament.

Anyhow, the evaporation of metal filament is not really eliminated and it still burns on after accumulated long enough operating hours and switches; normally it takes less than 2,000 h, equal to 16 weeks. It is possible for the lamp manufacturing to take some representative lamps to burn till it fail and verify the life the lamps.

A standard for incandescent lamp lifetime measurement named LM-49-01 [1] measuring and reporting rate lamp life is published by the IES. It sets up testing conditions, sample sizes, and methodologies for generalizing test data to arrive at rated life specifications. LM-49-01 specifies a statistically valid sample to be tested within the manufacturer's stated operating temperature range and voltage. Lamps are allowed to cool down to ambient temperature once a day (usually for 15–30 min). The point at which half the lamps fail is the rated average life to the lamp. For example, 22 lamps randomly selected from a batch of new design incandescent lamp were tested in rated temperature and voltage, the half of lamps failed till 1,500 h. Therefore, the rated life of this batch of lamp is 1,500 h.

For other conventional lamps, a series of standards is also published by the IES, for example, LM-40-01 defines life testing procedures for fluorescent lamps (FLs), LM-65-01 [2] for compact fluorescent lamps (CFLs). LM-65-01 specifies samples to be tested in a cycle of 3 h on /20 min off (as CFL life is appreciably shortened by the frequency with which the lamp is started). For incandescent lamp, the rated life for CFLs is the point where half the lamps fail.

The failure mechanism of incandescent lamp in the lifetime is quite simple, i.e., the burn out of the filament. The lifetime of incandescent lamp could be extended with slowing down the process of evaporation. For example, filling the bulb with an inert gas such as argon or an argon–nitrogen mixture, the lifetime of the lamp could be increased 20% or more. The lifetime of incandescent lamp is described as (16.1):

$$\frac{\text{Life}_{\text{rated\_voltage}}}{\text{Life}_{\text{Acc\_Voltage}}} = \left(\frac{V_{\text{Acc}}}{V_{\text{rated}}}\right)^{n} \tag{16.1}$$

where

- n is around 13–16,
- V_{Acc} is the accelerate voltage
- V_{rated} is the rated voltage,

This means that a 5% increase in input voltage will reduce half of the life of the bulb. So that it is possible to shorter the period of lifetime evaluation in the product development and process qualification by increasing test voltage. In the previous example, the life test could be shortened to 1,000 h if the input voltage is 105% of rated voltage. In another words, the lifetime measurement of incandescent lamps is simple, fast, and efficient.

16.4 Reliability of LED Retrofit Lamp

As is the same for incandescent lamp and other conventional lamp, lifetime is used to describe the reliability level of a LED retrofit lamp. For the conventional incandescent lamp, the lifetime is defined as the time when 50% of the lamps fail due to any causes, called as [B50, L70], is only thousand hours and could be easily to measured and tested. In order to evaluate the lifetime of a new developed incandescent lamp, a certain number of new developed lamp were tested in the life test rack and the time to failure for each lamp was recorded. The failure mechanism of incandescent lamp was burn out because of evaporated filament, which was easily to be identified and recorded. Then, the time when half of the total test lamps failed was defined as the lifetime (as shown in Fig. 16.1).

In order to compare with conventional lamps, the lifetime of LED Retrofit lamps also use B50L70 to represent its reliability level, which is defined as its ability to perform required functions under stated conditions for a specified period of time, with:

- *Required functions*: lamps are majors in the lumen output and color maintenance, in which the required lumen output values should not be lower than 70% of initial lumen, defined as L70, and the color should be maintained within 7SDCM in its

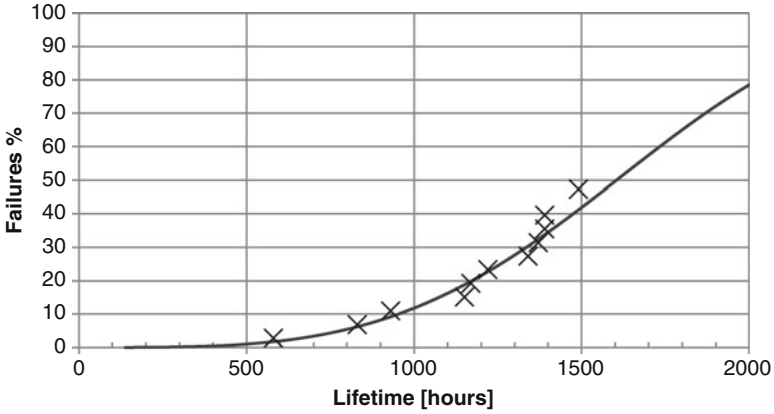


Fig. 16.1 A typical lifetime curve on an incandescent lamp

useful life. The number of 70% is set as the lower limit of lumen maintenance because below this value the initial lighting system design is judged to be too compromised for the user.

- *Stated conditions*: lamp is widely used in different environments, e.g., high temperature and high humidity in tropical countries, but cold and dry in north of European countries and the United States, also the temperature and humidity varies over year. On the other hand, lamp is normally installed in the luminaries, either open luminaries or closed luminaries, which also caused the lamp operating in higher temperature than in a fully open free air environment. The investigation of the user conditions shows that the lamp are normally used in an open luminaries (10 mm space between lamp outline to the inner of luminaries), and the average temperature is 25°C. Therefore, the lifetime of LED lamp is claimed under 25°C open luminaries.
- *Specified period of time*: the investigation tells that the average operating hours per year is around 1,000 h for consumer lamp and 3,000 for profession lamp.
- *Ability*: Possibility is used to describe the ability of lamp survive over time, and B50 is general used to indicate that 50% lamp still meet the required functions till the end of lifetime.

16.5 LED Retrofit Lamp Reliability Analysis and Modeling

To address the reliability of a LED lamp, it is necessary to understand its structure and failure mechanism to be able to set up a reliability model for it. LED lamps include the following four subsystems:

1. LED as light source
2. Electronic driver which provides power to LED lighting source
3. Mechanical housing used for thermal dissipation, electronic isolation, and final installation
4. Optical lens or bulb, fulfill the optic requirements, e.g., color over angle, beam angle.

The reliability of the whole LED Lamp could be illustrated in shown in Fig. 16.2. The reliability of whole LED Lamp can be described as follows:

$$R_{\text{LED-system}} = R_{\text{LED}} \times R_{\text{Driver}} \times R_{\text{Optical}} \times R_{\text{Mechanical}} \tag{16.2}$$

Each subsystem has multi failure mechanisms, in which each failure mechanism has its own failure distribution. A single subsystem's reliability can be described as follows:

$$\begin{aligned} R_{\text{subsystem}-1} &= R_{\text{failure}-\text{mode}-1} \times R_{\text{failure}-\text{mode}-2} \times R_{\text{failure}-\text{mode...}} \\ &= \sum_{i=1}^{n} R_{\text{failur}-\text{mode}-i} (i = 1 \ldots n) \end{aligned} \tag{16.3}$$

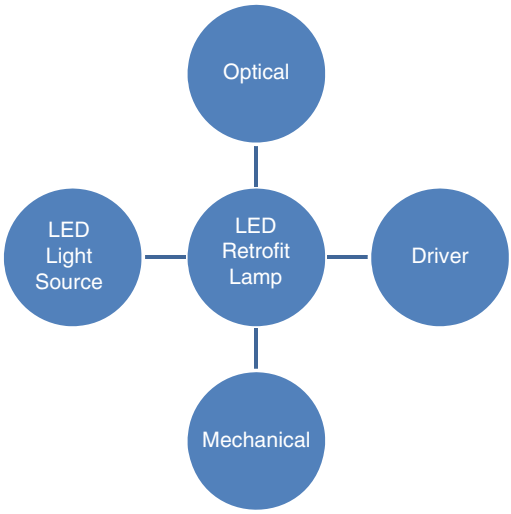


Fig. 16.2 LED lamp system reliability diagram

For example, a failure of LED Lamp could be resulted from 30% lumen decay caused by LED die and package material or the catastrophic failure caused by the LED die crack, and breakdown. The reliability of the LED light source is modeled per equation (16.4) as below:

$$R_{\mathrm{LED}} = R_{\mathrm{lumen\_decay}} \times R_{\mathrm{catastrophic\_failure}} \tag{16.4}$$

Therefore, in order to evaluate the system reliability, it is necessary to understand both the reliability of each subsystem in the lifetime and the failure mechanisms of each subsystem.

In September 2008, the IES issued Measuring Lumen Maintenance (MLM) of LED Light source and IES LM-80-08 [3]. IEC also issued a PAS version of 62612 [4] which majorly focus on the lumen maintenance of LED lamp and reliability tests in these standards as below:

Table 16.2 showed that instead of measuring lamp lifetime, the current standards call for how much a LED light source or lamp's lumen output decay over lifetime with expecting extremely low catastrophic failure in the whole lifetime. The 6,000 h lumen maintenance data give a good indication of lumen maintenance in LED lifetime. The manufacturer should provide the raw data in 6,000 h and predict the time of L70/50, indicated as $R_{L70/50.}$ However, 6,000 h life test of lamp last almost 1 year, which is not applicable in current LED lamp development cycle.

The thermal shock test is only 5 cycles per IEC/PAS 62612, which does not simulate lamp's usage profile in the whole life cycle. In 15 years lifetime the lamp will experience thousands cycles of thermal stresses in each switch on/off cycle. Rapid-cycle stress test only has limited thermal to the LED light source and electronic components, which could not assess the reliability of LED lamp.

Table 16.2 Reliability requirements of LED light source and lamp in current standards

Test item	Standards	Description	Remark
Lumen maintenance	IES LM-80-08/ Energy Star	6,000 h life test at 3 different case Temperatures: 55°C 85°C defined by manufacturer	10 samples by Energy Star
Rapid-cycle stress test	Energy Star	Cycle times: 2 min on, 2 min off. Lamp cycled once for every 2 h of required minimum L70 life	10 samples by Energy Star
Lumen maintenance	IEC/PAS 62612	6,000 h life test at 45°C ambient temperatures	Sample size 10
Rapid cycle stress test	IEC/PAS 62612	Cycle times: 30 s on, 30 s off. Lamp cycled once for every 2 h of required minimum L70 life	
Thermal shock	IEC/PAS 62612	−10°C to + 50°C 1 h dwell 5 cycles	

Table 16.3 Failure mechanisms and failure distribution

Subsystem	Failure mechanism	Typical failure rate distribution
LED	Lumen maintenance depreciation color shift over lifetime	Lognormal ($\beta > 3$)
	Catastrophic failure, wire-bond broken, die crack, etc.	Weibull ($\beta > 1$)
Electronic driver	Electronic component fails in useful life	Exponential ($\beta = 1$)
	Solder joint fatigue	Normal ($\beta = 3.5$)
Mechanical	Plastic housing crack	Normal ($\beta = 3.5$)
Optical	Optical coating discoloration Glass bulb crack	Normal ($\beta = 3.5$)

In order to evaluate and assess the reliability of LED lamp, a systematic reliability approach is required to identify the major failure mechanisms of each subsystem, then build a system reliability based on (16.2).

In Figure 16.2, a LED lamp consists of four subsystem and the more than 30 total failure mechanisms of system. Major failure mechanisms for each subsystem of LED lamp are listed in Table 16.3:

Weibull distribution [5] is used to describe the failure rate over time (also called as Hazard Function) for each failure mechanism, and shape parameter (β) tells the character of failure mechanism as showed in Fig. 16.3 Bath curve.

With understanding the failure rate distribution of each failure mechanism, real shape and scale parameters for each failure distribution by reliability tests are found out. Failure mechanisms are caused by different stresses, which could not be covered by only one reliability test. For example, the wear out failure of solder joint fatigue is mainly caused by the thermal cycling; the electronic component failure in useful life is commonly resulted from the thermal stresses and electronic stresses in normal usage.

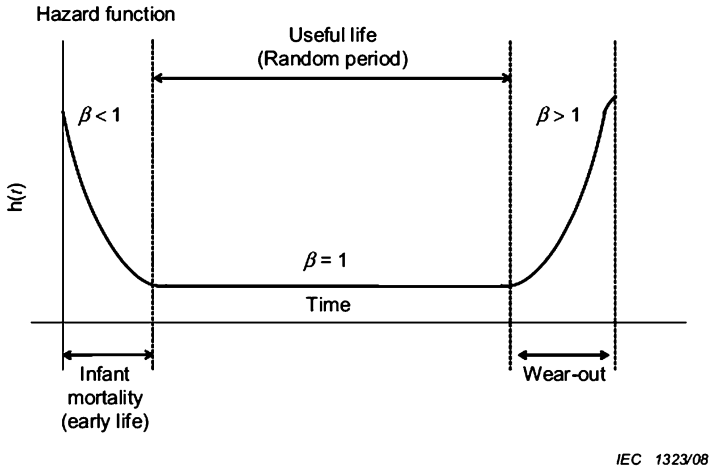


Fig. 16.3 Bath curve according to the IEC 61649 standard.

The system reliability should include failure mechanisms in different stress conditions in product life cycle:

- Lumen maintenance failure (L70) caused by led light source and optic system degradation
- Electronic and thermal stresses for random failure rate of electronic component and LED light source and,
- Wear-out failure of aluminum electrolytic capacitor, the thermal cycling for solder joint fatigue, mechanical housing crack, wire-bond broken of LED die.

The reliability of mechanical of LED lamp is considered as 100% in the whole lifetime for normal application because lamp is normally installed in the socket, and the mechanical stresses from vibration and external shock are rather small and neglected, which is not covered in the paper.

16.5.1 Lumen Maintenance Failure (L70)

IES had published a standard IES LM-80-08 in 2008, defined the methodology to measuring the lumen maintenance of LED light source. It is widely accepted by LED light source manufacturing and lighting industrial. LEDs are tested in three kinds of temperatures (55 C, 85 C and 3rd temperature defined by LED manufacturing) for 6,000 h. Energy Star [6] also requires a 6,000 h life test of LED lamps to demonstrate lumen maintenance. Table 16.4 shows the lumen maintenance of lamp after 6,000 h and the prediction of L70 by exponential degradation model is also listed in Table 16.4.

Table 16.4 The lumen maintenance in 6 K versus L70

Minimum lumen maintenance at end of 6,000 h (% of initial lumens; −3% tolerance)	Maximum L70 life claim (hours)
91.80%	25,000
93.10%	30,000
94.10%	35,000
94.80%	40,000
95.40%	45,000
95.80%	50,000

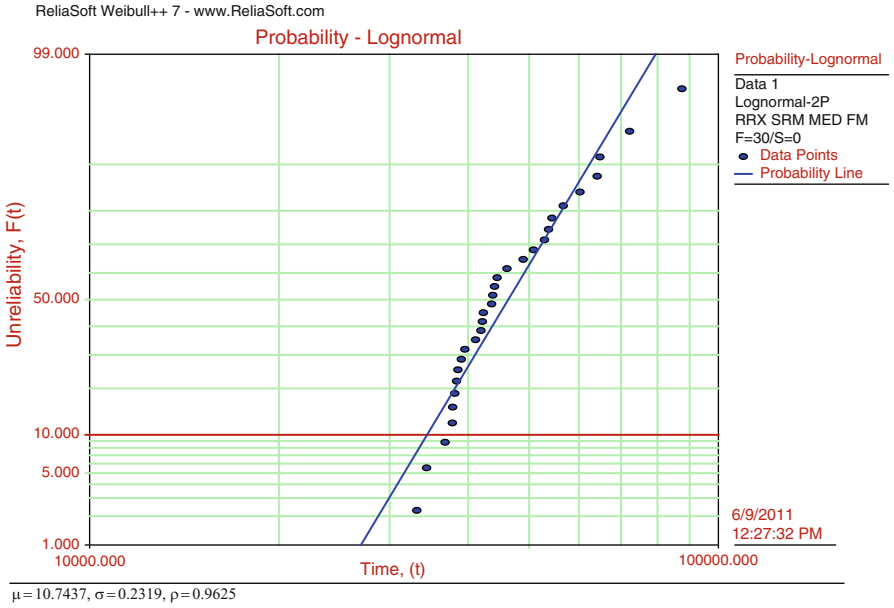


Fig. 16.4 Lumen maintenance per LM-80 data with Weibull plot

The requirement of Energy Star only focuses on the lumen maintenance, and it is an average value of 10 samples. Therefore, it is a B50L70 for lumen maintenance. Moreover, lamps could not burn for 6,000 h before product release which normally is only half of year.

Fortunately, The LM-80 data from LED manufacturing is available already in most case, so it is better to use the LM-80 data of LED light source for the lumen maintenance degradation prediction with exponential degradation model. An example of L70 prediction is shown in Fig. 16.4, based on 30 pcs samples 6,000 h LM-80 test data.

The distribution of L70 is lognormal, mean is 10.7437, and standard deviation is 0.2319. This information will be used for system level reliability modeling.

16.5.2 Random Failure Rate of Driver's Electronic Components

The failure rates of electronic components are well known and several standards are already available, the mostly used in the field are MIL-STD-217 [7] and Telcordia SR-332 [8]. As long as components' case temperature, current, voltage and power are provided, each components' failure rate are calculated and the total failure rate of whole driver is the sum of failure rate of each component.

$$R_{\text{driver}} = \sum_{i=1}^{n} R_{i\text{th}-\text{component}} = \sum_{i=1}^{n} \exp^{-\lambda_i t} = \exp^{\sum_{i=1}^{n} \lambda_i t} \tag{16.5}$$

If the standard is not appropriate, the testing data or field failure data also could be used to calculate the failure rate (λ) of whole driver.

The reliability of LED lamp is estimated as below:

$$R_{\text{random\_failure\_LED\_Lamp}} = \exp(-\lambda T) \tag{16.6}$$

where, λ is the failure rate in Table 16.4. T is the specified operating hour.

16.5.3 Wear Out Failure Mechanism

The heat generated from LED and electronic components is dissipated from housing passively. Because the small design space of LED retrofit lamp, it is very difficult for heat dissipation. It causes the temperature of components, solder joint in LED retrofit lamp are higher than in normal electronic equipment. The wear out of aluminum electrolytic capacitors, fans, and fatigue of solder joint also impact the overall lifetime of lamp.

For example, the LED solder joint temperature is also driven to 90°C in operating in room temperature, which has a 65°C temperature change in a cycle of switch on/off in normal room temperature (25°C). In the whole lifetime of 25,000 h, the product is subjected to more than 10,000 cycles switch on/off cycles, the higher switch cycles leads to more solder joint fatigue, indicating the solder joint fatigue failure is really critical in this switch on/off user environment. The thermal shock is an effective and efficient to evaluate the solder joint fatigue, the acceleration model of thermal shock is Coffin-Mansion equation [9, 10] as follows:

$$N_f = C_0 \times (\Delta T)^{-n} \tag{16.7}$$

And the acceleration factor is described as below:

$$\text{AF} = \left(\frac{N_{\text{use}}}{N_{\text{test}}}\right) = \left(\frac{\Delta T_{\text{test}}}{\Delta T_{\text{use}}}\right)^{n} \tag{16.8}$$

where n is the material property to thermal shock, about 2.66 [10] for lead free.

For normal user conditions (25°C), the temperature of major components, e.g., solder joint is around 90°C. The estimated acceleration factor in a thermal shock test (−40°C to 125°C) is:

$$\mathrm{AF} = \left(\frac{125 - (-40)}{90 - 25}\right)^{2.66} = 11.9 \tag{16.9}$$

Note: the thermal shock temperature range could be adjusted by manufacturer base on the user application conditions and the limitation the product component specification.

Then the failure distribution in a thermal shock test could be translated into the real application condition.

$$R_{\mathrm{wear\_out\_LED\_Lamp}} = \exp\left(-\left(\frac{T}{\eta}\right)^{\beta}\right) \tag{16.10}$$

where β is the shaped parameter, $\beta = 2$ is typical; η is the scale parameter from thermal shock test; T is the switch on/off cycles in operating.

After getting the failure distribution of lumen maintenance, random failure in useful life and wear-out failure of on/off switch, the reliability of LED lamp system is as follows:

$$R_{\mathrm{LED-system}} = R_{\mathrm{L70/50}} \times R_{\mathrm{Random\_failure\_LED\_lamp}} \times R_{\mathrm{Wear-out}} \tag{16.11}$$

16.5.4 System Modeling

In a typical LED lamp system, the reliability distribution for each subsystem and failure mechanisms are as follows:

1. L70: mean = 10.7437, standard deviation = 0.2319 lognormal distribution per Fig. 16.4.
2. Total Failure Rate (λ) is 2863FIT per Telcordia SR-332.
3. Solder Joint Fatigue: $\beta = 2$, $\eta = 2{,}244$

Based on (16.11), the cumulative failure distribution (CFD) and each subsystem failure distribution are obtained as shown in Fig. 16.5.

From the cummulaive failure distribution curve, the B50L70 is around 35,000 h, which is far lower the average L70 = 46,000 h.

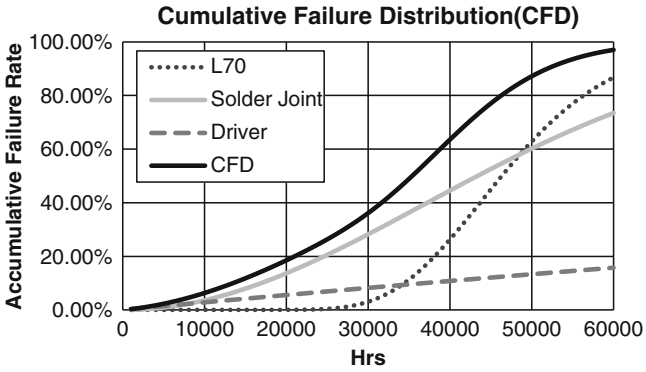


Fig. 16.5 CFD of LED lamp

16.5.5 Reliability Evaluation

As mentioned before, the lifetime evaluation of conventional lamps is simple, efficiency and quick since the failure mechanisms are fully understood. LED retrofit lamps' system is more complex and has multiple failure mechanisms stimulated by multiple stresses. It is impossible to stimulate all failure mechanism with single stress test condition. On the other hand, the failure mechanisms are occurred in different time frame in its long lifetime. A test to exposure all failure mechanism in the lifetime will last very long in multiple stresses.

To manufacturers and end-users, the failure rate in the warranty period of products is more critical. A low failure rate means high reliability, low maintenance cost which helps to improve the manufacturer' image and reputation; to end user, the low failure rate improves the user experience.

Therefore, the reliability evaluation should focus more on the failure mechanism and failure rate in the warranty period. The warranty is normally less than 5 years, in which majority failures are caused by electronic components, workmanships in assembly, or product design. Figure 16.6 shows a color shift the lamp after 300 h test in damp heat environment, in which LED was polluted by chemical gas from material. Accelerated Life Test (ALT) has been used for year and effectively exposure the failure in short period.

Secondly, electronic components are most standardized components and used for decades, their failure rate is stable. The life test for conventional lamps per LM-49-01also could used to evaluate the failure mechanism and accuracy of reliability modeling in early stage even though it takes even more than a year. It is close to the real application and test data could be used for next generation product design and reliability growth. Figure 16.7 shows a comparison between 10,000 h life test data and reliability lifetime modeling result. The result comes from 10,000 h life test in room temperature with 135 pcs samples. The blue curve is the accumulated failure

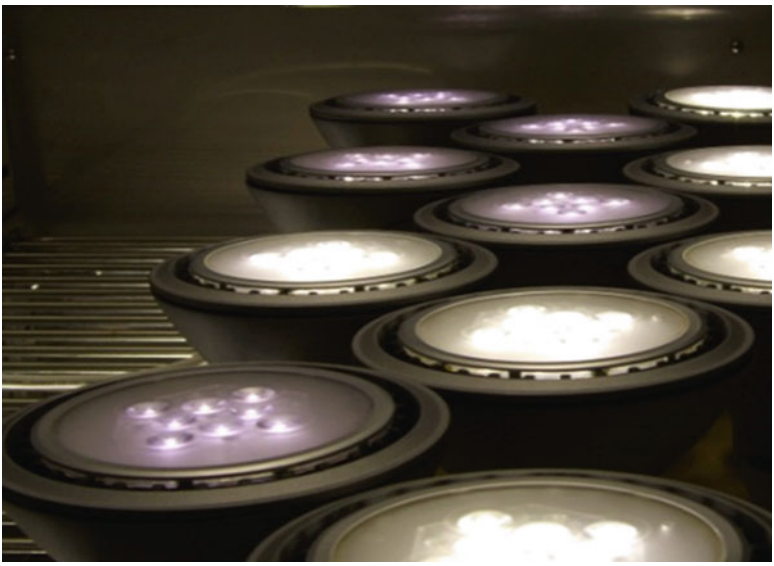


Fig. 16.6 Color shift in damp heat test

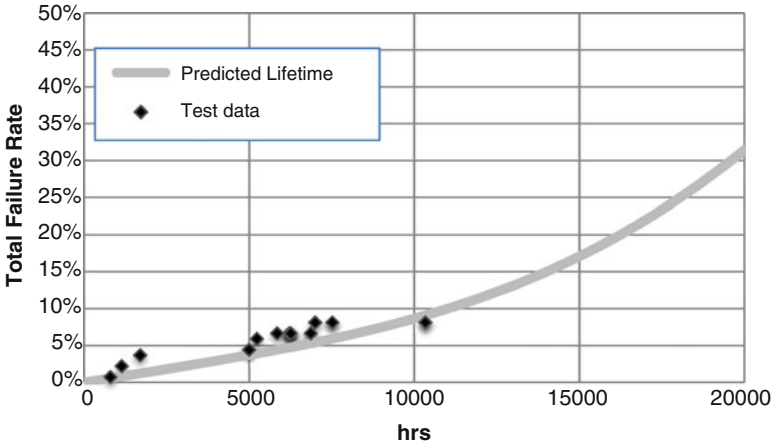


Fig. 16.7 Comparison between modeling and real test data in lab

rate in life tests; the green curve is the lifetime modeling result. The failures in 10,000 h are from electronic components and align with the modeling result.

In other words, the evaluation of LED lamps lifetime should focus on the failure mechanism and failure rate in the warranty period, and the life test should be combined with accelerated or normal environments.

16.6 Summary

Due to the longer lifetime and different reliability definitions of lifetime, the lifetime of LED lamps is more complex than general electronic equipment or traditional lamps. In its lifetime, it includes minimum three types of failure mechanisms, i.e., lumen maintenance, random failure in useful life, and wear-out before end of lifetime.

To obtain the lifetime of a LED lamp system (B50L70), the reliability information for these three types of failures are needed:

- A lumen maintenance data from LED light source manufacturing by IES LM-80-08
- A random failure of electronic driver by external standards, or testing data
- A thermal shock data to address the wear out failure mechanism in the whole lifecycle.

Reliability prediction of LED lighting system lifetime can be achieved as (13) based on above data.

In this chapter we show how such a reliability exercise for a LED Lamp should look like. Guidelines for both reliability predictions and testing are discussed and it is shown that they can be matched quite accurately.

References

1. LM-49-01 IESNA approved method for life testing of filament lamps. Illuminating Engineering Society/1 Dec 2001
2. LM-65-01 IESNA approved method for life testing of single-ended compact fluorescent lamps. Illuminating Engineering Society/1 Dec 2001
3. IES LM-80-08 Approved method for measuring lumen maintenance of LED light sources LM-80
4. IEC 62612 PAS Self-ballast LED-lamps for general lighting services–performance requirement
5. International standards weibull analysis—61649
6. Energy Star® program requirements for integral LED lamps
7. MIL-STD-217 reliability prediction of electronic equipment
8. Telcordia SR-332 reliability prediction procedure for electronic equipment Issue 3, Jan 2011
9. Nelson WB. Accelerated testing: statistical models, test plans, and data analysis. ISBN-13: 978-0471522775
10. “Thermal cycling and thermal shock failure rate modeling”, R.C. Blish, IEEE, IRPS, 1997 and “An acceleration model for sn-ag-cu solder joint reliability under various thermal cycle conditions”, N. Pan et al. HP2005

Chapter 17
SSL Case Study: Package, Module, and System

Daoguo Yang and Miao Cai

Abstract As early as 2004, high power LED was expected to be the dominant lighting technology by 2025. Nowadays, this tendency is becoming more and more obvious based on the higher luminous efficiency and reliability. Many case studies, like thermal design and analysis, junction temperature measurement, reliability assessment, etc., focus on package and module level product. However, for actual application of solid state lighting (SSL) system, only a few studies are carried out by now. Generally, the material degradation and structure damage due to the electrical, thermal, chemical, and mechanical stress will lead to the lumen degradation, color variation or even early death of LEDs. It is clear that SSL system reliability is a challenging and important task that needs to be addressed. In this chapter, the LED reliability issues are divided into four categories according to the LED product forms, which are reliability of LED package, reliability of LED module, reliability of multichip LED module, and reliability of LED system. Several case studies are used to illustrate each kind of LED reliability issues by theoretical/numerical modeling, reliability test, various methods and experiments.

17.1 Introduction

Along with global low-carbon and environmental awareness boosting up, as the fourth generation of lighting sources, LEDs nowadays have caused a revolution in illumination due to its many distinctive advantages of long lifetime, power saving and environment-friendly. In many LED lighting applications, such as traffic lights, the backlighting of liquid crystal display, vehicle headlights and so on, LEDs have played an important role. As early as 2004, high-power LEDs were expected to be

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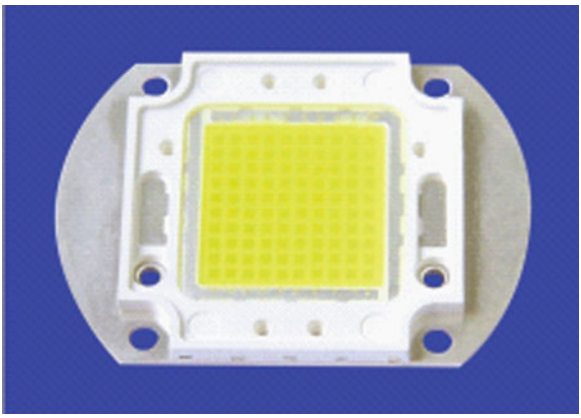


Fig. 17.1 100 W multichip LED module

the dominant lighting technology by 2025. Nowadays, this tendency is becoming more and more obvious due to the higher luminous efficiency and reliability. Especially in general lighting, the market penetration is being accelerated [1, 2].

However, the material degradation and structure damage due to the electrical, thermal, chemical and mechanical stress will lead to the lumen degradation, color variation or even early death of the LEDs [3]. The reliability of the high power LEDs is becoming a big issue for the emerging illumination applications which must be dealt with during LED product development phase with concept of design for reliability which has been practiced in many industries in the past few decades [4].

Some studies indicated that only 15–35% of the electrical power of LEDs is converted into optical power in general high-power LEDs packaging products, and 65–85% of input power is dissipated as excess heat power [5]. In order to dissipate excess heat and increase luminous efficiency for general lighting application, some thermal analysis of LEDs performance, packaging ways of high-power LEDs and heat dissipation methods have been studied and proposed. Biber investigated light emission efficiency of LEDs as a function of thermal condition [6]. It has been reported that high junction temperature of the LEDs would lead to reliability problems such as low quantum efficiency, wavelength shifts, short lifetime, and even catastrophic failure. Some studies showed that the optical output power is degraded with the junction temperature [7].

Multichip LED module is attracting more and more researchers' interests due to its great advantages. For example, hundreds of chips can be integrated into one smaller substrate, white LED modules can be packaged using RGB LED chips, thermal resistance of the module is smaller than that of single chip LED module, and optical efficiency of the module is higher than that of single chip module [8]. Figure 17.1 shows a 100 W multichip LED module. Figure 17.2 illustrates schematic diagram of RGB multichip LED module.

However, when the multichip LED module is operating, if heat dissipation is not proper, it could lead to some reliability problems, such as heat accumulation,

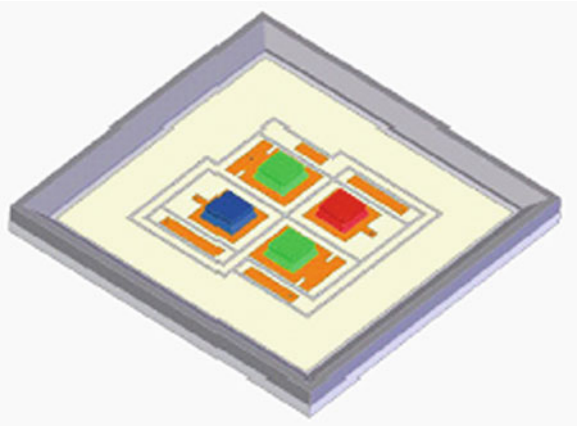


Fig. 17.2 RGB multichip LED module

hotspots, and so on. It is the heat accumulation during the high power operation that causes the recombination of electron and hole at the p-n junction increasingly difficult, which not only reduces the light output and shortens the lifetime of LED, but also changes the forward voltage and shifts the peak wavelength of LED [9]. Besides, hotspots on the LED module could lead to single chip or several chips failure due to higher junction temperature, and ultimately the whole module failure.

So far in package and module levels, many studies have been done on junction temperature measurement, thermal dispersion simulation, reliability test modeling and experiments [10–15]. However, only a few design cases and thermal simulation have been reported for multichip LED module, like COB and RGB [16, 17]. In LED system level, very limited study has been conducted on LED system reliability for SSL applications. Only a few case studies are performed, such as on a generic approach using Monte Carlos algorithm [18], an approach of LED lamp system lifetime prediction [19] and one simulation method of LED lamp to obtain thermal and thermo-mechanical properties [20]. And now LED system reliability is a challenging task since its multidisciplinary issue as well as functional SSL system requires close cooperation between different functional subsystems. This challenge mainly comes from the following [18]:

- The large amount of unknown failure modes and mechanisms;
- The technological gap to physically describe these mechanisms.
- None existing acceleration test methods and/or standards;
- The requested lifetime levels;
- The lack of design for reliability rules.

In this chapter, the LED reliability issues are divided into three categories according to the LED product forms, which are package, module, and system level. Several case studies are used to illustrate each kind of reliability issues by theoretical/numerical modeling, reliability test, and experimental measurements.

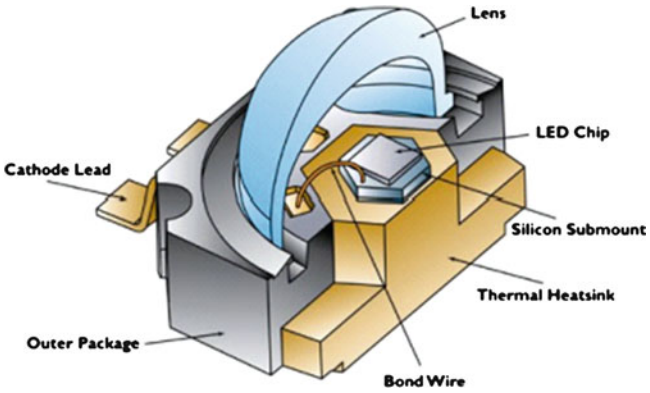


Fig. 17.3 Typical structure of high power LED package

17.2 Case Study 1: Package Level

In this part, LED package refers to single-chip LED package, which contains a single chip in the LED packaging. The reliability of LED packages is related with many aspects, such as humidity, thermal, hydrothermal, etc., and the component reliability as well. The junction temperature of a single-chip LED package is one of the key factors which affect its reliability. And its effective analysis and measurement are important to get solution for reliability issue, which is illustrated by several case studies below.

17.2.1 Thermal Performance Analysis on LED Package

In this study, the forward voltage, the relative flux output, color rending index (CRI) and luminous efficiency of three different LED package samples under seven different junction temperatures were measured, and the data were collected and analyzed.

17.2.1.1 Description of Experiments

Figure 17.3 shows schematically a typical structure of LED package [21]. In the package, the LED chip with vertical structure is mounted on the silicon substrate. Heat sink is used to conduct the superfluous heat generated by LED chip. Cathode and anode leads are connected to chip with bond wire. The LED chip is covered with silicone lens with phosphor. The size and amount of the chip in the high power LED package should be designed according to different product needs.

Three high power LED packages are selected as measurement samples, which are referred as A, B and C, respectively. The packages are consisted of LED chip, silicone resin lens with phosphor, substrate, PCB etc. Both sample B and C are blue LED chip plus phosphor, but with some additional red phosphor in the silicone lens



Fig. 17.4 Data acquisition, 0.5 m integrating sphere system, and multimeter

for sample B. The packaging structure of sample A is different from the other two. It contains blue LED-chip with phosphor and red LED-chip. These three samples were supplied by different packaging companies, and the number, dominant wavelength and distribution location of module chips, packing phosphor material, are also different more or less.

The measurement equipment consists of 0.5 m Integrating Sphere System with related Spectrometer and Instrument System, special Heater with 20 cm-heat block, Multimeter, Data Acquisition, and so on. They are partly shown in Fig. 17.4. The package samples are mounted on the heat sink of an automatic heater located on the surface of 0.5 M optical integrating sphere.

In the measurement, the junction temperature is controlled at seven levels (25°C, 50°C, 65°C, 75°C, 85°C, 95°C, 100°C) in sequence, the ambient temperature of test lab is maintained at 25°C (room temperature). The samples are measured in DC pulse at each temperature level. The related test data is acquired and consolidated by the data acquisition system. In the measurement, the typical current is 350 mA for sample A, 480 mA for sample B and 40 mA for sample C, respectively. The measurement time of pulse current is set to 25 ms for all samples.

Figure 17.5 shows the curves of the forward voltage vs. the junction temperature, indicating that the forward voltage decreases linearly as junction temperature increases. The corresponding values of K factor for sample A, sample B and sample C are 0.0158 V/°C, 0.0128 V/°C and 0.0505 V/°C, respectively.

With rising of the junction temperature, the relative flux output and the luminous efficiency of the three samples decrease, shown in Fig. 17.6. The measured data of sample B change least with junction temperature. The CRI value of sample A decreases, from 90.5 at 25°C to 84.8 at 100°C; the CRI value of sample B is stable and around 86; the CRI of sample A increases, but the change is not very obvious.

Due to different packaging phosphor and LED chip technology partly mentioned above, the high power LED packaging modules have different performance: the module B has the best performance stabilization; the temperature stability of module A is not good, but it has excellent luminous efficiency and CRI, especially R9 index; the luminous efficiency of module C is high but its CRI is low.

The test results indicate that raising junction temperature would decrease luminous efficiency, and junction temperature beyond reasonable range would affect the

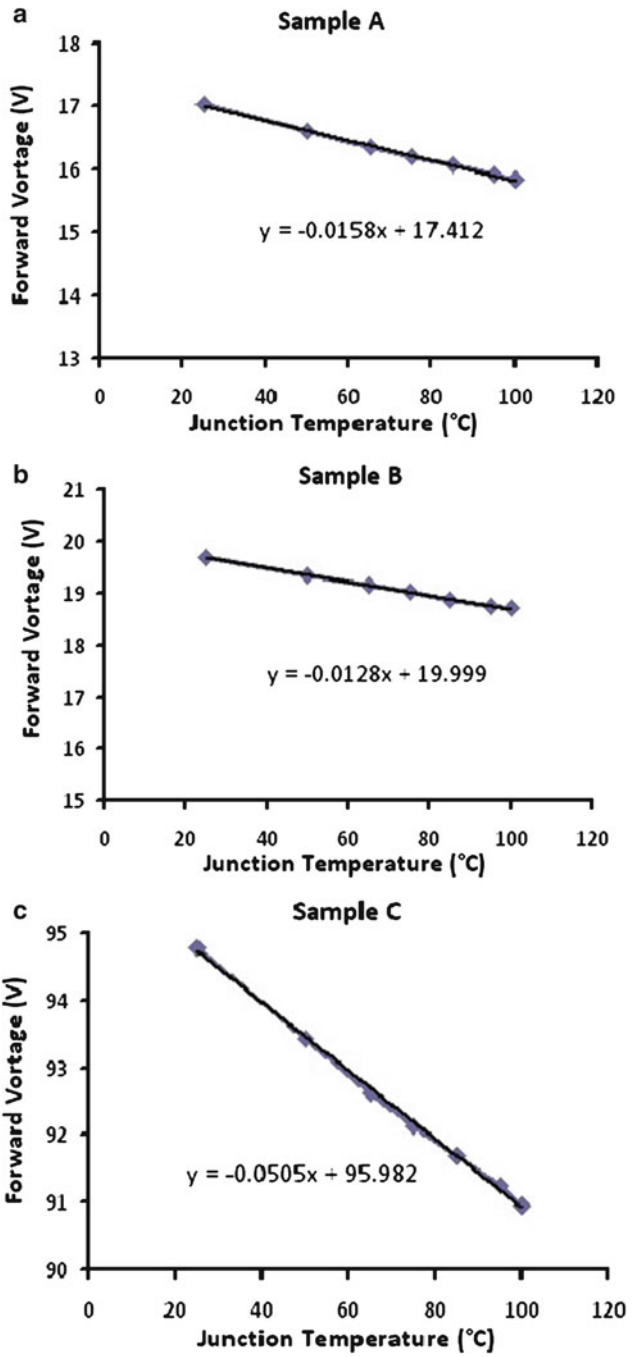


Fig. 17.5 (**a**) Forward voltage vs. Junction temperature for sample A; (**b**) Forward voltage vs. Junction temperature for sample B; (**c**) Forward voltage vs. Junction temperature for sample C

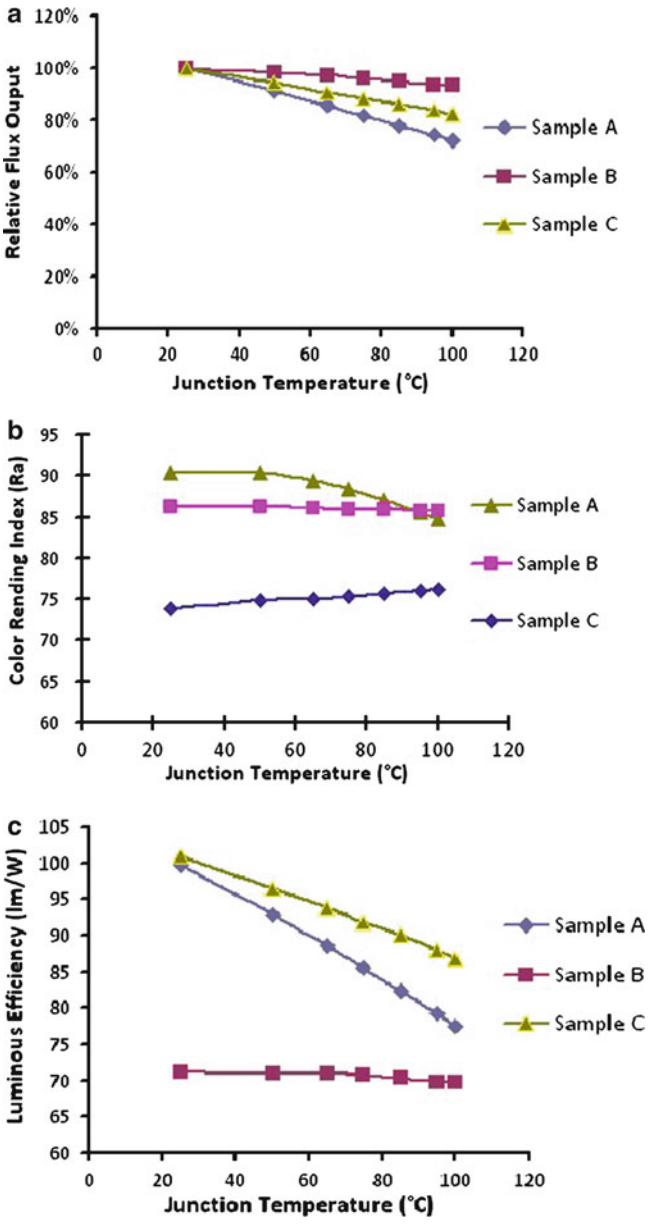


Fig. 17.6 (**a**) The relation between relative flux output and junction temperature; (**b**) The relation between color rending index (CRI) and junction temperature; (**c**) Luminous efficiency vs. Junction temperature

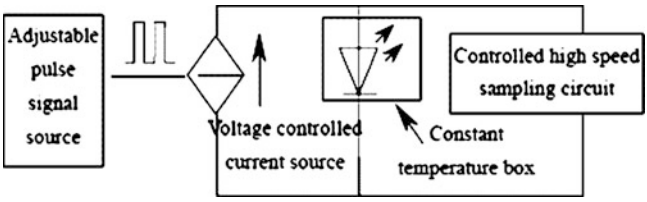


Fig. 17.7 The principle of pulse current measurement

practicality and reliability of packaging modules. So we need some heat dissipation solutions, such as heat pipes, fans, micro-jet array cooling and so on, to drop the operating junction temperature of LED packaging modules.

17.2.2 Measurement of LED Junction Temperature Using Pulse Current

This study investigates the pulse current method used as a junction temperature measurement method of LED package. The theory of the method is described and some experiments are carried out. The pulse current method is a new method which can be used to measure the junction temperature simultaneously [22]. Figure 17.7 shows the principle of pulse current measurement. By applying short pulse of square-wave current with constant pulse amplitude to the LED, the LED's forward voltage is measured at different junction temperatures.

The sensitivity coefficient of forward voltage and junction temperature can be expressed as:

$$s = \frac{V_{\mathrm{F}}(j) - V_{\mathrm{F}}(0)}{T_j - T_0} \tag{17.1}$$

in which T_0 is the initial temperature of constant temperature box; and $V_{\mathrm{F}}(0)$ is the forward voltage when injecting constant short pulse; $V_{\mathrm{F}}(J)$ is forward voltage at different temperature T_j.

Then, the junction temperature is represented as:

$$T = \frac{-\Delta V}{S} \tag{17.2}$$

After the sensitivity coefficient of forward voltage and junction temperature are obtained under a rated current, the junction temperature can be calculated by measuring the forward junction voltage (V) under the rated current and certain temperature.

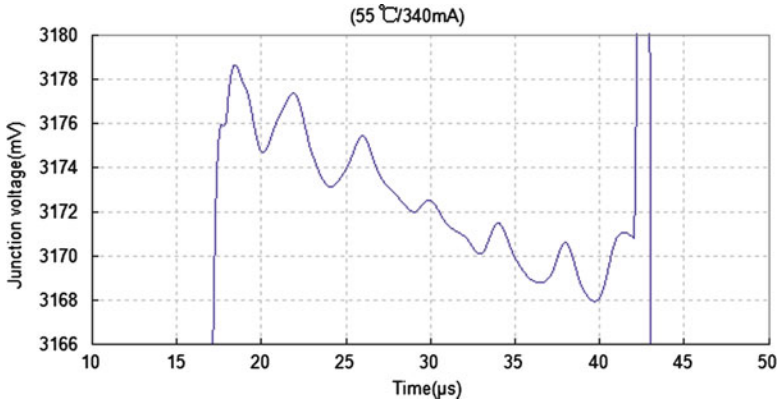


Fig. 17.8 Junction volt variation at 40 μs of pulse current

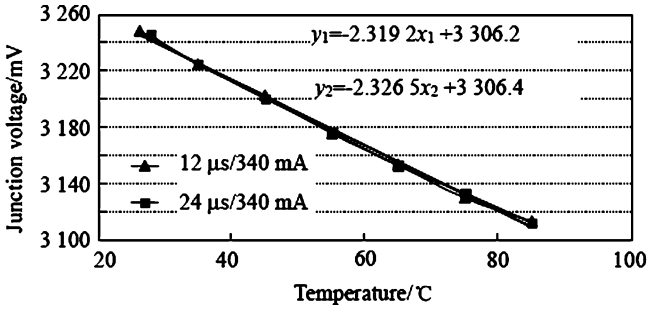


Fig. 17.9 Pulse current VF-T relation curves

Using above-mentioned procedure, by injecting constant short pulse of square-wave current to the LED, the forward voltage (VF) of LED is measured at 40 μs of pulse current 340 mA at 55°C. As shown in Fig. 17.8, the LED's forward voltage is fast decreasing by about 10 mV within the 40 μs, and the maximum voltage can be selected as our junction voltage objective. In Fig. 17.9, a linear function of VF-T is obtained during constant temperature of 20–85°C, which indicates the sensitivity coefficient S is −2.326 5 (mV/°C). Then the junction temperature can be calculated by using (15.2) if forward junction voltage is under certain constant current and temperature.

Figures 17.10 and 17.11 are the example applications on junction temperature assessment. The influence of pulse current width on the measurement of junction temperature is investigated on two LED packages in Fig. 17.10. Figure 17.11 shows the junction temperature variation while injecting different width pulse current. These results show that, in order to achieve that the measuring accuracy of junction temperature is lower than 1°C, the pulse width should be controlled from a few to a dozen microseconds.

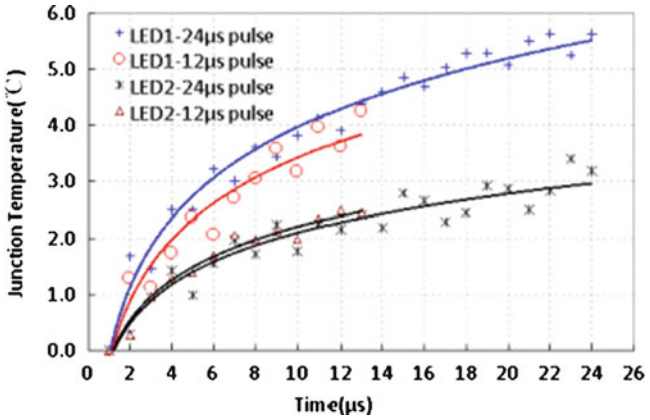


Fig. 17.10 The different LED junction temperature variation by single pulse input

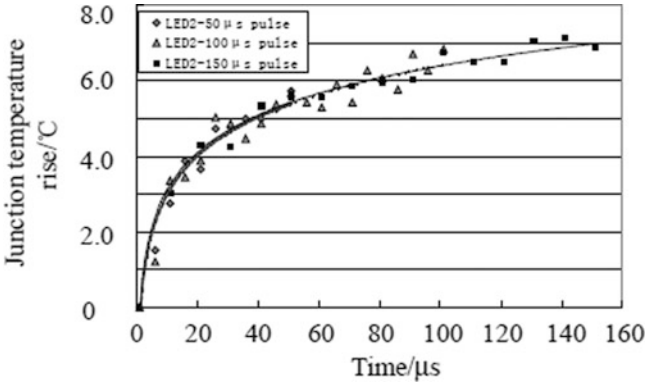


Fig. 17.11 The same LED junction temperature variation by different width pulse input

Above measurement application shows that it is promising to use the pulse current method for measuring LED junction temperature. More investigations should be carried out on reliability relevant study on LED package, module and system in the future.

17.3 Case Study 2: Module Level

The junction temperature of LED array module and multichip LED module is concerned in this part due to its fatal influence on the LED reliability. Proper structure design can low the junction temperature of LED array module. Finite element method (FEM) is helpful to design the structure and experiments can verify the design result [13]. One case study for array module, and two case studies for multichip LED module are employed to illustrated the issue.

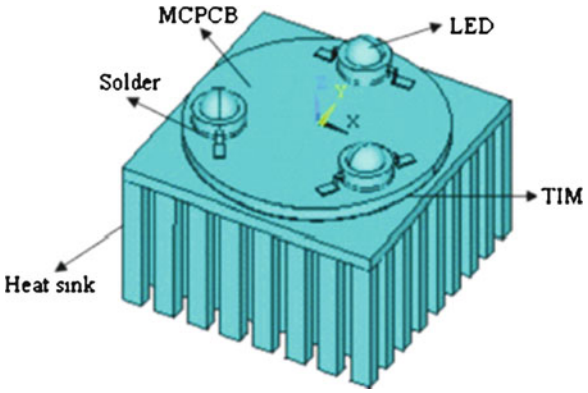


Fig. 17.12 Finite element model of the high power LED array module

17.3.1 Thermal Analysis of LED Array Module

In this section, an investigation on a 3 W high-power LED array module with an in-line pin fin heat sink is conducted. The module was designed, fabricated, and then studied for thermal transient analysis [13]. Finite element simulation was conducted and electrical test method was used to evaluate the thermal performance of the LED array module.

17.3.1.1 Finite Element Simulation

The LED array module is mainly consisted of high power LED array, SnAgCu solder, MCPCB, thermal interface material (TIM), in-line pin fin heat sink and etc. The LED array is mounted on a circular MCPCB. The size of MCPCB is: 18 mm in radius and 1.758 mm in thickness. In order to improve the capability of heat dissipation, an in-line pin fin heat sink is installed onto the MCPCB with TIM. The geometric parameters of the in-line pin fin heat sink are: the base size is $38 \times 38 \times 2$ mm, the fin size is $3 \times 2 \times 20$ mm, and the pitch is 5×4.5 mm. The finite element model of the module is shown in Fig. 17.12.

The temperature distribution of the LED array is shown in Fig. 17.13. It can be seen that the maximum temperature of the module is 40.9°C. Such a thermal performance meets the requirement that the LED junction temperature must be below 120°C so that it works normally. It is critical to maintain a junction temperature below 120°C during operation in order to obtain better performance with a longer life of high power LED [19]. The simulation result indicates that the heat dissipation of the structure design is reasonable and the effect of heat dissipation is effective and satisfactory.

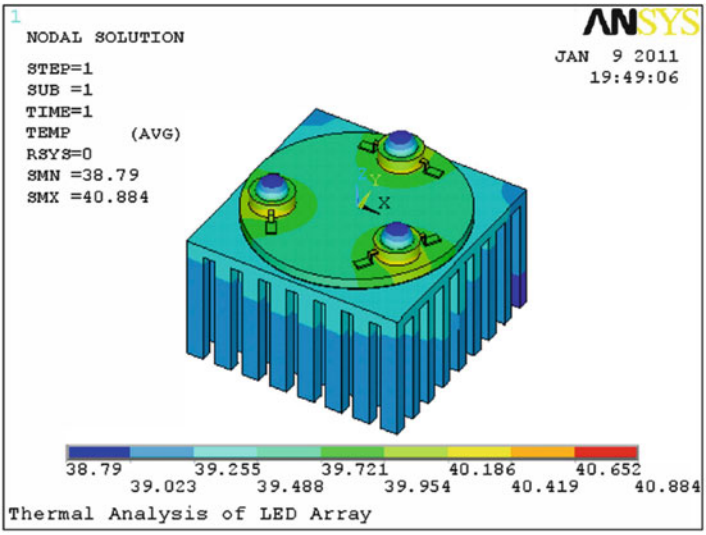


Fig. 17.13 Temperature distribution of the LED array system

17.3.1.2 Thermal Transient Measurement

High power LED array system with an in-line pin fin is fabricated according to the simulation model. Electrical test method is used and thermal resistance and photoelectric performances of the fabricated LED array system are measured through the T3ster and the integrating sphere, respectively. In the testing process, drive current is 290 mA, heating time is 60 s, sense current is 10 mA, measuring time is 100 s, and the ambient temperature is 25°C. The measured input electrical power is 2.81 W.

Figure 17.14 shows the calibration factor of the LED array. It is defined as the ratio of the forward voltage drop to the temperature rise. It can be seen that when 10 mA sensor current is used in the temperature range of 20–40°C with an increasing step of 5°C, the factor of the array is −3.445 mV/°C. Figure 17.15 shows the optical power of the LED array. It is indicated that the output optical power is 500 mW when the ambient temperature is 25°C and the drive current is 300 mA.

Figures 17.16 and 17.17 show the cumulative and differential structure function of the LED module, respectively. The thermal resistance of the chip, die attach, heat slug, solder, MCPCB, TIM, and heat sink can be obtained from the data. It can be seen that the thermal resistance of solder is 2.09 K/W, the highest among them. The cumulative thermal resistance from LED array average junction to the ambient is the sum of them, and it is about 6.7 K/W. The cumulative thermal capacitance is infinite. According to the equation of thermal resistance [20], it can be calculated that LED junction temperature is 40.5°C. As shown in the Fig. 17.16, the same local slope shows a kind of material in the heat flow path. As shown in Fig. 17.17, the local peaks and valleys indicate reaching new materials or changed cross sectional area in the heat flow path. In order to get accurate thermal resistance of every kind of material in the heat flow path, the

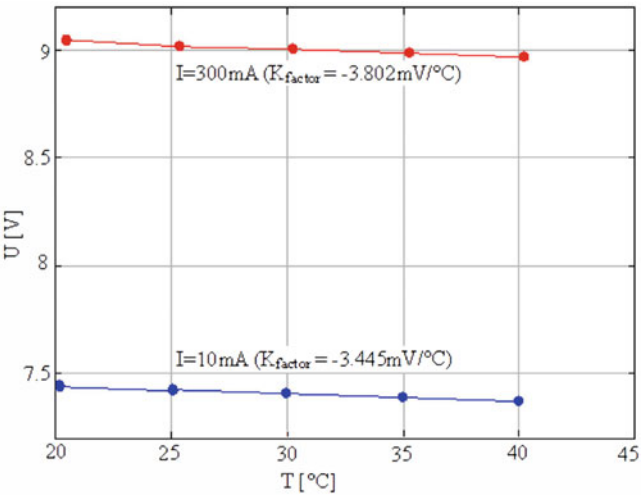


Fig. 17.14 The calibration factor of the LED array

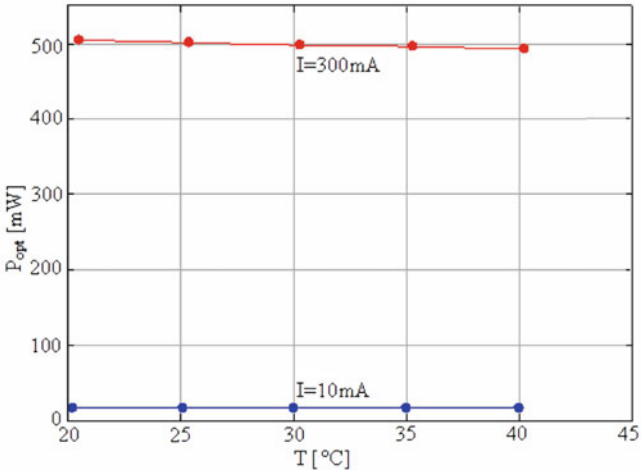


Fig. 17.15 Optical power of the LED array

curves of cumulative structure function and differential structure function should be analyzed simultaneously.

In this case, the LED array average junction temperature analyzed by FEM is 40.884°C, the measured cumulative thermal resistance of the LED array system by electrical test method is about 6.7 K/W, and corresponding LED array average junction temperature is 40.5°C. By comparison, a good agreement between simulation and experiment result is seen.

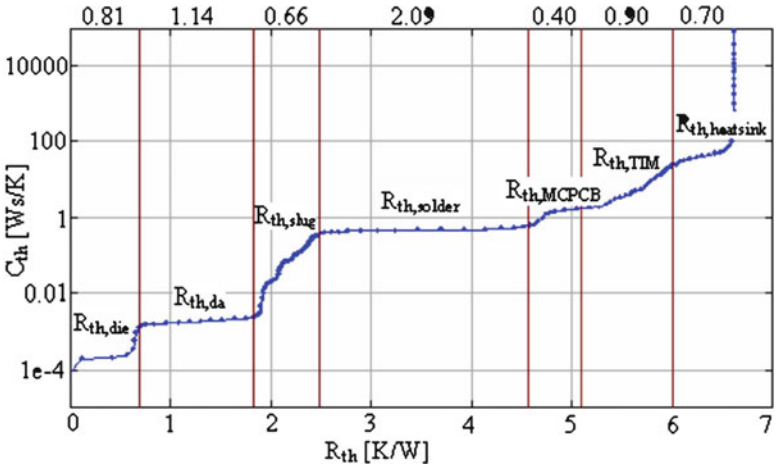


Fig. 17.16 Cumulative structure function

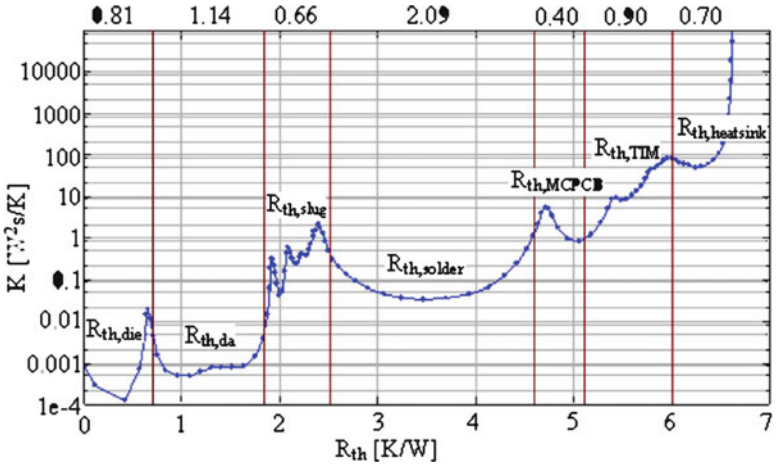


Fig. 17.17 Differential structure function

17.3.2 Thermal Design of Multichip LED Module with Vapor Chamber

Heat dissipation is very important for the reliability of multichip LED module due to its high power and small heat dissipation area. In this study, a model for a 100 W multichip LED module with vapor chamber printed circuit board (VCPCB) coupled with sunflower heat sink is established using the software ANSYS, and the temperature distribution of the module is simulated [16].

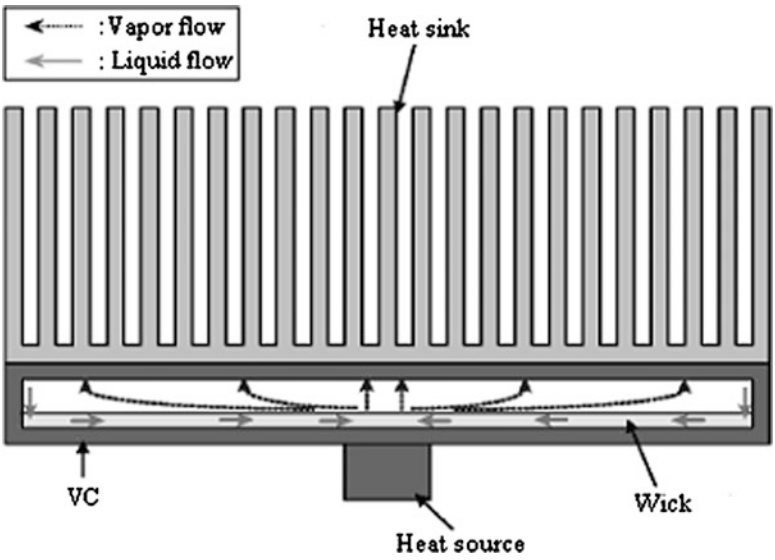


Fig. 17.18 Schematic illustration of VC

17.3.2.1 Description of the Carrier

A vapor chamber (VC) is a flat rectangular heat pipe with large effective thermal conductivity due to the phase change phenomena. A schematic illustration of VC is shown in Fig. 17.18. Heat generated by heat source below the evaporator section comes into the VC through conduction. Liquid saturated in the wick evaporates into vapor which carries the heat into vapor space. The vapor flows from the higher pressure region in the evaporator section to the condenser section that covers the entire top of the structure, and transfers the heat to the ambient through condensation and external cooling. The liquid flows back to the evaporator section by capillary action in the wick structure. For electronics applications, the combination of water and sintered copper powder wick structure is often used [21].

In general, metal core printed circuit board (MCPCB) consists of solder mask, copper circuit layer, thermally conductive dielectric layer, and aluminum plate layer. However, thermal conductivity of aluminum plate is 216 W/m°C, which is much smaller than that of vapor. Besides, uniform temperature performance of VC is much better than that of aluminum. Hotspot of multichip LED module can be eliminated. Reliability of multichip LED module can be improved. VCPCB is thus expected to have excellent thermal conductive capability. Figure 17.19 shows the structure of VCPCB.

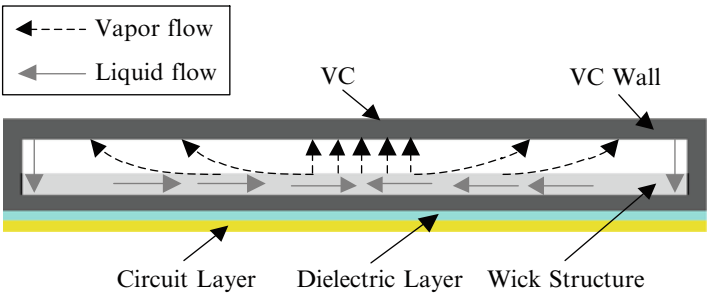


Fig. 17.19 The structure of VCPCB

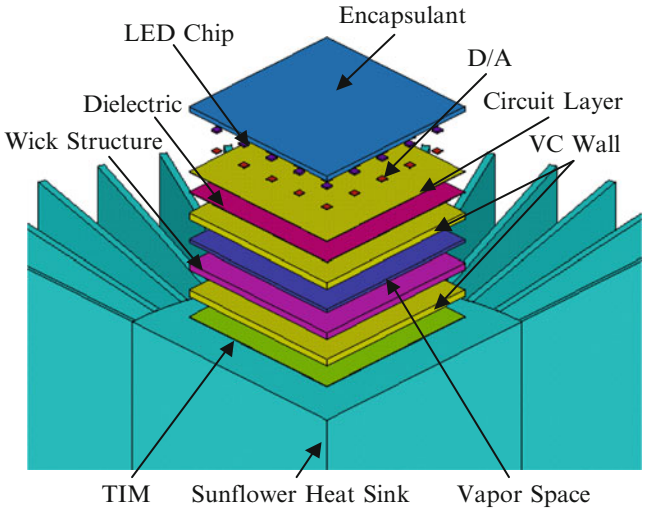


Fig. 17.20 A quarter model of the module

17.3.2.2 Finite Element Modeling

Figure 17.20 shows a quarter model of a 100 W multichip LED module with VCPCB coupled with sunflower heat sink after magnification and separation. In this model, 10 × 10 GaN-based blue chips array are soldered by eutectic 80Au20Sn solder. 10 chips are in series and then in parallels. Heat is generated from the p-n junction of LED chips and is transferred through various paths to the ambient [22]. A major fraction of the heat is transferred by conduction to the sunflower heat sink base through die attach (D/A), copper circuit layer, dielectric layer, VC, and TIM, respectively. At the fin surfaces of sunflower heat sink, heat is dissipated into the ambient by means of convection.

Temperature distribution of the LED module is shown in Fig. 17.21. As can be seen from the figure, the lowest and highest temperature are about 56.0°C and 68.1°C, respectively, and the lowest temperature occurs at the end of fins. Because the heat is generated at the LED junction, the highest temperature occurs in the LED junction, and the highest junction temperature of the LED module is about 68.1°C, which meets the

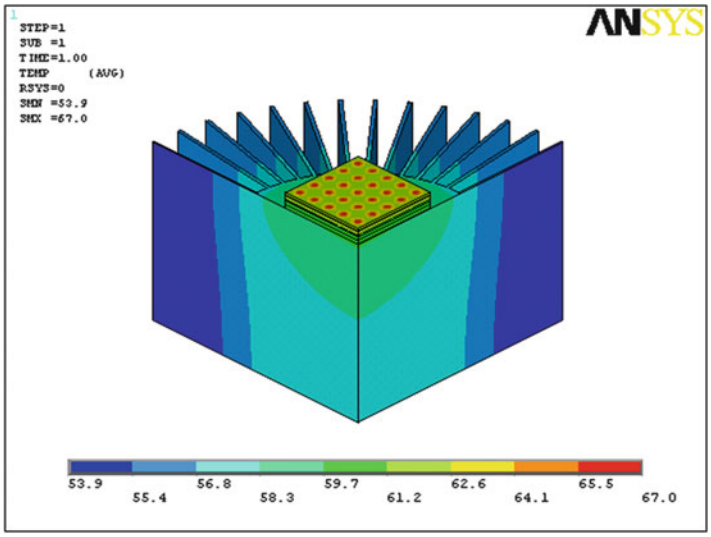


Fig. 17.21 Temperature distribution

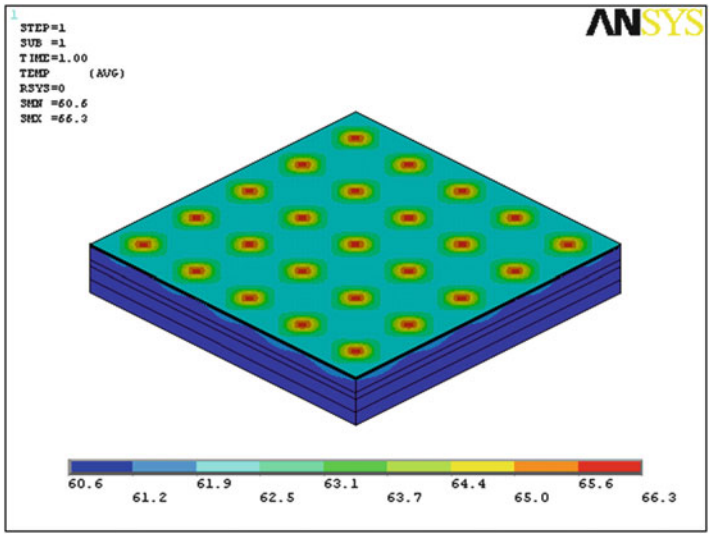


Fig. 17.22 Temperature distribution of VC

requirement that the LED junction temperature must be below 120°C when it works normally. It is critical to maintain a junction temperature below 120°C during operation in order to obtain better performance with a longer life of high power LED [23]. The simulation result indicates that the overall design of the heat dissipation structure of the LED lamp is reasonable and the effect of heat dissipation is effective and satisfactory.

Figure 17.22 shows the temperature distribution of the module with VC. It is found that the temperature is almost uniform at the top of VC, which reveals that VC has

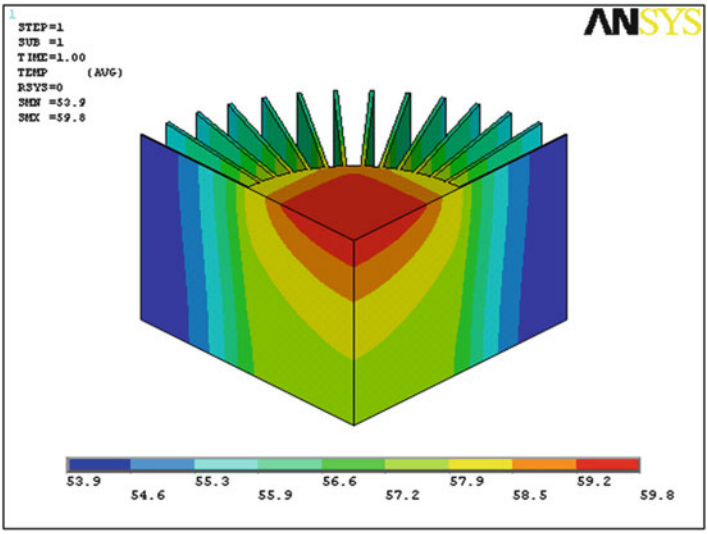


Fig. 17.23 Temperature distribution of heat sink

good temperature uniformity, and thus can ensure uniform temperature of all LED chips and improve the reliability of LED module. Figure 17.23 illustrates the temperature distribution of the module with a sunflower heat sink. It can be seen that the temperature is highest at the center of the sunflower heat sink. Heat is transferred from the center to the bottom and surroundings, finally to the fins. The temperature gradient shows the heat sink is perfect for the heat dissipation of the multichip LED lamp.

Simulation results indicate that the overall design of the heat dissipation structure of the LED lamp is reasonable and the effect of heat dissipation is effective and satisfactory, uniform temperature performance of VC is good, and the sunflower heat sink is perfect for the heat dissipation of multichip LED lamp. Therefore, multichip LED module with VCPCB coupled with sunflower heat sink provide a better solution to improve the heat dissipation issue.

17.3.3 Thermal Design of Multichip LED Module with Ceramic Substrate

In this study, multichip LED modules with aluminum nitride (AlN), Al, and aluminum oxide (Al_2O_3) based substrates are designed, fabricated, and investigated [17].

17.3.3.1 Description of the Carrier

In this case, multichip LED modules with aluminum nitride (AlN), Al, and aluminum oxide (Al_2O_3) based substrates are designed, fabricated, and investigated.

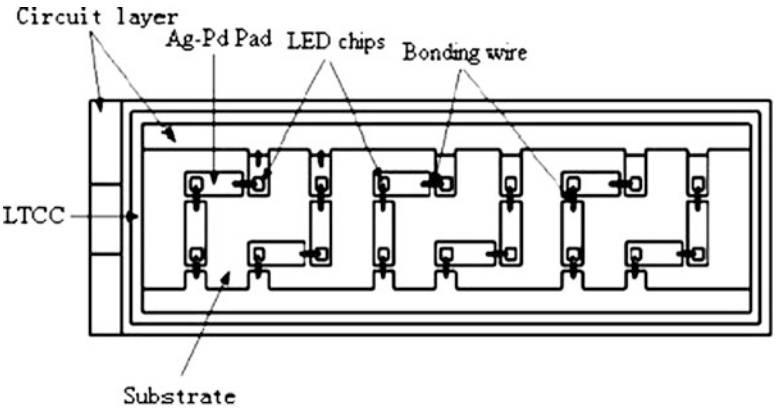


Fig. 17.24 Structure of multichip LED module

Figure 17.24 shows the structure of multichip LED module with the three kinds of substrates. The structure is mainly consisted of four different parts, 18 LED chips, silver paste, substrate, and aluminum heat sink. FEM and electrical test method were used to evaluate the thermal performance of the LED modules.

17.3.3.2 Finite Element Simulation

FEM is used to optimize the thermal design of LED modules with three different substrates. The simulation results of chip distribution in three and two rows were shown in Fig. 17.25a, b, respectively. Comparing the simulation results, it is obviously the highest junction temperature of the model (b) is 0.14°C lower than that of model (a). It can be concluded that chip distribution in two rows is a better choice than in three rows. Figure 17.25c, d shows the temperature distribution of the model with Al and Al_2O_3 based substrates, respectively. It can be seen that the maximum temperature in Fig. 17.25b is lowest. From the simulation results, it can be concluded that the module with AlN-based substrate exhibits better thermal performances.

17.3.3.3 Experiments

Figure 17.26 shows the fabricated LED module with AlN-based substrate. Thermal resistances of the devices are measured through a thermal resistance measurement system. Figure 17.27 shows the average thermal resistance of the three substrate packages. From the figure, it is observed that the thermal resistance of device with AlN-based substrate is 54.9% and 40.2% lower than that with Al and Al_2O_3 based substrate, respectively.

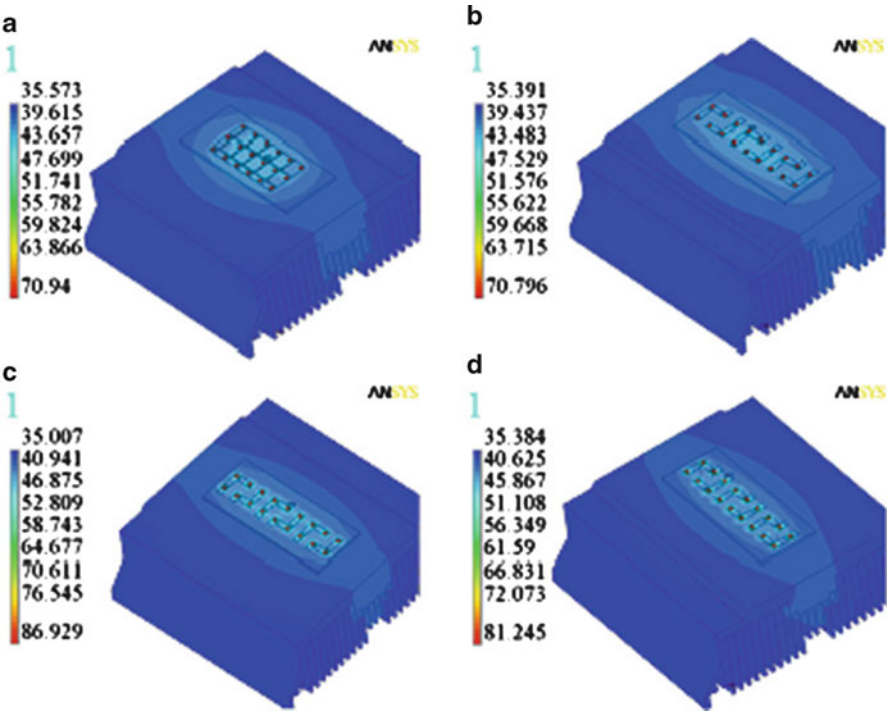


Fig. 17.25 Temperature distribution of (**a**) AlN-based substrate module with chips in three rows; (**b**) AlN-based substrate module with chips in two rows; (**c**) Al based substrate module with chips in two rows; (**d**) Al_2O_3 based substrate module with chips in two rows

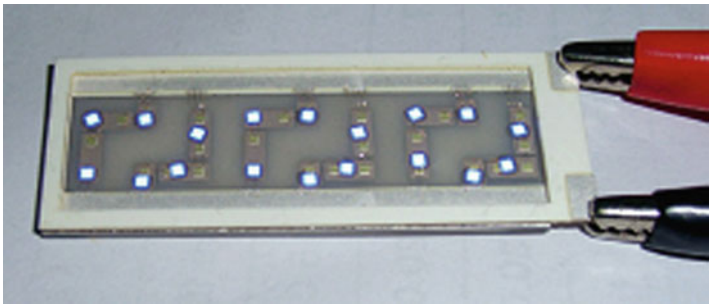


Fig. 17.26 Fabricated LED module with AlN-based substrate

Both the simulation and experimental results show that the module with AlN-based substrate exhibits better thermal performances than modules with Al and Al_2O_3 based substrates. Therefore, multichip LED module with AlN-based substrate has better reliability.

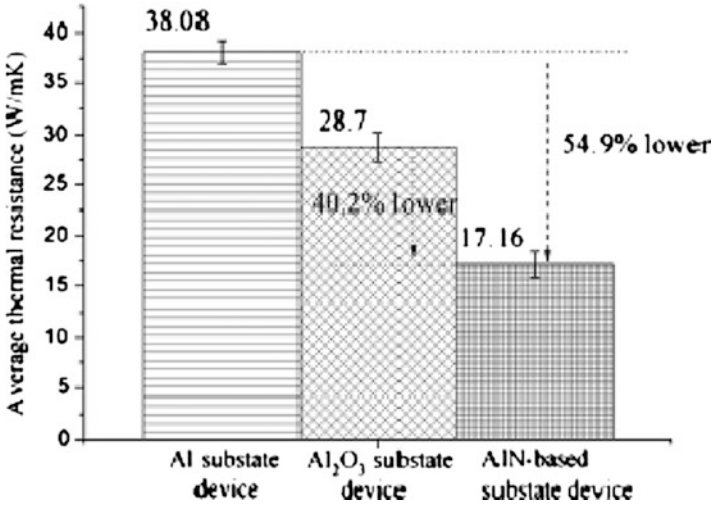


Fig. 17.27 The average thermal resistance of three substrate packages

17.4 Case Study 3: System (Luminiare) Level

Normally a LED Lamp includes the four subsystems [5]: (1) LED as light source; (2) Electronic driver which provides power to LED lighting source; (3) Mechanical housing used for thermal dissipation, electronic isolation, and final installation; (4) Optical lens or bulb which fulfills the optic requirements, e.g., color over angle, beam angle. In order to evaluate the system reliability, it is necessary to understand the reliability of each subsystem in the lifetime and the failure modes of each subsystem. In this section, three methods for evaluation of the reliability of LED system are overviewed and a new method is proposed. One of the most commonly used methods is based on lumen depreciation test outlined in LM-80[24]. The physic based approach was introduced to study a LED lamp system where its failed due to the failure of the epoxy lens[25]. Others continued this study and conducted a series of work on LED system reliability and lifetime prediction, such as traditional approach[25], generic system level approach[18], and an approach for "Design for Reliability" in SSL[26]. In this section, three methods for evaluation of the reliability of LED system are summarized.

17.4.1 Overview of Evaluation Methods for LED System Reliability

17.4.1.1 Monte Carlos Algorithm

A generic approach using Monte Carlos algorithm is shown in Fig. 17.28 [18]. This approach has been used to predict SSL system reliability by a standard conducted by van Driel et al [24]. Figure 17.29 shows that the LED emitters account for 30%

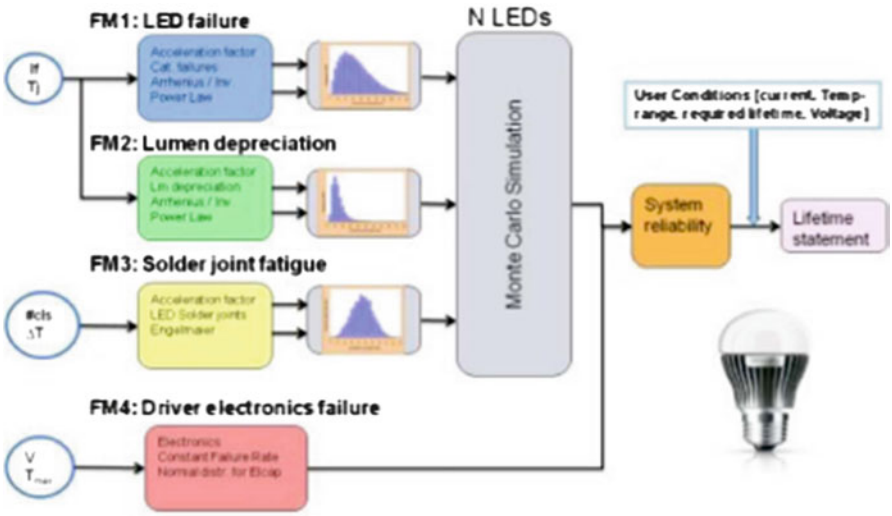


Fig. 17.28 A schematic illustration of the generic system reliability approach using Monte Carlo simulation

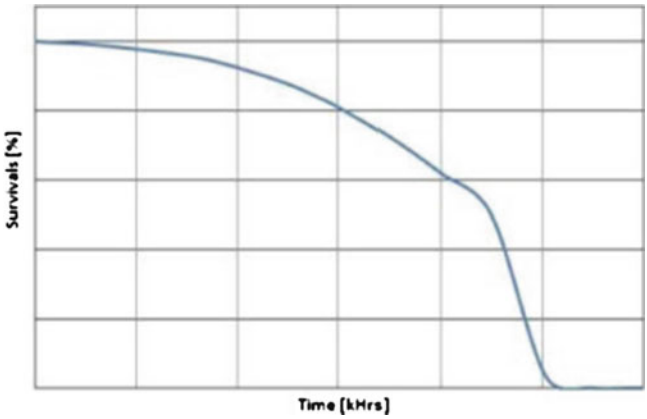


Fig. 17.29 Survival over time for a typical SSL system

of the failure whereas solder interconnect and driver account for 44% and 26% of the failure respectively after 20,000 h of operation.

17.4.1.2 The Hybrid Statistic Approach

An approach based on hybrid statistic method has been proposed for investigation of LED system level reliability [18]. This approach consists of fault tree (FT), Bayesian Belief Net (BBN) and Markov Chain (MC). The FT is used initially to

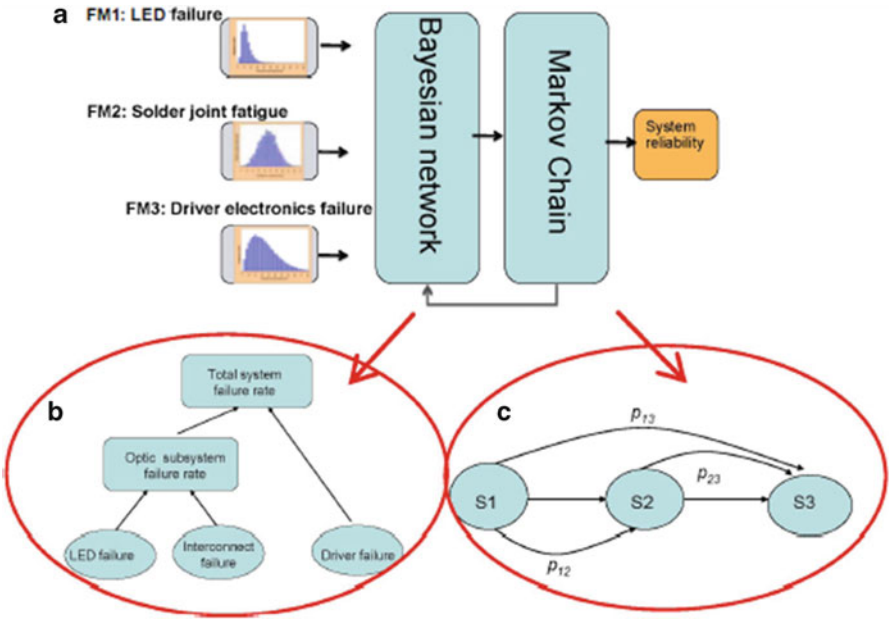


Fig. 17.30 The hybrid statistic approach y for system reliability of SSL system

quantitatively model the root cause of the failure of the whole system. Basically, the complexity of the system can be reduced. BBN is then applied to account for the interaction among the failure mechanisms. In this way, the application of FT and BBN has systematically modeled the system reliability as well as the component level reliability within each time step. MC is a dynamic statistical approach, which can then be used to model the evolution of each individual failure mechanism with respect to time.

Figure 17.30 shows a schematic illustration of using MC for predicting evolution of the failure mechanisms. S1, S2 and S3 are the three different stages of failure mechanisms evolution. The steps of the approach are as follows [18]:

- Identify the main failure mechanism of SSL system using FT.
- Investigate the degradation of each failure mode.
- Predict the interaction of the different failure modes using BBN.
- March the time forward using Markov chain analysis.
- Repeat step 3 and 4 until system failed.

17.4.1.3 Simulation Method

Simulation tools, such as ANSYS-CFX, CoventorWare, etc., have been widely used for modeling of the thermal and thermo-mechanical properties of LED luminaries. Jakovenko et al. [6] used ANSYS-CFX and CoventorWare to simulate

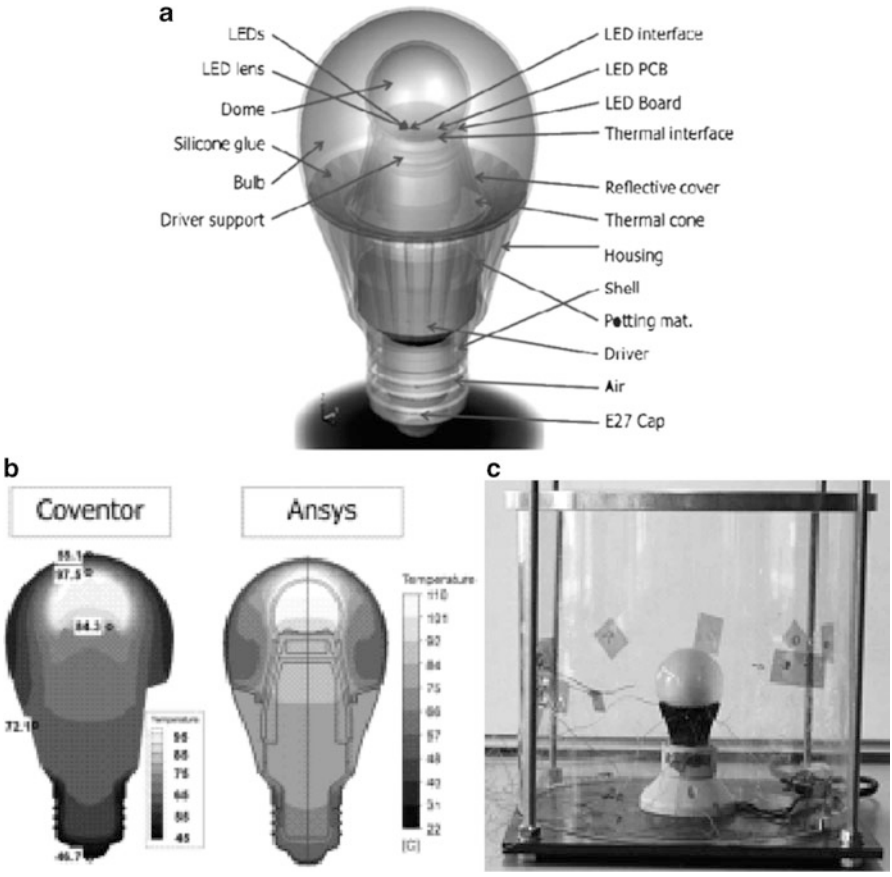


Fig. 17.31 (**a**) 8 W LED lamp 3-D model, (**b**) Steady state thermal analysis, comparison between Coventor and ANSYS simulation tool, (**c**) Measurement setup

the thermal performance of a LED lamp. The simulated thermal distribution has been validated with thermal measurement on a commercial 8 W LED lamp as depicted in Fig. 17.31. The LED lamp was placed in a tube with air temperature control (22°C). The temperature was measured as a function of time at several locations on inner and outer parts of the lamp using thermocouples. Thermocouples were placed on the LED board, thermal cone, housing and shell of the lamp. Also the air temperature in the tube was measured.

The obtained results are in reasonable agreement as depicted in Fig. 17.32. Improvement of the simulation model and prescribed heat generation will result in a better prediction of the measured temperatures. The simulated LED temperature was 90°C for the Coventor simulation and 86°C for the ANSYS simulation; a temperature of 91°C was measured on the board close to the LED die. Their research showed that with these thermal simulation tools critical parts can be determined when designing higher power LED lamps and solutions for thermal problems explored.

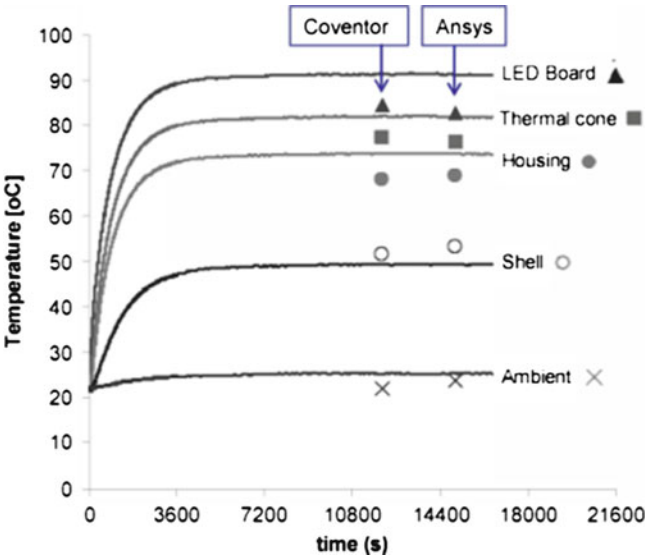


Fig. 17.32 The measured (*line*) and simulation (*symbol*) temperatures for an open top luminiare

17.5 Summaries and Conclusions

This chapter shows the reliability case studies of LED package, module and system. To demonstrate the reliability study of LED package, the case of thermal performance analysis on LED Package is presented. The results indicate that raising junction temperature decreases luminous efficiency, and junction temperature beyond reasonable range affects the practicality and reliability of packaging modules, and heat dissipation solutions are needed to drop the operating junction temperature of LED packages. In addition, one measurement method of LED junction temperature is presented. Its application result shows it is effective to use pulse current to obtain LED junction temperature.

In the module level, thermal transient measurement of LED array module is used to illustrate the reliability study of LED module. It is found that, in order to get accurate thermal resistance of every kind of material in the heat flow path, we should analyze the curves of cumulative and differential structure function simultaneously.

The reliability study of multichip LED module is also presented. The reliability of multichip LED module with VCPCB coupled with sunflower heat sink was investigated. Simulation results indicate multichip LED module with VCPCB coupled with sunflower heat sink has better reliability. The case of Thermal design of multichip LED module with ceramic substrate concerns the substrate material selection. Both simulation and experimental results show that the module with AlN-based substrate exhibits better thermal performances than modules with Al and Al_2O_3 based substrates.

Several methods for studying the reliability of LED system are overviewed. And one of the methods is concerned about thermal distribution of a commercial 8 W LED lamp. The simulation and experiment results indicate that critical parts can be determined with thermal simulation tools when designing higher power LED lamps and solutions for thermal problems explored.

Acknowledgments The authors acknowledge the support of the National Science and Technology Support Program (grant no. 2011BAE01B14) and the Education Department of Guangxi Province for their financial support (Major Project, grant no. 201101ZD007). The research work was also supported by Guangxi Key Laboratory of Manufacturing System & Advanced Manufacturing Technology Grant No. GuiKeNeng09-007-05_001 and No. GuiKeNeng 11-031-12_001). The authors express thanks to Zaifu Cui, Hongyu Tang, Wanchun Tian, Ming Gong, Lili Liang, Fengze Hou and Lei Liu for their contributions.

References

1. Weng C-J (2009) Advanced thermal enhancement and management of LED packages. Int Commun Heat Mass Transfer 36:245–248
2. Kirkpatrick DA (2004) Is solid-state the future of lighting? third international conference on solid state lighting. Proc SPIE 5187:10–21
3. Chen Zhaohui, Zhang Qin, Wang Kai et al (2011) Reliability test and failure analysis of high power LED packages. 32(1):014007
4. Sheng Liu, Xiaobing Luo (2010) LED packaging for lighting applications: design, manufacturing and testing. Wiley, New York
5. Li XP, Chen L, Chen M (2011) An approach of LED lamp system lifetime prediction[J]. ICQR 6031691:110–114
6. Jifi Jakovenko, Robert Werkhoven, Jan Formanek et al (2011) Thermal simulation and validation of 8W LED Lamp[J], ESIME. 5765818:1/4-4/4
7. Xi Y, Gessmann T et al (2005) Junction temperature in ultraviolet light-emitting diodes. Jpn J Appl Phys 44(10):7260–7266
8. Jeung WK, Shin SK, Hong SY et al (2007) Silicon-based, multi-chip LED package [C]. Proceedings of electronic components and technology conference, Sparks, NV, USA, pp 722–727.
9. Li X, Chen X, Lu GQ (2010) Reliability of high-power light emitting diode attached with different thermal interface materials [J]. J Electron Packag 132:031011.1–031011.5
10. Lei Liu, Daoguo Yang GQ Zhang et al (2011) Thermal performance analysis of photoelectric parameters on high-power LEDs packaging modules[C]. IEEE thermal, mechanical and multiphysics simulation and experiments in micro/nano-electronics and microsystems.
11. Park SH, Kim KH, Ryu YC et al (2010) The analysis of failure rate and reliability test for LED based general lighting[C]. Proc 17th Physical and failure analysis of integrated circuits (IPFA), Singapore,July. 2010:1–2
12. Tongchang Zheng, Bingqian Li, Zhenghao Xia (2011) Monte-Carlo simulation of lifetime distribution on ar ray interconnec tion of LED module. J Optoelectronics Laser. 2(22):207–210
13. Fengze Hou, Daoguo Yang, Zhang GQ (2011) Thermal transient analysis of LED array system with in-LINE Pin Fin heat sink[C].Proc 12th EuroSimE, Linz, 1/5-5/5
14. Lan Kim, Jong Hwa Choi, Sun Ho Jang, Moo Whan Shin (2007) Thermal analysis of LED array system with heat pipe. Thermochimica Acta. 455:21–25
15. Wen Huai-jiang,Mou Tong-sheng (2010) The measurement of LED junction temperature and thermal capacity using pulse current. Opto-Electronic Eng. 37(7):53–59

16. Hou FZ, Yang DG, Zhang GQ et al (2011) Research on heat dissipation of high heat flux multi-chip GaN-based white LED lamp [C]. 12th international conference on electronic packaging technology and high density packaging, Shanghai, China, 8:1101–1105
17. Yin LQ, Yang WQ, Zhang JH et al (2010) Thermal design and analysis of multi-chip LED module with ceramic substrate [J]. Solid-State Electron. 54(12):1520–1524.
18. van Driel WD, Yuan CA et al (2011) LED system reliability [C]. Proc 12th EuroSimE, Linz, 1/5-5/5
19. Ming-Tzer Lin, Chao-chi Chang et al (2009) Heat dissipation performance for the application of light emitting diode, design, test, integration & packaging of MEMS/MOEMS, 2009. MEMS/MOEMS'09. Symposium on, Rome, April, pp 145–149.
20. Electronic Industries Association (EIA), Integrated Circuits Thermal Measurement Method – Electric Test Method (Single Semiconductor Device) [S], EIA/JESD51-1, 1995-01-01.
21. Wei XJ, Sikka K (2006) Modeling of vapor chamber as heat spreading devices [C]. Proceedings of thermomechanical phenomena in electronic systems conference, San Diego, CA, May, pp 578–585
22. Zhang GQ, van Driel WD, Fan XJ (2006) Mechanics of microelectronics. Springer, Dordrecht, pp 65–76
23. Tan LX, Li J, Wang K (2009) Effects of defects on the thermal and optical performance of high brightness light-emitting diodes. IEEE Trans Electron Packag Manuf 32(4):233–240
24. Koh S, van Driel WD et al (2011) Solid state lighting system reliability [C]. ChinaSSL. China, 121–126.
25. Kohl S, Willem Van Driel, Zhang GQ (2011) Degradation of epoxy lens materials in LED systems [C]. ESIME. 5765850:1/5–5/5.
26. Tarashioon S, Baiano A, van Zeij H et al (2011) An approach to design for reliability in solid state lighting systems at high temperatures[C]. Microelectron Reliab. 06.029:1–11.

Chapter 18
Hierarchical Reliability Assessment Models for Novel LED-Based Recessed Down Lighting Systems

Bongtae Han, Bong-Min Song, and Mehmet Arik

Abstract This chapter describes development of hierarchical reliability assessment models for novel LED-based lighting systems. Much of the chapter is excerpted from references (Arik et al., IEEE Trans Compon Packag Tech 33:668–679, 2010; Song et al., IEEE Trans Compon Packag Tech 33:728–737, 2010; Song et al., Microelectron Reliab 2011) and technical details omitted in the chapter can be found in the references. After a brief introduction about the motivation of LED-based recessed down lighting systems, Sect. 18.2 is devoted to luminaire subcomponent development and the challenges to realize a high-lumen luminaire at an affordable cost. In Sect. 18.3, a hierarchical reliability prediction model to assess the lifetime of LED-based lighting systems is first described, and the model is subsequently implemented for the LED-based recessed down lighting system cooled by synthetic jets.

18.1 Introduction

The US Department of Energy (DOE) estimates that lighting accounts for 22% of the total primary energy consumption annually [1, 2], and represents an annual cost of $152 billion. About half of the energy consumption for lighting can be attributed

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to the use of inefficient incandescent lamps. Consequently, there have been recent trends and legislation to replace incandescent lamps with halogen and compact fluorescent lamps (CFLs). While linear fluorescent lamps (LFLs) and CFLs can have very high efficacies [2], they are very mature technologies that offer limited scope for further improvement.

On the other hand, recent advances in development of light emitting diodes (LEDs) strongly suggest that they potentially offer significantly higher efficacies compared to LFLs and CFLs. Interestingly, LEDs were not initially considered for general illumination because efficient blue LEDs were not developed at that time. Instead, they were mostly used as red, yellow, and green color indicator lights based on AlInGaP semiconductor technology. A major advance in the use of LEDs for lighting was the development of "ultra-bright," low power blue LEDs (based on the InGaN semiconductor system) by Nichia. Subsequently, higher power blue, green, and violet LEDs were developed and have enabled semiconductor-based light sources. The first commercial high-power LED was developed by Lumileds Lighting [3], where AlGaInP was used to produce red and yellow light and AlGaInN to produce blue and green light. While high power and high efficacy are clearly crucial to the market penetration of LEDs for lighting purposes, color quality is an equally important aspect. Color quality is represented by two key metrics-the correlated color temperature (CCT) and the color-rendering index (CRI). For a given spectral power distribution, the CCT is defined as the temperature of an equivalent blackbody light source. As a reference, sunlight has a CCT ranging from 5,000 to 6,500 K, while incandescent and halogen lamps have CCTs ranging from 2,500 to 3,200 K.

The CRI is a metric that defines how colors appear under a specific light source with blackbody light sources defined to have CRI of 100. Typical LFLs and CFLs have a CRI of about 82.

Today, the efficacies for blue LEDs + phosphor systems can be more than 120 lm/W for 1 W devices and are therefore significantly better than LFLs and CFLs. However, these LEDs have very high CCTs (>5,000 K) and low CRIs of ~75, producing an unappealing "cold" bluish light. Therefore, these LEDs are unlikely to replace low CCT, high-CRI incandescent or halogen lamps. Recent advances in phosphor and LED system technology have led to warmer white light (2,600–3,500 K) that now approach and surpass CFL efficacies. One example of a warm white, high CRI, LED package is the GE Lumination Vio [1] that demonstrates the benefits of solid state lighting (SSL): long life, robustness, and energy savings with exceptional light quality. This effort to make the efficacy of LED lighting competitive with traditional light sources has required advances in LED chip efficiency, polymeric and silicone encapsulants, phosphors, thermal management, and power electronics. Along with power, efficacy, and color quality requirements, cost is a major consideration in general LED lighting (typically >700 lm) due to the high-base cost of LEDs.

One mitigating solution would be to drive LEDs at the highest current possible while retaining high efficacy and long lifetime. However, high-LED drive currents results in a phenomenon known as "droop," which reduces the extrinsic quantum efficiency and results in lower efficacy at high-drive currents. Although recent

progress in device design has helped to attenuate this issue [4], controlling the otherwise high-junction temperature associated with high-driving currents is critical in ensuring high-LED efficiency and lifetime. It is important to note that lumen output data cited by many LED manufacturers are based on LED junction temperature (T_j) of 25 °C (see [5] and [6]), which differs from the actual operation temperature in fixtures and lamps.

In general, T_j is always higher at steady state when operated under constant current in a fixture. Even in a well-designed fixture with adequate heat sinking, the LED light output can be reduced by 10–15% compared to the indicated "typical luminous flux" rating of the LED package. In addition, direct incandescent or CFL replacement bulbs using LEDs will require careful thermal design since typical sockets do not provide an adequate thermal path. These two aspects point to the important role that thermal management will play in the adoption and widespread use of an efficient LED-based lighting. Reference [7] notes that a major milestone in the packaging of high-power LEDs was the reduction of thermal resistance from 300 K/W to less than 15 K/W. Currently, high-brightness LEDs have a thermal resistance on the order of 5 K/W.

While much of this chapter focuses on LED packages and their thermal management, it is important to note that the entire lighting system must be optimized to minimize energy consumption. White light can be created by LEDs in several ways as indicated in ref. [8]. For the luminaire considered in this chapter, white light from blue chips with an appropriate phosphor is used to achieve warm light of around 3,000 K.

18.1.1 Energy Efficiency and Environmental Impact

While the efficacy of white light LED systems can surpass the efficacy of traditional lighting sources, there are still expectations for significant improvements in efficacy. The US DOE has defined a long-term efficacy goal of 160 lm/W for warm white LED systems over the next decade [2]. If this efficacy goal is reached along with a reduction in the initial cost of LED-based lighting systems, the energy and economic benefits from the development of LED-based lighting will be enormous. For example, a 100% incandescent replacement would reduce the total primary energy consumption in the USA by ∼10%, leading to a reduction in the national energy bill of approximately $65 billion and a reduction in the total carbon emission of 45 million metric tons. Even achieving intermediate DOE goals will lead to significant energy savings and reductions in carbon emissions. While this estimate is for incandescent lamp replacements, high-efficiency SSL will eventually also give significant energy savings vs. CFLs, especially when considering that optical losses in CFL fixtures can be more than 50%.

The development of a 100 W replacement lamp with LED technology enabled by novel thermal management, LED packaging, and driver electronics is presented. Subsequently, reliability assessment about the lamp is discussed.

18.2 Development of Led-Based Recessed Down Light

This section discusses the luminaire subcomponent development and the challenges to realize a high-lumen luminaire at an affordable cost.

18.2.1 Thermal Management

LED chips and driver electronics performances are highly temperature dependent. An LED lumen output degradation of as much as 16% can be observed when LED junction temperature is 100 °C compared to 40 °C. Therefore, thermal design is critical for optimal performance and reliability of the LED-based luminaire s. Passive cooling with conventional aluminum heat sinks and active cooling by thermoelectric or synthetic jets have been proposed by several groups [8].

It is also well known that high-LED junction temperature can result in LED degradation. The development and widespread use of high-brightness LEDs and the application to the lighting industry require the development of advanced heat management systems to ensure the integrity of the LEDs and the electronics that drive them. Although the technology and efficacy are steadily improving, there is still a need for advanced cooling in confined space, as in typical lighting applications. This issue is further compounded by use of higher drive currents that increase the heat output. Thermal management and distribution is critical to the reliability and functionality of the LEDs; it was reported that hotspots and attachment defects have a severe effect on the LED chip life [5] and lead to problems such as LED degradation, wavelength shift, loss of radiant flux and increase of forward voltage.

The primary means for heat removal from an LED is through conduction while in conventional incandescent light bulbs, radiation into the room removes a significant portion of the heat generated. While most of the power in incandescent light is radiated into the illuminated room at infrared wavelengths, a large portion of the input power in LEDs is dissipated into the LED circuit board through heat conduction (and later convection) [9] (refer to Table 18.1 and Fig. 18.1).

Elevated system temperature is not a concern in incandescent systems. On the contrary, LEDs are semiconductors and the LED chip temperature should not exceed a certain value in order to maintain their durability and luminous efficacy. Thus, there is a need for technologies that reduce LED count, with each LED operating at high-drive currents, and still restrain the chip temperatures below 110 °C through thermal management strategies. The need to remove heat through conduction has driven the development of materials with high-thermal conductivity as well as similar coefficients of thermal expansion to match that of the LEDs and electronics [11]. Progressing from package on board technology to chip on board technology offers clear benefits in output and reduces the thermal resistance to the heat sink; however, the material of the circuit board and its thermal conductivity

Table 18.1 Power conversion for white light sources [10]

	Incandescent (% power)	LED (% power)
Visible light	8	20
Infrared	73	0
Heat	19	80
Total	100	100

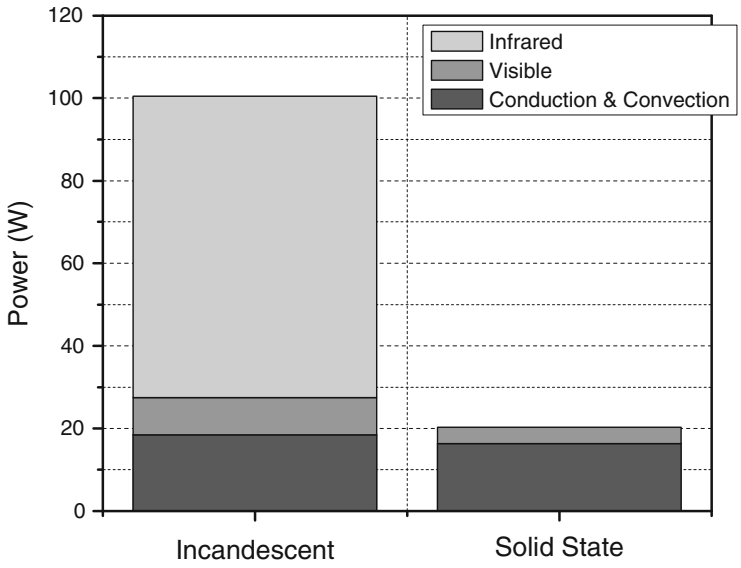


Fig. 18.1 Distribution of input power for 1,000 lumen incandescent and LED lighting system

play a critical role in the thermal management solution. Additionally, the most expensive component in SSL is the LED chip itself. Therefore, as a means of reducing the cost, technologies that can enable a substantial reduction in the LED count are in quest. Naturally, the use of fewer LEDs implies the necessity of a proportional increase in the power input per LED while maintaining reliability. Besides the efficacy, the power conversion/distribution of the input heat between incandescent and LED lighting is radically different.

Passive cooling systems account for the majority of the LED luminaire cooling solutions. However, in high-lumen applications their use may be limited by size and weight constraints. Liu et al. proposed and tested a closed microjet array to maintain a low junction temperature [12]. During this study, conventional heat management methods were evaluated such as natural convection, a heat sink and a heat pipe. The results were compared to the performance of the microjet array cooling and it was reported that the microjet array cooling provided superior performance (i.e., lower junction temperature). Yet, issues pertaining to cost and reliability need to be addressed.

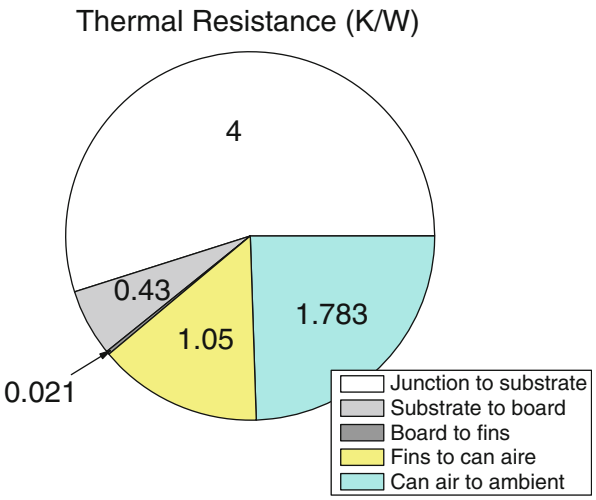


Fig. 18.2 Thermal resistance breakdown for a lamp from a single die to the ambient

A 1,500 lm, 21 W, 6 in downlight was analyzed using computational models, as a baseline design, to understand the thermal resistance breakdown from the substrate to the ambient/attic air, and subsequently highlight trends for varying lamp power, can size, and LED count. As seen from Fig. 18.2, the thermal resistance chain from a single LED chip to the ambient air is dominated by the conduction resistance between the single chip and the board, and the convection heat transfer between the lamp surface and the enclosed air inside the housing. Naturally, using more LEDs creates multiple parallel conduction paths for the same heat between the chip and the board, and tends to reduce the "effective thermal resistance" from the chip to the system.

The resistance values estimated from thermal models were employed to determine the entitlements of passive cooling for a 1,500 lm lamp under varying lamp can sizes and LED count. A 12 LED light engine is considered on the basis of a 50–60% reduction in the LED count for 1,500 lm output. Figure 18.3 depicts that a can size of 10 in is required to realize a purely passive cooling solution for a 1,500 lm lamp using 12 LEDs. The reduction of resistance due to venting holes along the map trim was evaluated using the computational models. Note that some commercial downlight luminaires use 12 LEDs for 660 lm output. At the same drive current levels per chip, a 1,500 lm (20 W) passively cooled lamp would need to use ~27 LED chips. Thus, Fig. 18.3 highlights the fact that the lamp volume would need to be increased by 2.4 times to yield more than 50% reduction in the LED chip count (12 instead of 27), without any advanced thermal management strategy. Note that the heat transfer "goal" is based on the need to remove 20 W of heat under a worst-case attic temperature of 60 °C, without letting the LEDs heat above 100 °C.

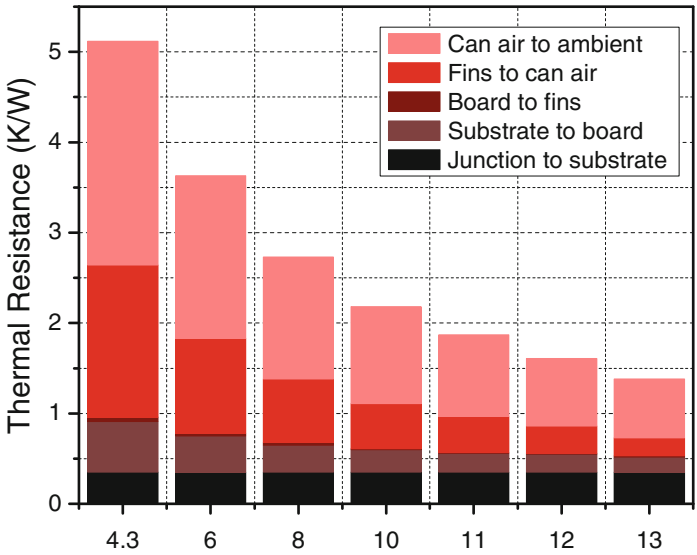


Fig. 18.3 Thermal resistance trend with increasing can size for a 1,500 lm lamp using 12 LEDs

Table 18.2 LED count versus can size required by a purely passive cooling solution for a 1,500 lm lamp

LED count	Can size [in.]
4 (85% reduction)	17
6 (77% reduction)	13
12 (50% reduction)	10

Table 18.2 extends the results from Fig. 18.3 to estimate the can size that would be required to realize a passively cooled 1,500 lm lamp at various LED counts. Clearly, without any advanced thermal management, the only way of obtaining a reduction in the LED count is by increasing the can size, which is an unattractive and unacceptable trend for the lamp design.

18.2.2 Experimental Investigation

Experimental testing was performed on a surrogate 6 in downlight in a simulated ceiling environment. The test setup comprises a 6 in downlight can, wrapped around with 1.5 in thick insulation, and elevated 5 ft above the ground level by using a tripod. A heat sink integrated with an air mover is used for thermal management. Thermocouples are instrumented at various key locations to measure the temperatures at relevant points along the thermal chain. The base of the heat sink is artificially heated using a Kapton based heater. The heat sink is attached to

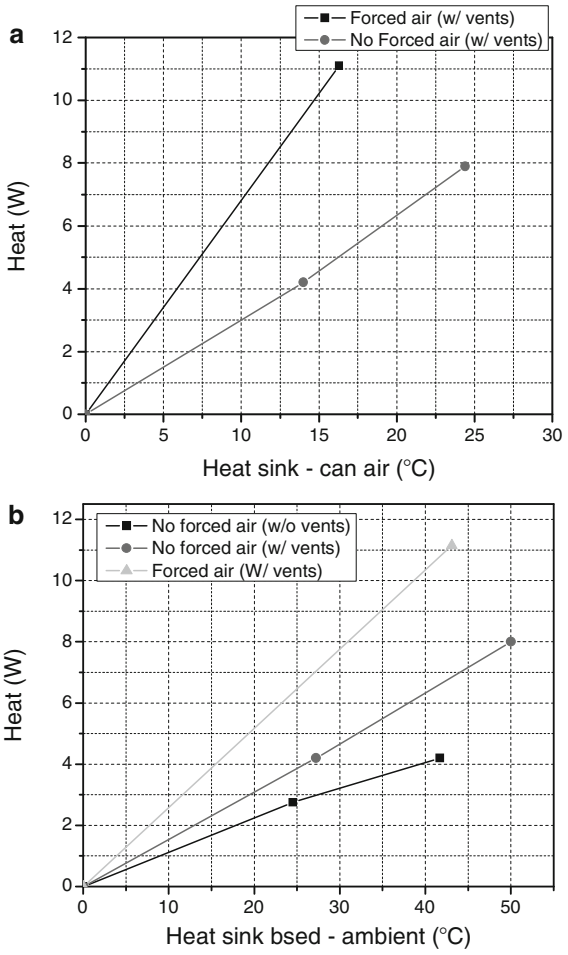


Fig. 18.4 (**a**) Heat sink base to ambient temperature drop for various scenarios. (**b**) Heat sink base to can air temperature drop for different scenarios

an insulated circular plate ($k < 0.2$ W/m·K) having the same area at the 6 in can cross section. Experiments are performed in a complete air blockage condition (no air exchange between the can and ambient) and by drilling circular vents on the plastic board near the circumferential region.

Experiments were run at different heating loads under varying conditions of venting and forced air circulation and the results are summarized in Fig. 18.4. The heat sink base undergoes a rise of 40 °C above ambient even with forced cooling, at 11 W of heat. Although venting and forced convection cause an increase in the cooling level, it is not adequate enough to meet the 21 W heat removal requirement. The temperature rise of the heat sink base above ambient at 11 W is 41 °C, while that between the fins and can air is 16 °C. This suggests that for 11 W the can air is 25 °C warmer than the ambient air. The air circulation in the can fails to create any net air exchange with the room ambient air. This causes the warm air inside the can to stagnate. The lack of air replenishment

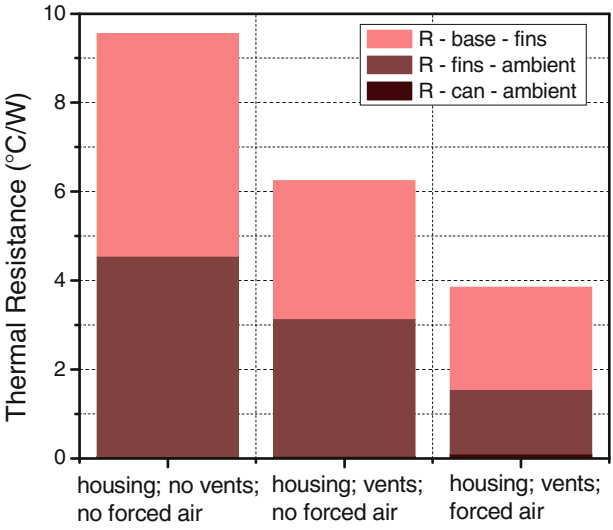


Fig. 18.5 Thermal resistance stack up for various cooling scenarios

adds a substantial limitation to the thermal resistance (Fig. 18.4). The end result is that little heat is transferred from the can to the attic environment through the insulation and virtually none into the illuminated room.

Noting that the attic temperature under worst conditions can reach 60–70 °C, it is preferable for the thermal management system to "dump" all the heat to the room instead of the attic. The strong need for a thermal management strategy that can exchange mass and heat with the room air motivated the linear heat sink described in the following section. Figure 18.5 summarizes various scenarios with the use of a radial heat sink solution.

18.2.3 Active Cooling with Synthetic Jets

Synthetic jets are zero net mass flow devices that comprise a cavity or volume of air enclosed by a flexible structure and a small orifice through which air is forced as illustrated in Fig. 18.6. The structure is induced to deform in a periodic manner causing a corresponding suction and expulsion of the air through the orifice [13]. They have also been shown to be effective for heat transfer applications by improving local convection cooling. The synthetic jet imparts a net positive momentum to its external fluid. During each cycle, this momentum is manifested as a self-convecting dipole that emanates away from the orifice. The vortex dipole then impinges on the surface to be cooled, such as an LED circuit board assembly, disturbing the boundary layer and convecting the heat away from its source. Over steady-state conditions, this impingement mechanism develops circulation patterns

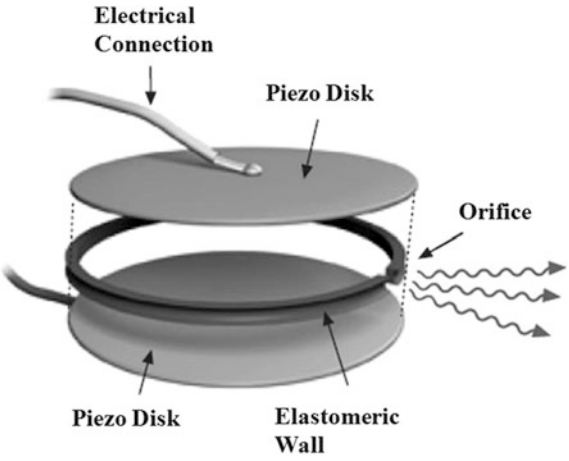


Fig. 18.6 Schematic of a typical GE synthetic jet

near the heated component and facilitates mixing between the hot air and ambient fluid. The cooling enhancement, EF, provided by the synthetic jet, is defined as the ratio of the heat dissipated at constant temperature with the active cooling from the synthetic jet, Q_{sj}, to the heat dissipated from natural convection alone, Q_{nc}

$$\mathrm{EF} = \frac{Q_{sj}}{Q_{nc}} \tag{18.1}$$

Synthetic jets designed with piezoelectric disks and a silicone o-ring have demonstrated cooling enhancements (EF) of at least 10 with low-cost components and a simple design. While such cooling enhancement performance from a simple, low cost device are impressive, it is important to note that the synthetic jet operating condition must be chosen to be practical within the limits of light applications. For example, large deflections are possible by driving the disks at resonance. In practice, lighting applications require high levels of reliability that are better achieved at low-stress conditions, limiting the out-of-plane deflection. Also, at high amplitudes and high frequencies, the synthetic jet makes a tonal noise with substantial harmonics due to the asymmetric pressure wave-form at the orifice exit. Many lighting applications are intolerant to excessive noise. Therefore, the operating conditions of the synthetic jet are chosen to be at low-voltage amplitude and low-frequency such that human sensitivity to the noise is substantially reduced. Although electromagnetic actuators have been used for low-frequency synthetic jets, the power consumption is also much higher compared to piezoelectric disks, reducing overall system efficacy.

A GE synthetic jet comprises a pair of piezoelectric disks that are energized out of phase at high frequency to change the volume of the cavity between the disks and force air out through the orifice (see Fig. 18.6). Further information about these synthetic jets has been presented in refs. [13–15].

18.2.4 Light Engine Development

Several design goals for the luminaire were established. In addition, some optional features were considered. The light engine design goals are an Edison base, 6 in compatible can downlight, LED replacement bulb producing 1,500 face lumens at 75 lm/W, CRI > 80, CCT = 2,700–3,200 K, 50,000 h (70% output) lifetime at a 100 °C LED junction temperature. Optional design goals included color sensing and feedback and a minimum of 50° FWHM beam angle control. The initial light engine design investigated blue chips at 470 nm die with a phosphor and considered additional red die for enhanced CRI.

Several LED manufacturers were surveyed for their LED performance. The desired format for the LED is bare die. This will allow for the smallest light engine, reduced optic size for beam control, reduced thermal impedance and the easiest interchangeability amongst 1 mm^2 power LED die manufacturers.

The blue die utilizes a yellow phosphor for the cool white conversion. Red lumen output will be adjusted to attain the warm white 2,700–3,200 K color temperature. Initial calculations show that to hit the color temperature targets a 5.6–1 white to red contribution is needed. Based on this and a derating temperature of 100 °C, the number of die needed for the revision one design is 12 blue driven at 500 mA and six reds driven at 350 mA to achieve the 1,500 lm target.

Optical design efforts involved calculations to size the light engine and optics to fit within the luminaire while delivering the proper beam uniformity and angle. Several designs were evaluated utilizing optical modeling to determine the optical efficiency and optical output (shape, uniformity) of the luminaire. Initial designs were aimed at utilizing a small densely packed chip on board light engine within an optical mixing cavity and remote optics to provide beam angle control. However, due to space restraints, mainly the depth of the optical cavity, in the luminaire, a favorable optical efficiency and beam control could not be met. The best profile and efficiency assumes an 87% reflectivity for the reflector, and an uncoated polycarbonate lens, 73.2% of the source light is delivered into a beam of about 34° FWHM [16].

An alternate approach was investigated which tiles commercially available high-brightness LED warm white packages with commercially available optics to provide an overlapping beam with approximately 50° beam angle control. This design unfortunately does not allow the use of red LEDs as there is no optical mixing cavity but provides a much larger light engine and thus aids in thermal spreading. The elimination of the reds required increasing the number of LEDs to 19 to meet the lumen target of 1,500 lm, the CRI and CCT were met by choosing the appropriate LED binning [16]. Initial prototypes were assembled for evaluation and comparison. Photos and optical results are shown below in Fig. 18.7.

Table 18.3 presents the initial optical results from the luminaire developed to meet 1,500 lm. The color temperature and CRI were also within the specified values. The efficiency for the steady-state 80 °C board temperature condition was 51 lm/W. Figure 18.8 presents the various losses in the optical design of the luminaire.

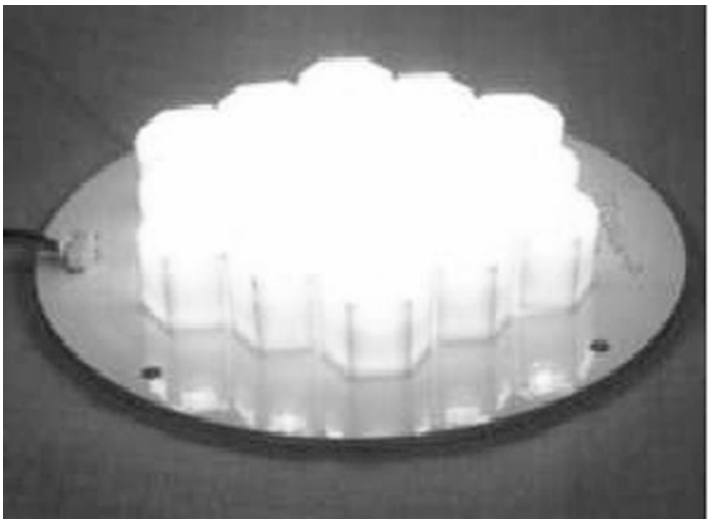


Fig. 18.7 Light engine prototype

Table 18.3 Summary of test condition

Test condition	Board temperature	Total lumens	CCT	CRI
500 mA @ 59 V	80 °C	1,750	2,930	86.3

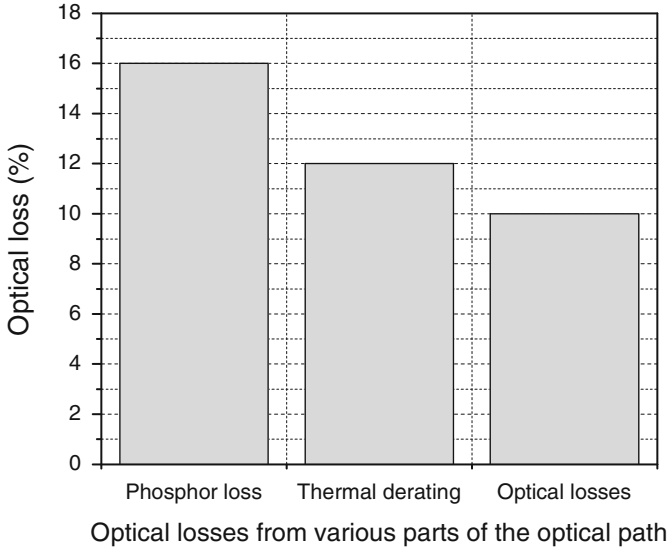


Fig. 18.8 Optical losses from different sections of the optical path

While the published data shows high-chip level efficacies, system level efficiencies degrade due to several effects such as thermal management, optical losses, and chip-to-chip quality variation. In this development, we have observed all three of those causing lower efficacies than predicted.

18.2.5 Driver Electronics

The development of driver electronics for the high efficiency, high-lumen (1,500 lm) LED luminaire with synthetic jet cooling is critical to system performance. Before delving into the implementation details, we enumerate some of the salient design constraints. First, the driver electronics clearly needs to be low-cost to encourage market penetration of high lumen LED luminaire. Second, high efficiency ($> 90\%$) is very important in order to achieve high-luminaire efficacy. Third, power electronics is required to fit in a volume occupied by circular substrate of a 10 cm diameter and a height of 2.54 cm. Fourth, the power to be supplied by the driver electronics to the LEDs is based on the discussion in the preceding section on light engines. Specifically, 19 white LEDs from CREE, Inc. [17], chosen by virtue of their lumen efficiency (5 mW/lm), are used to achieve adequate lumen output. The voltage drop of 3.6-V/LED, in part, dictates the detailed design and configuration of various components in the electronics. The power supply to the synthetic jets is based on 0.5 W/jet consumption.

A fly-back converter topology was chosen to provide galvanic isolation between the input ac voltage of 120-V rms at 60 Hz and the output voltages. The advantages of using a flyback converter are that it is well understood and has been widely used in traditional lighting applications; consequently, it is expected to be cost effective. The fly-back topology provides isolation and also allows adjustment of voltage conversion ratio through the turns ratio of the constituent transformer. The switching frequency of the circuit was chosen to be 140 kHz.

The circuit consists of an EMI filter, a rectifier to rectify the ac input voltage. The fly-back transformer converts an input voltage (with peak value V_i) to dc voltages V_o for the LEDs and V_{cc} for auxiliary electronics that power "house-keeping" circuits and also the power electronics for the synthetic jets. The switch Q_1 operates at the switching frequency of interest f_{sw}. One important consideration in the design of this converter was the ability to maintain a high-power factor during operation. A fly-back converter operated in discontinuous mode of operation achieves a natural power factor of 1 (see [18, 19]), which was one of the design requirements.

A rated input voltage 120-V was measured to provide an output voltage of 60.7-V dc. The input rms current was measured to be 291 mA. The output dc current was measured to be 488 mA. It is also apparent that the input current and voltage are sinusoidal and in-phase with each other—the result of operating in discontinuous conduction mode. No control electronics were implemented to achieve this power factor other than the converter operating in open-loop. The power factor was measured to be 0.96.

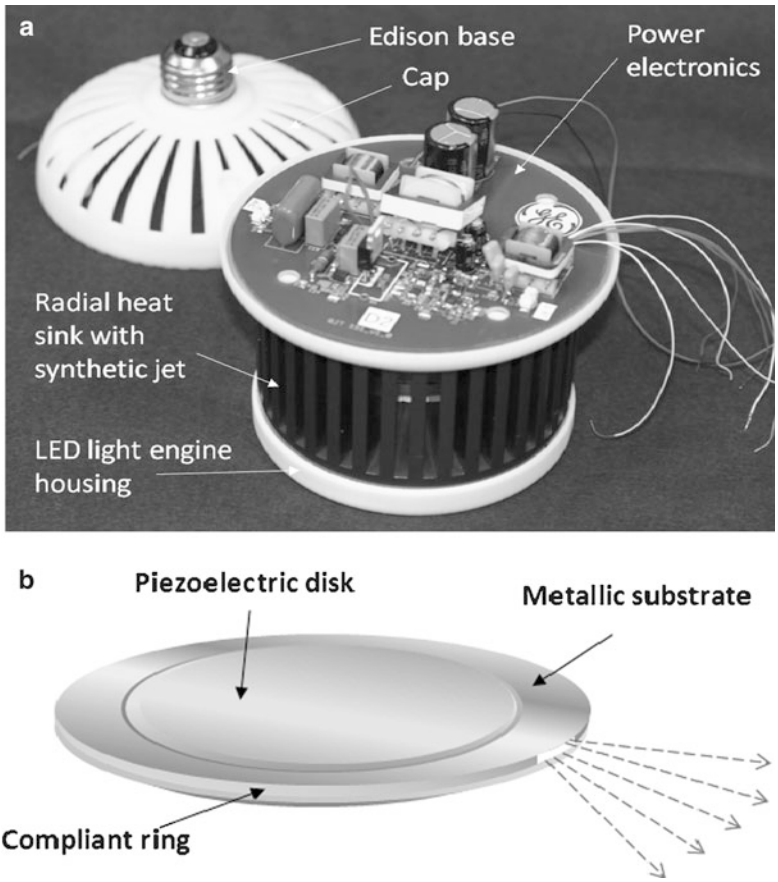


Fig. 18.9 (**a**) Photo of an LED-based luminaire cooled by synthetic jet [20] and (**b**) schematic of synthetic jet

18.3 Reliability Assessment

A hierarchical reliability prediction model is proposed to assess the lifetime of the proposed luminaire cooled by synthetic jets. In order to construct a lifetime prediction model of the luminaire, a Physics of Failure (PoF) model of each component is necessary. The concept of the hierarchical reliability model is described first and the life prediction using individual PoF models will be followed.

18.3.1 Hierarchical Life Prediction Model

The concept of a hierarchical model was first proposed in ref. [20]. A model refined to be specifically aimed for the luminaire described in Sect. 18.2 (Fig. 18.9) is presented in Fig. 18.10. The model is articulated on four levels: LED chip/package,

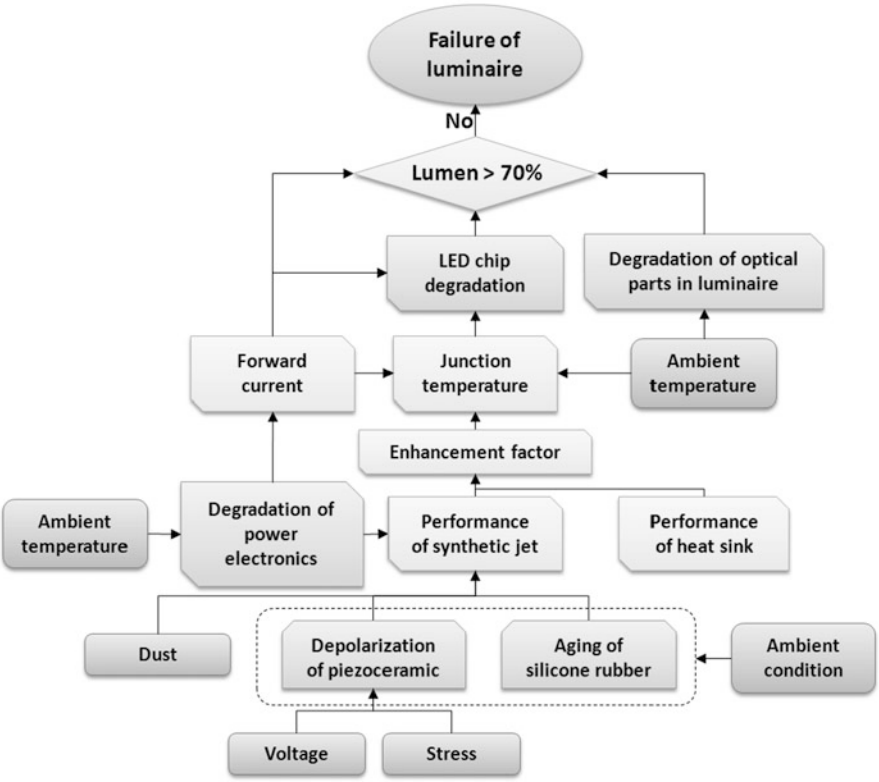


Fig. 18.10 Hierarchical life prediction model for LED-based luminaire cooled by synthetic jets

optical components in the fixture, synthetic jet with a heat sink, and power electronics. Figure 18.10 also shows all the sub-models and the associated loading conditions at each level.

The lifetime of the luminaire is determined by the lumen maintenance of LED and the reduction of the fixture efficiency, which can be expressed as [20]:

$$t_{\text{life}} = F(g_{\text{LED}}(t), F_{\text{fixture}}(t)) \tag{18.2}$$

where t_{life} = luminaire lifetime at lumen maintenance of 70%, g_{LED} = lumen maintenance of LED, and F_{fixture} = fixture efficiency.

The lumen maintenance of LED is the most critical sub-model, which has an empirical exponential form. The light output of LEDs, L_{LED}, can be expressed mathematically as:

$$L_{\text{LED}} = L_0 g_{\text{LED}}(t) = L_0 e^{-\alpha(T_j, I_f)t} \tag{18.3}$$

where α is the light output degradation rate that depends on the junction temperature (T_j) and the forward current (I_f) [21–23], t is the operation time measured in hours, and L_0 is the initial light output in lumen [24, 25].

The cooling performance of synthetic jets is expressed with an enhancement factor (EF) which is defined as the ratio of heat removed with an active cooling device (Q_{active}) to the heat removed through passive means only, largely through natural convection (Q_{nc}), at the same temperature (18.1). Considering the fact that the junction temperature increases as the ambient temperature and forward current increase, the dependence of the junction temperature on the aforementioned terms can be expressed as [20]:

$$T_j = T(T_a, R_{\text{cond}}, I_f, \text{EF}) \tag{18.4}$$

where $T_{\text{a}} =$ ambient temperature; $R_{\text{cond}} =$ internal conduction resistance of LED.

The power electronics drives the LED light engine and the synthetic jet. The degradation of power electronics is mainly caused by capacitance reduction of electrolytic capacitors. The reduced capacitance increases the ripple voltage, and thus the applied current to LED is reduced [26]. The decreased current affects the light output and junction temperature. As mentioned above, the decay constant is a function of forward current; as a result the decay constant decreases with the decreasing current.

The remaining sub-models of the proposed hierarchical model are physics-of-failure (PoF) models to describe the degradation mechanisms of the synthetic jet performance. The PoF models of the synthetic jet degradation can be separated into depolarization of the piezoceramic disk and aging of the compliant ring. The degradation mechanisms change the amplitude response of the synthetic jet, thereby reducing the EF at any given time.

18.3.2 Reliability Analysis of Synthetic Jet

The degradation of synthetic jet performance (i.e., the reduction in amplitude) increases the junction temperature of the luminaire, which is a dominant factor for the lifetime of the luminaire. After developing a model that can predict amplitude response, the time-dependent performance of the synthetic jet can be predicted by aging characteristics of each component in the synthetic jet. The performance change is then converted into the junction temperature change using the relationships between the amplitude of the synthetic jet and junction temperature.

18.3.2.1 Performance Characterization

The performance of the synthetic jet was tested by applying a harmonic voltage input at various frequencies. The center out-of-plane displacement amplitudes of the disk were measured by a laser doppler vibrometer [CLV-1000, Polytech].

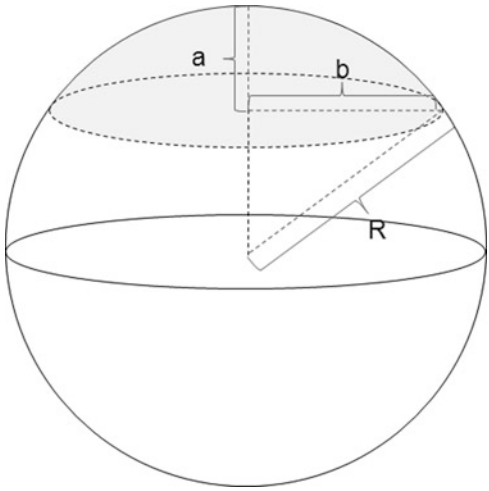


Fig. 18.11 Air volume in a synthetic jet (colored region), where a = amplitude of synthetic jet, b = radius of metal substrate and R = radius of a sphere

The junction temperature is directly related to the performance of the synthetic jet and the heat sink. The enhancement factor (EF) is proportional to the amount of air-flow rate, which is a function of the amplitude of the jet and the excitation frequency.

Assuming that the deflection of the disk can be modeled as a part of a perfect sphere, the air flow rate can be approximated as (Fig. 18.11):

$$\mathrm{AFR} = 4\pi\left\{\frac{(R-a)^3 - R^3}{3} + R^2 a\right\} \times f_{\mathrm{jet}} \tag{18.5}$$

where AFR = air flow rate; f_{jet} = operating frequency of synthetic jet; a = amplitude of synthetic jet; and b = radius of nickel coated substrate. Geometrical considerations require that, the radius of the sphere, R, be expressed as $R = \frac{a^2+b^2}{2a}$

A relationship between the EF and the air-flow rate is depicted in Fig. 18.12a, which was obtained by changing the amplitude of the disk (or by changing the amplitude of the excitation voltage) at a fixed excitation frequency. In order to determine the junction temperature for a given EF, an empirical relationship should be obtained for each synthetic jet and heat sink design. Figure 18.12b shows such a relationship, obtained from synthetic jets incorporated with a radial heat sink.

The enhancement factor decreases as the synthetic jet ages. The aging is caused by two degradation mechanisms: depolarization of the piezoceramic and change in the elastic modulus and damping ratio of the compliant ring. This can be expressed as:

$$\mathrm{EF} = \mathrm{EF}(P_{\mathrm{jet}}); \quad P_{\mathrm{jet}} = P_{\mathrm{jet}}(T_a, D_{\mathrm{pzt}}, E_{\mathrm{td}}, \zeta_{\mathrm{td}}, P_{\mathrm{ps}}) \tag{18.6}$$

where P_{jet} performance of jet; D_{pzf} = depolarization effect of piezoceramic; E_{td} = elastic modulus change of compliant ring; ζ_{td}= damping ratio change of compliant ring; and P_{ps} = performance of synthetic jet driving circuit.

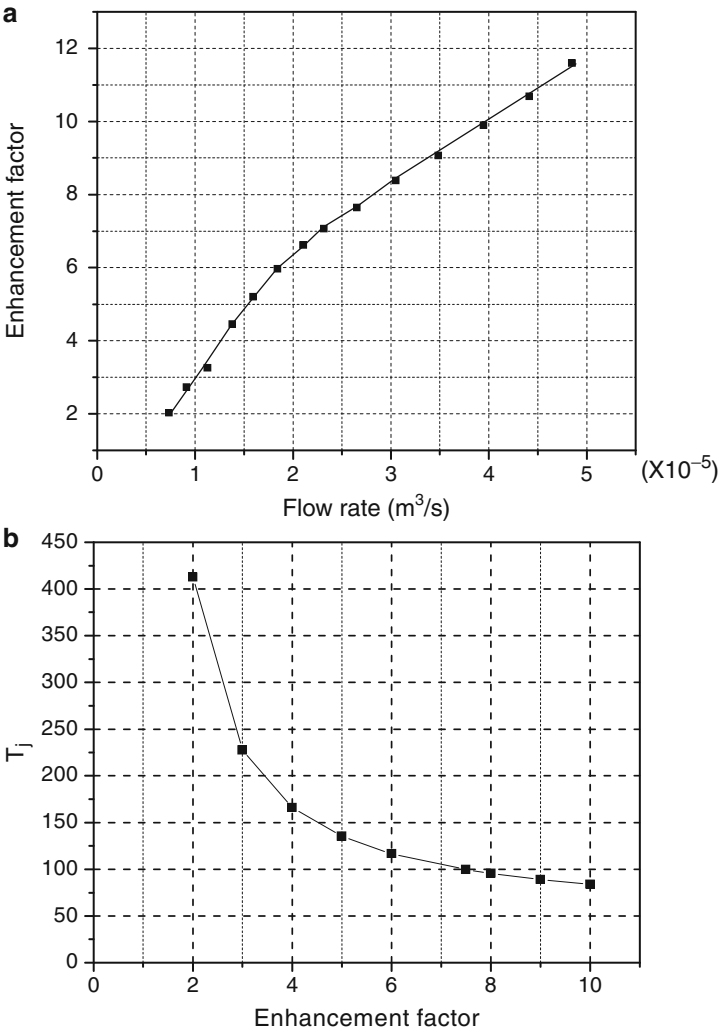


Fig. 18.12 (**a**) Air flow rate vs. enhancement factor (EF) and (**b**) EF vs. junction temperature

18.3.2.2 Hybrid Modeling

The amplitude reduction can be predicted using numerical modeling if the degradation rates of the piezoelectric disk and the compliant ring are known. A hybrid experimental/numerical model is developed to predict the amplitude reduction as a function of time by adopting the property degradation characteristic of each material used in the synthetic jet.

A commercial FEM package (ANSYS 12.1) was used to build an FEM model for a harmonic analysis using the quarter symmetry (Fig. 18.13a). In order to

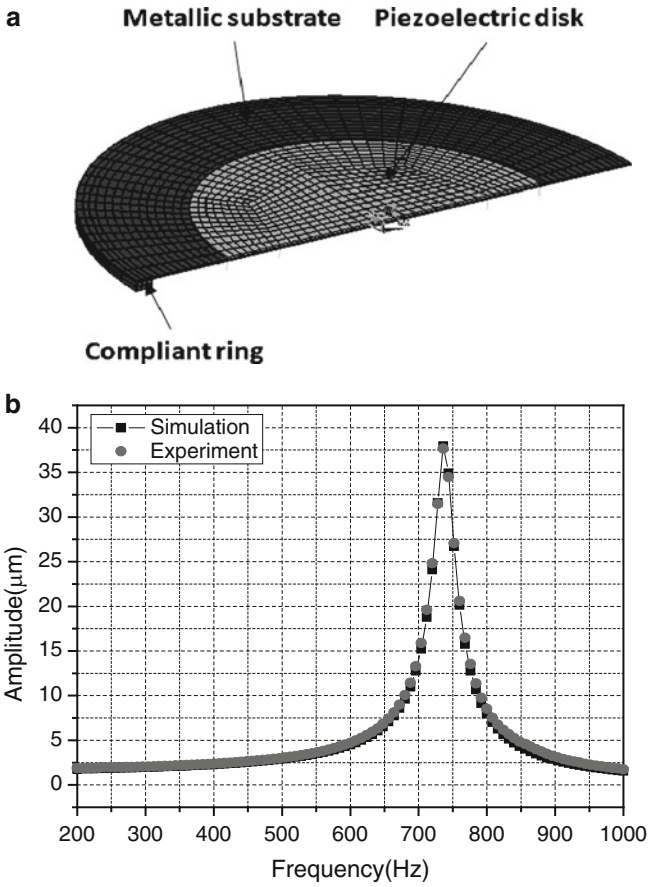


Fig. 18.13 (**a**) FEM model of a synthetic jet for harmonic analysis using the quarter symmetry and (**b**) experimental data obtained at vacuum is compared with simulation results considering only material damping

incorporate the material damping, Rayleigh damping was used [27], which can be expressed as:

$$\zeta_{\mathrm{mr}} = \frac{\alpha}{2\omega_R} + \frac{\beta\omega_R}{2} \tag{18.7}$$

where ζ_{mr} is the rth modal damping ratio, ω_R is the resonant frequency in rad/s, α is the mass damping multiplier, and β is the stiffness damping multiplier. Since α is zero for the current case of viscous damping [27], (18.7) can be rewritten as:

$$\beta = \frac{2\zeta_{\mathrm{mr}}}{\omega_R} \tag{18.8}$$

The damping ratio of each material in the synthetic jet was converted to β by using (18.8). Figure 18.13b shows the comparison between simulation and experimental result at vacuum condition. The simulation result is in good agreement with experimental results.

The ambient pressure at the operating condition is 1 atm and thus the effect of the air damping known as "squeeze film damping" [28] must be considered in the modeling. Squeeze film damping occurs when two surfaces separated by a thin viscous fluid film move symmetrically. This effect is illustrated in Fig. 18.14a, where the amplitude response of the synthetic jet at 1 atm and the vacuum are compared. As expected, the resonant frequency and the amplitudes were altered significantly with damping: the resonant frequency decreased and the amplitude at the resonant frequency also decreased.

The data of Fig. 18.14a was normalized and plotted again in Fig. 18.14b to distinguish the characteristics of amplitude distributions more clearly. The frequency and the amplitude were normalized by the resonant frequency of each case and the amplitude at the resonant frequency, respectively. It can be seen from Fig. 18.14b that the amplitudes at frequencies other than the resonant frequency tend to decrease more slowly with the air damping, especially at the frequencies higher than the resonant frequency ($f > f_R$). An advanced CFD model can be used to handle the squeeze film damping effect. In this study, a hybrid numerical/experimental scheme was developed since the reliability model only concerned the final amplitude.

The rationale for the hybrid approach can be explained by comparing the numerical prediction of synthetic jet with the experimental data. The goal of the approach is to force the numerical prediction to match the experimental data by effectively adjusting the original properties to account for the effect of squeeze film damping.

The jet is essentially a second order system subjected to a sinusoidal input. The resonant frequency of the second order system, ω_R, is expressed as [29]:

$$\omega_R = \omega_n \sqrt{1 - 2\zeta^2} = \sqrt{\frac{k}{m} - \frac{c^2}{2m^2}} \tag{18.9}$$

where m is the mass, c is the damping coefficient, k is the stiffness, ζ is the damping ratio ($\zeta = \frac{c}{2\sqrt{km}}$), and ω_n is the natural frequency ($\omega_n = \sqrt{\frac{k}{m}}$). For a given mass, the resonant frequency can be changed by adjusting the stiffness or the damping coefficient.

The amplitude of the second order system subjected to a harmonic excitation is expressed as [29]:

$$X = \frac{F_0}{k} \frac{1}{\sqrt{\left\{1 - \left(\frac{\omega}{\omega_n}\right)^2\right\}^2 + \left\{2\zeta\left(\frac{\omega}{\omega_n}\right)\right\}^2}} = \frac{F_0}{\sqrt{\{k - \omega^2 m\}^2 + \left\{\frac{\omega^2 c^4}{4mk}\right\}}} \tag{18.10}$$

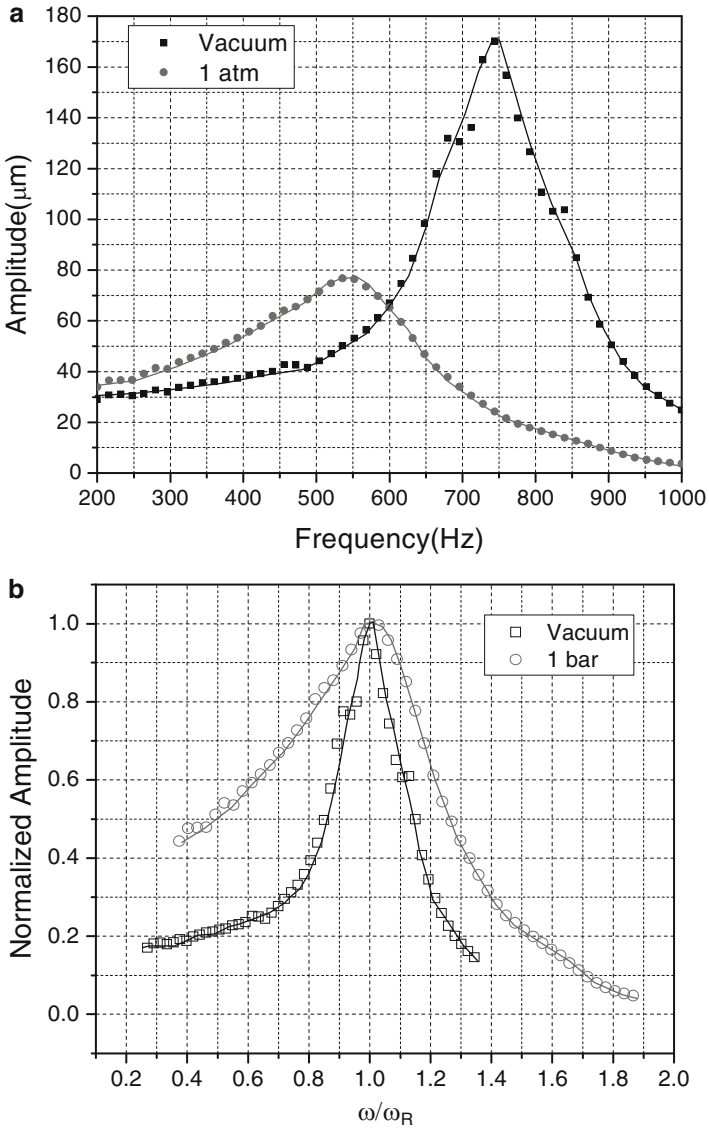


Fig. 18.14 Squeeze film damping effect in synthetic jet: (**a**) Comparison between with and without squeeze film damping effect and (**b**) normalized plot of (**a**) where the frequency is normalized by the resonant frequency and amplitude is normalized by the amplitude at the resonant frequency

where X is the amplitude at each frequency, F_0 and ω are the excitation force and frequency, respectively. Equation 18.10 implies that the most practical way of adjusting the amplitude is to manipulate the force. Then the amplitude normalized by the amplitude at the resonant frequency can be expressed as:

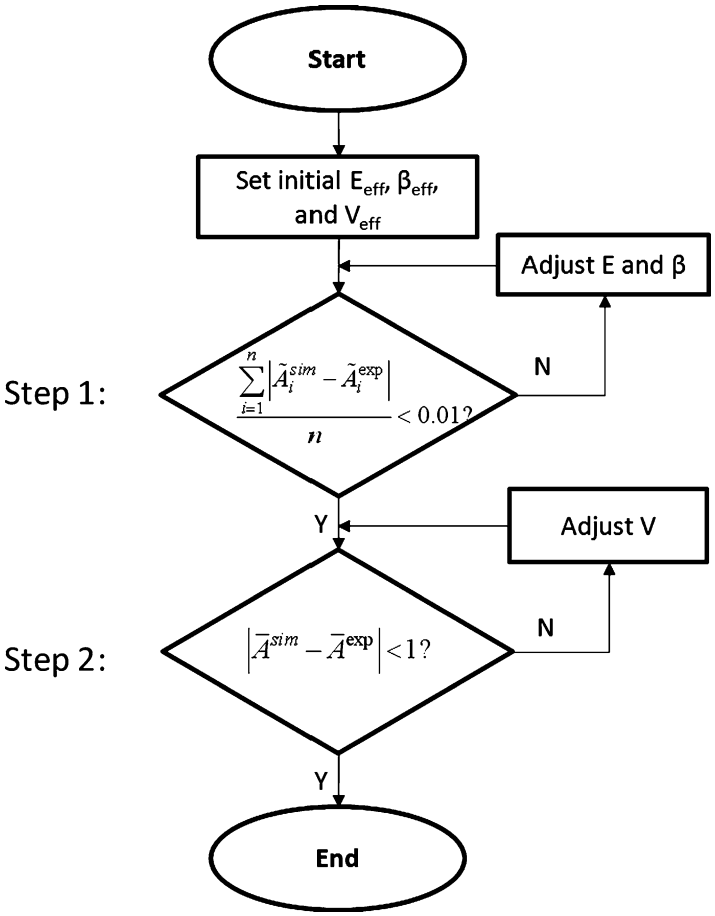


Fig. 18.15 Flow chart to determine effective properties for the hybrid model

$$\bar{X}=\frac{X}{X_R}=\sqrt{\frac{\left(\frac{kc^2}{m}\right)-\left(\frac{c^4}{4m^2}\right)}{\{k-\omega^2 m\}^2+\left\{\frac{\omega^2 c^4}{4mk}\right\}}} \tag{18.11}$$

For a given mass, the normalized amplitude can also be changed by adjusting the stiffness or the damping coefficient.

A sequential optimization procedure was developed for the hybrid approach. The flowchart is shown in Fig. 18.15 and the detailed description of each step is provided below.

- Step 1: Profile of normalized amplitude
  Since the elastic and damping properties of the piezoceramic disk/substrate assembly do not change with time, the effective modulus and the stiffness

damping multiplier of the assembly are used to modify the system stiffness and the damping. The effective properties of the piezoceramic disk/substrate assembly can be expressed as:

$$E_{\text{eff}} = \frac{E_{\text{sub}}V_{\text{sub}} + E_{\text{PZT}}V_{\text{PZT}}}{V_{\text{sub}} + V_{\text{PZT}}}$$
$$\beta_{\text{eff}} = \frac{\beta_{\text{sub}}V_{\text{sub}} + \beta_{\text{PZT}}V_{\text{PZT}}}{V_{\text{sub}} + V_{\text{PZT}}} \tag{18.12}$$

where E, β and V represent the modulus, the stiffness damping multiplier and the volume, respectively. The subscripts of "sub" and "PZT" denote the substrate and piezoelectric disk, respectively.

The objective of this step is to adjust the amplitude response. The amplitude data normalized by the maximum amplitude was used to determine an effective E-β combination by using an optimization routine. The objective function (R_1) can be expressed as:

$$R_1 = \frac{\sum_{i=1}^{n} \left|\tilde{A}_i^{\text{exp}} - \tilde{A}_i^{\text{sim}}\right|}{n} \tag{18.13}$$

where $\tilde{A}^{\text{exp}}$ and $\tilde{A}^{\text{sim}}$ are the amplitudes of experimental and simulation data normalized by each maximum, respectively; and n is the number of data points. The optimization routine adjusts the E-β combination until the objective function has the minimum value. Figure 18.16a shows the results obtained using the effective E-β set at an input voltage of 30 V.

- Step 2: Absolute amplitude
  The absolute amplitude level can be adjusted by changing the input voltage. The objective function (R_2) for the optimized V quantifies the degree of coincidence between the experimental and the simulated data. The metric can be expressed as:

$$R_2 = \left|\bar{A}_{\text{exp}} - \bar{A}_{\text{sim}}\right| \tag{18.14}$$

where $\bar{A}_{\text{exp}}$ and $\bar{A}_{\text{sim}}$ is the average amplitude of all the experimental and the numerical data points, respectively.

The optimum combination of the effective properties and the input voltage is computed and the result obtained is compared with the experimental data in Fig. 18.16b. The result corroborates the effectiveness of the hybrid approach.

18.3.2.3 Depolarization of Piezoelectric Disk

The depolarization of the piezoelectric disk is attributed to the applied voltage, the mechanical stress, and the ambient temperature. If significant, it reduces piezo-coupling and thus reduces the amplitudes. In order to characterize the depolarization

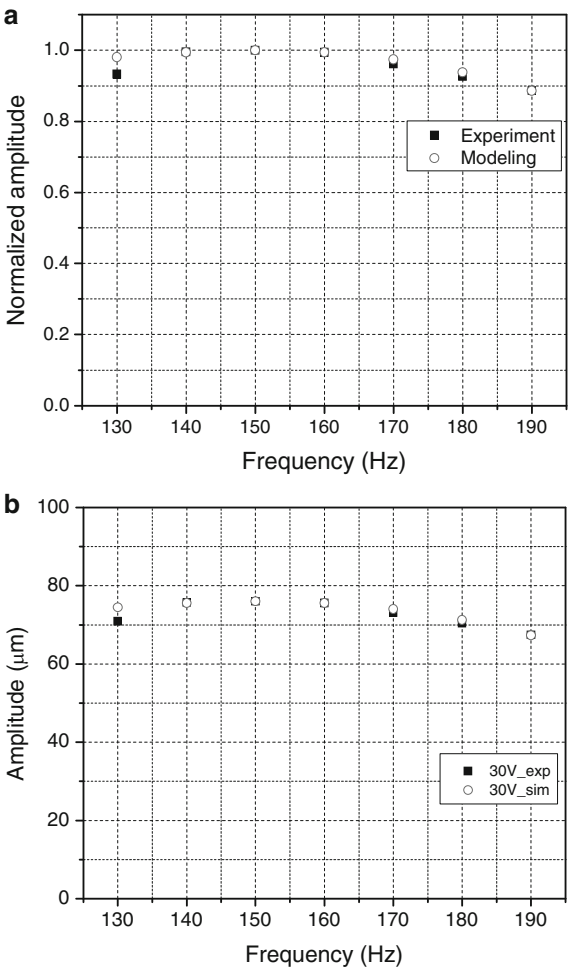


Fig. 18.16 Results of hybrid model at an input voltage of 30 V: (**a**) normalized amplitudes and (**b**) absolute amplitudes

effect, three groups of synthetic jets have been tested for 3,000 h at three different temperature conditions (60, 90 and 120 °C). The planer coupling coefficient which indicates the amount of polarization property has been measured during operation.

Figure 18.17 shows the experimental results. The coupling coefficient decreased initially but stabilized at 0.9, 0.86 and 0.81 for 60, 90 and 120 °C, respectively. The results confirm that the effect of depolarization on the piezoceramic disk is not significant and thus it will not be considered when the performance of the synthetic jet is to be evaluated in the PoF model.

18.3.2.4 Aging of Compliant Ring

For most polymers in oxygen-containing environments, oxidation is the dominant factor in aging [30]. The ductile polymer material becomes brittle due to the

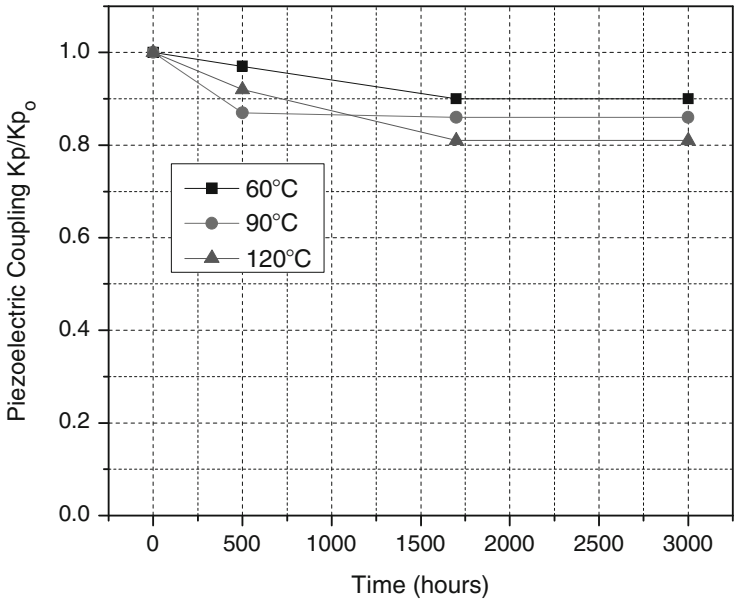


Fig. 18.17 Coupling coefficient of piezoelectric disk during aging

chemical reaction; the material modulus increases and the damping ratio decreases. In order to predict the material property change of polymer as a function of time and temperature, the Arrhenius relation, which is well known in chemical kinetics, can ascertain thermo-oxidative aging of polymers.

Time/Temperature Superposition Method

The principle of time/temperature superposition was adopted to characterize the aging of the compliant ring. The time/temperature superposition is a well-known procedure, which can be applied to verify the temperature dependence of the rheological behavior of a polymer or to expand time or frequency regime for a polymer at a test temperature. This is accomplished by multiplying the data points from the experiment with a shift factor a_T at a temperature of interest. The shift factors a_T are chosen empirically, to give the best superposition of the data. The shift factors a_T are related to the Arrhenius activation energy, E_a, by the following expression [30]:

$$a_T = \exp\frac{E_a}{R}\left(\frac{1}{T_{\text{ref}}} - \frac{1}{T}\right) \tag{18.15}$$

where a_T is the shift factor, E_a is the activation energy, R is the Boltzmann constant, T_{ref} is the reference temperature, and T is the testing temperature.

Equation 18.15 can be rewritten as:

$$\ln(a_T) = \frac{E_a}{R}\left(\frac{1}{T_{\text{ref}}} - \frac{1}{T}\right) \tag{18.16}$$

By plotting three shift factors using (18.16), the activation energy is obtained from the slope of the linear relationship.

Accelerated Test for Compliant Ring

In order to characterize the aging behavior of the compliant ring, aging test has been conducted. Three different aging temperatures (230, 250 and 275 °C) have been selected to accelerate the aging rate. Ten specimens have been exposed to each temperature. DMA tensile tests were conducted to measure the storage modulus and the loss tangent (tan δ) at 175 Hz at various time intervals.

Figure 18.18 shows the storage modulus and the loss tangent, changes over time at the three different aging temperatures. Each data point represents the average value of 10 specimens. The principle of time/temperature superposition was implemented with the reference temperature of 275 °C. All other curves were shifted to the curve at 275 °C to determine the shift factors.

The shift factors for the storage modulus and loss tangent were plotted in Fig. 18.19 (18.16). The slopes of linear lines represent the activation energies (E_a): the activation energies of the storage modulus and the loss tangent are 126 kcal and 128 kcal, respectively.

The data shifted by the shift factors are shown in Fig. 18.20. The results clearly indicate that the time/temperature superposition is valid for the data. The master curves for the storage modulus and the loss tangent can be expressed by the following exponential functions:

$$E(t;T) = A\exp\left(\frac{a_T(T)}{B}t\right) + E_0 \tag{18.17}$$

$$\tan\delta(t;T) = C\exp\left(\frac{a_T(T)}{D}t\right) + \tan\delta_0 \tag{18.18}$$

where $E(t;T)$ and $\tan\delta(t;T)$are the time-dependent modulus and the loss tangent at a given temperature T. Three unknown constants (A, B, and E_0) for the storage modulus and (C, D, and $\tan\delta_0$) for the loss tangent can be determined by a nonlinear regression analysis: the constants for equations (18.17) and (18.18) are summarized in Table 18.4. The function described by (18.17) and (18.18) are also shown in Fig. 18.20a, b, respectively.

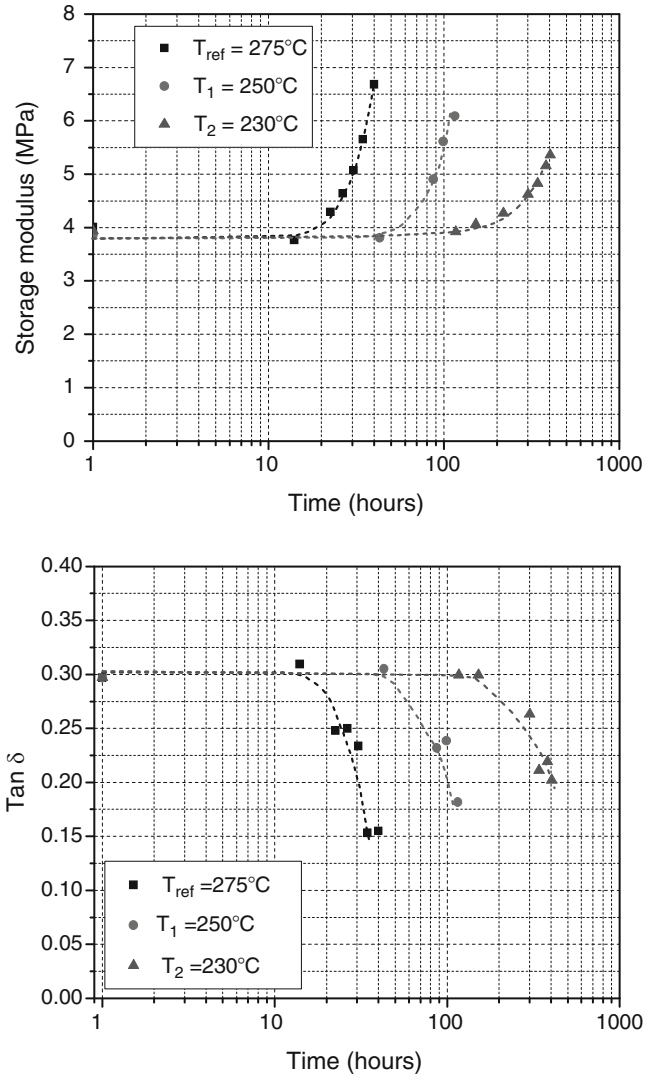


Fig. 18.18 (**a**) Storage modulus and (**b**) tan δ over time at different aging temperatures

The actual operating temperature of the synthetic jet is 55 °C [31]. The shift factor for 55 °C was obtained from (18.15): 8.63×10^{-9} and 6.55×10^{-9} for the storage modulus and tan δ, respectively. The change in storage modulus and loss tangent was subsequently predicted by (18.17) and (18.18) and the results are shown in Fig. 18.21a, b. The storage modulus is predicted to be 3.8 MPa at 50,000 h, while the loss tangent does not show any noticeable change.

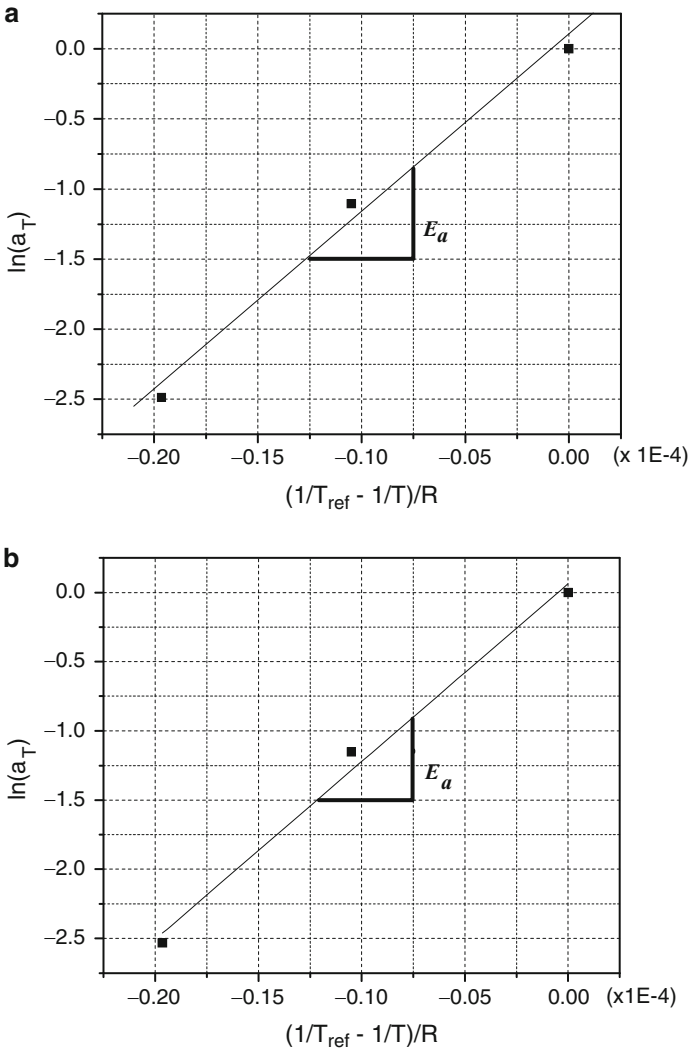


Fig. 18.19 Activation energies of (**a**) storage modulus and (**b**) tan δ

18.3.3 Prediction of Junction Temperature Versus Time

The amplitude change of the synthetic jet is shown in Fig. 18.22a. The amplitude data is converted to the air flow rate (18.5) and the air flow rate is subsequently converted to enhancement factor (EF) using the empirical relationship between EF vs. air flow rate. The EF is plotted in Fig. 18.22b. Finally, the junction temperature is determined from the relationship between the junction temperature and the EF. The result is shown in Fig. 18.22c. The junction temperature remains nearly the same after 50,000 h.

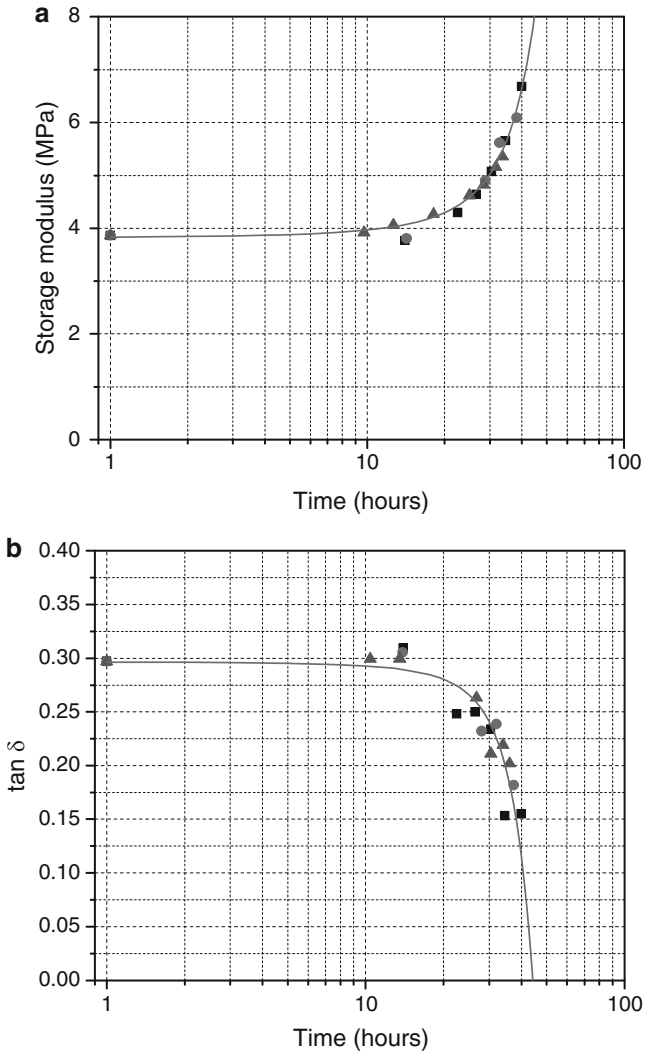


Fig. 18.20 Master curves of (**a**) storage modulus and (**b**) tan δ obtained from Fig. 18.10 where the reference temperature is 275 °C

Table 18.4 Constants of master curves of modulus and tan δ

Constant	Value
A	0.103
B	−11.9
E_0	3.70
C	−0.00178
D	−8.63
tan δ_0	0.298

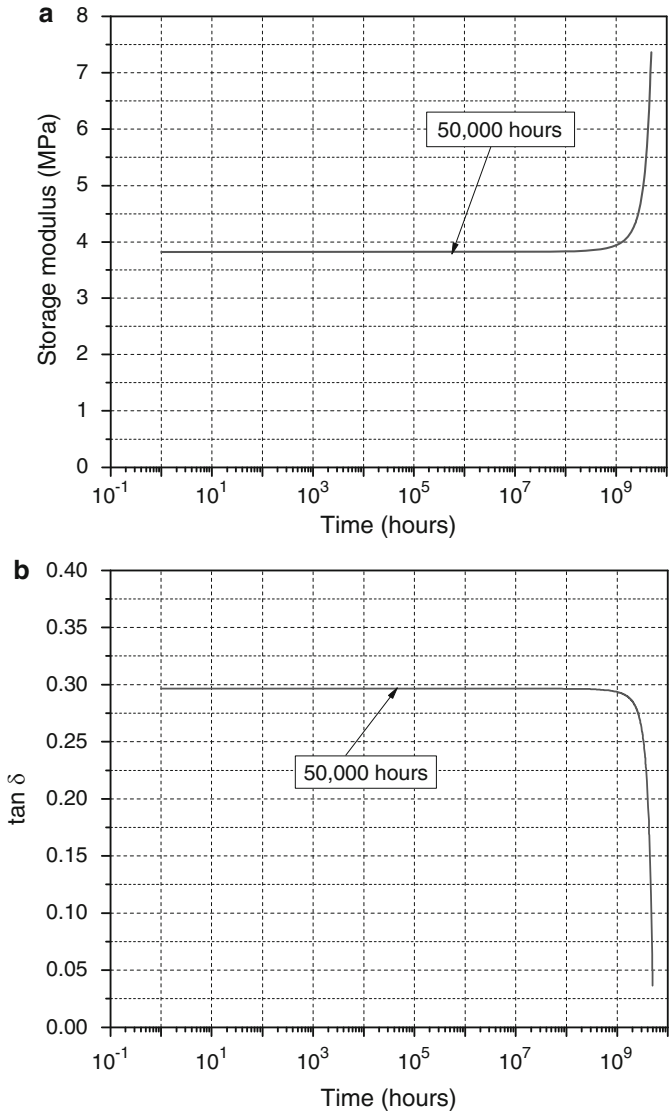


Fig. 18.21 (**a**) Storage modulus and (**b**) tan δ at 55 °C as a function of time

18.3.4 Analysis of Power Electronics

The reliability of power electronics is critical to the operation of the synthetic jet and LED light engine. The analysis of the power electronics in this section is limited only to the degradation mechanisms that cause output voltage drop; the breakages of other passive devices that cause catastrophic failure of the circuits is not considered.

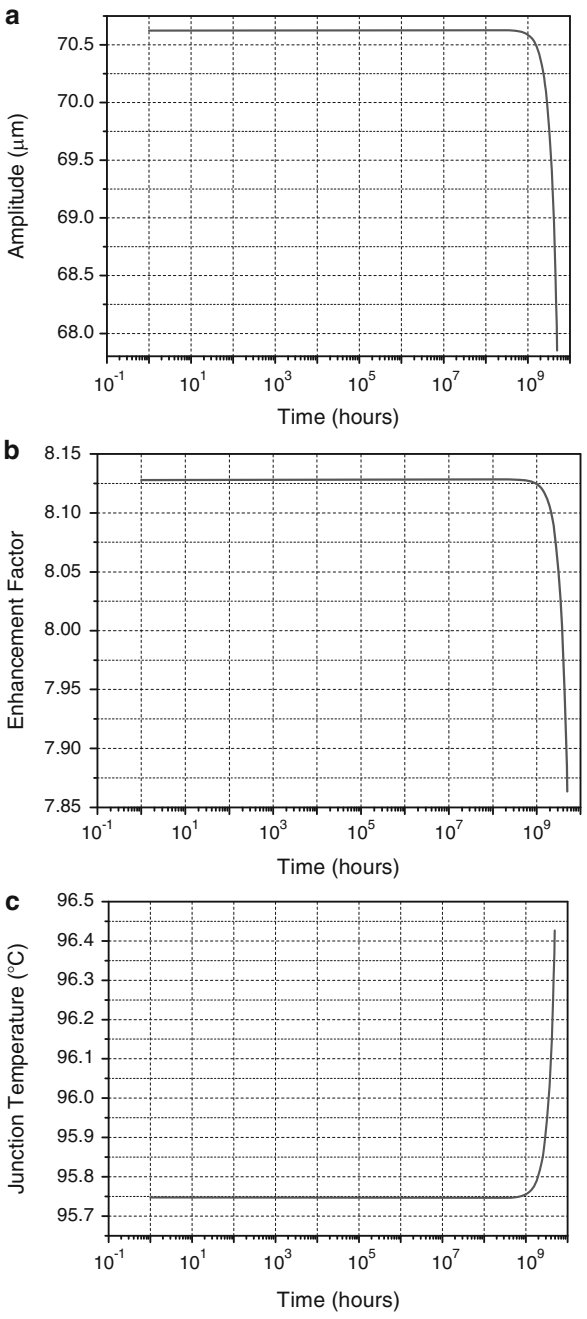


Fig. 18.22 (**a**) Amplitude, (**b**) enhancement factor, and (**c**) junction temperature as a function of time

Table 18.5 Values of passives in the jet driving circuit

Component	Value
R	200 Ω
L	500 mH
C_{jets}	565 nF
C_{circuit}	1,220 nF

18.3.4.1 Synthetic Jet Driving Circuit

The synthetic jet driving circuit is a resonant circuit, which provides an excitation voltage of ±30 V at 175 Hz of frequency. The piezoceramic disks in the synthetic jets act as one of the capacitors in the circuit. The capacitance of the piezoceramic disk can be degraded over time [32, 33], which in turn can change the operating voltage of the driving circuit.

The impedance of the resonant circuit can be expressed as:

$$X_{\text{total}} = \sqrt{R^2 + \left(2\pi fL - \frac{1}{2\pi fC_{\text{total}}}\right)^2} \tag{18.19}$$

where X_{total} is the impedance of the circuit in ohms, R is the resistance in ohms, f is the frequency in Hz, L is the inductance in henrys, and C_{total} is the total capacitance of capacitors in the circuit and a synthetic jet in parallel in farads. Then the current (I) of the circuit is expressed as:

$$I = \frac{V}{X_{\text{total}}} \tag{18.20}$$

where V is input voltage. Table 18.5 shows the actual values of the passives used in the circuit.

The applied voltage to synthetic jet then becomes:

$$\begin{aligned} V_{\text{jets}} &= IX_C = \frac{I}{2\pi fC_{\text{total}}} \\ &= \frac{V}{2\pi f(C_{\text{total}} + C_{\text{jets}})\sqrt{R^2 + \left\{2\pi fL - \frac{1}{2\pi f(C_{\text{total}}+C_{\text{jets}})}\right\}^2}} \end{aligned} \tag{18.21}$$

where V_{jets} is the applied voltage to synthetic jets and X_C is the impedance of the total capacitance.

The effect of capacitance reduction of synthetic jet (C_{jets}) on applied voltage (V_{jets}) is shown in Fig. 18.23. The initial capacitance of synthetic jet was 565 nF and the voltage was about 30 V. The result shows that the voltage remains about 30 V even when the capacitance of synthetic jet becomes 0. The capacitance degradation of piezoceramic disk does not have a significant effect on the applied voltage in the synthetic jet.

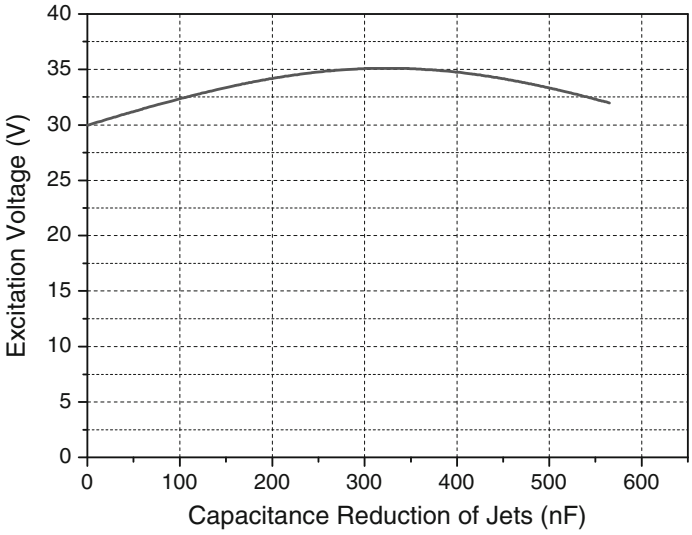


Fig. 18.23 Effect of SJ capacitance reduction on excitation voltage

18.3.4.2 LED Driving Circuit

The current design of power electronics which drives LED light engine is composed of many electronic components such as capacitors, diodes, resistors, inductors and transistor-transistor logic (TTL). The most critical parts have been identified as electrolytic capacitors [34–37]. The effect of electrolytic capacitor degradation on the LED driving circuit is evaluated.

The LED drive circuit supplies a constant power to the LEDs, which are connected in series, set by the DCM (Discontinuous Conduction Mode) operation of the standard flyback converter. Any fluctuation of the voltage output will thus affect the current through the LEDs [26]. The current fluctuation can be estimated by the forward voltage and the current relationship [38] assuming that the LED impedance remains constant over the range of voltage fluctuation. The major source of voltage fluctuation is the ripple voltage magnitude in the dc output.

The forward voltage oscillates between $V_{\max}$ and $V_{\min}$; the magnitude of ripple voltage, V_r, is $V_{\max} - V_{\min}$. The amount of ripple voltage can be estimated through the relationship between the capacitance and the ripple voltage, which is expressed as:

$$V_r = \frac{I}{2fC} \tag{18.22}$$

where V_r is the ripple voltage, I is the current, f is the frequency, and C is the capacitance of capacitors in the circuit. Then the average voltage (V_{ave}) can be expressed as:

$$V_{ave} = V_{max} - \frac{V_r}{2} \tag{18.23}$$

The capacitance degradation can be expressed as [39, 40]:

$$C = C_0\left(Ee^{-\frac{t}{t_1}} + F\right) \tag{18.24}$$

where C is capacitance, C_0 is initial capacitance, t is time and E, t_1 and F are constants. The data in ref. [39, 40] was also used as a conservative representation of the capacitance degradation. The percentage drop of the capacitance based on the function is shown in Fig. 18.24a.

The voltage applied to each LED can be estimated by

$$V_f = \frac{V_{ave}}{N} \tag{18.25}$$

where V_f is the voltage drop across each LED and N is the total number of LED in the circuit. The forward voltage decrease can be shown in Fig. 18.24b. The decrease of forward voltage can be converted to forward current reduction with the V_f versus I_f relationship. If the data in ref. [38] is used, the current decreases by about 5% while the capacitance decreases by 12%. Since the current reduction is not significant with this data, it will not be considered when the performance of the power electronics is to be evaluated in the PoF model.

18.3.5 Life Time Prediction

18.3.5.1 Lifetime of LED

Since the lifetime of luminaire is governed by the lumen maintenance of LED, LED lifetime directly affects the failure of the luminaire (L70 lifetime). In order to estimate the LED lifetime, major LED manufactures adopted IESNA LM-80 which prescribes standard test methods for LED under controlled conditions to measure lumen maintenance of LED while controlling the junction temperature and ambient temperature in DC constant current mode [41].

The lifetime of LED in the luminaire is estimated based on data in ref. [42]. The luminaire utilizes the polycarbonate lens and the ambient temperature inside the lens is 65 °C. The L70 lifetime at 65 °C of ambient temperature is shown in Fig. 18.25 [25]. It is to be noted that the L70 lifetime at the applied current of 500 mA was interpolated using the data at 350 and 700 mA.

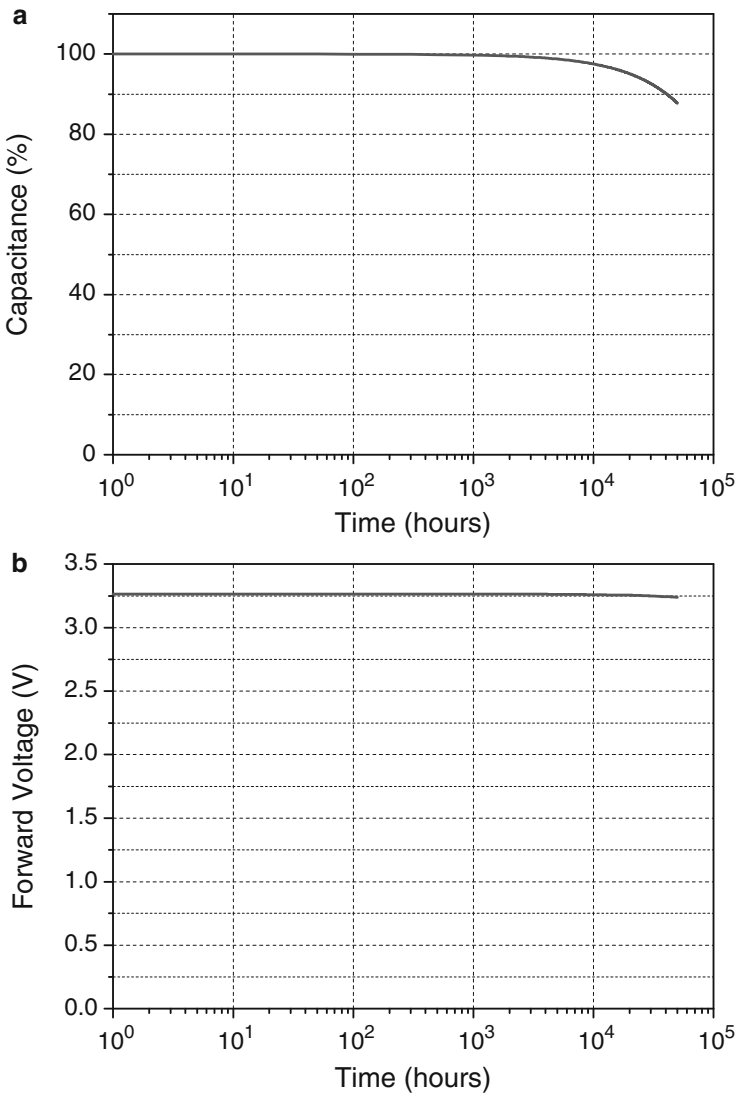


Fig. 18.24 Reduction as a function of time: (**a**) capacitance and (**b**) forward voltage

18.3.5.2 Computation of Luminaire Lifetime

All the information for the computation of lifetime has been obtained in the previous sections. The purpose of experiments and calculations was to predict the decay constant profile with time by using the junction temperature and forward current prediction data. The lumen maintenance then can be determined using the decay constant profile.

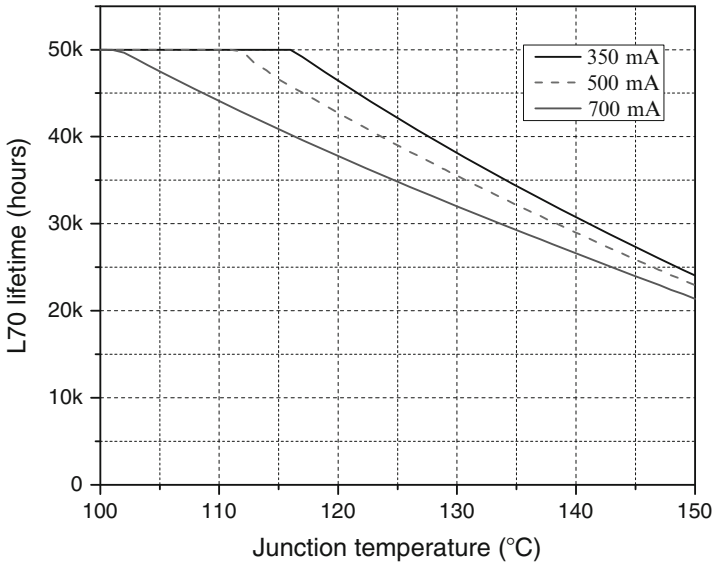


Fig. 18.25 Mean L70 Lifetime at 65 °C of ambient temperature, operated at $I_f = 350$ mA and 700 mA

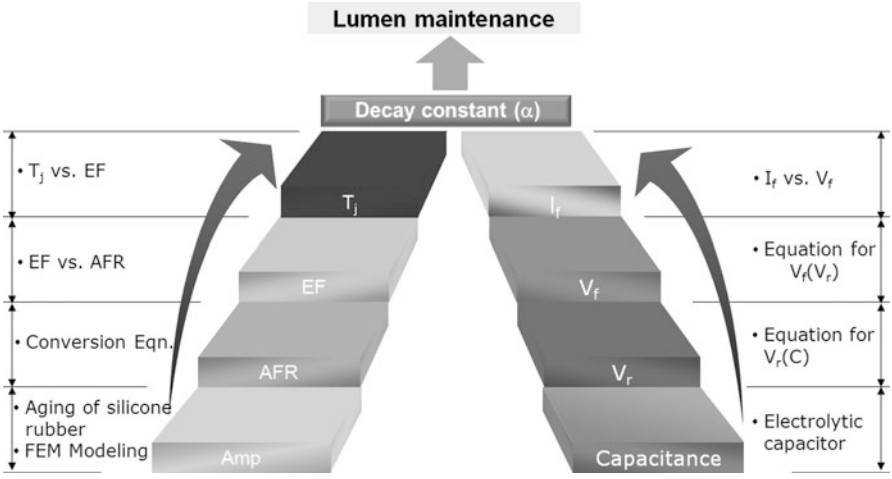


Fig. 18.26 Computation procedure for luminaire lifetime

Figure 18.26 summarizes the procedure to compute the luminaire lifetime. The left track shows all the processes from the amplitude degradation of the synthetic jet to the junction temperature. The amplitude degradation of the synthetic jet is first determined through the hybrid experiment/numerical model

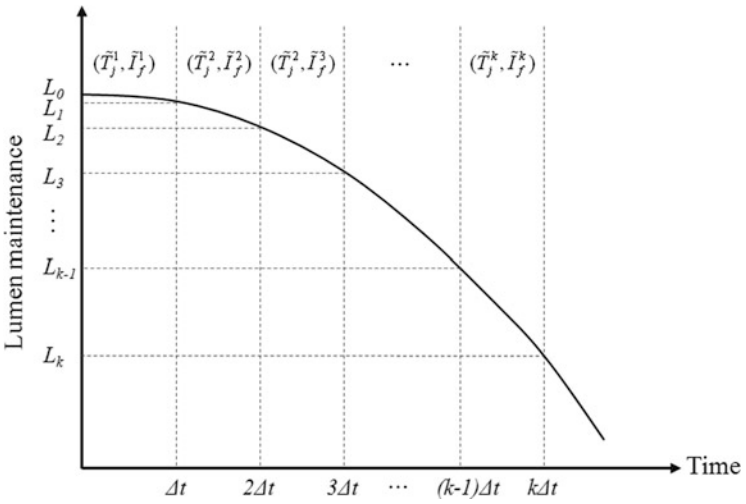


Fig. 18.27 Illustration of lumen maintenance after each time interval

considering the compliant ring aging. The amplitude is converted to the air flow rate (18.5). Then the junction temperature is determined as a function of time using the empirical relationship between the enhancement factor and the junction temperature.

The right track deals with the issues associated with the driver electronics. The increase in the ripple voltage, caused by the capacitance degradation of the electrolytic capacitors in the LED driving circuit, is determined as a function of the operating time using the data in ref. [40]. Then the reduction of the forward current is subsequently determined from the relationship between the forward current and forward voltage.

From (18.3), the decay constant for a given junction temperature and a forward current can be expressed as:

$$\alpha(T_j, I_f) = -\frac{1}{t_{L70}(T_j, I_f)} \ln 0.7 \tag{18.26}$$

where t_{L70} is the time at the lumen maintenance of 0.7.

The junction temperature will rise with time, which can be expressed in a general form as $T_j(t) = T_j^0 + K(t)$ where T_j^0 is the initial junction temperature and $K(t)$ is a function that defines the junction temperature increase as a function of time. The forward current will decrease with time, which can also be expressed as $I_f(t) = I_f^0 + I(t)$ where I_f^0 is the initial forward current and $I(t)$ is a function that defines the forward current decrease as a function of time.

As illustrated in Fig. 18.27, the lumen maintenance after each small time interval of Δt can be expressed as:

$$L_k = L_0 \exp\left[-\Delta t \sum_{i=1}^{k} \alpha(\tilde{T}_j^i, I_f^i)\right] \quad \text{for } k = 1, 2, 3... \tag{18.27}$$

where

$$\tilde{T}_j^k = \frac{T_j((k-1)\Delta t) + T_j(k\Delta t)}{2} = \frac{T_j(t^{k-1}) + T_j(t^k)}{2}$$
$$\tilde{I}_f^k = \frac{I_f((k-1)\Delta t) + I_f(k\Delta t)}{2} = \frac{I_f(t^{k-1}) + I_f(t^k)}{2}$$

where L_k is the lumen maintenance after the kth time interval; $\tilde{T}_j^k$ is the averaged junction temperature over the kth time interval; I_f^k is the averaged forward current over the kth time interval; L_0 is the initial lumen output at time zero. It is worth noting that the function, $K(t)$, is directly related to the time-dependent performance degradation of the active cooling system (i.e., EF reduction). The function, $I(t)$, in the computation is 0 due to the small amount of reduction of the current and thus I_f^k is constant (500 mA). Then the lifetime criterion can be expressed as:

$$0.7L_0 \geq L_k \tag{18.28}$$

If t is set, the unknown "k" can be determined. In practice, the optical component degradation in the fixture as a function of temperature is ignorable. Then the final expected life at 70% lumen maintenance can be determined as

$$t_{\text{life}} = k\Delta t \tag{18.29}$$

The decay constant for each time interval can be computed by (18.26). The result is shown in Fig. 18.28. Then, the lumen maintenance is calculated by (18.27). Figure 18.29 shows the final result. Based on this calculation, the lumen maintenance is estimated to be 76% after 50,000 h operation.

18.4 Summary

A novel luminaire design approach with thermal, light engine, driver electronics technologies was developed for a 100 W incandescent replacement lamp. The number of LEDs in the luminaire is certainly a major driver for the cost of the luminaire. It is critical to have the lowest possible number of LEDs so that the product can be affordable. In addition, different subcomponents must interact with each other seamlessly for the lifetime of the luminaire (>50,000 h) and is critical for the SSL product.

A physics-of-failure based, hierarchical reliability model was implemented subsequently to determine the lifetime of the luminaire. The degradation mechanisms of each of the main components (LED light engine, cooling system, and power electronics) were analyzed and their combined effect on luminaire

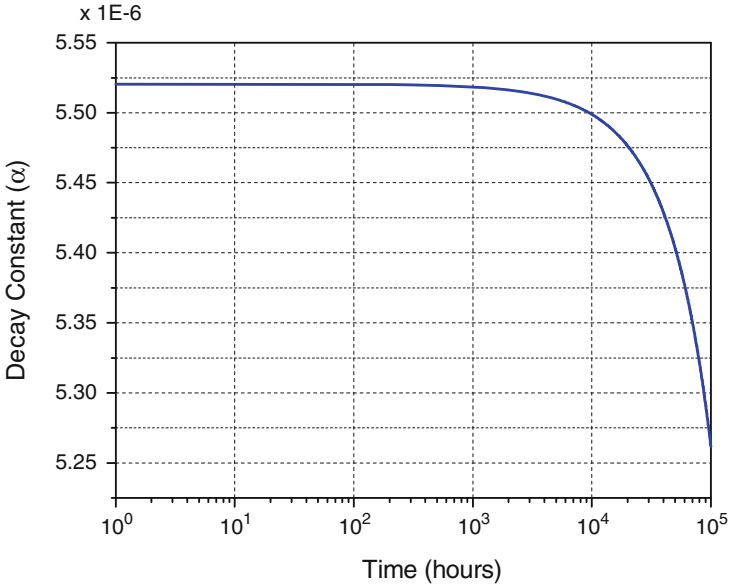


Fig. 18.28 Decay constant versus time

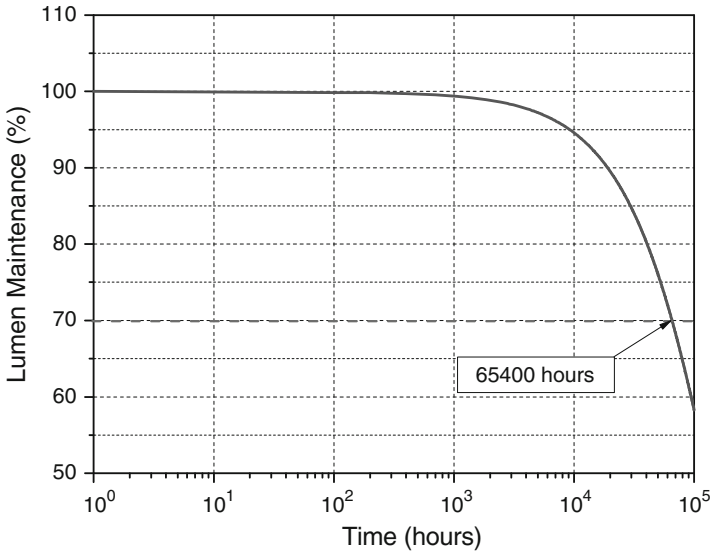


Fig. 18.29 Lumen maintenance versus time

reliability was calculated. The degradation rate of the synthetic jet was extremely low and the junction temperature rise over the intended life (50,000 h) was negligible. For the power electronics, only time-dependent degradation of large electrolytic capacitors was considered and its effect on the ripple voltage increase was estimated using the existing data in the literature. Based on the proposed hierarchical model, the lumen maintenance was estimated to be 76% after 50,000 h operation.

References

1. Vio white LEDs. http://www.lumination.com/product.php?id=56
2. Solid-state lighting research and development. http://apps1.eere.energy.gov/buildings/publications/pdfs/ssl/sslmypp2009web.pdf
3. http://www.newark.com/pdfs/datasheets/Lumileds/LUXEONIII_STAR.pdf
4. Gardner NF et al (2007) Blue-emitting InGaN-GaN double-heterostructure light-emitting diodes reaching maximum quantum efficiency above 200 A/cm(2). Appl Phys Lett 91
5. http://www.cree.com/index.asp
6. Nichia Corporation. http://www.nichia.com/
7. Hofler GE et al (1996) Wafer bonding of 50-mm diameter GaP to AlGaInP-GaP light-emitting diode wafers. Appl Phys Lett 69:803–805
8. Arik M, Setlur A (2010) Environmental and economical impact of LED lighting systems and effect of thermal management. Int J Energ Res 34:1195–1204
9. Arik M et al (2007) Chip to system levels thermal needs and alternative thermal technologies for high brightness LEDS. J Electronic Packag 129:328–338
10. Energy efficiency and renewable energy. http://www1.eere.energy.gov/buildings/ssl/comparinglights.html
11. Kückmann O (2006) High-power LED arrays, special requirements on packing technology. Proc SPIE 6134:613404
12. Liu TLS, Luo X, Chen M, Jiang X (2006) A microjet array cooling system for thermal management of active radars and high-brightness LEDs. In: Proceedings electronic component technology conference, pp 1634–1638
13. Arik M (2007) An investigation into feasibility of impingement heat transfer and acoustic abatement of meso scale synthetic jets. Appl Thermal Eng 27:1483–1494
14. Garg J et al (2005) Advanced localized air cooling with synthetic jets. ASME J Electron Packag 127:503–511
15. Arik YUM, Ozmusul M (2008) Effect of synthetic jets over a natural convection heat sink. Proc ASME IMECE, p 68784
16. Arik M et al (2010) Development of a high lumen solid state down light application. IEEE Trans Compon Packag Tech 33:668–679
17. Cree EZ1000 LEDs datasheet. http://www.cree.com/products/pdf/CPR3CR.pdf
18. Erickson RW, Maksimovic D (2001) Fundamentals of power electronics, 2nd edn. Kluwer, Norwell, MA
19. Mohan N et al (1989) Power electronics, converters, applications, and design. Wiley, New York
20. Song BM et al (2010) Hierarchical life prediction model for actively cooled LED-based luminaire. IEEE Trans Compon Packag Tech 33:728–737
21. Ishizaki S et al (2007) Lifetime estimation of high power white LEDs. J Light Vis Environ 31:11–18

22. Meneghesso G et al (2010) Recent results on the degradation of white LEDs for lighting. J Phys D: Appl Phys 43:354007
23. Deshayes Y et al (2005) Long-term reliability prediction of 935 nm LEDs using failure laws and low acceleration factor ageing tests. Qual Reliab Eng Int 21:24
24. Narendran N et al (2004) Solid-state lighting: failure analysis of white LEDs. J Cryst Growth 268:449–456
25. Gu Y et al (2004) White LED performance. Presented at the 4th international conference on solid state lighting, 2004
26. Han L, Narendran N (2009) Developing an accelerated life test method for LED drivers. Presented at the 9th international conference on solid state lighting, San Diego, 2009
27. Nader G et al (2004) Effective damping value of piezoelectric transducer determined by experimental techniques and numerical analysis. ABCM Symp Ser Mechatronics 1:271–279
28. Bao MH, Yang H (2007) Squeeze film air damping in MEMS. Sens Actuators A Phys 136:3–27
29. Rao SS (1995) Mechanical vibrations, 3rd edn. Addison-Wesley, New York
30. Wise J et al (1995) An ultrasensitive technique for testing the arrhenius extrapolation assumption for thermally aged elastomers. Polymer Degrad Stabil 49:403–418
31. Song B-M et al (2012) Life prediction of LED-based recess downlight cooled by synthetic jet. Microelectron Reliab 52(1):937–948
32. Chen WP et al (2003) Degradation in lead zirconate titanate piezoelectric ceramics by high power resonant driving. Mater Sci Eng 99:203–206
33. Tai W-P, Kim S-H (1996) Relationship between cyclic loading and degradation of piezoelectric properties in Pb(Zr, Ti)O3 ceramics. Mater Sci Eng B38:182–185
34. Stevens JL et al (2002) The service life of large aluminum electrolytic capacitors: effects of construction and application. IEEE Trans Ind Appl 38:1441–1446
35. Harada K et al (1993) Use of ESR for deterioration diagnosis of electrolytic capacitor. IEEE Trans Power Electron 8:355–361
36. Lahyani A et al (1998) Failure prediction of electrolytic capacitors during operation of a switchmode power supply. IEEE Trans Power Electron 13:1199–1207
37. Sankaran VA et al (1997) Electrolytic capacitor life testing and prediction. Presented at the IEEE industry applications society annual meeting, New Orleans, Louisiana, 1997
38. Cree® XLamp® XR-E LED data sheet [Online]
39. Application guidelines for aluminum electrolytic capacitors [Online]
40. Pabjanczyk W et al (2009) Influence of ambient temperature on LED luminaires. Przeglad Elektrotechniczny 85:320–323
41. Subcommittee on Solid State Lighting of the IESNA Testing Procedures Committee (2008) Approved method: measuring lumen maintenance of LED light sources, LM-80-08. New York: Illuminating Engineering Society of North America
42. Huang BJ et al (2009) A PWM constant average current driving technique for solar LED lighting systems. J Chin Soc Mech Eng 30:455–465

Chapter 19
Design for Reliability of Solid State Lighting Products

Liyu Yang and Xiantao Yan

Abstract Light-emitting diode (LED) and SSL products, including packages, arrays, and modules are in the initial adoption stage, and there are many reliability and design challenges facing the industry. This chapter discusses several key aspects focusing on the reliability and the life time prediction for LED SSL products. Upfront product design for reliability activities to enable reliable SSL products are studied from both the product construction, manufacturing and application point of view.

19.1 Introduction

19.1.1 Light-Emitting Diodes Technology and Packaging

Light-emitting diodes (LEDs) are semiconductor devices which emit light by electrons moving from a point of high energy to a point of low energy when electric power is applied to them. The wavelength of the emitting light depends on the band gap energy of the materials forming the P–N junction. The direct band gap of LED material determines the wavelengths of the emission from near infrared light to ultraviolet light. The preferred method of regulating LED current is to drive the LED with a constant-current source, which translates into a constant LED brightness. Multiple LEDs can be connected in series to keep an identical current flowing in each LED. As a future lighting source, high power or ultra high power LEDs should be able to provide at least the following

- High luminous efficiency
- High power capability
- Good color rendering capabilities

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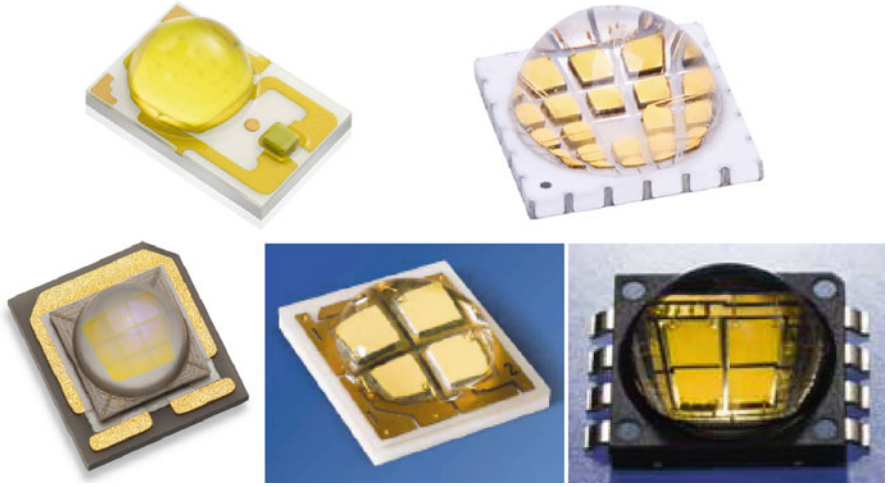


Fig. 19.1 Types of ultra high power LED packages ranging from substrate-based LED package (*upper left*, Philips Lumileds), substrate-based high density LED package (*upper right*, LED ENGIN Inc.), multi-die LED Emitters (*lower left*, Philips Luminleds), substrate-based LED Emitters (*lower middle*, Osram) to Cree's lead frame-based MC-E emitters (*lower right*)

- High reliability (lumen maintenance and color stability) and life time
- Low cost manufacturability and high flexibility

The lumen output of LEDs can be increased by enhancing the quantum efficiency using larger LED die and adopting heat-extraction methods. It can also be obtained by packaging more LED chip into one emitter or a module. However, the heat generated during the operation must be conducted away as fast as possible. The better the LED packages or SSL systems are at moving the heat quickly, will allow the more reliable LED will provide higher efficacy and a more consistent light output over time.

LED products should be optimized to achieve deliver consistent color and high efficacy, high light output, low cost, and long life. They should have high thermo-mechanical stability and low thermal resistance. During the package design, optical, electrical, thermal, and mechanical analyses must be refined in an iterative process with consideration for manufacturability, reliability, performance, and cost to arrive at an optimized design. Commercially available LED packages work adequately for many low power applications (less than 1 W). However, for high power or ultra high power LED emitters or applications requiring high luminous flux output, there will be many challenges for the packaging design and material selection.

LED packages typically include one or more LED chip mounted on the lead frame or a ceramic substrate using conductive adhesives or solders. Gold wires or flip chip bumps are used for electrical connections. Encapsulant are used for covering LED chip and gold wires, or acting as phosphor carrier, even acting as lenses. Additional optical lens are an option. Figure 19.1 and Table 19.1 show several representative LED packages used in the industry.

Table 19.1 Key attributes of leading high power emitters using one or multiple die

Product	Theta J, C/W	T_j max, °C	I_F max, mA	Vf, V	MSL Grade	LM80 Results @ 6K hours 85°C T_s
XP-G	4	150	1,500	3.75	1	98.7% (1A) @ $T_s = 85°C$
XM-L	2.5	150	1,000	14	1	97.2% (2A) @ $T_s = 85°C$
MC-E	3	150	700		NA	92.8% (0.7A) @ $T_s = 85°C$
MT-G	1.5	150	700 (185)	40.2	1	NA
MP-L	NA	NA	250 (125)	27.5	2A	96.7% (0.25A) @ $T_s = 85°C$
LZ1	6–10	150	1,500	3.5	1	97% (1A) @ $T_s = 50°C$
LZ4	1.7	150	1,200	14.5	1	99.9% (0.7A) @ $T_s = 85°C$
LZC	1.0	150	1,200	37.5	1	98.0% (0.7A) @ $T_s = 85°C$
LZP	0.7	150	1,000	78.5	1	NA
Rebel ES	6	150	1,000	3.5	1	50 (@ If = 1,000 mA and $T_j \leq 135°C$)
Luxeon-S	1.3	115	700	18	1	50 (@ If = 700 mA and $T_j \leq 110°C$)
OSLON	4.2	110	700	14.8	2	NA
OSTAR	7.0	135	800	3.5	2	NA

In many applications, long-term degradation and failures of GaN-based LEDs are primarily associated with the packages used. The common failure mechanisms of the package include package cracking, interface delamination, fatigue of wire bonding, and discoloration of encapsulation materials. In addition, all components surrounding the LED chip such as solder paste, silicone gel, phosphor materials, will degrade at different rates together with the LED chip during operation. The degradation of LED packages will be more serious at high operating temperature and high drive current. To build a robust LED package, the packaging materials should be carefully chosen and compatible with each other in order to reduce the thermo-mechanical stress and improve light out efficiency. For instance, a coefficient of thermal expansion (CTE) mismatch between LEDs die and the bonding solder will introduce stresses during temperature cycling or in the manufacturing process (e.g., SMT processes), the stress can cause die cracking and/or delamination between the die bonded surfaces. In the manufacturing process, the curing of the encapsulant is accompanied by shrinkage and development of internal stress. The larger the difference between the thermal expansion coefficients of the encapsulant and the substrate materials is, the higher the internal stress is, then may cause device failure during processing.

Package design and manufacturing processes are critical for reliable LED components and SSL systems. For high power or ultra high LED emitters, material selection are especially challenging in order to handle large amount of heat generated and contract more light out of the sources

- Encapsulant

Encapsulant has several functions in LED packages. First, it protects the device from the environment, such as contaminants and mechanical impacts; second, it

behaves as a lens focusing the light in the desired way; third, it helps improve the light output of LED device by increasing light extraction from LED chip. The encapsulant materials should be thermally matched with other packaging materials to reduce the risks of cracking and delamination. It should have high flame resistance and easy in–out path for moisture. The encapsulant materials should be high resistance to UV damage as well.

Typical encapsulant materials include silicone and epoxy. Encapsulant delamination, browning and cracking are typical failure mechanisms. Comparing with epoxy resin, silicone is considered a better choice for high power or ultra high power LEDs.

- Phosphor materials

White LED light can be made in different ways. The common approach is to use a blue-emitting diode that excites a yellow-emitting phosphor where the combination of blue and yellow makes a white-emitting LED. The performance of white LED will require the optimization of phosphors. In the application, the phosphor is embedded in an optical grade resin or silicone material. During the conversion process, phosphor materials will absorb light and often operate at a high temperature environment. Phosphor materials should maintain high thermal stability during the operation or order to maintain constant lumen output and color stability.

In general, LED packaging materials should be highly thermal conductive in order to enhance the heat transfer. In addition, the materials should be resistant to thermal aging and help extend reliability life of the lighting sources. Hotspots and attachment defects have a severe effect on the LED life and will lead to problems including LED degradation, wavelength shift, loss of radiant flux, and increase of forward voltage. Table 19.2 summarizes the key challenges for encapsulant materials and LED packages.

In terms of energy efficiency, LED emitters with multichip approach offer clear advantages. By providing direct emission at the necessary visible wavelengths, multichip LEDs avoid the absorption and emission losses of the phosphor as well as down conversion losses associated with generating lower energy phosphor emission from a higher energy blue source. The multichip approach has greater potential for actively controlling the light's spectral distribution, providing smart lighting capabilities far beyond traditional lamp systems. Using more LEDs creates multiple parallel conduction paths for the heat between the die and the board, and tends to reduce the effective thermal resistance from the die to the system.

19.1.2 Solid State Lighting Systems

The main driver for the adoption of solid state lighting (SSL) is the potential of energy efficiency, high efficacy, light quality, long life span, energy saving, and the environmental impact. SSL systems usually compromise of LED lighting sources

Table 19.2 Materials challenges and solutions for HB-LEDs packaging

Challenges	Issues	Solutions
Light extraction	Refractive index mismatch between LED die and encapsulant and secondary lenses	High refractive index encapsulant; efficient lens/cup design
Encapsulant yellowing/ browning	Degradation of encapsulants induced by high junction temperature; degradation of encapsulants induced by photonic energy	Silicone-based encapsulant to be used; high thermal conductivity materials; low thermal resistance for the packaging; high photonic resistance silicone-based encapsulant to be used
Delamination	Interface delamination failures caused by the CTE mismatch among encapsulant, LED die, and substrates/lead frames; contamination of interfaces as well as manufacturing defects at interfaces	Compatible materials in packaging; excellent adhesion between the bonded surfaces; optimal manufacturing processes to be defect and contamination free
Cracking	Encapsulant and package cracking failures due to thermo-mechanical stresses during manufacturing and field applications; elevated junction temperature	Low thermal resistance of the packages; high thermal stability materials, appropriate junction temperature, benign application conditions
Fatigue failures	Solder joint fatigue failures due to thermal cycling loads	Optimal solder joint formation and soldering processes; optimal solder materials; optimal surface mounting processes
Bond pad corrosion	Bond pad corrosion causing performance degradation and catastrophic failures	Clean bond pad surface; resistance to moisture under harsh environment and package structure improvement
Lifetime	Shorter life time comparing to expectations (e.g., 10K h or less instead of over 50K h)	Optimal operating conditions; low thermal resistance and compatible materials; optimal manufacturing processes; implementation of design for reliability practices

(e.g., emitters), thermal management designs (e.g., fans and heat sinks), electrical systems, and lens to achieve desired light color and reliability and life time.

In SSL systems, LED chip and driver electronics are highly temperature dependent. The driver electronics is critical to the system performance and high efficiency ($>$90%) is important in order to achieve high luminaire efficacy. The degradation of the electronics in the driver board can adversely impact the driving conditions and system reliability.

During SSL application, a large portion of the input power in LEDs is dissipated into heat that gets conducted into the LED circuit board. Thermal design is critical for optimal performance and reliability of the LED-based lighting systems. Of equal importance in SSL lighting system is how well the LED design handles

heat dissipation to the electronic board, how well the electronic board dissipates heat to the substrate and how well the substrates dissipates heat to the heat sink systems. And then, how well the fixture manufacturer dissipates the heat away from the lighting fixture.

High efficiency and long life design on the optical and driver side are crucial for the success of SSL. The optimized SSL system will help avoid light pollution as well.

19.1.3 Reliability Challenges of LED Components and SSL Systems

Reliability of LED components and SSL systems will impact the adoption of SSL technology and be a potential deal breaker. LED packages, array, modules, and SSL systems can be highly reliable achieve long life, and can help reduce the total cost of LED systems.

However, SSL technology is still in the early stage, some of the challenges can be summarized as:

- Tradeoff between high drive current and high efficacy.

High drive currents will increase the brightness of the LEDs. However, it will reduce the extrinsic quantum efficiency and result in lower efficacy. In addition, higher drive current will require better thermal management designs and possible increased cost, while potentially reduce the lifetime and reliability of SSL products.

- Ways to keep LED cool

At a high junction temperature, the overall LED efficacy will be significantly reduced. High temperature will lead to material degradation and short life time, thus giving substantial lumen losses that could nullify one of the key advantages of LED-based lighting. Controlling the junction temperature is critical in ensuring high LED efficiency and long life time.

- Performance improvement

High luminous flux is critical as well as efficacy for the system. However, it is also important to understand the mechanisms of the Lumen maintenance and color stability of LED components and SSL systems. It is desired to have high luminous flux and efficacy while maining the flux and color during the application.

- Materials and volume manufacturing

LED packaging materials and manufacturing processes are in fast development stage to help build robust packages, high reliability and long operating life. Thermal stability of the materials at high temperature will be a huge advantage. Phosphor materials stability and efficiency will help improve the performance and reliability

respectively. Packaging materials should be highly resist to corrosion and provide strong interface bond strength.

- Reliability and failure rate prediction.

Reliability and failure rate for LED products are built upon the understanding of IC components and electronics. There are no LED specific accelerated stress testing methods available in the industry. It is hard to compare the reliability of LEDs from various manufacturers. However, new testing methods and data processing approaches are being developed to standardize the description of reliability for SSL products. The definition of failure criteria for SSL products is being defined and understood. However, there are lack of reliability prediction models too. Reliability measurement and prediction methods are significant for the progress of LED industry. High reliability and low failure rate of LEDs need to be assured.

19.2 Reliability of LED Components (Packages, Arrays, and Modules)

19.2.1 Introduction

Reliability is defined as the probability of the components or systems to perform their intended functions within certain time under the application conditions. It can be predicted for given time under certain conditions. To conduct a successful reliability analysis, the failure criteria for LED components should be determined, additionally, the time-to-failure data should be collected.

Failures can be broadly categorized by the nature of the loads, like mechanical, thermal, electrical, radiation, or chemical, that trigger or accelerate the failure mechanisms. LED failures can be divided into catastrophic and parametric failures. Catastrophic failures are failures that will result in nonfunction of LED components. Parametric failures will result in changes of key characteristics in radiometric, photometric, and chromatic measurements.

For instance, in lighting industry, lumen maintenance is used to demonstrate the amount of light emitted from a source at any given time relative to the light output when the source was first measured (shown in Fig. 19.2, T_s is the solder joint temperature of the emitters). The parametric failure for a common LED application such as general lighting in an office environment, a level of 70% lumen maintenance could be considered as an appropriate failure criteria.

Besides lumen degradation, the chromaticity of light will shift with time as well, which is expressed by chromaticity coordinates (x, y) and (u', v'). The chromaticity of white light can also be expressed by CCT and the distance from the Planckian locus. CCT is a more intuitive measure of the shade of white light than (x, y), and is defined based on the $(u', 2/3v')$ chromaticity diagram. $Du'v'$ is defined as the closest distance from the Planckian locus on the $(u', 2/3v')$ diagram [2]. It should be kept in

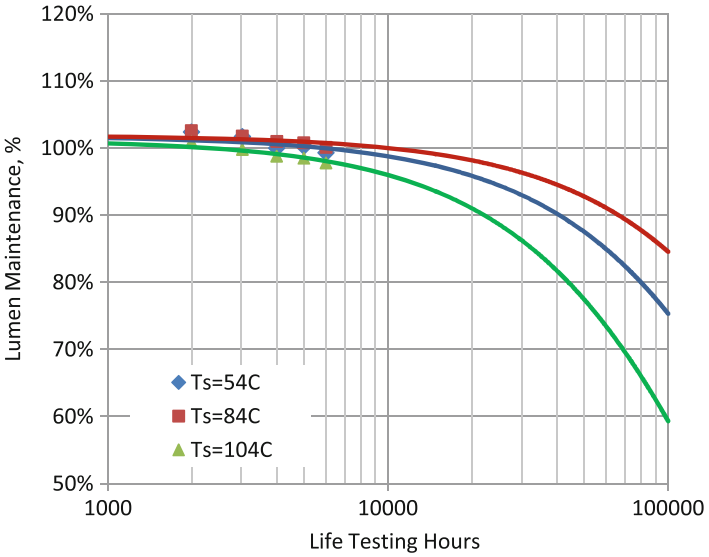


Fig. 19.2 Lumen maintenance curve of HB-LEDs

mind that color properties of LED lighting sources may change over the life span even they are manufactured with consistent correlated color temperatures (CCTs). The dominant mechanism of degradation of color temperature could be related to the LED chip due to the reverse leakage current dramatically increased. An extremely high current density at the junction interface could damage LED chips and rendered them inactive. Figure 19.3 shows one example of CCT and $Du'v'$ shift during accelerated stress testing of LED emitters.

In reliability terms, color stability describes the ability of a light source to maintain its color properties over time. A large and permanent shift in the exact color of white light output, called the white point or color shift is becoming more and more important in considering LED reliability. This shift can be accelerated by high temperatures, high moisture contents in materials and interfaces, and high drive currents. It is possible for the design of the phosphor and packaging systems to minimize these shifts and contain the shifts to be less than what can be detected by the human eyes.

Table 19.3 shows the most useful light sources color characteristics from a survey where stability and consistency were highly rated in the results.

LM-80-08 test method published by IESNA has required to include the chromaticity shift in the report. EPA Energy Star program defines the maximum color shift $Du'v'$ to be below 0.007 (7-step MacAdam Ellipse) over life time.

The reliability of LED components can be impacted by various factors, including packaging materials, package design, manufacturing processes, as well as the application conditions. The most important stress factors are LED junction temperature, drive currents, ambient temperatures, and chemical and photonic radiation. The drive current not only affects the LED chip itself, it also influences the junction temperature and subsequently the light output and the decay rate of the packaging

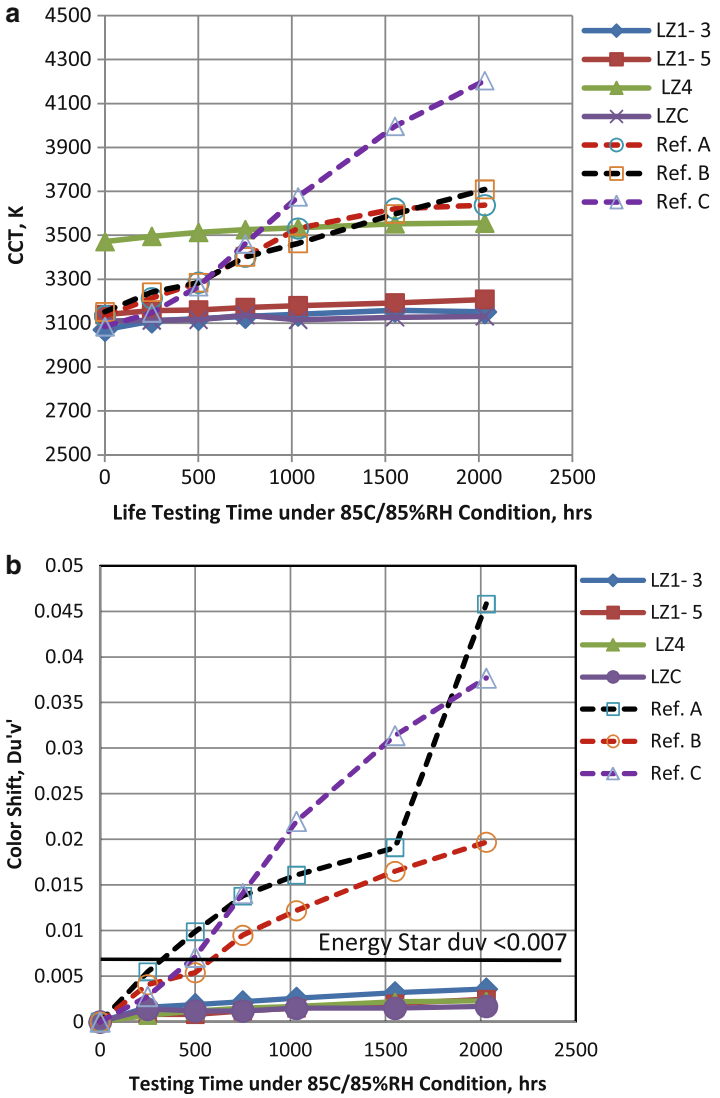


Fig. 19.3 Color shift Du′v′ under WHTOL testing conditions

Table 19.3 Most useful light sources color characteristics

Characteristics	Average useful ratings
Color rendering index (CRI)	3.5
Correlated color temperature (CCT)	3.2
Color stability	3.2
Color consistency	3.1

materials. Package design and material can help improve the thermal and optical performance and lower the thermo-mechanical stress induced by the mismatch of the CTE of packaging materials. The substrate materials and design will dramatically impact the thermal resistance and the reliability of LED components. For the LED manufacturers, the influencing factors should be taken into consideration in the package development phase. It should be reminded that field failures can be introduced by the interaction between defects in manufacturing and environmental loads. In general, the degradation of LED lumen output follows an exponential trend.

With the increase of photon energy from the high power or ultra high power LEDs, the material degradation will accelerate failures especially with high temperature. The degradation rate depends on both the junction temperature and the amplitude of short-wavelength radiation, but the temperature effect was much greater than the rest factors.

The reliability of LED components is not the same as LED quality or LED lumen maintenance or color shift. The reliability should consider all aspects of the failures, including random failures and degradation failures such as lumen maintenance failures (L70) and color shift ($Du'v'$) failures. The chromatic properties of white LEDs for lighting applications are determined both by the quality of the blue LED light and by the characteristics of the phosphor/package system used for white light generation and light extraction. Physics of failure (POF) is an approach to aid in the design, manufacture, and application of a product by assessing the possible failure mechanisms due to expected life-cycle stresses. POF is a very useful tool to understand the failure observed and help identify the root causes. However, it is not a tool for reliability prediction. Excessive reliability testing needs to be conducted to collect failures data in order to understand the impact of stress factors on the performance as well as develop prediction models under use conditions.

19.2.2 Failure Mechanisms of LED Components

Although LED components tend not to fail catastrophically, the light output and color quality degrades gradually over time due to many reasons, including LED junction temperature, drive current, photonic radiation, and packaging materials. Other failures could be caused by manufacturing defects or application conditions, including ohmic contact deterioration, poor bonding, and contaminations. Electrostatic discharge (ESD) and electrical overstress (EOS) are main causes of LED failures during fabrications and handling processes. In the following sections, common failure mechanisms seen in LED components are discussed:

- Interface delamination and silicone cracking.

Interface delamination and component cracking failures could be seen due to thermal cycling magnitude, elevated temperature, interface adhesion degradation and moisture stressing. Besides the thermo-mechanical loads, silicone cracking could also be introduced by excessive high temperature and the radiation damage

[12]. In white LEDs, delamination can either occur between the phosphor coating and the silicone encapsulant or between the LED die and the phosphor coating. The delamination failure or silicone cracking might not cause a catastrophic failures but can cause a permanent reduction in light output over time. Figures 19.4 and 19.5 show the cracking and interface delamination failures observed in LED packages.

- Silicone browning/darkening.

With the increased power in LED emitters, the radiant power and junction temperature will likely increase, encapsulant material degradation through browning/darkening likely could limit the LED performance such as a significant reduction of light output. The failure mechanism is usually caused by excessive heat experienced by the package. To address the challenges, conventional overmolded lead frames have been replaced with multilayer ceramic packages in order to reduce the thermal resistance of packages. Epoxy adhesive layers in die attach have been replaced by solder paste to improve heat conduction. Copper spreader slugs have been utilized to spread heat within the package more efficiently (Fig. 19.6).

- Fatigue failures

Fatigue failures are usually seen in bonding wires or solder joints, introduced by thermo-mechanical stress due to repeated thermal and mechanical loading and unloading, such as thermal cycling and power cycling.

When LED packages are mounted on application boards or MCPCBs, solder joints can experience fatigue failures during thermal cycling testing or in power cycling. Many tests demonstrated that Cu MCPCBs can achieve better thermal cycling performance comparing to popular low cost Al MCPCBs. In addition, many design factors including solder paste volume, stand-off height, solder fillet can significantly affect the assembly reliability. It was found the influence of package size will affect the thermo-mechanical performance dramatically. Fatigue failures will cause catastrophic failures of LED products. Figure 19.7 shows a typical solder joint failure in LED packages mounted on AL MCPCBs.

- Corrosion failures

Corrosion is the disintegration of materials into its consistent atoms due to chemical reaction with its surroundings. It means electrochemical oxidation of metals in reaction with oxidant. Corrosion failures often occur in the presence of chemical activators, temperature, voltage, moisture, and contaminants. They can be bonding pad corrosion or internal corrosion. Three standard accelerated stress tests are typically used to accelerate corrosion failure mechanism, including 85°C/85%RH, HAST and autoclave testing. K. Striny and A. Schelling [84] studied the aluminum corrosion failures during temperature and humidity testing. It showed the use of silicon nitride passivation, RTV silicone rubber encapsulation and effective cleaning can be the leading factors in preventing the corrosion failures. In addition, device operating with high power dissipation will see much lower failure rates since the heat will drive away the moisture. J. M. Kang et al. [44]

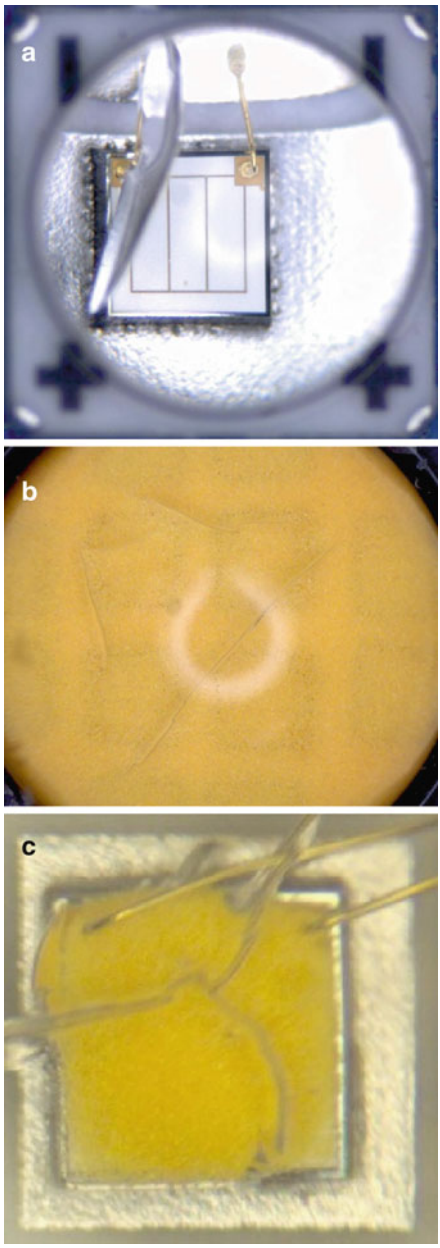


Fig. 19.4 Silicone cracking in LED packages. (**a**) Silicone cracking in LED Emitter. (**b**) Siicone cracking in white LED Emitter. (**c**) Silicone/phosphor cracking in die top white LEDs

studied a new metal-based package. Comparing to traditional plastic packages, the light output degradation is up to 40% within aging time of 5,000 h, but no light-out. Power degradation was not observed using the new metal package, while a 40% degradation seen for traditional packages.

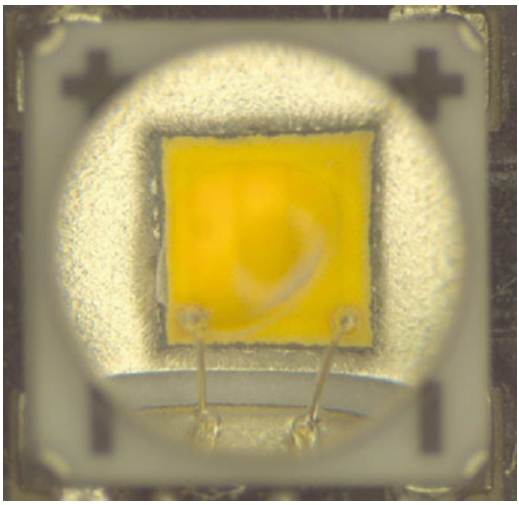


Fig. 19.5 Delamination of encapsulant in LED packages

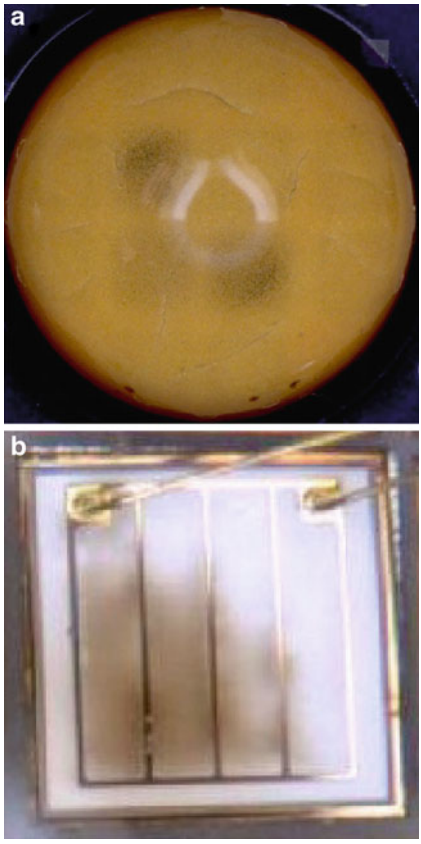


Fig. 19.6 Silicone browning and darkening seen in LED packages. (**a**) Silicone browning and cracking in white LEDs. (**b**) Silicone browning in color LEDs

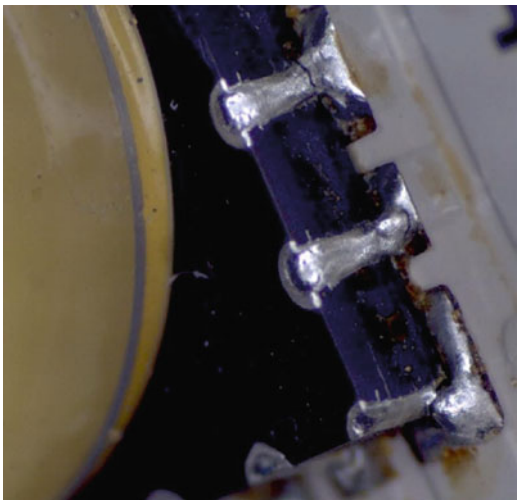


Fig. 19.7 Solder fatigue failures

- ESD and EOS failures.

ESD may cause immediate failure of the semiconductor junction, a permanent shift of its parameters, or latent damage causing increased rate of degradation. LEDs grown on sapphire substrate are more susceptible to ESD damages. EOS to the die is another causes of open failures. The forward biased pulse will pass through the LED without damage, but a reverse biased pulse can prove catastrophic. EOS can include fusing of the wire bonds due to over current situation. Wide bandgap diodes (e.g., GaN-based diodes) are particularly prone to ESD failures, due to low reverse saturation currents and high breakdown voltages. It is important to develop ESD protection circuits which consists of a series of Si diodes, one Si Zener diode, or two Si zener diodes. The electrostatics stress has little influence on aging of GaN/Si blue LEDs when the ESD voltage is less than 1,000 V. On the other hand, GaN-based LED is vulnerable to ESD damage [48]. During the manufacturing, handling, and application of LEDs, it is inevitably to suffer electrostatic stress which results in a rapid decay of intensity, internal leakage, and eventually device failure. Figure 19.8 shows the EOS damage on the LED emitters.

- Chip degradation and materials degradation

Most LEDs have a natural life span that ends in wear-out mechanism. Defects within the active region can introduce nucleation and dislocation growth. The degradation of LED devices will occur due to the generation of nonradiative defects, modification of the electrical properties of the ohmic contents and changes in the local indium concentration in the quantum wells (QWs) under electrical and thermal stresses.

GaN is a very hard and mechanically stable wide bandgap semiconductor materials with high heat capacity and thermal conductivity. It can be doped with silicon or with oxygen to n-type and with magnesium to p-type during LED

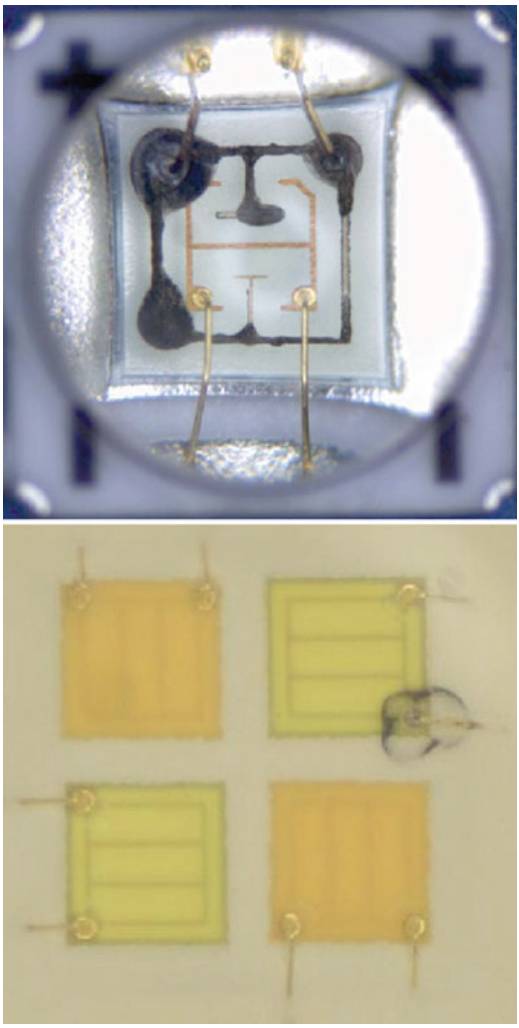


Fig. 19.8 ESD/EOS failures seen in LEDs

manufacturing. However, the Si and Mg atoms change the way the GaN crystals grow, introducing tensile stresses and making them brittle. Many processes have been indicated as being responsible for the degradation of GaN LEDs, including

1. The generation of nonradiative defects, which limit the internal quantum efficiency of the devices.
2. Modifications of the electrical properties of the ohmic contacts, with subsequent current and emission crowding due to the increased material resistivity.
3. Changes in the mechanisms of charge injection into active layer
4. Generation/modifications of complexes involving hydrogen and the acceptor dopant.

5. Changes in the local indium concentration in the QWs.
6. Modifications of the properties of the epoxy lens and plastic package, reducing the light transmission.

For AlGaN-based deep-UV LEDs, the reduction of Quantum efficiency and lifetime degradation are key concerns. Three major factors contribute to reduced UV LED reliability and efficiency, including dislocations, junction temperature and the package thermal impedance. The micropixel LED geometry reduces the series resistance and the current crowding which leads to a decrease in the junction temperature. M. Meneghini et al. [58, 60, 61] disclosed that the optical properties of the deep-UV LEDs are strongly influenced by the presence of deep level related radiative transitions. The driving current stress determines the gradual decrease of the output power of the LEDs, which is more prominent at low measuring current levels. Degradation is attributed to the increase of the nonradiative recombination rate. The mechanism is considered to be related to the generation of new defect states near/within the active region.

L. Zhang et al. [108] found that aging of phosphors and deterioration of the LED junction are primary causes of luminous attenuation of white LEDs. Under the thermal and electrical stresses, the resistance of the P–N junction will increase then cause the reduction of current density in the light-emitting region and luminous flux will be reduced.

- Leakage failures

LED packages have the potential to observe leakage failures if not handled correctly or the manufacturing process is not controlled well. J. S. Jeong et al. [45] reported the leakage from the mesa defects of P–N junction area is one of the key failure mechanism seen during temperature and humidity testing. A pin-hole in P–N junction area cause the indium exposed and then damaged InGaN quantum damage. The pin hole could be due to ESD injection. The temperature and moisture can introduce leakage failures of LEDs. Electromigration can be caused by high current density and move atoms out of the active regions or metallization, leading to emergence of dislocations and point. Metal diffusion is caused by high electrical currents or voltages at elevated temperature. The migration failures can cause short or leakage failures.

19.2.3 Stress Factors Affecting LED Reliability

The most dominant stress factor for LED reliability is junction temperatures, followed by drive currents, the combination of temperature and moisture of ambient conditions, thermal cycling and mechanical stresses in field applications.

The design of the accelerated stress test will run the products at a higher usage rate or overstress testing. Typical accelerating stresses are temperature, moisture, current, thermal cycling range, and vibration and high radiation. However, test

stress level should not be so high as to produce mostly other failure modes that rarely occur at the design process.

– Temperature

During the process of converting electrical signals to an optical form, LED emitters will produce heat. Light trapped inside a package often be absorbed by the package materials and then convert into heat as well, which lead to an extrathermal loading of LED devices. The thermal behavior of white LEDs is affected by internal and external factors. The internal factor includes light conversion efficiency of LED chip. The external factor is in terms of the ratio of light extracted from the LED package. A less light is extracted from the LED package, light is more likely to be absorbed by the package materials. Furthermore, due to the increasing integration and miniaturization of LED components, heat flux is increasing.

High LED junction temperature will post many challenges to LED components. First of all, reduced lighting efficacy will be observed, then the defects in the junction will accelerate the degradation of the LED characteristics, and third, high temperature will cause the degradation of packaging materials, such as browning/yellowing of silicone. Additionally, high junction temperature will shorten the life time of LEDs and reduce color stability. If the temperature is extremely high, LED die will seen catastrophic failures.

It is reasonable to assume that different product have different degradation rates as a function of heat, even at the same drive current [63]. M. Meneghini et al. [58, 60, 61] found the degradation of the electrical and optical properties at high temperatures is strongly related to the presence of the SiN passivation layer that is deposited by plasma-enhanced chemical vapor deposition (PECVD) on the LEDs for surface leakage reduction and for chip encapsulation.

The authors also reported the efficiency of LED devices decreased significantly during high temperature stress. The most important consequence of stress has been the decrease of the phosphor-related yellow emission with respect to the blue peak. The decrease of the relative ratio between the intensity of the yellow and blue peaks determine a significant shift of the light emitted by the LEDs toward blue. High temperature can alter the properties of the lenses and reducing their transmittance as well.

C. G. Moe et al. [59] showed, for a constant drive current, LED lifetime decreases faster and with greater magnitude when operated at an higher temperature. W. H. Chi et al. [13] observed when the junction temperature of 1 W LED is reduced from 110°C to 25°C, there is close to 40% increase of light output. Derating junction temperature can improve reliability and extend operating life [100] (Fig. 19.9).

M. Arik et al. [6] presents that the light degradation due to thermal issues can occur in the die attach. Both high thermal conductivity and perfect bonding enables the lowest possible thermal gradient in the chip, then help lower the junction temperature.

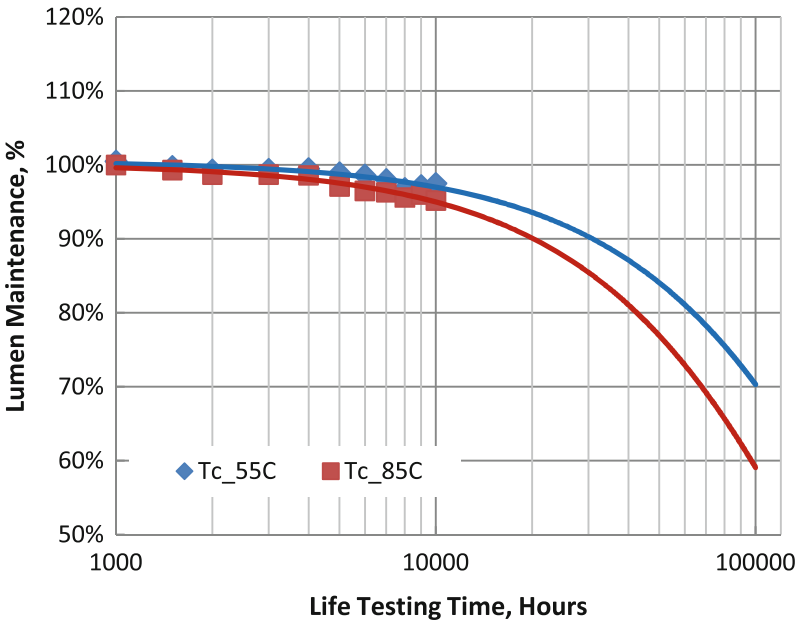


Fig. 19.9 Effect of temperature on LED lumen maintenance

Y.C. Hsu et al. [30] found the key package-related failure modes under thermal aging was the degradation of the plastic lens and lens materials. In addition, a hemispherical shaped plastic lens exhibited a better life time due to their better thermal dissipation than those with cylindrical or elliptical shaped plastic lens.

M. Arik et al. [7] presents the elevated package temperature and local phosphor hot spots are detrimental to phosphor performance. In addition, coating the phosphor on the chip external surfaces will increase the junction temperature but reduced the phosphor temperature when compared to the suspended phosphor case. It also depends on the structure of the package design and thermal patches in the package.

S. C. Yang et al. [104] described the degradation rates of luminous flux increased with electrical and thermal stresses. High electrical stress will induce surface and bulk defects in the LED chip during the short-term aging, which will rapidly increase the leakage current. Yellowing and cracking of encapsulating lens are observed with higher junction temperature while running at the same electrical stress levels. The degradation reduced the light extraction efficiency to an extent that is strongly related to junction temperature and the aging time. The encapsulation lenses exhibited obvious yellowing and cracking under both 0.7A/85°C and 0.7A/55°C conditions. Under the normal aging conditions (0.35A and $T_a = 25°C$), no obvious changes occurred and the luminous flux had only degraded by 6% after 6,180 h. Under the stress of 0.7A/55°C and 0.7A/85°C conditions, the degradation mechanisms both

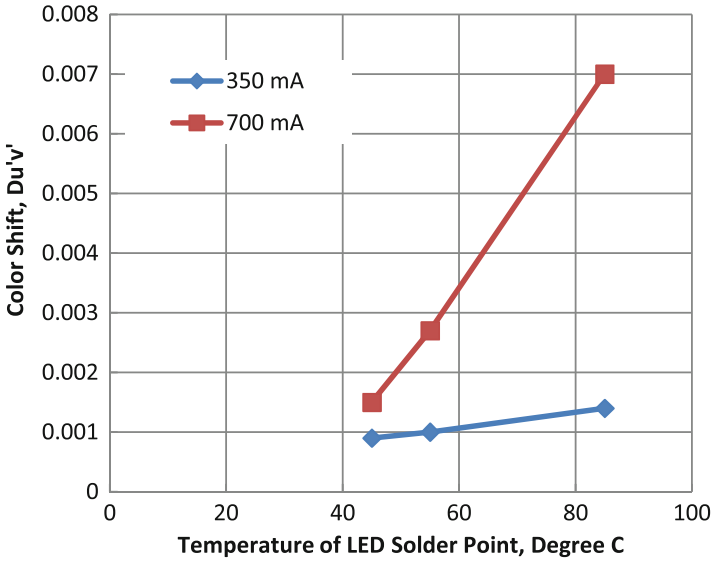


Fig. 19.10 Color shift vs. temperature

involved encapsulant materials and the LED chip, as revealed by the yellowing and cracking of lens and the simultaneous increase in leakage current. The failure of the encapsulated materials is attributed to the applied stress, which influences the chemical bonding of the encapsulation lenses, causing the sensitivity in thermal stability and photo-degradation after long-term burn-in testing. The increase in reverse leakage current also reduced the radiative recommendation efficiency, causing an overall decline in the intensity distribution. The devices under the stresses of 0.7A/85°C and 1A/55°C showed the approximately junction temperature, but they exhibited different failure modes. Under the stress of 0.7A/85°C, samples exhibited two failure mechanisms-chip degradation and package damage. In contrast, under the stress of 1A/55°C, the electrical stress induced by the higher forward current was the major cause of the complete failure of the LED chip.

The chromatic properties of white high power LEDs are strongly affected by high temperature due to the degradation of the package material that determines the decrease of the yellow emission with respect to the main blue peak, as some observations shown in Fig. 19.10. However, improvement can be make to achieve excellent color stability under high temperature and combined with other stress factors, as shown in Fig. 19.11.

– Drive Current

Typically, LED components are constant current driven, the magnitude of constant current will influence the performance and degradation characteristics of the LEDs. The higher the drive current, the higher the luminous flux or radiant power; however, the reliability and lumen and radiant power maintenance could be decreased.

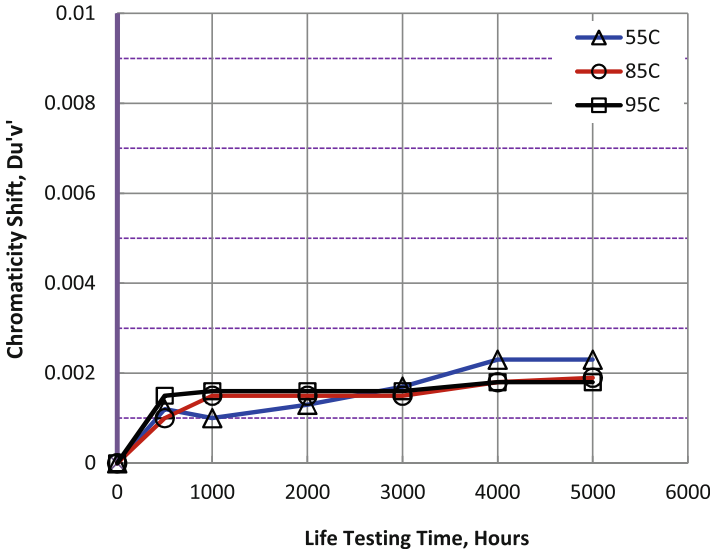


Fig. 19.11 Color stability vs. reference temperature of the LED emitters

M. Meneghini et al. [58, 60, 61] describes the degradation of the operating power of the devices is strongly related to the modifications of the apparent charge profiles, mostly on the region at the boundary between the active layer and the bulk side, often influenced by drive current. M. Vazquez et al. [98] observed drive current is one of the key factors influencing the degradation rate.

With the increase of drive current, assuming the same thermal solution, LED emitters will usually operating at a increased junction temperature, as a result, the packaging materials will degrade faster. The combination of high drive current and high junction temperature could cause catastrophic failures, fused metallization on the die or other failure mechanisms influencing the LED performance. However, the effect of high temperature on LEDs is dominant comparing to that of drive current (Fig. 19.12).

– Thermo-Mechanical Loads

During accelerated stress testing and in field applications, LED components will go through temperature cycling or power cycling. For instance, when the emitters is working, the temperature will be higher and when the emitter is turned off, then the components will be kept in a lower temperature. Thermo mechanical failures are caused by stresses and strain generated within the package or modules due to the temperature changes. In the case of severe temperature cycle, the thermo mechanical deformation leading to device catastrophic failures will result in package or silicone cracking failure, solder fatigue failures, and wire bonding failures. Large package and die size and incompatible packaging materials will imply a worse performance in thermal cycling testing. The higher the temperature range, the worse of the thermo-mechanical performance.

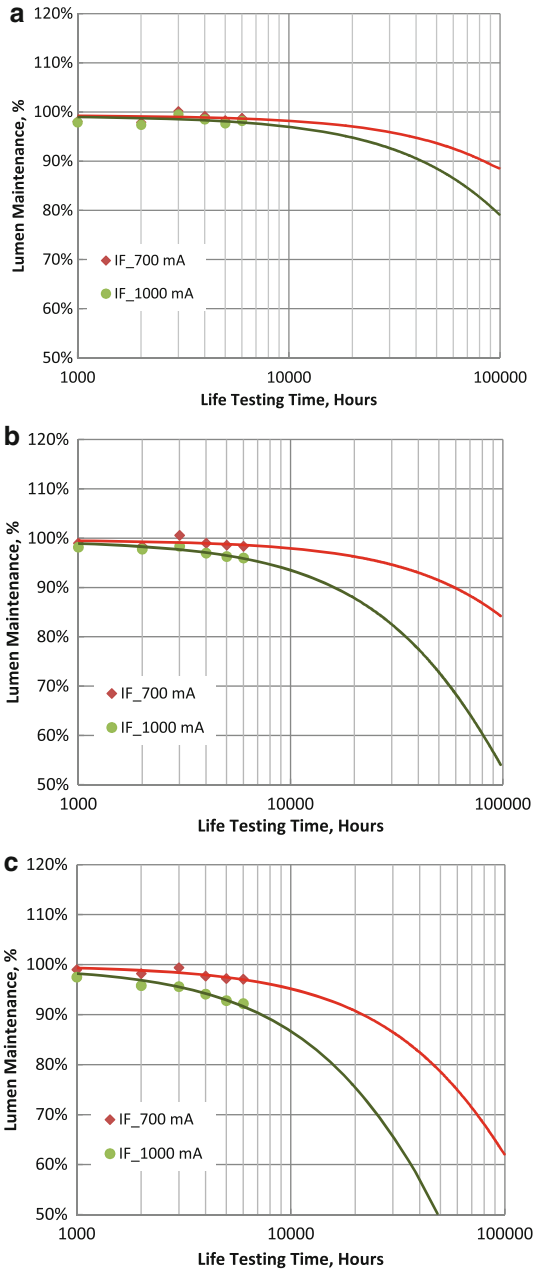


Fig. 19.12 Effects of drive current on LED lumen maintenance. (**a**) *Tc* temperature at 55°C. (**b**) *Tc* temperature at 85°C. (**c**) *Tc* temperature at 105°C

For popular surface mounted LED packages, the solder joint failures due to thermo-mechanical stress load could cause a failure of the LED components. Unmatched packaging materials, especially the encapsulant, die and substrates can introduce thermo-mechanical failures. Thermo-mechanical failures in LEDs are associated with the operating conditions of LEDs, such as drive current, and the temperature of operation.

– Temperature and Humidity

For nonhermetic packages, one of the key stress factors for failures is the moisture contents. The diffusion of moisture into the packaging structure could cause various failure mechanisms, including interface delamination, cracking, corrosion, leakage, and short failures. Combined with elevated temperature, the damage from moisture will be more severe. The moisture contents will increase with elevated ambient temperature, which will affect the performance of phosphor that is deposited around the LED die or on top of LED die. The degradation of phosphor materials will accelerate LED aging and performance degradation.

Moisture penetration paths are most commonly at interfaces, preexisted microcracks, pre-existed delamination, pin holes in passivation, or other defects in the package. Typical contaminants include normal atmospheric pollutants as well process residuals, even packaging materials used, such as soluble chlorides. The key driving stress element in temperature and humidity test is the vapor pressure and density of moisture. The higher the temperature, the higher of the vapor pressure and density for the relative humidity.

X. Luo et al. [57] reported the higher the temperature and relatively humidity (RH%) of the environment, the faster the light efficiency of the LED will decrease. The regression rate of the LED luminous flux is higher at high temperature under the same moisture levels. Delamination failures were observed during the high temperature and high reactive humidity testing.

C. T. Tan et al. [88] found the humidity failure models used for the extrapolation of the lifetime for ICs could not be applied to high power LEDs, it implied that the photonic radiation could contribute to the LED performance degradation under the temperature and humidity conditions.

Wu et al. [103] found that the combination of both temperature and relative humidity played significant roles in causing the light out degradation and interface delamination failures. The humidity could invade into the defect spot on the interfaces. In addition, the pressure caused by the evaporation is large enough to lead to the extension of the crack. The method to roughen the surface of the LED chip might indeed weaken the reliability of the LED packages.

C. H. Chen et al. [11] observed the wire bonding failures and the reduction of thermal conductivity of die attach materials under 85°C/85%RH testing conditions.

C. M. Tan et al. [89] observed two failure mechanisms for high power white LEDs under high temperature and high humidity testing (85°C/85%RH), one is the chip degradation related and the other is the degradation of phosphor, or the combination of the two failure mechanisms. The authors pointed out that Zn activator from the phosphor in LEDs could have diffused out of the packaging

through the moisture path during the accelerated humidity test due to the dissolution of the phosphor. The adhesion strength of the phosphor material on the GaN-based LED is also noted to degrade under the effects of the accelerated humidity test. The dissolution conditions of the phosphor coating are especially noticeable on the edges of the GaN-based LED and are observed to be more severed for LEDs.

C. T. Tan et al. [88] described that sharp degradation of luminous during 85°C/85RH testing was due to the absorption of moisture by the silicone epoxy that caused scattering of light from the die before going out of the packages. High vapor pressure entrapped in the package could also cause die cracking failures. In addition, the dissolution of the phosphor coating on the die contributed to the degradation failure as well. Different reliability models might be needed for LEDs under temperature and humidity testing conditions. Through optimal package design, material section, nonhermatic LED packages can perform as we as a hermetic packages. Many substrate based SMT packages can pass MSL level 1 and HAST/Autoclave testing.

The combination of temperature, moisture, and voltage bias will cause metal migration failures and followed by LED catastrophic failures. The metal migration failure mechanism will happen because of interface delamination which will make it easier to form a conduction bridge. The metal migration coupled with moisture contents at the interfaces will cause short or leakage failures. It has been reported that the combination of temperature and moisture will dramatically affect the chromaticity shift as well, which might be an concern at low moisture environment with high temperature.

– Radiation

It is understood that junction heat would influence the LED degradation. On the other hand, short-wavelength emission will also accelerate the LED degradation [63].

One of the unique features in LED packages is the photonic radiation. During LED operation, both heat and light will be generated. Most of the heat are not radiated, instead of transmitted through a conduction path. Different from IC component, significant portion of the energy are transmitted by light. Photonic energy in the light will cause significant degradation of the package materials, especially the encapsulant materials and phosphor materials in white LEDs.

Figures 19.13 and 19.14 showed the failure mechanism observed in white LEDs and UV LEDs. All the failures are observed after thousands of hours of operating. The damage is likely due to the photoradiation damage on the polymer materials, coupled with heat generated.

The radiation factor posed many challenges for high power LEDs, such as specified UV LEDs. In application, all stress factors could work together against the stability of LED components. The material aging characteristics are not only dependent on the junction temperature but also on the moisture and current density. As the power increase for LEDs, material degradation such as darkening or cracking of the encapsulating, adhesion degradation of die mounting epoxies or optical lenses will limit the lifetime of the LEDs.

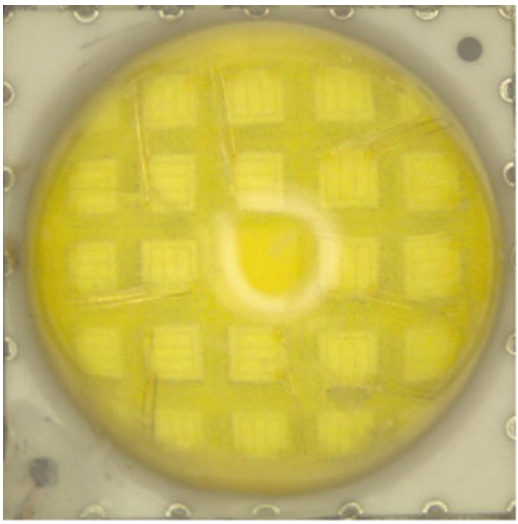


Fig. 19.13 Silicone/phosphor cracking in white HB-LEDs

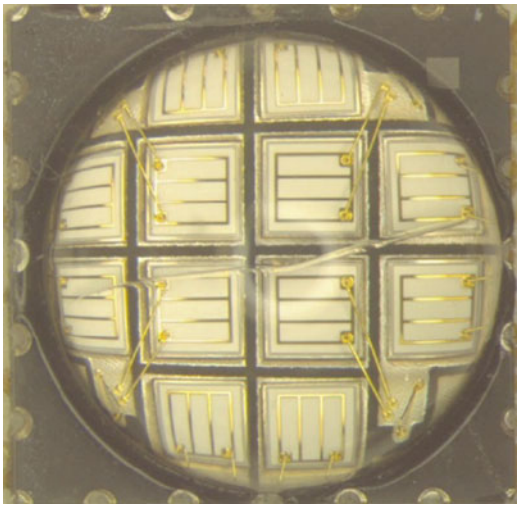


Fig. 19.14 Silicone cracking seen in high power UV LEDs

During the package/product design, all stress factors should be evaluated. Design for reliability and high volume manufacturing activities should be implemented.

19.2.4 Design for Reliability in LED Packaging

With the continuous advancements in LED chip technology, the dominant factors influencing the reliability of HB-LEDs or ultra HB-LEDs have shifted to the LED

packaging technologies, including design, materials, assembly processes and reliability testing. LED packaging techniques provide the electrical connections between LED chip and external circuits and protection of LED chip from mechanical damages, ESD, temperature, chemical oxidation, vibration, and shock. More importantly, good LED packages will enhance light extraction to achieve high luminous flux, help dissipate heat from the chip to increase reliability and life time. Everything from the chip design and fabrication, thermal management techniques, optical design and materials, phosphors materials, and the assembly of the entire package will impact the performance and reliability. Moreover, with the input power increasing, packaging is becoming more critical for the overall system integration and performance. In order to make robust, high quality, and highly reliable LED components, LED packaging technology is holding the key. In this section, the aspect of design for reliability and reliability improvement practices applied in LED packaging will be discussed.

19.2.4.1 Package Materials

The packages materials will dramatically affect the photometric performance and reliability of LEDs, including the long-term lumen maintenance and color shift. Material challenges for HP-LEDs include light extraction efficiency, encapsulant yellowing and cracking, material degradation, interface adhesion degradation, high lumen maintenance, color stability, long lifetime.

Due to CTE mismatch of packaging materials, exposure to high internal temperatures beyond the maximum ratings or repeated thermal cycling can potentially cause different types of catastrophic failures. The temperatures in the package can arise either due to excessive ambient temperature or the junction temperature of LED chip. Significant aging will occur when the temperature is higher than the glass transition temperature (T_g) of the materials.

High power and high brightness LED emitters require materials that will survive high temperatures and high photonic radiation for many thousand hours. In addition, encapsulant and optical materials should have a relatively high index of refraction to maximize light extraction from the LED chip. The packaging material should have significant mechanical stability (hardness, fracture toughness), and be thermo-mechanically compatible. The package should be moisture resistant as well. Moreover, the materials should be easy to handling and a high yield can be achieved for high volume manufacturing.

- Substrate materials

For a typical LED packaging technology, LED die will directly in contact with substrate. Thermal management is critical to reduce the LED junction temperature and expand LED lifetime and performance. High thermal conductivity substrate materials will significantly facilitate the fast heat removal and help lower the LED temperature. Aluminum nitride (AIN) is an effective substrate material due to its excellent dielectric constant (8.6), high volume resistivity and thermal conductivity

(150 W/m K). The superior high temperature and chemical resistance properties made it a useful choice for LED emitters.

Alumina is an alternative material for package substrates. It has similar material properties comparing to AIN, but is in a advantage to reduce the cost, which is critical for companies to survive in a competitive market.

- Die attach materials

High thermal conductivity die attach materials will help reduce the interface thermal resistance, and improve the efficiency of heat dissipation from the LED chip to the heat spreader or substrates.

Solder materials including 80%Au20%Sn are widely used for high power LED emitters. Advanced new die attach materials are also being developed to enhance the thermal dissipation.

X. Li et al. [49] studied nano-silver paste for die attachment in LED packages. Higher thermal conductivity and pure metallic bonds formed by the paste were responsible for the superior performance and reliability comparing to other die attach materials.

Besides high thermal conductivity, die attach materials should be void-free after the assembly in order to minimize the interface thermal resistance. It is even more critical to control the void size and volume for emitters high flux density.

- Interconnects

Most widely used packaging interconnects in today's LED assembly are wire bonding. The bonding wire can fail due to thermal aging and thermo-mechanical loads; however, the failure rate is low, and a lot has been learned from the application experience in IC industry.

Electrical overstress can cause wire bonding failures. When there is a pulse of high electrical load, the input electrical signal could introduce the damage on interconnects.

Wire bond fatigue failure due to thermo-mechanical stress is common wear-out failure mechanism due to CTE mismatch between the encapsulant and the wire and bond surface. Long term exposure to high temperature and high humidity can also cause bond pad corrosion failures. In the future years, flip chip LED chip will be popular in the market. Flip chip LED will provide the advantages of generating more flux, however, flip chip bumps might be subjected to thermo-mechanical failures easily. Au bumps or solder bumps are popular bump materials. The knowledge learned from IC flip chip assembly will help reduce the failure rate of bumps from LEDs, the challenges will be achieving high reliability after exposing to high temperature the LED die will be working under.

- Phosphor materials

One of the most common methods to produce white light LEDs is to use a cerium-doped Yttrium Aluminum Garnet (YAG:Ce) phosphor with Gallium Nitride-based blue LEDs. The phosphor absorbs the short-wavelength emission from the primary LED chip and down convert it to a longer wavelength emission. The inclusion of a small amount of red phosphor with the YAG:Ce or using red die

will improve the CRI to higher than 80 and increase light conversion efficiency. Typically, the phosphor is embedded inside an encapsulant that surrounds the LED die or cover the die top. The type of phosphor materials will affect the photometric properties of LED emitters. In many cases, mixed phosphor materials will be required for a desired color characteristics of emitters.

The absorption and emission spectra of a given phosphor are determined by the interactions between these dopant ions and the chosen lattice. The phosphors must retain their efficiency at high temperatures in order to maximize the lumen output of LED devices under typical operation conditions. More efficient and more stable phosphors with improved aging and characteristics is needed, by the progress in doping activation, particle sizes optimization, particle coatings and even nano-dots. Reducing phosphor thermal quenching is a focus within the industry.

The light extraction of the package depends on phosphor materials, such as particle size, conversion efficiency, phosphor geometrical placement, and phosphor concentration. As phosphor concentration increases, the overall photon scattering is expected to increase and such an increase in scattering may eventually lead to the photon trapping and absorption by the LED package and LED die. In addition, with the phosphor concentration increase, more heat will be built up inside the package, which is not a good thing. With mixing of varies type of phosphor materials, the CRI of the light could be changed significantly.

Phosphor-converted white LEDs degrades faster than the similar type of blue LED because of the presence of phosphor materials.

J. You et al. [105] reported the light out of LEDs with higher phosphor concentration was having a larger degradation in constant current compared with pulse current that with lower phosphor concentration. The junction temperatures of phosphor-converted white LEDs raised with an increasing phosphor concentration, then with a decreased phosphor conversion efficiency both in pulse and constant current. As the wt.% of phosphor increased, the optical power, CRI, and CCT decreased. However, a decreasing trend of luminous efficiency was observed when the phosphor concentration was over a threshold. There was an optimum luminous efficiency point for different LED packages. The chromaticity coordinates of white LEDs could be adjusted by changing the phosphor wt.% in the package [50]

Z. Y. Liu et al. [53] pointed out that conformal phosphor coating was not a favorable packaging method for desired color binning. Planar remoter phosphor improved the brightness level and its consistency. Moreover, hemispherical remoter phosphor could fulfill the requirements of both high color consistency and high brightness consistency due to its capability of larger variation ranges of the phosphor thickness and concentration.

Chun-Chin Tsai et al. [90] showed the lumen loss, chromaticity, and spectrum intensity reduction increased as the concentration of Ce:YAG phosphor-doped silicone increased. Silicone degradation was attributed to the final thermal degradation, however, was not a dominant factor until a much thicker layer of silicone was employed. The major degradation mechanism of the pc-LEDs resulted from the higher doping concentration of Ce:YAG in silicone. A lower doping concentration of the Ce:YAG phosphor in thin silicone was a better choice in terms of having less

thermal degradation for use in packaging of the high power pc-LEDs modules and was essential to extend the operating lifetime of the phosphor-based white LED modules.

Phosphor materials are critical to generate various white light, on the other hand, they also post significant challenges for the reliability and life time of SSL products. It is one of the critical areaes for breakthrough in order to enhance the adoption of LED technology in general lighting applications.

- Encapsulant materials

Encapsulant materials can both provide physical protection of the chip and interconnects and enhance the optical efficiency. Comparing to epoxy resin, silicone materials have excellent thermal flexibility and light resistance characteristics. It can reduce the yellowing or darkening issues of conventional epoxy type encapsulants in many applications. J. Emerson et al. [22] reported that silicone coating materials showed excellent HAST performance for preventing corrosion failures. However, silicone materials has a very low viscosity, and are much harder to be applied in manufacturing process.

Encapsulant materials in LED packages can suffer from thermal- and radiation-induced degradations and then lead to failures. The degradation rate of the encapsulation materials depends on the temperature of LEDs. In the case of poorly designed LED packages, the junction temperature will rise rapidly, finally lead to adhesive thermal fatigue, phosphor conversion efficiency decrease, epoxy resin carbonization, and yellowing even cracking. Material yellowing/darkening and cracking are the most severe failures associated with encapsulant in high power LED packages. The yellowing of encapsulant will result in a significant loss of light output over time. For UV LEDs, high temperature, coupled with radiation with wavelength less than 300 nm significantly contribute to the yellowing of encapsulant and cracking of encapsulant materials.

Z. Wu et al. [101] found the light transmittance of epoxy resin encapsulant decreased significantly, especially in UV wavelength range. It suggested that silicone encapsulant was more suitable for LED packaging especially for LEDs wavelength less than 380 nm.

Lin et al. [51] found the degree of yellowing phenomena could be judged by the loss of the transmittance of the encapsulant. The authors observed that different encapsulant material could dramatically affect the lumen maintenance of the LEDs under UV or thermal aging or 85°C/86%RH ambient conditions. Optical grade epoxy showed much better delamination resistance than silicone under 85°C/85% RH conditions for 500 h. However, high RI-silicone had better lumen maintenance than optical grade epoxy.

C. C. Tsai et al. [91] demonstrated higher thermal stability of high power phosphor-converted white LEDs by incorporating a Ce:YAG-doped glass as the phosphor layer. The results showed the high power PC-WLEDs with 6 wt.% of Ce:YAG-doped glass exhibited 60% less lumen loss, 50% lower chromaticity shift and 20% smaller transmittance loss than with the Ce:YAG doped silicone, subjecting

the parts to 500 h operating at 150°C. When there was a degradation of the reflective properties of the package takes place, in turn it leads to a decrease in intensity of the emitted light. Silicone materials used for LED demonstrated these key features, including:

1. Excellent UV stability and cause non/less yellowing.
2. Excellent thermal stability
3. Very low moisture uptake, typically less than 0.2%. Package conform to JEDEC level 1 handling.
4. Low Young's modulus. Materials is able to absorb stress due to CTE mismatches in the package.
5. Good adhesion to varieties of materials.
6. High purity and excellent optical properties. Well suited for IR, visible, or UV optical applications.

19.2.4.2 Assembly Processes

During LED package assembly, key assembly modules should be optimized and monitored to make sure the LED packages will be build with high quality and high yield, which will be reflected on their high reliability. G. Lu et al. [55] discussed bubbles in encapsulant materials could cause LED to decay quickly, die attachment cracking would likely make LED be dimmed because of the impact of cracking on thermal performance. The thermal stress that produced during temperature intensive processes make the active region further deteriorated. Table 19.4 shows LED package-related failures related to package assembly.

In the following section, key assembly modules will be discussed, organized as interconnects, die attachment processes, encapsulant dispensing/molding, and curing as well as lens attachment.

- Interconnections

Wire bonding is the most widely adopted form of first level interconnections in LED packaging. It is reliable, flexible and low cost. During the wire bonding process, the process conditions are controlled by wire types and diameters, bond pad metallization, and device configurations. In LED assembly, poor electrode bonding quality may cause uneven current diffusing and local overheating in the chip, which may lead to significant drop of luminous efficiency and accelerate contact degradation even catastrophic failures.

Evaluation of wire bond pull strength is used to assess the quality of the wire bonding process. Gold wires have been the dominant material used for the ball bonding process. The automated bonders together with improvements in bond pad metallurgy, reduction in unwanted impurity content, more effective pad cleaning processes, stable die attach adhesives, and reduced temperature bonding processes have contributed to the reliability.

Table 19.4 LED package assembly-related failures

Package elements	Defects/failures	Root causes and potential damages
Die attach	Excessive voids	Voids can lead to higher thermal resistance and higher LED junction temperature. Failures associated with excessive voids include die attach cracking during temperature cycling and thermal shock, burned LED die, faster lumen degradation, and light out failures. The root causes for die attach voids include oxidation of bonding surfaces, nonwetting, die attach materials and processes and out gassing.
	Die cracking	Die microcracking can lead to die fracture during temperature cycling and thermal shock. Catastrophic failures in application can be seen. Die cracking can be caused by Locally higher stress induced by a CTE mismatch between the chip and the package, die attachment processes, saw-and-break method used in die separation processes.
	Interface delamination	Interface delamination can cause catastrophic failures and light out failures. The delamination can result from surface contamination, excessive temperature, high humidity and material degradation.
	Incorrect die attach thickness and die attach materials	The defects can result in higher thermal resistance with higher BLT. High junction temperature will cause light output degradation and ultimate LED catastrophic failures.
Bonding wires	Bond pad cratering	Cratering will reduce the strength of the die and wire bonding. It is due to incorrect bonding parameters or set-up procedures.
	Incorrect bond placement	The defects will cause short circuits or crossed wires. It can be caused by poor design and/or inadequate process control.
	Excessive intermetallics	Excessive Intermetallics may weaken the interface bonds and cause bond failures. The growth of the intermetallics can be attributed to excessive high temperature, long operation lifetime, as well as the bonding materials.
Bump failures (flip chip)	Intermetallics	UBM materials and plating materials, external temperature, and compatibility of bump materials all contribute to the growth of intermetallics.
	Corrosion	High humidity and high temperature will accelerate corrosion failures. Moisture contents will be a key contributor.
	Fatigue failures	Thermo-mechanical stresses during the operation will put the bumps under stress. Structure and the compatibility of the materials will play key roles too.
Encapsulant	Cracking	

(continued)

Table 19.4 (continued)

Package elements	Defects/failures	Root causes and potential damages
		Thermo-mechanical stresses, elevated temperature, photonic energy can introduce cracking. Delamination and voids from manufacturing processes can be the starting points.
	Delamination	Surface contamination, outgasing, interface degradation and contamination all contribute to delamination failures. In some cases, delamination can be introduced by moisture contents and elevated temperature.
	Yellowing/browning	Elevated temperature and high current are the key factors.
Substrate	Cracking	Thermal shock and thermal cycling introduced thermo-mechanical stress.
	Corrosion	Contamination, moisture and voltage bias
	Solder joint failures	Thermal cycling and thermal shock stress; meta migration failures and solder volume.
Lead frame	Corrosion	Moisture and voltage bias load.
	Solder joint failures	Thermal cycling, process variation and solder volume control.

Some of the typical problems in wire bonding include mechanical wire fatigue due to conditions of thermal or power cycling, interactions both chemical and mechanical with encapsulation during molding and curing, corrosion induced by the die attach material, process-related contamination; and wire structural changes.

The wire bond reliability is associated with the alloying reactions that occur at the gold wire-aluminum alloy bonding pad interface. Aluminum–gold intermetallic formation occurs naturally during the bonding process and contributes significantly to the integrity of the gold–aluminum interface. Intermetallics are generally brittle and may break due to metal fatigue or stress cracking, then result in bond failures. Excessive intermetallics growth can lead to the coalescence of voids, which then lead to a bond crack or lift and an open circuit. Impurities in the bonding wire, on the pad metallization, or at the wire–bond pad interface have been shown to cause rapid intermetallics growth and kirkendall voiding.

Cratering can be a significant problem associated with the bonding and subsequent shearing of ball bonds. Intermetallic formation, bonding stress, metallization thickness, and underlying dielectric layers have all been noted to have impacts. A flatter bond with a larger weld area is less prone to produce silicon cratering when shear tested [54]. Gold–gold or aluminum–aluminum, have been shown to be more reliable in high temperature applications.

F. Wu et al. [102] observed LEDs were seen degrading dramatically in usage when the bonding interface has less than 10% intermetallics region compared to the pad surface. White LED aged quickly and caused aging failures.

- Die attachment

To dissipate the amount of heat generated during the LED application, the LED die needs to be bonded to a heatsink or substrate with high thermal conductivity, often using solder materials such as AuSn. If there were voids in the solder attach and it created an insufficient thermal path, the resulting hot spots would eventually lead to thermal runaway and failures. In addition, Whisker growth caused by electromigration, which can come from internal strain, temperature, humidity, and material properties can lead to electrical short circuits. In choosing the die attach materials, the following should be considered:

(a) Stress relaxation at the interface
(b) Excellent adhesion between the bonded surfaces
(c) Effective heart dissipation as well as high thermal conductivity
(d) CTE matching materials between the bonded surfaces
(e) Help achieve void free assembly process.

Building a defect free chip is a major challenge, but furthermore, placing it in a reliable package brings more mechanical and operational challenges. Both high thermal conductivity and perfect bonding interfaces enables the lowest possible thermal gradient in the chip. The chip to the submount should be void free. It is necessary to strength the inspection of chip, lead frame and substrates, and silver filled die attach material before the die attachment process. Chip pad should be clean and pollution free and complete without breakage, lead frames and substrates should not be rusty and deformed.

The reliability of LED strongly depends on the die attach quality since any voids or small delamination may cause instant temperature increase and lead to later failure in operation. H. H. Kim et al. [46] found thermal transient simulation of die attach characteristics was a useful method to represent the thermal behavior of high power LED packages.

- Encapsulation dispensing/molding and curing processes

The application of silicone encapsulant in LED packages are usually through dispensing or molding techniques. The silicone alone or mixture of silicone and phosphor will be dispensed to seal the die, even form desired lens shape. The implementation of silicone dispensing or molding processes are complicated depending on the structure of the package design, the viscosity of the materials and equipment used. Phosphor setting might cause change of the conversion efficiency and should be controlled in LED packaging and assembly. During the dispensing or molding processes, there could be bubbles entering into the interfaces or in the mixture of silicone and phosphor, the bubbles will significantly decrease the optical efficiency of the LED because of the refractive index changes among too many interfaces.

Silicone curing can significantly influence the internal stress generated during the process, as well as the subsequent reliability of the LED packages. Step curing is

usually implemented to reduce the stress build-up to achieve high reliability in field applications.

- Surface mounting design and reflowing processes

Solder paste are typically used to mount the device/components on MCPCBs for LEDs. The solder bonding action is initiated by intermetallics compound formation, which is chemical reaction. There are two fundamental properties that a solder must possess in the application.

1. The solder must wet the surface.
2. The metal comprising the surfaces must be soluble in the molten solder. The solid solubility coefficient of the metal in the solder must be finite and greater than zero.

In general, the Sn in the molten solder reacts with Cu to form intermetallic compound (IMC), often known as wetting action. Without IMC, a soldering process could not be successful. The purpose of the flux is to reduce the oxide and to shield both solder and base metal against oxidation. Solder paste stencil aperture openings can be 1:1 with the peripheral PCB pad sizes. However, the stencil aperture opening should be smaller than the large PCB exposed pad regions to reduce the chance of solder bridging. The reliability of the solder joints can be improved by forming the right shape of solder fillets. Some of the factors that can significantly affect the mounting of LED packages on the boards and the quality of the solder joints are listed here

(1) Amount of solder paste coverage in the pad region.
(2) Stencil design.
(3) Surface finish of the package pads and contacts.
(4) Types of solder paste.
(5) Reflowing profile which have a strong influence on void formation as well.

SnAgCu (SAC) is the most prevailing alloy family for lead free soldering. Its hardness, tensile strength, yield strength, shear strength, impact strength, and creep resistance are all higher than eutectic SnPb. However, its wetting is poor than eutectic SnPb.

Factors that will minimize the thermo-mechanical stress include

1. TCE match: the amount of stress generated in a component is directly proportional to the difference in TCE between the component and the substrate.
2. Bond thickness: an increase in bond thickness contributes to a reduction in stress on the die by having a greater ability to flex when a force is applied. The principle is commonly employed by increasing the thickness of solder joints.
3. Bonding voids. Small voids in the bond distributed over the area of the die reduce the stress. However, voids in the bond area increase the thermal resistance and consequently, the temperature of the die, which counters the positive effect. Large voids tend to concentrate the stress at the point of bonding and increase the probability of cracking.

4. Compliant bonding materials. The use of a compliant bonding materials, such as a soft solder or epoxy, enables the bond to absorb much of the stress, minimizing the stress on the die.
5. Processing temperatures. Selecting materials for minimum processing temperature has a dramatic effect on stress reduction as the stress is initially applied at the time the bonding material is solidified or cured.

In order for the solder joint to form, both the surface and the solder must be clean and free from oxides.

19.2.4.3 Package Design

A good and reliable LED product will start with a reliable package design. The package should have low thermal resistance, thermo-mechanically stable, high efficiency for light conversion, and be highly reliable.

During the package design process, the following aspects should be considered.

- Heat removal capability

The key is for a good LED package design is to present a low thermal resistance, so the heat generated can be removed as fast and efficient as possible. The package will use high thermal conductivity materials, as well as optimized thermal conduction path.

- Phosphor application

In white LED packages, phosphor materials can significantly absorb the heat during the light conversion process. The heat in phosphor should be conducted away as soon as possible, otherwise, the consequences will be increased junction temperature and reduced light extraction efficiency.

Phosphor materials can be applied only on the die top, or immersing the die or on remoted surfaces. Narendran et al. [62] demonstrated that the phosphor layer closer to the die would cause the LED degrade faster; however, the authors found it was better to have the phosphor as close to the die top as possible, then the heat generated could be conducted away in unique designed packages.

When the phosphors are only applied on the die top, there is a risk of potential lumen degradation if there were cracking or darkening in the silicone materials on the die top. In mixture phosphor in cup process, the risk of sudden lumen flux degradation is lower, since there are phosphor materials around the die which will help generate luminous flux. This phenomenon has been observed in a configuration with multiple die in single LED packages.

- Substrate design

Substrate design is one of the most important elements to assure high reliability of LED components and luminaries. The substrate materials should be highly thermal conductive, in addition, thermo-mechanical stress is low.

In today's high power LED packages, ceramic substrates are widely used because of their thermal conductivity and thermal stability. However, bench marking tests showed the performance of different design of substrates could be significantly different. The dominant failure mechanism is substrate cracking. The substrates should be thermally matched to other materials in the packages, in addition, the thickness and the size should be optimized. There are also many techniques to design a multiple layer substrate which is more flexible to handle the lighting design.

- Compatible packaging materials

The packaging materials should be thermally compatible so that thermo-mechanical stress generated during testing or operation can be minimized. A strong bonding among the package interfaces will prevent interface delamination. The waken interfacial strength in the LED structure is one of the reasons for the reduction of optical efficiency and reliability.

- Thermal stability of lenses

LED packaging will be equipped with either built in lenses or secondary lenses to optimize the light extraction efficiency or increase of luminous flux. Because of the high temperature the lenses will be indulged in the risks of failure for lenses are very high.

The lenses should be thermally stable. Glass lenses will be preferred to handle the extreme temperature conditions during LED operation.

Y. C. Lin et al. [50] studied the performance of flat-top (FT) emitters and flat-top-with-lenses (FTWL) packages. Due to the TIR at the encapsulant to air interface, FT packages showed a 10% power reduction comparing to FTWL. However, at the same phosphor concentration level, FT packages provided a more efficient way of utilizing phosphor than FTWL packages based on the same target chromaticity coordinates, resulting in a reduced phosphor usage with a similar lumen output.

- Design-for-manufacturing

LED packages should be designed so high volume manufacturing can be implemented with high yield and high quality. Design-for-manufacturing can improve the quality and reliability in the field application.

19.2.5 LED Reliability Testing Methods

Reliability predictions are based on testing a small number of samples of the general population. One of the most commonly used approaches for testing products within stated constraints is accelerated life testing where products are subjected to more severe stress conditions than normal operating conditions. Significant degradation data can be obtained by observing degradation of a small

number of products over time. In some ways, LED packages are similar to IC packages, so much knowledge learned in IC packages can be applied in LED packaging so potential failures can be reduced or removed. However, there are significant differences between IC packages and LED packages, which is driving the development of new testing standards/methods.

19.2.5.1 Reliability Testing and Qualification

Reliability testing and qualification are essential to achieve high reliability products. During the practice, stress tests are applied to reproduce the failure modes that would be observed on field applications. In addition, it should be reminded that test methods applicable to lower power LEDs might not be applicable for high power LEDs, which is more challenging as expected.

Qualification of emitters means to confirm their fitness for use as a result of appropriate processes for their realization, which includes (1) verification of their function and performance and (2) validation in the system. The type of tests listed in Table 19.5 are widely applied in the industry. However, different manufacturers might adopt different test conditions. For instance, manufacturers might qualify the parts using WHTOL at 60°C/90% instead of 85°C/85%RH. Other manufacturers might use cyclic WHTOL in stead of continuous WHTOL testing.

Reliability testing is usually performed to determine if devices have any fundamental reliability-related failure mechanisms, which can be divided into four main groups, including

1. Process- or die-related failures, such as oxide-related defects, metallization-related defects, and diffusion-related defects.
2. Assembly-related defects such as wire bonding or package-related failures.
3. Design-related defects.
4. Miscellaneous, undetermined, or application-induced failures.

In order to effectively implement reliability tests and qualify the conformance of the components, first of all, the target failure mechanisms should be documented, then the stress factors that will activate the failure mechanisms should be applied to accelerate the failure mechanism through accelerated stress testing in order to shorten the test duration and reduce the design cycle.

In general, the degradation of color stability and luminescence of LEDs has been investigated using long-term aging or operating methods. The driving stresses include drive currents, temperature, temperature changes, and relative humidity. For white LEDs, both phosphor degradation and chip defects can be inferred from variations in the power spectrum and changes in the voltage characteristics when applying the loads.

Besides reliability testing methods which will test design defects or manufacturing defects, there are additional testing methods available for evaluating the LED photometric performance, as shown in Table 19.6.

Table 19.5 Lists of reliability tests which are conducted for LED components, arrays, and modules

Number	Test types	Test standards	Test conditions
1	High Temperature Operating Life	JESD22-A108C	Ambient 85°C; derated Max I_F based on data sheet; for 1,000 h
2	Room Temperature Operating Life testing	JESD22-A108C	Ambient @ 25°C; Max I_F based on data sheet; for 1,000 h
3	Low Temperature Operating Life	JESD22-A108C	Ambient @ −40°C; Max I_F based on data sheet; for 1,000 h
4	Wet High Temperature Operation Life	JESD22-A101C	Ambient @ 85°C/85 %RH; I_F should be determined based on power dissipation of the emitters; for 1,000 h
5	Temperature Cycling	JESD22-A104D Condition G	Temperature range @ −40°C/125°C; 20 min dwell and 5 min ramp; 1,000 cycles
6	Thermal Shock	JESD22-A106B/ MIL-STD-202G 107G	Temperature range @ −40°C/125°C; 20 min dwell and <20 s transition; 500 cycles
7	High and Low Temperature Storage	JESD22-A103C Condition B	150°C or −40°C; nonoperating for 1,000 h
8	Mechanical Shock	JESD22-B104C Condition B	1,500G, 0.5 ms pulse, 5 shocks each 6 axis
9	Variable Vibration Frequency	JESD22-B103B	10-2000-10 Hz, log or linear sweep; 20G for 1 min, 1.5 mm, each applied 3 times per axis over 6 h 10-55-10 Hz, ±0.75 mm excursion, 55–2,000 Hz, 1 octave/min, 10G, 3 times per axis
10	Random Vibration	JESD22-B103B	6G RMS from 10 to 2 KHz, 10 min per axis
11	Solder Heat Resistance	JESD22-B106D JESD22-A111	260°C for 2 min; 3 times
12	Solderability	JESD22-B102E Condition D	Steam age for 16 h then solder dip at 245°C for 5 s
13	Salt Atmosphere	JESD22-A107B Condition A	35°C for 48 h; salt deposit 30 g/m^2/day
14	ESD (MM and HBM)	JESD22-A115B JS001	8 kV, Class 3B or 2 kV (Class 2).
15	Autoclave	JESD22-A102-C	121°C/100%RH at 2 atm. pressure for 96 h
16	IPC/JEDEC Moisture Sensitivity Levels	J-STD-020D.01 JESD22-A113	Level 1: 85°C/85 %RH, 3 times reflow with peak temp at 260°C
17	Lumen Maintenance	IES LM-80-08	Case temperatures at 55, 85, and third temperature.

IESNA LM-80-08 prescribes uniform test methods under controlled conditions for measuring LED lumen maintenance and color shift while controlling the LED's case temperature (T_s) using continuous mode operation for a specified minimum duration. LED packages, arrays, or modules are tested over time at a minimum of

Table 19.6 LED photometric testing standards and documentation

Performance characteristics	Reference standards	Required documentation
Luminaire efficacy; light output; input Power	IESNA LM-79-08 ANSI C82.2-2002	Test reports from a laboratory accredited by NVLAP or one of its MRA signatories
Lumen maintenance testing of LEDs	IESNA LM-80-08	Test reports from a laboratory accredited by NVLAP or one of its MRA signatories
Long-term lumen maintenance life projection for LEDs	IES TM-21-11	IES Technical Memorandum—a method of projecting long-term lumen maintenance of an LED light source based on 6,000 h of lumen depreciation data collected per LM-80-08
Color rendering index	ANSI C78.377-2008 IESNA LM-79-08 CIE 13.3-1995 IESNA LM-58-94	Test reports from a laboratory accredited by NVLAP or one of its MRA signatories
Chromaticity and correlated color temperature	IESNA LM-79-08 CIE 15-2004 IESNA LM-58-94 IESNA LM-16	Test reports from a laboratory accredited by NVLAP or one of its MRA signatories
Eye safety testing	IEC 62471	Photobiological safety of lamps and lamp systems. It provides a risk group classification system for all lamps and lamp systems. The assigned risk group of a product maybe be used to assist with risk assessments
Color spatial uniformity and color maintenance	IESNA LM-79-08 CIE 15-2004 IESNA LM-58-94 IESNA LM-16	Self-certification
Maximum measured power supply case or manufacturer designated temperature measurement point temperature	ANSI/UL 153 UL1598	Lab test results must be produced
Safety	ANSI/UL153 UL 1598 UL 8750	Provide the cover page of a safety test report or a general coverage statement from an OSHA NRTL Laboratory

three discrete case temperature, 55°, 85°C and a third chosen temperature. During lumen maintenance testing, LED is allowed to cool to room temperature and tested at air temperature of 25°C. However, LM-80 does not specify pass and fail criteria, and LM-80 does not provide guidance for estimating or extrapolating lumen maintenance collected.

TM-21-11 is an IES technical memorandum and intended to be a companion to LM-80 test method. It specifies how to extrapolate the LM-80-08 lumen

maintenance data to times beyond the LM-80 test time. It will help project long-term lumen maintenance of an LED light source based on 6,000 h or beyond of lumen depreciation data collected per LM-80. It creates a common playing field for LED competitors to specify lumen maintenance behavior for their white LED products intended for illumination applications. Extending the time period of observations will provide improved predictions of the L70 life.

The methods can be briefly described as follows

1. Normalize all data to 1 at zero hours
2. Average each point for all samples of the device for each test condition. Suggested minimum samples size is set at 20 for each given temperature and drive current.
3. Early measurement before the LED has "warmed-up" should not be included in the modeling. In general, test data beyond 1,000 h are used for analysis since later data shows more characteristic decay curve. Later decay is chip driven and relatively consistent with exponential curve. In addition, verification with long duration data sets shows better model to reality fit with at 5,000 hour of 10,000 hour data. For 6,000 hours of data and up to 10,000 hours, the last 5,000 hours data will be used for analysis. Uncertainty will be reduced in the prediction when using the full data set.
4. Apply exponential least square curve fit $\varphi(t) = B\ \exp(-\alpha t)$. B and α are constants derived by the least square curve-fit. Time t is in hours and $\varphi(t)$ is averaged normalized luminous flux output at time t.
5. Lumen maintenance "life" can be projected as $L_p = \ln(100 \times B/P)/\alpha)$

Where L_p is lumen maintenance life in hours where p is the maintained percentage of initial lumen output.

However, the lack of standardization for high power LED reliability and prequalification testing is still lacking. Every qualification test must have acceptance criteria, optimized test conditions and duration for use conditions. In general, no single part is allowed to show luminous flux degradation of greater than 10% for RTOL and HTOL or 15% for WHTOL after 1,000 hour's testing. Some suggests to have no more than 0.2 V forward voltage shift during the test duration as well. Long-term maintenance testing should be conducted for qualified products to understand the useful life in the application fields.

Manufacturers can choose appropriate test methods to qualify their products. On the other hand, the test methods used should warrant a reliable products and confidence of the products.

19.2.5.2 Reliability Prediction for LED Components

Life time and failure rate prediction are key purposes of reliability testing. Reliability assessment and prediction will require an appropriate degradation model, a carefully designed test plan and insightful investigation of the field operating environment in order to achieve high accuracy of reliability estimates. An appropriate decay model is the one that accurately interprets the effects of

the stresses on the decay process of a product based on its physical properties and the related probability distribution.

In reality, even if LED could last for a long time, its lumen output will diminish over time to a point where they would no longer function as a useful lighting source. In addition, catastrophic failures do happen in LED industry; however, the failure rate is low.

- Failure rate

For reliability analysis, failures can be defined as catastrophic failures or performance failures. It has been reported that the light output decrease overtime is exponential in nature. However, different decay constant for different LEDs may be yielded. The exponential decay of light output as a function of time provided a convenient method to rapidly estimate life by data extrapolation.

In order to predict the failure rate, the following lighting failures can be considered.

1. All LED light up, but at a reduced light level
2. One or more catastrophic LED failures, but the light level is maintained.
3. There is a single or multiple catastrophic LED failure, perhaps running at a reduced light level
4. No LEDs light up, due to system failure other than the LED.

The failure rate models based on a constant failure rate, failure in time (FIT), can be calculated as

$$\mathrm{FIT} = \frac{\chi^2_{2n+2}}{2\mathrm{AF}Nt} \times 10^9, \tag{19.1}$$

Where

χ^2 is Chi-square value;
n is the number of failures
AF acceleration factor
N total number of failures
t total testing time

Mean-time-to-failure of LED components could be defined as the point in time at which 50% of the components have failed (including catastrophic failures or parametric failures). It is considered as a reverse of failure rate with the assumption of a constant failure rate.

- Acceleration Models

Life models can be obtained by applying regressive techniques to time-to-failure data collected under applied stresses and are ideally based on physical failure mechanisms. Without a physical model, the use of accelerated testing will be hindled. Once the life model is available, it can be used to predict reliability.

A statistical model for an accelerated life test consists of (1) a life distribution that represents the scatter in product life (2) a relationship between life and stress. Typically the mean of the life distribution is expressed as a function of the accelerating stress factors. The most widely used relationships are Arrhenius relationship for temperature-accelerated tests and the Inverse Power relationship for temperature change, current, or voltages.

– Arrhenius models

The Arrhenius-based models have been used to predict the influence of temperature on device reliability for long time. For LED components, the model is typically used to account for the temperature effect on decay rate constraints. IES TM-21-11 reported the estimated lifetime using an exponential fit is reliable when the initial 1,000 h of data is omitted and a minimum of 5,000 h of data beyond the initial 1,000 h is used.

According to Arrhenius rate law, time t to failure can be expressed as

$$t = A\exp\left[\frac{E_a}{kT}\right] \tag{19.2a}$$

Where A is the constant that depends on product specifies, such as geometry, size and fabrication and test methods.

The AF expression using Arrhenius model which only consider the impact from temperatures is shown in (19.2b). Users should be cautious when applying generic activation energy standards to new technologies. However, the use of an activation energy to describe a device failure rate is complex, but misleading sometimes. It was observed that the activation energy for any given failure mechanisms will vary over a wide range and depend on many factors, including materials, geometries, manufacturing processes, and controls.

$$\mathrm{AF} = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_a} - \frac{1}{T_t}\right)\right) \tag{19.2b}$$

Different LEDs might have significantly different life values [64]. M. Vazquez et al. [98] obtained the activation energy for AlInGaP LED degradation failure mechanisms is 1.2–1.5 eV.

Although Arrhhenius model are considered a accurate description of delay of LED components, there is not much data available. In the future, there is a need to collect more data, especially for high power LEDs in order to predict the life more accurately. There may be a need to choose an accelerating variable and to develop and verify an appropriate model. The work will involve long-term efforts.

– Inverse Power Model

The Inverse power relationship can be used to model product life as a function of an accelerating stresses factors other than temperature. The relationship is empirically adequate for many products modeling.

The inverse power relationship between life t of a product and stress V is

$$t(V) = A/(V^{-n}).$$

Both A and n are parameters characteristics of the product, samples, geometry, and manufacturing processes and test method.

The acceleration models using Inverse Power Relationship can be expressed as

$$\mathrm{AF} = \left(\frac{V_t}{V_u}\right)^n.$$

The acceleration from current and humidity can be model by the Inverse Power law.

– Combination Models

For nonhermetic packages, the combination of high temperature and high relative humidity plays an essential role in its reality. Available models assume that during thermal humidity bias test, the failures induced by temperature and by RH are fully independent and acceleration factors can be expressed as AF = AF (T), AF(RH).

J. Gao et al. [25] successfully estimated LED life time based on Arrhenius acceleration models and the RH acceleration, shown as

$$\mathrm{AF} = \left[\frac{\mathrm{RH}_t}{\mathrm{RH}_u}\right]^3 \exp\left[\frac{E_a}{k}\left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right] \tag{19.3}$$

In other models, the exponent for RH term is using 2 instead of 3.

K. String and Schelling [84] developed the following model more appropriate for Aluminum corrosion failure mechanism, shown as:

$$\mathrm{AF} = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_u} - \frac{1}{T_t}\right) + \beta\left[\frac{1}{\mathrm{RH}_u} - \frac{1}{\mathrm{RH}_t}\right]\right] \tag{19.4}$$

P. Bojta et al. [8] found that 85°C/85%RH test had higher thermal acceleration factor while its humidity acceleration was lower than that of 40°C/95%RH. The likelihood of moisture condensation depended on the RH in the environment, the temperature difference between the condensation surface and environment, the pressure and the surface roughness. A number of potential failures were revealed in 40°C/95%RH but hidden in 85°C/85%RH conditions.

If considering the impact of current, a current factor in the life model can be added based on the time to failure data with the supplying current. Most common models used for nonthermal stresses are Inverse Power Model with nonlinear fitting [1], where

$$\mathrm{MTTF} = \mathrm{AI}_F^{-n},$$

the acceleration model considering the influence of current, temperature, and humidity can be written as

$$\mathrm{AF} = A\left[\frac{I_t}{I_u}\right]^m \left[\frac{\mathrm{RH}_t}{\mathrm{RH}_u}\right]^3 \exp\left[\frac{E_a}{k}\left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]. \tag{19.5}$$

Both the impact of drive current and relative humidity should follow a power law relationship.

It should be reminded that if the acceleration condition is too serious, entirely new failure modes can be introduced, which might not be a realistic failure mechanism in the field application.

- Life stress relationships

A simple life stress relationship does not describe the scatter in the life of the produst. For each stress level, the products share statistical distribution of life. The refined life stress model should consist of a combination of a life distribution and a life stress relationship. For LED products, the distributions can be typically described by exponential and weibull distributiones. Several life stress models will be appropriate to depict the life-stress relationships, including

a) Arrhenius-Weibull
b) Arrhenius-Exponential
c) Inverse Power-Weibull
d) Inverse Power-Exponential

19.3 Reliability of SSL Systems

The reliability of a system is the ability of the system to meet the required specifications for a given period of time. The stated lifetime of any lighting product is a statistical measure of the performance of a given design.

SSL systems differ significantly from traditional lighting technologies in terms of materials, drivers, system architecture, controls, and photometric properties. SSL systems are complex and many design defects and unknowns in the system can significantly cut short the life time of the system and lower their reliability.

Total SSL systems reliability depends upon the weakest components within the system. Even though an LED's life time can be very long, such as more than 50,000 h; LED driver's life time can be much shorter and therefore shorten the life time of the whole SSL system.

An SSL system is typically composed of lighting sources, drivers, secondary lenses, as well as heat sinks. The key features for SSL systems include drivers and

the thermal management designs. If there is a problem to remove the heat from the LEDs, then the system could be over heat and subsequent failures could follow. In order to determine SSL system reliability, the possible failure modes for each components in the system should be evaluated and analyzed.

Lifetime of the SSL systems should consider all failure mechanisms possible, lumen maintenance is just one of the criteria the industry can use. The reliability and failure rate should be evaluated from system point of view. There are a number of mechanisms which can cause failures in a SSL system, including:

1. Failures due to mechanical interconnections. This includes failures due to wire bonds, connections wires, solder joints, and traces on the boards.
2. Failures due to chemical reactions. These include failures such as corrosion or the formation of intermetallics compounds, which can be manifested as a mechanical failure.
3. Failures due to inherent manufacturing defects in active devices. This includes defects due to pinholes in the insulating oxide, defects, or impurities in the body of the semiconductor, or mask defects.
4. Failures due to EOS. Failures in this category can be created either by overstress during operation or test or by exposure to ESD.

19.3.1 SSL System Reliability

It should be reminded that SSL product reliability is not LED reliability or lumen maintenance or color stability failures. However, higher LED or component reliability will make higher SSL system reliability possible. SSL product reliability is typically lower than LED or other component reliability. Key SSL system components include but not limited to LEDs, electrical components, optical, connections, drivers, and mechanical assembly. SSL product reliability can be expressed as the equation below

$$R_{\mathrm{sys}} = R_{\mathrm{e}} \times R_{\mathrm{con}} \times R_{\mathrm{led}} \times R_{\mathrm{op}} \times R_{\mathrm{th}} \times R_{\mathrm{me}} \tag{19.6}$$

Where

R_{system}: SSL product or system reliability
R_{e}: Reliability of electronic components
R_{con}: Reliability of connections
R_{led}: Reliability of LEDs
R_{op}: Reliability of optical components
R_{th}: Reliability of thermal management components
R_{me}: Reliability of mechanical components

The failure rate of the SSL system will increase with the number of LEDs and required components. The reliability of an LED module or system could decrease

rapidly after a certain amount of time of operation. Y. Aoyama and T. Yachi [4] pointed out that increasing the number of series used in the lighting system could result in a major decrease in reliability.

19.3.2 Design for Reliability of SSL Systems

It should be more efficient to take a system reliability approach in the design of the LED lighting fixture. LED fixture manufacturers measure LEDs in-situ as a system under the drive current, thermal, and optical conditions specific to their products. An SSL system in many ways is an electromechanical system that includes the essential light-emitting source, provisions for heat transfer, electrical control, optical conditioning, mechanical support, and protection, as well as other design elements. However, all of the elements will impact SSL system life.

- LED drivers

The luminous flux of LEDs is mostly determined by the drive current at a given temperature. In order to achieve stable light output, a constant current control is the preferable method to drive LEDs. The power supply and electronics must provide a well controlled DC drive current and possibly other control features, and must not fail for the life of the product.

It is widely known that one of the weakest parts of SSL system is the LED driver due to the number of components it contains, including transformers, capacitors, MOSFETs and inductors. The electrolytic capacitors have the highest probability of failure, it might also cause secondary failures such as transistor failures and regulation failures [27]. The use life of an electrolytic capacitor decreases exponentially as the capacitor body temperature increases therefore it is vital that a high temperature rated capacitor is used within the LED driver and that the maximum operating temperature is well below their temperature rating. Higher quality products will use drivers with high driver efficacy and good LED current control. The reduction in driver efficiency has a major impact on operating temperature of the LED driver and as such reduces its reliability especially for current carrying devices such as MOSFETs or e-caps.

A LED driver's reliability will depend on

1. The number and quality of components used within the driver design.
2. The rated wattage of the LED driver and the maximum operating temperature of the electrolytic capacitors.
3. The ambient operating temperature where the driver is used.
4. The overall efficiency
5. The safety, EMC and thermal considerations of the components used in the driver system.

- Heat sinking systems

To benefit from the long life feature of LEDs, the final system that has to operate at an optimized temperature for a long time. LED system manufacturers can design and build long lasting systems by managing the thermal management well. If systems are not properly designed with good thermal management techniques, even if they use long-life white LEDs, the life of the final system would be short.

Heat management and an awareness of the operating environment are critical considerations to the design of LED luminaires for general illumination. Ensuring necessary light output and life of LEDs requires careful thermal management. If excess heat is not properly managed, the immediate effects are color shift and reduced light output which can lead to accelerated lumen depreciation and thus, shortened useful life.

- Optical systems

Any optical components must be able to withstand years of exposure to intense light and possibly heat without yellowing, cracking, or other significant degradation. Reflecting materials need to stay in place and maintain their optical efficiencies.

Fixture efficiency and light distribution play an equal role in determining optical efficiency. Fixture efficiency is a function of the secondary optics and light loss within the fixture. Good design that considers both fixture efficiency and light distribution is required to achieve energy efficiency and produce minimal light pollution.

- Manufacturing quality

It is important to achieve a quality emitter mounting on MCPCBs. If the surface mounting processes cause large voids at the interface, thermal resistance of the interface will increase dramatically (especially true for high power LED emitters, e.g., 40 W or higher), then emitters will be over heated and failed catastrophically.

The optimal process will require proper stencil design for solder paste printing. It is recommended that the stencil should be 1:1 to MCPCB pad sizes. Outgasing might occur during reflowing process and will cause many voids. In general, small voids with greater than 20% solder coverage under the exposed pad should not result in performance degradation. Solder profile and peak temperature have a strong influence on void formation as well.

During the mounting process, a right solder joint formation should be achieved in order to have a robust thermo-mechanical performance during thermal cycling, thermal shock, or field applications. The key variables controlling the formation of the fillets include solder paste used, flux activity level, PCB land size, solder volume, and the package stand-off height.

For LED components with multiple die, experimental data show that a limited number of catastrophic failures have minimal impact on lumen output. It is another advantage to design LED components with multiple die inside.

It should be reminded that color stability is not exclusively determined by the performance of the LED. Some examples of how luminaire design and manufacturing practices will impact color quality and color shift include

1. Different heat sink designs will mean that LEDs and the associated electronic circuits will likely see different operating conditions despite operating similar times under similar temperature conditions.
2. Different materials used in secondary optics may age differently.
3. Different environmental conditions may cause materials in different luminaire to behave differently.
4. Different luminaire designs will create nonuniform color characteristics such as halos or yellowish, bluish, or greenish hues around the edges of the beam and these color characteristics may vary over time.

19.3.3 Accelerated Stress Testing for SSL Systems

The SSL systems might be modeled by a constant failure rate model. The prerequirement for failure rate modeling is to collect failure data, which is usually through accelerated stress testing.

Because LEDs will take a long time to fail, accelerated stress testing techniques should be used to collect the failure data. The desire of the testing matrix is critical to make sure correct failure mechanisms are accelerated. The following information should be documented for the testing:

(1) The number of samples tested
(2) A description of the test heat sink used. The heat sink system will affect the temperature of LED junction.
(3) The ambient temperature and relative humidity.
(4) The voltage and current applied to the device during the test.

Accelerated stress testing can be designed to have acceleration on junction temperature, drive current, and relative humidity. Driving the SSL products at a level below its maximum rated forward current will extend its useful lifetime, thereby increasing the quotable lumen maintenance life at the same drive current conditions. The combination of high drive current and high junction temperature can significantly stress the LEDs and make it fail faster. For this reason, thermal design considerations are an important aspect of designing an LED-based lighting system.

Based on the acceleration results, a acceleration factor and reliability model can be developed to predict the life in use conditions.

19.3.4 Design for Reliability for SSL Systems

When designing the SSL lighting systems, designers consider the total lumination, the minimum light level specified, the expected life time of the LED lamps and failure rate, the desired relamping interval and the lamp operating conditions.

These factors need to be considered in order to design a robust system with the desired light output, at the same time, achieve the benefits of SSL provided. For instance, reducing the operating current for the LED components will reduce the brightness of the SSL system but also extend the lifetime. To manage the same trade-offs for LED installations, designers can specify drivers to control the forward current. On the other hand, designers can increase the drive current to increase the luminous flux, but a extensive thermal management scheme should be implemented to control the operating temperature of the components in order to achieve desired life time and thermal stability of the system. In addition, a longer relamping interval can result in large cost saving for the end customers.

For LED lamps, system lifetime consideration will need to assure at least

1. Good heat sink design: if this is poorly designed, all the other components can be compromised.
2. Reliable drivers: Drivers are the weakest point of the SSL system. One of the focus is to use high efficiency highly reliable drivers.
3. Optimum optical components: Optical components can be yellow over time and lose light, it is a system design choice.

EPA presents a list of information needed to evaluate the performance of SSL products:

(1) LM-79 test reports. Manufacturers should provide LM-79 testing reports with the following data, including electrical data (input voltage, current, power, power factor, and THD), total light output (luminous flux in lumens, luminous efficacy in lm/W, and a zonal lumen summary), luminous intensity distribution (candela distribution and polar graph), and color characteristics (color temperature, color rendering index, chromaticity coordinates, and spectral power distribution (SPD)).
(2) LM-80 test reports. Manufacturers should provide the LED package manufacturer IES LM-80 test report with results showing relative light output over time at 55°C, 85°C and at a third temperature at the manufacturers' choice.
(3) In-situ temperature testing. Manufacturers may be asked to provide a report indicating the temperature of the hottest LED in-situ in ANSI/UL 1598-04 (hardwired) or ANSI/UL153-05 (corded) environments. The temperature measurement will be used with LM-80 data to validate lumen maintenance and useful life of products.
(4) L70 life prediction. Manufacturers should provide written explanations of how L70 lifetime of products is determined using the IES LM-80 standard and in-situ temperature tests referenced below.
(5) Warranty information of products. Manufacturers maybe asked to provide 3–5 year warranties on LED products.

Heat dissipation is essential for LED's reliability, especially for power LEDs. In case of poor heat dissipation, rising junction temperature will contribute a sharp drop in luminous efficiency by high current density. The thermal path from the die to the underlying lead frame or substrates should be improved, or even changed by

placing the die on a large metallic heat sink slug for a more effective conduction path. The first step in the system level thermal management is to spread and move the heat away from the LED package. This is frequently done through the use of thermally conductive circuit boards, such as metal core PCBS (MCPCBs). Merely placing LEDs onto a thermally conductive board is not a complete solution for solving the thermal issue. LEDs are often placed closely together for optical reasons and the close packaging can elevate LED junction temperature once a LED is within another's "thermal zone". Once the heat has been spread away from the LED, a system's unique design dictates what type of cooling will dominate. The heat in the PCB must be sunk to either the fixture's metal and dissipated into the open air or sunk to a dedicated heat sink for similar dissipation. The next issue is to use low thermal resistance contact between the PCB and the system.

Designers attempting to create high power LED systems are well served by understanding the thermal problems associated with LEDs. Smart thermal management will increase the operating temperature range, and thermal monitoring will maintain the accuracy of LED products.

The performance reliability and life expectancy of electronic equipment are inversely related to the component temperature of the equipment. A reduction in the temperature corresponds to an exponential increase in the reliability and life expectancy of the device.

19.4 LED Emitters and SSL Luminiare Safety

SSL product safety compliance is a legal requirement worldwide, and is a necessity when introducing new SSL products into different markets. According to the requirements of the Occupational Safety and Health Administration (OSHA), electronic equipment is deemed to be safe for use in the workplace if it is listed by a Nationally Recognized Testing Laboratories (NRTLs).

As LED technology has evolved in newer, high voltage, and light output applications, potential safety concerns include the risk of overheating, electric shock, eye safety, and fire. All lighting products sold in the United States are subjected to industry standards governing safety and performance. Underwriters Laboratories (UL) has published ANSI/UL 8750 "Safety Standard for Lighting Emitting Diode (LED) Equipment for Use in Lighting Products." It creates a global platform of safety requirements for LED lighting equipment as well as the entire supply chain of components used in lighting products employing LED technology.

In North America, NRTLs are authorized to conduct product safety testing and certification of LED products according to standards. In order to ensure that the LED technology enjoys the same level of acceptance and consumer confidence as other lighting technologies, LED manufacturers need to consider the following when designing their products:

Risk of shock: For this purpose, two kinds of applications are considered: LEDs supplied by a Class 2 supply and those that are either line connected or otherwise connected to a non-Class 2 supply. The first group does not present a shock hazard due to the voltage and current limitation, while the second one will need to comply with standard insulation and accessibility requirements. The only additional concern even for Class 2 supplies is for devices used in wet locations. This further limits the maximum open circuit voltage to 15 VAC or 30 VDC.

Risk of fire: When dealing with risk of fire, many different aspects will impact the performance of a fixture, including but not limited to: proximity between the LEDs, diffuser design and material, type of enclosure, installation, etc. While using a Class 2 power supply reduces the risk of fire by limiting the available electrical energy, there are evidences that these systems may exceed 90°C (the maximum permitted by the building code in the US on combustible surfaces) due to the thermal energy dissipated by the LED in converting electrical energy to light. Therefore LED luminaires need to be designed to take this into account and to undergo temperature testing to ensure all components within the luminaire and the outside surfaces are operating within their specified temperature ratings.

Biological hazards: Issues like retinal damage and other health issues that could arise from exposure to these light sources are always a concern, but currently there is no conclusive research that proves that there is a significant risk involved with using this technology. As with any light source, using a diffuser may mitigate personal injury risks from the electromagnetic radiation it produces.

In Europe, additional safety test based on IEC62471 should be conducted to understand the risks to eye.

During the safety evaluation process, the process of conducting product certification can be broken down into several steps.

First, a review of the product's construction and design is performed, which includes careful evaluation of specific product information, including the bill of materials, applicable ratings of the individual components and materials, product design drawings, and spacing and dimensional requirements. From the review of all submitted information, it is possible to determine the appropriate testing that will be required to sufficiently satisfy the requirements stated in the applicable standard(s).

Next comes the actual product testing phase, which is performed in accordance with the requirements of the applicable standard(s). Such tests may include temperature, electrical, dielectric, strain relief, environmental (wet location), and mechanical tests, among others.

Step three includes the creation and issuance of the formal test report and "authorization to mark" (ATM), which grants the manufacturer permission to label the product with the applicable safety mark from an NRTL (an example would be the ETL Listed mark from Intertek).

Finally, the manufacturer must agree to participate in the NRTL's follow up services program. This typically involves an initial audit of the manufacturing facility, as well as periodic manufacturing facility inspections to ensure consistent

design, production, and labeling of the product. It is also necessary to maintain and update files to remain current with the latest revision of the applicable standards.

For SSL systems and luminaries, UL 1993 are applied to cover both self-ballasted lamp adapters. The key test listed in UL 1993 for LED lamps include

1. LED drivers
2. Fire enclosures
3. Dielectric withstand
4. Drop performance
5. Temperature measurement
6. Humidity conditioning

Examples reference testing plan is shown in the Table 19.7.

UL 8750 covers LED equipment that is an integral part of a Luminaire or other lighting equipment, including LED drivers, controllers, arrays, modules, and packages.

19.5 Energy Star SSL Certification

SSL products differs from traditional lighting technologies in terms of materials, drivers, system architecture, controls, and photometric properties. SSL technology is rapidly evolving but not all LEDs or SSL systems are created equal. The Energy Star program from EPA is developed and will be awarded to selected fixture types that meet strict efficiency, quality, and lifetime criteria. It will facilitate the fast adoption of SSL products in general lighting industry.

EPA released many document to encourage the SSL Energy Star activities, including program requirements for SSL products and manufacturer's guide for qualifying SSL luminaires.

19.5.1 Temperature Measurement for Energy Star Certification

LED packages, array, or module manufacturers designate specific locations on their products acting as reference points for measuring junction temperature, often called temperature measurement points in DOE/EPA document. Knowledge of the thermal pathway between the LED die junction and a designated external measurement pint on the package array or module allows manufacturers to accurately estimate LED junction temperatures. Some manufacturers use temperatures measured at the solder joints at the board attachment site, others use the package case temperature or the board temperature on the module.

In luminaire or LED lamp applications, the in-situ measured TMP_{led} is bounded above and below by case temperature data collected according to LM-80-08

Table 19.7 Test Plan listed in UL 1993

Test types	Test descriptions
Electrical tests	
Input measurements	The input current should not be more than 110 % of the marked rating. The input wattage shall not be more than 110 % of the marked rating
Starting and operating measurements	The measurement shall be carried out for each lamp type that can be accommodated by the device amp holder. The measured lamp voltage and current shall not differ by more than 10 % from the rated value
Enclosure leakage current test	The device with an exposed noncurrent carrying metal part shall comply with the leakage current requirements in UL 935
Normal temperature test	The maximum temperature shall not exceed the maximum temperature specified for materials
Dielectric voltage-withstand test	A device with accessible noncurrent carrying metal parts that could be energized from within shall withstand for 1 min, without breakdown A device with accessible nonmetallic parts and opening in the enclosure shall withstand for 1 min without breakdown
Mechanical tests	
Drop test	A device with a polymeric enclosure shall be subjected to the tests. There should be no damage to the enclosure making uninsulated live parts or internal wiring accessible to contact or defeating the mechanical protection of internal parts of the equipment afforded by the enclosure. A device shall be dropped 3 times so that in each drop, the samples strikes the surface in a different position. It should be done combined with dielectric withstand tests for a device having accessible noncurrent-carrying metal parts
Mold stress relief conditioning	The tests will be conducted in an oven with a temperature maintained 10°C higher than the maximum temperature during the normal conditions. The sample shall not be distorted or have any damage that could impair the usage. It should be capable of maintaining the dielectric voltage withstand test
Defection test	The enclosure of the device shall be capable of withstanding specified force applied
Special tests	
Tests with dimmer circuits	The tests include normal operation test and abnormal tests specified
Humidity conditioning test	A device intended for use in damp or wet locations and having accessible noncurrent-carrying metal parts shall be exposed to moist air having a relative humidity of 95 % at 25°C. After exposure for certain hours, the device will comply with the requirements for dielectric voltage withstand test between current carrying parts and accessible noncurrent-carrying metal parts
Water spray test	The test is for devices intended to be used in wet locations
Cold impact test	A device with a polymeric enclosure and marked for use in wet locations shall comply with the cold impact test (−35 C).

(continued)

Table 19.7 (continued)

Test types	Test descriptions
	While the units is cold, the samples shall be subjected to the drop test described
Lamp fault conditions test	Special fault conditions are set-up and the samples shall accept the fault conditions specified without increasing the risk of fire or shock
End of lamp life tests	The specified tests include asymmetric pulse test, asymmetric power dissipation test, and open filament test. The test results shall be in compliance when the wattage or current is less than the limit specified in the tests

procedures. In this case, linear interpolation shall be used to determine the lumen depreciation (maintenance) for the proposed product, as follows

$$L_{\text{tmp}} = L_{\text{below}} + \left(\frac{L_{\text{above}} - L_{\text{below}}}{T_{\text{s,above}} - T_{\text{s,below}}}\right)\left(\text{TMP}_{\text{led}} - T_{\text{s,below}}\right) \tag{19.9}$$

where

L_{below} = lumen maintenance (%) below TMP_{led} @ ≥6,000 h
L_{above} = lumen maintenance (%) above the TMP_{led} @ ≥6,000 h
$T_{\text{s,below}}$ = LM-80 case temperature below the TMP_{led}
$T_{\text{s,above}}$ = LM-80 case temperature above TMP_{led}
TMP_{led} = in-situ measured TMP of the hottest LED within the luminaire
L_{tmp} = calculated lumen maintenance of the hottest in situ LED within the luminaire.

19.5.2 Lumen Maintenance Testing

There are two compliance methods for lumen depreciation testing applied in Energy Star Certification. The first is component performance and the second is luminaire performance. The component performance option allows the applicant to demonstrate compliance with the lumen depreciation requirements by demonstrating the hottest LED package, array, or module operates at or below temperatures yielding an L70 of 25,000 hours or 35,000 hours. The luminaire performance option allows the applicant to show compliance with the lumen depreciation requirement by demonstrating the light output from the Luminaire at ≥6,000 hours yields ≥91.8% lumen maintenance for a projected L70 of 25,000 hour or ≥94.1% lumen maintenance for projected L70 of 35,000 hours. Lamps that are 10 W or more must be subjected to elevated temperature testing for lumen maintenance. The summarized requirements for SSL luminaires are shown in Table 19.8.

Table 19.8 Energy star requirements for luminiare

Performance characteristics	Requirements
Luminaire efficacy	IESNA LM-79-08
Minimum light output	IESNA LM-79-08
Zonal lumen density	IESNA LM-79-08
Correlated color temperature	Nominal CCT (2,700, 3,000, 3,500, 4,000, 4,500, 5,000, 5,700, and 6,500 K)
Color spatial uniformity	The variation of chromaticity in different directions shall be within 0.004 from the weighted average point on the CIE 1976 (u', v') diagram
Color maintenance	The change of chromaticity over the lifetime of the product shall be within 0.007 on the CIE 1976 (u', v') diagram
Color rendering index (CRI)	Indoor luminaires shall have a minimum CRI of 75
Off-state power	Luminaires shall not draw power in the off state
Warranty	A minimum of 3 years from the date of purchase
Thermal management	Luminaire manufacturer shall adhere to device manufacturer guidelines, certification programs, and test procedures for thermal management
Lumen maintenance of LED light source (L70)	IESNA LM-08-08 for LED packages or IESNA LM-79-08 lumen maintenance for luminaires. At least 70 % of initial lumens for the minimum number of hours specified below: Residential indoor: 25,000 h Residential outdoor: 35,000 h All commercial: 35,000 h
Power factor	Residential $\geq$ 0.7 Commercial $\geq$ 0.9
Output operating frequency	$\geq$120 Hz
Electromagnetic and radio frequency interference	Must meet FCC requirements for consumer use (FCC 47 CFR Part 15/18 consumer emission limits); or nonconsumer use (FCC 47 CFR Part 15/18 nonconsumer emission limits)
Noise	Power supply shall have a Class A sound rating
Transient Protection	Power supply shall comply with IEEE C.62.41-1991, Class A operation. The line transient shall consist of 7 strikes of a 100 kHz ring wave, 2.5 kV level, for both common mode and differential mode

EPA recognizes the certification of product families which shall be identical to the tested, representative model with the exception of allowed variations listed in the Table 19.9. Any variation in lamp design that impacts the performance of the lamp is considered a new, separate product and therefore must be tested in accordance with all requirements detailed in the EPA Energy Star Specification. EPA will permit the use of long-term lumen maintenance data across multiple model numbers which vary only in paint color and/or beam angle. Variations in paint shall be limited to color/pigmentation only. To apply lumen maintenance data across multiple models which vary only in paint color/pigmentation, EPA will require submission of in-situ temperature measurements of each of the models in question. The use of long-term lumen maintenance data across multiple models which vary only in beam angle will be permitted so long as the variation between models is limited to the dimensions of

Table 19.9 EPA allowable variations within product families

Housing/chassis	Allowed so long as the light source or lampholder, ballast or driver, and heat sink are integrated into housing/chassis variations in such a way that the thermal performance of the luminaire is not degraded by changes to the housing/chassis. Thermal measurement of each variation may be required
Heat sink/thermal management components	Not allowed
Finish and mounting	Allowed
Reflector/trim	Allowed so long as luminaire light output is not reduced
Shade/diffuser	Allowed
Light source	Allowed so long as variations will not negatively impact luminaire's compliance with any performance criteria in this specification
Correlated color temperature (CCT)	Allowed so long as the lamp series or LED package/module/array series, ballast or driver, and thermal management components are identical, and so long as variations will not negatively impact luminaire's compliance with any performance criteria in this specification. The representative model shall be the version within the product family with the lowest CCT
Ballast/driver	Allowed so long as variations will not negatively impact luminaire's compliance with any performance criteria. Thermal measurements of each variation may be required

the secondary optics, and so long as these changes do not have a measureable effect on in-situ temperature measurements. Variations in secondary optic material will not be permitted. To apply lumen maintenance data across multiple models which vary only in beam angle, EPA will require the following to be submitted:

(a) In-situ temperature measurements of each of the models in question.
(b) A signed statement on the partner company's letterhead stating that there are no material variations between the models in questions except for the dimensions of the secondary optics.

19.6 Summary

LED components, especially high power LEDs or ultra high power LEDs for general illumination, including packages, arrays, and modules are still in the initial adoption stage, and there are many challenges facing the industry. This chapter discusses some of the key areas in terms of reliability and life time prediction facing the industry as, summarized in below:

- Determination of failure criteria, including catastrophic failures as well as degradation failures. LED performance degradation should consider lumen maintenance, color shift, and forward voltage shift.

- There are unique testing standards emerging and being characterized for high power LEDs. When planning and executing reliability testing for LED components, special care should be implemented so the test results will be reflecting what the components will experience in field applications.
- It is important to accumulate knowledge of failure mechanisms in high power or ultra power LEDs, and dominant stress factors for LED performance and reliability life. It is usually assumed that LED won't fail suddenly; however, testing results have consistently show LEDs can fail catastrophically and an optimized application window should be defined to make sure LED will achieve long life time and high reliability, including junction temperatures and drive currents.
- There are new package design, packaging materials and assembly processes being developed to improve the LED efficacy and reliability life. Any new developments adopted in LED components will potentially change the life time and reliability.
- There are still not enough data available to verify current adopted reliability models for LED components and SSL systems. Many testing data should be collected in order to understand and develop the failure rate models and reliability life models. The impact from critical stress factors are known, but no systematic and quantitive assessments available to describe the impacts. Key model parameters for Arrhenius Models and Hallberg–Peck models should be validated.
- Design-for-reliability activities should be implemented throughout the design, manufacturing, and field application process. Field failures should be monitored to help improve the design and testing methodologies.

References

1. Albertini A, Masi MG, Mazzanti G, Peretto L, Tinarelli R (2010) A test set for LEDs life model estimation. IEEE, Austin. ISBN 978-4244-2833-5/10
2. ANSI_NEMA_ANSLG C78.377 (2008) Specifications for the chromaticity of solid state lighting products
3. ANSI/UL 153 (2005) Portable electric luminaires. ISBN 1-55989-842-9
4. Aoyama Y, Yachi T (2008) An LED module arrays system designed for streetlight use. IEEE Energy 2030, Atlanda, GA, 17–18 November 2008.
5. Arik M, Petroski J, Weaver S (2002) Thermal challenges in the future generation solid state lighting applications: light emitting diodes. IEEE Inter Society Conference on Thermal Phenomena, pp 113–120
6. Arik M, Sharma R, Jackson J, Prabhakaran S, Seeley C, Utturkar Y, Weaver S, Kuenzler G, Han B (2010) Development of a high lumen solid state down light application. IEEE Trans Compon Packaging Technol 33(4):668–679
7. Arik M, Setlur A, Weaver S, Haiko D, Petroski J (2007) Chip to system levels thermal needs and alternative thermal technologies for high brightness LEDs. Trans ASME J Electron Packaging 129:328–338
8. Bojta P, Nemeth P, Harsanyi G (2002) Searching for appropriate humidity accelerated migration reliability tests methods. Microelectron Reliab 42:1213–1218
9. Chan HA, Englert PJ (2001) Accelerated stress testing handbook. IEEE Press, New York

10. Chen CZ, Li W et al (2010) Lumen maintenance lifetime prediction of power LED
11. Chen CH, Tsai WL, Tsai MY (2008) Thermal resistance and reliability of low-cost high-power LED packages under WHTOL test. IEEE X-plore, Taipei, pp 271–276. ISBN 978-1-4244-3621-7108
12. Chen Z, Zhang Q, Wang K, Luo X, Liu S (2011) Reliability test and failure analysis of high power LED packages. J Semicond 32(1):14001–14007
13. Chi WH, Chou TL, Han CN, Yang SY, Chiang KN (2010) Analysis of thermal and luminous performance of MR-16 LED lighting module. IEEE Trans. On Component and Packaging Technologies, ID 10.1109/TCAPT.2010.2073469, pp 1–9
14. Crawford M (2009) LEDs for solid-state lighting: performance challenges and recent advances. IEEE J Sel Top Quantum Electron 15(40):1028–1040
15. (2010) Cree Technical Article, LED eye safety, CLD-AP34 Rev. 1
16. (2007) CREE XLamp LED Reliability, March 2007
17. (2009) CREE XLamp MX-6 LED Reliability, September 2009
18. (2009) CREE XLamp XR Family LED Reliability, December 2009
19. Day M (2004) LED-driver considerations. Analog Applications Journal Q1, TI, pp 14–17
20. Freescale Semiconductor Inc. (2007) Application Note AN2467: Power Quad Flat No-Lead (PQFN) Package
21. Dodson B, Nolan D (1999) Reliability engineering handbook, quality and reliability/56. Marcel Dekker, Tucson
22. Emerson J, Peterson DW, Sweet JN (1992) HAST evaluation of organic liquid IC encapsuants using Sandia's assembly test chips 0569-5503. IEEE, pp 951–956
23. Energy Star Program Requirements for Solid State Lighting (SSL) Luminaires-Eligibility Criteria-Version 1.3. http://www.energystar.gov/ia/partners/product_specs/program_reqs/Solid-State_Lighting_Program_Requirements.pdf
24. Energy Star Program Requirements Product Specification for Luminaires (Light Fixtures) Eligibility Criteria Version 1.0. http://www.edisonreport.net/files/4612/9784/2321/ENERGY_STAR_Luminaires_V1_0_Final.pdf
25. Gao J, Hao P et al (2009) Evaluation of power LED operation life. Semicond Technol 34 (5):452–454, Chinese
26. Han BT, Jang C, Bar-Cohen A, Song B (2010) Coupled thermal and thermo-mechanical design assessment of high power light emitting diode. IEEE Trans Compon Packaging Technol 33(4):688–697
27. Han L, Narendran N (2010) An accelerated test method for predicting the useful life of an LED driver. IEEE 2010
28. Hodapp M (2010) Evaluating the lifetime behavior of LED systems. DOE Manufacturing Workshop, San Jose
29. Hahn B (2010) High power LEDs for solid state lighting. IEEE X-plore, 978-1-4244-6661-0/10, pp 57–63
30. Hsu YC, Lin YK, Kuang JH, et al (2007) Failure mechanisms associated with lens shape of high power LED modules in aging test. IEEE 2007, 1-4244-0925-X/07, section WS3
31. Huang X, Chen S, Huang G, Zhang X (2011) Reliability study of LED modules. 2011 Conference on Optical Technology, ChingYun University, Zhongli, 27 May 2011
32. IPC-7530 (2001) Guidelines for temperature profiling for mass soldering processes (reflow and wave), May 2001
33. IEC 62471 (2006) Photobiological safety of lamps and lamp systems
34. IESNA LM-16, Correlated color temperature
35. IESNA LM-58-94 (1994) Color rendering index and correlated color temperature
36. IESNA LM-79-08 (2008) Approved method: electrical and photometric measurements of solid-state lighting products
37. IESNA LM-80-08 (2008) Approved method for measuring lumen maintenance of LED light sources
38. IES TM-21-11 (2011) Projecting long term lumen maintenance of LED light sources, July 2011

39. IES TM-21-11 (2011) Update: method for projecting lumen maintenance of LEDs, CORM 2011 technical conference, May 2011
40. JEDEC Standard (2008) JESD22-A113F: preconditioning of nonhermetic surface mount devices prior to reliability testing
41. JEDEC Standard (2009) JESD 22 A101-C: steady state temperature humidity bias life test, March 2009
42. JESD22-A118A (2011) JEDEC standard accelerated moisture resistance unbiased HAST, March 2011
43. JESD22-A101C (2009) JEDEC standard steady state temperature humidity bias life test, March 2009
44. Kang JM, Kim JW, Choi JH, Kim DH, Kwon HK (2009) Lifetime estimation of high power blue light-emitting diode chips. Microelectron Reliab 49:1231–1235
45. Jeong JS, Jung JK, Park SD (2008) Reliability improvement of InGaN LED backlight module by accelerated life test (ALT) and screen policy of potential leakage LED. Microelectron Reliab 48:1216–1220
46. Kim H, Choi SH, Shin SH, Lee YK, Choi SM, Yi S (2008) Thermal transient characteristics of die attach in high power LED PKG. Microelectron Reliab 48:445–454
47. Lall P, Pecht M, Hakim E (1997) Influence of temperature on microelectronics and system reliability. CRC, New York
48. Le SP, Zheng CD, Jang FY (2007) Influence of ESD on aging of GaN/Si blue LEDs. J Nanchang University (Nat Sci) 31(3):246–248, 252
49. Li X, Chen X, Lu GQ (2010) Reliability of high power light emitting diode attached with different thermal interface materials. Trans ASME J Electron Packaging 132:031011-1–031011-5
50. Lin YC, You JP, Tran N, He Y, Shi F (2011) Packaging of phosphor based high power white LEDs: effects of phosphor concentration and packaging configuration. J Electron Packaging 133:011009-1–011009-5
51. Lin YH, You JP, Lin YC, Tran NT, Shi FG. Development of high-performance optical silicone for the packaging of high-power LEDs. IEEE Trans. On Components and Packaging Technologies, 10.1109/TCAPT.2010.2046488, pp 1–6
52. Lin YC et al (2009) LED and optical device packaging and materials, Chapter 18. In: Lu D, Wong CP (eds) Materials for advanced packaging. Springer, Berlin, pp 629–680
53. Liu ZY, Liu S, Wang K, Luo XB (2010) Studies on optical consistency of white LEDs affected by phosphor thickness and concentration using optical simulation. IEEE Trans Compon Packaging Technol 33(4):680–687
54. Lu D, Wong CP (2009) Materials for advanced packaging. Springer, New York
55. Lu G, Huang Y, En Y, et al (2009) The relationship between LED package and reliability. IEEE Proceedings of 16th IPFA, China, 2009
56. Lumileds Application Brief AB05. Thermal design using LUXEON power light source.
57. Luo X, Wu B, Liu S (2010) Effects of moist environments on LED module reliability. IEEE Trans Device Mater Reliab 10(2):182–186
58. Meneghini M, Trevisanello LR, Meneghesso G, Zanoni E (2008) A review on the reliability of GaN-based LEDs. IEEE Trans Device Mater Reliab 8(2):323–331
59. Moe CG, Reed ML, Garrett GA et al (2009) Degradation mechanisms beyond device self-heating in deep ultraviolet light emitting diodes. IEEE CFP09RPS-CDR 47th annual international reliability physics symposium Montreal, 2009, pp 94–97
60. Meneghini M, Trevisanello LR, Meneghesso G, Zanoni E (2008) A review on the reliability of GaN-based LEDs. IEEE Trans Device Mater Reliab 8(2):323–331
61. Meneghini M, Pacesi M, Trivellin N, Gaska R, Zanoni E et al (2008) Reliability of deep-UV light emitting diodes. IEEE Trans Device Mater Reliab 8(2):248–254
62. Molian R, Shrotriya P, Molian P (2008) Improved method of CO_2 laser cutting of aluminum nitride. Trans ASME J Electron Packaging 130:024501-1–024501-3
63. Narendran N, Gu Y, Freyssinier JP, Yu H, Deng L (2004) Solid state lighting: failure analysis of white LEDs. J Cryst Growth 268:449–456

64. Narendran N, Gu Y (2005) Life of LED-based white light sources. IEEE/OSA J Display Technol 1(1):167–171
65. Nelson W (1990) Accelerated testing statistical models, test plans, and data analyses. Wiley, New York
66. NEMA SSL-3 (2010) High power white LED binning for general illumination
67. NEMA LSD 45-2009 (2009) Recommendations for solid state lighting sub-assembly interfaces for luminaires
68. Nichia Corporation. STS-DA1-0634 C: specifications for Nichia chip type white LED model NS6W183T-H3
69. Nichia Corporation. STS-DA1-1453A: specifications for Nichia chip type white LED model NS6L183T-H3
70. Nichia Corporation. STS-DA1-1370B: specifications for Nichia chip type warm white LED model NS3L183AT-H3
71. Nichia Corporation. STS-DA1-0994B: specifications for Nichia chip type warm white LED model NCSL119T-H3
72. Nichia Corporation. STS-DA1-1447A: specifications for Nichia chip type warm white LED model NS3L183T-H3
73. Nichia Corporation (2010) SQETC100201A LM-80 test report
74. Nichia Corporation (2010) SQETC100202A LM-80 test report
75. Nichia Corporation (2010) SQETC100301A LM-80-08 test report
76. NGLIA (2010) Solid state lighting product quality initiative: LED luminaire lifetime, recommendations for testing and reporting, 1st edn.
77. OSRAM Opto Semiconductors (2008) Application Note: Reliability and lifetime of LEDs, July 2008
78. OSRAM Opto Semiconductors (2009) Application Note: reliability of the DRAGON product family, Feb 2009
79. Peng C (2009) Influence of fluorescent glue packaging technology on the color rendering index of high power LED. Adv Display 103:56–60
80. Philips Lumileds. Application Brief AB32, LUXEON Rebel and LUXEON Rebel ES assembly and handling information. www.philipslumileds.com/uploads/252/AB32-pdf
81. Philips Lumileds (2010) Technology white paper: understanding power LED lifetime analysis
82. Rada BM, Triplett GE (2010) Thermal and spectral analysis of self-heating effects in high-power LEDs. Solid State Electron 54:378–381
83. Remsburg R (2001) Thermal design of electronic equipment. CRC, Boca Raton
84. Striny KM, Schelling W (1981) Reliability evaluation of aluminum metallized MOS dynamic RAM's in plastic packages in high humidity and temperature environments. IEEE Trans Compon Hybrids Manuf Technol CHMT-4(4):476–481
85. Su YF, Yang SY, Chi WH, Chiang KN (2010) Light degradation prediction of high power light emitting diode lighting modules. IEEE 11th international conference on thermal, mechanical and multiphysics simulation and experiments in micro-electronics and micro-systems, EuroSimE 2010, pp 1–5
86. Suhling JC, Gale HS, Johnson RW, Islam MN et al (2004) Thermal cycling reliability of lead free solders for automotive applications. 2004 Inter society conference on thermal phenomena, pp 350–357
87. Shao X, Yan D, Lu H, Chen D, Zhang R, Zheng Y (2011) Efficiency droop behavior of GaN-based light emitting diodes under reverse-current and high temperature stress. Solid State Electron. doi:10.1016/j.sse.2010.12.008
88. Tan CM, Chen BKE, Xiong M (2010) Study of humidity reliability of high power LEDs. 2010 I.E. International conference on Solid-State and Integrated Circuit Technology (ICSICT), pp 1592–1595
89. Tan CM, Chen BK, Xu G, Liu Y (2009) Analysis of humidity effects on the degradation of high-power white LEDs. Microelectron Reliab 49:1226–1230

90. Tsai CC, Wang J, Chen MH et al (2009) Investigation of Ce:YAG doping effect on thermal aging for high-power phosphor-converted white-light-emitting diodes. IEEE Trans Device Mater Reliab 9(3):367–371
91. Tsai CC, Chung CH et al (2010) High thermal stability of high-power phosphor based white-light-emitting diodes employing Ce:YAG-doped glass. 2010 I.E. ECTC, pp 700–703
92. Tuttle RC (2011) White LED chromaticity control_the state of the art. Transformations in Lighting, 2011 DOE Solid-State Lighting R&D Workshop, 2011
93. US DOE. Lifetime of white LEDs, PNNL-SA-50957
94. US Department of Energy (2008) ENERGY STAR manufacturer's guide for qualifying solid-state lighting luminaires, September 2008
95. UL 1598 (2004) Luminaires
96. UL 8750 (2009) Light emitting diode (LED) equipment for use in lighting products, 1st edn. Underwriters Laboratories Inc., Canada
97. UL 1993 (2009) Self-ballasted lamps and amp adapters, 3rd edn. Underwriters Laboratories Inc., USA
98. Vazquez M, Nunez N, Nogueira E, Borreguero A (2010) Degradation of AlInGaP red LEDs under drive current and temperature accelerated life tests. Microelectron Reliab 50:1559–1562
99. Wang QL, Xia ZQ, Wen J (2008) LED junction temperature a thermal resistance and its impact. Adv Display 6:59–61
100. White M, Cooper M, Chen Y, Bernstein JB (2003) Impact of junction temperature on microelectronic device reliability and considerations for space applications. 2003 IRW Final Report, pp 133–136
101. Wu Z, Qian K et al (2007) Study on packaging technology of ultraviolet LED with high efficiency and reliability. J Optoelectron Laser 18(1):1–4
102. Wu F, Zhao W, Yang S, Zhang C (2009) Failure modes and failure analysis of white LEDs. The ninth International Conference on Electronic Measurement and Instruments, ICEMI-2009, pp 4-978–4-981
103. Wu B, Luo X, Liu S (2010) Effect mechanism of moisture diffusion on LED reliability. Electronic System-Integration Technology Conference (ESTC), pp 1–5
104. Yang SH, Lin P, Wang CP, Huang SB et al (2010) Failure and degradation mechanisms of high power white light emitting diodes. Microelectronics Reliability 50:959–964
105. You JP, Lin YH, Tran NT, Shi FG (2010) Phosphor concentration effects on optothermal characteristics of phosphor converted white light-emitting diodes. Trans ASME J Electron Packaging 132:031010–031011
106. Zhang J, Hu X et al (2005) AlGaN deep-ultraviolet light emitting diodes. Jpn J Appl Phys 44 (10):7250–7253
107. Zhang Q, Mu X, Wang K et al (2008) Dynamic mechanical properties of the transparent silicone resin for high power LED packaging. 2008 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2008)
108. Zhang L, Zhou L, Zhang J, Luo Z, Cui Y (2009) Research on mechanism of high power LED luminous attenuation. Semicond Technol 34(5):474–477. doi:10.3969/J, issn 1003-353x

Chapter 20
Color Consistency Reliability of LED Systems

B. Bataillou, N. Piskun, and R. Maxime

Abstract LEDs are devices with inherent variability, which cause luminaire manufacturers a challenge to guarantee a color point, as the base component needs to be selected and carefully checked to ensure that the specification is reached. In this chapter, we propose a method to embrace this variability by using standard linear optimization algorithms and statistical methods, to reach a reliable color point specification, and we analyze limits, methods, and future developments on color specification.

20.1 Introduction

As a result of uncontrolled variability in the fabrication method, LEDs exhibit significant color variability. The common strategy used by manufacturers to reduce this variability is post selection or binning by similar color, luminous flux, voltage, etc. But this strategy has limitations, and LEDs products of well-controlled color can be challenging to make in real cases. A couple facts are hampering extreme color specifications

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- Specifications of LED luminaires can be narrower than the binning size
- For multi-LED products, variability of the flux from LED to LED also affects the color point of the product.
- LEDs color point change over time
- Narrower color specification can be purchased. However, this result in higher costs and increase the risk of shortages.

Due to those limitations, it is at this time difficult to predict, specify and guarantee color specifications for luminaire products. In this chapter we show that for luminaire products made of many LEDs, these limitations can be overcome by carefully choosing and arranging the LEDs contained in an LED shipment using standard optimization & statistical methods.

In the first section, we remind basic notions used in colorimetry, which are used in the second section for the problem description (dealing with "interbin variability"). The third section contains the justifications of the several methods to reduce color variation of the given product as well as color consistency of subsequent production by taking into account "intrabin variability". The fourth section describes the shift over time ("color maintenance, lumen maintenance") to reach a reliable color specification. Finally, the fifth section evaluates the limits of the technology, on the color consistency point of view, and proposes a guideline to get close to the extreme specifications, as close as possible to the best conditions derived from Mac Adam works.

20.2 Color Space and SDCM

20.2.1 Basic Notions of Colorimetry

The science which tries to associate unambiguously a color sensation as experienced by an average human—i.e., visual stimulus—with numerical values is called colorimetry. Many colorimetric systems are possible, but all are subject to the following set of simple rules:

- Stimuli that look alike have equal specifications;
- Stimuli with equal specification when viewed by an observer with normal color vision under same observing conditions results in identical color sensation, i.e., complete color matching;
- Numerical values associated with a given color stimulus are given by a continuous function of the parameters describing the spectrally dependent response to light intensity of the human eye.

The experimental laws of color matching also referred as trichromatic generalization provides the basis for any colorimetric system [1, 2].

Another very important aspect of colorimetry deals with specification of small color differences that an observer may perceive. In this case the differences in the

spectral radiant power distributions of the given visual stimuli do not provide a complete color match.

International Commission on Illumination, usually abbreviated CIE (Commission Internationale de l'Eclairage), is an international authority that provides CIE Colorimetric System with standards, specification and measurement procedures that makes colorimetry a useful tool for color science technology and standardization [3–5]. For further reference on colorimetry terms and definitions are summarized in the fourth edition of the International Lighting Vocabulary [6].

20.2.2 Trichromatic Generalization and Grassman's Law

The experimental laws of color matching are called trichromatic generalization. Couple basic colorimetric terms need to be introduced:

- A *color stimulus* is radiant power of given magnitude and spectral composition, entering the eye and producing a sensation of color.
- Primary color stimuli are color stimuli by whose additive mixture nearly all other color stimuli may be completely matched color. These color stimuli are often chosen to be red, green and blue.

Trichromatic generalization states that over a wide range of conditions of observations color stimuli can be matched in color completely by additive mixtures of three fixed primary stimuli with adjusted radiant powers (radiometric flux). Additive mixture means that a color stimulus for which the radiant flux in any wavelength interval in any part of the spectrum is equal to the sum of the fluxes in the same interval of the elements of the mixtures. Elements of the mixtures assumed to be optically incoherent. The color matching results obeys linearity laws:

(a) Symmetry law

$$A = B \leftrightarrow B = A$$

(b) Proportionality law

$$\text{if } A = B \rightarrow \alpha\, A = \alpha\, B$$

where α is positive radiant flux factor, while relative spectral distribution is kept the same

(c) Transitivity law

$$\text{if } A = B \text{ and } B = C \text{ than } A = C$$

(d) Additivity law

$$\text{if } A = B \text{ and } C = D \text{ and } (A + C) = (B + D) \text{ than } (A + D) = (B + C)$$

Trichromatic generalization of color mixing was formulated by Grassman in 1853 [7] and known as Grassman's law. Modern formulation of Grassman's law was given by Judd and Wyszecki [8] and detailed mathematical explanation was given by Kranz [9]. Following assumptions were made:

(a) Color matching is independent on observation conditions;
(b) Previous exposure to light by an eye is not considered;
(c) Difference in color perception of different observers is negligible.

20.2.3 Tristimulus RGB Space

It is convenient to represent the three color stimuli defined in the Grassman's law by vectors in three-dimensional space called tristimulus or RGB space. R, G, B are primary stimuli and Q is an arbitrary color stimulus. Spectral distribution of a specific color stimulus Q is uniquely defined by its spectral radiant power distribution:

$$Q = \int P_\lambda f(\lambda) d\lambda \tag{20.1}$$

where $P_\lambda d\lambda$ represents the radiant power in the wavelength interval of width $d\lambda$ centered at the wavelength λ, and f a function representing the response of for example a specific eye receptor. Similar notation used for primary stimuli R, G, and B though they can be regarded as primary stimuli of unit amounts. Using above notations a color matching between Q and additive mixture of R, G, and B is given by the following equation:

$$Q = R_Q R + G_Q G + B_Q B \tag{20.2}$$

where R_Q, G_Q, B_Q are coefficients measured in terms of R, G, B units and called the tristimulus values of Q. To define Q_λ—monochromatic stimulus of wavelength λ—equation (20.2) should be transferred into:

$$Q_\lambda = R_\lambda R + G_\lambda G + B_\lambda B \tag{20.3}$$

where $R_\lambda, G_\lambda, B_\lambda$ are the spectral tristimulus values of Q_λ. An important set of the spectral tristimulus values is obtained when all monochromatic stimuli Q_λ contained in the spectrum of the given color stimulus Q have unit radiant power at every wavelength λ within the visible spectrum:

$$P_\lambda = E_\lambda = \text{const} \tag{20.4}$$

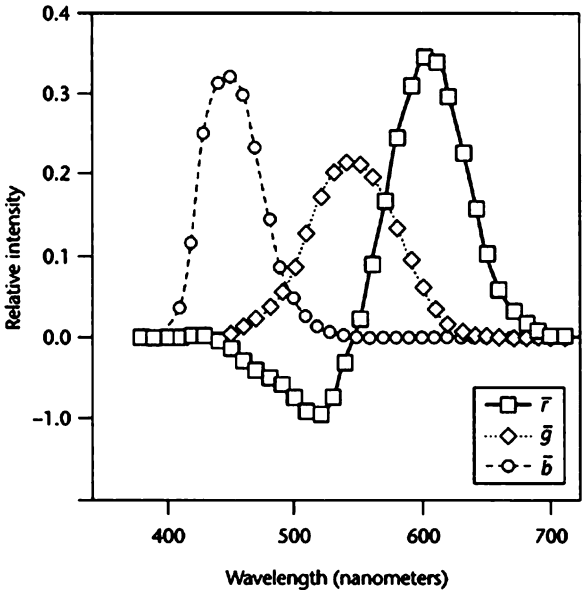


Fig. 20.1 1931 CIE Color matching functions

Such stimulus is called equal-energy stimulus E. The spectral distribution $\{E_\lambda d\lambda\}$ of the equal-energy stimulus is uniform across the visible spectrum. Equation (20.4) for a color matching of equal-energy monochromatic stimulus E_λ is:

$$E_\lambda = \bar{r}(\lambda)R + \bar{g}(\lambda)G + \bar{g}(\lambda)B \tag{20.5}$$

where $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, $\bar{b}(\lambda)$ are the spectral tristimulus values of E_λ. The sets of spectral tristimulus value $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, $\bar{b}(\lambda)$ of monochromatic stimuli E_λ of unit radiant power called color matching functions.

An observer makes color matching according to trichromatic generalization. The color matching properties of an observer are defined by specifying three independent color matching functions. The color matching functions of 1931 CIE are based on the experiments done by Guild and Wright [1, 10]. Guild transformed his and Wrights measurements to a common system in which the primary stimuli were monochromatic and the chromaticity units used the equal-energy point.

Figure 20.1 shows the 1931 CIE color matching functions. E_λ of a unit of radiant power varies from 380 nm to 700 nm. Fixed monochromatic primary stimuli R, G, B are $\lambda_R = 700$ nm, $\lambda_G = 546.1$ nm, $\lambda_B = 435.8$ nm [1].

Let's consider example E_λ at $\lambda = 475$ nm [11]. At this wavelength $\bar{r}(475) = 0.045$, $\bar{g}(475) = 0.032$ and $\bar{b}(475) = 0.186$. Thus (20.5) becomes:

$$E_{475} = -0.045R + 0.032G + 0.186B \tag{20.6}$$

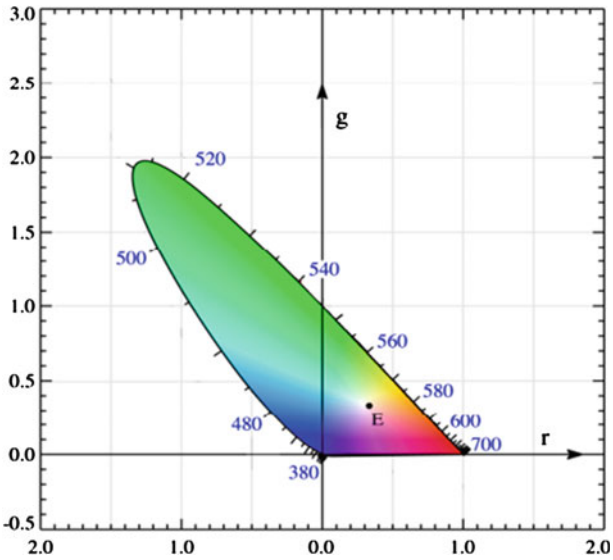


Fig. 20.2 1931 CIE RGB "*rg*" chromaticity coordinates

The negative value of red means that in the actual color matching $0.045R$ had to be added to E_{475}:

$$E_{475} + 0.045R = 0.032G + 0.186B \tag{20.7}$$

Chromaticity coordinates could be obtained from the color matching functions using following equations:

$$\begin{aligned} r(\lambda) &= \frac{\bar{r}(\lambda)}{\bar{r}(\lambda) + \bar{g}(\lambda) + \bar{b}(\lambda)} \\ g(\lambda) &= \frac{\bar{g}(\lambda)}{\bar{r}(\lambda) + \bar{g}(\lambda) + \bar{b}(\lambda)} \\ b(\lambda) &= \frac{\bar{b}(\lambda)}{\bar{r}(\lambda) + \bar{g}(\lambda) + \bar{b}(\lambda)} \end{aligned} \tag{20.8}$$

With

$$r(\lambda) + g(\lambda) + b(\lambda) = 1 \tag{20.9}$$

The entire set of r and g solutions of (20.9) is called *spectral locus*, and is shown on Fig. 20.2. In the 1931CIE color matching experiment the units of the R, G, B were chosen in the radiant power ratio 72.1:1.4:1.0. This ratio places chromaticity point of equal-energy stimulus E at the center of the (r,g) chromaticity diagram, as illustrated in Fig. 20.2.

After color matching functions introduction it is possible to determine the tristimulus values of the color stimulus Q defined by a spectral radiant power distribution $\{P_\lambda d\lambda\}_Q$ that is not restricted to a narrow bands. If further assumed that P_λ is a continuous function in the visible spectrum, then tristimulus values of Q will be given by:

$$\begin{aligned} R &= \int_{\lambda_a}^{\lambda_b} P_\lambda \bar{r}(\lambda) d\lambda \\ G &= \int_{\lambda_a}^{\lambda_b} P_\lambda \bar{g}(\lambda) d\lambda \\ B &= \int_{\lambda_a}^{\lambda_b} P_\lambda \bar{b}(\lambda) d\lambda \end{aligned} \tag{20.10}$$

20.2.4 *RGB to* XYZ *Colorimetric System*

Color matching functions $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, $\bar{b}(\lambda)$ and corresponding chromaticity coordinates include negative values. This is very inconvenient when tristimulus values are evaluated from spectral radiant power distribution (20.10). Sign change in color matching function also made the development of direct-reading photoelectric colorimeters difficult. Thus after *RGB* space development members of CIE developed another color space.

Assuming Grassman's law is true, new color space is related to *RGB* color space by linear transformation. New X, Y, Z primary stimuli are presented on Fig. 20.3. The standardized transformation from *RGB* to *XYZ* CIE agreed upon [5] is summarized in Table 20.1.

Using above transformation Fig. 20.2 will be transformed into Fig. 20.4. CIE 1931 *xy* chromaticity coordinate space is widely used for chromaticity specification. The *xy* chromaticity diagram represents all of the chromaticity visible to the average person and this region is called the gamut of human vision. The curved edge of the gamut is called the spectral locus and corresponds to monochromatic light with each point representing a pure hue of a single wavelength. All visible chromaticities correspond to nonnegative values of X, Y, and Z and therefore to nonnegative values of x and y. All the colors that lie in a straight line between the two points can be formed by mixing these two colors and this is valid for any two points of color on the chromaticity diagram. But an equal mixture of two equally bright colors will not generally lie on the midpoint of that line segment.

In more general terms, a distance on the *xy* chromaticity diagram does not correspond to the degree of difference between two colors. The system "equal energy point", or in other words light with, in terms of wavelength, equal power in every 1 nm interval, corresponds to the point $(x,y) = (1/3,1/3)$, as in ***rg*** coordinate system. Another important point is that the CIE *XYZ* color space was deliberately designed so that the Y parameter was a measure of the brightness or luminance of a color, thus very often in the literature term *xyY* color space is used.

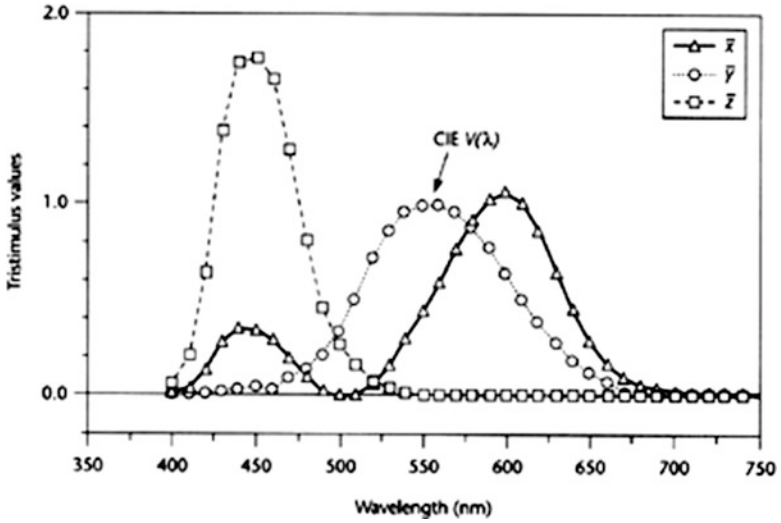


Fig. 20.3 CIE 1931 *XYZ* color matching functions with corresponding *xy* chromaticity coordinates

Table 20.1 *XYZ* to *RGB* transformation matrix

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \frac{1}{b_{21}} \begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$
$$= \frac{1}{0.17697} \begin{bmatrix} 0.49 & 0.31 & 0.20 \\ 0.17697 & 0.81240 & 0.01063 \\ 0.00 & 0.01 & 0.99 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

20.2.5 CIE 1960 and 1976 Color Coordinate Systems

Nonuniformity of *xy* color coordinate system leaded to attempts to design a new color coordinate system. Judd determined that a more uniform color space could be found by a simple projective transformation of the *XYZ* tristimulus values [12]. MacAdam simplified Judd's approach for computational purposes [13], that later was accepted as CIE 1960 *uv* coordinate system[14].The relationship between *xy* and *uv* coordinate system is given by:

$$u = \frac{4x}{12y - 2x + 3}$$
$$v = \frac{6y}{12y - 2x + 3} \tag{20.11}$$

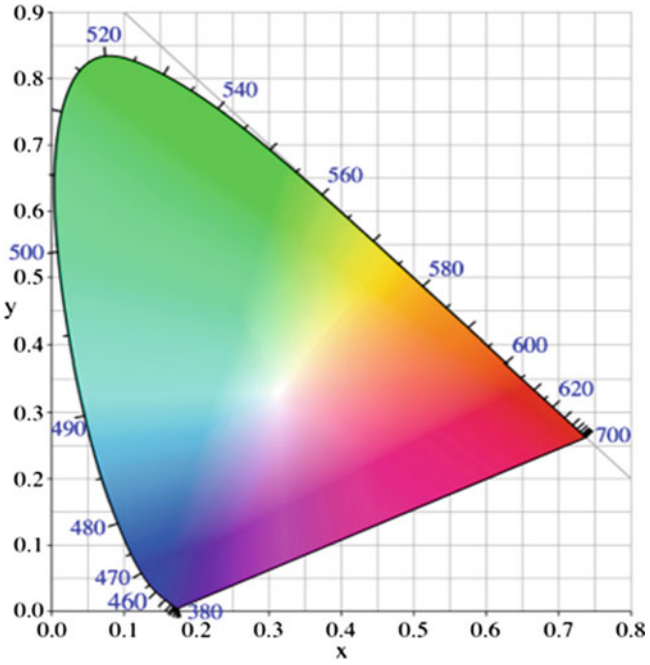


Fig. 20.4 CIE 1931 color chart

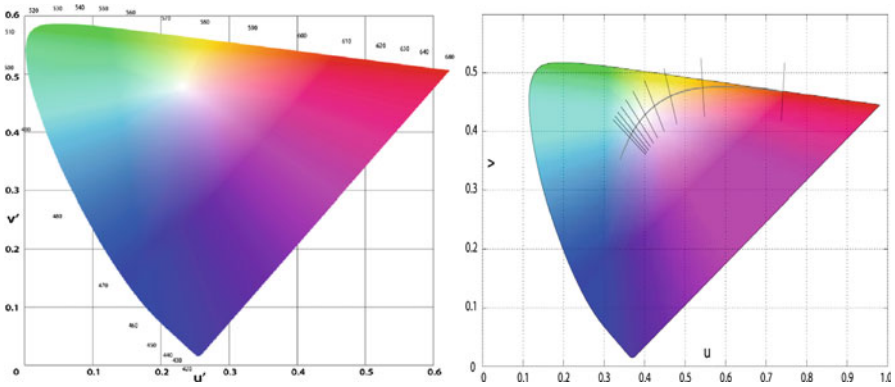


Fig. 20.5 CIE 1960 *uv* and CIE 1976 $u'v'$ uniform chromaticity coordinate systems

Another popular coordinate system is the CIE 1976 ($u'v'$) color space, commonly known by CIE uniform color space [33]. Transformation from the 1931 CIE *XYZ* color space to CIE 1976 could be found in 2nd edition of Colorimetry [15]. Below is given simple relationship between *xy* and $u'v'$ coordinate system (Fig. 20.5):

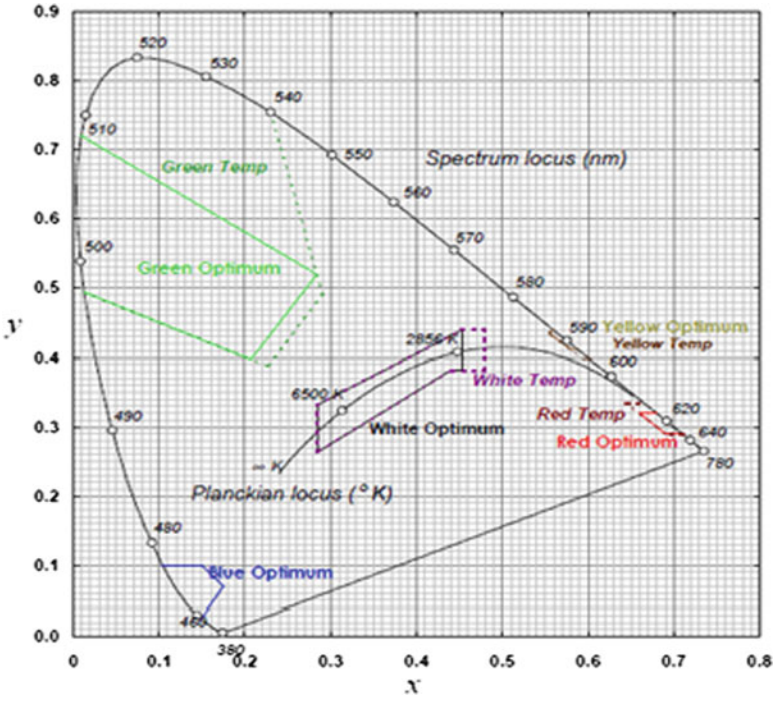


Fig. 20.6 CIE 1931 (x,y) chromaticity diagram with recommended domains for signal lightings

$$x = \frac{9u'}{6u' - 16v' + 12}$$
$$y = \frac{4v'}{6u' - 16v' + 12} \tag{20.12}$$

20.2.6 Specification of Color Tolerance

The set-up of color tolerance is extremely important for industrial applications. The main methods used in specifying color tolerances are based on acceptable values for quantities computed from measurements.

In that respect the CIE system of color specification is commonly used. Example of such tolerance specification is shown in Fig. 20.6 the polygon delimits an area inside which the color variability is defined as acceptable by CIE in the context of signal lights [16].

In the industry it is required to specify not only color difference within the given product but acceptability of color variations between a given standard and its reproduction. The perceptibility of a color difference is a visual judgment, which

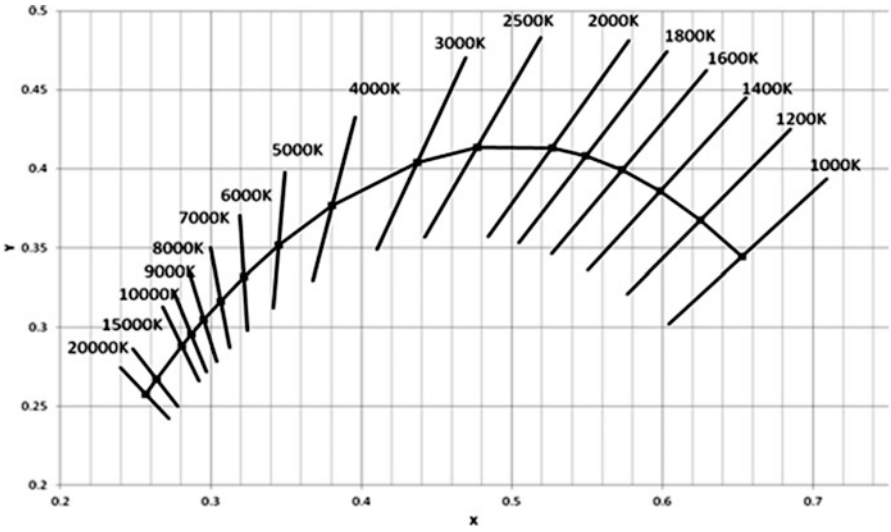


Fig. 20.7 CIE 1931 diagram with iso-thermal lines

is biased by considerations involving the intended application [8]. In the context of white light source, color temperature and correlated color temperature are terms used to specify color tolerance. The color temperature of a light source is the temperature of an ideal black-body radiator that radiates light of comparable hue to that of the light source. Color temperature is conventionally stated in the unit of absolute temperature (K). The term correlated color temperature was introduced when the chromaticity of a fluorescent lamp was not exactly equal to the chromaticity of the black-body radiator. The correlated color temperature (CCT) is defined as the temperature of the black-body radiator whose perceived color most closely resembles the color of the selected fluorescent lamp at the same brightness. Judd [17] was the first who proposed the terms of iso-temperature lines for the evaluation of CCT, later iso-temperature lines were computed by Kelly [18]. Figure 20.7 shows Planckian locus (black-body line) with iso-temperature lines in white domain.

20.2.7 Average Minimal Perceptible Color Difference: MacAdam Ellipses

Visual sensitivity to small color differences is the essential factor determining the precision of color matching. The first systematic studies of matching precision in different parts of tristimulus space were made by MacAdam [19]. He set up an experiment in which an observer viewed two different stimuli, at a fixed luminance of about 48 cd/m^2.

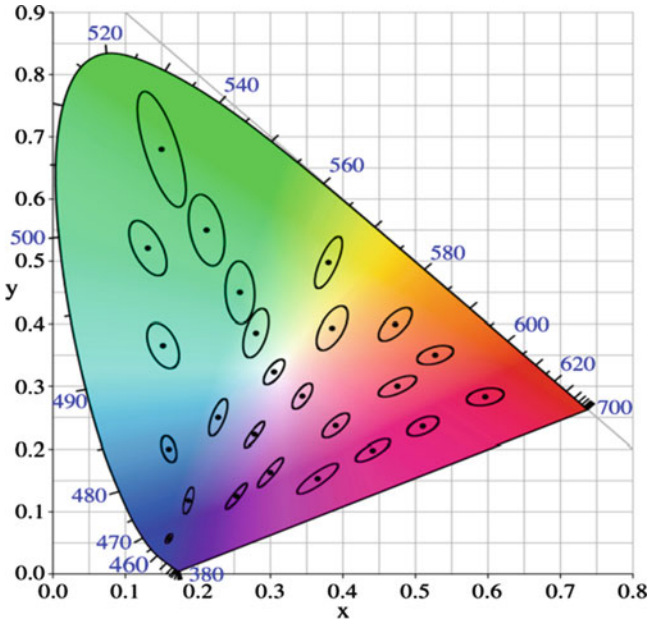


Fig. 20.8 CIE 1931 diagram with MacAdam ellipses. The axes of the plotted ellipses are ten times their actual lengths

One of the stimuli was fixed and the other was adjustable by the observer. The observer was asked to adjust that color until it matched the test color. Both fixed and variable stimuli were mixtures of the same set of red, green and blue primaries. The JND, "just noticeable difference" was found to be about three times as large as the corresponding standard deviation. It was found that all of the matches made by the observer fell into an ellipse on the CIE 1931 chromaticity diagram. The measurements were made at 25 points on the chromaticity diagram, and it was found that the size and orientation of the ellipses on the diagram varied widely depending on the test color. These 25 ellipses measured by MacAdam, for a particular observer is shown on the chromaticity diagram on Fig. 20.8.

MacAdam ellipses have following major strengths: they are easy to see, easy to understand, and easy to explain. Also MacAdam ellipses are specified in *xy* chromaticity coordinates, which is the standard color space for reporting colorimetric data in the illumination industry, for example ANSI C78.376-2001 Chromaticity specification for the fluorescent lamps. In this chapter we define an "X step MA ellipse" as: centered on a given point, those ellipses are circles in $u'v'$ space, with a *radius* of X SDCM. ANSI C78.378 standard is modified fluorescent specification to meet the needs of SSL products [20].

It defines quadrangles rather than ellipses on chromaticity diagram (Fig. 20.9). Size of this quadrangle is based on 7-step MacAdams ellipse. On Fig. 20.10, 3,000 K quadrangle is shown with 1, 3, 5 and 7-step MacAdam ellipsis. Center

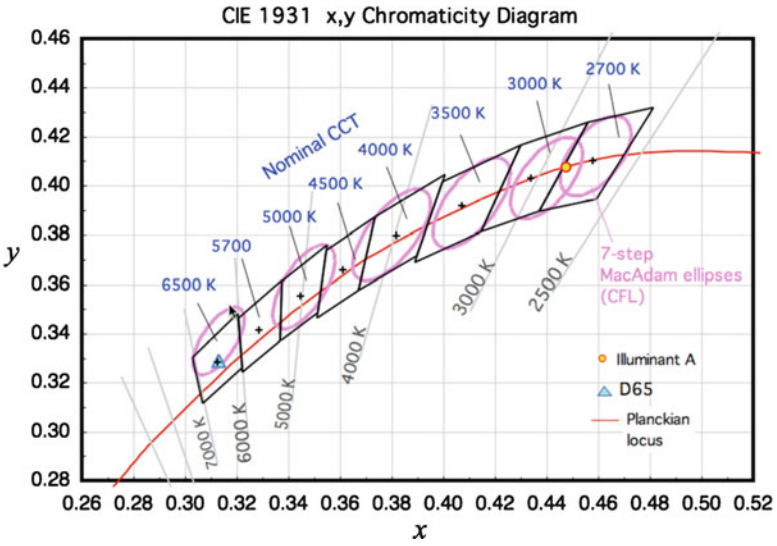


Fig. 20.9 ANSI bin definitions from Energy star. The quadrangles contain a 7 step MA ellipse [21]

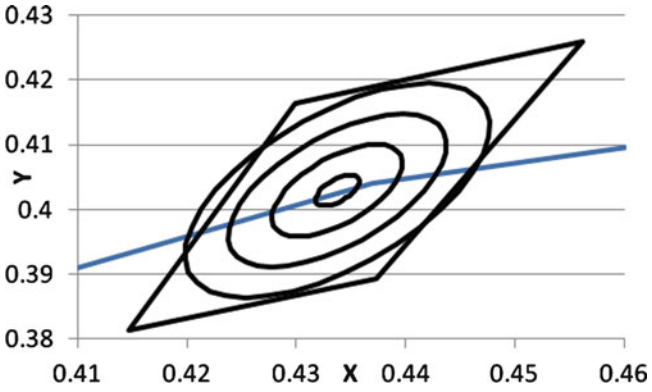


Fig. 20.10 ANSI 3,000 K quadrangle and 1, 3, 5, 7 MA ellipses

point of this quadrangle and MacAdam ellipses is 3,045 K ($x = 0.4338$; $y = 0.4030$) by ANSI definition. Figure 20.9 shows the ANSI recommendations over the entire white color space.

LED makers test their products for several parameters including position on xy chromaticity diagram, by defining a xy box and calling it a color bin. Prior to standardization LED manufacturers were free to define such xy boxes. After successful introduction and following wide adoption by industry of ANSI binning standards, luminiare manufacturers realized that 7 steps SDCM is too broad

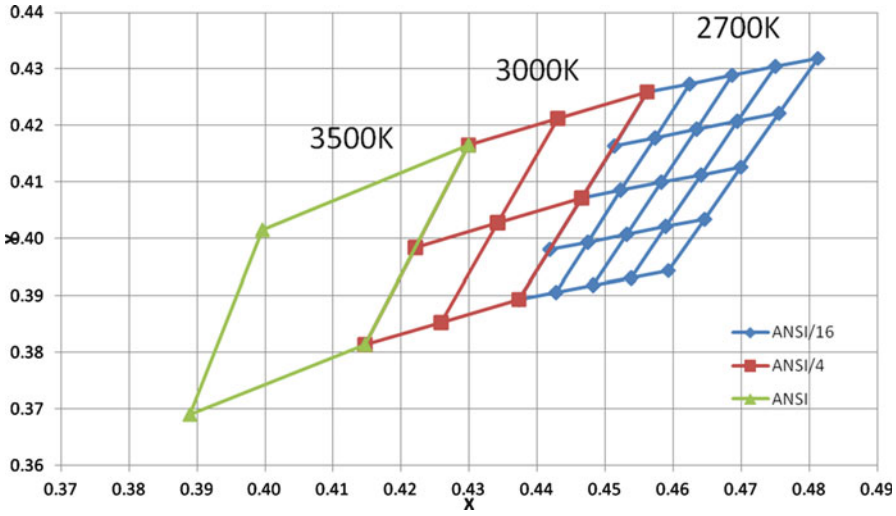


Fig. 20.11 ANSI quadrants: 3,500 K—7 step ANSI, 3,000 K—ANSI/4, 2,700 K—ANSI/16

specification for several applications. LED manufacturers addressed market need for better color consistency by introducing more granularities in already defined 7 step ANSI specification. First step is to divide ANSI quadrant by 4 using iso CCT line (same correlated color temperature) and black body line. Such binning scheme is known by ANSI/4. Second step is to divide each ANSI/4 space on 4 more quadrants. This binning scheme is known as ANSI/16. ANSI, ANSI/4, and ANSI/16 are shown on Figs. 20.10 and 20.11.

20.3 Binning Optimization: Rationale, Definition and Methods

LEDs are generally sold in "bins", as seen on previous section for color bins. Other parameters can also be binned, for example, luminous flux, radiant flux, forward voltage Vf, etc. The goal of the system architect is to obtain a *fixture* color point, flux and forward voltage within a given tolerance. Complete (final) fixture requirements on color consistency is not the same as an individual LED specification—for example, simply adding tolerances of each parameter would lead to very large numbers. Furthermore, the system architect must obtain a *reliable* specification. We will explore methods to provide a reliable, consistent specification, taking into account, and taking advantage of LED variability, in each parameter, and in time. This review will take into account:

1. LED measurement tolerances given by the manufacturer
2. LED binning scheme
3. LED evolution with time ("lumen maintenance" and "color shift")

We will only take color point and flux into account in this paper, and limit to white LEDs. Though, the approach is still fully applicable to any other parameter or LED color (RGB, WRGB, etc.) as they can be described the same way.

Formally, to average and calculate easily, we need an additive system (any parameter P where the results for 2 LEDs is the average or the sum of the results of each individual LED). For this reason we use the CIE1931, which is an additive color system (example, two LEDs of color coordinates X_1 and X_2, will result in a color point of coordinate $X_r = (X_1 + X_2)/2$). With this choice of color space, a bin B_i of LEDs is defined as a vector of three components X_i, Y_i, Z_i, plus for instance a fourth component Vf_i:

$$B_i = [X_i Y_i Z_i Vf_i] \tag{20.13}$$

For example, ANSI/4 structure, which is the ANSI bin, subdivided in four quadrants, for a given LED, with bins of average XYZ, and an average Vf of V can be described as

$$B = \begin{bmatrix} XA & YA & ZA & VA \\ XB & YB & ZB & VB \\ XC & YC & ZC & VC \\ XD & YD & ZD & VD \end{bmatrix} \tag{20.14}$$

This matrix size is $M \times N$, M being the number of parameters to take into account (here 4) and N being the number of bins of the binning structure.[1]

Note that this matrix can contain color, Vf, but also *any parameter than can be expressed as an additive quantity* (any parameter P where the results for 2 LEDs is the average or the sum of the results of each individual LED). For example the spectra could be added, to enable CRI or wavelength optimization or different color point system calculation (RGB etc.).

A possible way of working to reach a given color specification is to manually choose and select in every case the LED bins. To allow a better control and a faster processing method, we are looking for a method to process LED specifications with a given formalism, only difference specification to specification being how the LEDs are chosen and placed together.

20.3.1 Generalized Formalism of Binning Optimization

The specification is X, a known color point, flux, or other, with an acceptable tolerance, given by the fixture designer, on the final result, is $D = [DX\ DY\ DZ$

[1] In this example, the number of rows is $4 \times 1 \times 1 = 4$. With ANSI/16, 3 bins of flux and 3 bins of Vf, the matrix then contains $(16 \times 3 \times 3) = 144$ rows.

DVf]. The LEDs are mixed together, in quantities defined by the vector α. For example, with 4 bins, and $\alpha = [0\ 0.2\ 0.5\ 0.3]$ means mixing ratios of the four bins B1, B2, B3, B4 of 0 %, 20 %, 50 % and 30 %. The vector α can also be written in quantities of LEDs per bin, for example $\alpha = [0\ 4\ 8\ 8]$ with $4 + 8 + 8 = 20$ LEDs in the fixture.

We can write our target for which this tolerance applies as $X = [x0\ y0\ Y0\ Vf0]$ in this example.[2] With this formalism, the general problem of a reliable specification can be written by:

$$\left|\sum \alpha_i B_i - X\right| < D \tag{20.15}$$

This equation falls into the "Linear Optimization" set of problems, and extensive literature exists on methods to solve those sets of equations. This inequality must stay true at any point in time and in the operating conditions. The goal here is then to solve this inequality and find the sets of α which satisfy the specification

It is not solvable analytically in most cases but several methods can be used to solve it.

An interesting effect is also that the left part of the inequality can be written fully when testing subsets *and such the result can be converted in any unit to compare to D or to D + X*. For example, spectra can be used in the left part, and the end result can be a CRI or peak wavelength value, which can be compared to the tolerance D. This is useful as we will often calculate using *XYZ* system and compare to a tolerance in $u'v'$. In this case we can write the general problem to allow nonadditive optimizations (limit 1 and limit 2 in (20.1) are $X - D$ and $X + D$). Thus, Only B_i has to be additive quantities, and f is any function which output is numeric:

$$\text{Limit 1} < f\left(\sum \alpha_i B_i\right) < \text{Limit 2} \tag{20.16}$$

Then, the goal is to evaluate the central part, convert it to the proper system or units, and compare with the predefined limits. The goal of our methods is to propose one or several sets of vector α, the other parameters being either specified separately (amount of B_i, tolerance D), or derived from the actual technological parameters (shift with temperature, current, time). We can list several binning methods:

1. All LEDs in spec (initial distribution selection, no binning)
2. Case by case (manual binning)
3. Complete solution scan method
4. Newton method (trial and error)

Other binning methods exist but are based on the four described below:

[2] Using a α vector of length 1, the target X must be normalized as an average per LED.

20.3.2 Method 1: All LEDs in Spec

The goal of this method is to only consider LEDs which are within the final fixture specification, by forcing (20.15) or (20.16) to be true in all cases. This method allows for a complete control of the specification, but does not allow reaching extreme specifications on large quantities of products. All the B_i are preselected to be within the tolerance, so any combination of B_i stays within the tolerance. The risk added by this method is a risk of low utilization, as described in the following example:

Given a distribution of *Vf*, Flux and color, where the specification has a yield of 50 % on each parameter, the final specification yield, or "utilization factor", is $0.5^3 = 12.5$ %.

That forces the LED manufacturer to reroute 87.5 % of its production to other specifications, and is in general considered as a major risk for large volume products. However, recent developments showed this could be done at LED level [22], and such, allow extreme color consistencies by using for example the rest of the results of this paper.

20.3.3 Method 2: Case by Case (Manual Binning)

This method provides a reliable control of the final result, and is mathematically solving (20.15) or (20.16) on a every received shipment, with a subset of B_i (the received LED bins). The base principle is to accept large quantities of bins, in our outside the specification, on a *predetermined distribution centered within the specification*. It is easy to implement; however, it requires intensive effort and maintenance in operation for large volumes of shipments.

20.3.4 Method 3: Complete Scan Method

LEDs can be seen as a "scarce source". The price, in general, is not negligible in the fixture cost, and a smart use of the variability can be a great benefit for the fixture manufacturer to maximize the usage of the production distribution. In more precise terms, it is possible to find the largest subset of B_i, *even if the individual* B_i *are outside the specification*, so that the *mixing* of LEDs is within specification. It adds a constraint: the product must allow such feature to be acceptable, but it adds a considerable flexibility. This method gives the comprehensive set of solutions α based on all possible B_i combinations and gives the largest LED distribution utilization. Let's first define a set of acceptable bins (B_i). We write the entire space of combinations of α

Example with 3 light sources with 4 acceptable bins

α (choice 1) = [0 0 0 4]
α (choice 2) = [0 0 1 3]

...
Etc. till

α(choice N) = [4 0 0 0]

The algorithm will cycle through the α sets (or use matrix methods), and store each set of α which allows to reach the specification. The limit of this exhaustive method is the computational power. The space to explore increases as the number of LEDs to the *power* of the number of bins which limits the method to a small set of accessible bins and number of LED sources. Example: binning ANSI/4, 16 LEDs: the size of the explored space is $16^5 = 1{,}048{,}576$ combinations (10^6), which can be explored using a standard computer and proper software. With ANSI/16 and 8 LEDs, the size of the space is $8^{17} = 2.2 \times 10^{15}$. This matrix size is challenging even for modern methods and software.

In many practical cases, "sub assembly" techniques can be used to solve the computational problem for larger LED counts, for example, by defining a sub pattern, optimizing on the pattern, and multiplying the pattern. This will reduce the solution set compared to the full method, but enable computation to be ran.

20.3.5 Method 4: Simplex Method

The second method is often nicknamed "Newton's method" and is based on the Simplex algorithm [23]. We start from a set of α (a random fixed set of bins), and we will permute one light source by another. This is equivalent to write a matrix of permutations, and test each of them. In detail:

We calculate one "distance" from the fixed starting set:

$$\text{Dist} = \sum \alpha_i B_i - X \tag{20.17}$$

- We permute one light source by another randomly (one of the alpha will be reduced by one, another will be raised by one).
- We compare this "distance" Dist with the previously calculated distance.
- If the distance decreased (norm of dist reduced), we will keep on doing the same permutation.
- If the distance increases, we try another random permutation.
- If we run into a cycle, try a new random starting set.

With modern software, it is also possible to define the entire set of permutations, and test every possible permutation to find an optimal route. The main advantage of

this method is to allow exploring any kind of set of bin structure, regardless of its size, number of LEDs, and number of bins. The main drawback is to be a trial and error method, which will not find all solutions, and often converge in local minima. This set of algorithms allow for coverage of all practical cases.

20.3.6 Choosing the Right Method

A practical problem one faces when trying to optimize binning is the choice of the right method. The key parameters to consider for a proper choice are the number of bins and the number of LEDs. By calculating the space size (L^B), one can directly estimate if the "Complete Scan" method is appropriate given the available software/hardware infrastructure. Knowledge of the number of LEDs will help to estimate if the Newton method, with full set of permutations is correct, or if the Newton method with random permutations can be used.

20.3.7 Example of Applications: Large Number of LEDs, Few Bins

In this example we will consider a hypothetical luminiare made of 80 LEDs and 4 bins. The specification is to reach the center of those 4 bins, with a tolerance of the size of one of the single bin, with a voltage specification of the average sum of 80 of those LEDs, and a tolerance of for example 10 %. After converting in the proper additive units, we need to build the matrix B_i and the vector D, and write equation (20.17). Estimating if the complete scan method can be used, we see that the space size is about 41×10^6. Such space is processable on any computer.

Execution of the algorithm will deliver a list of solutions α, as defined above, each of them being a recipe which guarantees the color mixing to be within the defined specification. As LEDs are binned separately in color and Vf, the solutions have to be organized by Vf solutions (In other words, the solutions are a 3 dimensional matrix, so visualization can be a challenge).

20.3.8 Bridging with Real Conditions: Distributions and Intrabin Variability

Depending on the size of the bins, it is important to prove that the entire set of solutions is within the specification, taking into account the production variations:

- Color points or voltage are variable with current, temperature.
- Color point or voltage are not necessarily centered in their respective bins ("corner samples").

First point can be easily adjusted by shifting the specification to the operating condition, assuming a constant shift from LED to LED. This is technology dependent from the manufacturer and such can be solved on a case by case basis. We will discuss the second point in this next section

20.4 Color Point of an Optimized Product Made of *N* LEDs

In the present state of the technology, an LED cannot be fabricated in a deterministic way at a precise color point. Instead, LEDs come out of the fabrication chain with a certain probability of being of a particular color, and are sorted and binned. Each bin generally has a rhomb shape (we will consider squared shape here for simplicity) in (XZ) plane of side length l (in SDCM units). The bin size depends on the manufacturer and standards. Color bins units are xyY system or $u'v'$, and the tolerance unit is the "SDCM", expressed in $u'v'$, as defined in Sect. 20.1. In other words, when the customer purchases LEDs within a given color bin, LED shipments will consist of LEDs of identical color plus or minus $l/2$ SDCM with respect to the center of the bin. The probability to get a precise color within its bin is given by a distribution $D_1(u',v')$.

20.4.1 Relevance of the Central Limit Theorem

Let's discuss a real situation, with LEDs provided in a way described above: a product is composed of several LEDs.

- What is the color point of this product? How is this color point distributed from product to product? How is it distributed compared to the single LED distribution within each bin used?
- After applying optimization defined in previous section, and listing all the binning scenarios which were made on "perfect" color points centered in their bins, what is the "real" color distribution including all sources of variability?
- What is the color point of this product and how is this color point distributed from product to product, as compared to the single LED distribution within each bin used and the bin size a?

There is a straight and simple answer to that question which is provided by a result of statistical mathematics: the central limit theorem [24]. Rephrased in our context, it can be formulated in the following way:

For a product made of a large number N of LEDs, (i) the distribution of its color point turns into a normal distribution whatever the shape (flat, linear, normal. . .) of the single LED distribution D_1. (ii) The distribution gets narrower and narrower for increasing N. Its variance $\sigma_N{}^2$ eventually decreases like $\sigma_1{}^2/N$, where $\sigma_1{}^2$ is the variance of D_1.

20.4.2 General Properties on the Color Point of an N-LED Product

In the following discussion we are going to determine analytically the distributions of the product color, and verify that it is consistent with the prediction of the central limit theorem. To do so, we will use a vector representation $\boldsymbol{a} = (a_{u'},a_{v'})$ of the color points in the bi-dimensional plane (u',v'). Importantly, we are using an additive color space (*XYZ*, CIE1931), i.e., if two sources have two different coordinate in this space, the color resulting from their overlap is given by the mean value of their coordinate.

Then, a product of color $\boldsymbol{A}$ which is made out of N LEDs each taken within $M < N$ bins of coordinate a_i verifies

$$A = \frac{1}{N}\sum_{i=1}^{M} n_i a_i \tag{20.18}$$

where n_i, $(N = \sum n_i)$ is the number of LEDs taken within bin i. This vector $\boldsymbol{A}$ is the resulting color obtained for one set of LEDs, and optimized as described in previous section. Now, if we repeat the same operation, i.e., we choose a new set $\{a_i'\}$ of N LEDs in the same way as previously, and make a second product with them tentatively identical to the first one. As a result, we will obtain a color $\boldsymbol{A}'$ different from $\boldsymbol{A}$ since the LEDs colors can vary, in agreement with the finite size of the bin, and the color of the bin they are taken from.

The question that we are trying to address is how to *determine quantitatively the statistical distribution D_N of all the **A's** obtained in the same way*.

Equation (20.18) provides a first interesting property of D_N in our context which results from the linear relationship between $\boldsymbol{A}$ and the a_i's. We assume that all the bins have the same squared shape of side length r like shown schematically in Fig. 20.1. Let us consider a given set of $\{a_i\}$ and shifts them all by a constant vector $\boldsymbol{s}$. Then it is easy to check with (20.18) that $\boldsymbol{A}$ also shifts by $\boldsymbol{s}$. A consequence of this fact is that since the single LED distribution D_1 is by definition entirely contained within the considered bin (of squared shape, and side length l), then the color distribution D_N of the N-LED product is also entirely contained within an identical squared shape surface of side length l.

This is illustrated on Fig. 20.12 for a 4-LED product: A_1 is the surface in color space which entirely contains D_4, the color distribution of a product fabricated by picking one LED from each of the four bins 1–4, based on one of the scenarios of previous section.

A_2 is the resulting surface for a different product, made of 2 LEDs from bin 4 and 2 LEDs from bin 3. Although having a different average color (position in the plane), A_1 and A_2 both have the same shape and size. Of course this conclusion wouldn't hold if every bin had different shapes (then the final surface would be a convolution of the different shapes). In this case, A_1 and A_2 would have a different

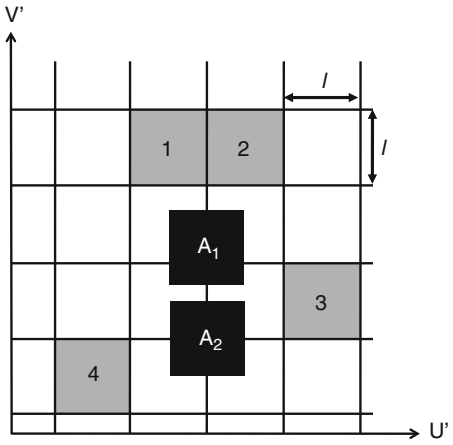


Fig. 20.12 Schematic representation of bins in color space. *Schematic representation of bins in color space. Each square represents a color bin. Bins labeled from 1 to 4 are used to manufacture a multiple LED product (see text). A_1 sets the edges of the color distribution of a product featuring one LED of each bin 1–4. A_2 sets the edges of the color distribution of a product featuring 2 LEDs in bin 4 and 2 LEDs in bin 3. l is the size of the bin in this color space*

shape which can be obtained using (20.18) and with sets $\{a_i\}$ where each LED is located on the edges of its bins.

20.4.3 Exact Derivation of D_N

We have understood how to determine the position and edges in color space of A_N which contains D_N (u,v). Let us discuss now how to determine quantitatively $D_N(u,v)$, provided $D_1(u,v)$ the color point probability distribution of a single LED is known. The occurrence probability $D_N(\boldsymbol{a})$ of color point $\boldsymbol{a}$ $(a \in A_N)$ of the N-LED is reads

$$D_N(a) = \iint_{B1} \mathrm{d}^2 a_1 \iint_{B2} \mathrm{d}^2 a_2 \ldots \iint_{BN} \mathrm{d}^2 a_N \times D_1^{B1}(a_1) D_1^{B2}(a_2) \ldots D_1^{BN}(a_N) \delta(a_1 + a_2 + \ldots + a_N - Na) \tag{20.19}$$

where each $\boldsymbol{a_i}$ runs over the surface of each bin B_i, $D_1^{B_i}(a_i)$ is the single LED distribution of bin i, and δ is the Dirac function. This expression selects every set of variable $\{\boldsymbol{a_1}, \boldsymbol{a_1}, \ldots \boldsymbol{a_N}\}$ which contribute to the color point $\boldsymbol{a}$ (by setting the argument of the Dirac function to match (20.18), and sums the probability of occurrence of every sets. Interestingly, this complicated expression can be rewritten in a simpler way in terms of successive convolutions of the $D_1^{B_i}$'s:

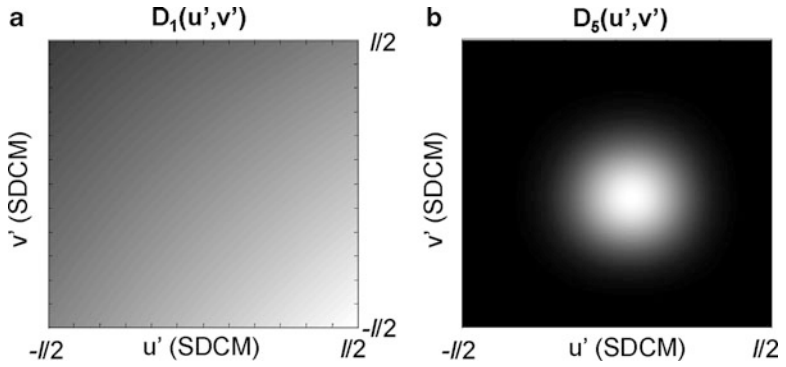


Fig. 20.13 (**a**) Distribution function $D_1(u',v')$. The frame is limited to the bin size a. The magnitude of D_1 is color coded in *black and white*: The whiter the larger. (**b**) Calculated distribution function $D_5(u',v')$. Note that the distribution is shifted

$$D_N(a) = [D_1^{BN} * D_1^{BN-1} * \ldots * D_1^{B1}](Na) \tag{20.20}$$

where "*" stands for the convolution operation $[f * g](t) \equiv \int_{-\infty}^{+\infty} f(t')g(t-t')dt'$.

Equation 20.21 is very general: it can be used whether every $D_1^{B_i}$'s are different or not.

Another property of this formula is that *the shape of the distribution is not affected by the* relative *positions of bins Bi with respect to each other, but depends only on the shape of the* $D_1^{B_i}$*'s and on N*. For the sake of illustration we have applied this method to a *N*-LED product where every LEDs have the same single LED distribution (in terms of shape):

$$\begin{aligned} D_1(u',v') = {} & H(u'+l/2)H(-u'+l/2)H(v'+l/2)(-v'+l/2) \\ & \times (u'v'/4 + lu'/2 + lv'/2 + 2l) \end{aligned} \tag{20.21}$$

Where the center of the bin is arbitrarily set to ($u' = 0$, $v' = 0$) and H is the Heaviside function which sets the distribution equal to zero out of the squared bin of side l. We chose to use this distribution which is monotonically increasing from the upper left corner of the bin to the lower right corner because it mimics a realistic one that results from the fabrication process of LEDs, and the subsequent subdivision into several bins. D_1 is plotted in Fig. 20.13 in shades of grey.

Then, using the expression derived above, we calculate $D_5(u', v')$, the color point distribution of a product made of 5 LEDs. The result is shown on Fig. 20.13b. *As expected from the central limit theorem, the distribution width has substantially decreased with respect to that of* D_1 *and the distribution shape resembles already quite accurately a normal distribution (a Gaussian of revolution in this case) in spite of a small* $N = 5$.

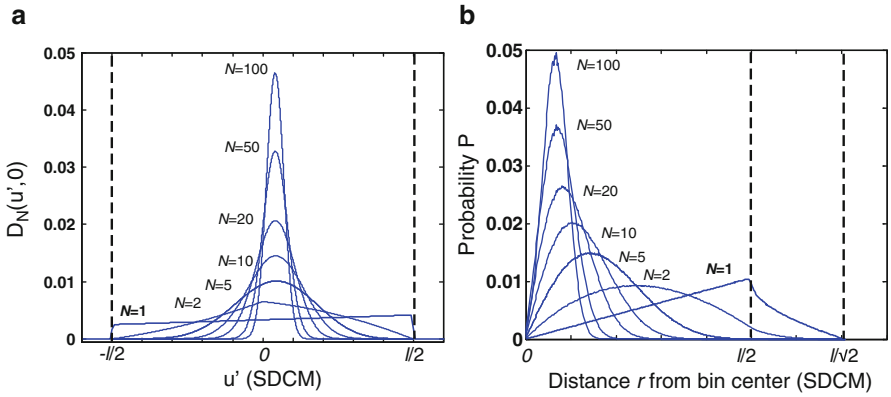


Fig. 20.14 (**a**) $D_N(u',0)$ for $N = 1, 2, 5, 10, 20, 50, 100$. The *dashed lines* show the edges of the bin (that at $r\sqrt{2}$ is half the length of the diagonal of the squared bin). (**b**) Probability distribution $P(r)$ of finding a product of any color situated at a distance d from that of the target color point (assumed to be the mean value of the distribution)

To show this result more quantitatively, we plot $D_N(u',0)$ in Fig. 20.14b for several N from 1 to 100.

From the fixture manufacturer point of view, two useful quantities can be easily computed out of the D_N. A first quantity is the answer to the question "*by how much will my N-LED product deviate from the exact color I target, regardless of the direction of that deviation in the color space?*". Assuming that the LEDs have been chosen so that this target is the average value $< \boldsymbol{a} >$ of the distribution, the probability $P_N(r)$ to find a product that is shifted by exactly r (in SDCM) from the target is obtained by integrating the distribution within a ring of diameter r and centered on the target:

$$P_N(r) = \int_0^{2\pi} D_N(r,\theta) r \mathrm{d}\theta \tag{20.22}$$

where the distribution is D_N is defined in polar coordinate in color space, and $r = 0$ is set at the target color point. Such a calculation is shown Fig. 20.15, using the distributions shown Fig. 20.13. As expected, thanks to the central limit theorem, the probability of picking a product closer to the target increases for increasing N.

A similar quantity $P'_N(r)$ can be computed to answer to the question: *"what is the probability to pick a product which color point is contained within an area of radius r around the target?" :*

$$P'_N(r) = \int_0^r P_N(r')\mathrm{d}r' \tag{20.23}$$

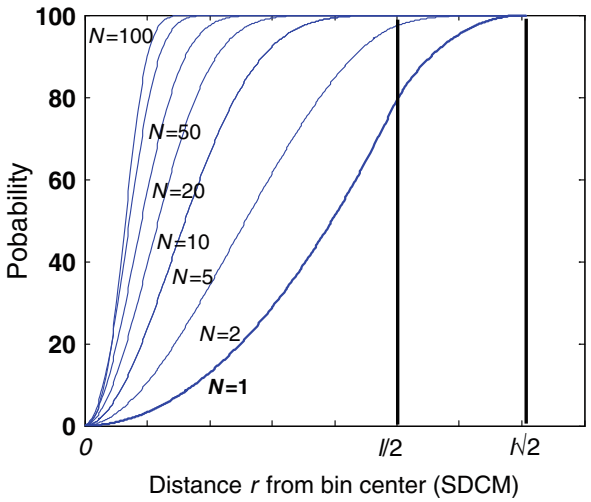


Fig. 20.15 $P'(r)$ for $N = 1$, 2, 5, 10, 20, 50, 100. The *dashed lines* show the edges of the bin

The result is shown in Fig. 20.15. Again, we see that thanks to the central limit theorem, the larger N the lower the color point dispersion around the target color.

As explained earlier, the distribution D_N needs to be derived explicitly in an additive color space. However, it can be represented subsequently into any other—nonadditive—color space using the right transformation.

20.4.4 Impact of Flux Differences on Color Point, Impact on Specification

Proper optimization of bins leads to the mixing of different flux bins. In this section we will look at the impact of flux differences on the resulting color point. SDCM distance from an average color point could be calculated when two LEDs have a different flux. By taking two LEDs on the corners of the "ANSI 7" bin (color points respectively $x = 0.4242$, $y = 0.3919$, and $x = 0.4449$, $y = 0.4142$), with a luminous flux of 100 lm for LED1 and a variable from 50 to 150 lumen on LED2 we can plot the resulting color point, and its shift from the average point (where both LEDs have a flux of 100 lm). Results are plotted on Fig. 20.16.

For an unrealistic flux difference of 50 %, average color shift is less than 2 SDCM. With a realistic 10 % difference, the color shift compared to the equal flux point is under 0.4 SDCM. For this reason we recommend executing an optimization on color *considering all fluxes as identical. Though, it must be verified that given color specification is below the impact of a flux difference, being the maximal width of the flux distribution.*

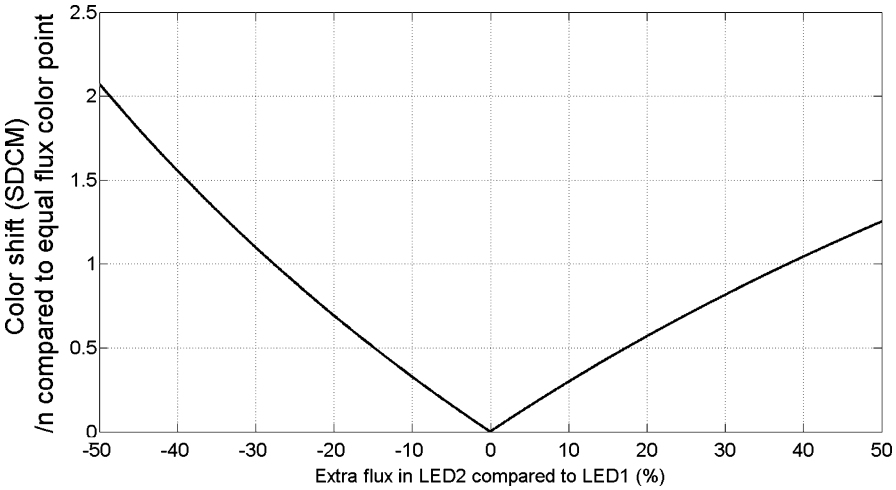


Fig. 20.16 Impact of a flux difference on the color point: 50 % flux difference shifts the color point of only 2.1 SDCM. 10 % shifts it of 0.3 SDCM

20.5 Technology and Method Limits

In this section, we will focus on answering three questions:

- What color consistency could be reached, given the current technology, taking all tolerances?
- What would be needed in the LED technology to reach the "limit case", 99.7 % of users seeing the same color, which can be expressed by a color consistency of 0.08 SDCM around a color point we will choose.
- Based on those results we will provide recommendations to reach "better color consistency"

20.5.1 Current Limits of the Binning Methods

Starting from ANSI bin structure on one "large ANSI bin" (bin 7) we will subdivide the bin in 1, 4 and 16. Those three subdivisions exist through the industry, as discussed earlier, and we will compare the results that can be reached with all three binning schemes. The rationale of the method is as follows:

- Fixed target point is in the center of the bin.
- We ignore shift over temperature, current and time.
- 99.7 % of our products must be within specifications ("3 sigma rule")

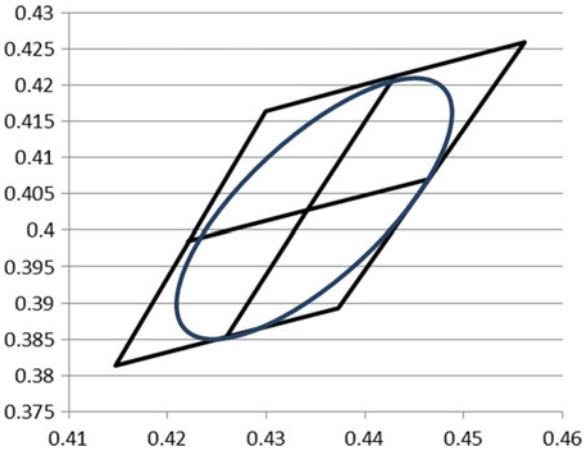


Fig. 20.17 ANSI bin 7 with four subdivisions ("ANSI/4") and a 7 step MA ellipse. The overall amplitude in SDCM of the full ANSI bin (corner to corner) is 19.5 SDCM

Two variables are used: subdivision of ANSI (1,4,16) and number of LEDs (Fig. 20.17)

Note that a significant portion of the ANSI quadrangle is outside the MA 7 ellipse. Table 20.2 shows, with an ANSI/16 subdivision, the distance from the center of the sub-bin to the ANSI center $x = 0.4338$ $y = 0.4030$. The full ANSI bin is contained in a *10* step MA ellipse, and thus individual LEDs can have a color distance close to 20 SDCM while being in ANSI bin 7. For ANSI/4 subdivision the distance can be 10 SDCM, and for ANSI/16 the distance can be 5 SDCM. The width in x&y of the bins are respectively 14, 7 and 3.5 for ANSI, ANSI/4 and ANSI/16.

We optimize 300 different products, with the number of LEDs ranging from 4 to 100. Using results from previous section, taking real bin shapes into account, and adding tolerances on optimized results, we obtain the following table (S99 is defined here as the "SDCM value for which 99.7 % of the population is within this SDCM distance from target", S90 for 90 %) (Table 20.3).

We can see from the table above that the binning subdivision has a considerable impact on the reachable color consistency specification. Second to that, the number of LEDs on the product, by the effect of the central limit theorem, leads to a narrower result, but the gain becomes limited past 32 LEDs.

20.6 The Route to Perfect Consistency

20.6.1 Further ANSI Subdivision

In this part we will demonstrate the achievable color consistency vs. the number of LEDs, from a subdivision of the initial ANSI bin (/1, /4, /16). Considered a hypothetical specification is "99.7 % of the user population will not see a color

Table 20.2 Distance from center (center $x = 0.4338$ $y = 0.4030$) of ANSI sub-bin, in SDCM

ANSI sub-bin name	Distance from 3,000 K center $x = 0.4338$ $y = 0.4030$ in SDCM
7A1	9.2
7A2	5.9
7A3	3.0
7A4	7.2
7B1	4.8
7B2	6.9
7B3	6.0
7B4	2.1
7C1	3.3
7C2	7.2
7C3	9.6
7C4	6.5
7D1	6.5
7D2	2.7
7D3	5.4
7D4	7.4

Table 20.3 Reachable specifications versus number of LEDs and subdivision

Number of LEDs	Subdivision	S99 (SDCM from target for 99.7 % of the population)	S90 (SDCM from target for 90 % of the population)
4	ANSI	15.7	11.5
4	ANSI/4	6.3	3.9
4	ANSI/16	3.0	1.9
12	ANSI	11.4	11.4
12	ANSI/4	5.9	3.6
12	ANSI/16	2.4	2.4
32	ANSI	15.6	11.4
32	ANSI/4	5.8	3.5
32	ANSI/16	1.8	1.1
64	ANSI	15.7	11.4
64	ANSI/4	6.0	3.7
64	ANSI/16	1.6	0.9
100	ANSI	15.6	11.4
100	ANSI/4	5.1	3.1
100	ANSI/16	1.6	0.9

difference". This means the desired color consistency is 0.08 SDCM (Based on above definitions, we want S99 = 0.08). One can also calculate $S_x = 0.08$ (x—which will be calculated—is the population of products within this spec) in those cases. Figure 20.16 shows that the flux consistency of the individual LEDs has to be better than ±2.5 %. This value also follows the central limit theorem conclusions, and as such will be reduced like $1/\sqrt{N/2}$.

Table 20.4 Trying to reach perfect color consistency: limits

Number of LEDs	Subdivision	Population within spec (%) for $Sx = 0.08$	S99 from figure 20.15 // S99 from Monte Carlo simulation
4	ANSI/16	0 %	2.7 // 3
12	ANSI/16	1 %	2.1 // 2.4
32	ANSI/16	2 %	1.6 // 1.8
64	ANSI/16	3 %	1.4 // 1.6
100	ANSI/16	3 %	1.3 // 1.6

Table 20.5 A possible way to approach perfect consistency: further subdivision of ANSI

Number of LEDs	Subdivision	Population within spec (%) for $Sx = 0.08$	S99(SDCM)
4	ANSI/64	2	1.29
16	ANSI/64	3	0.88
32	ANSI/64	5	0.74
64	ANSI/64	11	0.59
100	ANSI/64	15	0.56

Taking results from Fig. 20.15 we need a target $d = a/43.75$ for ANSI, $d = a/21.9$ for ANSI/4 and $d = a/10.9$ for ANSI/16. This cannot be reached with ANSI, ANSI/4, and ANSI/16, even with large amount of LEDs, as illustrated in Table 20.4.

From this table, we can see the abacus Fig. 20.15 can be used as a reference point to quickly estimate color consistency limits. Extending the result further, ANSI/64, allowing to write $d = a/5$, gives the results shown below (Table 20.5).

Note that tolerances on the color point within the bin ("tester tolerances") are following the results from the central limit theorem, and as such reduce as $1/\sqrt{N}$. Thus, they become negligible as LED count raises and should not be taken into account when designing a fixture with large LED count.

20.6.2 Impact of Color Variation During Time ("Color Maintenance")

During operational life of an LED, color point can shift. Two possible scenarios exist:

- A consistent shift of all LEDs ("systematic error case").
- A random shift of all LEDs.

The first case cannot be overcome as it leads to inconsistencies, namely when a product with "new" LEDs is placed next to an old one. However, this shift can be ignored when comparing products made at the same time. With a random shift in color (second case), the effect can be compensated. The random shift is simply an SDCM value to add to the bin size, which will follow central limit theorem.

However, the requirement of 0.08SDCM, applied to color shift as seen on literature (<2 SDCM over 6,000 h) [25, 26] leads to an unrealistic requirements on fixture LED count to achieve this target ($2/\frac{3}{\sqrt{N}} = 0.08 \; => N = 625$ with 2 SDCM, 156 with 1 SDCM). This is clearly a limiting point to achieve extreme color consistency.

In both cases, a reliable specification, which would have to include color point stability, has to take into account a "real bin size" which is then close to *twice* the already proposed ANSI/16 (and +30 % for 1SDCM shift)

20.6.3 Impact of Flux Variation During Time ("Lumen Maintenance")

As seen previously, the influence of flux differences is limited on the color shift. The flux difference LED to LED has to be more than 2.5 % to pass above a 0.08 SDCM value. Lumen depreciation over lifetime applies to the *entire set of LEDs*, so no averaging is possible. Taking a time of 50,000 h to reach 70 % of the flux, one can define a "flux depreciation per hour". To estimate the color consistency drift due to this flux change, one can apply the result from Fig. 20.16. This shows that after 4,200 h, the color consistency goes above 0.08 SDCM and thus limits the interest of replacing LEDs within a fixture. For products made with LEDs having similar operating age, flux imbalance has no reason to have consequences. If the time to reach 70 % of the flux ("L70" in literature) is longer, one can estimate the "acceptable time to replace an LED within the fixture". If the flux F is written as $F = 1 + \alpha t$ (linear fit -or exponential if α is a small number-), the specification lifetime will be $t0 = -0.025/\alpha$. If an hypothetical LED reaches values below $\alpha = 1e - 6$, the lifetime of the spec becomes greater than $t0 = 25{,}000$ h

20.6.4 Estimation of Relative Weights of Sources of Deviation

For this paragraph is considered an hypothetical luminiare made of 32 LEDs, with LEDs binned as ANSI/4 and ANSI/16 bins, from three bins of flux, Those LEDs also shift in color point of 3 SDCM over their lifetime. One can evaluate the color distribution of those luminaries, and evaluate the relative sources of color shift. Considering normal distributions of color shifts due to binning size, flux variation, and lumen maintenance variations, one can calculate the overall color distribution and the relative weight of each source of deviation following the reasoning of previous sections. One can use "99.7 % of the population" as a rough estimate of 3. σ of a distribution. The end result σ is calculated using a combination of normal distributions from the different sources of variability, and use three times the

combined standard deviation as an estimation of 99.7 % of the fixture distribution. The sum of two normal distributions of mean μ and average σ are as follow:

$$\mu_{X+Y} = \mu_X + \mu_Y$$

$$\sigma_{X+Y}{}^2 = \sigma^2{}_X + \sigma^2{}_Y$$

So the distribution in SDCM, due to the three main causes of variability, is:

$$\sigma^2 = \sigma^2_{\text{bin}} + \sigma^2_{\text{flux}} + \sigma^2_{\text{color}(t)}$$

Comparing the distributions seen above and taking the numbers estimated in previous paragraph,

$$\sigma^2 = \frac{\left(\left(\frac{7}{3}\right)^2 + \left(\frac{0.4}{3}\right)^2 + \left(\frac{2}{3}\right)^2\right)}{N}$$

That gives an estimated best result, for a 32 LED product, with nowadays LED technology, of 3. $\sigma = 1.34/\sqrt{N}$ SDCM. For ANSI/16, the result is $\frac{0.88}{\sqrt{N}}$ and for ANSI/64, $0.62/\sqrt{N}$. This result proves a clear gain to go from ANSI/4 to ANSI/16, but the benefit is limited going to ANSI/64. Those results also prove that 1 SDCM or better is achievable now, but the 0.08 SDCM to achieve a "99.7 % of users not seeing any color differences in perfect conditions", cannot be reached at this stage of the technology.

To evaluate the limiting factors impacting color consistencies, we can plot the relative weights calculated above for nowadays technologies, for ANSI/4, ANSI/16 and ANSI/64 in Fig. 20.18.

In all cases the flux distributions or flux decrease over time do not impact optimized products with sufficient LED count. We can see that to achieve extreme color consistencies, the first point is to reach ANSI/16 at least. Then, the color shift over time becomes the limiting point.

20.7 Conclusion

In this chapter we propose a way to embrace the LED variability to enable reliable color consistency specification. We described how to optimize the binning usage, and how to evaluate the distributions of color of optimized products. We list the core challenges for color consistency and provide tentative guidelines to achieve, at a fixture level, a perfect consistency. Lighting system architects and fixture manufacturers can reach more reliable specifications by adopting those methods.

In conclusion, reliability of the color specifications is a challenge that could be solved with further developments of color selection at LED manufacturer side, and mostly by improving the color stability over lifetime.

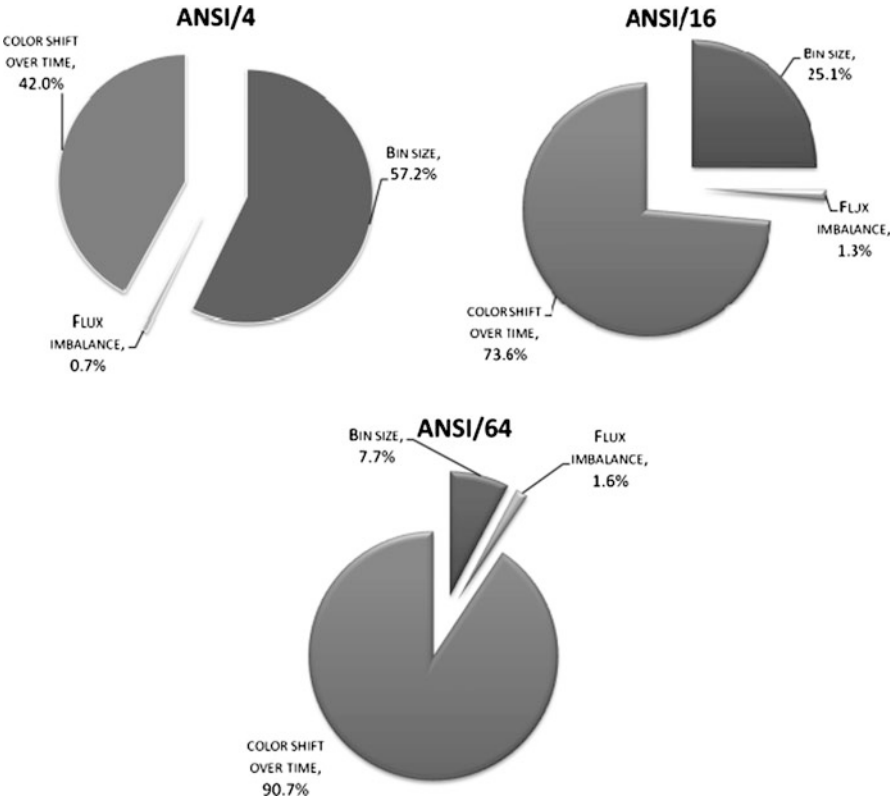


Fig. 20.18 Relative impact on flux imbalance, color shift over time and binning subdivision on color consistency, for a 32 LED product

The LED Luminiare industry needs standardization and improvements from LED manufacturers to capitalize on the results of color consistency. This was one of the key "early issues" with Solid State Lighting technology, and still, in the general mind, a negative comparison point with technologies like halogen lamps. Applying those methods, LED technology color consistency gets a leading edge against halogen or CFL. Furthermore, with proper acceptance, technical understanding, and communication, those LED-only techniques provide a guaranteed color point, for a guaranteed lifetime, enabling mass adoption.

References

1. Guild J (1931) The colorimetric properties of the spectrum. Phil Trans Roy Soc (London) 230:149
2. Maxwell JC (1860) On the theory of compound colors, and the relations of the colors of the colors of the spectrum. Phil Trans Roy Soc (London) 150:57–84

3. CIE (1971) Colorimetry (official recommendations of the international commission on illumination), CIE publ. no. 15 (E-1.3.1), Bureau Central de la CIE, Paris
4. CIE (1972) Special metametrism index: change in illuminant, supplement no. 1 of CIE publ. no.15 (E-1.3.1) 1971, Bureau Central de la CIE, Paris
5. CIE (1978) Recommendation of uniform color spaces, color-difference equations, psychometrics color terms, supplement no. 2 of CIE publ. No. 15 (E-1.3.1) 1971, Bureau Central de la CIE, Paris
6. CIE (1987) International lighting vocabulary, 4th ed. CIE publ. no. 17.4, IEC (Publ. 50 (845))
7. Grassman H (1853) Zur Theorie der Farbenmischung, Poggendorf. Ann Phys 89:69
8. Judd DB, Wyszecki G (1975) Color in business, science, and industry, 3rd edn. Wiley, New York
9. Krantz DH (1975) Color measurement and color theory: I. Representation theorem for Grassman structures. J Math Psychol 12:283–303
10. Wright WD (1928–1929) A trichromatic colorimeter with spectral stimuli. Trans Opt Soc 29: 225
11. Wyszecki G, Stiles WS (1982) Color science: concepts and methods, quantitative data and formulae, 2nd edn. Wiley, New York
12. Judd DB (1935) A maxwell triangle yielding uniform chromaticity scales. JOSA 25(1):24–35
13. McAdam DL (1937) Projective transformations of I.C.I. color specifications. JOSA 27 (8):294–297
14. CIE (1960) Brussels session of the international commission on illumination. JOSA 50 (1):89–90
15. CIE (1986) Colorimetry, 2nd edn. CIE publ. no. 15.2 (E-1.3.1), Bureau Central CIE, Vienna
16. CIE (1975) Colors of light signals (official recommendations of the CIE), Publ. CIE no. 2.2 (TC-1.6) Bureau Central de la CIE, Paris
17. Judd DB (1936) Estimation of chromaticity differences and nearest color temperature on the standard 1931 ICI colorimetric coordinate system. J Opt Soc Am 26:421
18. Kelly KL (1963) Lines of constant correlated color temperature based on MacAdam's (u, v) uniform chromaticity transformation of the CIE diagram. J Opt Soc Am 53:999
19. MacAdam DL (1942) Visual sensitivities to color differences in daylight. J Opt Soc Am 32:247
20. ANSI (2008) Specification of the chromaticity of solid state lighting products, ANSI_NEMA_ANSLG C78[1].377
21. Energy star program requirements for solid state lighting luminaires. http://www.energystar.gov/ia/partners/prod_development/new_specs/downloads/SSL_FinalCriteria.pdf
22. http://www.philipslumileds.com/uploads/news/id137/PR149.pdf
23. Murty KG (1983) Linear programming. Wiley, New York
24. Spiegel MR (1992) Theory and problems of probability and statistics. McGraw-Hill, New York, pp 112–113
25. http://www.cree.com/products/pdf/XLamp_XP_Reliability.pdf
26. http://www.philipslumileds.com/uploads/294/DR04-pdf
27. NIST/SEMATECH e-Handbook of statistical methods. http://www.itl.nist.gov/div898/handbook/

Chapter 21
Reliability Considerations for Advanced and Integrated LED Systems

X.J. Fan

Abstract This chapter presents an overview of advanced packaging and integration of solid state lighting (SSL) systems. A full realization of wafer level SSL system integration requires wafer level phosphor coating, wafer level LED chip encapsulation, wafer level optics manufacturing, the application of through silicon vias (TSV) between LED and silicon/ceramics/polymer wafers, the application of wafer-to-wafer or wafer-to-chip bonding and stacking, and the adoption of wafer level bumping technologies. Advances in reconfiguration (or reconstitution) of LED/silicon wafers are described in this chapter. Different technologies in TSV formation and various wafer-to-wafer or wafer-to-chip bonding technologies are illustrated. The finite element modeling of TSV process, essentially a chemical etching and subsequent passivation process, is discussed. A variety of wafer level bumping technologies is introduced, such as ball on I/O (BON), ball on polymer (BOP), redistribution dielectric layer (RDL) process, and copper post bumping process. The reliability improvement among different bumping technologies and the implications in SSL systems are presented. Newly developed polymer-core interconnect technology and nanocolumn interconnect are discussed.

21.1 Introduction

Light emitting diode (LED) is a solid-state lighting (SSL) source that converts electricity directly into light. SSL provides high energy efficiency in lower power consumption, longer life (up to 50,000 h), and higher performance, such as ultrahigh-speed response time, a wider range of controllable color temperatures, and a wider operating temperature range. Because of this, general lighting and

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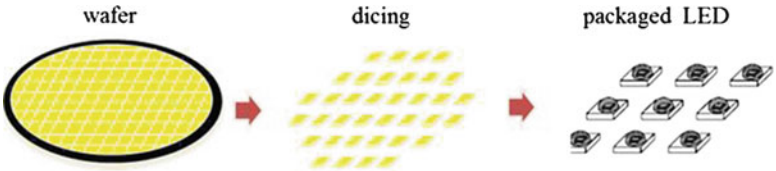


Fig. 21.1 Component level LED packaging process illustration

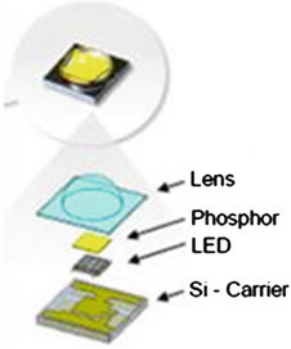


Fig. 21.2 Key assembly steps in LED chip packaging

illumination is now going through a radical transformation from traditional incandescent bulbs and fluorescent lamps to SSL based illumination systems [1].

LED packaging is critical to achieve desired performance, lifetime and reliability. The package should be optimized to achieve system performance, cost, reducation size and manufacturability, including thermal mechanical stability, low thermal resistance and high reliability. Solid state lighting (SSL) systems usually compromise of the following subsystems: LED lighting sources (packaged LED or LED module/emitter), thermal management designs (e.g., fans and heat sinks), driver and control electronics, and optics. Most of LEDs today are packaged on an individual component basis. Figure 21.1 is a schematic illustration of current LED chip packaging process. LED wafer is diced into individual LED chips first before packaging. The packaging process includes silicon submount (by flip chip or wire bond), phosphor coating, epoxy encapsulation, lens attachment, heat sink and outer package assembly, as illustrated in Fig. 21.2. Such a component level packaging process has a relatively low throughput. Consequently it is more difficult to implement automation for large scale mass production, which is a critical element for low cost manufacturing. Therefore, a more efficient packaging process at wafer level in batch process is in demand in the LED industry.

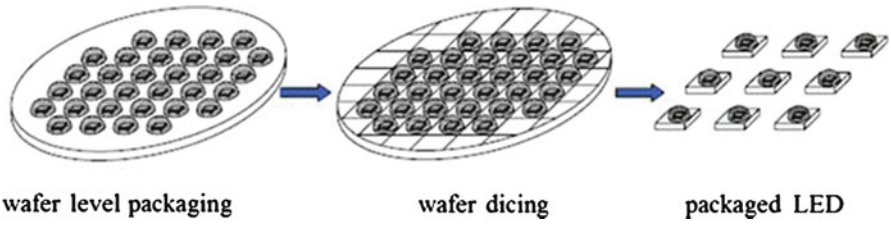


Fig. 21.3 Conceptual illustration of wafer level LED packaging and integration

The packaged LED module (or emitter) must work with other components, such as application specific integrated circuits (ASIC), LED driver, sensor, radio frequency (RF) circuit, power controller, processor, or memory, and additional heat dissipation component etc. The construction of SSL system is somewhat similar to a microelectronics system. Therefore, there is a potential breakthrough and technology development for 3D system integration for SSL systems. By performing batch wafer level packaging, integration and testing, the SSL system costs can be brought down significantly in the future.

Tsou et al. [2] attempted to demonstrate a silicon-based packaging platform for wafer level LED packaging using silicon bulk micromachining technology. The process uses a wafer with embedded solder interconnections as the substrates for LED arrays. In this process, functional LED arrays can be fabricated in a batch process, hence the cost is reduced. However, this process does not include a solution to the encapsulation process, and a functional LED package is not yet fabricated. Lim et al. [3] developed a wafer level encapsulation process for LED packages. The most critical issue for this process is the high matching requirement between the whole piece of encapsulation array and the wafer. It has a small tolerance to tilting and deformation of the mold, the encapsulation array, and the wafer. Zhang and Lee developed a deep reactive ion etching (DRIE) trenches based LED wafer level packaging process [4, 5]. The encapsulation process takes advantage of DRIE trenches that are integrated with the silicon substrate to define the encapsulation region, and can adjust the geometry of the encapsulation via controlling the volume of the epoxy. Both the fabrication of the LED substrates and the encapsulation for LEDs are completed at wafer level. LED packages can be directly obtained after wafer singulation. For wafer level LED chip packaging, the corresponding equipment is also made available, for example, for wafer level phosphor coating and wafer level optics process [6].

The rapid advancement in integrated circuit (IC) wafer level packaging (WLP) may be readily applied to a SSL system. The recent developments in through silicon via (TSV) and wafer-level bonding and stacking technologies make it possible for a full 3D integration of LED system at wafer level. Figure 21.3 is a schematic illustration of wafer level SSL system packaging and integration process. The final SSL system can be directly obtained after wafer singulation. Lau et al. [7] demonstrated a conceptual 3D LED and IC wafer level packaging integration. Figure 21.4 is a schematic conceptual illustration of an integrated SSL system [7].

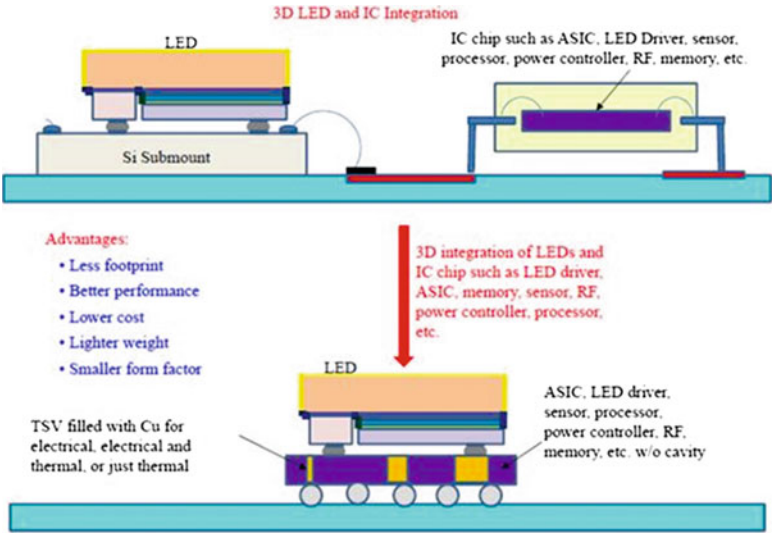


Fig. 21.4 3D LED and IC (e.g., LED driver, ASIC, memory, processor, sensor, power controller, and RF) integration [7]

The passive Si submount in a LED module is replaced by an IC chip such as the ASIC, LED driver, processor, power controller, sensor, RF, etc., i.e., integrating the LEDs and the IC chip together in a 3D manner. Their electrical feed-through and some of the thermal paths can be effectively achieved by the through silicon vias (TSV) filled with copper w/o redistribution layers (RDL) on the IC chip. The integrated device is assembled using wafer level bumping technology. More details of the integration are shown in Fig. 21.5. The active IC chip can be used to support the multi-LEDs for many functions, e.g., dimming and lighting control, step-up and step-down topologies, power conversion, electrical feed-through, and thermal management.

Wafer level bumping plays an important role in final wafer level production. A variety of WLP bumping technologies have been developed [8–10], such as ball on nitride (BON) [11], ball on polymer (BOP) [11–13], and copper post WLP [14]. To meet the demand in increasing I/O count, fan-out WLP technologies have been developed, such as embedded wafer-level ball grid array (eWLB) technology [15], and redistributed chip packaging (RCP) technology [16]. It is well understood that solder joint thermo-mechanical reliability performance become a critical concern of WLPs with larger die packages [17]. The ability of solder joint to survive the required thermal cycle testing has limited the WLPs to the products having relatively small die sizes and a small number of I/O. The intrinsic difference in the coefficient of thermal expansion (CTE) between silicon (~2.6 ppm/°C) and PCB (~17 ppm/°C) determines that the solder ball thermal cycling fatigue performance is limited by die-size. New bump structures have demonstrated the significant enhancement and improvement on solder joint reliability [18–20].

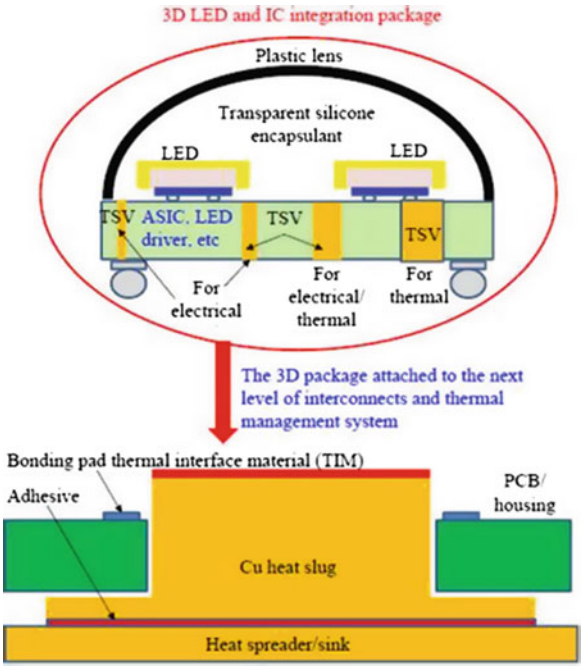


Fig. 21.5 3D LED and IC integration package (without a cavity) on an ordinary thermal management system [7]

It can be seen that wafer level packaging and integration of a SSL system consists of the following areas

- Wafer level LED chip packaging
  - Wafer level optics
  - Wafer level encapsulation
  - Wafer level phosphor coating
- Wafer level IC packaging and integration
  - Wafer level IC packaging
  - 3D integration with TSV and wafer bonding/stacking

This chapter is organized as follows. In the next section, wafer level LED chip packaging is described. Wafer level LED chip packaging includes wafer level phosphor coating, wafer level encapsulation and wafer level optics. In Sect. 21.3, 3D integration with integrated circuit (IC) using TSV is illustrated. A variety of wafer bonding and stacking technologies is introduced. TSV process simulation using finite element modeling is presented. In Sect. 21.4, wafer level bumping technologies are demonstrated, with an emphasis on thermo-mechanical reliability considerations. New interconnect technologies such as hollow solder balls and polymer-core balls are also presented concerning reliability enhancement. Finally a summary of the chapter is given.

21.2 Wafer Level LED Chip Packaging

Wafer level LED chip packaging consists of wafer level phosphor coating, wafer level encapsulation, wafer level optics, and LED wafer reconfiguration. Figure 21.6 describes a wafer level encapsulation process, developed by Lim et al. [3]. As illustrated in Fig. 21.6, a high viscous photoresist is patterned on wafer and reflowed into dome-shaped islands. The Nickel plating process is then performed on wafer to form a mold. Subsequently, a UV curable polymer is dispensed onto the Ni mold and is cured to form a whole piece of encapsulation array. The encapsulation array can then be attached onto a wafer on which LED arrays are mounted. In this manner a wafer level LED packaging process is realized. This wafer level encapsulation process is actually still a molding process. The most critical issue for this process is the high matching requirement between the whole piece of encapsulation array and the wafer. It has a small tolerance to tilting and deformation of the mold, the encapsulation array, and the wafer.

Zhang and Lee [4] developed a DRIE trenches based LED wafer level packaging process. A 4-in. p-type wafer serves as the substrate for LED arrays. The fabrication of the wafer substrate is made by microfabrication and wafer level plating process. The fabrication process was performed as follows.

(a) The wafer was first deposited with a 3 μm silicon low-temperature-oxide (LTO) layer by the CVD Furnace B4. The LTO layer served as the mask for patterning in the subsequent deep-reaction-ion-etching (DRIE) process due to its high resistance to plasma etching compared with silicon (the etching rate by DRIE is SiO2:Si = 1:50). Subsequently, 50 μm deep double-line trenches as illustrated in Fig. 21.7 were fabricated by the DRIE process (Fig. 21.7a). A positive thin photoresist (PR) PR204 was used for photolithography in this step due to its high resolution (1 μm).

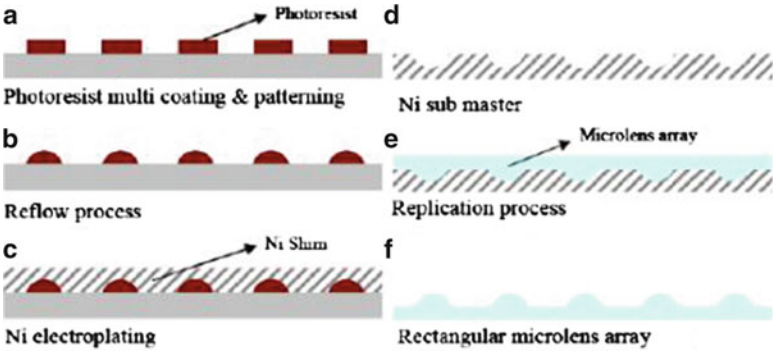


Fig. 21.6 Fabrication of the microlens array for wafer level LED packaging [3]

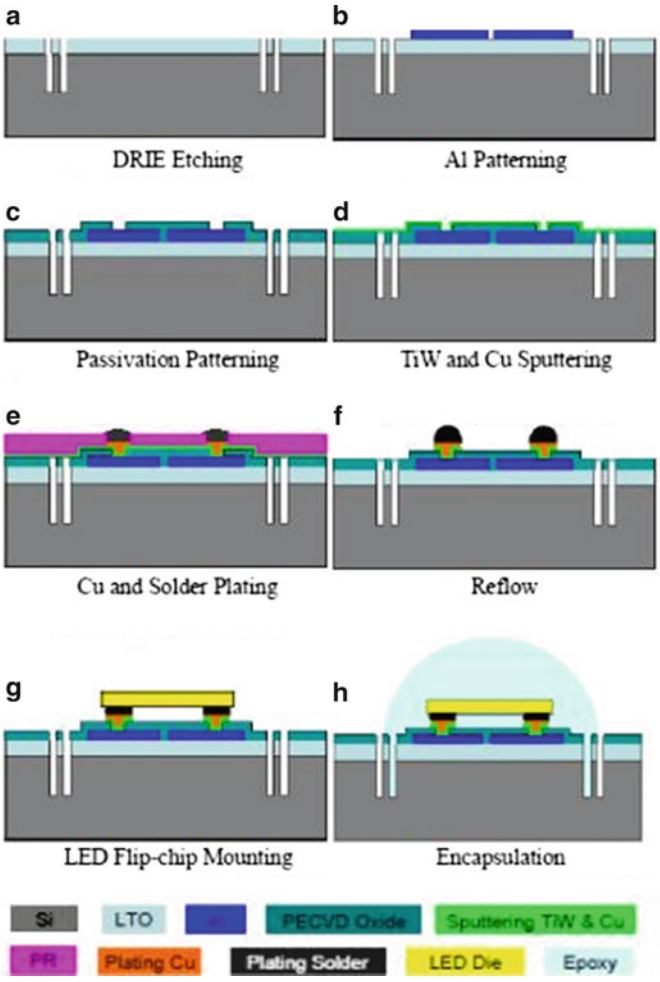


Fig. 21.7 Wafer level LED packaging process [6]

(b) After the trenches were etched, a pure Al layer with a thickness of 2.5 μm was sputtered by Varian 3180 onto wafer and then patterned by dry etching using Cl_2 and BCl_3 gas by Metal Etcher AME 8130 (Fig. 21.7b). HPR207 with a standard thickness of 3–4 μm was applied for Al etching.

(c) Subsequently, a SiO_2 layer, which served as the passivation layer for the LED mounting pattern, was deposited onto the wafer using Plasma-enhanced chemical vapor deposition (PECVD), it was then patterned by dry etching by Oxide Etcher AME 8110 (Fig. 21.7c).

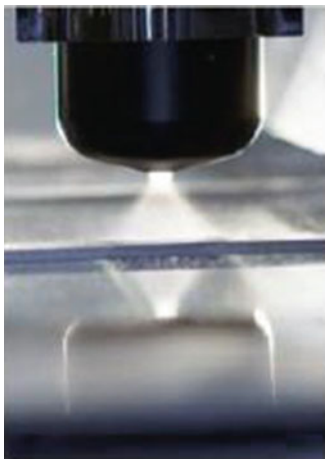


Fig. 21.8 Spray coating of diluted phosphor solutions on processed LED wafers

(d) 500 Å thick TiW and 5,000 Å thick Cu seed layer for the subsequent electroplating process were then sputtered onto the whole wafer (Fig. 21.7d) by ARC-12 M.
(e) A 31 μm thick photoresist P4903 was coated on wafer and patterned, and the 6 μm thick Cu and 30 μm thick SnPb solder layers were electroplated (Fig. 21.7e).
(f) After plating, the photoresist was stripped by acetone, the sputtering Cu layer was stripped by copper etchant, and the TiW layer was stripped by RCA SCl solution (a solution of $NH_4OH:H_2O_2:H_2O = 1:1:5$). The whole wafer then went through reflow to form solder bumps (Fig. 21.7f).
(g) LED dies were flip-chip mounted onto the substrates by a reflow oven (Fig. 21.7g).
(h) The glop-top dispensing encapsulation process was performed to encapsulate the LED dies (Fig. 21.7h) and complete the whole LED packaging process.

Figure 21.8 shows the wafer level phosphor coating by spray coating of diluted phosphor solutions on processed LED wafers [6]. The advantages of such a process are: (1) high coating uniformity of topside and sidewalls of the dies; (2) low phosphor consumption; (3) easy solution-based tuning of the color temperature and color rendering index; (4) fast batch processing on wafer-level; (5) reduced binning; and (6) multiple remote phosphor layers possible.

To perform wafer level optics and wafer level phosphor coating, the LED wafer needs to be reconfigured. Figure 21.9 shows a typical process of wafer reconstitution (or reconfiguration) [8]. The "good tested" LED dies are placed face-down onto a carrier with an adhesive tape. The distance (pitch) between the dies on the carrier defines the fan-out area around the chips and is freely selectable. The carrier with the adhesive tape holds the dies in position and protects the active side of the dice during molding. A mold compound is used to combine the placed LED dies to wafer format in compression mold technique.

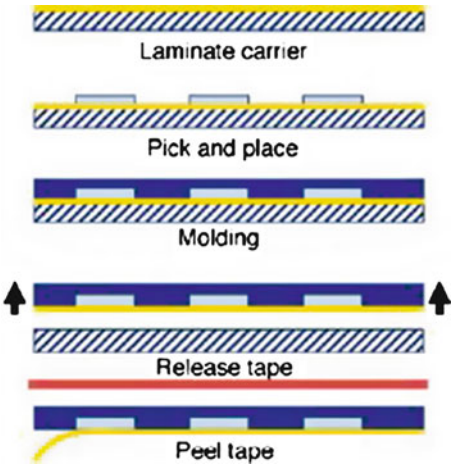


Fig. 21.9 A typical process of wafer reconstitution (or reconfiguration) of LED dies

After this, the reconstituted wafer is released from the carrier system, which can be reused afterwards.

21.3 TSV Process and 3D LED and IC Packaging Integration

Many new developments are currently underway to incorporate 3-D packaging technology with WLP solutions into SSL systems for a full integration realization. TSV technology has been one of key elements in 3D integration. The main advantage of the TSV technology with WLP is to reduce the size of the device module. Three-dimensional integrated circuits (3D IC) have been generally acknowledged as the next generation semiconductor technology with the advantages of small form factor, high-performance, low power consumption, and high density integration. TSV and stacked bonding are the core technologies to perform vertical interconnect for 3D integration. For the fabrication approach, there are three stacking schemes in 3D integration: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-to-wafer technology can be applied for homogeneous integration of high yielding devices. Wafer-to-wafer bonding maximizes the throughput, simplifies the process flow, and minimizes cost. The drawback for this wafer-to-wafer method is the number of known-good-die (KGD) combinations in the stacked wafers will not be maximized when the device wafer yields are not high enough or not stable. In this case, chip-to-chip or chip-to-wafer will be adopted to ensure vertical integration with only good dies. Considering mass production in future, the chip-to-wafer and wafer-to-wafer technologies have gradually become the mainstream for 3D integration.

Wafer bonding and stacking technologies can be further differentiated by the method used to create TSVs: either via-first or via-last. The common definition for via-first and via-last is based on TSVs formed before and after BEOL process. TSV

fabrication after the wafers are bonded, using a "drill and fill" sequence, is definitely via-last approach. Whereas via-first and prebonding via-last approaches, building TSVs on each wafer prior to the bonding process are generally more efficient and cost-effective. The leading wafer-level bonding techniques used in 3D integration include adhesive bonding (polymer bonding), metal diffusion bonding, eutectic bonding, and silicon direct bonding [21].

Lau et al. [7] demonstrated an example of the manufacturing processes of two 3D LED and IC integration, shown in Figs. 21.3 and 21.4. The fabrication of the reflector cup (cavity) of the active silicon IC wafer is by wet anisotropic etched with the etchants such as potassium hydroxide solution (KOH), ethylenediamine pyrocatechol solution (EDP), and tetramethylammonium hydroxide (TMAH). Depending on the dimensions of the mask opening, a V-groove or trapezoidal basin can be formed in the active IC wafer. KOH is the most commonly used etchant. It is much less dangerous (toxic) than others, easy to handle, readily available, and etches fast. The greatest disadvantages are that KOH is IC incompatible and that the selectivity to plasma-enhanced chemical vapor deposition oxide is rather poor. TMAH is nontoxic and IC compatible, but fewer studies exist on this system. EDP is not easy to handle. It is toxic, and the solution degrades if it comes in contact with oxygen. Thus, EDP is mainly used in research laboratories and is not used in mainstream semiconductor fabrications.

Deep reactive ion etching (DRIE) is one of the most important techniques in making TSVs [22–30]. The facilities for making TSVs and the fabrication processes are very expensive. The simulation and modeling of TSV processes provides an alternative because it not only can provide better understanding and modeling of the processes, but more importantly facilitates rapid process optimization at reasonable cost. In recent years, extensive researches were conducted to develop numerical modeling tools for the TSV processes. Oldham et al. [31] extended the general process simulator SAMPLE to the simulation of plasma etching and metal deposition. McVittie et al. [32] proposed the surface profile simulator SPEEDIE for dry etching and LPCVD which focused on the role of near surface particle transport and surface kinetics in controlling the profile shapes. Gerodolle and Pelletier [33] presented a model for plasma etching of silicon by SF6 in which the surface diffusion of the reactive species was emphasized. Harafuji and Misaka [34] developed the etching topography simulator MODERN in which a surface reaction model was proposed and the reaction rate was determined by considering the interactions between the incoming ion/radical fluxes and a time-dependent adsorbed particle layer on the surface. Zhou et al. [35] presented the 2D profile simulator DROPIE for the simulation of the etching/polymerization alteration in the Bosch process. Empirical models for both etching and deposition processes were developed and the simulator demonstrated the ability to simulate the etching of different material types based on a string-cell hybrid method. Tan et al. [36] presented the extension of the Bosch process simulator DROPIE to the modeling and simulation of the lag effect in the DRIE process. Miao et al. [37] further extended the simulator to the simulation of TSVs with tapered sectional profiles.

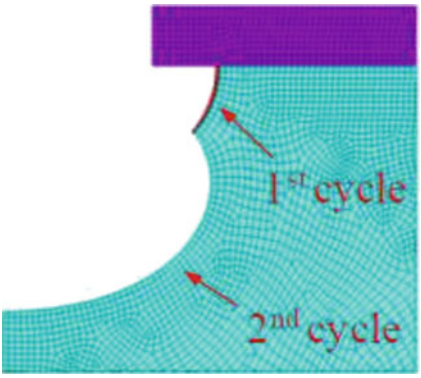


Fig. 21.10 Finite element simulation results of two-cycle etching process [38]

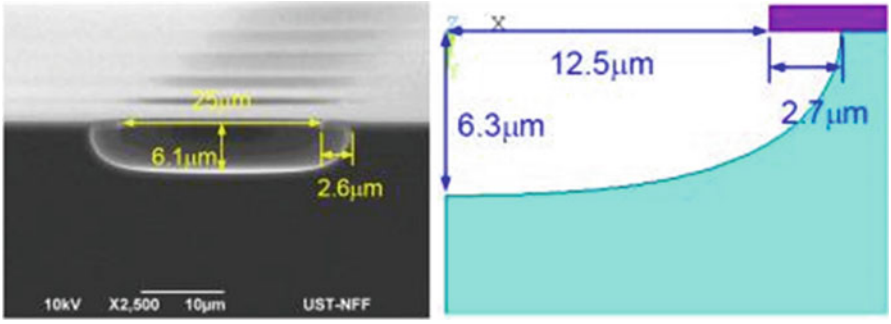


Fig. 21.11 Comparison between experimental results and simulation for an etching process [38]

The governing equation of the etching process can be expressed as

$$\frac{\partial C}{\partial t} = D\left(\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} + \frac{\partial^2 C}{\partial z^2}\right) \tag{21.1}$$

where C is concentration of etching gas (g/μm^3), t is time (s) and D is diffusion coefficient (μm^2/s). According to the diffusion law in (21.1), the etching gas concentration inside the silicon after a certain time can be calculated by performing finite element analysis. It may be assumed that the portion of silicon with the etching gas concentration above a certain critical value is etched away by the applied gas. The TSV formation is realized by a continuous process of etching/passivation alternations. Figure 21.10 demonstrates the results to simulate the etching/passivation alternations with the finite element method for a two-cycle process [38]. The experimental results and the corresponding simulation results are shown in Fig. 21.11. The simulation results agree well with the experimental observations.

21.4 Wafer Bumping and Reliability Considerations

Wafer bumping is one of the most important assembly steps in wafer level packaging and integration. Since there exists an intrinsic difference in the coefficient of thermal expansion (CTE) between LED/silicon wafers (~2.6 ppm/°C) and PCB (~17 ppm/°C), solder ball reliability under thermal cycling loading is apparently limited by die-size [8–10]. The larger the die size is, the greater thermal stresses are developed at the outmost solder balls due to the effect of distance from neutral point (DNP). To improve solder ball reliability performance, several bumping technologies have been developed, such as ball on nitride (BON) [11], ball on polymer (BOP) [11–13], and copper post WLP [14]. Although ball on nitride (or ball on I/O) is seldom used in today's applications, it will be introduced first in the following as a benchmark to compare with other WLP configurations.

Figure 21.12 shows a redistributed bump on nitride (BON) bump structure, consisting of solder bump and under bump metallurgy (UBM) seated on the thin inorganic passivation [8, 11]. In the case of WLPs with a BON structure (or ball on I/O), the added redistribution layer and the passivation layer do not provide additional benefit to solder joint reliability performance since the solder ball is directly connected to the silicon base. In this case, solder balls become the weakest link under thermal cycling loading conditions. It has been reported that this WLP structure is limited to 6×6 array size (or less) at 0.5 mm pitch (~3mm×3mm die-size) to meet the thermal cycling reliability requirement [11]. The predominate failure mode has been fatigue crack propagation in bulk solder near solder ball/die interface, as shown in Fig. 21.13 [8].



Fig. 21.12 Bump on nitride (BON) stack-up structure

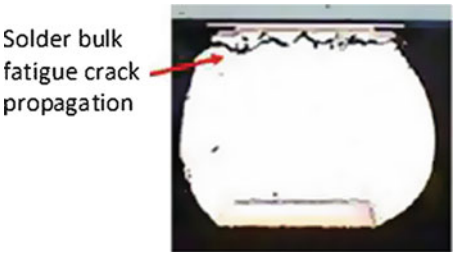


Fig. 21.13 Typical solder bulk fatigue crack propagation in thermal cycling

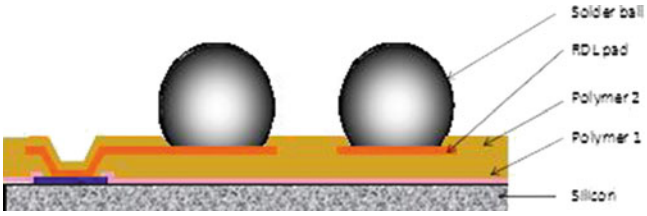


Fig. 21.14 Bump on polymer (BOP) without UBM stack-up structure

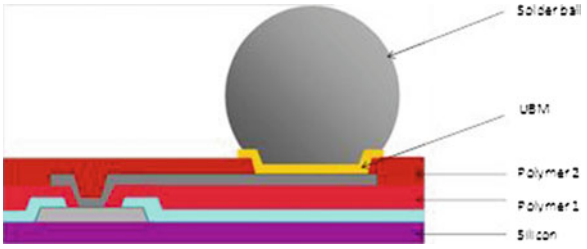


Fig. 21.15 Bump on polymer (BOP) with UBM stack-up structure

Figure 21.14 shows a schematic diagram of ball on polymer (BOP) WLP structure without UBM layer [9]. The redistribution copper traces allow a process without UBM since the diffusion barrier requirements of the UBM are no longer needed. In the case of the ball on polymer, the bump rests on the polymer film, and thus any stress applied to the solder ball will directly propagate to the underlying polymer film. The common materials for polymer films are polyimide (PI) or benzocyclobutene (BCB), both of which are extremely complaint. Polymer films serve two purposes, passivation for the redistribution layer (RDL) and stress buffer. Because polymer films are very compliant, stresses will be partially 'absorbed' by the films during thermal cycling. As consequences, potential failures might occur at film/copper trace build-up stacks other than in solder balls.

Figure 21.15 is a schematic of WLP structure for ball on polymer with UBM layer. The UBM now functions only as an adhesion layer that facilitates the bump electroplating process. In this case solder balls also sit on a polymer film layer to avoid a direct connection with the silicon base. Similar to the WLP without UBM, although there may be a concern on failures at film/copper trace stacks, it has been demonstrated that with BOP WLP structures with or without UBM layer (Figs. 21.4 and 21.5), the array size can be extended to 12×12 with 0.5 mm pitch meeting reliability requirement. In other word, the die size is now extended to 6mm×6mm and the ball count to 144 from the benchmark design of BON WLP of 3mm×3mm and the ball count to 36 [8–10].

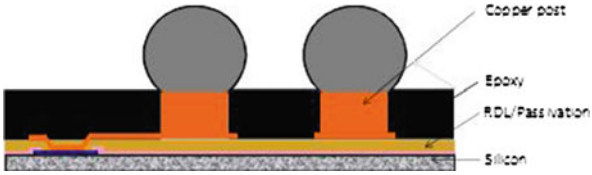


Fig. 21.16 Copper post stack-up structure

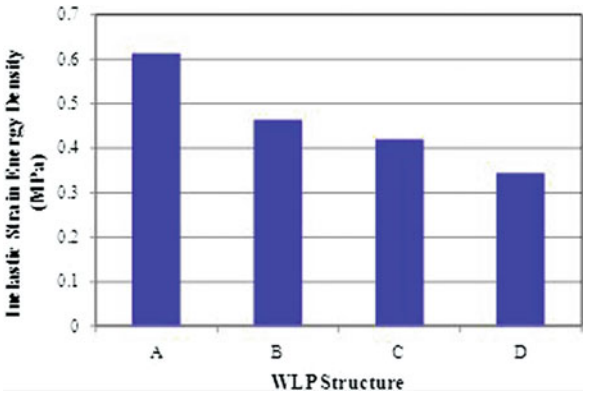


Fig. 21.17 Inelastic strain energy density for different bump structures: (**a**) BON; (**b**) BOP without UBM; (**c**) BOP with UBM; and (**d**) Copper post

Figure 21.16 shows a schematic of a copper post WLP structure. Thick copper pillars (~70 μm) are electroplated, followed by an epoxy encapsulation. In this case, solder balls rest on the copper post. The standard process uses 100 μm thick photoresist to form ~70 μm copper pad and ~35 μm tin plating. The copper post WLP can also incorporate with redistribution layer, as shown in Fig. 21.6. In the case of a copper post WLP even without redistribution layer, it has been demonstrated that the copper post structure has superior thermo-mechanical reliability performance. The array size can be extended to 12×12 with 0.5 mm pitch [14].

There are also other bump structures, such as double bump WLPs and compliant layer process [39], which can be applied for large array applications. The underlying mechanism to improve thermal cycling reliability of fan-in WLPs is to make the WLP structures more flexible so that the stresses transmitted to solder balls can be reduced [8–10].

To understand the mechanism of reliability for various bump structures, first, the attention is confined to solder ball fatigue failures under thermal cycling conditions. Finite element modeling is performed to investigate the accumulated inelastic strain energy density at solder ball/chip region subjected to −40 °C and 125 °C thermal cycling [10]. Figure 21.17 plots the per-cycle inelastic strain energy densities for the four fan-in WLP structures, for a 12×12 array package with 0.5 mm pitch. It can be seen that, compared to the ball on nitride structure, all other three structures: BOP without UBM, BOP with UBM, and copper post WLP, show more than 30%

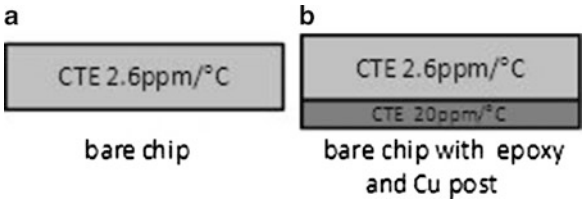


Fig. 21.18 Effective CTE increase of the "molded die" in copper post WLP

reduction in terms of the accumulated inelastic strain energy density per cycle. This means that, with the incorporation of a dielectric polymer film or an encapsulated copper post layer embedded in an epoxy, between solder balls and chip, the stresses in solder joints can be reduced significantly compared to a "rigid" ball connection as in a BON configuration.

For ball on polymer structures, the extreme compliance of the polymer film is attributed to be the reason for thermal-mechanical performance improvement in solder joints. The Young's modulus of polyimide film is 1.2 GPa, which is one order lower than the modulus of solder alloy (50 GPa for SAC305). The polymer film creates a "cushion" effect to reduce the stresses transmitted to solder joints. Studies have shown that the coefficient of thermal expansion (CTE) of the polymer film has insignificant effect on solder joint stresses provided that the polymer film modulus is extremely low.

On the other hand, for copper post WLP structure, the beneficial effect comes from the larger CTE of copper post and epoxy, which are typically 17 ppm/°C and 20 ppm/°C, respectively. The combined silicon chip and epoxy/copper post stack-up can be thought of as a 'molded' die with an effective CTE (in Fig. 21.18), which will be significantly greater than the CTE of the silicon die itself (2.6 ppm/°C). This results in a significant reduction of the stresses on solder joints. For a copper post WLP, the redistribution layer (RDL) may be incorporated if needed. However, It has been found that the effect of the polymer film in copper post WLP is not as effective as that in BOP structures [10]. This indicates that for the copper post WLP structure, the dominant effect to reduce the solder joint stresses is due to the larger CTE of copper and epoxy. The modulus of copper/epoxy and the appearance of the RDL (polymer film) are of the secondary effect in solder joint reliability improvement.

As shown in Fig. 21.13, the predominant failure mode for BON WLP structure is solder bulk fatigue crack propagation under thermal cycling. However, for BOP and copper post WLP structures, the copper interconnect reliability might be more important than solder joint reliability. For example, for a BOP WLP, studies have shown that the failures were predominantly on copper RDL trace cracks at the component side under drop and thermal cycling test [40–42]. The copper RDL failures were found along the 2 outer rows of I/O in a JEDEC board set up subjected to drop (Fig. 21.19). Figure. 21.20 shows an example of Cu/UBM delamination using dye & pry, which correlates to cross sectional pictures. This means that the failure mode in BOP WLPs may shift to wherever the weakest link of the system from solder ball regions. Nevertheless, the overall reliability

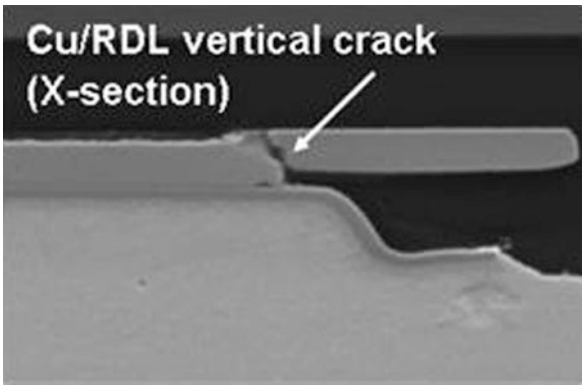


Fig. 21.19 Copper RDL trace failure under drop test

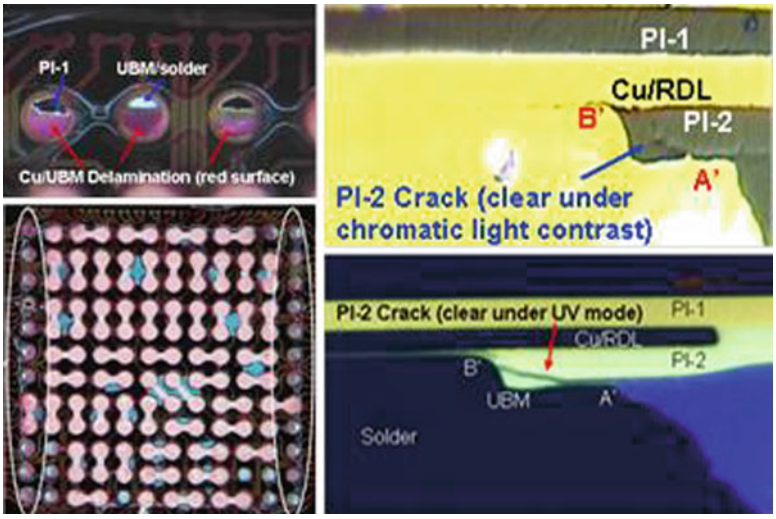


Fig. 21.20 Polymer film/UBM delamination

performance of BOP WLP structures has been greatly improved as compared to the BON WLP structure.

For wafer level packages, PCB is considered as "part" of the package since one cannot decouple the PCB from the WLP. PCB design plays an important role to assess the reliability of WLPs. With the conventional JEDEC board test set up and design, PCB trace cracks were often observed at locations near the outer row balls. All failures occurred in the PCB traces approach in the longitudinal direction under drop test (Fig. 21.21). This is because the traces in the longitudinal direction are suffered more mechanical stresses than other directions under drop. After the PCB

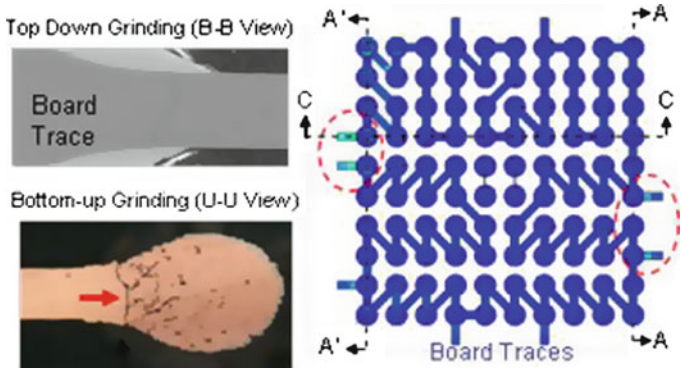


Fig. 21.21 PCB copper trace failures

trace direction was changed from a longitudinal routing to trace latitudinal routing, Cu trace failures in PCB can be eliminated [42]. It is also important to use low-CTE PCB board, which will improve the WLP reliability under thermal cycling significantly [10].

As opposed to a conventional fan-in WLP, fan-out WLPs start with the reconstitution or reconfiguration of single dies to an artificial molded wafer. The fan-out WLP has received increased attention because of the demand for thinner features and increasing I/O count devices. The reconfigured wafer or fan-out solution provides several advantages:

- Reduced package thickness,
- Fan-out capability (for the increased number of I/O),
- Improved electrical performance,
- Good thermal performance, and
- A substrate-less process.

Fan-out WLPs are structurally similar to the conventional ball grid array (BGA) packages, but eliminate expensive substrate processes. The critical solder balls in a fan-out WLP are located beneath silicon chip area, where the maximum CTE mismatch occurs between the silicon chip and PCB [8]. In Figure. 21.22, the per-cycle inelastic energy density is plotted against the location of solder balls in a diagonal direction for a 16×16 array fan-out WLP package, in which 6×6 array solder balls are under die area. Figure 21.22 shows that outermost ball right beneath silicon die has the maximum inelastic energy density among all balls. This is because the maximum local CTE mismatch is between silicon chip and the PCB. Thus the thermal stresses of solder balls beneath the chip are expected to be higher than the stresses on the outermost solder balls. The results show that fan-out WLP packages can extend the array size greatly while meeting thermo-mechanical reliability requirement.

To improve the compliance of WLP structures, solder balls may be constructed with nano-size column like or honeycomb like structures [43]. Some possible

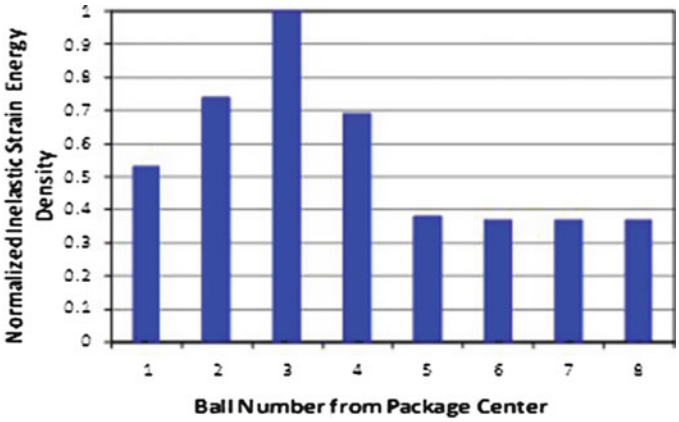


Fig. 21.22 Inelastic strain energy density for a fan-out package

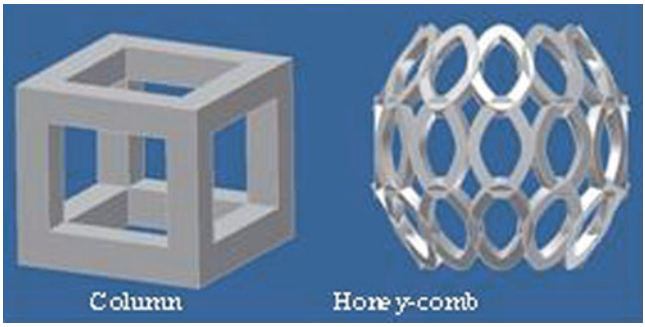


Fig. 21.23 Nanosize column-like or honeycomb-like interconnects to replace solder balls

configurations of "hollow solder balls" are illustrated in Fig. 21.23. These new ball structures would need new process to realize. The rapid advances in nanomaterial and nanomanufacturing developments would make it happen in the near future. The "ball" materials are not limited to "solder alloys".

Another option is the use of polymer-cored solder balls. A plastic core solder ball consists of a large polymer core coated by a copper layer and covered with eutectic and/or lead-free solder. The main advantages of such a system are higher reliability due to the relaxing of stress by the polymer core and a defined ball height after reflow [44, 45]. These balls could improve the solder ball reliability significantly due to the compliant feature of balls. Figure 21.24 is a schematic of horizontal view of polymer core ball. Figure 21.25 shows the photos of the plastic core solder balls. Table 21.1 shows the comparison of Young's modulus of polymer core material and SnPb. It can be seen that polymer core material has only one-tenth

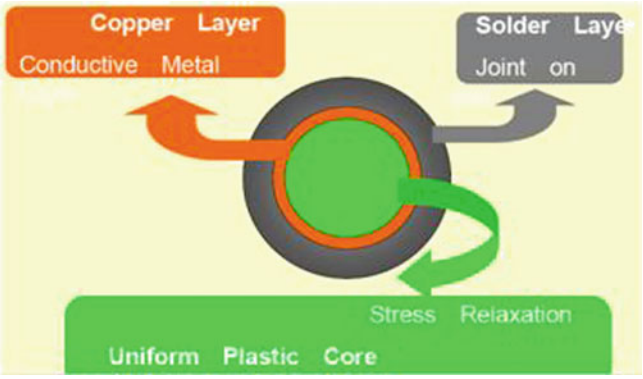


Fig. 21.24 Cross-sectional structure of polymer core ball

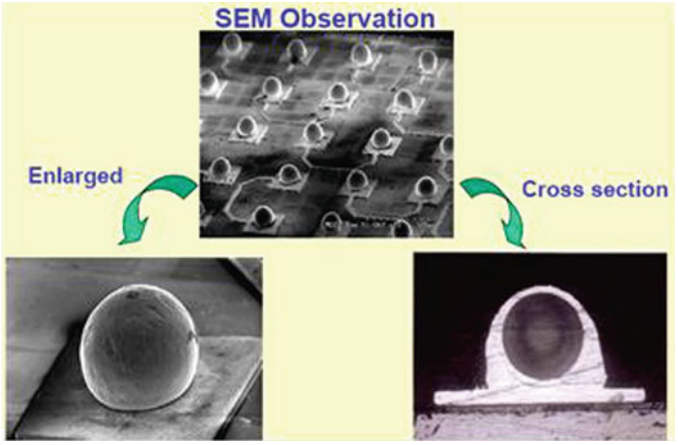


Fig. 21.25 Real images of plastic core solder balls on WLP

Table 21.1 Material properties for polymer core and SnPb solder

	Young's modulus (GPa)			CTE (ppm/°C)	
	20 °C	150 °C	Poisson's ratio	20 °C	150 °C
Plastic core	4.7		0.38	40.2	46.2
Solder (Sn/Pb)	40.2		0.4	24.7	
Substrate board	24.5	10.8	0.3	14	

of the modulus of SnPb, which will make the structure more flexible when subjected to temperature cycling.

A hollowed solder ball structure, which has the exact same geometry of a regular solder ball, is also proposed [43]. Table 21.2 shows the results of the inelastic strain energy density and von Mises stress for three ball structures, including regular

Table 21.2 Comparison of the inelastic strain energy density and von Mises stress for three cases

	Ball structures		
	Regular	Polymer-cored	Hollowed
Ball height (μm)	95	295	295
Max von Mises stress (MPa)	3.20	54.71	36.8
Max plastic work (MPa)	0.62	1.54	0.40
Avg. von Mises stress (MPa)	4.09	30.72	26.49
Avg. plastic work (MPa)	.23	0.20	0.07

solder ball, polymer-cored ball, and hollowed solder ball. The displayed results are for the outermost ball in the diagonal direction. Both the maximum and the averaged results are obtained. Table 21.2 clearly shows the significant reduction in both inelastic strain energy density and stress in solder balls when hollow structure is applied. Hollowed ball structures increase the compliance of the WLP during thermal cycling, and thus, less stresses are exerted on the solder ball interface with copper post. On the other hand, it is observed that for polymer-cored solder balls, complicated results are obtained. Maximum stress in polymer-cored solder balls does not show much reduction, especially after the averaged process is done. This indicates that for polymer-cored ball structures, stress distribution is more "uniform" than regular balls. Such results are also confirmed from inelastic strain energy density. The averaged inelastic strain energy density for polymer-cored balls is almost same with the regular balls when the same height is used. In actual applications, the ball height is much less for the regular balls, which will reduce the thermal cycling performance.

21.5 Summary

This chapter presents an overview of wafer level packaging and integration of solid state lighting (SSL) systems. A full realization of wafer level SSL system integration requires wafer level phosphor coating, wafer level LED chip encapsulation, wafer level optics manufacturing, the application of through silicon vias (TSV) between LED and silicon/ceramics/polymer wafers, the application of wafer-to-wafer or wafer-to-chip bonding and stacking, and the adoption of wafer level bumping technologies. Advances in reconfiguration (or reconstitution) of LED/silicon wafers are described. Different technologies in TSV formation and various wafer-to-wafer or wafer-to-chip bonding technologies are illustrated. The finite element modeling of TSV process, essentially a chemical etching and subsequent passivation process, is discussed. A variety of wafer level bumping technologies is introduced, such as ball on I/O (BON), ball on polymer (BOP), redistribution dielectric layer (RDL) process, and copper post bumping process. The reliability improvement among different bumping technologies and the implications in SSL systems are presented. Newly

developed polymer-core interconnect technology and nanocolumn interconnect are discussed.

References

1. Zhang GQ, Beenakker CIM (2009) Shaping the new technology landscape of lighting, keynote address. In: Proceedings of the China SSL conference, 2009, Shenzhen, China.
2. Tsou C, Huang YS, Lin GW (2005) Silicon-based packaging platform for light emitting diode. In: 6th international conference on electronic packaging technology (ICEPT), 2005.
3. Chang-Hyun Lim, Won-Kyu Jeung, Seog-Moon Choi (2006) LED packaging using high sag rectangular microlens array, Micro-Optics, VCSELs, and Photonic interconnects II: fabrication, packaging, and integration. Proc SPIE 6185.
4. Zhang R, Lee SWR (2008) Wafer level LED packaging with integrated DRIE trenches for encapsulation. In: International conference on electronic packaging technology & high density packaging, ICEPT-HDP.
5. Zhang R, Lee SWR, Xiao DG, Chen HY (2011) LED packaging using silicon substrate with cavities for phosphor printing and copper-filled TSVs for 3D interconnection. In: 61th electronic components and technology conference (ECTC).
6. Uhrmann T (2010) Wafer-level-packaging for cost reduction of HB-LED. Semicon West.
7. Lau J, Lee SWR, Yuen M, Chan P (2010) 3D LED and IC wafer level packaging. Microelectron Int 27(2):98–105.
8. Fan XJ (2010) Wafer level packaging (WLP): fan-in, fan-out and three-dimensional integration. In: International conference on thermal, mechanical & multi-physics simulation, and experiments in microelectronics and microsystems (EuroSimE).
9. Fan XJ, Liu Y (2009) Design, reliability and electromigration in chip scale wafer level packaging, ECTC professional development short course notes.
10. Fan XJ, Varia B, Han Q (2010) Design and optimization of thermo-mechanical reliability in wafer level packaging. Microelectron Reliab. 50:536–546.
11. Reche JHJ, Kim DH (2003) Wafer level packaging having bump-on-polymer structure. Microelectron Reliab 43:879–894.
12. Kim D-H, Elenius P, Johnson M, Barrett S (2002) Solder joint reliability of a polymer reinforced wafer level package. Microelectron Reliab 42:1837.
13. Bumping design guide. http://www.flipchip.com/.
14. Kawahara T (2002) SuperCSPs. IEEE Trans Adv Packag 23(2).
15. Meyer T, Ofner G, Bradl S, Brunnbauer M, Hagen R (2008) Embedded wafer level ball grid array (eWLB). EPTC, 994.
16. Keser B, Amrine C, Duong T, Hayes S, Leal G, Lytle M, Mitchell D, Wenzel R (2008) Advanced packaging: the redistributed chip package. IEEE Transact Adv Packag 31(1).
17. Fan XJ, Han Q (2008) Design and reliability in wafer level packaging. In: Proceeding of IEEE 10th electronics packaging technology conference (EPTC), pp 834–841.
18. Rahim MSK, Zhou T, Fan XJ, Rupp G (2009) Board level temperature cycling study of large array wafer level packages. In: Proceeding of electronic components and technology conference (59th ECTC), pp 898–902.
19. Varia B, Fan XJ, Han Q (2009) Effects of design, structure and material on thermal-mechanical reliability of large array wafer level packages. ICEPT-HDP.
20. Ranouta AS, Fan XJ, Han Q (2009) Shock performance study of solder joints in wafer level packages. ICEPT-HDP.
21. Ko CT, Chen KN (2005) Wafer-level bonding/stacking technology for 3D integration. Microelectron Reliab. doi: 10.1016/j.microrel.2009.09.015.
22. Laermer F, Schilp A (1996) Method of anisotropically etching silicon. US Patent 5501893.

23. Laermer F, Urban A (2003) Microelectron Eng 67–68:349.
24. Kassing R, Rangelow IW (1996) Microsys Technol 3:20.
25. Ko WH (1995) Mater Chem Phys 42:169.
26. Chang KM, Yeh TH, Wang SW, Li CH, Yang JY (1996) Mater Chem Phys 45:22.
27. Chen KS, Ayon AA, Zhang X, Spearing SM (2002) J Microelectromech Syst 11:264.
28. Chung CK (2004) J Micromech Microeng 14:656.
29. Marty F, Rousseau L, Saadany B, Mercier B, Francais O, Mita Y, Bourouina T (2005) Microelectron J 36:673.
30. Beaudry R (2009) Deep reactive ion etching. US Patent 2009/0242512 A1.
31. Oldham WG, Neureuther AR, Reynolds JL, Nandgaonkar SN, Sung C (1980) IEEE Trans Electron Dev 27:1455.
32. McVittie JP, Rey JC, Bariya AJ, IslamRaja MM, Cheng LY, Ravi S, Saraswat KC (1991) Proc SPIE 1392:126.
33. Gerodolle AF, Pelletier J (1991) IEEE Trans Electron Dev 38:2025.
34. Harafuji K, Misaka A (1995) IEEE Trans Electron Dev 42:1903.
35. Zhou RC, Zhang HX, Hao YL, Wang YY (2004) J Micromech Microeng 14:851.
36. Tan YY, Zhou RC, Zhang HX, Lu GZ, Li ZH (2006) J Micromech Microeng 16:2570.
37. Miao M, Liao HG, Wan X, Zhao LW, Guo YX, Jin YF (2008) ICEPT-HDP, Shanghai, China.
38. Dong L, Lee SWR (2010) Simulation of through silicon via (TSV) forming with finite element modeling. Mater Chem Phys (to appear).
39. Mitsuka K, Kurata H, Jun Furukawa, Takahashi M (2005) Wafer process chip scale package consisting of double-bump structure for small-pin-count packages. Electron Compon Tech Conf 572–576.
40. Anderson R, Tee TY, Tan LB, Ng HS, Low JH, Khoo CH, Moody R, Rogers B (2008) Integrated testing, modeling, material and failure analysis of CSP for enhanced board level reliability, 2008, IWLP.
41. Tee TY, Tan LB, Anderson R, Ng HS, Low JH, Khoo CP, Moody R, Rogers B (2008) Advanced analysis of WLCSP copper interconnect reliability under board level drop test. 10th EPTC conference proceeding, 1086–1095.
42. Tee TY, Ng HS, Syed A, Anderson R, Khoo CP, Rogers B (2009) Design for board trace reliability of WLCSP under drop test, 2009. EuroSimE.
43. Varia R, Fan XJ (2011) Reliability enhancement of wafer level packages with nano-column-like hollow solder ball structures. In: 61th electronic components and technology conference (ECTC).
44. Eagelmaier W (2007) Achieving solder joint reliability in a lead-free world—part 2, Global SMT & Packaging, v.7, 45–46. http://www.globalsmt.net/documents/Columns-Engelmaier/7.7_engelmaier.pdf.
45. Okinaga N, Kuroda H, Nagai Y (2001) Excellent reliability of solder ball made of a compliant plasticcore. Electron Compon Tech Conf 1345–1349.

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