MEMS Reference Shelf

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MEMS Material

MEMS Materials and Processes Handbook

MEMS Reference Shelf

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Foreword

The field that is affectionately known as "MEMS" (an acronym for Micro-Electro-Mechanical Systems) is a descendant of the integrated circuits industry, but a descendent that has developed in ways and directions never anticipated by its parent. Now a highly specialized discipline in its own right, MEMS draws not only on all of conventional microelectronics but also on novel fabrication methods and uses of non-microelectronic materials to create devices that are mechanical, or fluidic, or biochemical, or optical, many without any transistors in sight. The key words are *sensors* and *actuators*, sometimes combined with (or without) microelectronics to create complete microsystems. MEMS devices and microsystems are now found everywhere – in automobiles, in ink-jet printers, in computer games, in mobile telephones, in forensic labs, in factories, in sophisticated instrumentation systems launched into space, in the operating room and in the clinic. The genie is out of the bottle. MEMS devices are everywhere.

Because of this immense diversity, no single book can capture the essence of the entire field. But all MEMS devices represent highly specific answers to two critical questions: "How shall I make it? And from what materials shall I make it?" Processes and materials. Materials and processes. Because these two challenges are common to *all* MEMS devices, it makes sense to gather the wisdom of the least several decades on "how to make it" and "from what materials" into a single data-rich, process-detail-rich compendium. That is the *raison d'etre* for this volume, and that is its goal: to document MEMS processes and materials at a sufficient level of detail to be of significant practical use.

I congratulate the co-Editors, Reza Ghodssi and Pinyen Lin, as well as our consulting editors and all of the contributors, for their diligence, persistence, care, and skill in bringing this material to published form, and I invite the MEMS community world-wide to benefit from the knowledge, wisdom and cumulative expertise gathered into these pages.

Brookline, Massachusetts — Stephen D. Senturia
June 2010

Preface

Throughout the relatively short history of microelectromechanical systems (MEMS), there have been numerous advances and inventions directly related to device fabrication. From humble beginnings using borrowed and modified IC fabrication techniques to current MEMS-specific tools such as deep reactive ion etching (DRIE) using inductively coupled plasma (ICP) sources, MEMS researchers have continually advanced and augmented the capabilities of wafer-based fabrication technologies. These advances have been instrumental in the demonstration of new devices and applications – Texas Instruments' Digital Micromirror Device, the MIT microturbine, Analog Devices' accelerometers – and even in the creation of new fields of research and development: bioMEMS, microfluidic devices, and optical MEMS.

To date, a number of books have been written about these new fabrication technologies and materials in general, but discussion of their relationship to MEMS design has been minimal. As a particularly diverse and multidisciplinary area of research, the field of MEMS offers a vastly different set of challenges relative to typical IC fabrication and design. Much effort is often focused on characterization runs and developing in-house recipes and specific processes to develop and manufacture MEMS structures, each time at the risk of wasting research efforts and "reinventing the wheel." A wealth of knowledge exists in the MEMS community, but much of this expertise is most readily accessed by informal, nonmethodological means such as discussions with colleagues at conferences. The authors of this book have observed an unnecessarily steep learning curve for the development of common MEMS processes, and believe the time spent traversing this curve would be better spent brainstorming new ideas and uncovering new applications. This book was conceived and born of this belief.

A fundamental and comprehensive MEMS-focused reference book will be an important asset for current and future research scientists and engineers. It was decided early in the brainstorming sessions for this book to include *materials* as well as *processes* in the discussion, as MEMS utilizes a wide variety of each in common applications. We intend this book to provide the reader with the basics of MEMS materials and processes, but beyond this goal, we intend for it to give practical insight into the workings and standard procedures carried out in research labs

and production facilities on a daily basis. To this end, each chapter has an extended section with case studies, giving step-by-step examples and recipes prepared by experts in industry and academia. Particularly, the effect of processing conditions on material properties are covered where applicable, illustrating the interdependence and multidisciplinary nature of MEMS fabrication. The chapters are meant to be a springboard of sorts, providing basic information about each topic, with a large number of classic and contemporary literature references to provide in-depth knowledge. Ultimately, it is our goal to provide a useful design reference volume for the seasoned researcher and the MEMS newcomer alike. We hope this book consolidates important information for readers and thereby spurs the creation of many new devices and processes.

MEMS devices are essentially microsystems that have structures and empty space built together. The authors of this book view the materials and processes as the fundamental building blocks for making those structures and empty spaces. Keeping this in mind, the book is divided into two main sections: Chapters 2, 3, 4, 5, and 6 covering materials and Chapters 7, 8, 9, 10, 11, 12, and 13 covering fabrication techniques. These two general thrusts are bookended by Chapter 1, which discusses general MEMS design, and Chapter 14, which deals with MEMS process integration.

Chapter 1 provides a basic framework for the design of MEMS systems and processes, which we highly recommend reading before diving into the materials and process sections of the book. Chapter 2 presents an overview of the recipes and methods used in the deposition of semiconductor and dielectric thin-films, particularly those most commonly used in the fabrication of MEMS. The basics here include chemical vapor deposition, epitaxy, physical vapor deposition, atomic layer deposition, and spin-on techniques. Additive processes for depositing metal films are discussed in detail in Chapter 3, where particular attention is paid to thick metal deposition with significant coverage devoted to electrochemical and electroless plating processes that are often required for MEMS fabrication. The entirety of Chapter 4 is devoted to the use of polymeric materials for MEMS. Polymers, such as polydimethylsiloxane (PDMS), are important materials for a vast array of devices, as encapsulants for tactile sensors and as an integral enabling technology for the emerging field of bioMEMS. The piezoelectric films detailed in Chapter 5 are an important part of MEMS technology, serving as both sensor and actuator elements. The basic properties of these materials and the physics of operation are described in detail as well as practical deposition and fabrication methods. Chapter 6 focuses on the fabrication and integration of shape memory alloy (SMA) materials, which provide high-force and high-displacement actuator mechanisms for MEMS.

Chapter 7 begins the section on processing of materials for MEMS applications by covering the very important area of dry etching methods (including DRIE), particularly the influence of different parameters on the etch recipe development process. Complementing the coverage of dry etching, wet etching processes for MEMS micromachining are covered in Chapter 8 with a comprehensive recipe and reference list included in this chapter to aid in finding etch rates and etch selectivities for a wide range of materials from silicon to III–V compound semiconductors.

Chapter 9 describes the technology of lithography and related techniques, covering traditional contact lithography, projection and X-ray lithography, and more exotic direct-write and printing lithographic techniques. Doping processes typical in and for MEMS applications for electrical purposes and etching control are reviewed in Chapter 10, along with diagnostic techniques for these methods. Wafer bonding, a crucial fabrication technique for silicon MEMS encapsulation and structure fabrication, is covered in detail in Chapter 11 with emphasis placed on direct and intermediate layer bonding methods.

Chapter 12 discusses the still-evolving field of MEMS packaging, pointing out differences with current microcircuit packaging techniques; this chapter in particular highlights how MEMS devices present very unique challenges as compared to traditional microcircuits. Surface treatments for MEMS devices are discussed in Chapter 13, covering antistiction and planarization coatings, functionalization of surfaces for biological and optical applications, and chemical mechanical polishing (CMP). Chapter 14 concludes the book with a discussion of the integration of any number of the above processes and materials into a compatible and efficient process flow, referred to here as *process integration*. The final chapter also discusses economic and practical aspects of process integration, citing some commercially successful examples of MEMS devices.

This reference volume would not have been possible without the help of many of our colleagues in the MEMS fields, from both academia and industry. We would like to extend words of thanks and gratitude to Stephen (Steve) Senturia for providing the vision, support, and guidance to our team over the past five years in navigating the completion of the chapters and for reviewing them diligently, and to the Series Associate Editors Roger Howe and Antonio (Tony) Ricco for carefully reviewing the chapters, providing helpful comments, and for recommending prospective contributing authors. We thank Steven (Steve) Elliot, from Springer, for his patience in dealing with thirty-five unique and independent experts, and his persistence in contacting each of us in order to develop the logistics for the book publishing process. Last but not least, we acknowledge all thirty-five contributing authors, who selflessly gave time, expertise, effort, and creativity to make this book a one-of-a-kind contribution to the current and future MEMS community, including industry and government professionals, academic faculty and staff, and students.

The idea for this book was born at the *Transducers 2005 Conference* in Seoul, South Korea, and it was finalized and finished at *The Hilton Head 2010 Workshop* on Hilton Head Island, South Carolina. The five years of cooperative activity that culminated in this handbook prove that great ideas can become reality when colleagues work collaboratively to achieve a common goal. This message, which we have tried to convey by writing this book, is what the greater MEMS community is all about.

College Park, Maryland Reza Ghodssi
Taoyuan, Taiwan Pinyen Lin

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Chapter 1
The MEMS Design Process

Tina L. Lamers and Beth L. Pruitt

Abstract Today's ubiquitous commercial MEMS devices, such as accelerometers, inkjet printheads, pressure sensors, and micromirror arrays, took 10–20 years from first report to commercialization. Timelines from initial development through product release for some successful MEMS commercial products have been getting shorter as MEMS technologies have matured. Companies can no longer afford such long development times. MEMS development time can be systematically shortened through the use of structured design methods. This chapter overviews the design process and design methods, illustrating structured design methods through case studies. We suggest reading this chapter prior to getting into the details of materials and process seletion, and applying the methods described to shorten development time.

1.1 Introduction

Innovation still thrives, but MEMS designers increasingly leverage existing processes and technologies in new products. Figure 1.1 shows the timelines of some of the earliest MEMS technologies from initial reports, typically based on academic research, to launch as a mature commercial product. Figure 1.1 also includes representative images of modern products reprinted with permission of the following companies: a digital pressure sensor by Freescale incorporates calibration and compensation in a paired ASIC; an inkjet cartridge by Hewlett Packard uses integrated circuitry in the nozzle region of thermal inkjet chip to control droplet size and placement; high aspect ratio MEMS accelerometers by Freescale provide on-axis stability; the digital micro-mirror for digital light projection by Texas Instruments led a revolution in optical MEMS and light switching products; Seacoast Science's micro gas chromatograph sensor arrays use micromachined,

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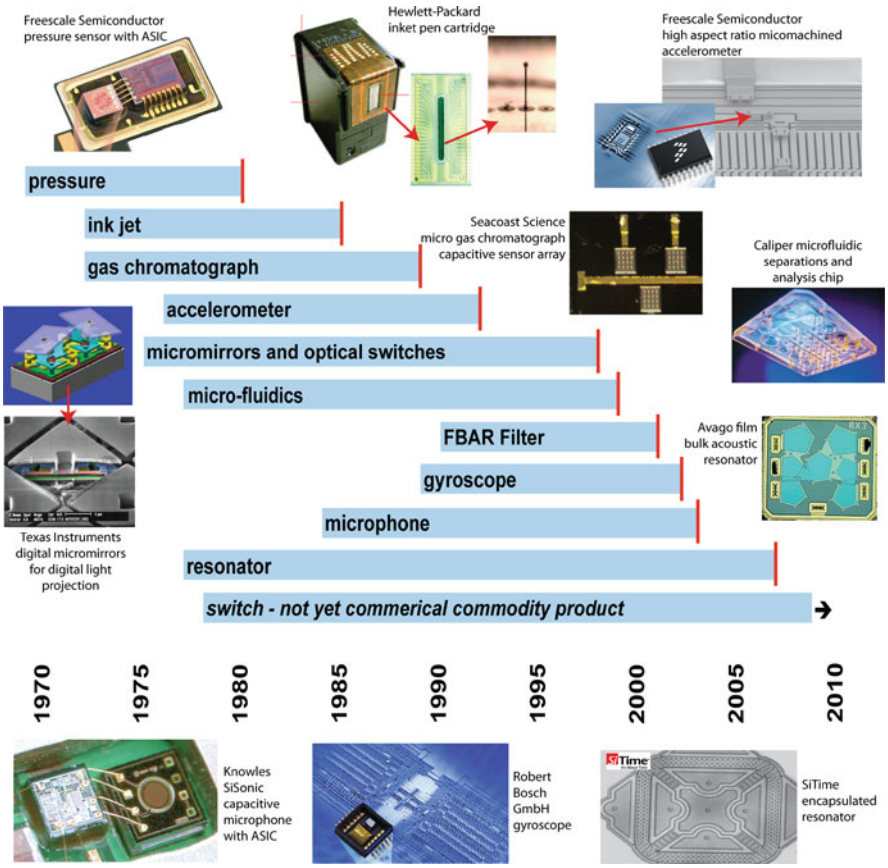


Fig. 1.1 Timeline of research and development cycles from first research reports to first commercialization of several MEMS products. Modified figure, used with permission of Kurt Petersen. Product images used with permission of the copyright holders as indicated above

parallel-plate polysilicon capacitors filled with polymers; microfluidic chips by Caliper integrate sampling, separations, and analysis; film bulk acoustic resonators (FBAR) by Avago Technologies revolutionized electronic filter design for the handset market; encapsulated resonator timekeeping references by SiTime compete with quartz; micromachined MM3 electronic stability program (ESP) gyroscopic sensor cluster by Bosch enables consumer and automotive orientation sensing; SiSonic microphones by Knowles dramatically enhance the manufacturability of printed circuit boards compared to polymeric electret condenser microphones. This historical timeline is far too long for most new products; companies cannot afford to fund development efforts that may not be profitable in one or two decades. However, MEMS product placement can be improved and development time can be systematically shortened through the use of structured design methods. This chapter overviews the design process and design methods, illustrating structured design

methods through case studies. We suggest reading this chapter prior to getting into the details of materials and process selection, and applying the methods described to shorten development time.

First, we review what is arguably the beginning of MEMS history. Piezoresistive silicon strain gauges were introduced in the late 1950s by Kulite Semiconductor, Bell Lab's first licensee of patents on semiconductor piezoresistance reported in 1954 [1]. Kulite's strain gauges represent some of the first commercially distributed microelectromechanical systems (MEMS) [2]. Although research on microsystems grew over the ensuing decades [3, 4] relatively few became widespread commercial products until manufacturing advances driven by the integrated circuits industry were widely available; Fig. 1.2 details several time points of developments in the integrated circuits industry that advanced piezoresistive MEMS design.

Accelerated product development cycles can be expected if designers leverage existing knowledge of materials and processes to simultaneously design new transducers. For example, Fig. 1.1 shows fairly short design-to-market timelines for pressure sensors and inkjet printheads; these earliest commercial devices leveraged recent material and process developments in the integrated circuits (IC) industry, primarily with the addition of wet etch technology to create through-holes and membranes. Many ensuing MEMS developments track technological advances in the IC industry and the development of micromachining (MEMS) specific processes accelerated innovation and commercialization of improved versions of existing MEMS transducers and development of new MEMS products (e.g., Fig. 1.2 for piezoresistive MEMS). For example, advances in polysilicon, metals, and surface micromachining also enabled rapid advances for accelerometers, digital micromirrors for digital light projectors, gas chromatographs, and film bulk acoustic resonators. Subsequent advances in dry etching created opportunities for smaller devices, denser packing on a wafer, and the large aspect ratios needed for channels or multiaxis devices. Silicon-on-insulator (SOI) wafer processes enabled thinner membranes of high-quality single crystal silicon (SCS) and epitaxy and other thick film growth processes enabled wafer scale packaging of high-vacuum components such as SiTime's resonators. Note also that the more recent product development cycles for gyroscopes and film bulk acoustic resonators were shorter than many previous products as these products leveraged existing materials and processes with targeted innovations in material and design performance. Follow-on products must reach market quickly if they are to compete with existing products and build or maintain market share with new designs.

This chapter begins with an overview of the design process and then moves into recommended MEMS design methodologies. Case studies are used to illustrate the methods. Material and process selection approaches are then described. Additional methods such as modeling, design optimization, uncertainty analysis, and failure modes and effects analysis are also introduced. Finally, the timing for utilizing design methods is discussed. Although it is not possible to cover all aspects of design methods for MEMS in this chapter, the following sections provide a good introduction to a set of useful tools for MEMS development as well as references for finding more in-depth information.

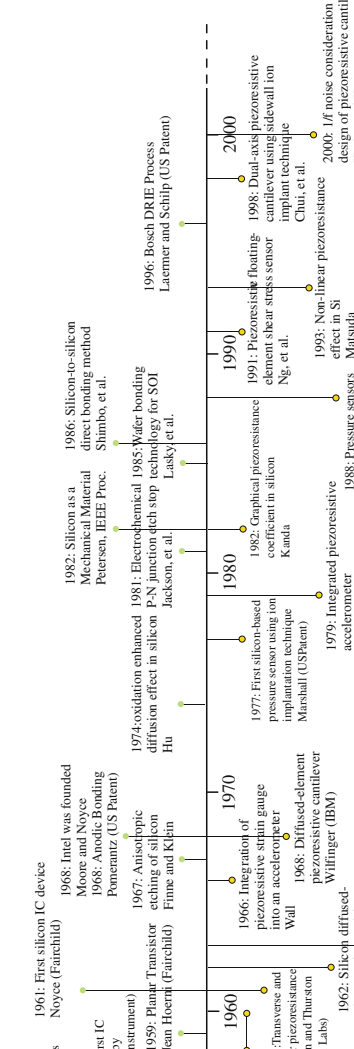


Fig. 1.2 Timeline of some technological advances in fabrication (above the *horizontal line*) and micromachining, particularly as pertains to piezoresistive sensing (below the *horizontal line*) [1, 2, 5–33]. Modified figure, used with permission of IEEE. First appearing in Barlian et al. [34]

1.1.1 Design Process

The design process begins with defining product requirements for the MEMS device. These requirements are determined through interviews and surveys of customers and users, as well as reviews of competitive products, and are defined in terms of customer specifications. Ultimately, quantitative metrics for the specifications are needed to measure and compare product performance against the requirements. The first step of describing the customer and defining the market can be challenging for a MEMS designer. A flowchart of the design process begins with the product definition phase and requires customer and market knowledge (Fig. 1.3). Very different requirements will be voiced depending upon whether the MEMS device is targeted as a component in a consumer product (e.g., accelerometers or microphones in Smartphones), or as an enabling technology integrated in a larger system (e.g., Polychromix *PhazIR*™ portable near-infrared spectrometer systems leverage software, hardware, and custom chips) to deliver an integrated, portable material inspection tool.

The product definition phase is often driven by marketing and sales teams who interface directly with consumers. However, design, process, and test engineers best know the in-house and supply chain capabilities, can readily define quantitative process and performance metrics, and can evaluate how these trade off with customer requirements. Thus, the product definition phase should involve all stakeholders in this product and customer/market definition phase. Once participants agree on the customer and market, the "voice of the customer" in terms of "soft" customer wants and "hard" measurable performance metrics can be related and ranked by importance. The design team then knows where to focus the most effort to achieve a product that best meets the most customer requirements, usually trading off cost with complexity. Quality function deployment (QFD) is a tool that formalizes this process, as explained in more detail later in this chapter.

A separate analysis of requirements and their relative weights should be completed for each customer and market. With these customer requirements, the design team can brainstorm concepts that simultaneously consider materials, processing, and packaging (Chapters 2–13 provide guidance on coupled material and process selection as well as packaging options). Concepts with geometric and material property detail are analyzed for predicted performance and the design can be refined based on results from analytical, numerical, or finite element models using data from in-house processes or the literature. Models for the performance of common classes of MEMS transducers are available elsewhere [35–37]. Concept screening (CS), a tool to streamline the process of selecting a design idea to prototype, is demonstrated later in this chapter.

Designers should take care to build in test structures and checkpoints in the process to more accurately evaluate process-dimensional tolerances and resulting material properties of as-fabricated structures. The overall performance of the device or system should be carefully considered with signal conditioning and systems integration (see Chapter 14). MEMS commercial products use both complementary metal oxide semiconductor (CMOS) integrated signal conditioning on the

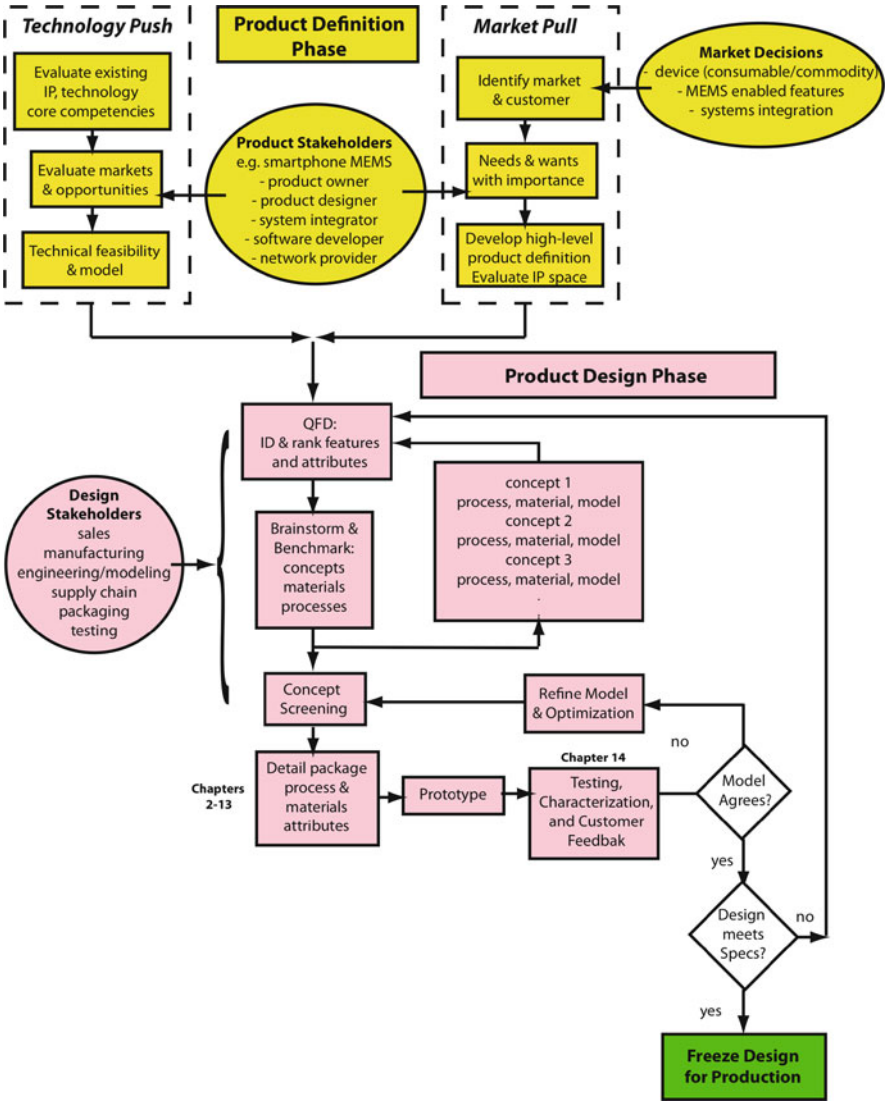


Fig. 1.3 Design flowchart. The product definition phase begins with defining and understanding the customer(s) and market. Structured design methodologies guide the translation of customer requirements into design features and concepts and allow the designer to simultaneously consider process, material, and performance in the design. The design process is not linear and short loops on materials and process selection should feed back frequently through stakeholder design reviews

same chip as the MEMS structures and also application-specific integrated circuits (ASICs) in multichip modules for signal conditioning. Usually, the impact of reliability and yield on overall size and cost requirements drive this decision. At each stage of the process, short loops on critical design parameters (materials, dimensions, interfaces, processes) should be investigated with appropriate test wafers and test structures before entire lots of wafers are processed. This enables the design team to revisit aspects of the design before an entire mask set or entire fabrication run is committed.

The rest of this chapter provides more detail and case studies demonstrating the flowchart steps in Fig. 1.3.

1.2 Design Methods for MEMS

Many examples demonstrate the benefits of using design methods [38–41], and design methods are commonly applied in industries from automotive to aerospace to semiconductors. Yet, design methodologies have less frequently been applied to MEMS products [42, 43].

1.2.1 History of Design Methodologies

One of the key design methods used in product development is quality function deployment (QFD). QFD is a tool that helps relate what is important to the customer to decisions made in the design and manufacturing process. Mapping the customer requirements to the metrics and specifications the design team uses helps in the creation of a product that satisfies customer desires, resulting in more focused development and higher sales volumes.

QFD was first used in 1971 in the Kobe shipyard of Mitsubishi Heavy Industries [38]. In 1972, Dr. Yoji Akao published an article on what he called Quality Deployment and is now called QFD [44]. Akao had been developing and teaching his method for several years prior to the publication of the article. The Kobe shipyard work was published by Nishimura shortly after Akao's first article [45]. Over time, the demonstrated results of using QFD encouraged others to adopt the tool and usage became widespread in Japan. Toyota and its suppliers continued development of QFD to help with their focus on customer values. Through the 1970s and early 1980s, Japanese companies used QFD to improve the effectiveness of their product development [38, 46]. In the mid 1980s, Xerox and other U.S. companies started to use QFD along with design for assembly (DFA) as part of their drive to regain competitiveness in U.S. manufacturing. Primarily heavy industry companies, such as automobile manufacturers, adopted QFD, with limited adoption into high-technology fields such as semiconductors. QFD has typically been applied to products as opposed to manufacturing processes. Professor Don Clausing at MIT helped champion QFD in the United States [46], and some companies such as ITI even created QFD software [38].

QFD is meant to provide guidance in product development. As such, it should be used with other management and technical tools, such as strategy planning, rapid prototyping, design of experiments, and design for assembly, to produce an effective development project. The output of QFD still needs to be subject to human judgment and is not meant to automate the design process [47].

The effectiveness of QFD has been documented in many sources over the past 30 years. A few examples noted by ReVelle, Moran, and Cox [38] include:

- A Brazilian steel company, which used QFD on the components it produced for automotive suspension springs, experienced a market share increase of 120%, a fall in customer complaints by 90%, and a 23% reduction in production costs between 1993 and 1998.
- Motorola America's Parts Division, where customers reported being 60% more satisfied with their product and pricing information after QFD principles were used to improve the system.
- The Wiremold Company used QFD for its new product development starting in 1991. By 1994, new product development time had fallen from 24–30 months to 6–9 months, enabling the introduction of six to eight times more products per year.
- Toyota Auto Body Company in Japan reduced startup costs for the introduction of four van models by 61% over a 7-year period, while simultaneously reducing the product development cycle time by one-third.

QFD is a multiple-stage tool, although frequently only the first one or two parts are used on a given product development effort. The stages of QFD are commonly referred to as houses. The houses are pictorially shown in the top part of Fig. 1.4. House I, sometimes referred to as the House of Quality, translates the "soft" customer wants into measurable engineering attributes or specifications. House II then takes these engineering characteristics and maps them to parts characteristics, or attributes of the product's parts. House III matches up parts characteristics to process operations, and House IV aligns process operations with production requirements.

1.2.2 Structured Design Methods for MEMS

Existing design methods are not always well suited to the MEMS product structure or development process. In the case of QFD, some of the difficulty of using the tool for MEMS comes in QFD Phase II, where engineering metrics are linked to parts. Most MEMS do not have physical "parts" that are assembled into a final device, but instead have product specifications and a manufacturing process used to create the product. The physical form is determined through the fabrication process, demonstrating a tight linkage between the MEMS product and process. MEMS also have more integrally linked material functions with process and specifications than many other types of products. For example, silicon comes in several crystalline forms such as amorphous, polysilicon, and single-crystal silicon, each with distinctly different properties. The desired end product specifications and physical

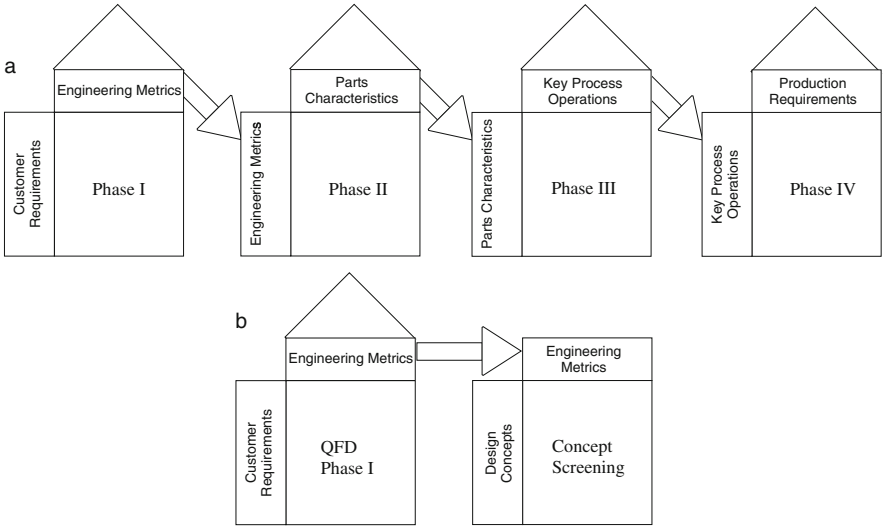


Fig. 1.4 (**a**) Houses of QFD, after Hauser and Clausing [46] and (**b**) QFD Phase I plus concept screening to enable consideration of design of process and devices simultaneously for MEMS. Modified figure, used with permission of K.L. Lamers. First appearing in Lamers [43]

form have large ramifications on which fabrication process and material variety are chosen, and vice versa. The tight link between product and process was utilized in creating concept screening, a tool that relates engineering metrics to design concepts, including product conceptualization and manufacturing process. Concept screening is a simple matrix tool that allows designers to evaluate design concepts against important engineering metrics. The tool combines portions of QFD Phases II and III into one phase to make the tool more readily applicable to MEMS. It also contains aspects of Pugh concept selection [48], and differs from typical QFD primarily in consideration of product idea and manufacturing process together in the early phases of product definition. The design methods recommended for MEMS are shown in the lower portion of Fig. 1.4.

QFD Phase I and concept screening are demonstrated in this chapter as design methods well suited to MEMS. Additional methods, such as brainstorming and materials selection, are utilized in concert with QFD and CS. Using methods to be better aligned with the unique requirements of MEMS may lead to improved MEMS product development. Improvements in MEMS product development may be measured through a decrease in time to market, fewer development iterations, reduced development or product costs, or increased product revenue.

1.3 Brainstorming

Brainstorming is an idea generation activity involving the key stakeholders in product definition, development, and implementation [49]. It may be carried out in one

session or it may be done over several sessions covering multiple topics, such as user requirements, technical specifications, and design concepts. In a corporate setting, the constituents participating in brainstorming may include engineers for devices, packaging, testing, manufacturing, marketing, and sales. Briefly, the brainstorming session process might be comprised of: a moderator (project leader) who gathers the key participants in a comfortable space with ample whiteboard space, markers, Post-its, or other means to record and move information around, keeping ideas visible to participants. If the group does not regularly work together, the moderator should lead icebreaker or warm-up activities to familiarize participants with each other and encourage free-thinking and communication. The moderator then describes the objective(s) of the exercise with the key requirements (high-level) for the product; the moderator ensures all ideas are captured. Some brainstorming rules the moderator must enforce include:

- No idea is a bad idea (try saying "yes, and...", then morphing and building to other ideas).
- Be creative and take risks (above all, keep ideas rolling).
- No criticism allowed (no "buts, excepts, or howevers").

At the end of the brainstorming session, the group should review the ideas generated, consolidate like concepts, check these against product requirements and restrictions, and then vote on the top candidates to trim the list to the top five to ten ideas. These ideas are then fleshed out with materials, processes, structures, and rough performance models. The concepts are benchmarked against similar products and processes, and then systematically evaluated against customer requirements. Another brainstorming loop may be needed if none of the concepts looks promising.

1.4 Microphone Case Studies

1.4.1 Microphone Background

Microphones, in the class of acoustic sensors, provided motivation for Avago Technology's acoustic sensor project and Knowles SiSonic MEMS microphone. The Avago case study demonstrates a technology-push-type of program that employs formal design methods to evaluate the applicability of existing technology to a perceived market opportunity, whereas the Knowles SiSonic case study demonstrates a market-pull design process whereby a microphone company without MEMS technology developed the tools and processes to meet market needs.

Microphone (mic) technology, which had been fairly stable for the better part of 50 years, has seen large changes in the past few years with the introduction of MEMS microphones. Electret-condenser microphones (ECMs) comprise the majority of microphones (mics) used in consumer electronic devices, such as cellular handsets. They offer reasonable sound quality at low cost and typically contain a polymer membrane within a metal case. ECMs could not withstand solder reflow processes due to their low melting point materials. As a result, costly

hand insertion was required to mount ECMs on a board. This limitation provided an opportunity for alternative mic technology to penetrate the cellular handset and other large audio markets. Capacitive silicon mic technology is one such alternative, currently growing over 100% per year and accounting for nearly all the growth in new mic technology today.

Capacitive mics have limitations due to their dual plate design, such as failures related to moisture exposure and the need for a charge pump to bias the membrane. Piezoelectric mics comprise a single membrane, therefore alleviating these challenges, although their sensitivity is lower for mics on the MEMS scale.

1.4.2 The Avago Story

Avago Technologies has produced more than one billion film bulk acoustic resonator piezoelectric bandpass filters, primarily used in cell phones. Inasmuch as Avago's FBAR technology dominates the cell phone bandpass filter market, the company decided to look for ways to extend the use of their technology. Investigation began to apply FBAR and other core technologies to new uses and markets such as acoustic sensor applications. The high-volume FBAR production process was leveraged to enable fast prototyping of piezoelectric MEMS microphones. Using FBAR to create an acoustic sensor involves many design analysis aspects, including basic plate bending theory, more complex finite element analysis, device layout, and fabrication. Characterization, acoustic modeling, packaging, and testing methods all have to be developed and implemented. Design of each element must be cognizant of the requirements of the other elements in order to optimize the product for performance, cost, and fit to market [50]. QFD Phase I and CS help focus development efforts on the most important aspects of the design from a customer perspective, balancing efforts among the design elements and providing a means to assess tradeoffs. Design for manufacturability methodologies can help project teams make their way through the maze of product development issues and emerge with a technically and financially successful product. The application of QFD Phase I and CS to Avago's acoustic sensor program serve to demonstrate the use of these tools. Although development of Avago's acoustic sensor is on-going, activities described in this case study exemplify a means to develop products rapidly and gain understanding of potential market impact, which provide useful understanding for other product development efforts.

1.4.2.1 Design Process and Methods

A standard FBAR fabrication process was used as the basis of the initial microphone process to enable fast prototyping. A plate mechanics model and finite element analysis guided initial design and process choices [50]. While the initial experiments were being run, QFD Phase I and CS were applied to the acoustic sensor, with the tool application repeated for several potential market applications. The results were used in three ways. First, they were used to determine on which aspects of the design to focus. Second, the results helped determine which design concepts were likely to

be viable to carry forward through prototyping. Finally, CS was used to determine which market or markets were a good fit for the technology.

QFD Phase I

Figure 1.3 shows where QFD fits in the overall product development effort. For the Avago mic project, QFD Phase I was used in the Stanford University Manufacturing Modeling Lab standard format, relating customer requirements to engineering metrics [39]. In this format, a matrix is generated in which rows correspond to qualitative customer desires such as size or ease-of-use. The customer requirements are listed in the leftmost column of the matrix, and defining the customer requirements is the first step in QFD I. These customer needs are then rated 1, 3, or 9, where "1" is considered somewhat important, "3" is important, and "9" represents very important. Customer requirements and their weightings can be determined via customer interviews, focus groups, competitive products, or sales and marketing inputs, among other means. Brainstorming, described in the following section, can also be used to generate aspects of QFD and CS.

Columns correspond to specific, quantitatively measured engineering metrics, for example, linear dimension less than 1 mm. The engineering metrics are synonymous with product or process specifications, and are listed in the top row of the matrix. Where possible, quantitative targets that correspond to these metrics are located in a row labeled "Technical Targets" near the bottom of the matrix.

Next, the matrix is filled out with the relative relationship between each customer requirement and engineering metric in the intersecting matrix element. The weighting scheme of 0, 1, 3, or 9 is used, where "0" denotes no relationship, "1" shows a slight relationship, "3" means a significant relationship, and "9" represents a very important relationship. The products of the customer requirement importance and the relationship weighting between customer requirement and engineering metric are summed over each column to generate raw scores for each engineering metric. Each column score is then translated to a percentage of the total score, with the highest percentage items denoting the most critical engineering metrics. The relative importance percentages for the engineering metrics provide guidance on the appropriate amount of product development effort to be spent achieving each engineering metric. For background and more detailed information on performing QFD, see [38, 39].

The results of QFD Phase I as applied to the use of the piezoelectric microphones in cellular handsets, laptops, and automotive sensor applications are shown in Figs. 1.5, 1.6, and 1.7, respectively. The customer requirements and their weightings for each application were gathered through domain research and conversations with industry insiders. For example, each application has a customer requirement related to size. Cellular handsets have "fits in cell phone," laptops have a requirement of "fits in computer bezel or speaker phone," and automotive has "fits in engine compartment or body cavities." Although size is important in all three applications, as shown by the size requirement having a weight of 9 in all three cases, the specifics of the size required depend on the application. Auto engine compartments are much

			Engineering Metrics												
	Customer Requirements	Customer Weights	Sensitivity	Dynamic range	Noise Floor	Current Consumption	# of Manufacturing steps	Shock resistance	Moisture tolerance	Total packaged linear dimensions	Linearity/Distortion	Expected lifetime	Layout fit to ECMs	Temperature range of operation	Manufacturing capacity
1	Easy to hear (clear sound)	9	9	1	3	0	0	1	1	0	9	0	0	1	0
2	Fits in cell phone	9	3	0	0	3	1	0	0	9	1	0	0	0	3
3	Little to no sound distortion	3	9	9	9	0	0	1	3	0	9	0	0	1	0
4	Inexpensive	9	9	3	3	3	9	0	0	9	3	1	1	0	0
5	Lasts a long time	3	0	0	0	0	0	3	3	0	0	9	0	3	0
6	Can handle harsh use conditions	3	0	3	0	0	0	9	9	0	0	9	0	3	0
7	Doesn't degrade battery life	1	0	0	0	9	0	0	0	0	0	0	0	1	0
8	Covers human voice range	3	1	9	3	0	0	0	0	1	1	0	0	0	0
9	Drop-in replacement for ECM	3	9	3	3	3	0	3	3	3	3	3	9	3	1
10	Assurance of supply	3	0	0	0	0	0	0	0	0	0	1	0	0	9
	Technical Targets		?5mV/Pa	?40-110dB	40dB	?200uA @ 1.5-5.5V	<70 steps	>10,000g per IEC 68-2-27	>192Hr @ 85/85	?10mm	?1% THD (Total Harmonic D	>24 months	pad compatible	?-40 to 100C	>10 million/mo.
		Raw score	246	108	99	72	90	57	63	174	156	75	36	40	57
		Relative Weight	19%	8%	8%	6%	7%	4%	5%	14%	12%	6%	3%	3%	4%

Fig. 1.5 QFD Phase I application of piezoelectric acoustic sensor to cell phones (Modified figure, used with permission of ASME. First appearing in Lamers and Fazzio [50])

larger than cell phones, providing more leeway for fitting the automotive customer space requirement.

The engineering metrics and their targets came from existing product data sheets and the knowledge of the project technical team (Knowles; Akustica; Hosiden; Panasonic). The relationship weights between customer requirements and engineering metrics also came from members of the technical team. Customer feedback and comparisons to competitor products were used to validate the inputs and the results of QFD Phase I, in an attempt to improve the robustness of the results. Many engineering metrics appear in all three applications, although their target values vary according to the requirements of each application. In Figs. 1.5, 1.6, and 1.7 the engineering metrics that garnered the highest relative weights are highlighted. It is interesting to note that "Dynamic Range" and "Total packaged linear dimensions" were in the top weighted engineering metrics in all three applications. At the same time, the other top engineering metrics changed depending on the application. For example, "sensitivity" had the highest weight in both the cellular handset and laptop applications, but was just outside the top group for the automotive sensor application.

			Engineering Metrics												
	Customer Requirements	Customer Weights	Sensitivity	Dynamic range	Noise Floor	Current Consumption	# of Manufacturing steps	Shock resistance	Moisture tolerance	Total packaged linear dimensions	Linearity/Distortion	Expected lifetime	Layout fit to ECMs	Temperature range of operation	Manufacturing capacity
1	Easy to hear (clear soud)	9	9	3	3	0	0	1	1	0	1	0	0	1	0
2	Fits in computer bezel or speaker phone	9	3	0	0	3	0	0	0	9	0	0	0	0	0
3	Little to no sound distortion	3	3	9	9	0	0	3	3	0	9	0	0	3	0
4	Inexpensive	9	9	3	3	3	9	0	0	9	3	1	1	1	0
5	Lasts a long time	3	0	3	0	0	0	3	3	0	0	9	0	3	0
6	Can handle harsh use conditions	3	0	3	0	0	0	9	9	0	0	9	0	9	0
7	Requires little power	1	0	0	0	9	0	0	0	0	1	0	0	0	0
8	Covers human voice range	3	3	9	3	0	0	0	0	0	3	0	0	0	0
9	Drop-in replacement for ECM	3	9	3	1	9	0	3	3	9	3	3	9	3	0
10	Assurance of supply	3	0	0	0	0	1	0	0	1	0	1	0	0	9
	Technical Targets		?5mV/Pa	?40-110dB	30dB	?500uA @ 1.5-5.5V	≤70 steps	>10,000g per IEC 68-2-27	>192Hr @ 85/85	?25mm	?1% THD (Total Harmonic Di	>48 months	pad compatible	?-40 to 100C	>2 million/mo.
		Raw score	234	135	93	90	84	63	63	192	82	75	36	72	27
		Relative Weight	19%	11%	7%	7%	7%	5%	5%	15%	7%	6%	3%	6%	2%

Fig. 1.6 QFD Phase I application of piezoelectric acoustic sensor to laptops (Modified figure, used with permission of ASME. First appearing in Lamers and Fazzio [50])

Concept Screening (CS)

The output of QFD Phase I is used as input for CS. The intent of CS is to screen design ideas, providing the development team insight on which concepts are worth pursuing. CS is structured as a matrix, with design concepts comprising the rows and the most critical engineering metrics from Phase I in the columns. Each concept is evaluated in comparison to the high-importance engineering metrics.

The concept screening mechanics are detailed for application to readers' projects. Refer to Figs. 1.8, 1.9, and 1.10 for the Avago examples of the CS matrix format. To perform CS, follow these steps.

1. Analyze the QFD Phase I results to select the three, four, or five engineering metrics with the highest weightings. Only the three to five most important engineering metrics from Phase I are utilized in CS to make the tool fast and easy to use. The decision of whether to use three, four, or five engineering metrics is driven by the location of a natural breakpoint in the importance weightings of the engineering metrics. For example, if the percentages for the top five engineering metrics proceeded in decreasing order: 19, 15, 13, 12, and 8%, there is a natural breakpoint between the fourth and fifth most important metrics. In this case, the

			Engineering Metrics													
	Customer Requirements	Customer Weights	Sensitivity	Dynamic range	Noise Floor	Current Consumption	# of Manufacturing steps	Shock resistance	Moisture tolerance	Total packaged linear dimensions	Linearity	Expected lifetime	Standard Interface	Temperature range of operation	Manufacturing capacity	Process Lifetime
1	Takes correct action	9	3	3	0	0	0	9	9	0	0	0	0	1	0	0
2	Fits in engine compartment or body cavities	9	3	0	0	3	1	0	0	9	1	0	0	0	3	0
3	Accurate response over wide range of input levels	9	3	9	9	0	0	3	3	0	3	0	0	3	0	0
4	Inexpensive	3	9	3	3	3	9	0	0	9	3	1	1	1	0	0
5	Lasts a long time	3	0	3	0	0	0	3	3	0	0	9	0	3	0	0
6	Can handle harsh use conditions	3	0	3	0	0	0	9	9	0	0	9	0	9	0	0
7	Requires little power	1	0	0	0	9	0	0	0	0	1	0	0	1	0	0
8	Few or one system needed for whole auto	3	9	0	3	0	0	0	0	0	1	0	0	0	0	0
9	Easy to integrate into automobile	9	0	1	3	9	0	1	1	9	1	0	9	3	0	0
10	Assurance of supply	3	0	0	0	0	1	0	0	0	0	1	0	0	9	0
11	Available for many years	3	0	0	0	0	0	0	0	0	0	1	0	0	0	9
	Technical Targets		?18mV/g	?0-200g	?5mg/?Hz	?100uA @ 1.5-5.5V	<?0 steps	>10,000g per IEC 68-2-27	>380hr 85C/85%Rel. Humidity	?12mm	0.2% of full scale	>10 years	Serial Peripheral Interface	?-65 to 150C	>1million/mo.	>7 years
		Raw score	135	144	126	126	39	153	153	189	58	63	84	103	54	27
		Relative Weight	9%	10%	9%	9%	3%	11%	11%	13%	4%	4%	6%	7%	4%	2%

Fig. 1.7 QFD Phase I application of piezoelectric acoustic sensor to automotive (Modified figure, used with permission of ASME. First appearing in Lamers and Fazzio [50])

top four engineering metrics would be used in CS. If no such breakpoint is evident, use the top five engineering metrics. Put the chosen engineering metrics in the top row of the CS matrix.

2. Use design and manufacturing team brainstorming, competitor product information, literature, knowledge of process capabilities, or whatever other means are appropriate to create design concepts. Concepts should include physical form as well as materials and manufacturing process, but should not be to the level of detailed design. In this respect, the concepts are illustrated similarly to those used in Pugh's Concept selection [48]. Five to seven design concepts is a good target. Record the name of each design concept in the leftmost column of the CS matrix.
3. Evaluate each concept in comparison to the engineering metrics in the top row of the CS matrix, recording the score in the box where the concept and engineering metric intersect. A concept receives a "–1" if it is likely unable to meet the metric, "0" if it will likely meet the metric, and "1" if it is likely to exceed the metric.
4. Sum the scores for the concepts across the engineering metrics, and record the total score in a column on the right of the CS matrix. Rank concepts according to their total score.

Phase II QFD High Relative Weight Engineering Metrics

	Cellular Handset Application	Sensitivity	Dynamic range	Noise Floor	Total packaged linear dimensions	Linearity	Total Score	Rank
	Design Ideas							
1	Piezoelectric mic w/ DRIE backside cavity and annular electrodes	-1	0	0	1	0	0	1
2	Piezoelectric mic w/ KOH backside cavity and annular electrodes	-1	0	0	0	0	-1	2
3	Piezoelectric mic w/ DRIE backside cavity and continuous electrodes	-1	0	0	1	-1	-1	2
4	Piezoelectric mic w/ KOH backside cavity and continuous electrodes	-1	0	0	0	-1	-2	4
5	Piezoelectric mic w/ shallow cavity and annular electrodes	-1	-1	-1	1	-1	-3	5
6	Piezoelectric mic w/ shallow cavity and continuous electrodes	-1	-1	-1	1	-1	-3	5

Fig. 1.8 CS for piezoelectric acoustic sensor in cell phones (Modified figure, used with permission of ASME. First appearing in Lamers and Fazzio [50])

Phase II QFD High Relative Wt. Eng. Metrics

	Laptop Application	Sensitivity	Dynamic range	Total packaged linear dimension	Total	Rank
	Design Ideas					
1	Piezoelectric mic w/ DRIE backside cavity and annular electrodes	-1	0	1	0	1
2	Piezoelectric mic w/ KOH backside cavity and annular electrodes	-1	0	0	-1	3
3	Piezoelectric mic w/ DRIE backside cavity and continuous electrodes	-1	0	1	0	1
4	Piezoelectric mic w/ KOH backside cavity and continuous electrodes	-1	0	0	-1	3
5	Piezoelectric mic w/ shallow cavity and annular electrodes	-1	-1	1	-1	3
6	Piezoelectric mic w/ shallow cavity and continuous electrodes	-1	-1	1	-1	3

Fig. 1.9 CS for piezoelectric acoustic sensor applied to laptop (Modified figure, used with permission of ASME. First appearing in Lamers and Fazzio [50])

Phase II QFD

High Relative Wt. Eng. Metrics

	Automotive Sensor Application	Dynamic range	Shock Resistance	Moisture Tolerance	Total packaged linear dimension		
	Design Ideas					Total Score	Rank
1	Piezoelectric mic w/ DRIE backside cavity and annular electrodes	1	1	1	1	4	1
2	Piezoelectric mic w/ KOH backside cavity and annular electrodes	1	1	1	0	3	3
3	Piezoelectric mic w/ DRIE backside cavity and continuous electrodes	1	1	1	1	4	1
4	Piezoelectric mic w/ KOH backside cavity and continuous electrodes	1	1	1	0	3	3
5	Piezoelectric mic w/ shallow cavity and annular electrodes	−1	−1	−1	1	−2	5
6	Piezoelectric mic w/ shallow cavity and continuous electrodes	−1	−1	−1	1	−2	5

Fig. 1.10 CS for piezoelectric acoustic sensor applied to automotive (Modified figure, used with permission of ASME. First appearing in Lamers and Fazzio [50])

5. Analyze the results. The highest ranking concept or concepts are those most likely to be viable and most worthwhile to prototype. Overall scores indicate how well the design concepts fit the intended application, with scores above zero indicating a better fit than negative scores.
6. If there is more than one potential application, repeat QFD Phase I and CS for each application, keeping the design concepts constant. A comparison of total scores across applications will highlight how well the technology and design concepts fit the respective applications.
7. Utilize the CS results in determining the viability and direction of the project.

The interested reader is referred elsewhere [43] (ASME IMECE on scent dispenser) for more examples of the application of CS.

The CS results for the application of piezoelectric mics to cellular handsets, laptops, and automotive sensors are shown in Figs. 1.8, 1.9, and 1.10. The same six design concepts were used in each of the application areas. The concepts are the following.

1. Piezoelectric mic with Deep Reactive Ion Etching (DRIE) backside cavity and annular electrodes

2. Piezoelectric mic with Potassium Hydroxide (KOH) backside cavity and annular electrodes
3. Piezoelectric mic with DRIE backside cavity and continuous electrodes
4. Piezoelectric mic with KOH backside cavity and continuous electrodes
5. Piezoelectric mic with shallow cavity and annular electrodes
6. Piezoelectric mic with shallow cavity and continuous electrodes

These concepts were developed by the project technical team through consideration of such factors as ease in leveraging the current FBAR process capabilities, available in-house processing options, literature results for similar devices, and currently successful product structures.

QFD and CS were performed after the first round of prototyping, so the team was able to use initial test results in creating potentially viable design concepts. The concepts vary in aspects of the manufacturing process, such as using DRIE versus KOH versus RIE (Reactive Ion Etching) to create a cavity beneath the mic membrane. The concepts also differ in physical structure through the comparison of continuous versus annular electrodes. In this manner, important aspects of the physical design layout and function as well as critical manufacturing process options are represented in the concepts. The assessment of how likely a given concept was to meet a particular engineering spec was based upon the judgment of members of the technical team as well as initial test data and published results from other organizations. In analyzing the outcomes of CS, it is noted that design concept 1, "Piezoelectric mic with DRIE backside cavity and annular electrodes," ranked first in all three of the application areas, although it was tied for first with concept 3, "Piezoelectric mic with DRIE backside cavity and continuous electrodes," in the laptop and automotive areas. The relative ranking of the other concepts shifted depending upon the application. This result demonstrates that CS can be useful in distinguishing the viability of concepts in different application spaces. A second, even more enlightening result can be observed by considering the total scores the design concepts received. The total scores varied between the application areas, as the engineering metrics and targets changed. For example, "Sensitivity" was critical for cellular handsets and laptops but not as important for automotive applications. All the piezoelectric design concepts struggle to meet sensitivity targets, making the total scores generally lower in cell phone and laptop applications. The higher total scores in the automotive application suggest the piezoelectric acoustic sensor is better suited for automotive applications. This insight on technology fit to market is important to recognize and utilize.

The outcomes of the QFD I and CS offer clarity regarding which design concepts are most likely to succeed so that resources may be assigned commensurately. Reviewing the scores for each design can be a worthwhile exercise for assessing how many of the concepts have the potential to be successful. A score greater than or equal to zero shows a fair likelihood of the concept meeting the design requirements, whereas a negative score shows the concept will probably fail to meet critical design requirements. Designs with negative scores are probably not worthwhile to pursue further or require modification to become viable to pursue.

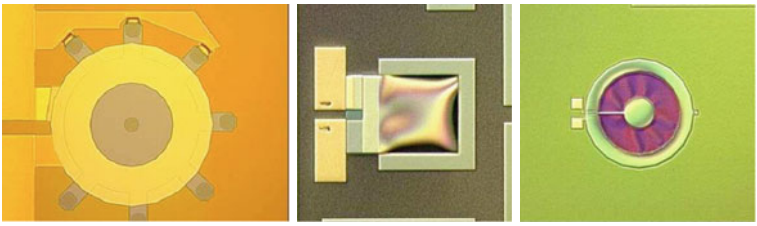
Results

Performance results of the Avago microphones are published elsewhere [50]. Over the course of the first 8 months of the project, hundreds of different designs were prototyped. These included circular membranes with electrodes covering the entire membrane surface, circular membranes with annular electrodes, circular membranes with electrodes restricted to the center of the membrane, circular membranes with combinations of annular and central electrodes connected in series and parallel combinations, and a variety of cantilevers.

Figure 1.11a–c provides images of representative devices showing several of these configurations. Other projects which diverged less substantially from existing technology have historically taken between 6 months and 2 years of iterations to progress as far as this much more difficult project did in 8 months through utilizing concurrent design and product definition phase design methodologies.

Extensive leverage of the FBAR process and infrastructure enabled fast fabrication of initial prototypes and allowed many iterations of prototyping in a short time span. Five complete mask turns and 17 distinct experimental runs were fabricated and tested within the first 8 months of the program. As devices were produced, they were tested for sensitivity. The results were then used in guiding future experiments and device layouts. Phase I of QFD provided the team with technical targets and guidance on which engineering metrics were most critical to achieve. "Dynamic range" and "Total packaged linear dimensions" were very important in all three application areas, whereas "Noise floor," "Shock resistance," "Moisture tolerance," and "Sensitivity" were key in at least one application.

CS gave the project team direction on which design concepts were most likely to meet the technical requirements for a given application space. In all three cases, the design concept of creating a piezoelectric microphone with a DRIE backside cavity and annular electrodes came with the highest rank. This concept was prototyped, and the test results supported the CS findings. Even more important than suggesting which design concepts to pursue, CS indicated which application space the technology might best fit through analysis of the total scores. In the cellular handset and laptop applications, the concept total scores tended to be zero or negative, showing



(a) (b) (c)

Fig. 1.11 Representative mic design options. (**a**) Annular electrodes, (**b**) cantilever, and (**c**) nested electrodes (Modified figure, used with permission of ASME. First appearing in Lamers and Fazzio [50])

the piezoelectric microphone design ideas would have difficulty meeting critical technical specifications. In automotive sensors, the total scores ranged from –2 to +4. The design concepts with positive scores are more likely to meet the important technical requirements. This result indicates, at least for the design concepts considered, that the technology is better fit to application in automotive sensors than in cellular handsets or laptops. Early prototype test results aligned with this CS outcome. The CS results drove realignment of the program to markets that matched the technology capabilities. Technical challenges remain in piezoelectric microphone development. As development continues, QFD Phase I and CS should be repeated with refined customer requirements, engineering metrics, and design concepts. In this manner, the tools will provide continued guidance throughout the course of the project.

The general methodology of QFD I and CS may be utilized for rapid development of other products and technologies. QFD Phase I can be applied to MEMS in the standard format, and gives insight on the most critical engineering metrics on which to focus design efforts. The results of Phase I are made more robust through validating the customer requirements and engineering metrics via feedback from customers and competitive product data. Use of engineering judgment in evaluating the tool results is also important. The concept screening tool, used to evaluate design concepts versus critical engineering metrics, can easily be applied to other MEMS development efforts. CS provides a screening mechanism for selecting design concepts to pursue further, and gives a first brush look at the fit of technology and design concepts to applications. CS was utilized in the development of a piezoelectric MEMS microphone, enabling fast iterations of assessing the fit of the technology and design concepts with various applications. Used in combination with concurrent engineering techniques, CS could speed the development of other MEMS products and increase profitability through addressing applications that best fit the technology and design.

The Avago story demonstrated a case of extending an existing technology to new applications, which is in essence a technology-driven project. In comparison, the Knowles story, discussed next, demonstrates a technology that evolved through the forces of market pull.

1.4.3 The Knowles Story

Knowles was started more than 60 years ago and has been successful in a number of product areas, including hearing aids. Knowles began their program to develop a MEMS mic as a defensive strategy to protect their hearing aid business. Dr. Pete Loeppert led the development effort, assisted by a few process engineers initially, and later by three test, design, and modeling engineers. This effort ultimately resulted in the Knowles SiSonic mic. Information for this case study was primarily obtained through an interview with Dr. Loeppert [51].

Initially the team pursued a two-piece design, where the capacitive plates were fabricated on separate wafers and later assembled together, as this was the design of

choice in the literature at the time. This approach did not provide very good results, so the team migrated to a one-piece design, fabricating both capacitive plates on the same wafer. Film stress was the largest variable in performance. As film stress is very hard to control consistently from batch to batch, performance varied widely across wafers and lots. As the main designer, Loeppert knew it was important to design a product robust to process variations such as stress. His knowledge and understanding of product design and process interactions led to a free-plate design that eliminated dependence on as-deposited film stress and reduced the effects of package stress, a critical breakthrough. Loeppert also knew to choose materials and processes that would give the mics the desired characteristics, resulting in a migration from PECVD nitride to LPCVD nitride to allow better control over the stress gradient.

The team utilized finite element modeling and crude electrostatic modeling to create designs that would prevent electrostatic collapse. The modeling served as a jumping-off point, with building and testing product the primary means of learning. Rapid prototyping led to the addition of corrugation to the backplate to reduce membrane bowing. A representative geometry is shown in Fig. 1.12.

By 1996, Knowles had achieved a working design, but it was relatively expensive and the hearing aid market was too small to justify the product and development costs. Knowles decided to switch applications from hearing aids to consumer products, first targeting laptops and eventually cellular phones. The switch in application necessitated design changes for cost reduction and process simplification so that the

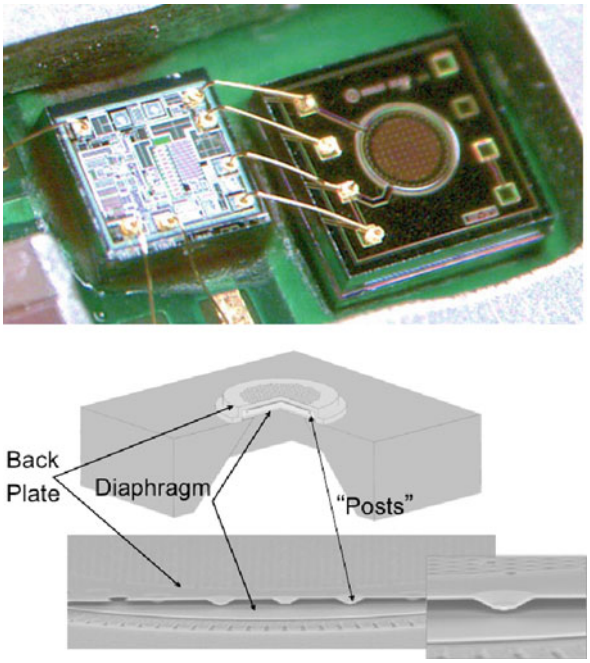


Fig. 1.12 Knowles Sisonic^{TM} Microphone packaged with signal conditioning chip and cross-section showing the floating diaphragm, antistiction posts, and back plate. Original figure, used with permission of Knowles Electronics

process could be run on standard equipment and would be easily scalable. By 1999, the team had good prototypes but struggled to find production fabrication and packaging partners. In 2002, they began working with Sony for wafer fabrication, and ultimately built their own packaging facility. In 2003, Motorola put the SiSonic in what was anticipated to be a low-volume phone platform. SiSonic sales to Motorola exceeded 30 million by 2009.

Although the Knowles team did not use design methods such as QFD and FMEA formally, they kept the fit of the technology to the market application in mind throughout the development process. As the project leader, Loeppert kept a running Pareto list of critical needs. A Pareto list is a means to determine priorities for process improvement via identifying the biggest improvement opportunities. As each opportunity is addressed, the list must be updated with the next largest improvement areas. Loeppert continuously guided the team on working down the Pareto list in much the same way as the outcomes of QFD would be used. Loeppert also kept a focus on developing the right product for the application at the right market time, rather than just building something that was technically outstanding but did not meet customer and market needs. QFD and CS can both help with this process if the team lacks the experience to maintain the focus on market application without formal methods. Loeppert suggests that all MEMS engineers obtain exposure to design and process, even if the ultimate job aspiration is one or the other. The hands-on learning provides deep understanding that enables an engineer to do a much better, more efficient job in developing new products. It is also necessary to have a balance between technical knowhow in the relevant areas and market understanding on a project team, whether those skills come together in one person or through multiple team members.

Given Knowles position at the top of the MEMS mic market and the fact that they shipped over one billion units in the first 6 years of production [52], the success of the SiSonic development project is indisputable. SiSonic provides a prime example of developing MEMS technology to fit the requirements of a specific target market. SiSonic's market dominance shows the team hit the mark.

1.4.4 Summary of Key Concepts

The design process is nonlinear and requires short loops and systematic evaluation of process and materials in parallel with transducer physics analysis and geometric design. Structured design methodologies minimize the time and resources spent on design, rigorously employing and weighting the numerous parameters and voices essential to a good design outcome. The methods find use in helping companies with patented, well-characterized, or otherwise advantageous materials or technology knowhow to evaluate new markets and applications (technology-push) and also help companies sift through a wider range of technologies and design options in pursuing a new product or market (market-pull). The rest of the chapter is devoted to advice for structuring steps of the product design process outlined in Fig. 1.3.

1.5 Materials and Process Selection

1.5.1 Materials Selection

The materials list for MEMS continues to grow, while CMOS compatible materials and silicon still comprise a large fraction of commercial products for their obvious compatibilities with electronics and attributes for micromachining. Srikar and Spearing [53] classified five materials indices to aid in materials selection. For their resonator case study these are based on attributes including mass, stiffness, inertial load, deflection, and frequency and are related to materials properties. As the design process progresses, increasing detail and quality of data are needed to accurately predict device performance, as shown in Fig. 1.13. To obtain detailed materials data, test structures fabricated in the same process as the device should be evaluated and results fed back to a design iteration.

Furthermore, materials selection plots for classes of devices and desirable materials attributes can be consulted as the design embodiment progresses. For example, micromechanical flexures are a common design element in MEMS and reliable robust flexures require large displacements at small forces and without fracture. The materials selection space may be represented thus as in Fig. 1.14. Material properties may also be affected by their processing history, such as pressure, temperature, deposition method, etchant exposure, and the like.

1.5.2 Process Selection

MEMS devices consist of primary (structural) materials and secondary (dielectric, interconnect) materials [54]. MEMS processes frequently also utilize secondary

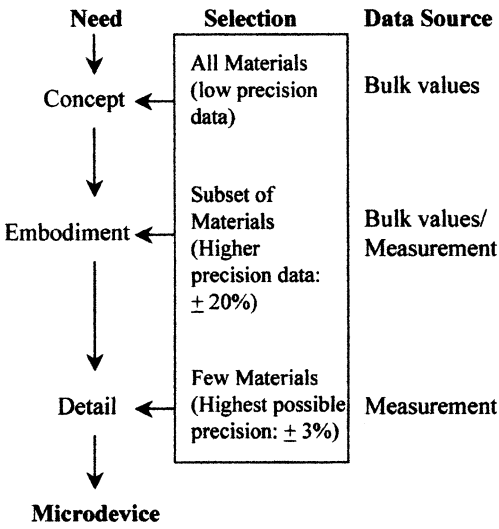


Fig. 1.13 The quality of materials data required for design increases as the design process progresses (Modified figure, used with permission of IEEE. First appearing in Srikar and Spearing [53]. Reprinted with permission. Copyright 2003 IEEE)

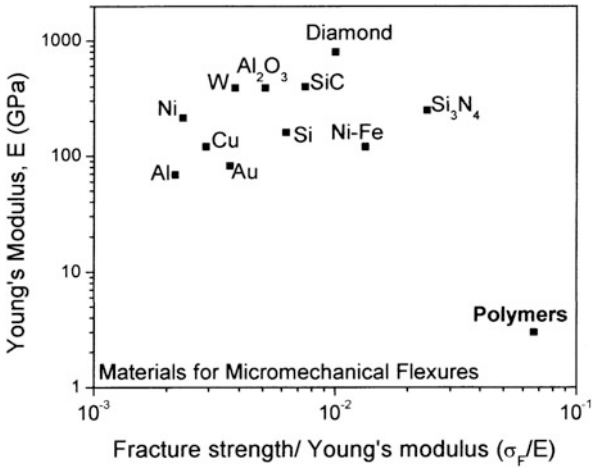


Fig. 1.14 Micromechanical flexures require a large ratio of fracture strength to Young's modulus (First appearing in Srikar and Spearing [53]. Modified figure. Reprinted with permission. Copyright 2003 IEEE)

materials (not contributing to the structure) as sacrificial materials in the fabrication flow. Attributes of concern to the design process include the material properties, net shape of the device including surface roughness and tolerances, the processing constraints on pressure, temperature, and materials interfaces/compatibilities. For example, many MEMS devices are integrated with CMOS electronics and thus are limited in their processing materials set, equipment, and temperature. Most CMOS integrated circuits (ICs) should be kept below 300°C once the IC devices are fabricated. Selecting the best process for a given geometry and material requires screening of available process capabilities, ranking of available processes, and detailed comparisons of their merits in terms of dimensional control, roughness, stress, temperature, and so on. D. J. Quinn et al. proposed a systematic classification of process chains for standard processes and materials capabilities (Table 1.1). For first-iteration concept generation, the proposed process attributes charts show achievable dimensional space for beams versus trenches as a function of process for process capabilities published as of 2006.

Quinn et al. further develop process attributes charts for tolerances achievable by the process capabilities of 2006 (Fig. 1.15). For first-order design selection of process with material, they present a case for the design space of a piezoresistive pressure sensor and treat the membrane with constraints similar to beam process capabilities in Fig. 1.15. Such process selection charts are especially helpful in guiding a designer selecting from a range of process capabilities reported in the literature versus in-house capabilities. However, the materials and process selection charts inherently assume the embodiment of the design concept is already known. A company entering a new market or a student entering a new research area will benefit from a full design cycle to generate and select the best concepts meeting customer requirements. Concept selection, discussed in Section 1.2, can guide the

Table 1.1 Process chains and capabilities

Process Chain Family		Process Chain Name	Fabrication Sequence Summary	Primary Material	Secondary Material(s)
Bulk Micromachining	Wet Etch	Anisotropic Wet Etching of (100) Si–KOH	Deposit mask material; pattern; etch; remove mask material (if desired)	Si	SiO_2, SiN
		Anisotropic Wet Etching of (110) Si–KOH	Deposit mask material; pattern; etch; remove mask material (if desired)	Si	SiO_2, SiN
		Anisotropic Wet Etching of (100) Si–TMAH	Deposit mask material; pattern; etch; remove mask material (if desired)	Si	SiO_2, SiN
		Anisotropic Etched Beam in (100) Si–KOH	Deposit mask material; pattern; underetch / release beam	SiN	Si
		Anisotropic Wet Etching of (100) Si–EDP with P++ Etch Stop	Thin wafer; boron diffuse and drive in; define mask and pattern; etch	Si	SiO_2, SiN
	Dry Etch	Anisotropic Dry Etching (RIE) of Si – Metal Mask	Deposit (electroplate) metal mask and pattern; RIE; remove mask	Si	Metal (Ni)
		Deep Etch, Shallow Diffusion Process	Deposit mask material; RIE; boron diffuse; short RIE; release OR bond to glass, thin and release	Si	Metal (Ni)
		Dissolved Wafer Process	Etch anchor recesses; boron diffuse and drive in; pattern structure; etch recess in glass; bond Si wafer to glass; thin wafer; EDP etch	Si	Glass
		SCREAM – Si (Thick Oxide Mask)	Short thermal oxidation and pattern; RIE; long (thick) thermal oxidation; RIE; thermal oxidation of sidewalls; deposit metal; deposit resist; isotropic release etch	Si	SiO_2
		SCREAM I – Si (Deposited Oxide Mask)	Deposit mask oxide and pattern; long RIE; deposit sidewall oxide; short RIE; long RIE; isotropic release etch; deposit metal	Si	SiO_2

Table 1.1 (continued)

Process Chain Family	Process Chain Name	Fabrication Sequence Summary	Primary Material	Secondary Material(s)
	SCREAM II – GaAs	Deposit nitride mask and pattern; RIE; deposit nitride layer; deposit metal; spin on resist, bake and remove; RIE exposed metal; RIE nitride; isotropic release etch	GaAs	SiN
	Deep Reactive Ion Etching (DRIE – Bosch Process)	Deposit mask and pattern; short isotropic etch (SF6); passivate sidewalls (C4F8); repeat to desired depth	Si	C_4F_8
	Trilayer Mask Dry Etch Process with Thermal Oxidation Finishing	Deposit mask layer #1 (metal); deposit mask layer #2 (resist and bake); deposit mask layer #3 (metal); pattern trilayer mask (RIE); RIE; thermal oxidize sidewalls; isotropic wet (finishing) etch of sidewalls	Si	Ni, SiO_2
Surface Micromachining	Polysilicon Surface Micromachining	Deposit isolation layer (if desired); deposit sacrificial layer (densification bake if necessary); open up anchors in sacrificial layer; deposit structural (polysilicon layer) and anneal (if necessary); pattern structure (RIE); wet isotropic release etch of sacrificial layer	PolySi	PSG, SiO_2

Table 1.1 (continued)

Process Chain Family	Process Chain Name	Fabrication Sequence Summary	Primary Material	Secondary Material(s)
	Silicon Carbide Surface Micromachining	Deposit isolation layer (if desired); deposit sacrificial layer; open up anchors in sacrificial layer; deposit structural (Silicon Carbide); pattern structure (RIE); wet isotropic release etch of sacrificial layer	SiC	Si, PSG, SiO_2
	Polyimide Surface Micromachining	Deposit isolation layer; deposit sacrificial layer; spin-on thin polyimide layer and partial cure; deposit conductor layer (if necessary); alternate spin casting and soft baking for remaining structural depth; final cure; deposit metal mask and pattern; plasma etch; isotropic release etch	Polyimide	PSG, SiO_2
	Multilayer Polysilicon Surface Micromachining (Sandia SUMMIT / SUMMIT V)	Deposit buffer/isolation layer; deposit sacrificial layer; deposit structural (polysilicon) layer; planarize using CMP; repeat to desired height up to 5 structural layers; wet isotropic release structure	PolySi	PSG, SiO_2
Soft Lithography Processes	E-beam Defined, Hard Master Mold Making (Nano-scale Molds)	Thermal oxidize layer and pattern (e-beam); RIE	Si, SiO_2	SiO_2
	Micro-contact Printing (μCP)	Ink master stamp with pattern material; transfer patter to target material (press); use pattern as etch or deposition mask (if desired)	"Inks" (polymers, SAMs etc.)	PDMS (Master Material)

Table 1.1 (continued)

Process Chain Family	Process Chain Name	Fabrication Sequence Summary	Primary Material	Secondary Material(s)
	Micro-molding in Capillaries (MMIC)	Press PDMS master mold against target substrate; insert liquid polymer via capillary action and cure; remove mold	Polymers	PDMS, SiO_2
	Micro-molding in Capillaries (MMIC) – Vacuum Assisted	Press PDMS master mold against target substrate; insert liquid polymer via vacuum action and cure; remove mold	Polymers	PDMS, SiO_2
	Micro Replica Molding (REM)	Cast and cure PDMS against hard master mold (Si, SiO_2, or SU8) and remove	PDMS	PDMS, SU8, Si (Master Material)
	Micro Transfer Molding (μTM)	Fill master PDMS mold with liquid polymer; press / pattern against substrate; remove excess polymer and cure; remove mold	Polymers	PDMS
	Hard Master Embossing / Nano-Imprint Lithography (NIL)	Deposit polymer; imprint pattern into deposited polymer and cure; complete pattern transfer with RIE; deposit metal on patterned polymer and lift off	Polymers	SiO_2
LIGA		Deposit thick resist layer (PMMA); X-Ray pattern and develop; electroplate metal and release	Metal (Ni)	PMMA

Modified figure used with permission of IEEE. First appearing in Quinn et al. [54]

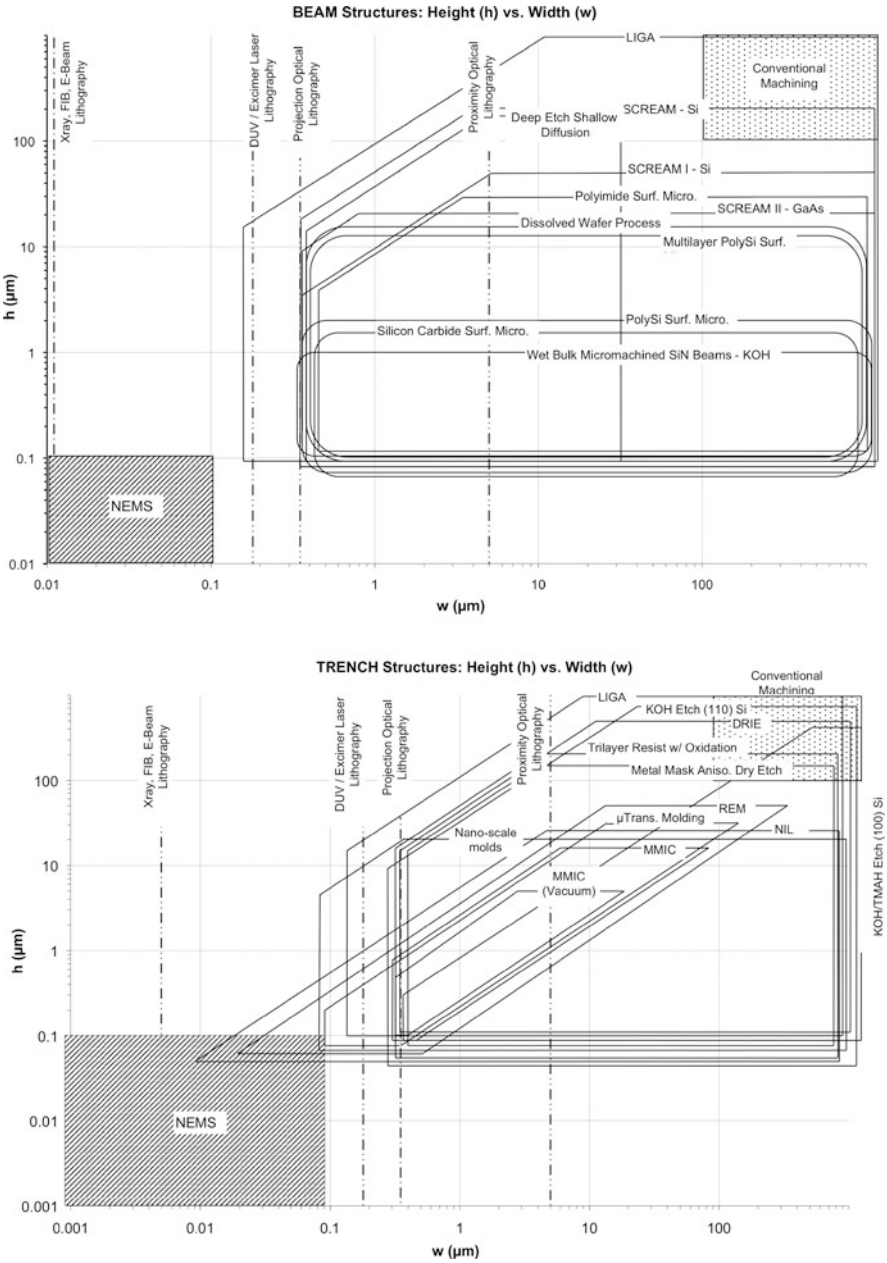


Fig. 1.15 Dimensional capabilities for beams (*top*) and trenches (*bottom*) versus process selection (Modified figure used with permission of IEEE. First appearing in Quinn et al. [54])

process of selecting a design concept, including embodiment and fabrication process. The design process should further determine if a MEMS concept is the best solution or at least is competitive with existing macroscale solutions on performance metrics.

1.6 Evaluate Concepts

1.6.1 Modeling

Much as in materials selection, the level of detail in modeling device performance increases as the design advances from a concept to embodiment as a prototype and product. Analytical models using closed-form electrical or mechanical relationships are available in most MEMS textbooks [36, 55, 56]. These models should be employed during and after brainstorming of concepts expected to meet customer requirements (this stage is based somewhat on team experience) and certainly before concept screening of the top candidates. Once a design is advanced toward prototyping plans, short loops for a more detailed analysis of materials properties and process capabilities should be undertaken. This phase may require short fabrication loops to deposit and characterize films or test structures. Finite element software such as COMSOL™ or ANSYS™ enables multiphysics coupled modeling between domains such as mechanics, electromagnetism, fluidics, and thermal. This level of prediction will enable design for baseline performance as well as local optimization iterations and sensitivity analysis via scripting. Some analysis and design software providers (e.g., Coventorware™) seek to provide a suite of tools to designers from layout to process tolerance analysis. The designer must still gather the requisite information about her process before building the model and must have materials, geometry, and a process flow in hand. A large company can build a database of their tool capabilities and process specifications for fixed process recipes.

For example, for Avago's microphone design process, the mic was modeled first by coupling thin-plate bending theory equations, taken from Timoshenko and Woinowsky-Krieger [57], with piezoelectric electromagnetic and stress–strain constitutive relations to produce an estimated potential difference across the piezoelectric membrane as a function of a uniformly applied pressure. Finite element analysis (FEA) using ANSYS with the multiphysics solver confirmed the theoretical results. Theoretical analysis provided the ability to make quick tradeoffs between a few general parameters, such as membrane size or piezoelectric film thickness, but FEA provided a more effective means for making detailed design decisions. Rapid-turn prototype manufacturing was also done simultaneously with theoretical analysis and FEA. As results of theoretical analysis and FEA became available, they were incorporated into layouts. Layout of more than one set of designs was often done simultaneously as simulation, intuition, and data offered insight into new possibilities, without waiting for full test characterization of the previous set of designs. As test data became available, they also guided design decisions. Details of the Avago modeling efforts can be found in [43, 50].

1.7 Optimization and Other Design Methods

1.7.1 Design Optimization

Once a baseline transduction mechanism, device geometry, materials, and process are known, optimization techniques are useful to determine critical parameters and combinations of parameters contributing to local optimum performance via numerical, analytical, and statistical-based simulation, design of experiments, sensitivity analysis, or Pareto optimal techniques. Such techniques can be applied to account for geometric design with tolerances related to process uncertainty and material properties uncertainty [58]. Sensitivity analyses (variability of the desired output parameter with small changes in input control parameters) in different domains have been presented with optimization performed by trading off subsets of critical parameters while other process parameters remain fixed [35, 59–64]. Design of experiments (DOE) is an alternative approach where the settings of various parameters are changed over experimental runs such that the effect of varying each parameter as well as interactions between parameters can be calculated [65]. The DOE approach requires more time spent in upfront experimental planning versus approaches that vary one parameter at a time, but the knowledge of parameter interactions gained can be crucial.

1.7.2 Uncertainty Analysis

The designer must consider the sources of uncertainty in the output parameter of the device or system [66]. Uncertainty analysis (e.g., root mean sum of square errors) can reveal the input dimensions and properties that require the most attention to mitigate their tolerance effects on performance, to measure their as-fabricated values during the process, or that require final calibration but govern linearity, repeatability, and hysteresis of the output. Manufacturability and reliability can be assessed if the critical dimensions and parameters of the design are identified and compared to available process capabilities. Parameterized wafer layouts and process maps can help determine how to adjust or compensate designs versus wafer position in a lot [67, 68].

Most optimization studies assume a priori material and process selection and look for Pareto-optimal designs, meaning designs that provide optimal results given known uncertainty distributions of material and fabrication properties and tolerances. Probabilistic methods, such as Monte Carlo simulation, have also been applied to MEMS to predict reliable operation given variability in dimensions and operating parameters [69]. Of course before this level of optimization, the designer must make materials and process selections, and potentially fabricate and test initial devices.

1.7.3 FMEA

Failure modes and effects analysis (FMEA) is a design method typically used during the development process to assess weak aspects of the design or process [70]. Those

aspects are then targeted for improvement. FMEA can also be used on products currently in production to evaluate problem areas ripe for redesign.

Of the few reports in the literature documenting design methods applied to MEMS, FMEA and optimization methods (on a settled design architecture) are the most commonly applied. In several cases FMEA has delivered substantial results on MEMS programs:

Agilent Technologies used FMEA on their FBAR products to improve yield in new products. Over several generations of technology development utilizing FMEA, typical wafer level yields rose from less than 50% to well above 50%, significantly reducing product cost [43].

Texas Instruments' use of FMEA on their digital micromirror device (DMD) is one prominent example of the application of FMEA to MEMS. Starting in approximately 1992, TI began performing FMEA on every new DMD design and each major design change. These efforts are described in several papers by M. R. Douglass [40, 41]. Using FMEA helps TI maintain good reliability and performance in addition to rapid development cycles, resulting in faster time to market with larger margins and lower risk of failures [40, 41]. Development is streamlined by identifying testing and process development needs prior to testing units. FMEA enables the development team to avoid problems later in development or in production by predicting high-risk areas to focus on early in product development. Once high-risk items have been identified, the team develops methods to test for those issues, testing to failure to explore the limits of the DMD. This method uses stress levels far in excess of product specifications to identify design weaknesses [41].

As units failed, the results were investigated to determine whether process or design changes were warranted. In some cases where changes could be made easily, modifications were implemented regardless of whether they were needed to meet product reliability specifications. According to Douglass, "These decisions resulted in further improvements to DMD robustness, resulted in large margins, and provided flexibility for tradeoffs during future development activities" [41].

For each proposed change, the product engineer coordinates gathering the appropriate inputs for the FMEA. Characterization tests are then performed. TI credits FMEA for much of the robustness, reliability, and commercial success of the DLP projection systems [41, 70, 71].

1.7.4 Design Method Timing

The MEMS designer is referred to Fig. 1.3 again to observe that the successful process is not linear but rather involves multiple iterative loops to uncover the process and material parameters particular to his facilities, the dimensional tolerances applicable to the combination of geometry, dimensions, and processes proposed, and evolving models of their relationship to overall device and system performance. Critical parameters may not be observable in the final device output, for example,

resonator performance is coupled to several geometric parameters, material properties, and packaging induced stresses and isolation ability. The designer should consider how to independently observe and account for these process variables. The overall performance of the device should include typical sensitivity and resolution specifications, but also metrics including reliability, cost, yield, and repeatability, which are difficult to predict at the outset of the design process but become more apparent through careful evaluation of test structures and process steps. The relative complexity and cost of design concepts, as well as how well concepts fit user requirements can be evaluated through structured design methodologies that will aid the designer in selecting the best concepts to carry forward through prototyping and production.

1.8 Summary

This chapter provided examples of design methods that can be applied to MEMS development programs to streamline and shorten the development process. The product development process is shown via flowchart in Fig. 1.3, highlighting the product definition steps and stakeholders. Options for both market-pull and technology-push projects are demonstrated in the figure, as well as described in the Knowles and Avago case studies, respectively. QFD Phase I and concept screening are highlighted as tools that can be readily applied to MEMS projects. These tools can help determine the most critical technical aspects of the product from a user perspective, the most viable design concepts to prototype, and the best market fit for a technology, ultimately resulting in faster time to market and increased likelihood of market success.

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References

1. C.S. Smith: Piezoresistance effect in germanium and silicon, Phys. Rev. 94, 42–49 (1954)
2. H.A. Nielsen: From Locomotives to Strain Gauges (Vantage Press, New York, NY, 1985)
3. S.C. Terry, J.H. Jerman, J.B. Angell: A gas chromatographic air analyzer fabricated on a silicon wafer, IEEE Trans. Electron Dev. ED-26, 1880–1886 (1979)
4. L.J. Hornbeck: Digital light processing and MEMS: Timely convergence for a bright future. Proceedings of SPIE, 2639, 1–21 (1995)

5. J.A. Hoerni: Planar Silicon Diodes and Transistors. Proceedings of the International Electron Devices Meeting, pp. 50–50 (1960)
6. W.G. Pfann, R.N. Thurston: Semiconducting stress transducers utilizing the transverse and shear piezoresistance effects, J. Appl. Phys. 32, 2008–2019 (1961)
7. O.N. Tufte, P.W. Chapman, D. Long: Silicon diffused-element piezoresistive diaphragms, J. Appl. Phys. 33, 3322–3327 (1962)
8. K.E. Petersen: Silicon as a mechanical material, Proc. IEEE 70, 420–457 (1982)
9. Y. Kanda: A graphical representation of the piezoresistance coefficients in silicon, IEEE Trans. Electron Dev. 29, 64–70 (1982)
10. O.N. Tufte, E.L. Stelzer: Piezoresistive properties of silicon diffused layers, J. Appl. Phys. 34, 313–318 (1963)
11. W.D. Cussins: Effects produced by the ionic bombardment of germanium, Proc. Phys. Soc. Lond. 68, 213–222 (1955)
12. B.W. Chui, T.W. Kenny, H.J. Mamin, B.D. Terris, D. Rugar: Independent detection of vertical and lateral forces with a sidewall-implanted dual-axis piezoresistive cantilever, Appl. Phys. Lett. 72, 1388–1390 (1998)
13. M. Tortonese, R.C. Barrett, C.F. Quate: Atomic resolution with an atomic force microscope using piezoresistive detection, Appl. Phys. Lett. 62, 834–836 (1993)
14. J.A. Harley, T.W. Kenny: 1/f noise considerations for the design and process optimization of piezoresistive cantilevers, J. Microelectromech. Syst. 9, 226–235 (2000)
15. K. Matsuda, K. Suzuki, K. Yamamura, Y. Kanda: Nonlinear piezoresistance effects in silicon, J. Appl. Phys. 73, 1838–1847 (1993)
16. R.J. Wilfinger, P.H. Bardell, D.S. Chhabra: The resonistor: A frequency selective device utilizing the mechanical resonance of a silicon substrate, IBM J. Res. Dev. 12, 113–118 (1968)
17. T.N. Jackson, M.A. Tischler, K.D. Wise: An electrochemical P-N junction etch-stop for the formation of silicon microstructures, IEEE Electron Dev. Lett. 2, 44–45 (1981)
18. K. Petersen, P. Barth, J. Poydock, J. Brown, J.J. Mallon, J. Bryzek: Silicon Fusion Bonding for Pressure Sensors. Proceedings of the IEEE Solid-State Sensor and Actuator Workshop (Hilton Head Island, SC), pp. 144–147 (1988)
19. L. Roylance, J. Angell: Batch-fabricated silicon accelerometer, IEEE Trans. Electron Dev. 26, 1911–1917 (1979)
20. K.-Y. Ng, J. Shajii, M.A. Schmidt: A Liquid Shear-Stress Sensor Fabricated Using Wafer Bonding Technology. Proceedings of the International Conference on Solid-State Sensors and Actuators, TRANSDUCERS'91, San Francisco, pp. 931–934 (1991)
21. J. Bardeen, W.H. Brattain: The transistor, a semi-conductor triode, Phys. Rev. 74, 230 (1948)
22. D.I. Pomerantz: Anodic Bonding, US Patent No. 3,397,278, Oct 3, 1968
23. R. Noyce: Semiconductor Device-and-Lead Structure, US Patent No. 2,981,877, April 25, 1961
24. W.F. Brinkman, D.E. Haggan, W.W. Troutman: A history of the invention of the transistor and where it will lead us, IEEE J. Solid-State Circuits 32, 1858–1865 (1997)
25. R.M. Finne, D.L. Klein: A water-amine-complexing agent system for etching silicon, J. Electrochem. Soc. 114, 965–970 (1967)
26. C.S. Fuller: Diffusion of donor and acceptor elements into germanium, Phys. Rev. 86, 136 (1952)
27. S.M. Hu: Formation of stacking faults and enhanced diffusion in the oxidation of silicon, J. Appl. Phys. 45, 1567–1573 (1974)
28. E.B. Karlsson: The Nobel Prize in Physics, In A.W. Levinovitz, N. Ringertz (Eds.): The Nobel Prize: The First 100 Years, p. 235 (World Scientific, Singapore, 2001)
29. J.S.C. Kilby: Turning potential into realities: The invention of the integrated circuit (Nobel lecture), ChemPhysChem 2, 482–489 (2001)
30. F. Laermer, A. Schilp: Method of anisotropically etching silicon, US Patent No. 6,284,198, Mar 26, 1996

31. J.B. Lasky: Wafer bonding for silicon-on-insulator technologies, Appl. Phys. Lett. 48, 78–80 (1986)
32. J.F. Marshall: Method for electrolytically etching semiconductor material, US Patent No. 4,054,497, Oct 18, 1977
33. M. Shimbo, K. Furukawa, K. Fukuda, K. Tanzawa: Silicon-to-silicon direct bonding method, J. Appl. Phys. 60, 2987–2989 (1986)
34. A.A. Barlian, W.-T. Park, J.R. Mallon Jr., A.J. Rastegar, B.L. Pruitt: Semiconductor piezoresistance for microsystems, Proc. IEEE, 97, 513–552 (2009)
35. B. Bae, B.R. Flachsbart, K. Park, M.A. Shannon: Design optimization of a piezoresistive pressure sensor considering the output signal-to-noise ratio, J. Micromech. Microeng., 14, 1597–1607 (2004)
36. S.D. Senturia: Microsystem Design, p. 720 (Springer, New York, NY, 2004)
37. N. Yazdi, F. Ayazi, K. Najafi: Micromachined inertial sensors, Proc. IEEE, 86, 1640–1659 (1998)
38. J.B. Revelle, J.W. Moran, C. Cox: The QFD Handbook (Wiley, New York, NY, 1998)
39. K. Ishii, M.V. Martin: QFD Template (Stanford University Manufacturing Modeling Lab Course Website, 2000)
40. M.R. Douglass: DMD Reliability: A MEMS Success Story. Proceedings of the Reliability, Testing, and Characterization of MEMS/MOEMS II, Bellingham, WA, (2003)
41. M.R. Douglass: Development of the Digital Micromirror Device (DMD) Microsystem. Proceedings of the Second Mechatronics and Microsystems Symposium (2005)
42. M.G. daSilva: MEMS Design for Manufacturability (DFM). Proceedings of the Sensors Expo, Rosemont, IL, (2002)
43. K.L. Lamers: Components of an Improved Design Process for Micro-Electro-Mechanical Systems, Doctoral Dissertation, Stanford University (2008)
44. Y. Akao: New product development and quality assurance – quality deployment system, Standard. Qual. Control 25, 9–14 (1972)
45. H. Nishimura: Ship design and quality table, Jpn. Union Sci. Eng. Qual. Control 23, 16–20 (1972)
46. J. Hauser, D. Clausing: The house of quality, Harv. Bus. Rev. May–June, No. 3, 63–73 (1988)
47. M.V. Martin, K. Ishii: ME 317 Design for Manufacturability Course Reader: Section 3.2. Introduction to Quality Function Deployment (2000)
48. S. Pugh: Concept Selection – A Method That Works, in Creating Innovative Products Using Total Design, pp. 167–176 (Clausing, D., Andrade, R. (Eds.) Addison-Wesley, Reading, MA, 1996)
49. T. Kelley: The Art of Innovation (Currency/Doubleday, New York, NY, 2001)
50. T.L. Lamers, R.S. Fazzio: Accelerating Development of a MEMS Piezoelectric Microphone. Proceedings of the 2007 ASME IDETC, Las Vegas, NV (2007)
51. P. Loeppert: Personal communication to Lamers, T.L., interview by Tina Lamers, Denver, CO, 6/23 (2009)
52. P. Loeppert: Personal communication to Lamers, T.L., email to Tina Lamers, 8/17 (2009)
53. V.T. Srikar, S.M. Spearing: Materials selection in micromechanical design: An application of the Ashby approach, J. Microelectromech. Syst. 12, 3–10 (2003)
54. D.J. Quinn, S.M. Spearing, M.F. Ashby, N.A. Fleck: A systematic approach to process selection in MEMS, J. Microelectromech. Syst. 15, 1039–1050 (2006)
55. G.T.A. Kovacs: Micromachined Transducers Sourcebook (McGraw-Hill, Boston, MA, 1998)
56. M.J. Madou: Fundamentals of Microfabrication: The Science of Miniaturization, 2nd ed. (CRC Press, Boca Raton, FL, 2002)
57. S. Timoshenko, S. Woinowsky-Krieger: Theory of Plates and Shells: Chapter 3, pp. 51–56 (McGraw-Hill, New York, NY, 1959)
58. M. Liu, K. Maute, D.M. Frangopol: Multi-objective design optimization of electrostatically actuated microbeam resonators with and without parameter uncertainty, Reliab. Eng. Syst. Safety 92, 1333–1343 (2007)

59. A.A. Barlian, S.-J. Park, V. Mukundan, B.L. Pruitt: Design and characterization of microfabricated piezoresistive floating element-based shear stress sensors, Sens. Act. A: Phys. 134, 77–87 (2007)
60. J.C. Doll, S.-J. Park, B.L. Pruitt: Design optimization of piezoresistive cantilevers for force sensing in air and water, J.Appl. Phys. 106, 064310 (2009)
61. J.C. Liu, S.C. Heilshorn, D.A. Tirrell: Comparative cell response to artificial extracellular matrix proteins containing the RGD and CS5 cell-binding domains, Biomacromolecules, 5, 497–504 (2004)
62. S.-J. Park, A.J. Rastegar, T.H. Fung, A.A. Barlian, J.R. Mallon, B.L. Pruitt: Optimization of piezoresistive cantilever performance. Proceedings of the Solid-State Sensors and Actuators Workshop, Hilton Head Island, SC, pp. 98–101 (2008)
63. R. Bharadwaj, J.G. Santiago, B. Mohammadi: Design and optimization of on-chip capillary electrophoresis, Electrophoresis 23, 2729–2744 (2002)
64. S. Bhardwaj, M. Sheplak, T. Nishida: Signal to noise optimization and noise considerations for piezoresistive microphones. Proceedings of the 16th International Conference on Noise in Physical Systems and 1/f Fluctuations, Gainesville, FL (2001)
65. G.E.P. Box, W.G. Hunter, J.S. Hunter: Statistics for Experimenters: An Introduction to Design, Data Analysis, and Model Building (Wiley, New York, NY, 1978)
66. J.P. Holman: Experimental Methods for Engineers, 7th ed. (McGraw-Hill, New York, NY, 2000)
67. K.O. Abrokwah, P.R. Chidambaram, D.S. Boning: Pattern based prediction for plasma etch, IEEE Trans. Semicond. Manuf. 20, 77–86 (2007)
68. D.S. Boning, J.E. Chung: Statistical metrology: Understanding spatial variation in semiconductor manufacturing. Proceedings of the SPIE Symposium on Microelectronic Manufacturing, Microelectronic Manufacturing Yield, Reliability, and Failure Analysis II, Austin, TX (1996)
69. S. Reh, P. Lethbridge, D.F. Ostergaard: Quality based design and design for reliability of micro electro mechanical systems (MEMS) using probabilistic methods. Proceedings of the International Conference on Modeling and Simulation of Microsystems, San Diego, CA, pp. 708–711 (2000)
70. P. Palady: Failure Modes and Effects Analysis, Author's Edition, 2nd ed. (Pal Publications, Pottstown, PA, 1998)
71. R.E. McDermott, R.J. Mikulak, M.R. Beauregard: The Basics of FMEA (Productivity Press, NY, NY, 1996)

Chapter 2
Additive Processes for Semiconductors and Dielectric Materials

Christian A. Zorman, Robert C. Roberts, and Li Chen

Abstract This chapter presents an overview of the key methods and process recipes commonly employed in the deposition of semiconductor and dielectric thin films used in the fabrication of microelectromechanical systems (MEMS). These methods include chemical vapor deposition, epitaxy, physical vapor deposition, atomic layer deposition, and spin-on techniques. The materials featured in this chapter include silicon and its oxide, nitride, and carbide derivatives, silicon–germanium, diamond and diamondlike carbon, III-V semiconductors, aluminum oxide, and other notable semiconductor and dielectric materials used as structural, sacrificial, and passivation layers. The process recipes presented in this chapter largely come from publications that report not only processing details, but also key material properties of importance to MEMS that result from the reported processes. Whenever possible, the references included in this chapter are papers that are readily available via commonly used electronic databases such as IEEE Xplore™ and ScienceDirect™ so as to aid the reader in gathering more detailed information than can be practically presented herein. Furthermore, the processes selected for inclusion in this chapter were, for the most part, successfully used in the fabrication of MEMS structures or components, thus verifying their utility in MEMS technology. For select materials, case studies are included to provide process-related details that cannot easily be tabulated but are nonetheless of critical importance to successful usage of the process.

2.1 Overview

Semiconductors and dielectrics constitute the two most heavily utilized material classes in the MEMS fabrication toolset owing in large measure to the key properties of these materials. The rapid development of MEMS technology during the late

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1980s and throughout the 1990s can be attributed to the ability to leverage heavily the expertise, know-how, and physical infrastructure developed for silicon and its oxide and nitride derivatives for the silicon IC industry. And although MEMS continues to benefit from advancements in processing technologies made for the silicon IC industry, MEMS also benefits from the emergence of new semiconductors and dielectric materials that are being developed for application areas that are not compatible with silicon as the principle material.

This chapter focuses on additive processes for semiconductor and dielectric materials for MEMS. These materials include those commonly used in the IC industry such as polysilicon, silicon dioxide, silicon nitride, and silicon–germanium, as well as other semiconductors, such as gallium arsenide, indium phosphide, and silicon carbide. Newly emerging semiconductors such as diamond and gallium nitride are also included, as well as dielectrics such as aluminum oxide. Like most thin films, some of the key properties of these materials are linked to the methods and specific recipes used to create the thin films. The principle purposes of this chapter are threefold: (1) to provide an overview of the common semiconductors and dielectrics used in MEMS technology, (2) to examine the methods used to deposit thin films of these materials, and (3) to provide an in-depth review of actual process recipes used to deposit the films and the key MEMS-centric material properties that result from proper execution of these recipes.

The chapter is organized by deposition technique and for each technique, by material. Each section is constructed around a set of data tables that contain key processing parameters along with associated material properties. The chapter is constructed in this manner to give the reader the ability to quickly perform side-by-side comparisons between recipes and resulting properties. As stated previously, the references used in this chapter are widely available in common electronic databases so that the reader can further investigate promising recipes by referring directly to the published work. This approach enables inclusion of a much larger body of information than can be accommodated with the summary-based approaches used in most reviews. For quick reference, Table 2.1 lists the materials and the deposition techniques described in detail in this chapter.

2.2 Thermal Conversion

This section presents an overview of the most common thermal conversion process used in the fabrication of MEMS devices: thermal oxidation of silicon, and describes general aspects of thermal oxidation of silicon, specific methods used in thermal oxidation, specific oxidation recipes, important material properties that result from these recipes, and some unconventional, MEMS-centric applications of thermal oxidation.

2.2.1 Process Overview

Silicon's position as the dominant semiconductor in modern IC technology can, in large part, be attributed to the passivating oxide that can be readily formed on its

Table 2.1 Additive processes used to deposit semiconductor and dielectric films used in MEMS fabrication as detailed in this chapter

Material	Thermal conversion	LPCVD	APCVD	PECVD	Epitaxy	PVD	ALD/ ALE	Spin cast
Silicon		X		X	X	X		
Silicon dioxide	X	X		X		X		X
Silicon nitride		X		X				
Silicon–germanium		X		X				
Germanium		X						
Silicon carbide		X	X	X	X	X	X	
Diamond		X						
Carbon/DLC[a]				X		X		
Gallium arsenide					X			
Indium phosphide					X			
Ternary III-V					X			
Gallium nitride					X			
Aluminum oxide							X	
Zinc oxide							X	

[a]DLC = Diamondlike carbon

surface. Commonly referred to by process engineers as "silicon oxide" this material is technically "silicon dioxide" in chemical composition. Silicon dioxide (SiO_2) naturally forms on the surface of Si by a process known as oxidation. Oxidation is a thermally driven conversion process that occurs over a very wide range of temperatures, including ambient conditions. If grown at room temperature, the material is known as a "native oxide" and has a thickness of roughly 1–2 nm. For MEMS applications, much thicker oxides (hundreds of nm to several microns) are typically required, necessitating the need for processing tools to produce such films. Of all the thin-film growth processes used in MEMS, oxidation of silicon is one of the most straightforward owing to the simplicity of the process. Known as thermal oxidation, the key ingredients aside from the silicon substrate itself are elevated temperature and a gaseous oxidant. Although a thin oxide can be formed on silicon under ambient conditions, oxides with thicknesses of relevance to MEMS (i.e., > several hundred nm) require temperatures of around 1000°C to be grown in a reasonable amount of time. Thermal oxidation is primarily performed at atmospheric pressure in an oxidizing environment that can be comprised of O_2, a mix of O_2 and H_2, or water vapor. Oxidation in O_2 is referred to as "dry oxidation" whereas oxidation in water vapor or mixtures of O_2 and H_2 is known as "wet oxidation."

Without question, thermal oxidation of silicon is the most thoroughly studied and well understood of all the film growth processes used in MEMS due to its critical importance in IC processing. From an engineering perspective, the most common and useful model to describe the oxidation process is known as the Deal–Grove model for thermal oxidation. This model describes the process in terms of several

fluxes, namely: (1) flux of oxidants from the main gas flow regime of the oxidation furnace to the substrate surface, (2) flux of oxidants through a pre-existing oxide to the oxide/Si interface, and (3) flux that describes the chemical conversion process. Oxidation reactors, commonly called furnaces, are operated in steady-state mode, meaning that key processing parameters such as temperature and oxidant flow rates are held constant with respect to time once the process is initiated. Steady-state considerations require that the three fluxes be equal, therefore the lowest flux will ultimately determine the oxidation rate. Reactors are constructed and operated in such a way that the flux of oxidants through the gaseous environment is not the rate-limiting flux, allowing the oxidation rate to be determined by the remaining two fluxes. The flux of oxidants through the pre-existing oxide is governed by the diffusion properties of the oxidant in SiO_2 whereas the flux at the oxide/Si interface is governed by reaction kinetics. Both fluxes are temperature dependent, increase with increasing temperature, and depend on the properties of the oxidant. The Deal–Grove model handles both the diffusion characteristics and kinematic properties of the process by assuming that the relevant first-order information for a particular oxidation process can be adequately quantified in terms of proportionality constants. As such, the diffusion properties of an oxidant in SiO_2 are described by its diffusivity, and information about the interfacial reactions of the oxidant with Si is represented by a constant known as the interface reaction rate constant. Equations (2.1) and (2.2) represent mathematical expressions for the fluxes associated with oxidant diffusion through the oxide and the interfacial reactions, respectively.

$$F_{\text{diffusion}} = D(C_0 - C_{\text{I}})/x_0 \tag{2.1}$$

$$F_{\text{reaction}} = k_{\text{i}} C_E \tag{2.2}$$

where C_0 is the oxidant concentration at the surface, C_{I} is the oxidant concentration at the SiO_2/Si interface, D is the diffusivity of oxidant in SiO_2, x_0 is the thickness of the resulting oxide and k_{i} is the interface reaction rate constant.

From a processing perspective, Equations (2.1) and (2.2) are not very useful in determining the final oxide thickness because it is difficult to quantify the oxidant concentrations at the SiO_2 surface and at the oxide/Si interface. However, further mathematical analysis yields an expression for the final oxide thickness that utilizes input parameters that have been determined from empirically derived data. Equation (2.3), known as the linear parabolic growth law, expresses oxide thickness in terms of oxidation time.

$$x_0^2/B + x_0/(B/A) = t + \tau \tag{2.3}$$

where t is the oxidation time and τ is given by the following expression,

$$\tau = (x_{\text{i}}^2 + Ax_i)/B \tag{2.4}$$

where x_{i} is the initial oxide thickness and x_0 is the final oxide thickness.

In Equation (2.3), B is known as the parabolic rate constant and is proportional to the diffusivity constant, whereas B/A is known as the linear rate constant and is proportional to the interface reaction rate constant. For thermal oxidation of Si, both the linear and parabolic rate constants B/A and B have been determined from empirical data and are readily available to the process engineer. As expected, these parameters exhibit a strong temperature dependence as shown in Equations (2.5) and (2.6) below.

$$B = C_1 \exp(-E_1/kT) \tag{2.5}$$

$$B/A = C_2 \exp(-E_2/kT) \tag{2.6}$$

where C_1 and C_2 are constants and E_1 and E_2 are activation energies. In these expressions, the constants and activation energies are readily available, enabling simple calculation of the linear and parabolic rate constants, and therefore a straightforward calculation of either oxidation time or oxide thickness.

As mentioned previously, the parabolic rate constant is proportional to diffusivity and the linear rate constant is proportional to the interfacial reaction rate constant. Consequently, the parabolic rate constant will depend on the oxidant and the linear rate constant will depend both on the oxidant and the crystalline orientation of the Si substrate. As such, the parameters needed to calculate these constants using Equations (2.5) and (2.6) have been determined for each oxidation process (dry, wet, and steam) as well as crystal orientation. In the case of the linear rate constant (B/A), it has been found that the relationship between this constant and the three technically relevant crystal orientations of Si is as follows:

$$(B/A)_{111} = 1.68(B/A)_{100} \tag{2.7}$$

$$(B/A)_{110} = 1.45(B/A)_{100} \tag{2.8}$$

A detailed description of the oxidation process, including a thorough development of the Deal–Grove model, as well as the data required to calculate oxidation times and thicknesses can be found in nearly any advanced undergraduate or graduate text on silicon VLSI fabrication technology, including two notable texts commonly used by MEMS process engineers [1–3].

Figure 2.1 is a schematic diagram of a standard oxidation furnace. The furnace consists of a long cylindrical fused quartz tube sized in length and diameter to hold large numbers (sometimes > 100), large diameter (i.e., 200 mm) Si wafers. Thermal oxidation is a conversion process using a gaseous source as the oxidant, so wafers can be loaded in a close packed configuration, with separation distances of a few millimeters being very common. The quartz tube is jacketed by a resistive heater that can reach temperatures in excess of 1200°C. The process is performed at atmospheric pressure and therefore vacuum sealing is not required. When not in use, the furnace is idled at a low temperature (600–800°C) and continuously flushed with an inert gas such as nitrogen. During operation, the inert gas is displaced by the oxidant, thus no vacuum pumping system is used. A gas manifold equipped with mass

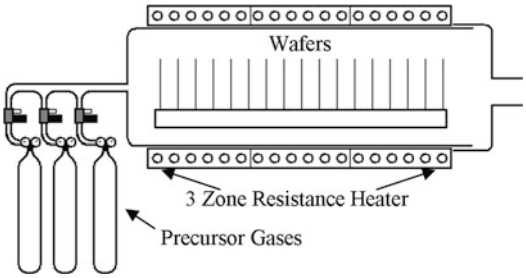

Fig. 2.1 Schematic diagram of a typical oxidation furnace

flow controllers is used to supply the furnace with the proper flow rates and relative concentrations of oxidant gas species.

The typical thermal oxidation process begins with a thorough cleaning of the Si wafers. The standard cleaning process is known as the RCA clean. The main purpose of the RCA clean is to ensure that any organic, ionic, and metallic contaminants are removed from the wafers prior to high-temperature processing. The process, detailed in Table 2.2, consists of a series of aqueous chemical baths into which the wafers are immersed for a prescribed length of time. Each bath is designated to remove a particular class of contaminants, and all aqueous processing, including rinses, is performed in deionized water. At the conclusion of the process, the wafer surfaces meet the cleanliness standards of CMOS processing. Although MEMS structures are generally not as sensitive as MOS transistors to such contamination, performing an RCA clean prior to each oxidation ensures that cross-contamination is kept to an absolute minimum.

Table 2.2 The RCA cleaning process[a]

Process step	Purpose	Details
RCA-1	Removed organics and metals	500 ml NH_4OH (29%) 500 ml H_2O_2 (30%) 2.7 l DI water 15 min at 70°C
HF Dip	Removes oxide formed during RCA-1	5 l DI water 100 ml HF (49%) 30 s
RCA-2	Removes alkali ions and cations	500 ml HCl (32–38%) 500 ml H_2O_2 (30%) 2.7 l DI water 15 min at 70°C

[a]Used in the Microfabrication Laboratory at Case Western Reserve University. The process is designed for a single batch of 25, 100 mm-diameter wafers.
1. Each step of the process is followed by a rinse in deionized water
2. After the final rinse, the wafers are spin–rinse dried
3. If necessary, a piranha clean is performed prior to RCA-1 in order to remove excessive organic and/or metallic contaminants

Once the wafers have been cleaned, they are ready for loading into the oxidation furnace. Once loaded, the furnace temperature is ramped up from its idle setpoint to the designated oxidation temperature, and the inert purge gas is displaced by the gaseous oxidant. The oxidation process proceeds under steady-state conditions until the desired oxide film is grown, after which the oxidant is displaced by the inert purge gas and the furnace temperature is ramped to its idle state.

2.2.2 Material Properties and Process Selection Guide for Thermal Oxidation of Silicon

Because the thermal conversion process occurs at the buried oxide/Si interface, thermal oxidation is inherently a diffusion-driven, self-limiting process. As a result, the maximum practical oxide thickness that can be obtained is about 2 μm. At this thickness, thermal oxides can be used for a wide range of applications, including masks for selective-area doping, etch masks for silicon bulk micromachining, and sacrificial layers for polysilicon and silicon carbide surface micromachining. Unlike other materials commonly used in MEMS, thermal SiO_2 films can only be grown on silicon substrates, thereby limiting their applicability in multilayered structures. That being said, thermal oxidation is not restricted to single crystalline Si wafers, but can also be performed to produce SiO_2 on polysilicon films, for as long as the materials beneath the polysilicon layer can tolerate the high temperatures associated with the oxidation process. Thermal oxides can also be grown on silicon carbide substrates, albeit at a much lower rate than for silicon [4].

At a given temperature, wet and steam oxidation rates are higher than dry oxidation rates, an effect that has been attributed to higher oxidant solubilities (i.e., H_2O) in SiO_2 than O_2. As such, thick oxides, such as would be required for masks used in dopant diffusion or solution-based bulk micromachining, are generally grown using wet or steam oxidation processes. Dry oxidation, on the other hand, is typically used to form the gate oxide in MOS transistors owing to its better electrical properties, but can be used in any application that does not require thick oxides (>500 nm).

Table 2.3 details the key thermal oxidation processes performed in the Microfabrication Laboratory at CWRU and is provided here to give the reader a sense of how process parameters such as gas flow relate to furnace size. As with many other MEMS fabrication facilities, oxidation is performed in commercially available, high-thoroughput systems. Due at least in part to the simplicity of the oxidation process, most commercial systems operate in much the same manner, and any significant process differences are likely due to scaling issues associated with differences in reactor geometry. For reference purposes, the system at CWRU is an MRL Industries™ Model 1118 which accommodates a 1.93 m long, 235 mm diameter quartz tube.

Thermal oxides have many properties that are attractive to silicon-based ICs and MEMS [1]. Thermal SiO_2 has a resistivity between 10^{14} and 10^{15} Ω cm, a dielectric strength of 5×10^6 V/cm and a dielectric constant of 3.9, making it exceptionally

Table 2.3 Thermal oxidation processes performed in the MRL industries™ model 1118 system at CWRU[a]

Type	Temp (°C)	Source gases	Flow rates	Growth time	Thickness (nm)
Dry oxidation	1050	O_2	6 slm	30 min	20
				1 h, 30 min	130
				3 h, 40 min	200
Wet oxidation	1075	O_2	6 slm	25 min	300
		H_2	10 slm	1 h, 35 min	500
				3 h, 55 min	1000
				10 h	2000

[a]The furnace idle temperature is 800°C. Typical ramp up and ramp down times are 60 and 90 min, respectively

well suited for electrical isolation, especially for electrostatically actuated devices. Silicon dioxide has an extremely high melting point (1700°C) and a low thermal conductivity (0.014 W/cm °C), especially when compared with Si. The etch rate in buffered HF (commonly used when photoresists are used as etch masks) is nominally 100 nm/min. As with every electrical insulator, SiO_2 has a large electronic bandgap at 9 eV and low electron mobilities (20–40 cm^2/Vs). The mass density of thermal oxide is 2.27 g/cm^3.

Thermal oxide has a thermal expansion coefficient of $5 \times 10^{-10}/°C$, which when compared to Si leads to a significant buildup of residual stress when oxidized silicon substrates are cooled to room temperature. Table 2.4 summarizes published data regarding the mechanical properties in wet thermal oxides. In both cases, the stress is moderately compressive. This level of stress would be more than sufficient to induce measurable bow in the Si wafer substrates; however, the typical oxide furnace configuration enables simultaneous oxide growth on both sides of each wafer, thereby negating the effect, especially when double-side polished wafers are used. In many MEMS applications, stress in thermal oxides is of secondary concern because the films are used as sacrificial layers or are patterned into small isolated structures.

Table 2.4 Residual stress in thermal SiO_2 films

References	Temp (°C)	Source gases	Thickness (μm)	Residual stress (MPa)	Plain strain modulus (GPa)	Fracture stress (GPa)
[5]	1000	O_2/H_2	433	–331		
[6]	950–1050	O_2/H_2	0.5–1	–258	49	0.89

2.2.3 Case Studies

By virtue of the fundamental nature of the thermal conversion process, there is very little process-dependent variation in the physical properties of thermal oxide films. Likewise a high degree of standardization in the industry has led most fabrication facilities to use very similar processes. As such, interesting case studies involving thermal oxide films don't involve links between specific process parameters and measured film properties, but rather creative ways to utilize thermal oxides as sacrificial layers to create Si structures that would otherwise be difficult to fabricate using conventional etching techniques. For example, Desai et al. described a process to fabricate silicon nanoporous membranes using a thermal oxide as a sacrificial material for pore formation [7]. The process involves the growth of a thin (20–100 nm) thermal oxide on a boron-doped Si substrate that is photolithographically patterned and etched to form an array of vias. The oxide grows uniformly on all exposed Si surfaces, including the vertical sidewalls of the vias. A boron-doped polysilicon film is then deposited onto the oxidized substrate, completely filling the vias and encasing the thermal oxide. The polysilicon is patterned to allow access to the thin oxide on the sidewalls of the vias. A freestanding single crystalline/polycrystalline membrane is then fabricated by selectively removing the Si substrate from the backside up to the boron-doped region. Nanopores are then fabricated in the membrane by etching the thin, vertically oriented thermal oxide in HF. Use of thermal SiO_2, the ability to grow a uniform oxide on vertically oriented Si surfaces by thermal oxidation, and the ability to control the oxide thickness by proper selection of temperature and oxidation time enables the fabrication of highly uniform (± 1 nm) nanopores using conventional microscale fabrication techniques.

2.3 Chemical Vapor Deposition

Section 2.3 reviews the use of chemical vapor deposition as an additive process for semiconductors and dielectrics in MEMS. This section begins with an overview of a generic chemical vapor deposition process and is followed by a detailed description of specific CVD methods commonly used in MEMS fabrication. This section continues by describing specific semiconductor and dielectric materials deposited by CVD, including specific deposition recipes and important material properties that result from these recipes. Where appropriate, case studies that illustrate key aspects of the CVD films are included.

2.3.1 Process Overviews

2.3.1.1 Introduction

Chemical vapor deposition (CVD) is the most widely employed means to deposit semiconductor and dielectric materials used in MEMS. In a general sense, CVD

is a process where a thin film is formed by the deposition of vapor-phase components onto a heated substrate. The vapor is comprised of gases that contain the constituents of the thin film. These source or precursor gases are introduced into the CVD reactor in a regulated manner so as to control the gas mixture and deposition pressure. Process parameters such as gas flow, reactor pressure, and substrate temperature are highly regulated so that the precursors dissociate into the proper reactive components such that the desired material is formed on the substrate surface and not in the vapor, because vapor-phase reactions could lead to unwanted particulate contamination of the substrate surface and pinholing in the films.

CVD has several key characteristics that make it the dominant deposition method for semiconductors and dielectrics in MEMS. For silicon and its derivatives, high-quality precursors that will readily dissociate into reactants at reasonable temperatures are commercially available. In most cases, the precursors are in the gas phase at room temperature, making delivery to the reactor and flow control relatively simple. In some cases, the precursors are in the liquid phase at room temperature. In these instances, an inert gas such as nitrogen, or a reactive gas such as hydrogen, can be used as a carrier gas to deliver precursor vapor to the reaction chamber. In many cases, the gaseous precursors are diluted in a carrier gas at the source to enable safe storage. Along similar lines, precursor gases for conductivity modification, commonly known as doping gases, are readily available, enabling in situ doping of the as-deposited films. The CVD process, by its very nature, lends itself well to implementation in large-scale reactors. Commercial low-pressure CVD systems, for instance, can typically accommodate loads in excess of 50 wafers, with wafer diameters up to 200 mm. These attributes form the basis for the claim that MEMS benefits from batch fabrication.

The CVD processes used to produce semiconductors and dielectrics in MEMS are, for the most part, those developed originally for the integrated circuit industry or are close variations of such processes. The general CVD process involves the following key steps: (1) transport of precursors to the substrate surface; (2) surface processes that include adsorption of precursors, dissociation of precursors into reactants, migration of reactants to reaction sites, and reactions; and (3) desorption of reaction byproducts from the substrate surface. An explicit mathematical treatment of the CVD process in terms of these steps would be unnecessarily complex for most applications. Fortunately a much less complex, but no less accurate method to quantify the process has been developed.

Known as the Deal–Grove model for CVD growth, this model views CVD growth in terms of two fluxes, namely: a flux of reactants through the boundary layer to the substrate surface, and a flux of reactants involved in film-forming reactions. The first flux is proportional to the difference in reactant concentration across the boundary layer by a proportionality constant known as the mass transfer coefficient. The second flux is also linear to first order with respect to the concentration of reactants at the surface by a constant known as the reaction rate coefficient. Under steady-state conditions (i.e., normal reactor operating conditions) the two fluxes are equal. As such, the lower flux will necessarily govern the process.

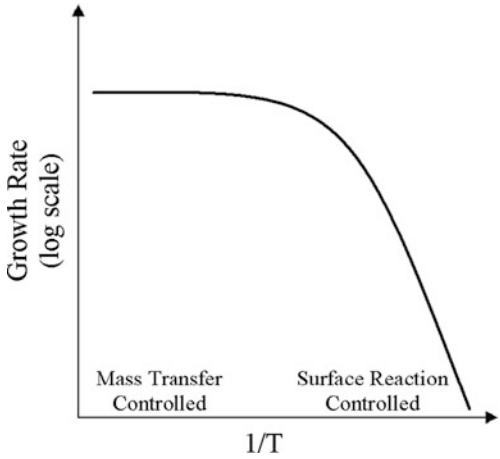

Fig. 2.2 Growth rate versus inverse temperature for a typical CVD process

Figure 2.2 presents an Arrhenius plot of growth rate versus inverse temperature for a representative CVD process.

The process can be divided into two distinct regions based on temperature. At relatively high temperatures, the process is in the mass transfer controlled regime and the process is governed by the flux of reactants through the boundary layer. The boundary layer thickness is generally held constant by way of well-controlled reactor geometries, therefore the growth rate varies relatively slowly with increasing temperature because the mass transfer coefficient is relatively constant with temperature over the temperature range of relevance for CVD. At moderate temperatures, both fluxes influence the deposition rate and thus control of the process is challenging. At relatively low temperatures, the process is described as being in the reaction controlled regime and surface reactions govern the process. In this regime, the growth rate is much more sensitive to temperature because the reaction processes are highly sensitive to temperature. CVD process recipes are generally designed to operate well within either the mass transport controlled regime or the reaction controlled regime as determined primarily by the temperature range required to produce the desired film. Arguably the best example to illustrate this point is the deposition of silicon films. If a single crystalline film is desired, a high-deposition temperature is necessary to initiate epitaxial growth (see Section 2.4 for details) and thus a CVD process in the mass transfer controlled regime is selected. Likewise, deposition of polysilicon requires a much lower substrate temperature; therefore a process in the reaction controlled regime is selected.

2.3.1.2 Low Pressure Chemical Vapor Deposition

Figure 2.3 is a schematic diagram of a typical LPCVD reactor used in MEMS fabrication. The reactor consists of a long, horizontal fused quartz reactor tube sized in length and diameter to accommodate large numbers (~50) of large-area (i.e.,

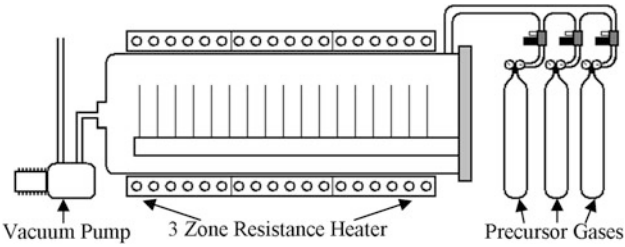

Fig. 2.3 Schematic diagram of a typical large-scale horizontal LPCVD system

200 mm dia.) silicon substrates. End caps with vacuum seals are mounted on each end of the reactor tube to enable operation in the tens to hundreds of mtorr range. The end caps are sometimes water cooled to ensure viable sealing to elastomer o-rings. The contents of the reactor are heated to temperatures up to 1000°C by a large resistive heater that envelops the reactor tube. Precursor gases are introduced via a gas manifold connected to at least one of the end caps. The manifold contains mass flow controllers and associated isolation valves for each precursor gas. The mass flow controllers are calibrated for a specific gas so as to enable precise control of gas flow, which translates to partial pressure of that species in the reactor. Typical flow rates are in standard cc/min (sccm). In addition to the precursor gases, the manifold will also have mass flow controllers for any desired doping gases, inert purge gases, and carrier gases. The process gases may be introduced through a simple port at the end cap or through injector tubes attached to flanges on the end caps that serve to distribute the gases evenly throughout the reactor tube. As mentioned previously, vapors from liquid precursors can be introduced into the reactor by passing the appropriate carrier gas through the source bottle. To maintain the desired deposition pressure, a vacuum system is attached to the end cap opposite the gas injection flanges. The typical vacuum system consists of a large, high-throughput rotary vane pump often assisted by a large roots blower and attached to an end cap through a vacuum line that contains both a pressure control valve and a vacuum isolation valve. The exhaust from the rotary vane pump is fed via a vacuum line to a gas conditioning system which treats the exhaust gas so that it may be safely released.

In general, operation of the aforementioned reactor (commonly called a "furnace" due to its high operating temperatures) follows a procedure that is fairly common for nearly all materials deposited by LPCVD. Prior to loading the furnace, the wafers are cleaned using the standard RCA cleaning procedure described previously. If the wafers have an oxide coating on them, the HF dips in the RCA process are eliminated. Likewise, if the wafers have been metalized, the RCA clean will also be omitted. After cleaning, the wafers are immediately loaded into the furnace by carefully placing them into holders called "wafer boats". Wafer boats are designed to hold the wafers upright and in close proximity to each other so as to maximize the furnace load. The spacing between wafers can be as small as several millimeters. Maintaining uniform deposition with such small spacing between wafers is possible because of the large mean-free path between molecular collisions

at the deposition pressures typically used, which results in a significant increase in diffusivity of precursors with the reactor. The boundary layer thickness increases with decreasing pressure; however, the effect is not nearly as pronounced as the increase in diffusivity. The mass transfer coefficient is proportional to the ratio of gas diffusivity to boundary layer thickness; therefore, decreasing the deposition pressure serves to increase the mass transfer coefficient, thus enabling uniform deposition.

LPCVD processes are typically performed at temperatures between 400 and 900°C in part because it is in this temperature range that good vacuum sealing can be maintained in the large-volume furnaces. One notable exception is epitaxy, where vacuum sealing is maintained for systems operating at temperatures in excess of 1500°C, but these systems are smaller in scale so that the vacuum seals can be kept cool. In the 400–900°C temperature range, the LPCVD furnace operates in the surface reaction controlled regime. In this regime, even small changes in temperature can have a measurable effect on deposition rate (see Fig. 2.2). Fortunately, large-scale furnaces have very large thermal masses, making it relatively easy to hold the reactor at a fixed temperature during film deposition. Operation at these temperatures typically translates to lower surface mobilities for reactant atoms as compared with epitaxial growth temperatures. This tends to promote three-dimensional film growth as a result of nucleation of adsorbed reactants, leading to the formation of amorphous and polycrystalline films. Fortunately, these films have properties needed for a wide range of MEMS devices, therefore eliminating the need for single crystalline films which are much more challenging to deposit.

Maintaining steady-state conditions in large-scale LPCVD reactors is critically important but fortunately relatively easy to achieve. Once the reactor is loaded and has reached the deposition temperature, precursor and doping gases (if desired) are introduced into the reactor at their prescribed flow rates through mass flow controllers that maintain constant flow. Proper vacuum pressure is maintained by adjusting the pressure control valve of the vacuum system. This valve adjusts the conductance in the vacuum line which effectively modulates the gas throughput in the reactor. For a fixed input flow and vacuum system pumping speed, decreasing the conductance leads to an increase in reactor pressure and vice versa. Rarely is input gas flow used as the primary means to control reactor pressure; however, absolute flow rates usually have to be adjusted with respect to the pumping speed of the vacuum system so as to achieve the desired chamber pressure.

For a typical deposition run, temperature, flow rates, and reactor pressure are held constant until the desired film is deposited, after which the gas flows are stopped, the reactor is cooled, and wafers unloaded. Although in principle multiple materials (i.e., polysilicon and silicon nitride) could be deposited using a single reactor, standard practice is to dedicate a reactor to a particular material, if not a particular recipe. This is because LPCVD reactors require "seasoning" in order to produce films with very low run-to-run variation in film properties. Seasoning typically involves the formation of a coating on the interior components of the reaction chamber. The coating, which typically consists of the same material as the deposited film, affects the thermal characteristics of the furnace tube. The coating can also affect the size

of the gas inlet orifices. For any given furnace, there typically is an optimum thickness range for this coating, below which the properties of the as-deposited film vary significantly between runs as well as location in the furnace and above which the coating becomes too thick to withstand thermal and mechanical shock and begins to crack and delaminate, resulting in particulate contaminants in the chamber. Limiting furnace use to a single material and thus restricting the coating to a single material, the thickness range for the coating can usually be extended, thus increasing reactor throughput.

Throughput issues aside, coating composition can affect the properties of the as-deposited film by a process known as autodoping. A form of cross-contamination, autodoping occurs when chemical impurities associated with reactor components are vaporized and incorporated into the deposited film. Autodoping is not a significant factor when a furnace is used to deposit a single material, inasmuch as the source and the deposited film are of the same chemical composition. The same may not be true for a furnace used to deposit multiple materials. Autodoping is even a risk in reactors equipped to deposit intentionally doped films. In the case of polysilicon, fabrication facilities interested in minimizing the risk of autodoping will have dedicated furnaces for both doped and undoped polysilicon.

2.3.1.3 Plasma-Enhanced Chemical Vapor Deposition

Figure 2.4 is a schematic diagram of a typical PECVD reactor. Like its LPCVD counterpart, a PECVD reactor consists of a vacuum chamber, vacuum pumping system, and gas manifold. The gas manifold differs very little, if at all, from the systems used in LPCVD reactors except perhaps for the gases to be used. Both liquid and gaseous precursors are used in PECVD processes. In large part, PECVD systems are used to deposit dielectric films such as silicon oxide and silicon nitride; however, amorphous and polycrystalline semiconductors like silicon can also be deposited. In these cases, doping gases are used to modify conductivity. The vacuum pumping system also closely resembles the LPCVD system, consisting of vacuum valving, gauging, a roots blower, and mechanical rotary pump, and are operated in the same manner.

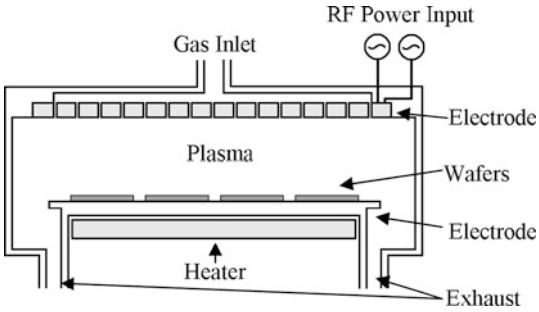

Fig. 2.4 Schematic diagram of a typical PECVD system

The main distinguishing features of the PECVD system can be found inside the vacuum vessel. Unlike the typical LPCVD system, the common PECVD reactor utilizes a stainless steel containment vessel. This is because sample heating is performed by an internal resistive heater that is connected directly to the substrate mounting stage, as opposed to LPCVD which uses an externally mounted resistive heating element. With this configuration, thermal conductivity and thermal mass issues associated with the vacuum vessel are much less a factor and thus stainless steel can be used. In addition to the heater, the vacuum vessel contains two large-area electrodes that are used to generate a plasma inside the chamber. The plasma is generated by connecting the substrate mounting stage to ground and the other electrode to an RF power supply. The RF power supply typically functions at 13.56 MHz and enables the formation of the high electric field required of the plasma.

The plasma is comprised of free electrons, energetic ions, neutral molecules, free radicals, and other ionized and neutral molecular fragments that originate from the precursor gases which are fed at prescribed flow rates from the manifold into the vacuum vessel. In the plasma, high-energy electrons interact kinetically with the precursor gases, causing them to dissociate into the aforementioned components. A film is formed on the wafer as these components are adsorbed on the surface. As with any successful CVD process, these adsorbates migrate to reaction sites where they undergo chemical reactions with other species to form a film. The concentration and composition of free radicals are particularly important because they are highly reactive as a result of having unsatisfied chemical bonds.

The film-forming process is influenced by bombardment of the wafer surface by ions and electrons that are accelerated by the electric field. The plasma supplies a significant source of nonthermal energy, which allows for film deposition to occur at much lower temperatures than would be required if conventional LPCVD were used, a significant advantage when thin film coatings for passivation or chemical or mechanical protection of environmentally sensitive structures are required. Unlike LPCVD processes, which are typically performed at temperatures between 400 and 900°C, typical standard PECVD processes are rarely performed above 400°C. In fact, most standard substrate heaters for PECVD systems have a maximum operating temperature of 400°C, although custom heaters can go much higher in temperature.

The low deposition temperatures, combined with the more complicated film formation processes (i.e., ion bombardment), result in films that exhibit an extremely high sensitivity to deposition parameters. For instance, commonly used precursors either contain hydrogen in their molecular structure or rely on hydrogen as a carrier gas for delivery into the vacuum vessel. The substrate temperatures associated with PECVD can be so low that hydrogen-containing reaction products, including hydrogen itself, cannot desorb from the substrate surface and instead become incorporated into the films. Incorporation of hydrogen results in films with a lower mass density than their stoichiometric counterparts. Under typical processing conditions, it is straightforward to produce films with hydrogen concentrations in excess of 30 at.%. Incorporation of hydrogen also affects the mechanical and optical properties of the as-deposited films in ways that are impossible to generalize but are well documented in the literature.

As-deposited films, especially silicon and its derivatives, are amorphous when deposited by PECVD, but in the case of semiconductors such as silicon and silicon carbide, can be transformed into nanocrystalline films by a postdeposition annealing step. Likewise, a modest postdeposition annealing step at temperatures above 400°C can be effective in modifying the residual stress as-deposited films. These anneals do not induce crystallization, but they are high enough in temperature to initiate densification by hydrogen evolution.

In terms of reactor usage, care must be given to ensure that the as-deposited films are free of pinhole defects. The most significant contributor to pinholes is particulate contamination either by gas phase nucleation or by degradation of coatings on reactor components. Unlike conventional LPCVD, PECVD reactors typically utilize a horizontal configuration where the substrates rest atop the grounded electrode. This geometry lends itself very well to particulate contamination. Mitigation procedures include regular chamber cleaning and proper chamber seasoning. Although cross-contamination is a real concern, most fabrication facilities allow multiple materials to be deposited in the same reactor and many commercially available reactors come equipped for this capability. In these cases, regular chamber cleaning is essential. Fortunately, most vacuum vessels utilize a clamshell design that facilitates easy access to the interior of the reaction chamber and its internal components.

2.3.1.4 Atmospheric Pressure Chemical Vapor Deposition

Simply put, APCVD is a CVD process that is performed at atmospheric pressure. As such, APCVD does not require active pressure control during operation, and thus is well suited for epitaxial growth of single crystalline Si, SiC, and other processes that require high substrate temperatures. Figure 2.5 is a schematic diagram of an APCVD reactor developed for silicon carbide growth. The reactor, which can be horizontally or vertically oriented, consists of a reaction vessel made from a fused quartz, double-walled tube in which water is circulated for cooling. Induction coils connected to an RF generator traverse the circumference of the reaction vessel. Substrates are mounted to an inductively heated, wedgelike susceptor as shown in Fig. 2.5. Precursor gases are mixed with a carrier gas that is delivered at high flow rates, often in the standard liter/min range (slm). The high flow rates serve to reduce the thickness of the boundary layer that forms at the surface of the substrates,

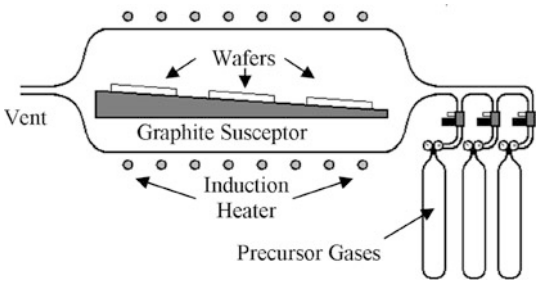

Fig. 2.5 Schematic diagram of a horizontal APCVD reactor

thus enhancing the flux of precursors to the wafer surface. Because of the relatively thick boundary layer, the process is performed in the mass transfer limited regime. High deposition temperatures ensure that surface reactions are not the rate limiting step. As implied by Fig. 2.2, film growth rates are substantially higher than the typical LPCVD process, but precursor depletion effects ultimately limit the number of substrates that a typical reactor can accommodate. Taking into account reactor preparation times, throughput is usually much lower than for the large-scale LPCVD systems, and therefore APCVD is not typically used to deposit polycrystalline and amorphous films for MEMS with the notable exceptions of silicon carbide and thick polysilicon (>10 μm), known as epi-poly, which are featured later in this chapter.

2.3.1.5 Hot Filament Chemical Vapor Deposition

Used primarily as a means to deposit polycrystalline diamond, HFCVD is a special case of LPCVD in which a heated tungsten filament is placed in close proximity to a heated substrate. For diamond growth, the purpose of the filament is to facilitate dissociation of hydrogen gas into atomic hydrogen, which is critical to the preferential formation of diamond over other forms of carbon. For other materials, the hot filament aids in the dissociation of precursor gases, enabling the substrate temperature to be kept lower than in conventional LPCVD. Reliance on the hot filament makes scaleup of HFCVD reactors challenging. HFCVD has also been used to deposit amorphous silicon at temperatures in the 200–300°C range [8–12].

2.3.1.6 Microwave Plasma Chemical Vapor Deposition

A variant of PECVD where instead of using parallel electrodes to generate an electric field at 13.56 MHz, the system is equipped with a microwave source that operates at 2.45 GHz. This method is commonly used in the deposition of polycrystalline, nanocrystalline and ultrananocrystalline diamond films.

2.3.2 LPCVD Polycrystalline Silicon

2.3.2.1 Material Properties and Process Generalities

For both MEMS and IC applications, polycrystalline silicon (polysilicon) films are most commonly deposited by LPCVD. Typical processes are performed in large-scale, horizontal furnaces at temperatures ranging from 580 to 650°C and pressures from 100 to 400 mtorr. The most commonly used source gas is silane (SiH_4). The microstructure of polysilicon thin films consists of a collection of small grains whose microstructure and orientation is a function of the deposition conditions [13]. For typical LPCVD processes (e.g., 200 mtorr), the amorphous-to-polycrystalline transition temperature is about 570°C, with polycrystalline films deposited above the transition temperature. At 600°C, the grains are small and equiaxed, whereas

at 625°C, the grains are large and columnar [13]. The crystal orientation is predominantly (110) Si for temperatures between 600 and 650°C, whereas the (100) orientation is dominant for temperatures between 650 and 700°C.

Although polysilicon can be doped by solid source diffusion or ion implantation, in situ doping during the LPCVD process is an effective means of modifying the electrical properties of the film. In situ doping of polysilicon is performed by simply including a dopant gas, usually diborane (B_2H_6) or phosphine (PH_3), in the CVD process. The inclusion of boron generally increases the deposition rate of polysilicon relative to undoped films, whereas phosphorus reduces the rate [14]. Inclusion of dopants during the LPCVD process leads to the production of conductive films with uniform doping profiles without the high-temperature steps commonly associated with solid source diffusion or ion-implantation. In situ doping is commonly used to produce conductive films for electrostatic devices, but has also been used to create polysilicon-based piezoresistive strain gauges, with gauge factors as high as 15 having been reported [15].

The thermal conductivity of polysilicon is a strong function of its microstructure, which, in turn is dependent on deposition conditions [13]. For fine-grain films, the thermal conductivity is about 25% of the value of single-crystal Si. For thick films with large grains, the thermal conductivity ranges between 50 and 85% of the single-crystal value.

Like the electrical and thermal properties of polysilicon, the as-deposited residual stress in polysilicon films depends on microstructure. For films deposited under typical conditions (200 mtorr, 625°C), the as-deposited polysilicon films have compressive residual stresses. The highest compressive stresses are found in amorphous Si films and in highly textured (110) oriented polysilicon films with columnar grains. Fine-grained polysilicon tends to have tensile stresses. The density of polysilicon has been reported as $2.25 - 2.33\,\mathrm{g/cm^3}$ under varied conditions [16]. The refractive index of polysilicon has been reported as $3.22 - 3.40$ also under varied conditions [16]. The fracture toughness of polysilicon has been measured to be $1.2 \pm 0.2\,\mathrm{MPa}\sqrt{\mathrm{m}}$ [17].

From both the materials properties and processing perspectives, polysilicon has matured to the point that commercial foundries are able to offer full service surface micromachining processes based on LPCVD polysilicon, the two most notable being the MEMSCAP MUMPs^{TM} process and the Sandia SUMMiT V^{TM} process. The MUMPs^{TM} process is a popular multiuser process whose design guidelines can be found in [18]. Although the exact growth conditions of these films are not typically published in the literature, it has been reported that the films are deposited using silane gas at a temperature of 580°C and pressure of 250 mtorr [19]. High-cycle fatigue testing of these films was explored in [20]. Table 2.5 details some of the important material properties that have been reported for the MUMPs^{TM} polysilicon.

Another multiuser process is the Sandia SUMMiT V^{TM} process. This process provides the MEMS designer with five low stress polysilicon structural layers whose conductivity is reported to be $9.10 \pm 0.23 - 33.99 \pm 5.14\,\Omega/\mathrm{sq}$. The complete design guidelines for this process can be found in [23].

Table 2.5 Material properties of polysilicon from the MEMSCAP MUMPs™ process as reported in the literature

References	Thickness (μm)	Young's modulus (GPa)	Poisson's ratio	Tensile strength (GPa)	Residual stress (MPa)	Sheet resistance (Ω/sq)
[21]	3.5	169 ± 6.15	0.22 ± 0.011	1.20 ± 0.15		
[22]	2	149 ± 10			-3.5 ± 0.5	
[18]	$0.5 - 2$	158 ± 10	0.22 ± 0.01	$1.21 - 1.65$	$-50 - 0$	$1 - 45$
[19]	2	162 ± 4	0.20 ± 0.03			

2.3.2.2 Process Selection Guidelines

Many device prototyping facilities that specialize in silicon surface micromachining utilize commercially available, large-scale LPCVD furnaces of the type described previously. From the processing perspective, most of the commercially available furnaces are similar in construction; therefore to first order, process parameters such as furnace temperature, precursor flow rates, furnace pressures tend to fall into fairly narrow ranges. Unfortunately, most process-oriented publications fail to provide details pertaining to the deposition hardware used in the production of the polysilicon films. As a point of reference for readers interested in examining the relationship between furnace hardware and deposition recipes, Table 2.6 details the standard LPCVD polysilicon processes offered by the Microfabrication Laboratory at CWRU. The lab is equipped with two large-scale MRL Industries™ Model 1118 LPCVD furnaces configured specifically for polysilicon, one for undoped polysilicon and the other for in situ phosphorus-doped polysilicon. Each furnace accommodates a 1.93 m long, 235 mm diameter quartz tube.

Table 2.6 LPCVD polysilicon deposition recipes for the two MRL industries™ model 1118 polysilicon furnaces in the microfabrication laboratory at CWRU

Film type	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (μm)	Residual stress (MPa)
Undoped	615	SiH_4	100	300	8.5	2	–220
Doped	615	SiH_4	100	300	5.5	2	–150
		PH_3	5				

Examination of the literature reveals that the preponderance of the work in developing LPCVD-based deposition processes for polysilicon MEMS has focused on characterizing the mechanical and electrical properties of the films. Tables 2.7–2.19 summarize a survey of the literature in this area. Tables 2.7, 2.9, 2.10, 2.11, 2.12, and 2.19 focus on undoped polysilicon and Tables 2.8, 2.13, 2.14, 2.15, 2.16, 2.17, 2.18, and 2.19 centern on doped films. Inasmuch as annealing is an important processing step for stress modification and dopant activation, Tables 2.11, 2.12, 2.13, 2.14, 2.15, 2.16, 2.17, 2.18, and 2.19 are specific to annealed films.

Table 2.7 Deposition conditions for undoped LPCVD polysilicon films

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Thickness (μm)	Dep. rate (Å/min)
[24]	560–630	SiH_4	30	300–550	2	
[25]	570	SiH_4	100	300	2	45
[26]	570	SiH_4	80	150	1.3	30
[27]	570	SiH_4	45	150		26
[28]	575	SiH_4	43	150	0.25–0.28	30
[27]	580	SiH_4	45	150		30
[29]	580	SiH_4	500	1000		87
[30]	580	SiH_4		300	2 ± 0.02	50
[31]	585	SiH_4	50	200	0.5	40
[27]	590	SiH_4	45	150		35.5
[32, 33]	600	SiH_4	125	550	0.1	
[27]	600	SiH_4	45	150		42
[34]	605	SiH_4	250	550	2	
[35]	605	SiH_4	125	550		100
[27]	610	SiH_4				49
[25]	615	SiH_4	100	300	2	83
[36]	620	SiH_4	70	100	0.46	
[37]	620	SiH_4	70	300	0.5	
[38]	625	SiH_4		250	0.25–1	100
[26]	625	SiH_4	80	180	3	100
[39]	630	SiH_4	20	400	0.2	
		N_2	110			
[40]	635	SiH_4		150	1.5–2	
[41]	640	SiH_4		600	0.23–2.3	100

2.3.2.3 Case Studies

It is generally the case that for LPCVD polysilicon films, the deposition rate increases with increasing temperature. Figure 2.6 is a plot of deposition rate versus deposition temperature for an LPCVD process where the pressure was fixed at 150 mtorr and the SiH_4 flow rate was held constant at 45 sccm [27]. The temperature range examined in this study was from the amorphous-to-polycrystalline transition temperature of roughly 570–610°C, where highly textured, columnar (110) oriented polysilicon is typically deposited. The data illustrate the dramatic increase in deposition rate as a result of the high growth rates associated with (110) Si grains in this temperature range as compared with other orientations. These data show the strong connection between deposition rate and film microstructure in LPCVD polysilicon, an effect that should be taken into account by the process engineer when selecting a particular process route.

Residual stresses in as-deposited polysilicon are heavily dependent on deposition temperature. Figure 2.7 is a plot typical of residual stresses in as-deposited polysilicon films [24]. This figure graphs residual stress versus deposition temperature for polysilicon films deposited at fixed SiH_4 flow rate and three distinct

Table 2.8 Deposition conditions for in situ doped LPCVD polysilicon films

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (mtorr)	Thickness (μm)	Dep. rate (Å/min)
[42]	560–610	SiH_4	100	375–800	2	22–83
		PH_3/SiH_4	1.4×10^{-4} to 1×10^{-2}			
[43]	560	SiH_4	100	800	2	
		PH_3	0.16			
[29]	580	SiH_4	500	1000		45
		PH_3/SiH_4	10×10^{-3}			
[43]	590	SiH_4	50	500	2	
		PH_3	0.16			
[43]	610	SiH_4	100	375	2	
		PH_3	1			
[44]	625	SiH_4	60	750	0.4	46.25
		PH_3	30			
		N_2	300			
[45]	650	PH_3/SiH_4	1:99	320	0.1–2	26.7
[46]	555	SiH_4	200–400	350		24–105
		BCl_3 [a]	0–180			

[a] 3% in N_2

Table 2.9 Mechanical properties of undoped LPCVD polysilicon films

References	Temp (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Fracture toughness (MPa$\sqrt{m}$)
[47]	565			1		2.84 ± 0.09	
[48]	580			2.1	175 ± 21		
[17]	580			3.5			1.2 ± 0.2
[49]	620			1–1.4	175 ± 25	2.7–3.4	
[36]	620	70	100	0.46	151 ± 6		
[36]	620	70	100	0.46	162 ± 8		
[39]	630	20[a]	400	0.2	160		
[50]	630	na[b]		4	190		

[a] N_2 gas at 110 sccm also used during deposition
[b] H_2 gas also used during deposition

deposition pressures. The residual stresses are compressive regardless of deposition pressure for temperatures below 580°C. At a temperature of 600°C, the residual stress is moderately or highly tensile, but transitions dramatically back to compressive for a deposition temperature of 620°C. These observations correlate strongly to the varying microstructure in polysilicon films over this relatively small temperature range.

Figure 2.7 above illustrates the difficulty in using deposition parameters to control the residual stress in as-deposited polysilicon films. Fortunately, postdeposition

Table 2.10 Residual stress in as-deposited, undoped LPCVD polysilicon films

References	Temperature (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Thickness (μm)	Residual stress (MPa)
[24]	560–630	30	300–550	2	–340 to 1750
[26]	570	80	150	1.3	82
[25]	570	100	300	2	270
[32, 33]	600	125	550	0.1	12
[25]	615	100	300	2	–200
[25]	570–615	100	300	2.72	<10[a]
[36]	620	70	100	0.46	–350 ± 12
[39]	630	20[b]	400	0.2	–180

[a]The stress gradient in this film is ≤2 MPa/μm
[b] N_2 gas at 110 sccm also used during deposition

Table 2.11 Residual stress in undoped LPCVD polysilicon films subjected to post deposition annealing

References	Deposition temperature (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Annealing conditions	Thickness (μm)	Residual stress (MPa)
[47]	565			1050°C, 10 s RTA[a]	1	142
[26]	570	80	150	1200°C, 6 h	1.3	17
[25]	570	100	300	1100°C, 30 min	2	30
[17]	580			1000°C, 1 h	3.5	12 ± 5
[31]	585	50	200	650°C, 3 h[b]	0.5	250
[25]	615	100	300	1100°C, 30 min	2	–20
[37]	620	70	300	900–1150°C, 1–10 s RTA	0.5	–340 to 90
[36]	620	70	100	1100°C, 2 h	0.46	Low stress
[26]	625	80	180	1200°C, 6 h	3	–205
[50]	630	Dna[c]		1000°C, 90 min	4	42

[a]RTA: Rapid Thermal Anneal
[b]Anneal performed at 500 mtorr
[c]H_2 gas also used during deposition

annealing is an effective means to alter the residual stress in as-deposited polysilicon films. Temperatures required for effective stress modification (~1000°C) are easily achievable. For example, it has been reported that residual stresses of about –500 MPa can be reduced to less than –10 MPa by annealing at 1000°C in a N_2 ambient [55, 56]. If performed in a conventional furnace, such high-temperature annealing could be problematic if the substrate contains temperature-sensitive elements such as selectively doped regions. Fortunately, rapid thermal annealing has proven to be an effective method of stress reduction in polysilicon films. It has been reported that a 10 s anneal at 1100°C was sufficient to completely relieve the stress

Table 2.12 Strain in undoped LPCVD polysilicon films subjected to postdeposition annealing

References	Temp. (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Annealing conditions	Thickness (μm)	Residual strain
[28]	575	43	150	600°C	0.25–0.28	~600 μstrain (tensile)
[48]	580			1000°C, 2 h 1050°C, 3 h	2.1	0.021–0.0084%
[30]	580		300	600°C, 180 min	2	–0.001 to 0.7% (comp)
[34]	605	250	550	950°C, 2 h	2	0.017% (tensile)
[40]	635		150		1.5–2	0.01%

Table 2.13 Mechanical properties of in situ doped LPCVD polysilicon films

References	Temp (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Doping and annealing conditions	Thickness (μm)	Young's modulus (GPa)
[43]	560	100	800	PH_3 at 0.16 sccm, 1050°C, 10 s RTA[a]	2	147 ± 2.4
[43]	590	50	500	PH_3 at 0.16 sccm, 1050°C, 10 s RTA	2	153 ± 2.8
[43]	610	100	375	PH_3 at 1 sccm, 1050°C, 10 s RTA	2	130 ± 3.9
[51]	650			Heavily P-doped	1.27	123

[a]RTA: Rapid Thermal Anneal

in films with an as-deposited stress of about –340 MPa [37]. Rapid thermal processing has even been used as the primary heat source in polysilicon LPCVD [57], offering a high-throughput, low thermal budget alternative to conventional LPCVD for applications where a thin polysilicon layer may be required on preprocessed wafers, such as polysilicon-based piezoresistors.

Figure 2.8 shows the relationship between residual stress and annealing temperature for films deposited at 550, 570, 580, and 615°C [25]. For this dataset, each anneal was each performed for 30 min in N_2. From a processing perspective, these data show that regardless of the as-deposited stress, residual stresses near zero can be achieved for annealing temperatures at or above 1000°C for films that were deposited near the amorphous-to-crystalline transition temperature, and 1100°C for high-textured polysilicon films. An early study showed that high-temperature annealing (~1100°C) resulted in grain growth and recrystallization, regardless of whether the polysilicon was deposited on thermal oxide or LPCVD oxide [56].

Table 2.14 Mechanical properties of LPCVD polysilicon films doped by ion implantation

References	Temp (°C)	Doping and annealing conditions	Thickness (μm)	Tensile strength (GPa)	Young's modulus (GPa)
[47]	565	P, 80 keV, $4.0 \times 10^6 cm^{-2}$, 1050°C 10 s RTA[a]	1	2.11 ± 0.10	
[47]	565	As, 120 keV, $4.0 \times 10^6 cm^{-2}$, 1050°C 10 s RTA	1	2.70 ± 0.09	
[47]	565	B, 15 keV, $2 \times 10^{16} cm^{-2}$, 1050°C 10 s RTA	1	2.77 ± 0.08	
[16]	620	Varied implant and annealing conditions	0.1–0.8		151–166

[a]RTA: Rapid Thermal Anneal

Table 2.15 Mechanical properties of LPCVD polysilicon films doped by PSG[a]-based diffusion and unspecified methods

References	Temp (°C)	Pressure (mtorr)	Doping and annealing conditions	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)
[19]	580	250	PSG, 1050°C 1 h	2	1.62 ± 4	
[43]	610		PSG, 1050°C 10 s RTA[b]	2	168 ± 7	
[16]	620	100	Varied doping Varied anneal	0.1–0.8	151–166	
[52]	630		PSG, 1000°C, 1 h	1	169	2–3
[51]	650		Heavily P-doped	1.27	123	

[a]Phosphosilicate glass
[b]RTA: Rapid Thermal Anneal

Reduction in residual stress can be achieved in polysilicon by means other than high-temperature annealing. For instance, a process has been developed that utilizes the residual stress characteristics of polysilicon deposited under various conditions to construct polysilicon multilayers that have the desired thickness and stress values [25]. The multilayers are comprised of alternating tensile and compressive

Table 2.16 Residual stress in doped LPCVD polysilicon films

References	Temp (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Doping and annealing conditions	Thickness (μm)	Residual stress (MPa)	Stress gradient (MPa/μm)
[42]	560–610	100	375–800	In situ: PH_3 PH_3/SiH_4: $1.4 \times 10^{-4} - 1 \times 10^{-2}$ Anneal: 900°C, 10–120 s RTA[a]	2	–195 to 310	
[53]	580			P implantation: $1 - 4 \times 10^{15}/cm^2$. Anneal: 950°C, 1–10 h	2	40.3–83.9	4.7–29.2
[54]	580		350	P diff. or ion implant, Varied anneal	2	26–72	0.3–24
[31]	585	50	200	$POCl_3$ diffusion: 850–950°C N_2: 2 slm O_2: 100 sccm $POCl_3$: 100 sccm 650°C, 3 h, 500 mtorr	0.5	–110	
[16]	620		100	Varied doping Varied anneal	0.1–0.8	–560 to 30	
[26]	625	80	180	$POCl_3$ diffusion: 1 h at 950–1100°C. Anneal: 1200°C, 6 h	3	–98 to 11	

[a]RTA: Rapid Thermal Anneal

Table 2.17 Electrical properties of in-situ doped polysilicon films

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (mtorr)	Dep. rate (Å/min)	Resistivity (mΩ cm)	Annealing
[42]	560–610	SiH_4 PH_3/SiH_4	$100\,(0.014-1)\times 10^{-2}$	375–800	22–83	0.46–5.3	RTA[a] 900°C, 10–120 s
[29]	580	SiH_4 PH_3/SiH_4	500 0.01	1000	45	0.5	980°C, 30 min
[44]	625	SiH_4 PH_3 N_2	60 30 300	750	46.25	1	900°C, 30 min
[46]	555	SiH_4 BCl_3[b]	200–400 0–180	350	24–105	0.002–0.03	None
[45]	650	PH_3/SiH_4	0.01	320	26.7	1.7	None

[a]RTA: Rapid Thermal Anneal
[b]3% in N_2

Table 2.18 Electrical properties of LPCVD polysilicon doped by diffusion

Reference	Deposition temperature (°C)	Gas	Flow rate (sccm)	Pressure (mtorr)	Diff. temp. (C)	Sheet resistance (Ω/sq)	Annealing conditions
[31]	585	SiH_4 O_2 N_2 $POCl_3$	50 100 2000 100	200	850–950	12	650°C, 3 h, 500 mtorr

Table 2.19 Surface roughness and refractive index of annealed LPCVD polysilicon

References	Temp (°C)	Gas	Pressure (mtorr)	Thickness (μm)	Dep. rate (Å/min)	Surface roughness (nm)	Refractive index	Annealing conditions
[30]	580	SiH_4	300	2	50	0.8		600°C, 180 min
[25]	615	SiH_4	300	2	83	71		1100°C, 30 min
[16]	620	SiH_4	100	0.1–0.8			3.2–3.4	Varied
[44]	625	SiH_4 PH_3 N_2	750	0.4	46	12		900°C, 30 min

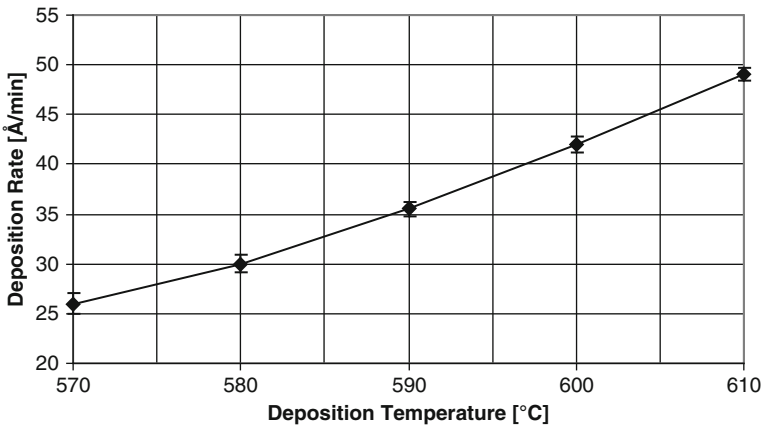

Fig. 2.6 Polysilicon growth rate as a function of temperature for silane gas reacted at 45 sccm and 150 mtorr in a 15 cm diameter horizontal LPCVD furnace [27] (Reprinted with permission. Copyright 2002 Elsevier)

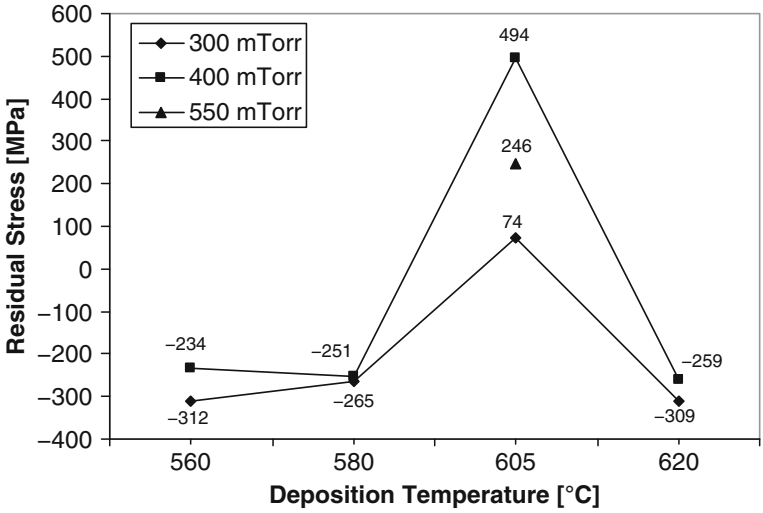

Fig. 2.7 Polysilicon residual film stress as a function of deposition temperature and pressure for 2 μm thick films deposited using silane at 30 sccm [24] (Reprinted with permission. Copyright 2001, Elsevier)

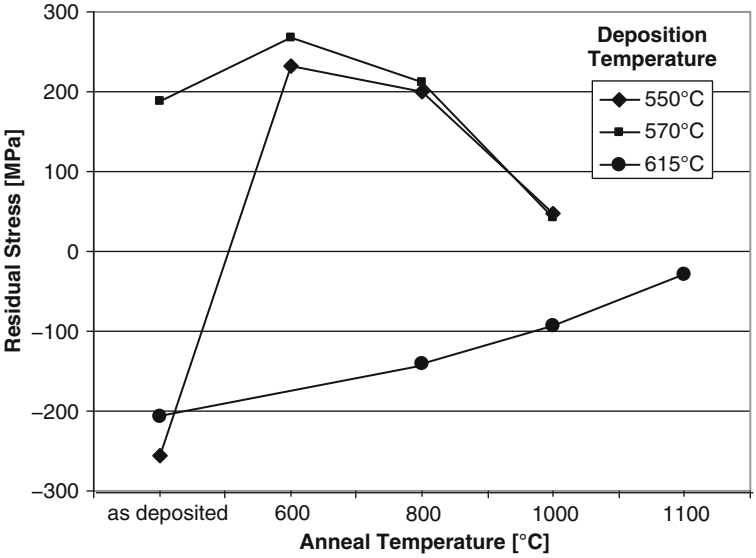

Fig. 2.8 Residual film stress as a function of annealing temperature for 2 μm thick polysilicon films deposited at varied temperatures and annealed for 30 min in N_2 [25] (Reprinted with permission. Copyright 2000 IEEE)

polysilicon layers that are deposited in a sequential manner. Known as the "multipoly process," the tensile layers consist of fine-grained polysilicon grown at a temperature of 570°C, and the compressive layers are made up of columnar polysilicon deposited at 615°C. The overall stress in the composite film depends on the number of alternating layers and the thickness of each layer. With the proper selection of layer thickness, a polysilicon multilayer can be deposited with near-zero residual stress (<10 MPa) and very little stress gradient (<0.2 MPa/μm) in a ten-layer stack. The process does not require annealing, a considerable advantage for MEMS fabrication processes with restricted thermal budgets.

Along similar lines, nickel silicide (Ni_xSi_y) films have been used to compensate for residual stress gradients in polysilicon thin films [58]. Silicides are used in CMOS technology to reduce sheet and contact resistances in polysilicon gates and thus are compatible with polysilicon MEMS processing. Silicide films are formed on polysilicon surfaces by depositing a Ni film by thermal evaporation and annealing the film at ~400°C. The resulting sheet resistance is reduced from 20,000 to 10 Ω/sq; and the stress gradient is completely eliminated by annealing at 290°C.

2.3.3 LPCVD Silicon Dioxide

2.3.3.1 Material Properties and Process Generalities

Like its thermally grown counterpart, SiO_2 deposited by LPCVD is an electrical insulator. The dielectric constant of LPCVD SiO_2, commonly referred to as LTO or low temperature oxide due to its low deposition temperature when compared to thermal oxidation, is 4.3. The dielectric strength of LTO is about 80% of that for thermal oxide [59]. Unlike thermal oxide, the residual stress in LTO is process-dependent and tends to be compressive in as-deposited films.

LPCVD SiO_2 is one of the most widely used materials in the fabrication of MEMS. In polysilicon surface micromachining, LPCVD SiO_2 is used as a sacrificial material because it can be easily dissolved using etchants that do not attack polysilicon. LTO is widely used as an etch mask for dry etching of thick polysilicon films, because it is chemically resistant to dry etching processes for polysilicon. LTO films are also used as passivation layers on the surfaces of environmentally sensitive devices.

LPCVD SiO_2 films can be deposited on a wide variety of substrate materials, including Si, polysilicon, silicon nitride, silicon carbide, and substrates metalized with temperature-tolerant metals. In general, LPCVD provides a means for depositing thick (>2 μm) SiO_2 films at temperatures much lower than thermal oxidation. LTO films have a higher etch rate in HF than thermal oxides, which translates to significantly faster release times when LTO films are used as sacrificial layers. Phosphosilicate glass (PSG) can be formed using nearly the same deposition process as LTO by adding a phosphorus-containing gas to the precursor flows in an in situ doping process that resembles in situ polysilicon doping. PSG films are useful as sacrificial layers because they generally have higher etching rates in HF than

LTO films. PSG is compatible with LPCVD polysilicon deposition conditions, thus enabling its use in multilayered polysilicon surface micromachining processes [60]. Polysilicon films deposited at 605°C on PSG sacrificial layers exhibit a strong (111) texture and very low residual strains ($< 5 \times 10^{-5}$) [61], which are in stark contrast to similar films deposited on thermal oxide and LTO, which have high residual strains ($\sim -3 \times 10^{-3}$) and are highly textured (110) oriented films. The difference may be attributed to the influence of phosphorous on nucleation and grain growth in polysilicon.

PSG has been used as a source of dopants for LPCVD polysilicon films [18]. The process simply involves cladding an undoped polysilicon layer between two PSG layers and annealing the structure at 1050°C in N_2. The annealing step serves to drive phosphorus dopant atoms into the polysilicon from both top and bottom surfaces simultaneously, which dopes the films and balances the residual stresses. PSG layers as thin as 300 nm can be used to dope 1.5 μm thick polysilicon with phosphorus to a resistivity of 0.02 Ω cm [62]. Anneals for doping purposes can be performed at temperatures above 1100°C, however, concerns over delamination of PSG from underlying silicon nitride layers cap the annealing at 1050°C [63].

PSG and LTO films are deposited in hot-wall, low-pressure, fused silica furnaces in systems similar to those described previously for polysilicon. Precursor gases include SiH_4 as a Si source, O_2 as an oxygen source, and, in the case of PSG, PH_3 as a source of phosphorus. The single-source precursor tetraethoxysilane (TEOS or $Si(OC_2H_5)$) is also used to deposit oxides by LPCVD, albeit at higher deposition temperatures (~700°C). Silane-based LTO and PSG films are typically deposited at temperatures of 425–450°C and pressures ranging from 200 to 400 mtorr. The low deposition temperatures result in LTO and PSG films that are slightly less dense than thermal oxides due to the incorporation of hydrogen in the films. LTO films can, however, be densified by an annealing step at high temperature (1000°C). The low mass density of LTO and PSG films is partially responsible for the increased etch rate in HF. It has been found that the residual stress in PSG is about 10 MPa for phosphorus concentrations of 8% [64]. LTO and PSG films conform to undulant topographies, however, the degree of conformation is affected by low surface migration associated with the low deposition temperatures. PSG will reflow at temperatures above 900°C, a characteristic that can be used to alter coating thicknesses and profiles on undulant topographies.

2.3.3.2 Process Selection Guidelines

A review of the literature reveals that efforts to develop LTO and PSG beyond their roles as sacrificial, etch mask, bonding, and passivation materials are very rare. As a consequence, the literature lacks the wealth of information linking process conditions to material properties that can easily be found for structural materials such as polysilicon, silicon nitride, and silicon carbide. Although many surface micromachined MEMS devices are fabricated using LTO and/or PSG in the process sequence, most papers simply mention that these films were used and do not provide details pertaining to their deposition. This is ostensibly due to the fact that in most

Table 2.20 Deposition conditions for LTO and PSG films deposited in the MFL at CWRU

Film type	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Dep. rate (nm/min)	Residual stress (MPa)
LTO	450	SiH_4	51	350	15	∼–150
		O_2	61			
PSG	450	SiH_4	40	350	9.5	∼40
		O_2	60			
		PH_3	37.5			

cases, the films are deposited in large-scale, commercially available systems using vendor-provided recipes that were developed several decades ago for IC processing and thus the properties are common knowledge in the MEMS community.

Because nearly all MEMS fabrication facilities that offer polysilicon surface micromachining have an LPCVD oxide as part of their CVD repertoire, it would be remiss to omit key information regarding the deposition of such films. Table 2.20 details the standard LTO and PSG processes offered by the Microfabrication Laboratory at CWRU. The LTO and PSG deposition processes in this facility are performed in the same furnace platform (MRL Industries™ Model 1118) as previously described for polysilicon. The deposition processes closely resemble those commonly used in MEMS prototyping facilities that are equipped with high-throughput LPCVD furnaces.

LTO and PSG films were initially developed for passivation and intermetal dielectric layers in silicon-based ICs and the body of work in these areas is quite extensive. Reviewing this work is beyond the scope of this chapter, although a few references are worth noting due to their impact on MEMS technology. Tables 2.21, 2.22, and 2.23 summarize the process parameters and resulting material properties of relevance to MEMS from these publications.

Table 2.21 Deposition parameters and material properties for as-deposited PSG films

References	Temp (°C)	Gas	Gas flow ratio	Pressure (mtorr)	Deposition rate (nm/min)	Etch rate in HF (nm/s)	Residual stress (MPa)
[65]	425	O_2/SiH_4	4.35	200	8.0	>7	
		PH_3/SiH_4	0.22				
[66]	425	O_2/SiH_4	2	200	20	5	–10
		PH_3/SiH_4	0.1				
[67]	700	O_2/TEOS	1.23		70	9	200
		PH_3/TEOS	0.19				

2.3.3.3 Case Studies

References [65–67] contain much more information that might be of interest to the MEMS process engineer than are summarized in Tables 2.21, 2.22, and 2.23

Table 2.22 Deposition parameters and material properties for as-deposited LTO films

References	Temp (°C)	Gas	Gas flow ratio	Pressure (mtorr)	Deposition rate (nm/min)	Etch rate in HF (nm/s)	Residual stress (MPa)
[65]	425	O_2/SiH_4	4.35	200	7.5	~0.5	
[66]	425	O_2/SiH_4	2	200	20	0.67	–100
[67]	700	O_2/TEOS PH_3/TEOS	1.23 0.19		70	9	200

Table 2.23 Properties of annealed PSG and LTO films

References	Film	Gases	Deposition temperature (°C)	Annealing time and temperature	Etch rate in HF (nm/s)	Residual stress (MPa)
[65]	PSG	$O_2/SiH_4/PH_3$	425	30 min, 850°C	~6.4	
	LTO	O_2/SiH_4	425	30 min, 850°C	<0.5	
[66]	PSG	$O_2/SiH_4/PH_3$	425	30 min, 600°C		~0
		O_2/SiH_4	425	30 min, 850°C		–20
[67]	PSG	O_2/TEOS/PH_3	700	10 min, 950°C	5	100

and thus the interested reader is urged to seek these papers. For instance, [67] details the optical properties of TEOS-based PSG films and [66] characterizes the absorption coefficient, transmittance, dielectric constant, and breakdown voltage of as-deposited and annealed films. In addition, [66] compares PSG films deposited by LPCVD to those deposited by APCVD and PECVD. With respect to MEMS fabrication, Poenar et al. investigated PSG films specifically for surface micromachining [65]. They reported that the vertical etch rate as well as lateral undercut etch rate increased exponentially with increasing phosphorous content in the films. After annealing, the etch rates decreased by up to 70%, but this was not solely due to phosphorus out-diffusion or densification, but rather other structural changes in the film, such as bond configuration. It was also found that the phosphorous content has little effect on strain in polysilicon structural layers. They concluded that for surface micromachining applications, a PH_3/SiH_4 ratio was optimum for PSG sacrificial etching, yielding an etch rate of 8.5 μm/min in 20% HF with a shrinkage upon annealing of only 6%. In addition to these papers, readers interested in an in-depth review of silicon dioxide sacrificial etching should consider an excellent review by Buhler et al. [68].

2.3.4 LPCVD Silicon Nitride

2.3.4.1 Material Properties and Process Generalities

Silicon nitride (Si_3N_4) is widely used in MEMS for substrate isolation, surface passivation, etch masking, and as an electrically insulating structural material in suspended membranes, bridges, and other related structures owing to its physical properties [1]. Si_3N_4 is extremely resistant to chemical attack with an etch rate in HF of ~1 nm/min, thereby making it the material of choice for surface micromachining applications where oxide is used as a sacrificial layer. Si_3N_4 is commonly used as an insulating layer because it has a resistivity of $\sim 10^{14}$ Ω cm and dielectric strength of 10^7 V/cm. Silicon nitride has an electric bandgap of ~5 eV, which is considerably lower than thermal oxide, but because it has no shallow donors or acceptors, it behaves as an insulator. Silicon nitride is amorphous in microstructure with a mass density of 3.1 g/cm^3.

LPCVD Si_3N_4 films are deposited in horizontal furnaces similar to those used for polysilicon deposition. Typical deposition temperatures and pressures range between 700–900°C and 200–500 mtorr, respectively. The standard source gases are dichlorosilane (SiH_2Cl_2) and ammonia (NH_3). To produce stoichiometric Si_3N_4 a SiH_2Cl_2-to-NH_3 ratio in the range of 1:10 is commonly used. The microstructure of films deposited under these conditions in amorphous.

The residual stress in stoichiometric Si_3N_4 is large and tensile, with a magnitude of about 1 GPa [69]. Such a large residual stress causes films thicker than a few hundred nanometers to crack. Nonetheless, thin stoichiometric Si_3N_4 films have been used as mechanical support structures and electrical insulating layers in piezoresistive pressure sensors [70]. For applications that require micron-thick, durable, and chemically resistant membranes, nonstoichiometric Si_xN_y films can be deposited by LPCVD. These films, often referred to as Si-rich or low-stress nitride, are intentionally deposited with an excess of Si by simply increasing the ratio of SiH_2Cl_2 to NH_3 during deposition. Nearly stress-free films can be deposited using a SiH_2Cl_2-to-NH_3 ratio of 6:1, a deposition temperature of 850°C and a pressure of 500 mtorr [71]. A detailed study concerning the influence of the Si-to-N ratio on the residual stress in silicon nitride films can be found in [72, 73]. The composition of low-stress nitride has been reported to be $Si_{1.0}N_{1.1}$ [74]. The increase in Si content not only leads to a reduction in tensile stress, but also a decrease in the etch rate in HF. Such properties have enabled the development of MEMS structures and fabrication techniques that would otherwise not be feasible with stoichiometric Si_3N_4. For example, low-stress silicon nitride has been bulk micromachined using silicon as the sacrificial material [75]. In this case, Si anisotropic etchants (TMAH) were used for dissolving the sacrificial silicon. Low-stress silicon nitride has also been employed as a structural layer in surface micromachining using PSG as a sacrificial layer [76], capitalizing on the HF resistance of the nitride films.

The strength of silicon nitride films also varies with the Si-to-N ratio. For example, the tensile strength has been reported to be 6.4 GPa for stoichiometric films and 5.5 GPa for silicon-rich films [77]. A similar decrease in fracture toughness is

observed for silicon-rich silicon nitride with an upper bound to be <14 MPa$\sqrt{m}$ for stoichiometric nitride and 1.8 MPa$\sqrt{m}$ for low-stress nitride [78].

2.3.4.2 Process Selection Guidelines

The MFL at CWRU offers both stoichiometric and low-stress silicon-rich silicon nitride films deposited using a MRL Industries™ Model 1118 LPCVD furnace as previously described for polysilicon. Recipe details for these processes are shown in Table 2.24.

Table 2.24 Deposition conditions for stoichiometric and low-stress nitride films deposited at CWRU

Film type	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Dep. rate (nm/min)	Residual stress (MPa)
Stoichiometric	820	DCS[a] NH_3	18 108	280	3	~1000
Si-rich	850	DCS NH_3	62.5 17.5	~200	1.8	~100

[a]DCS = dichlorosilane (SiH_2Cl_2)

Although the deposition rate for low-stress nitride in the CWRU system is lower than that of the stoichiometric nitride, others have reported that for a SiH_2Cl_2-to-NH_3 ratio of 4:1 at 835°C and 300 mtorr, the deposition rate is over twice the rate in the CWRU system at 4 nm/min [45].

Tables 2.24 and 2.25 describe the process-related material properties of LPCVD silicon nitride films. Table 2.25 describes processes with respect to the precursor flow rate and Table 2.26 is based on precursor flow ratio. Table 2.27 details the mechanical properties of annealed silicon nitride films deposited by LPCVD.

2.3.4.3 Case Studies

The chemical resistance of silicon nitride lends itself to the fabrication of very thin membranes by silicon bulk micromachining. Reference [69] describes a study to characterize the mechanical properties of stoichiometric Si_3N_4 using 70–80 nm thick membranes. A 70–80 nm thick Si_3N_4 film was deposited on (100) Si wafers that were coated with a 300 nm oxide film. Rectangular windows were patterned on the backside of the wafer and an anisotropic Si etch was performed, stopping on the thin oxide. A brief hydrofluoric acid etch was then used to dissolve the thin oxide film, revealing 200–600 μm wide by 2400–11000 μm long nitride membranes. Load-deflection testing was then used to characterize the films, yielding a biaxial modulus of 288 GPa, a fracture stress of 10.8–11.7 GPa, and a residual stress of 1040 MPa [69].

As mentioned previously, the high residual stresses found in stoichiometric Si_3N_4 limit its use to very thin films. In surface micromachining, a nitride layer is desirable to isolate devices electrically from the bulk substrate. To prevent wafer warpage

Table 2.25 Mechanical properties of LPCVD silicon nitride[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[6]	770	DCS[b]	50	0.25	0.3	305[c]	1132
		NH_3	300				
[39]	790	DCS	20	0.6	0.2	290	1000
		NH_3	170				
[77]	820	DCS	18	0.28	0.2	325	1170–1300
		NH_3	108				
[51, 74]	835	DCS	70	0.3	2.1	373	
		NH_3	15				
[34]	835	DCS	64	0.3	1.5		96
		NH_3	16				
[79]	840	DCS	64		0.5	220	280
		NH_3	16		0.7		360
[80]	850–880	DCS	80–448	0.25–0.6	0.4–2.4		–52 to 641
		NH_3	24–187				
[80]	880	DCS	96	0.6			0 ± 10
		NH_3	24				

[a] With respect to precursor flow rates
[b]DCS: Dichlorosilane (SiH_2Cl_2)
[c]Biaxial modulus

Table 2.26 Mechanical properties of LPCVD silicon nitride[a]

References	Temp (°C)	Gas	Ratio	Pressure (mtorr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[81]	770	DCS[b]/NH_3	0.05–0.5				~1000
[82]	785	DCS/NH_3	0.33	368		330	1020
[5]	800	DCS/NH_3	0.33				860
[83]	850	DCS/NH_3	0.33				1200
[76]	850	DCS/NH_3	0.33	150		320	967
[73]	775	SiH_4/NH_3	0.625	203			600
[73]	750	SiH_4/NH_3	2				<–50
[77]	na	DCS/NH_3	4		0.3	295	322
[71]	850	DCS/NH_3	4	500	2		98
[83]	850	DCS/NH_3	4				<–100
[84]	850	DCS/NH_3	5		1	186	108
[85]	800	DCS/NH_3	5.5	14			1200
[76]	850	DCS/NH_3	5.7	150		360	125
[82]	785	DCS/NH_3	6	368		230	430

[a] With respect to precursor flow ratios
[b]DCS: dichlorosilane (SiH_2Cl_2)

Table 2.27 Mechanical properties of annealed LPCVD silicon nitride films

References	Temp (°C)	Gas	Gas flow (sccm) or ratio	Pressure (torr)	Thickness (μm)	Annealing conditions	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)
[86]	840	DCS[a] NH_3	6–1	0.17	0.76	1100°C, N_2 2 h	202	12	291
[87]	840	DCS NH_3 N_2	1000 16 100	0.2	0.3–0.7	1100°C Forming gas 2 h	248		
[83]	850	DCS/NH_3	4			O_2, 1100°C, 3 h			10

[a]DCS = dichlorosilane (SiH_2Cl_2)

due to stress, the stoichiometric silicon nitride is typically left on the backside of the wafer. In order to access the bulk wafer electrically, one must pattern access vias through the nitride layer. The MEMSCAP MUMPS™ process incorporates a 600 nm low-stress nitride film to isolate devices, allowing complete backside nitride removal [18]. In order to characterize the in situ stress of a 1.5 μm thick low-stress nitride film, a microfabricated vernier strain gauge was realized [34]. Deposited at 835°C with a pressure of 300 mtorr using SiH_2Cl_2 and NH_3 flow rates of 64 and 16 sccm, respectively, the stress was measured to be 96 MPa.

Silicon-rich silicon nitride films are attractive for MEMS applications not only for their low residual stresses, but also for their attractive thermal properties. Matrangelo et al. describe a process to measure the thermal conductivity and heat capacity of low stress nitride using microbridge structures [74]. In their study, the authors used a low-stress nitride ($Si_{1.0}N_{1.1}$) deposited at 835°C using SiH_2Cl_2 and NH_3 flow rates of 70 and 15 sccm, respectively. The microbridge fabrication process began with the deposition of a 3 μm phosphosilicate glass layer on a silicon substrate, after which the PSG was annealed for 5 h at 1100°C. Next a 2–4 μm thick low-stress nitride was deposited using the parameters above. A 200–600 nm thick layer of undoped polysilicon was deposited and then heavily doped using PSG. The silicon and nitride layers were then formed into 200 μm long by 3 μm wide bridge structures by reactive ion etching (RIE). The bridges were released by etching away the PSG in HF. Using these bridge structures, the low-stress nitride films were found to have a mass density of 3.0 g/cm^3, a thermal conductivity of 3.2×10^{-2} W/cm K, and a heat capacity of 0.7 J/gK.

Surface micromachined structures have also been used to determine the Young's modulus of low-stress nitride films [51]. In this study, a silicon wafer was first coated with a 4 μm thick PSG layer, followed by the deposition of a 2 μm thick low-stress nitride film. The nitride film was then patterned into microbridges by RIE and a timed etch in buffered HF was used to release the structures. A stylus profilometer was scanned along the length of the microbridges, allowing the Young's modulus to be extracted. The Young's modulus in the $Si_{1.0}N_{1.1}$ films was found to be 373 GPa [51].

2.3.5 LPCVD Polycrystalline SiGe and Ge

2.3.5.1 Material Properties and Process Generalities

Germanium (Ge) and silicon–germanium (SiGe) are of interest to the MEMS community because of the low temperatures required to deposit polycrystalline films, making them potentially compatible with Si CMOS structures in integrated MEMS devices. Polycrystalline Ge (poly-Ge) films can be deposited by LPCVD at temperatures as low as 325°C on Si, Ge, and silicon–germanium (SiGe) substrate materials [88]. Ge does not readily nucleate on SiO_2 surfaces, which hinders the use of thermal oxides and LTO films as sacrificial layers, but facilitates the use of patterned oxide films as sacrificial molds. Residual stress in poly-Ge films deposited

on Si substrates can be reduced to nearly zero after anneals at modest temperatures (~600°C). Poly-Ge is essentially impervious to KOH, TMAH, and BOE, enabling the fabrication of Ge structures on Si substrates by anisotropic etching [88]. The mechanical properties of poly-Ge are comparable with polysilicon, with a Young's modulus of 132 GPa and a fracture stress ranging between 1.5 and 3.0 GPa [89]. Mixtures of HNO_3, H_2O, and HCl and H_2O, H_2O_2, and HCl can be used to isotropically etch Ge, enabling poly-Ge to be used as a sacrificial substrate layer in polysilicon surface micromachining. Using these techniques, poly-Ge-based thermistors and Si_3N_4 membrane-based pressure sensors made using poly-Ge sacrificial layers have been successfully fabricated [88]. Poly-Ge deposition processes are temperature-compatible with Si CMOS as shown by Franke et al. who found no performance degradation in Si CMOS devices following the fabrication of surface micromachined poly-Ge structures [89].

Like poly-Ge, polycrystalline SiGe (poly-SiGe) is a material that can be deposited at temperatures lower than polysilicon. Although the name implies a Si-to-Ge ratio of 1:1, the ratio of Si to Ge in the films does not have to be unity. Deposition processes use SiH_4 and GeH_4 as precursor gases. Deposition temperatures range between 450°C for conventional LPCVD [90] and 625°C for rapid thermal CVD (RTCVD) [91]. Like polysilicon, poly-SiGe can be doped with boron and phosphorus to modify its conductivity. In situ boron doping can be performed at temperatures as low as 450°C [90]. Sedky et al. [92] showed that the deposition temperature of conductive films doped with boron could be further reduced to 400°C if the Ge content was kept at or above 70%. Films grown at temperatures around 400°C exhibit a strain gradient in the range of $\sim 1 \times 10^{-5}/\mu m$, which has been attributed to the columnar microstructure of the films combined with a high compressive stress at the film/substrate interface [93]. Boron doping enhances uniformity in the columnar microstructure through the thickness of the film and thus reduces the strain gradient. It has recently been reported that deposition temperatures for poly-SiGe can be reduced to 210°C, however, to achieve strain gradients on the order of $1 \times 10^{-6}/\mu m$, the films must be annealed following deposition [94].

Unlike poly-Ge, poly-SiGe can be deposited on SiO_2 [91], PSG [89] and poly-Ge [89] substrates. For growth of Ge-rich films on oxide substrate layers, a thin polysilicon seed layer is sometimes used to enhance nucleation. As with many alloys, the physical properties of the material depend on chemical composition. For example, etching of poly-SiGe by H_2O_2, becomes significant for Ge concentrations over 70%. Sedky et al. [92] showed that the microstructure, film conductivity, residual stress, and residual stress gradient are related to the concentration of Ge in the material. Franke et al. [90] produced in situ boron-doped films with residual compressive stresses as low as 10 MPa.

The poly-SiGe/poly-Ge material system is particularly attractive for surface micromachining inasmuch as H_2O_2 can be used to dissolve poly-Ge sacrificial layers. It has been reported that poly-Ge etches at a rate of 0.4 μm/min in H_2O_2, whereas poly-SiGe with Ge concentrations below 80% have no observable etch rate after 40 h [95]. The ability to use of H_2O_2 as a sacrificial etchant makes the combination of poly-SiGe and poly-Ge attractive for surface micromachining

from processing, safety, and materials compatibility points of view especially when compared with the polysilicon/silicon dioxide material system. Poly-SiGe structural elements, such as gimbal-based microactuator structures have been made by high-aspect-ratio micromolding [95]. PolySiGe has a lower thermal conductivity than Si, making it a well-suited alternative to polysilicon for thermopiles [96].

Poly-SiGe films exhibit a residual stress that can either be moderately tensile or moderately compressive depending on the Ge content and deposition temperature [92, 97]. For instance, it was found that for polySiGe films deposited by LPCVD at 450°C, the residual stress ranged from –31 MPa for a film with a Ge concentration of 64 at % to –160 for a Ge concentration of 47 at.% [97]. Annealing can be used to reduce both stress and stress gradients, and in fact, RF MEMS structures fabricated from poly-SiGe have shown a nearly twofold increase in quality factor if the films are annealed at 600°C [98]. Unfortunately the temperature-sensitive substrates on which the poly-SiGe films are usually deposited ultimately limits the extent to which annealing can be performed. It has been shown that pulsed laser annealing can be an effective means to locally eliminate stress gradients in poly-SiGe films [99].

As mentioned previously, poly-SiGe is well suited as a structural layer for integrated MEMS [90]. The low deposition temperatures associated with poly-SiGe structural components and polyGe sacrificial layers enable the fabrication of complete Si CMOS structures prior to MEMS fabrication. Use of H_2O_2 as the sacrificial etchant eliminates the need for layers to protect the underlying CMOS structure during release. A significant advantage of this design lies in the fact that the MEMS structure can be positioned directly above the CMOS structure, thus reducing the parasitic capacitance and contact resistance characteristic of interconnects associated with conventional side-by-side integration strategies. Recent efforts to advance the use of poly-SiGe as a structural layer in CMOS integrated MEMS includes process development in a large-scale LPCVD furnace of a design-of-experiments methodology designed to explore the interplay among process parameters and thickness, residual stress, strain gradient, and resistivity [93] as well as strategies to realize low-resistance electrical contacts between poly-SiGe structures and interconnect metallization [100].

2.3.5.2 Process Selection Guidelines

Tables 2.28, 2.29, 2.30, and 2.31 provide process-related material property data for as-deposited and annealed SiGe films deposited by LPCVD.

2.3.6 LPCVD Polycrystalline Silicon Carbide

2.3.6.1 Material Properties and Process Generalities

Unlike Si, crystalline silicon carbide (SiC) is a polymorphic material that exists in cubic, hexagonal, and rhombohedral polytypes. Well over 100 possible polytypic configurations have been identified, but only three are technologically relevant

Table 2.28 Deposition conditions for LPCVD SiGe films on oxide coated Si substrates

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Dep. rate (nm/min)	Thickness (μm)
[101]	450	Si_2H_6 GeH_4 PH_3 (50% in SiH_4)	15 185 5	0.3	7	
[101]	450	Si_2H_6 GeH_4 B_2H_6 (10% in SiH_4)	25 175 4	0.3	20	
[102]	400	GeH_4 PH_3 (50% in SiH_4)	219 5	0.3	21	5.1
	450	GeH_4 SiH_4 (90% in B_2H_6) SiH_4	90 50 85	0.6	17	3.1
[103]	410–440	SiH_4 GeH_4 BCl_3 (in He)	104–120 50–70 6–18	600	4.7–12.5	1.7–2.6
[103]	350	GeH_4 BCl_3 (in He)	100 12	300	7.7	2.2

because methods exist to produce single crystalline substrates and/or epitaxial thin films. Two of these are hexagonal polytypes, denoted 4H-SiC and 6H-SiC, a nomenclature that references that stacking sequence of Si and C atoms. Both of these polytypes are available as single-crystalline wafers, and epitaxial films of the same polytype can be grown on these substrates. Owing to the challenges associated with micromachining SiC, the 4H- and 6H-SiC polytypes have seen limited use as structural elements in MEMS, although pressure transducers and accelerometers have been fabricated using selective photoelectrochemical etching [104] and deep reactive ion etching [105]. 4H- and 6H-SiC are both attractive for high-temperature electronics, due to their wide bandgaps, which are 2.9 and 3.2 eV for 6H-SiC and 4H-SiC, respectively. All polytypes of SiC do not melt, but rather sublime at temperatures in excess of 2200°C.

The third technologically relevant polytype is a cubic polytype known as 3C-SiC, which in fact is the only cubic configuration known to exist in SiC. Unlike its hexagonal counterparts, 3C-SiC is not commercially available as single-crystalline substrates, although several efforts over the years have been devoted to producing large-area single-crystalline wafers. 3C-SiC has a diamond lattice structure like Si that enables epitaxial growth of 3C-SiC films on Si wafers. This fact, coupled with the material properties of 3C-SiC makes it an attractive complement to Si for harsh environment MEMS [106]. The electronic bandgap of 3C-SiC is 2.3 eV, which is less than 6H-SiC but more than double that of Si (1.1 eV). 3C-SiC has a thermal conductivity of 5 W/cm °C, a breakdown field of 4×10^6 V/cm, a dielectric constant

Table 2.29 Mechanical properties of silicon germanium films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Fract. strain (%)	Strain gradient (10^4/μm)
[102]	400	GeH_4	219	0.3	5.1	132	–100	1.1	1.3
		SiH_4 (50% in PH_3)	5						
[102]	450	GeH_4	90	0.6	3.1	146	–10	1.2	1.9
		B_2H_6 (10% in SiH_4)	50						
		SiH_4	85						
[103]	410–440	SiH_4	104–120	0.6	1.7–2.6		–70 to –228		1.2–8.7
		GeH_4	50–70						
		BCl_3 (in He)	6–18						
[103]	350	GeH_4	100	0.3	2.2		–83		
		BCl_3 (in He)	12						
[101]	550	Si_2H_6	15	0.3	2		–50		
		GeH_4	185						
		PH_3 (50% in SiH_4)	5						

Table 2.30 Electrical properties of silicon germanium films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Resistivity (mΩ cm)
[102]	400	GeH_4 PH_3 (50% in SiH_4)	219 5	0.3	5.1	20
	450	GeH_4 SiH_4 (90% in B_2H_6)	90 50	0.6	3.1	1.8
[103]	410–440	SiH_4 GeH_4 BCl_3 (in He)	104–120 50–70 6–18	0.6	1.7–2.6	0.96–10
[103]	350	GeH_4 BCl_3 (in He)	100 12	0.3	2.2	5.0
[101]	550	Si_2H_6 GeH_4 PH_3 (50% in SiH_4)	15 185 5	0.3	2	20

Table 2.31 Mechanical properties of annealed silicon germanium films deposited by LPCVD[a]

Reference	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Residual stress (MPa)	Strain gradient (10^4/μm)
[102]	400	GeH_4 PH_3 (50% in SiH_4)	219 5	0.3	5.1	200	0.94

[a]Films annealed by rapid thermal annealing at 550°C for 30 s.

of 9.72, a coefficient of thermal expansion of 4.2×10^{-6}/°C and an electron mobility of 1000 cm^2/Vs, which is the highest of the three polytypes. The Young's modulus of 3C-SiC is still the subject of research, but most reported values range from 350 to 450 GPa, depending on the microstructure and measurement technique.

From a processing perspective, the 4H-SiC and 6H-SiC polytypes are not compatible with Si substrates due to the high temperatures required for film growth (>1500°C) as well as the incompatible crystalline structure (although one could argue that (111) Si presents a crystalline face that closely resembles a hexagonal configuration). In contrast, 3C-SiC can be grown directly on Si using the epitaxial processes described in more detail in Section 3.4.2 .

To first order, micromachining of SiC is independent of crystalline polytype. SiC is not etched in any wet Si etchants and is not attacked by XeF_2, a popular dry Si etchant used for releasing device structures [107]. Patterning of SiC films is performed by conventional reactive ion etching using fluorinated plasmas often mixed with O_2 and sometimes an inert gas. Selectivity to Si-based materials is a major issue and patterning with photoresist is not presently possible, at least for films in

the micron thickness range. Alternatives to photoresist for RIE masks include metals such as Al and Ni. Recent efforts in developing a RIE process for SiC surface micromachining have been successful in achieving an acceptable selectivity to SiO_2 [108].

Polycrystalline SiC (poly-SiC) is a more versatile material for SiC MEMS than its single-crystal counterparts because poly-SiC is not constrained to single-crystalline substrates but can be deposited on a variety of materials, including polysilicon, SiO_2, and Si_3N_4, Commonly used deposition techniques include LPCVD [107, 109, 110] and APCVD [111, 112]. The deposition of poly-SiC can be performed at temperatures ranging from 700 to 1200°C. The microstructure of poly-SiC films is dependent on the substrate material and the deposition process used to grow the films. For amorphous substrates such as SiO_2 and Si_3N_4, APCVD poly-SiC films deposited from SiH_4 and C_3H_8 are randomly oriented with equiaxed grains [112], whereas for oriented substrates such as polysilicon, the texture of the poly-SiC film can be made to match that of the substrate itself [111]. By comparison, poly-SiC films deposited by LPCVD from SiH_2Cl_2 and C_2H_2 are highly textured (111) films with a columnar microstructure [109], whereas films deposited from disilabutane have a distribution of orientations [107]. This variation suggests that device performance can be tailored by selecting the proper substrate and deposition conditions.

SiC films deposited by AP- and LPCVD generally suffer from large residual stresses that are tensile and on the order of several 100 MPa. Moreover, the residual stress gradients in these films tend to be large, leading to significant out-of-plane bending of structures anchored at a single location. The thermal stability of stoichiometric SiC makes a postdeposition annealing step impractical for films deposited on Si substrates, because the temperatures needed to significantly modify the film are likely to exceed the melting temperature of the wafer.

2.3.6.2 Process Selection Guidelines

Poly-SiC can be deposited by LPCVD using a wide range of carbon and silicon containing precursors; however, relatively recent efforts to develop the material specifically for MEMS applications have focused on two approaches: a dual precursor approach using acetylene and dichlorosilane [113, 116], and a single precursor approach based on disilabutane [114]. Both of these development efforts were performed using large-scale, horizontal furnaces so as to mimic the deposition processes used for polysilicon, silicon nitride, and LTO/PSG. Tables 2.32, 2.33, 2.34, and 2.35 summarize the principle findings of these groups as well as other notable efforts reported in the literature.

2.3.6.3 Case Studies

Widespread adoption of poly-SiC as a structural material for MEMS applications has been hindered by the large residual stresses (for the most part tensile) and associated stress gradients in films deposited on Si substrates. Unlike polysilicon, for

Table 2.32 Deposition conditions for dichlorosilane-based LPCVD poly-SiC processes[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Dep. rate (nm/min)
[115]	800	DSB[b] DCS[c]	45 0–40			4.2–5.3
[116]	900	DCS C_2H_2 (5% in H_2)	54 180	2.5–5	~0.5	3–5
[117]	900–1000	DCS	10	0.150	0.7–5	4.8
[118]		C_2H_2	10			

[a]Denoted biaxial modulus
[b]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[c]DCS: Dichlorosilane (SiH_2Cl_2)

which the residual stresses can be significantly altered by annealing, poly-SiC, for the most part, is immune to structural alteration, at least for annealing conditions compatible with Si substrates. Efforts have been made to address this issue for both the dual and single precursor approaches by developing methods to control residual stress during the deposition process. For the SiH_2Cl_2- and C_2H_2-based dual precursor system, a relationship between deposition pressure and residual stress has been found that enables the deposition of undoped poly-SiC films with nearly zero residual stresses and negligible stress gradients [113]. This work was performed in a MRL™ Model 1118 LPCVD furnace modified to support poly-SiC growth at a temperature of 900°C (see Tables 2.31 and 2.33 for more details). The pressure range where the residual stress was observed to vary significantly was between ~0.5 and 5 torr. In the lower range of pressures (<2.5 torr) the residual stress was tensile, decreasing from ~700 MPa at 0.5 torr to ~50 MPa at 2.5 torr. For pressures above 3 torr, the residual stress was moderately compressive at –100 MPa. The behavior was attributed to differences in alignment and size of the columnar <111> oriented grains in the films. A similar dependence on deposition pressure was also observed when NH_3 was used as an in situ doping precursor, although the minimum residual stress (29 MPa) was observed at a pressure of 5 torr and a transition to compressive stresses was not observed [128]. The minimum resistivity in these films was 0.017 Ω cm, and this occurred at a deposition pressure of 4 torr and a residual stress of ~60 MPa.

Like the dual precursor approach, development of poly-SiC film processes using the single precursor DSB focused on identifying a process that produced low-stress, highly conductive films. Early work centered on producing high-conductivity films using NH_3 as the doping gas [134, 135]. Films were grown at temperatures ranging from 650 to 850°C [135]. A minimum conductivity of 0.02 Ω cm was reported for films deposited at a temperatures of 850°C when using NH_3 as a doping gas [134]. At a deposition temperature of 800°C, the resistivity of as-deposited films is roughly 0.028 Ω cm, but this can be reduced to nominally 0.02 Ω cm when the film is annealed at 1000°C [135].

Table 2.33 Deposition conditions for non-dichlorosilane-based LPCVD poly-SiC processes

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Thickness (μm)	Dep. rate (nm/min)
[119]	780	DSB[a]	na	5×10^{-5}	0.6	3.5
[120]	800	DSB	5	0.1	1	
		NH_3 (5% in H_2)	NH_3: DSB = 0.05			
[121]	800	DSB	5		2	
		NH_3 (10% in H_2)	2			
[120]	850	DSB	5	0.11	2	
		TMA[b]	TMA: DSB = 0.1			
[122]	930–1150	TMS[c]	10	0.4	0.33–1.35	
		H_2	1000			
[123]	1100	3MS	40	4–8	1–3	
		H_2	1000			
[124]	1010	SiH_4	15	2.48	1	
		C_2H_2	7			
		HCl	Trace			
		H_2	10,000			
		B_2H_6	1.5			
[125]	1100	SiH_4	1.5	40	2	
		C_2H_4	4.5			
		H_2	3000			
		NH_3	0–5			

[a]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[b]TMA: Trimethyl aluminum: ($Al(CH_3)_3$)
[c]TMS: Tetramethylsilane ($Si(CH_3)_4$)

Table 2.34 Mechanical properties of poly-SiC films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Fracture toughness (MPa$\sqrt{m}$)
[121]	800	DSB[a]	5		2		23.4		
		NH_3 (10% in H_2)	2						
[115]	800	DSB	45						
		DCS[b]	0–40					240–1.2	
[116]	900	DCS	54	2.5–5	0.531			–98 to 172	
		C_2H_2 (5% in H_2)	180						
[126]	900	DCS	35	2	2.7	403		56	
		C_2H_2 (5% in H_2)	180						
[127]	900	DCS	54	2.75		373		26.9	
		C_2H_2 (5% in H_2)	180						
[128]	900	DCS	35	4		334		59	2.9–3.0
[129]		C_2H_2 (5% in H_2)	180						
		NH_3 (5% in H_2)	64						
[117]	900	DCS	10	0.150	0.7–5	347		30–250	
[118]	1000	C_2H_2	10						
[122]	930–1150	TMS[c]	10	0.4	0.33–1.35			–176 to 145	
		H_2	1000						

Table 2.34 (continued)

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Fracture toughness (MPa$\sqrt{m}$)
[124]	1010	SiH_4	15	2.48	1	530		300	
		C_2H_2	7						
		HCl	Trace						
		H_2	10,000						
		B_2H_6	1.5						
[123]	1100	3MS	40	4–8	1–3			120	
		H_2	1000						
[130]	1200	3MS	35						
		H_2	1000					188	
		N_2	1						
[131]	1200	SiH_4	na	40	0.04–1.4	322–415*	3.2–6.5	192–347	
		C_2H_4	na						
[132]	1280	C_3H_8	C/Si: 0.8 –1	300		246			
		SiH_4							
		H_2 (2% Ar)	SiH_4/H_2: 0.024%						
		C_2H_2 (5% in H_2)	180						

[a]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[b]DCS: Dichlorosilane (SiH_2Cl_2)
[c]TMS: Tetramethylsilane ($Si(CH_3)_4$)
*Plane-strain modulus

Table 2.35 Electrical properties of poly-SiC films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (mtorr)	Thickness (μm)	Resistivity (Ω cm)
[120]	800	DSB[a]	5	100		1000
[120]	800	DSB	5	100	1	0.03
		NH_3 (5% in H_2)	5:100[b]			
[120]	850	DSB	5	110	2	16
		TMA[c]	10:100[d]			
[133]	900	DCS[e]	35	2000	1	
		C_2H_2 (5% in H_2)	180			
		NH_3 (1% in H_2)	20			1.466
		NH_3 (1% in H_2)	100			0.036
[128]	900	DCS	35	4000		0.017
		C_2H_2 (5% in H_2)	180			
		NH_3 (5% in H_2)	64			
[124]	1010	SiH_4	15	2.48	1	0.01
		C_2H_2	7			
		HCl	Trace			
		H_2	10000			
		B_2H_6	1.5			
[125]	1100	SiH_4	1.5	40	2	
		C_2H_4	4.5			
		H_2	3000			
		NH_3	0			0.56
		NH_3	5			1×10^{-3}
[130]	1200	3MS	35			
		H_2	1000			4×10^{-2}
		N_2	1			

[a]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[b]Ratio of NH_3 to DSB
[c]TMA: Trimethyl aluminum: ($Al(CH_3)_3$)
[d]Ratio of TMA to DSB
[e]DCS: Dichlorosilane (SiH_2Cl_2)

In order to modify residual stresses and stress gradients in DSB-based poly-SiC films, several approaches have been explored. One approach uses a method similar to the Multi-poly process described earlier in this chapter. For DSB-based, nitrogen-doped poly-SiC films exhibiting a resistivity of 0.02–0.03 Ω cm, the average strain is roughly 0.2% [136]. However, as the resistivity increases to ~20 Ω cm in undoped films, the average strain drops to 0.1%. By properly sequencing doped and undoped poly-SiC layers, a 3 μm thick film with a strain gradient of $5 \times 10^{-5}/\mu m$ and a resistivity of 0.024 Ω cm could be produced [136].

A second approach to adjust residual stress in DSB-based poly-SiC films involves the use of a Si-containing precursor to adjust the chemical composition of the poly-SiC film [137]. In this method, DCS is used as the additional source of Si. Films were grown at 800°C using a DSB flow rate of 45 sccm, and the DCS flow rate was

varied to achieve DCS-to-total gas flow ratios from 0 to ~0.5. Under these conditions, the Si-to-C ratio in the as-deposited films varied from 1 to ~1.2. Likewise, residual stresses varied from 1.2 GPa for a Si-to-C ratio of 1 (no DCS flow) to 240 MPa for a Si-to-C ratio of 1.2. The mechanism responsible for the significant drop in residual stress is linked to an increase in grain size with increasing DCS flow, as well as a higher concentration of Si in the films.

A third approach to modify residual stress in DSB-based poly-SiC films involves a postdeposition anneal. It was recently shown that a postdeposition annealing step performed at temperatures between 925 and 1050°C on doped poly-SiC films deposited at 800°C using DSB and DCS precursors is effective at shifting the residual stress from nominally 400 MPa to roughly –300 MPa and reducing the resistivity from ~0.07 to ~0.03 Ω cm [138].

2.3.7 LPCVD Diamond

2.3.7.1 Material Properties and Process Generalities

Diamond has a collection of physical properties that makes it very attractive for a wide range of MEMS materials [106]. Diamond is commonly known as nature's hardest material, making it ideal for high wear environments. Diamond has a very large electronic bandgap (5.5 eV) which makes it attractive for high-temperature electronics. Undoped diamond is a high-quality insulator with a dielectric constant of 5.5; however, it can be relatively easily doped with boron to create p-type conductivity, and n-type conductivity can be achieved by doping with nitrogen. The electron mobility in diamond exceeds that of 3C-SiC at 2200 cm^2/Vs, and it has a breakdown field of $1 \times 10^7 V/cm$. Diamond has the highest Young's modulus among the materials used in MEMS (1035 GPa) and a thermal conductivity of 20 W/cm °C, which is double that of SiC and over ten times that of Si. Diamond is among nature's most chemically inert materials except perhaps in oxidizing atmospheres.

Diamond thin films used in MEMS are polycrystalline in microstructure and are often classified by the size of the crystallites in the film. Nucleation of diamond films on nondiamond substrates from the gas phase is challenging without the aid of a seed layer. Substrate seeding often involves sonication of the substrate with nano- or microscale diamond particles. An alternative called biased-enhanced nucleation (BEN) has eliminated the need for sonication and is particularly well suited when plasma techniques are used to grow the films. Micro- and nanocrystalline diamond films are typically grown by hot filament or microwave plasma CVD methods using a hydrocarbon precursor such as methane combined with hydrogen gas. The grain size is, in part, determined by the diameter and density of the seed particles. Atomic hydrogen is responsible for suppressing the growth of sp^2 bonded carbon. A relatively recent development in thin film diamond technology is ultrananocrystalline diamond (UNCD). UNCD films are particularly attractive for MEMS due to their outstanding physical and chemical properties and combined low deposition temperatures, making them more compatible with a wider range of MEMS materials than

their micro- and nanocrystalline counterparts. In terms of materials properties, it has been shown that UNCD films exhibit a measured hardness of 98 GPa, a Young's modulus of ~960 GPa and a fracture strength ranging from 3990 to 5080 MPa [139]. By comparison, similar test specimens made from single-crystalline 3C-SiC had a measured Young's modulus of ~435 GPa and a fracture strength of 2090–2680 MPa [139].

Fabrication of diamond MEMS is currently restricted to polycrystalline material inasmuch as single-crystal diamond wafers are not yet commercially available and thus epitaxial growth for MEMS is not feasible. Diamond films can be deposited on Si and SiO_2 substrates by CVD methods, but the surfaces must be seeded by diamond powders or biased with a negative charge to initiate growth. In general, microcrystalline diamond prefers to nucleate on Si surfaces than on SiO_2 surfaces, an effect that has been used to selectively pattern diamond films using SiO_2 molding masks [140].

2.3.7.2 Process Selection Guidelines

Tables 2.36, 2.37, and 2.38 provide process-related details for micro-, nano- and ultrananocrystalline diamond films used in MEMS fabrication.

2.3.7.3 Case Studies

Patterning of diamond structures is arguably the most challenging aspect of diamond MEMS fabrication due to the chemical inertness of the material. Early methods to pattern diamond included: use of Si molds to create bulk micromachined diamond structures [152], selective seeding using diamond-loaded photoresist [153], patterning seed layers using photoresist liftoff [154], O_2 ion beam etching of diamond thin-films [155], and biased enhanced nucleation through patterned SiO_2 masks [156]. Wang et al. [157] developed a process to fabricate a vertically actuated, doubly clamped micromechanical diamond beam resonator using conventional RIE. In this process diamond films grown by MPCVD on SiO_2 sacrificial layers were etched in a CF_4/O_2 plasma using Al as a hard mask. The etch was reasonably selective to SiO_2 (15:1), enabling the fabrication of diamond disk resonators suspended on a polysilicon stem with polysilicon drive and sense electrodes [158]. Along similar lines, Sepulveda et al. have successfully fabricated surface micromachined diamond cantilever-beam resonators by RIE using silicon dioxide as a sacrificial layer and a Ti film as an etch mask [159].

Microcrystalline diamond films grown using conventional techniques tend to have high residual stress gradients and roughened surfaces as a result of the highly faceted, large-grain polycrystalline films that are produced by these methods. The rough surface morphology degrades the patterning process, resulting in roughened sidewalls in etched structures and roughened surfaces of films deposited over these layers. Unlike polysilicon and SiC, a postdeposition polishing process is not technically feasible for diamond due to its extreme hardness. To address this issue, Krauss et al. [145] have developed an ultrananocrystalline diamond (UCND) film

Table 2.36 Deposition conditions and material properties of micro and nanocrystalline diamond deposited by MPCVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Resistivity (Ω cm)
[141]	450–550	CH_4	3	700	6.75–15	741–913	0.7		
		CO_2	8						
		H_2	200						
	625–725	CH_4	3	700	20–33	710–1015	0.8–1.6		
		CO_2	8						
		H_2	200						
[142]	400–800	CH_4	6	800		450–1050		550 to –440	
		H_2	30						
		Ar	564						
[143]	800	CH_4	6	800	97.5			200–1200	
		H_2	12–60						
		Ar	582–532						
[144]	850	CH_4	5	1500	40				0.2–300
		H_2	500						

[a]Film thickness: 0.5–5 μm

Table 2.37 Deposition conditions and properties of ultrananocrystalline diamond (UNCD) by MPCVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Fracture toughness (MPa√m)
[145]	300–800	CH_4 Ar	1 99		100		700–1000		
[146]	na	na	na			0.5–0.6	941–963	3.9–5.0	
[147]	800	CH_4 Ar	na na		100	0.6–0.8	975	0.89–5.0	

Table 2.38 Deposition conditions and properties of polycrystalline diamond deposited by HFCVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Resistivity (Ω cm)
[148]	680–740	CH_4 (0.3% in H_2)	400	11.25	600–1010	2.8–3.25	<5	
[149]	680	CH_4 H_2	na na		790		–370	0.2–300
[150]	800–900	CH_4 H_2	4 400	50				0.29–116
[151]	900	CH_4 (1% in H_2)		50				0.03–0.28

[a]Film thickness: 1–20 μm

that exhibits a much smoother surface morphology than its micro- and nanocrystalline counterparts. Unlike conventional CVD diamond films that are grown using a mixture of H_2 and CH_4, the ultrananocrystalline diamond films are grown from mixtures of Ar, H_2, and C_{60} or Ar, H_2, and CH_4. A typical process uses a 2.56 GHz MPCVD system with a precursor mixture consisting of 1% CH_4 balanced with Ar at a flow rate of 100 sccm and substrate temperatures in the 350–800°C range [160].

The process is in stark contrast with conventional HF- or MPCVD growth of diamond where a high concentration of hydrogen is used to suppress formation of sp^2 bonded carbon. The absence of hydrogen ensures that a very high density of ultrasmall nuclei ($\sim 10^{11}/cm^2$) form on the substrate surface. A typical film grown at 400°C consists of 3–5 nm equiaxed grains grown at rates as high as 0.4 μm/h [160]. UNCD films have proven to be effective as conformal coatings on Si surfaces, and have been used successfully in several surface micromachining processes [160]. Unlike diamond films grown by conventional means, the CH_4–Ar precursor system used in UNCD growth enables direct nucleation on SiO_2 surfaces, thus making UNCD highly compatible with conventional surface micromachining. For patterning, an oxygen-resistant hard mask such as SiO_2 is used in conjunction with a oxygen plasma. UNCD is highly resistant to HF, thus enabling the release of suspended structures. UNCD can readily be doped with nitrogen resulting in n-type conductivity with semimetal-like behavior in heavily doped samples.

Given the large bandgap of diamond (5.5 eV), UNCD is proving to be among the most versatile materials in the MEMS materials toolbox because films with

electrical properties ranging from highly insulating to highly conductive can be produced by controlled incorporation of dopants. At substrate temperatures of 400°C, the UNCD growth process is highly compatible with Si CMOS integration [161]. UNCD films tend to have lower stresses and stress gradients than micro- and nanocrystalline diamond films [148]. The hydrogen-terminated surfaces of ultrathin (submicron) UNCD films functionalized with DNA oligonucleotides exhibit a high degree of chemical stability and sensitivity, making them particularly well suited for biosensor applications [162].

2.3.8 APCVD Polycrystalline Silicon Carbide

2.3.8.1 Material Properties and Process Generalities

Like LPCVD, APCVD can be used to deposit poly-SiC films. The APCVD process is much less common than its LPCVD counterpart, but historically it was one of the first techniques used to deposit poly-SiC for MEMS applications and still remains a viable method. Like LPCVD poly-SiC, the properties of APCVD poly-SiC depend on the substrate temperature and material of the substrate. The most commonly used precursors are propane (C_3H_8) and SiH_4, with ultrahigh purity H_2 used as a carrier gas. However, any precursor or combination of precursors that contain Si and C are potential candidates. The deposition temperatures of APCVD poly-SiC tend to be several hundred degrees Celsius higher than LPCVD.

2.3.8.2 Process Selection Guidelines

Table 2.39 details relevant process information and mechanical property data for poly-SiC films deposited by APCVD.

2.3.9 PECVD Silicon

2.3.9.1 Material Properties and Process Generalities

Although much less commonly used than its LPCVD counterpart, PECVD has emerged as an alternative to LPCVD for the production of Si-based surface micromachined structures on temperature-sensitive substrates due to the much lower deposition temperatures needed to deposit the films. Gaspar et al. [166] reported on the development of surface micromachined microresonators fabricated from hydrogenated amorphous Si (a-Si:H) thin films deposited by PECVD. The vertically actuated resonators consisted of doubly clamped microbridges suspended over fixed Al electrodes. The a-Si:H films were deposited using SiH_4 and H_2 precursors and PH_3 as a doping gas. The substrate temperature was held to around 100°C, which enabled the use of photoresist as a sacrificial layer. The microbridges consisted of a large paddle suspended by two thin paddle supports, with the paddle providing a

Table 2.39 Deposition conditions and film properties for poly-SiC films deposited by APCVD

References	Substrate	Temp (°C)	Gas	Gas flow (sccm)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Fracture toughness (MPa$\sqrt{m}$)
[163]	SiO_2	1050	SiH_4 (5% in H_2) C_3H_8 (15% in H_2) H_2	204 52 25,000	2.8		150–214	2.8–3.4
[164]	Si	1100	HMDS[a] (90% in H_2)	na		367		
[165]	Poly	1160	SiH_4 (5% in H_2) C_3H_8 (15% in H_2) H_2	26 102 25,000	2	494	113	
[165]	Poly	1280	SiH_4 (5% in H_2) C_3H_8 (15% in H_2) H_2	26 102 25,000		340–357	401–486	

[a]HMDS: Hexamethyldisilane: ($(CH_3)_6Si_2$)

large reflective surface for optical detection of resonant frequency. The megahertz-frequency resonators exhibited quality factors in the 1×10^5 range when tested in vacuum. This work has since been extended to using polynorbornene polymer as a sacrificial layer material [167]. A polynorbornene known as Unity 4011™ thermally decomposes into vapor at 425°C, enabling a dry, nonplasma-based release process. Surface micromachined resonators were successfully fabricated from a-Si:H films deposited by PECVD using this method. Cracking observed near the anchor points of some structures was attributed to differences in thermal expansion coefficients.

Chang and Sivoththaman have used conventional photoresist as a sacrificial layer to fabricate a tunable RF MEMS inductor based on PECVD Si [168]. In this case, photoresist could be used because the PECVD Si film was deposited at a temperature of only 150°C. The as-deposited films exhibited a residual compressive stress of about 300 MPa. The PECVD Si films were used in conjunction with sputtered Al with a residual tensile stress of nominally 10 MPa to create bimorph inductors whose stress-induced vertical displacement could be regulated by an actuation voltage.

2.3.9.2 Process Selection Guidelines

Tables 2.40, 2.41, and 2.42 provide process-related details and material property data for as-deposited and annealed SiC films deposited by PECVD.

2.3.10 PECVD Silicon Dioxide

2.3.10.1 Material Properties and Process Generalities

PECVD is perhaps the most common method to produce silicon dioxide films. Using a plasma to dissociate the gaseous precursors, the deposition temperatures needed to deposit PECVD oxide films are lower than for LPCVD films by as much as several hundred degrees. Commonly used source gases include single precursors such as TEOS or dual precursors such as SiH_4 and N_2O. PECVD oxides are commonly used as masking, passivation, and protective layers especially on devices that have been coated with metals. For this reason, residual stress is the principle property of interest for process engineers considering PECVD SiO_2 films in MEMS structures. Residual stress is heavily dependent on process parameters which in turn may be dictated by the substrate. Annealing has been shown to be an effective means to modify residual stress in PECVD oxide films, both to reduce the magnitude of stress as well as to change its state.

2.3.10.2 Process Selection Guidelines

Tables 2.43 and 2.44 summarize the process-related material property data for SiO_2 films deposited by PECVD.

Table 2.40 Deposition parameters and insulating properties for Si films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Power or power density	Pressure (torr)	Dep. rate (nm/min)	Thickness (μm)	Conductivity (1/Ω cm)
[169]	150	SiH_4 Ar	10 7	77–114 mW/cm^2	0.5–0.75	22–31	0.5–3	Dark: 10^{-10} Light: 10^{-6}
[170]	250	SiH_4/H_2	10	50 mW/cm^2	0.1	0.6–2.4	0.1–0.8	10^{-3}
[171]		PH_3	na					
[172]	300	SiH_4 Ar	1/4–1/8	100–300 W	0.8	75		
[173]	300	SiH_4 Ar	40 20	50–215 W	0.38–0.53	7–16	1	

Table 2.41 Mechanical properties of Si films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Power or power density	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[169]	150	SiH_4	10	77–114 mW/cm^2	0.5–0.75	0.5–3		–370
		Ar	7					–130
[170]	250	SiH_4/H_2	10	50 mW/cm^2	0.1	0.1–0.8	146	
[171]		PH_3	na					
[172]	300	SiH_4	1/4–1/8	100–300 W	0.8			–360 to –380
		Ar						
[173]	300	SiH_4	40	50–215 W	0.38–0.53	1		–520 to –575
		Ar	20					

Table 2.42 Mechanical properties of annealed Si films deposited by PECVD[a]

Reference	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	As-deposited residual stress (MPa)	Postanneal residual stress (MPa)
[173]	300	SiH_4 Ar	40 20	50–215	0.38–0.53	1	–520 to –575	300

[a]Annealing conditions: 100 min at 367°C

Table 2.43 Deposition conditions and mechanical properties of SiO_2 films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Dep. rate (μm/min)	Thickness (μm)	Residual stress (MPa)
[174]	60	SiH_4 [a] N_2O	430 710	HF: 20 LF: 20	1			–25
[174]	300	SiH_4 N_2O	430 710	HF: 20 LF: 20	1			–200
[5]	300	SiH_4 N_2O N_2	na na na					–397
[175]	350	TEOS O_2	2.3[b] 9500			0.25	3.2 12.5	∼–90 ∼–45
[175]	400	SiH_4 N_2O N_2	300 9500 1500			1	20	∼–80

[a]2% in N_2
[b]For TEOS, the flow rate is in ml/min. TEOS: tetraethylorthosilicate: $(Si(OC_2H_5)_4)$

Table 2.44 Mechanical properties of annealed SiO_2 films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Thickness (μm)	As-deposited residual stress (MPa)	Annealing conditions	Residual stress after anneal (MPa)
[5]	300	SiH_4 N_2O N_2	na na na	0.3	–397	O_2, 800°C, 30 min	–172
[175]	350	TEOS O_2	2.3[a] 9500	3.2 12.5	∼–90 ∼–45	500°C 500°C	∼–80 <10
[175]	400	SiH_4 N_2O N_2	300 9500 1500	20	∼–80	500°C	20

[a]For TEOS, the flow rate is in ml/min. TEOS: tetraethylorthosilicate: $(Si(OC_2H_5)_4)$

2.3.11 PECVD Silicon Nitride

2.3.11.1 Material Properties and Process Generalities

PECVD silicon nitride (sometimes referred to simply as SiN or Si_xN_y:H) is generally nonstoichiometric and may contain significant concentrations of hydrogen. Use of PECVD silicon nitride in micromachining applications is somewhat limited because it has a high etch rate in HF (e.g., often higher than that of thermally grown SiO_2). However, PECVD offers the ability to deposit nearly stress-free silicon nitride films at temperatures lower than LPCVD-based low-stress nitride, an attractive property for passivation, encapsulation, and packaging. Like its Si and SiO_2 counterparts, PECVD SiN is commonly deposited using SiH_4 as the silicon-containing precursor gas with NH_3 being the nitrogen-containing precursor. Deposition temperatures are considerably lower than for LPCVD silicon nitride, ranging from roughly 100 to 300°C. Load deflection measurements using bulk micromachined square and rectangular membranes have shown that Si_xN_y:H thin-films (~300–700 nm) deposited by PECVD have a Young's modulus that increases with increasing deposition temperature, from 79 GPa at 125°C to 151 at 205°C [176]. The residual stresses in these films are below 30 MPa for each deposition temperature.

Table 2.45 Deposition parameters for silicon nitride films deposited by PECVD

References	Sub	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Dep. rate (μm/min)	Thickness (μm)
[177]	Si	300	SiH_4 NH_3	24 72–96	100	0.5–2	0.5–2.6	~0.5
[178]	Si	300	SiH_4 NH_3 N_2	120 75 1200	600	0.85	0.25–0.32	1

2.3.11.2 Process Selection Guidelines

Tables 2.45, 2.46, 2.47, 2.48, and 2.49 summarize the processing recipes and associated mechanical property data for silicon nitride films deposited by PECVD.

2.3.12 PECVD Silicon Germanium

2.3.12.1 Material Properties and Process Generalities

PECVD offers the same advantages to SiGe as it does to Si, SiO_2, and Si_3N_4, namely the ability to deposit the material at much lower deposition temperatures. SiGe is polycrystalline when deposited by PECVD at temperatures as low as 350°C, making

Table 2.46 Mechanical properties of silicon nitride films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[179]	50–300	SiH_4	5	100	0.45	0.5	50–150	–225 to 300
		NH_3	45					
		N_2	100					
[179]	55–330	SiH_4	5	75	0.88	0.7	150	–75 to 375
		NH_3	45					
		N_2	100					
[174]	60	SiH_4 *	1500	HF: 20	0.65			–121 to 36
		NH_3	5	LF: 20				
[180]	125–300	SiH_4		40–200	0.2–0.6	0.6–1.2	106–198	–250 to 250
		NH_3	10					
		N_2	2020					
[174]	300	SiH_4 *	1000	HF: 20	0.65			–850 to 300
		NH_3	20	LF: 20				
[181]	300	SiH_4	9	HF: 5	0.6		152	98
		NH_3	40	LF: 8				
		He	50					
[182]	300	SiH_4	600	100	0.9	0.68	133[a]	178
		N_2	1960					
		NH_3	55					
	300	SiH_4	600	100	0.9	0.68	140[a]	194
		N_2	1960					
		NH_3	55					
[83]	300	SiH_4	01:04.5		12	0.75		706
		NH_3						
[178]	300	SiH_4	120	600	0.85	1		4
		NH_3	75					
		N_2	1200					
[39]	300	SiH_4	15		0.5	0.5	210	110
		N_2	535					
[183]	350	SiH_4	2.4			0.5	112	
		N_2	1500					

*2% in N_2
[a]Plane-strain modulus

it attractive as an alternative structural material to polysilicon for electrostatically actuated MEMS. For SiGe MEMS, PECVD does offer one potential advantage over LPCVD when depositing films at such low temperatures, namely a higher growth rate, which is important for applications requiring film thicknesses in excess of 5 μm. The possible tradeoff for achieving higher growth rates is the increased likelihood that the films will have an amorphous microstructure and contain significantly more hydrogen than their microcrystalline LPCVD counterparts. The vast majority

Table 2.47 Fracture and failure data for silicon nitride films deposited by PECVD

Reference	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Biaxial modulus (GPa)	Residual stress (MPa)	Fracture strength (GPa)
[182]	300	SiH_4	600	100	0.9	0.68	133	178	1.53
		N_2	1960						
		NH_3	55						
	300	SiH_4	600	100	0.9	0.720	140	194	3.08
		N_2	1960						
		NH_3	55						

Table 2.48 Mechanical strain data for silicon nitride films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Strain (10^{-3})	Ultimate strain
[177]	300	SiH_4	24	100	0.5–2	~0.5		–1.59 to 0.38	0.0022
		NH_3	72–96						
[183]	350	SiH_4	2.4			0.5	112	–0.626	
		N_2	1500						

Table 2.49 Hardness data for silicon nitride films deposited by PECVD [180]

Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (mtorr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Hardness (GPa)
125 to 300	SiH_4	1	40–200	2–6	0.58–1.2	106–198	–250 to 250	11.9–22.1
	NH_3	10						
	N_2	2020						

of PECVD processes use SiH_4 and GeH_4 as Si- and C-containing precursors. Like polysilicon, B_2H_6 and PH_3 are common p-type and n-type dopants.

2.3.12.2 Process Selection Guidelines

Tables 2.50, 2.51, 2.52, and 2.53 provide process information and material property data for as-deposited and annealed SiGe films deposited by PECVD.

2.3.12.3 Case Studies

Development of PECVD as an alternative to LPCVD for the production of SiGe films is motivated by the desire to have a process that has reasonably high growth rates at substrate temperatures that are compatible with CMOS processing. LPCVD

Table 2.50 Deposition parameters for silicon germanium films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power density (mW/cm^2)	Pressure (torr)	Dep. rate (nm/min)	Thickness (μm)
[184]	350	SiH_4	0–22	370	1	23 (Ge: 56%)	2
		GeH_4	0–22			21 (Ge: 42%)	
		H_2	2000				
		B_2H_6 (1% in H_2)	10				
[184]	400	SiH_4	0–22			23 (Ge: 67%)	
		GeH_4	0–22			20 (Ge: 48%)	
		H_2	2000				
		B_2H_6 (1% in H_2)	10				
[185]	520–610	SiH_4	42		0.45	48	2–4
		GeH_4	3				

Table 2.51 Mechanical and electrical properties of hydrogenated microcrystalline silicon germanium films deposited by PECVD [186][a]

Temp (°C)	Gas	Gas flow ratio	Power (W)	Dep. rate (nm/min)	Thickness (μm)	Residual stress (MPa)	Resistivity (mΩ cm)
	$H_2/(SiH_4 + GeH_4)$	91					
	$(SiH_4 + GeH_4)/B_2H_6$	233					
300	SiH_4/GeH_4	1.8	203	17	2	–175	75
350	SiH_4/GeH_4	1.8	203	16	1.9	2	18
400	SiH_4/GeH_4	1.5	203	17	2	–9	7
400	SiH_4/GeH_4	1.8	370	23	2	–25	9

[a]Deposition conditions: 1 torr on SiO_2/Si substrates

is typically characterized by low growth rates (~2–30 nm/min for LPCVD SiGe [187]), although the low growth rates are compensated by the large-scale furnaces that can accommodate >50 wafers per run. Nevertheless, growth of film thicknesses beyond 5 μm is not convenient in such systems, especially if low wafer volumes are required. PECVD, on the other hand, can produce films at much higher growth rates, and if substrate heating is used, the as-deposited films can be polycrystalline. Rusu et al. developed a PECVD process for poly-SiC that produces low-stress, high-conductivity polycrystalline films at deposition temperatures <600°C [187]. Specific process details are given in Table 2.51. They found that poly-SiGe films can be deposited directly onto SiO_2 substrate layers without the need of a nucleation

Table 2.52 Mechanical properties of doped silicon germanium films deposited by PECVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Dep. rate (nm/min)	Residual stress (MPa)	Strain gradient ($10^4/\mu m$)
[184]	350	SiH_4	0–22	370[b]	1	23 (Ge: 56%)	48	13.9
		GeH_4	0–22			21 (Ge: 42%)	–238	14
		H_2	2000					
		B_2H_6 (1% in H_2)	10					
[184]	400	SiH_4	0–22	370		23 (Ge: 67%)	25	3
		GeH_4	0–22			20 (Ge: 48%)	–32	6.3
		H_2	2000					
		B_2H_6 (1% in H_2)	10					
[185]	520–610	SiH_4	42		0.45	48	–18 to –225	
		GeH_4	3					
[187]	590	GeH_4	166	30	0.2		79	
		SiH_4	30					
		PH_3 (1% in SiH_4)	80					
[187]	520	GeH_4	166	30	0.2		19	
		SiH_4	30					
		PH_3 (1% in SiH_4)	40					
[187]	590	GeH_4	166	30	0.2		100	
		SiH_4	30					
		B_2H_6 (1% in H_2)	40					

[a]Film thickness range: 2–4 μm
[b]Power density in mW/cm^2

Table 2.53 Mechanical properties of annealed silicon germanium films deposited by PECVD[a]

Reference	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	As-deposited residual stress (MPa)	Postanneal residual stress (MPa)
[185]	520–610	SiH_4 GeH_4	42 3	0.45	1	–18 to –225	200

[a]Film thickness: 2–4 μm

layer, and that the resulting films have moderate to low tensile stresses (<80 MPa). Films doped with PH_3 exhibit a reasonable conductivity (25 mΩ cm) and those doped with boron an even higher conductivity (0.64 mΩ cm). Moreover, films in the 2–10 μm thickness range could easily be deposited using a conventional commercially available PECVD system because the deposition rate is on the order of 200 nm/min.

Extensive work has been performed to use PECVD to lower the deposition temperatures of poly-SiGe to below 500°C. Mehta et al. describe a high growth rate process for poly-SiGe at temperatures on SiO_2 substrates as low as 300°C [188]. The authors used a standard, cold wall parallel plate reactor that can be operated in PECVD or LPCVD mode. To facilitate growth, the authors developed a multilayered process consisting of a thin (∼94 nm) SiGe seed layer deposited by PECVD which serves to promote nucleation of a LPCVD layer which is deposited directly on the seed layer and serves as a crystallization layer for bulk film growth by PECVD at temperatures that would otherwise lead to amorphous films. At 450°C, they were able to deposit a 1 μm thick $Si_{0.35}Ge_{0.65}$ film with an average residual stress of –5 MPa and a resistivity of 0.8–1.2 mΩ cm. The deposition rate at 450°C was 33 nm/min. For 11 μm-thick films produced under the same conditions, the average residual stress was 71 MPa, the average stress gradient was $3.6 \times 10^{-5}/\mu m$ and the resistivity was 0.9 mΩ cm. Films grown at 300°C under roughly the same gas flow and pressure conditions yielded a 2 μm thick film with a residual stress of –175 MPa and a resistivity of 75 mΩ cm. The growth rate was 17 nm/min. In a follow-up effort, this group explored means to reduce the stress gradient in these films and found that for 10 μm thick structures fabricated out of the aforementioned multilayered structure deposited at 450°C, a residual stress of 72 MPa and a stress gradient of 6.5 MPa/μm could be reduced to 57 MPa and 1.6 MPa/μm, respectively by the deposition of a 1.6 μm thick silicon-rich poly-SiGe film as the topmost layer of the structure [189]. Along similar lines, Mehta et al. showed that the seed layer need not be restricted to SiGe material [190]. They showed that a-Si can also be used not only to act as a nucleation surface, but also to provide a stress-compensating layer that reduces the thickness needed in the poly-SiGe capping layer. They were able to produce a 10 μm thick multilayered stack consisting of a thin a-Si seed layer and an 800 nm thick silicon-rich SiGe capping layer with an average stress of

35 MPa, a stress gradient of only $3.6 \times 10^{-6}/\mu m$ and a resistivity of 1.45 mΩ cm. The deposition rate was 90 nm/min.

For structures that suffer from excessive residual stresses and stress gradients in the as-fabricated state, annealing can be used to reduce their effects. However, the temperatures required for effective annealing may defeat the purpose of using the low-temperature deposition processes. To address this limitation, Sedky et al. have explored the use of KrF eximer laser processing for localized annealing of poly-SiGe structures [191]. In this work, films were deposited by PECVD at temperatures at and below 370°C, conditions that yield amorphous films. Laser parameters were selected to induce crystallization while avoiding conditions that would cause void formation due to excessive hydrogen out-diffusion as well as damage to structures beneath the SiGe films. The group found that subjecting a 0.77 μm thick amorphous $Si_{31}Ge_{69}$ film deposited at 300°C to 500 laser pulses at 70 mJ/cm^2 led to a reduction in residual stress from 93 to 48 MPa and the sheet resistance from 450 kΩ/sq to 0.6 Ω/sq. Moreover, a 0.4 μm thick $Si_{71}Ge_{29}$ film subjected to a single laser pulse at 500 mJ/cm^2 was effective at reducing the resistivity of the film from 12 kΩ cm to 1.3 mΩ cm.

2.3.13 PECVD Silicon Carbide

2.3.13.1 Material Properties and Process Generalities

SiC can be deposited at lower temperatures (25–400°C) by PECVD than either LPCVD or APCVD using many of the same precursors (both dual and single). For PECVD SiC films, the most commonly used precursors are SiH_4 and CH_4. The films are amorphous in microstructure and electrically insulating. As-deposited films typically have compressive residual stresses, but these can be converted to tensile stresses upon annealing at temperatures as low as 450°C. The films exhibit a much lower Young's modulus than their high temperature, polycrystalline counterparts, ostensibly due to hydrogen incorporation in the film as well as their amorphous microstructure. Hydrogen incorporation results from the fact that most precursors contain significant amounts of hydrogen. Annealing at 400°C can induce densification in hydrogenated films, and at temperatures above 800°C crystallization can occur. Like most PECVD films, the properties of SiC films deposited by PECVD are heavily dependent on process parameters, especially temperature inasmuch as it plays a key role in governing the amount of hydrogen that may get incorporated into the films.

PECVD SiC films are well suited for applications requiring a chemically resistant material. It has been reported elsewhere [192] that amorphous SiC films deposited by PECVD have an etch rate of <2 nm/h in KOH (33 wt% at 85°C), <2 nm/h in TMAH (25 wt% at 80°C), <1 nm/h in HF (40%) and 90–120 nm/h in HF/HNO_3 (2:5). These etch rates are generally independent of processing conditions as long as the film maintains a Si-to-C ratio of close to unity. Like other properties, the optical bandgap of amorphous SiC ranges between 1.8 and 3 eV depending on deposition conditions [192].

2.3.13.2 Process Selection Guidelines

Tables 2.54 and 2.55 summarize the material properties and associated deposition processes for PECVD SiC films.

2.3.13.3 Case Studies

As mentioned previously, residual stress can be a significant issue with SiC films deposited by PECVD. If the substrate temperature is kept at or below 400°C (the typical high setpoint on substrate heaters in commercial PECVD systems) the resulting films are amorphous and likely hydrogenated. Sarro et al. were among the first to systematically investigate the use of amorphous SiC films deposited by PECVD for micromechanical structures [200]. They used a Novellus Concept One™ PECVD system that was equipped with low- and high-frequency power supplies. The deposition temperature was held constant at 400°C and initial depositions were performed at 2.25 torr, a SiH_4 gas flow of 100 sccm, and a CH_4 gas flow of 300 sccm. The RF power was 1000 W divided equally between the low-frequency and high-frequency supplies. They found that the resulting residual stress was about –600 MPa. Experiments in varying the low-frequency component showed that films with –2 MPa of stress could be deposited with a low-frequency power of 0 W, but at a cost to thickness uniformity and deposition rate. Annealing at 600°C in nitrogen is sufficient to shift the residual stress into the tensile region.

In a follow-on study this group investigated the effect of substrate material on the residual stress in PECVD SiC films [204]. They found that for PECVD SiC films deposited under the same set of conditions, films deposited on thermal oxides had the lowest residual stress (10 MPa), and those deposited on PSG had considerably higher residual stresses, ranging from 169 MPa for a PSG layer with 2% phosphorus to 218 MPa for a PSG layer with 8% phosphorus. Moreover, doped SiC films on thermal oxides had a much higher residual stress than their undoped counterparts, measuring 177 and 367 MPa for phosphorus- and boron-doped SiC, respectively. The same doped films deposited on PSG with 4% phosphorus had residual stresses of 262 and 449 MPa for phosphorus- and boron-doped SiC, respectively.

The relatively low deposition temperatures associated with PECVD SiC make it potentially compatible with non-conventional substrate materials like high temperature polymers. Pakula et al. have recently demonstrated that polyimide PI2610™ can be used as a sacrificial layer to form surface micromachined PECVD SiC structures [199]. PI2610™ was selected because it is spin castable, patternable by plasma etching, and has a glass transition temperature above 400°C. In fact, it can be cured at 400°C. Amorphous SiC films were deposited in a Novellus Concept One™ system at a substrate temperature of 400°C, a SiH_4 flow rate of 250 sccm, a CH_4 flow rate of 3 slm, a pressure of 2 torr, a high-frequency power of 450 W and a low-frequency power of 150 W. Under these conditions, the as-deposited films do not require a postdeposition annealing step for stress relaxation because the average residual stress is 65 MPa. This group was able to demonstrate the utility of this capability by successfully fabricating a surface micromachined capacitive pressure sensor. The advantage that polyimide offers over other viable sacrificial materials

Table 2.54 Mechanical properties of SiC films deposited by PECVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Power (W)	Dep. rate (nm/min)	Young's modulus (GPa)	Residual stress (MPa)	Hardness (GPa)
[193]	200	$C_6H_{18}Si_2$	1000	0.375		53		–500	
	250	Ar				40		–600	
	300					27		–750	
[194]	300	$C_6H_{18}Si_2$					180	–750	
[195]	300	SiH_4	20	1	HF: 300			–450	
		CH_4	400		LF: 300				
[196]	320	SiH_4	3.6		20			–445	
		CH_4	14.0						
[197]	320	SiH_4	3.6				21–36	–93 to –356	
		CH_4	8.4–32.4						
[198]	350	SiH_4 [b]	2840	1.6	HF: 100		56	–80 to 16	8.8
		CH_4	1440		LF: 100–150				
[199][c]	400	SiH_4	250	2	HF: 450			65	
		CH_4	3000		LF: 150				
[200]	400	SiH_4	100	2.25	HF: 500	67		–350	
		CH_4	3000		LF: 500				
[201]	400	SiH_4	70	1.6	HF: 600	180		–5	
[202]		CH_4	500						
		Ar	700						
[203]	350	$(CH_3)_3SiH$ in He	38	160	HF: 400 LF: 100		75	–150	

[a]Film thickness range: 2–4 μm
[b]2% in Ar
[c]Substrate: polyimide

Table 2.55 Electrical properties and chemical resistance of SiC films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Press (torr)	Power (W)	Dep. rate (nm/min)	Thickness (μm)	Resistivity (Ω cm)	Etch rate (nm/h)
[195]	300	SiH_4 CH_4	20 400	1	HF: 300 LF: 300		1	10^7	HF: <1 KOH: 1.3 HF/HNO_3: 10.5
[201] [202]	400	SiH_4 CH_4 Ar	70 500 700	1.6	HF: 600	180	1.8		HF: 1 KOH: 78

such as SiO_2 is that the release step can be performed using an isotropic oxygen plasma, thus enabling the integration of such structures directly onto Si CMOS substrates.

2.3.14 PECVD Carbon-Based Films

2.3.14.1 Material Properties and Process Generalities

Diamondlike carbon films are commonly used in non-MEMS applications requiring materials that can withstand high mechanical wear conditions due to their high hardness properties. DLC is typically deposited by PECVD using a hydrocarbon precursor such as methane. DLC has been used as a structural material in MEMS, but the instances are limited, most likely due to high residual stresses in as-deposited films. DLC is more likely to be used as a protective coating for MEMS components, especially polysilicon actuators subject to mechanical wear [205, 206] and stiction [206] owing to its outstanding tribological properties and relatively benign surface chemistry.

2.3.14.2 Process Selection Guidelines

Table 2.56 summarizes the process-dependent properties of DLC films deposited by PECVD. The body of work in developing PECVD diamondlike carbon films is much more extensive than is represented here because the preponderance of the work has been for applications other than MEMS. The references in Table 2.56 were included in this chapter because they describe the development of DLC specifically for MEMS applications.

Table 2.56 Mechanical properties of diamondlike carbon films deposited by PECVD

References	Gas	Gas flow (sccm)	Power (W)	Bias voltage (V)	Pressure (torr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)
[207]	C_6H_6	na	700	100–500	10	16–133		400–1200
[208]	C_6H_6	na	800	400	10	87		–1300
[209]	CH_4 H_2	14 42	900–1100	375–400	0.02	35	0.12–0.9	–79 to –310

2.4 Epitaxy

2.4.1 Process Overviews

Epitaxy is a special case of thin-film growth where a single-crystalline thin-film is grown upon a single-crystalline substrate such that the crystalline structure of the film is formed using the crystalline structure of the substrate as a template. If the substrate and thin-film are of the same material, the process is known as homoepitaxy. If the substrate and thin film are of different materials, the process is known as heteroepitaxy. Epitaxial processes are not commonly used in Si-based MEMS, perhaps because most MEMS structures simply do not require thin single crystalline structures, and the ones that do can be fabricated using silicon-on-insulator (SOI) substrates. In some material systems, however, epitaxial films are extensively used. These include cubic silicon carbide (3C-SiC) on silicon substrates, III-V compounds on III-V substrates and, to a lesser extent, GaN on silicon substrates. In such cases, the film growth processes very closely resemble those developed for microelectronics where single-crystalline structures are a necessity.

From a first principles perspective, the film-forming mechanism associated with epitaxial growth can be described by a simple two-dimensional (2-D) growth model. Like the 3-D model that describes the formation of polycrystalline and amorphous films, the 2-D model involves the adsorption, surface migration, and reaction of vapor-phase reactants on the substrate surface. For epitaxial growth, this substrate must be single crystalline. Epitaxial growth does not require that the surface be atomically flat, just single crystalline. In fact, all single crystalline substrates are comprised of terraces that form steplike structures on the substrate surface with each terrace being comprised of one or more crystalline planes. It is these terraces that greatly facilitate epitaxial growth. Adsorbed reactants, at this stage of the process known as adatoms, migrate on the surface until they come to the edge of a terrace. Once there, the adatom forms a chemical bond with atoms in its vicinity using the crystalline structure on the surface and the terrace edge as a template. This process continues in a highly controlled manner, adatom by adatom, layer by layer, until the desired film is formed.

From the processing perspective, the epitaxial process must be performed under steady-state conditions, which requires tight control of key process parameters. The key distinguishing feature of the epitaxial process when compared with polycrystalline growth is surface migration of the adatoms. If surface migration is encumbered, then 3-D nucleation and growth is likely to occur, resulting in the formation of a polycrystalline or amorphous film. Encumbrance occurs because the surface lacks sufficient energy to sustain epitaxial growth, and this can occur for a number of reasons including excessive adsorption of reactants on the substrate or insufficient surface energy of the newly formed adatoms. The adsorption rate can be properly controlled by regulating precursor flow rates into the reactor and the adatom surface energy can be maintained by performing the growth process at high temperature. For example, polysilicon films are typically grown at temperatures around 600°C whereas epitaxial silicon films are grown at temperatures in excess of

1000°C. Likewise, poly-SiC films are deposited in the 800–900°C range, whereas epitaxial silicon carbide films are grown at temperatures in excess of 1200°C.

Most epitaxial semiconductor films are grown by a process called vapor phase epitaxy (VPE). VPE is essentially a special form of CVD. VPE can be performed at either low pressures or atmospheric pressure and thus follows the appropriate discussions on the topic as presented in previous sections of this chapter. Because of the high temperatures associated with Si and SiC epitaxy, atmospheric pressure CVD is often employed, although LPCVD can be used enabling epitaxial growth to occur at lower temperatures. VPE also works well for Si and SiC because the gaseous precursors required for film growth are readily available. These include SiH_4 and SiH_2Cl_2 for silicon sources and C_3H_8 for the carbon source. VPE also readily supports in situ doping of Si and SiC using PH_3 and B_2H_6 for silicon epitaxy and NH_3 and trimethyl aluminum ($Al(CH_3)_3$) for SiC.

Non-silicon-containing compound semiconductors, such as the III-V semiconductors can also be epitaxially grown by VPE. Sometimes known as MOCVD, short for metallorganic CVD as a result of the metal containing organic precursors used in the process, the process is commonly used to grow binary, ternary, and quaternary III-V compounds on GaAs and InP substrates. Common precursors include arsine and phosphine in conjunction with metallorganics such as trimethyl aluminum and trimethyl gallium.

Epitaxy is not limited to CVD, in fact, methods based on physical vapor deposition (PVD) are also commonly used to grow binary, ternary, and quaternary III-V compound semiconductors, the most popular being molecular beam epitaxy (MBE). The typical MBE system uses "atomic" or "molecular beams" that are thermally generated from discrete sources which are directed at a heated substrate. The flux of atoms or molecules from each source is regulated by control of the source heater, and the beam can be terminated altogether by shuttering the source. The process is performed in a chamber capable of achieving ultrahigh vacuum conditions (10^{-11} torr) in order to maintain conditions for high-purity epitaxial growth. Growth rates tend to be much lower than for CVD methods, however, complex multilayered ultrathin-film stacks, known as superlattices, can readily be grown using MBE. In addition to III-V based films, MBE can be used to grow epitaxial Si, SiGe, and even 3C-SiC films.

2.4.2 Epi-Polysilicon

2.4.2.1 Material Properties and Process Generalities

Some device designs require polysilicon thicknesses that are not easily achieved using conventional LPCVD. In such instances, epitaxial Si reactors can be used to grow polysilicon films. Unlike conventional LPCVD processes that typically have deposition rates less than 10 nm/min, epitaxial processes have deposition rates on the order of 1 μm/min [210]. The high deposition rates result from the much higher substrate temperatures (>1000°C) and deposition pressures (>50 torr) associated with epitaxial processes. Known as epitaxial polysilicon or simply epi-poly, these

Table 2.57 Deposition conditions and mechanical properties for epi-poly films

References	Temp (°C)	Gas	Gas flow (sccm)	Dep. rate (μm/min)	Thickness (μm)	Fracture strength (GPa)	Residual stress (MPa)	Stress gradient (MPa/μm)
[213]	1000	DCS	750–1050	0.55–0.75	10		–25 to 3	
[211]	1000	DCS	1050	0.5	10	0.76	3	2
		PH_3	5%					
[214]	1000	DCS						
		PH_3	5%		10	1	8	1
[210]	1050	DCS	360	~1	4		Low tensile	
[215]	1080	$SiCl_4$	15 g/min	~1			Low tensile	
		H_2	200 slm					

films exhibit many of the properties associated with LPCVD polysilicon but at much higher thicknesses due to the higher growth rates.

Unfortunately, the high growth temperatures associated with epi-poly generally leads to delamination of the films when SiO_2 is used as a substrate layer. This issue can be addressed by using a thin LPCVD polysilicon film as a seed layer for epi-poly growth. In addition to improving adhesion, the LPCVD polysilicon seed layer is sometimes used in order to control nucleation, grain size, and surface roughness.

As with conventional polysilicon, the microstructure and residual stress of the epi-poly films is related to deposition conditions. Compressive films generally have a mixture of <110> and <311> oriented grains [211, 212] and tensile films have a random mix of <110>, <100>, <111>, and <311> oriented grains [213]. The Young's modulus of epi-poly measured from micromachined test structures is comparable with LPCVD polysilicon [212].

2.4.2.2 Process Selection Guidelines

Details regarding the deposition of epi-poly films can be found in Table 2.57. Annealing is generally not required due to the fact that the films are grown at high substrate temperatures; however, if the films are doped, a postdeposition anneal is sometimes performed. Table 2.58 describes details regarding such anneals.

2.4.2.3 Case Studies

Epi-poly films are deposited at temperatures comparable to thermal oxidation temperatures (>1000°C) which, at first pass, might lead the process engineer to assume that these films should be stable from the perspective of mechanical properties, at elevated temperatures. In an effort to evaluate the compatibility of epi-poly with bipolar and CMOS processing, Gennissen et al. studied the sensitivity of various aspects of epi-poly films to high-temperature processing steps associated with bipolar electronics processing [210]. As with nearly all other reports on epi-poly

Table 2.58 Annealing behavior of $POCL_3$ doped epi-poly films

References	Temp (°C)	Gas	Thickness (μm)	Young's modulus (GPa)	Fracture strength (GPa)	Residual stress (MPa)	Annealing conditions	Stress gradient (MPa/μm)
[212]	1150		11.5	160–167	~1.2	–10	1100°C, 7 h	
[216]	1150	DCS[a]	11				N_2, 1100°C, 7 h O_2 1000°C, 0.5 h	–0.11

[a]DCS: Dichlorosilane (SiH_2Cl_2)

processing, they used a polysilicon seed layer to promote growth of epi-poly on oxide-coated wafers. They found that only thermal oxides were suitable as sacrificial layers for epi-poly processing because LTO and PSG lacked the thermal stability to survive growth even with the LPCVD polysilicon seed layer. They reported that LTO suffers from delamination whereas PSG suffers from outgassing, causing bubbles in the polysilicon layer. As for the high-temperature stability of epi-poly films, specimens subjected to oxidative conditions at high temperature (~1100°C) acquire a high degree of compressive strain relative to unexposed films as well as films exposed to high temperatures in an argon environment. The authors ascribe the increased strain to oxygen diffusion into the epi-poly film. It was shown that a nitride capping layer commonly used in the LOCOS process is sufficient to protect the epi-poly films from the adverse affects of oxidation.

The fact that epi-poly does not readily nucleate on SiO_2 surfaces has recently been exploited in a selective growth process for patterning epi-poly films [215]. The process is simple in concept: namely grow epi-poly films on patterned LPCVD polysilicon seed layers. Nucleation is inhibited in the large oxide field areas between patterned polysilicon structures. The growth rate of epi-poly from the sidewalls of the patterned polysilicon seed layer is approximately equal to the vertical growth rate, resulting in significant widening of the final structure as compared with the seed layer; however, for larger MEMS structures, this can be accounted for during process design and mask development. The selective growth process eliminates the need to use deep reactive ion etching to pattern thick (>15 μm) epi-poly films.

2.4.3 Epitaxial Silicon Carbide

2.4.3.1 Material Properties and Process Generalities

SiC thin films can be grown or deposited using a number of different techniques. For high-quality single-crystal films, APCVD and LPCVD processes are most commonly employed. Homoepitaxial growth of 4H- and 6H-SiC yields high-quality films suitable for microelectronic applications but typically only on substrates of the

same polytype. These processes usually employ dual precursors, such as SiH_4 and C_3H_8, and are performed at temperatures ranging from 1500 to 1700°C. Epitaxial films with p-type or n-type conductivity can be grown using aluminum and boron for p-type films and nitrogen and phosphorus for n-type films. Nitrogen is so effective at modifying the conductivity of SiC that growth of undoped SiC films is extremely challenging because the concentrations of residual nitrogen in typical deposition systems are sufficient for n-type doping.

APCVD and LPCVD can also be used to deposit 3C-SiC on Si substrates. Heteroepitaxy is possible despite a 20% lattice mismatch because 3C-SiC and Si have the same lattice structure. The growth process involves two key steps. The first step, called carbonization, converts the near surface region of the Si substrate to 3C-SiC by simply exposing it to a hydrocarbon/hydrogen mixture at high substrate temperatures (>1200°C). The carbonized layer forms a crystalline template on which a 3C-SiC film can be grown by adding a silicon-containing gas to the hydrogen/hydrocarbon mix. The lattice mismatch between Si and 3C-SiC results in the formation of crystalline defects in the 3C-SiC film, with the density being highest in the carbonization layer and decreasing with increasing thickness. The crystal quality of 3C-SiC films is nowhere near that of epitaxially grown 4H- and 6H-SiC films; however, the fact that 3C-SiC can be grown on Si substrates enables the use of Si bulk micromachining techniques to fabricate a host of 3C-SiC-based mechanical devices including microfabricated piezoresistive pressure sensors [217]. For designs that require electrical isolation from the substrate, 3C-SiC devices can be made directly on SOI substrates [218] or by wafer bonding and etchback, such as the capacitive pressure sensor developed by Young et al. [219]. High-quality 3C-SiC films can be grown on Si substrates by molecular beam epitaxy [220], although the process is much less commonly used than APCVD or LPCVD.

The mechanical properties of 3C-SiC are of particular interest to the MEMS community due to their potential in applications requiring a structural material with a high Young's modulus. Owing to its compatibility with silicon micromachining, structures to evaluate the mechanical properties of epitaxial 3C-SiC films, such as micromachined membranes and cantilever beams, can easily be fabricated using a combination of SiC reactive ion etching and Si bulk micromachining. Reported values of Young's modulus for 3C-SiC films vary significantly, from a low of 330 GPa [221] to a high of 694 GPa [222] for 2.7 and 10 μm thick undoped films, respectively. At present, it is not clear if or how the high defect density at the 3C-SiC/Si interface affects these measured values.

2.4.3.2 Process Selection Guidelines

Tables 2.59 and 2.60 summarize the processing data and mechanical properties measurements for epitaxial 3C-SiC films grown by APCVD and LPCVD, respectively.

2.4.3.3 Case Studies

It is generally believed that 3C-SiC films epitaxially grown on Si wafers using the conventional carbonization-based growth process will have tensile residual stresses

Table 2.59 Epitaxial growth conditions and mechanical properties of APCVD 3C-SiC films

References	Temp (°C)	Gas	Gas flow (sccm)	Thickness (μm)	Young's modulus (GPa)	Tensile strength	Residual stress (MPa)
[223]	1280	C_3H_8 (15% in H_2)	26	0.5–2	424	1.65	
		SiH_4 (5% in H_2)	102				
		H_2	25,000				
[224]	1350	C_3H_8	10	3.2			549–639
		SiH_4	1				
		H_2	10,000				
[225]		C_3H_8 (15% in H_2)	26	2	407		275
		SiH_4 (5% in H_2)	102				
		H_2	25,000				

Table 2.60 Epitaxial growth conditions and mechanical properties of LPCVD 3C-SiC films

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Young's modulus (GPa)	Residual stress (MPa)
[132]	1350	SiH_4	$Si/H_2 = 0.024\%$	300	446	
		C_3H_8	$C/Si = 0.8 - 1$			
		H_2 (98% in Ar)				
[226]	1350	SiH_4 (10% in H_2)	270	400		215–450
		C_3H_8	8			
		H_2	10,000			
[227]	1380	C_3H_8	8	100	430	265
		SiH_4 (10% in H_2)	270			
		H_2	30,000			

in the 200–400 MPa range due to the thermal and lattice mismatches between the film and the substrate. Gourbeyre et al. have shown that the conditions used during the carbonization step play a key role in determining the residual stress in the films [224]. Carbonization is usually initiated by exposing the substrate to the carbonizing precursor at relatively low temperatures (<500°C) then ramping up the substrate temperature to the carbonization/epitaxial growth temperature (>1200°C). They found that the stress in the epitaxial film could be made either tensile or compressive by (1) utilizing a three-step process that decouples the carbonization and epitaxial growth temperatures and (2) properly selecting the temperature at which the carbonization precursor is injected into the reactor. For instance, they found that compressive films are grown when the carbonization precursor is introduced at a substrate temperature of 300°C, carbonization is performed at 1150°C and epitaxial growth at 1350°C, whereas tensile films are grown when the introduction temperature is equal to or greater than 1150°C and carbonization temperature is also equal

to or greater than 1150°C. Using this knowledge, the authors were able to fabricate a freestanding 3C-SiC membrane with a tensile stress of 157 MPa.

2.4.4 III-V Materials and Gallium Nitride

2.4.4.1 Material Properties and Process Generalities

Gallium arsenide (GaAs), indium phosphide (InP) and related III-V compounds have favorable piezoelectric and optoelectric properties, high piezoresistive constants and wide electronic bandgaps relative to Si, making them attractive for various sensor and optoelectronic applications. Like Si, GaAs, and InP substrates are commercially available as high-quality, single-crystal wafers. In addition to the commonly known binary compounds, III-V materials can be deposited as ternary and quaternary alloys with lattice constants that closely match the binary compounds from which they are derived (i.e., $Al_xGa_{1-x}As$ and GaAs), thus permitting the fabrication of a wide variety of heterostructures that facilitate device performance.

GaAs has a zinc blend crystal structure with an electronic bandgap of 1.4 eV, enabling GaAs electronic devices to function at temperatures as high as 350°C [228]. High-quality, single-crystal GaAs wafers are widely available, as are well-developed MOCVD and MBE growth processes for epitaxial layers. Because the epitaxial growth processes used in the fabrication of III-V MEMS come directly from the electronic device industry, the MEMS literature lacks publications that link thin-film deposition details to material properties. Nevertheless, Table 2.61 summarizes important material properties of III-V compounds as measured using MEMS devices.

Interest in gallium nitride (GaN) as a material for MEMS has recently emerged, due to its large bandgap (~3.5 eV), its piezoelectric properties, and compatibility with 6H-SiC and (111) Si substrates. Epitaxial GaN films can be deposited on both substrate materials using AlN as an intermediate buffer layer. Development of this material is still in its early stage so data pertaining to its mechanical properties are sparse. Table 2.62 summarizes the mechanical properties of epitaxial GaN thin-films as measured using MEMS structures.

2.4.4.2 Process Selection Guidelines

Tables 2.61 and 2.62 detail deposition processes and associated material properties for III-V and GaN films developed specifically for MEMS applications.

2.4.4.3 Case Studies

Micromachining of GaAs is relatively straightforward, because many of the ternary and quaternary alloys used for epitaxial growth have sufficiently different chemical properties to allow their use as sacrificial layers [238]. For example, a commonly

Table 2.61 Mechanical properties of selected III-V semiconductors

References	Material	Substrate	Thickness (μm)	Young's modulus (GPa)	Fracture stress (GPa)	Residual stress (MPa)	Stress gradient (MPa/μm)
[229]	$Al_{0.3}Ga_{0.7}As$ $Al_{0.6}Ga_{0.4}As$	GaAs		107	0.75–1.25		
[230]	InP	$In_{0.53}Ga_{0.47}As$	1.7	82		–5.6	[a]
[231][b]	InP	InGaAs/InP				–100	
[232]	InP	InGaAs/InP					16.32
[233]	InP	$Ga_{0.47}In_{0.53}As$/InP	0.018				~200
			0.035				~100
			0.053				~–100
			0.070				~–150
			0.105				~–200
[234]		InGaAs/InP	1	~80			

[a] This sample exhibited a strain gradient of $4.37 \times 10^{-5}/\mu m$
[b] This sample was bonded to a SiO_2 coated Si wafer for micromachining

Table 2.62 Deposition conditions and mechanical properties of GaN films

References	Substrate	Method	Temp (°C)	Gas	Gas flow (μmol/min)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[235]	AlGaN/Si	MBE	800				0.5–1[a]	280	
[236]	AlN/SOI	CVD	1000	TMG[b]	150	100	1.7		440–530
[237]	AlN/Si			NH_3 H_2	0.45				810

[a]AlGaN buffer layer thickness = 20 nm
[b]TMG: Trimethyl gallium: ($Ga(CH_3)_3$)

used ternary alloy for GaAs is $Al_xGa_{1-x}As$. For values of x less than or equal to 0.5, etchants containing mixtures of HF and H_2O will remove $Al_xGa_{1-x}As$ without attacking GaAs, whereas etchants containing NH_4OH and H_2O_2 attack GaAs isotropically but do not etch $Al_xGa_{1-x}As$. This selectivity enables the micromachining of GaAs using lattice-matched etch stops and sacrificial layers. GaAs cantilevered structures have also been fabricated on Si wafers [239]. The process involves the growth of a 40 nm thick buffer layer of heteroepitaxial GaAs at 400°C on a (100) Si wafer that was deoxidized in H_2 at 950°C followed by exposure to AsH_3 during the cool-down step once the temperature reaches 850°C. After the buffer layer is grown, the main structural film is grown at 640°C. The GaAs multilayer is patterned using a $HBr:CH_3COOH:K_2Cr_2O_7$ solution at a ratio of 1:1:1. Devices are released by etching the underlying Si wafer in 30% KOH at 60°C. The fracture stress of these structures was measured to be ~1.5 GPa.

Many of the properties of InP are similar to GaAs in terms of crystal structure, mechanical stiffness, and hardness; however, the optical properties of InP make it particularly attractive for micro-optomechanical devices to be used in the 1.3–1.55 μm wavelength range. Micromachining of InP follows closely that used for GaAs. Like GaAs, single-crystal wafers of InP are readily available and ternary and quaternary lattice-matched alloys, such as InGaAs, InAlAs, InGaAsP, and InGaAlAs, can be used as either etch stop and/or sacrificial layers depending on the etch chemistry [238]. InP thin-films, for example, deposited on $In_{0.53}Al_{0.47}As$ sacrificial layers can be released using etchants containing $C_6H_8O_7$, H_2O_2, and H_2O. In addition, InP films and substrates can be etched in solutions containing HCl and H_2O using $In_{0.53}Ga_{0.47}As$ films as etch stops. InP cantilevers have even been fabricated on Si substrates [240]. The process involves epitaxial growth of InP on (100) Si wafers by MOCVD, followed by patterning of the InP thin-film into cantilevers using a 1:1 solution of HCl and H_3PO_4. The cantilevers are released by selectively etching the Si substrate in a 30% KOH solution at 60°C. The resulting structure is an InP cantilever with a large Si proof mass near its end. The structure was used to study the fracture characteristics of the InP films.

Indium arsenide (InAs) can also be micromachined into device structures. Despite a 7% lattice mismatch between InAs and (111) GaAs, high-quality epitaxial layers can be grown on GaAs substrates. Yamaguchi et al. developed a process to fabricate very thin conductive membranes of InAs on GaAs substrates [241]. Thin InAs films were grown directly on GaAs substrates by MBE and etched using a

solution containing H_2O, H_2O_2, and H_2SO_4. The structures were released by etching the GaAs substrate using a $H_2O/H_2O_2/NH_4OH$ solution. InAs cantilevers have also been fabricated on GaAs using a $Al_{0.5}Ga_{0.5}Sb$ sacrificial layer [242].

Ternary compounds have also recently been utilized in MEMS structures. For example disk-type microresonators based on epitaxial AlGaAs films have been fabricated [243]. The resonator consists of a surface-micromachined disk that is tethered to the substrate by four supporting beams. The disk is made from a Si-doped $Al_{0.3}Ga_{0.7}As$ layer that clads an undoped $Al_{0.3}Ga_{0.7}As$ layer. This three-layer stack is grown on a sacrificial $Al_{0.7}Ga_{0.3}As$ layer that is epitaxially grown on a commercially available GaAs wafer. The resonator is patterned by reactive ion etching and the device is released in HF.

2.5 Physical Vapor Deposition

2.5.1 Process Overviews

Physical vapor deposition (PVD) is a process by which a physical mechanism is the primary means by which a film-producing vapor is generated (in contrast to CVD where gaseous chemical precursors are used). The most common physical processes include sputtering and thermal evaporation, although alternative methods such as laser ablation are emerging for niche applications. As compared to CVD, PVD is not commonly used to deposit semiconductors and dielectrics for MEMS, although enough examples can be found in the literature to warrant inclusion in this chapter. For a detailed description of PVD, the reader is directed to [1–3].

Thermal evaporation is one of the oldest and most mature vacuum deposition methods. This technique involves the creation of the physical vapor by heating the source material. For materials with relatively low melting temperatures (i.e., polymers and metals such as Al), the source material can be heated using a simple resistive heater such as a tungsten filament. For materials with high melting temperatures (i.e., compounds and metals such as Pt), heating is by electron bombardment. Evaporation is generally performed under high vacuum conditions to ensure chemical purity of the as-deposited film and to minimize gas phase collisions that could lower the kinetic energy of the vapor. Deposition generally does not conform to complex topographies. For MEMS applications, deposition of semiconductors and dielectrics by evaporation is not commonly performed and thus is not reviewed in this chapter.

Sputtering uses ion bombardment of a solid target to generate the physical vapor. Argon gas is commonly used as the ion source because it is relatively easy to ionize, has a relatively high mass, and is chemically inert. The ion beam has an average energy in the keV range, which is sufficient to liberate atoms from most target materials. If the target material is electrically conductive, then a DC bias can be used to accelerate the Ar ions to the target. In contrast, if the material is electrically insulating, an RF bias is required to suppress charge buildup on the target surface.

Elemental semiconductors such as silicon and heavily doped wide-bandgap semiconductors such as SiC can be deposited by DC sputtering. Insulators such as silicon dioxide and undoped SiC can be deposited from targets of the same material by RF sputtering, which serves to suppress charging of the insulating targets. Alternatively, these compounds can be deposited by reactive sputtering, which involves DC sputtering of a Si target in the presence of a reactive gas. For example, sputtering a Si target using methane as the sputtering gas will yield a SiC thin-film. Sputtering is generally performed under high vacuum conditions to ensure chemical purity of the as-deposited film and to minimize gas phase collisions that could lower the kinetic energy of the vapor, although the vacuum conditions tend to be less stringent than for evaporation.

For some materials such as carbon, alternative techniques have been developed, the most notable being pulsed laser deposition. Instead of bombarding a target with an ion beam, laser illumination using extremely short laser pulses (~ns) is instead used. The incident radiation is absorbed in the near surface region of the target, resulting in highly localized heating and vaporation of target material. Process control is achieved through the laser pulse length, pulse repetition rate, and substrate heating. This approach enables the process to be performed at lower vacuum levels than conventional PVD because a sputtering gas is not required. The technique is not well suited for producing thick films, but can be used to produce thin-films such as those to be used as protective coatings.

2.5.2 Sputter-Deposited Si

2.5.2.1 Material Properties and Process Generalities

PVD techniques have been developed to produce Si thin films [244, 245] as a low temperature alternative to LPCVD polysilicon and PECVD amorphous silicon. Abe and Reed showed that sputtering could be used to deposit very smooth (2.5 nm) polysilicon films on thermally oxidized wafers at reasonable deposition rates and with low residual compressive stresses [244]. The process involved DC magnetron sputtering from a Si target using an Ar sputtering gas, a chamber pressure of 5 mtorr, and a power of 100 W. The authors reported that a postdeposition anneal at 700°C in N_2 for 2 h was needed to crystallize the deposited film and perhaps lower the stress. Honer and Kovacs developed a polymer-friendly, Si-based surface micromachining process based on polysilicon sputtered onto polyimide and PSG sacrificial layers [245]. To improve the conductivity of the micromachined Si structures, the sputtered Si films were sandwiched between two TiW cladding layers. Devices fabricated on polyimide sacrificial layers were released using oxygen plasma etching. The processing step with the highest temperature was in fact, the polyimide cure at 350°C. To test the robustness of the process, sputter-deposited Si microstructures were fabricated on substrates containing CMOS devices. As expected, the authors reported no measurable degradation of device performance. Pal and Chandra found that sputtered Si films deposited at a substrate temperature of ~250°C are amorphous

Table 2.63 Deposition conditions and material properties of Si films deposited by sputtering[a]

Reference	Substrate	Power (kW)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Resistivity (MΩ/sq)
[245]	Si	1.5	8	23		34	
	Si	1.5	14	19		141	
	PSG	1.5	8	23		97	
	PSG	1.5	14	19		106	
	Al/Si	1.5	8	23		31	
	Al/Si	1.5	14	19		109	
	Si	2.5	8	37		–22	
	Si	2.5	14	30		164	
	PSG	2.5	8	37		27	
	PSG	2.5	14	30		13	
	Al/Si	2.5	8	37		–16	
		2.0	9.5		600	~90	50
			9.5		2000	~98	20
			9.5		5000	~105	7

[a]Deposition temperature: room temperature

Table 2.64 Mechanical and electrical properties of annealed Si films deposited by sputtering

References	Power (kW)	Pressure (mtorr)	Thickness (nm)	Annealing temp (°C)	Residual stress (MPa)	Resistivity (MΩ/sq)	Strain (10^{-5})
[245]	2.0	9.5	600	350	95	125	
		9.5	2000		68	20	
		9.5	5000		70	6	
[244]	0.10	5		700			–5.6 ×

and that an annealing temperature of 800°C is required to induce crystallization [246].

2.5.2.2 Process Selection Guidelines

Table 2.63 details the various processes used to produce sputter-deposited Si films for MEMS applications and Table 2.64 describes the mechanical and electrical properties of sputter-deposited Si films after annealing.

2.5.3 Sputter-Deposited SiC

Sputtering can be used to deposit SiC films on temperature-sensitive substrates. In fact, sputtering is able to produce SiC films at temperatures as low as 25°C. Sputtered SiC films can be deposited by RF magnetron sputtering of a SiC target

[247] or by dual source DC magnetron sputtering of Si and graphite targets [248]. In both cases, the films are amorphous in microstructure and electrically insulating. Because the process does not involve hydrogen-containing precursors, the films consist only of Si and C.

Ledermann et al. developed a process to deposit low-stress (100 MPa), chemically resistant amorphous SiC films by RF magnetron sputtering [247]. Processing details are provided in Table 2.65. The sputtering target was an unspecified stoichiometric SiC target. Argon was used as the sputtering gas. The residual stresses in as-deposited films ranged from moderately tensile to highly compressive dependent on deposition conditions, in particular, chamber pressure, cathode power, and substrate bias [247]. These films retain excellent chemical durability as no degradation was observed in these films when exposed to a 40% KOH solution at 80°C.

Table 2.65 Mechanical properties of SiC films deposited by sputtering

References	Substrate	Temp (°C)	Power (kW)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Hardness (GPa)
[247]	Si, SiO_2	RT	0.05–0.3	4–31.95	5–20		100 to –1400	
[248]	Si, glass	RT	0.2	2.25–7.5		100–2000	–61 to 210	18

Inoue et al. developed a sputtering process for SiC films using a dual source approach [248]. In their approach, pure Si (99.999%) and graphite (99.999%) targets were sputtered using ultrahigh-purity Ar gas. Process details are provided in Table 2.65. They found that 2 μm thick films with tensile stresses of nominally 130 MPa could readily be deposited with 50 W of power on the Si cathode and 200 W of power on the graphite cathode. Free-standing membranes of only 100 nm in thickness and suitable for X-ray soft filters were fabricated from these films.

2.5.4 Sputter-Deposited SiO_2

Sputtered SiO_2 films are much like their PECVD counterparts in that they are electrically insulating and amorphous in microstructure. Like sputtered SiC, the deposition temperatures can be as low as 25°C, making them very attractive for backend processes. Residual stresses in as-deposited films can be both compressive and tensile, although the tensile stresses can be excessive. Bhatt and Chandra [249] have developed a sputtering process suitable for the production of micromachined SiO_2 structures. Their process involves RF sputtering of a SiO_2 target at substrate temperatures below 285°C. In fact, no substrate heating was used, but the authors measured a maximum substrate temperature of 285°C during the deposition process. Etch rates of the sputtered SiO_2 films depended on RF power and chamber pressure. It was found that the etch rates in buffered HF ranged from roughly 130 to 750 nm/min. The etch rates in KOH ranged from 3.5 to 5.0 nm/min whereas

that in EPW ranged from 0.25 to 0.6 nm/min. For comparison purposes, the authors reported the etch rates of thermal oxide in equivalent buffered HF, KOH, and EPW solutions to be 110, 3, and 0.2 nm/min, respectively. The authors found that the films were sufficiently mechanically and chemically stable to serve as masking layers for boron diffusion performed at 1050°C. The sputtered films were successfully used as interface layers in Si-to-Si wafer bonding, and free-standing cantilevers and micro-bridges could be fabricated by surface and bulk micromachining. In the case of the cantilevers, a thin ZnO film was used as the sacrificial layer. Table 2.66 provides process details for the sputtered SiO_2 films in [249].

Table 2.66 Deposition conditions and properties of silicon dioxide films deposited by sputtering [249]

Substrate	Temp (°C)	Power (kW)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Surface roughness (nm)
Si, quartz	25–285	0.1– 0.3	5–20	40–180	500	–90 to 3000	0.2–3.6

2.5.5 Sputter-Deposited Diamondlike Carbon

Sputter deposition of carbon films is not commonly used in MEMS fabrication but can be performed if films with high hardness and moderate resistivity are required. The films have a much lower Young's modulus value than polycrystalline diamond, but they can be deposited at much lower deposition temperatures. Unfortunately, residual stresses in these films are excessive thus limiting their utility. Table 2.67 summarizes the deposition conditions and observed mechanical properties for a DLC film developed for MEMS applications.

Table 2.67 Deposition conditions and properties of diamondlike carbon films deposited by sputtering[a] [250]

Temp (°C)	Power (kW)	Pressure (torr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Young's modulus (GPa	Resistivity (Ω cm)	Hardness (GPa)
100	1.5	3.75	5–20	500	2000	200	0.2	30

[a] Gauge Factor = 20

2.5.6 Carbon Films Deposited by Pulsed Laser Deposition

Pulsed laser deposition is an alternative deposition method to CVD-based techniques for diamond MEMS. The process is performed in a high vacuum chamber and uses a pulsed eximer laser to ablate a pyrolytic graphite target. Material from

the ejection plume deposits on a substrate, which is kept at room temperature. Background gases composed of N_2, H_2, and Ar can be introduced to adjust the deposition pressure and film properties. The as-deposited films consist of tetrahedrally bonded carbon that is amorphous in microstructure, hence the name amorphous diamond. Nominally stress-free films can be deposited by proper selection of deposition parameters [251] or by a short postdeposition annealing step [252]. The amorphous diamond films exhibit many of the properties of single-crystal diamond, such as a high hardness (88 GPa) a high Young's modulus (1100 GPa), and chemical inertness. Surface micromachined structures can be fabricated using these films; in part because the films can readily be deposited in oxide sacrificial layers and can be etched in an oxygen plasma. Cho et al. report a Young's modulus of 759 GPa and a tensile strength of 7.3 GPa for carbon films deposited by KrF eximer laser PLD [253]. Table 2.68 details the mechanical properties of diamondlike carbon films deposited by PLD for MEMS applications

Table 2.68 Mechanical properties of diamondlike carbon films deposited by pulsed laser deposition[a,b]

References	Target	Power (J/cm^2)	Pressure (μtorr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Hardness (GPa)
[251]	Graphite		1	759	7.3		
[252]	Graphite	>100		550		<–200	80

[a]Deposition conditions: Kr eximer laser
[b]Film thickness range: $1-2\,\mu m$

2.6 Atomic Layer Deposition

2.6.1 Process Overview

Atomic layer deposition (ALD) is a variant of CVD where compound materials, typically binary compounds, are formed on a substrate surface by sequential exposure to two highly reactive vapor-phase chemical precursors. Unlike the formation of compounds by conventional CVD where the precursors are introduced to the reaction chamber en masse and film growth occurs simultaneously, in ALD, the substrate is exposed to only one precursor at any given moment. The exposure periods are kept intentionally short so that submonolayer coatings of the adsorbed precursor are formed on the substrate. The two precursors are selected such that they have a high reactivity with each other. The process involves exposure of the substrate to the first precursor, which contains one component of the binary compound, followed by exposure to the second precursor, which contains the second component. Reaction of the first component with the second results in the formation of the desired material as well as the desorption of unwanted by-products. Deposition rates are often

expressed in terms of nm/cycle, where one cycle is complete after the two precursors have reacted following the second exposure period. In between each exposure period, the reaction chamber is purged of chemical precursors to inhibit gas phase reactions. The amount of precursor introduced into the reaction chamber is highly regulated to ensure that the surface reactions are self-limiting and that both precursors are fully reacted in one deposition cycle. ALD is particularly well suited for depositing metal oxide thin-films because many are contained in reactive metallorganic precursors which readily react with oxidants such as water vapor to form metal oxide. ALD is becoming increasingly popular in the development of next generation MOS-based ICs where alternative dielectrics to SiO_2 are being developed. For MEMS applications, the most common material is Al_2O_3, due in large measure to its convenient metallorganic precursor (trimethyl aluminum) combined with the fact that aluminum oxide can easily be formed by reaction of this precursor with water vapor at relatively low temperature.

2.6.2 Process Selection Guidelines and Material Properties

ALD is a relatively new deposition technique that has not yet found widespread use in MEMS technology due to the ultrathin-films that are typically produced by this method. However, the very high degree of conformality associated with the technique combined with the fact that metal oxides such as alumina are highly durable from both chemical and mechanical perspectives make it extremely attractive as a method to apply thin protective coatings on prefabricated MEMS components. Hoivik et al. showed that alumina films deposited by ALD can overcoat all exposed surfaces of a released surface micromachined polysilicon cantilever, albeit with a small variation in thickness between the top and bottom surfaces of the beam [254]. Yang and Kang investigated the chemical durability of ALD alumina films in aqueous and vapor phase HF and found that the films were much more chemically stable when exposed to vapor phase HF than when exposed to aqueous solutions [255]. As development of ALD is in its early stages relative to alternative deposition methods, much is yet to be learned about the MEMS-centric process-related properties of the as-deposited films. Tables 2.69, 2.70, 2.71, and 2.72 summarize much of what has been reported in the literature on the topic.

In addition to the deposition of metal oxides, ALD can also be used to deposit thin single-crystalline films. Known as atomic layer epitaxy, or ALE, this technique is not commonly used in MEMS due in large part to competing methods that are much better suited for producing films thick enough for most MEMS applications. In the case of silicon carbide, however, there is one example in the literature where ALE was used to grow single-crystalline 3C-SiC films for MEMS. Table 2.73 summarizes the findings of this study.

Tables 2.69, 2.70, and 2.71 detail processing conditions and resulting material properties for Al_2O_3 films deposited by ALD. Table 2.73 describes the mechanical properties of ZnO films deposited by ALD and Table 2.73 lists the measured mechanical properties of 3C-SiC films grown by ALE.

Table 2.69 Friction properties of Al_2O_3 films deposited by atomic layer deposition

References	Temp (°C)	Gas	Gas flow Cycle (s)	Pressure (torr)	Dep. rate (nm/cycle)	Thickness (nm)	Coefficient of friction
[256]	168	TMA[a]	1	1	0.101	10	0.3
		H_2O	1				
		N_2	5				
[257]	300–350	WF_6	2	2		10–30	0.008 on SiO_2
		H_2S	2				0.047 on Ni
		N_2	5				

[a]TMA: trimethyl aluminum: ($Al(CH_3)_3$)

Table 2.70 Mechanical properties of Al_2O_3 films deposited by atomic layer deposition

References	Temp (°C)	Gas	Gas flow cycle	Pressure (torr)	Dep. rate (nm/cycle)	Thickness (nm)	Young's modulus (GPa)	Hardness (GPa)	Residual stress (MPa)
[258]	100	TMA[a]	28 s		10		150	8.1	
		H_2O							
		N_2							
	177	TMA	12 s		12		180	12	
		H_2O							
		N_2							
[259]	130	TMA	na			80			258
		H_2O	na						
		N_2	na						
[260]	177	TMA	1 s	1		100–300	168–182		383–474
		H_2O	1 s						
		N_2	5 s						

[a]TMA: trimethyl aluminum: ($Al(CH_3)_3$)

Table 2.71 Electrical properties of Al_2O_3 films deposited by atomic layer deposition

Reference	Temp (°C)	Gas	Gas flow Cycle (s)	Dep. rate (nm/cycle)	Young's modulus (GPa)	Hardness (GPa)	Dielectric constant	Resistivity (Ω cm)
[258]	100	TMA[a]	28	10	150	8.1	6.8	10^{16}
		H_2O						
		N_2						
	177	TMA	12	12	180	12	6.8	10^{16}
		H_2O						
		N_2						

[a]TMA: trimethyl aluminum: ($Al(CH_3)_3$)

2.7 Spin-On Films

Spin-on dielectrics, such as siloxane-based spin-on glass (SOG), have become a mainstay material of backend processing in IC fabrication because the material can be conveniently deposited and processed at reasonable temperatures, and it retains acceptable dielectric properties for surface passivation and mechanical protection of electronic interconnects. SOG is also attractive for MEMS applications because it

Table 2.72 Mechanical properties of ZnO films deposited by atomic layer deposition

Reference	Temp (°C)	Gas	Flow cycle (s)	Pressure (torr)	Dep. rate (nm/cycle)	Thickness (nm)	Young's modulus (GPa)	Hardness (GPa)	Residual stress (MPa)
[258]	100	DEZ[a] H_2O N_2	28		19		134	6	
	177	DEZ H_2O N_2	12		20		143	9	

[a]DEZ: diethylzinc: ($Zn(CH_2CH_3)_2$)

Table 2.73 Mechanical properties of 3C-SiC films grown by atomic layer epitaxy[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Resistivity (Ω cm)
[117] [118]	1050	SiH_2Cl_2 C_2H_2	10 10	0.15	0.7–2	347	100–200	0.2

[a]The cycle time per precursor is 5 s. The purge period is 3 s. The growth rate per cycle is 0.9 nm

offers the opportunity to create thick oxide structures that would otherwise be difficult to realize using CVD or PVD methods. Processing of SOG basically involves spin casting the precursor in much the same manner as photoresist is cast, followed by a series of postdeposition thermal bakes. Although the processing conditions vary depending on the source of SOG, the following sequence is representative of a common SOG known as Honeywell Accuglass 512B^{TM} [261].

1. Clean the silicon substrate by immersion for 2 min in a H_2SO_4 and 30% H_2O_2 solution mixed to a 7-to-3 ratio and heated to 120°C.
2. Dip the silicon substrate in a 2.5% HF solution for 2 min.
3. Apply the SOG by spin coating at a rate of 3000 rpm for 10 s.
4. Subject the substrate to a bake at 80°C for 1 min
5. Subject the substrate to a bake at 150°C for 1 min
6. Subject the substrate to a bake at 250°C for 1 min
7. Subject the substrate to a final curing bake at 425°C for 30 min in a flow of N_2 at 1 slm.

In addition to its principle function as a low-temperature material for electrical isolation, SOG has been used in situations where thick sacrificial layers are required. For instance, SOG has been used as a thick film sacrificial molding material to pattern thick polysilicon films [262]. In this example, 20 μm thick SOG films were patterned into molds and filled with 10 μm thick LPCVD polysilicon films, planarized by selective CMP, and subsequently dissolved in a wet etchant containing HCl, HF, and H_2O to reveal the patterned polysilicon structures. The cured SOG films were completely compatible with the LPCVD process and posed

no contamination risk. SOG has also been used as a structural material in high-aspect-ratio channel plate microstructures [263]. Electroplated nickel (Ni) was used as a molding material, with the Ni channel plate molds fabricated using a conventional LIGA process. The Ni molds were then filled with SOG, and the sacrificial Ni molds were removed in a reverse electroplating process. In this case, the fabricated SOG structures were over 100 μm tall by virtue of the LIGA patterned Ni molds.

Casting processes are not limited to SOG; in fact, SiC-based structures have been fabricated using polymer precursors in conjunction with micromolding [264]. This technique uses SU-8 photoresists for the molds. Detailed later in this book, SU-8 is a versatile photodefinable polymer in which thick films (hundreds of microns) can be patterned using conventional UV photolithographic techniques. After patterning, the molds are filled with the SiCN-containing polymer precursor, lightly polished, and then subjected to a multistep heat-treating process. During the thermal processing steps, the SU-8 mold thermally decomposes and the SiCN structure is released. The resulting SiCN structures retain many of the mechanical and chemical properties of stoichiometric SiC.

References

1. J.D. Plummer, M.D. Deal, P.B. Griffin: Silicon VLSI Technology: Fundamentals, Practice and Modeling (Prentice Hall, New York, NY, 2000)
2. S. Wolf, R.N. Tauber: Silicon Processing for the VSLI Era (Lattice Press, Sunset Beach, CA, 1987)
3. M. Madou: Fundamentals of Microfabrication (CRC Press, Boca Raton, FL, 1997)
4. Y. Song, S. Dhar, L.C. Feldman, G. Chung, J.R. Williams: Modified deal grove model for the thermal oxidation of silicon carbide, J. Appl. Phys. 95, 4953–4957 (2004)
5. J. Leconte, F. Iker, S. Jorez, N. Andre, J. Proost, T. Pardoen, D. Flandre, J.P. Raskin: Thin films stress extraction using micromachined structures and wafer curvature measurements, Microelectron. Eng. 76, 219–226 (2004)
6. J. Yang, J. Gaspar, O. Paul: Fracture properties of LPCVD silicon nitride and thermally grown silicon oxide thin films from the load-deflection of long Si_3N_4 and SiO_2/Si_3N_4 diaphragms, J. Microelectromech. Syst. 17, 1120–1134 (2008)
7. T.A. Desai, D.J. Hansford, L. Kulinsky, A.H. Nashat, G. Rasi, J. Tu, Y. Wang, M. Zhang, M. Ferrari: Nanopore technology for biomedical applications, Biomed. Microdev. 2, 11–49 (1999)
8. J.P. Conde, P. Alpuim, M. Boucinha, J. Gaspar, V. Chu: Amorphous and microcrystalline silicon deposited by hot-wire chemical vapor deposition at low substrate temperatures: Application to devices and thin-film microelectromechanical systems, Thin Solid Films 395, 105–111 (2001)
9. P. Alpuim, V. Chu, J.P. Conde: Doping of amorphous and microcrystalline silicon films deposited at low substrate temperatures by hot-wire chemical vapor deposition, J. Vac. Sci. Technol. A 19, 2328–2333 (2001)
10. S.B. Patil, T. Adrega, V. Chu, J.P. Conde: Thin film silicon MEMS microresonators fabricated by hot-wire chemical vapor deposition, J. Micromech. Microeng. 16, 2730–2735 (2006)
11. M. Boucinha, P. Brogueira, V. Chu, J.P. Conde: Amorphous silicon air-gap resonators on large-area substrates, Appl. Phys. Lett. 77, 907–909 (2000)

12. M.S. Mason, C.M. Chen, H.A. Atwater: Hot-wire chemical vapor deposition for epitaxial silicon growth on large-grained polycrystalline silicon templates, Thin Solid Films 430, 54–57 (2003)
13. T. Kamins: Polycrystalline Silicon for Integrated Circuits and Displays, 2nd ed. (Kluwer, Boston, MA, 1998)
14. J.J. McMahon, J.M. Melzak, C.A. Zorman, J. Chung, M. Mehregany: Deposition and characterization of in-situ boron doped polycrystalline silicon films for microelectromechanical systems applications, Mater. Res. Symp. Proc. 605, 31–36 (2000)
15. L. Cao, T.S. Kin, S.C. Mantell, D. Polla: Simulation and fabrication of piezoresistive membrane type MEMS strain sensors, Sens. Act. 80: 273–279 (2000)
16. D. Maier-Schneider, A. Kprll, S.B. Holm, E. Obermeier: Elastic properties and microstructure of LPCVD polysilicon films, J. Micromech. Microeng. 6, 436–446 (1996)
17. H. Kahn, N. Tayebi, R. Ballarini, R.L. Mullen, A.H. Heuer: Fracture toughness of polysilicon MEMS devices, Sens. Act. A82, 274–280 (2000)
18. J. Carter, A. Cowen, B. Hardy, R. Mahadevan, M. Stonefield, S. Wilcenski: The PolyMUMPS Design Handbook (MEMSCAP Inc., Durham, NC, 2005, available at http://www.memscap.com/mumps/documents/PolyMUMPs.DR.v11.pdf). (Accessed 5 January 2009)
19. S. Jayaraman, R.L Edwards, K.J. Hemke: Relating mechanical testing and microstructural features of polysilicon thin films, J. Mater. Res. 14, 688–697 (1999)
20. C.L. Muhlstein, S.B. Brown, R.O. Ritchie: High-cycle fatigue and durability of polycrystalline silicon thin films in ambient air, Sens. Act. A94, 177–188 (2001)
21. W.N. Sharpe Jr, B. Yuan, R. Vaidyanathan, R.L. Edwards: Measurements of young's modulus, poisson's ratio, and tensile strength of polysilicon, Proceedings of the 10th Annual International Workshop on Micro Electro Mechanical Systems, Nagoya, Japan, pp. 424–429 (1997)
22. R.K. Gupta, P.M. Osterberg, S.D. Senturia: Material property measurements of micromechanical polysilicon beams, Proc. SPIE 2880, 39 (1996)
23. Sandia National Laboratories: "SUMMiT V Five Level Surface Micromachining Technology Design Manual," Science and Technology Department, Microelectronics Development Laboratory, drt@sandia.gov. Version 3.1a. (2008)
24. L. Chen, J. Miao, L. Guo, R. Lin: Control of stress in highly doped polysilicon multi-layer diaphragm structure, Surf. Coating Technol. 141, 96–102 (2001)
25. J. Yang, H. Kahn, A.Q. He, S.M. Phillips, A.H. Heuer: A new technique for producing large-area as-deposited zero-stress LPCVD polysilicon films: The multipoly process, J. Microelectromech. Syst. 9, 485–494 (2000)
26. Y.B. Gianchandani, M. Shinn, K. Najafi: Impact of high-thermal budget anneals on polysilicon as a micromechanical material, J. Microelectromech. Syst. 7, 102–105 (1998)
27. P.J. French: Polysilicon: A versatile material for microsystems, Sens. Act. A99, 3–12 (2002)
28. D. Poenar, R. Wolffenbuttel: Optical properties of thin-film silicon-compatible materials, Appl. Opt. 36, 5122–5128 (1997)
29. J.G.M. Mulder, P. Eppenga, M. Hendriks, J.E. Tong: An industrial LPCVD process for in situ phosphorus-doped polysilicon, J. Electrochem. Soc. 137, 273 (1990)
30. H. Guckel, D.W. Burns, C.C.G. Visser, H.A.C. Tilmans, D. Deroo: Fine-grained polysilicon films with built-in tensile strain, IEEE Trans. Electron Dev. 35, 800–801 (1988)
31. L. Elbrecht, R. Catanescu, J. Zacheja, J. Binder: Highly phosphorus-doped polysilicon films with low tensile stress for surface micromachining using POCl3 diffusion doping, Sens. Act. A61, 374–378 (1997)
32. G.M. Dougherty, A.P Pisano, T.D. Sands: Processing and morphology of permeable polycrystalline silicon thin films, J. Mater. Res. 17, 2235–2242 (2002)
33. G.M. Dougherty, T.D. Sands, A.P. Pisano: Microfabrication using one-step LPCVD porous polysilicon films, J. Microelectromech. Syst. 12, 418–424 (2003)
34. L.L. Lin, R.T. Howe, A.P. Pisano: A passive, in situ micro strain gauge. Proceedings of the 1993 IEEE Micro Electro Mechanical Systems Conference, Ft. Lauderdale, FL, pp. 210–206 (1993)

35. M. Madou: Fundamentals of Microfabrication, 2nd ed., p. 274 (CRC Press, Boca Raton, FL, 2002)
36. D. Maier-Schneider, J. Maibach, E. Obermeier, D. Schneider: Variations in Young's modulus and intrinsic stress of LPCVD-polysilicon due to high-temperature annealing, J. Micromech. Microeng. 5, 121–124 (1995)
37. X. Zhang, T.Y. Zhang, M. Wong, Y. Zohar: Rapid thermal annealing of polysilicon thin films, J. Microelectromech. Syst. 7, 356–364 (1998)
38. T.A. Lober, J. Huang, M.A. Schmidt, S.D. Senturia: Characterization of the Mechanisms Producing Bending Moments in Polysilicon Micro-Cantilever Beams by Interferometric Deflection Measurements, Technical Digest – Solid-State Sensor Actuator Workshop, Hilton Head, SC, pp. 92–95 (1988)
39. O. Tabata, K. Kawahata, S. Sugiyama, I. Igarashi: Mechanical property measurements of thin films using load-deflection of composite rectangular membrane. Proceedings of Micro Electro Mechanical Systems, Salt Lake City, UT, pp. 152–156 (1989)
40. H. Guckel, D.W. Burns: Planar processed polysilicon sealed cavities for pressure transducer arrays, Proc. Electron Dev. Meet 30, 223–225 (1984)
41. R.T. Howe, R.S. Muller: Polycrystalline silicon micromechanical beams, J. Electrochem. Soc. 130, 1420 (1983)
42. M. Biebl, G.T. Mulhern, R.T. Howe: In situ phosphorus-doped polysilicon for integrated MEMS, technical digest. 8th International Conference on Solid-State Sensors and Actuators, Eurosensors IX, Stockholm, Sweden, pp. 198–201 (1995)
43. M. Biebl, M.G. Brandl, R.T. Howe: Young's modulus of in situ phosphorus-doped polysilicon, technical digest. 8th International Conference on Solid-State Sensors and Actuators, Eurosensors IX, Stockholm, Sweden, pp. 80–83 (1995)
44. S. Bouwstra, E.L. de Weerd, M.C. Elwenspoek: In situ phosphorus-doped polysilicon for excitation and detection in micromechanical resonators, Sens. Act. A24, 227–235 (1990)
45. R.C. Anderson, R.S. Muller, C.W. Tobias: Porous polycrystalline silicon: A new material for MEMS, J. Microelectromech. Syst. 3, 10–18 (1994)
46. G. Fresquet, C. Azzaro, J.P. Couderc: Analysis and modeling of in situ boron-doped polysilicon deposition by LPCVD, J. Electrochem. Soc. 142, 538 (1995)
47. M. Biebl, H. von Philipsborn: fracture strength of doped and undoped polysilicon, technical digest. 8th International Conference on Solid-State Sensors and Actuators, Eurosensors IX, Stockholm, Sweden, pp.72–75 (1995)
48. H. Guckel, D.W. Burns, H.A.C. Tilmans, D.W. DeRoo, C.R. Rutigliano: Mechanical properties of fine grained polysilicon-the repeatability issue. Technical Digest, Solid-State Sensor Actuator Workshop, Hilton Head, SC, pp. 96–99 (1988)
49. J. Koskinen, J.E. Steinwall, R. Soave, H.H. Johnson: Microtensile testing of free-standing polysilicon fibers of various grain sizes, J. Micromech. Microeng. 3, 13–17 (1993)
50. J.A. Walker, K.J. Gabriel, M. Mehregany: Mechanical integrity of polysilicon films exposed to hydrofluoric acid solutions, J. Electron. Mater. 20, 665–670 (1991)
51. Y.C. Tai, R.S. Muller: Measurement of young's modulus on microfabricated structures using a surface profiler. Proceedings of Micro Electro Mechanical Systems, Napa Valley, CA, pp. 147–152 (1990)
52. L.S. Fan, Y.C. Tai, R.S. Muller: Integrated movable micromechanical structures for sensors and actuators, IEEE Trans. Electron Dev. 35, 724–730 (1988)
53. F. Ericson, S. Greek, J. Soderkvist, J. Schweitz: High sensitive internal film stress measurement by an improved micromachined indicator structure, technical digest. 8th International Conference on Solid-State Sensors and Actuators, Eurosensors IX, Stockholm, Sweden, pp. 84–87 (1995)
54. M.A. Benitez, L. Fonseca, J. Esteve, M.S. Benrakkad, J.R. Morante, J. Samitier, J.A. Schweitz: Stress-profile characterization and test-structure analysis of single and double ion-implanted LPCVD polycrystalline silicon, Sens. Act. A 54, 718–723 (1996)

55. H. Guckel, T. Randazzo, D.W. Burns: A simple technique for the determination of mechanical strain in thin films with application to polysilicon, J. Appl. Phys. 57, 1671–1675 (1983)
56. R.T. Howe, R.S. Muller: Stress in polysilicon and amorphous silicon thin films, J. Appl. Phys. 54, 4674–4675 (1983)
57. B. Semmanche, P. Kleimann, M. LeBerre, M. Lemiti, D. Barbier, P. Pinard: Rapid thermal processing of piezoresistive polycrystalline silicon films: an innovative technology for low cost pressure sensor fabrication, Sens. Act. A 46–47, 76–81 (1995)
58. T.J. Kang, H.Y. Lee, Y.H. Kim: Reduction of sheet resistance and low-thermal budget relaxation of stress gradients in polysilicon microcantilever beams using mickel-silicides, J. Microelectromech. Syst. 16, 279–288 (2007)
59. S.K. Ghandhi: VLSI Fabrication Principles – Silicon and Gallium Arsenide (Wiley, New York, NY, 1983)
60. K.S. Pister, M.W. Judy, S.R. Burgett, R.S. Fearing: Microfabricated hinges, Sens. Act. A 33, 249–256 (1992)
61. L.S. Fan, R.S. Muller: As-deposited, low-strain LPCVD polysilicon, technical digest. IEEE Solid State Sensors and Actuators Workshop, Hilton Head, SC, pp. 55–58 (1988)
62. R. He, C.J. Kim: On-chip hermetic packaging enabled by post-deposition electrochemical etching of polysilicon. Proceedings of the 18th International Conference on Microelectromechanical Systems, IEEE, Piscataway, NJ, pp. 544–547 (2005)
63. W.C. Tang, T.C.H. Nguyen, R.T. Howe: Laterally driven polysilicon resonant microstructures. Proceedings of Microelectromechanical Systems, Salt Lake City, UT, pp. 53–59 (1989)
64. W.A. Pilskin: Comparison of properties of dielectric films deposited by various methods, J. Vac. Sci. Technol. 14, 1064–1081 (1977)
65. D. Poenar, P.J. French, R. Mallee, P.M. Sarro, R.F. Wolffenbuttel: PSG layers for surface micromachining, Sens. Act. A 41–42, 304–309 (1994)
66. Y. Shioya, M. Mamoru: Comparison of phosphosilicate glass films deposited by three different chemical vapor deposition methods, J. Electrochem. Soc. 133, 1943–1950 (1986)
67. R.M. Levin, A.C. Adams: Low pressure deposition of phosphosilicate glass films, J. Electrochem. Soc. 129, 1588–1592 (1982)
68. J. Buhler, F.P. Steiner, H. Baltes: Silicon dioxide sacrificial layer etching in surface micromachining, J. Micromech. Microeng. 7, R1–R13 (1997)
69. J. Yang, O. Paul: Fracture properties of LPCVD silicon nitride thin films from the load-deflection of long membranes, Sens. Act. A 97–98, 520–526 (2002)
70. B. Folkmer, P. Steiner, W. Lang: Silicon nitride membrane sensors with monocrystalline transducers, Sens. Act. A51, 71–75 (1995)
71. M. Sekimoto, H. Yoshihara, T. Ohkubo: Silicon nitride single-layer x-ray mask, J. Vac. Sci. Technol. 21, 1017–1021 (1982)
72. J.G.E. Gardeniers, H.A.C. Tilmans, C.C.G. Visser: LPCVD silicon-rich silicon nitride films for applications in micromechanics studied with statistical experimental design, J. Vac. Sci. Technol. A 14, 2879–2892 (1996)
73. P. Temple-Boyer, C. Rossi, E. Saint-Etienne, E. Scheid: Residual stress in low pressure chemical vapor deposition SiN_x films deposited from silane and ammonia, J. Vac. Sci. Technol. A16, 2003–2007 (1998)
74. C. Mastrangelo, Y.-C. Tai, R. Muller: Thermophysical properties of low-residual stress, silicon-rich, LPCVD silicon nitride films, Sens. Act. A21–A23, 856–860 (1990)
75. P.P. Tsai, I.-C. Chen, C.J. Ho: Ultralow power carbon monoxide microsensor by micromachining techniques, Sens Act. B76, 380–387 (2001)
76. P.J. French, P.M. Sarro, R. Mallee, E.J.M. Fakkeldij, R.F. Wolffenbuttel: Optimization of a low-stress silicon nitride process for surface micromachining applications, Sens. Act. A58, 149–157 (1997)
77. A. Kaushik, H. Kahn, A.H. Heuer: Wafer-level mechanical characterization of silicon nitride MEMS, J. Microelectromech. Syst. 14, 359–367 (2005)

78. L.S. Fan, R.T. Howe, R.S. Muller: Fracture toughness of brittle thin films, Sens. Act. A21–A23, 872–874 (1990)
79. X. Zhang, T.Y. Zhang, T. Zohar: Measurement of residual stresses in thin films using micro-rotating-structures, Thin Solid Films 335, 97–105 (1998)
80. J.M. Olson: Analysis of LPCVD process conditions for the deposition of low stress silicon nitride. Part 1: preliminary LPCVD experiments, Mater. Sci. Semicond. Process. 5, 51–60 (2002)
81. P. Pan, W. Berry: The composition and physical properties of LPCVD silicon nitride deposited with different NH_3/SiH_2Cl_2 gas ratios, J. Electrochem. Soc. 132, 3001–3005 (1985)
82. S. Hong, T.P. Weihs, J.C. Bravman, W.D. Nix: Measuring stiffness and residual stresses of silicon nitride thin films, J. Electron. Mater. 19, 903–909 (1990)
83. B.C.S. Chou, J.S. Shie, C.N. Chen: Fabrication of low stress dielectric thin film for microsensor applications, IEEE Electron Dev. Lett. 18, 599–601 (1997)
84. E.I. Bromley, J.N. Randall, D.C. Flanders, R.W. Mountain: A technique for the determination of stress in thin films, J. Vac. Sci. Technol. B 1, 1364–1366 (1983)
85. D. Resnik, U. Aljancic, D. Vrtacnik, M. Mozek, S. Amon: Mechanical stress in thin film microstructures on silicon substrate, Vacuum 80, 236–240 (2005)
86. T.Y. Zhang, Y.J. Su, C.F. Qian, M.H. Zhao, L.Q. Chen: Microbridge testing of silicon nitride thin films deposited on silicon wafers, Acta Mater. 48, 2843–2857 (2000)
87. Y. Ren, D.C.C. Lam: Characterization of elastic behaviors of silicon nitride films with varying thicknesses, Mater. Sci. Eng. A 467, 93–96 (2007)
88. B. Li, B. Xiong, L. Jiang, Y. Zohar, M. Wong: Germanium as a versatile material for low-temperature micromachining, J. Microelectromech. Syst. 8, 366–372 (1999)
89. A. Franke, D. Bilic, D.T. Chang, P.T. Jones, T.J. King, R.T. Howe, C.G. Johnson: Post-CMOS integration of germanium microstructures. Proceedings of the 12th International Conference on Microelectromechanical Systems, IEEE, Piscataway, NJ, pp. 630–637 (1999)
90. A.E. Franke, Y. Jiao, M.T. Wu, T.J. King, R.T. Howe: Post-CMOS modular integration of poly-sige microstructures using poly-ge sacrificial layers. Technical Digest, Solid State Sensor and Actuator Workshop, Hilton Head, SC, pp. 18–21 (2000)
91. S. Sedky, P. Fiorini, M. Caymax, S. Loreti, K. Baert, L. Hermans, R. Mertens: Structural and mechanical properties of polycrystalline silicon germanium for micromachining applications, J. Microelectromech. Syst. 7, 365–372 (1998)
92. S. Sedky, A. Witvrouw, K. Baert: Poly SiGe, a promising material for MEMS monolithic integration with the driving electronics, Sens. Act. A97–98, 503–511 (2002)
93. C.W. Low, T.J.K. Liu, R.T. Howe: Characterization of polycrystalline silicon-germanium film deposition for modularly integrated MEMS applications, J. Microelectromech. Syst. 16, 68–77 (2007)
94. S. Sedky, A. Bayoumy, A. Alaa, A. Nagy, A. Witvrouw: Optimal conditions for micromachining $Si_{1-x}Ge_x$ at 210°C, J. Microelectromech. Syst. 16, 581–588 (2007)
95. J.M. Heck, C.G. Keller, A.E. Franke, L. Muller, T.J. King, R.T. Howe: High aspect ratio polysilicon-germanium microstructures. Proceedings of the 10th International Conference on Solid State Sensors and Actuators, Sendai, Japan, pp. 328–334 (1999)
96. P. Van Gerwen, T. Slater, J.B. Chevrier, K. Baert, R. Mertens: Thin-film boron-doped polycrystalline $silicon_{70\%}$-$germanium_{30\%}$ for thermopiles, Sens. Act. A 53, 325–329 (1996)
97. A. Witvrouw, H.A.C. Tilmans, I. De Wolf: Materials issues in the processing, the operation and the reliability of MEMS, Microelectron. Eng. 76, 245–257 (2004)
98. S.A. Bhave, B.L. Bircumshaw, W.Z. Low, Y.S. Kim: Poly-SiGe: A high-Q structural material for integrated Rf MEMS. Technical Digest, Solid-State Sensors, Actuator and Microsystems Workshop, Hilton Head, SC, pp. 34–37 (2002)
99. S. Sedky, R.T. Howe, T.-J. King: Pulsed-laser annealing, a low-thermal-budget technique for eliminating stress gradient in poly-SiGe MEMS structures, J. Microelectromech. Syst. 13, 669–675 (2004)

100. M.-A. Eyoum, T.-J. King: Low-resistance silicon-germanium contact technology for modular integration of MEMS with electronics, J. Electrochem. Soc. 151, J21–J25 (2004)
101. Y.C. Jeon, T.J. King, R.T. Howe: Properties of phosphorus-doped poly-SiGe films for microelectromechanical system applications, J. Electrochem. Soc. 150, H1 (2003)
102. A.E. Franke, J.M. Heck, T.J. King, R.T. Howe: Polycrystalline silicon-germanium films for integrated microsystems, J. Microelectromech. Syst. 12, 160–171 (2003)
103. T.-J. King, J.P. McVittie, K.C. Saraswat: Electrical properties of heavily doped polycrystalline silicon-germanium films, IEEE Trans. Electron Dev. 41, 228–232 (1994)
104. R.S. Okojie, A.A. Ned, A.D. Kurtz: Operation of a 6H-SiC pressure sensor at 500°C, Sens. Act. A66, 200–204 (1998)
105. G. Beheim, C.S. Salupo: Deep RIE process for silicon carbide power electronics and MEMS, Mater. Res. Soc. Symp. Proc. 622, T8.8.1–T8.8.6 (2000)
106. M. Mehregany, C.A. Zorman, N. Rajan, C.H. Wu: Silicon carbide MEMS for harsh environments, Proc. IEEE 8, 1594–1610 (1998)
107. C.R. Stoldt, C. Carraro, W.R. Ashurst, D. Gao, R.T. Howe, R. Maboudian: A low temperature CVD process for silicon carbide MEMS, Sens. Act. A97–98, 410–415 (2002)
108. D. Gao, R.T. Howe, R. Maboudian: High-selectivity etching of polycrystalline 3C-SiC films using HBR-based transformer coupled plasma, Appl. Phys. Lett. 82, 1742–1744 (2004)
109. C.A. Zorman, S. Rajgolpal, X.A. Fu, R. Jezeski, J. Melzak, M. Mehregany: Deposition of polycrystalline 3C-SiC films on 100 mm-diameter (100) Si wafers in a large-volume LPCVD furnace, Electrochem. Solid State Lett. 5, G99–G101 (2002)
110. L. Behrens, E. Peiner, A.S. Bakin, A. Schlachetzski: Micromachining of silicon carbide on silicon fabricated by low-pressure chemical vapor deposition, J. Micromech. Microeng. 12, 380–384 (2002)
111. C.A. Zorman, S. Roy, C.H. Wu, A.J. Fleischman, M. Mehregany: Characterization of polycrystalline silicon carbide films grown by atmospheric pressure chemical vapor deposition on polycrystalline silicon, J. Mater. Res. 13, 406–412 (1996)
112. C.H. Wu, C.A. Zorman, M. Mehregany: Growth of polycrystalline SiC films on SiO_2 and Si_3N_4 by APCVD, Thin Solid Films 355–356, 179–183 (1999)
113. X.A. Fu, R. Jezeski, C.A. Zorman, M. Mehregany: Use of deposition pressure to control the residual stress in polycrystalline SiC films, Appl. Phys. Lett. 84, 341–343 (2004)
114. D. Gao, M.B. Wijesundara, C. Carraro, R.T. Howe, R. Maboudian: Recent progress toward and manufacturable polycrystalline SiC surface micromachining technology, IEEE Sens. J. 4, 441–448 (2004)
115. C.S. Roper, R.T Howe, R. Maboudian: Stress control of polycrystalline 3C-SiC films in a large-scale LPCVD reactor using 1,3-disilabutane and dichlorosilane as precursors, J. Micromech. Microeng. 16, 2736–2739 (2006)
116. X.-A. Fu, J.L. Dunning, C.A. Zorman, M. Mehregany: Polycrystalline 3C-SiC thin films deposited by dual precursor LPCVD for MEMS applications, Sens. Act. A 119, 169–176 (2005)
117. Y. Yamaguchi, H. Nagasawa, T. Shoki, N. Armaka, H. Mitsui: Properties of heteroepitaxial 3C-SiC films grown by LPCVD, Sens. Act. A54, 695–699 (1996)
118. H. Nagasawa, Y. Yamaguchi: Atomic level epitaxy of 3C-SiC by low pressure vapour deposition with alternating gas supply, Thin Solid Films 225, 230–234 (1993)
119. C.R. Stoldt, M.C. Fritz, C. Carraro, R. Maboudian: Micromechanical properties of silicon carbide thin films deposited using single source chemical vapor deposition, Appl. Phys. Lett. 79, 347–349 (2001)
120. J. Zhang, C. Carraro, R.T. Howe, R. Maboudian: Electrical, mechanical and metal contact properties of polycrystalline 3C-SiC films for MEMS in harsh environments, Surf. Coatings Technol. 201, 8893–8898 (2007)
121. D. Gao, C. Carraro, V. Radmilovic, R.T. Howe, R. Maboudian: Fracture of polycrystalline 3C-SiC films in microelectromechanical systems, J. Microelectromech. Syst. 13, 972–976 (2004)

122. E. Hurtos, J. Rodriguez-Viejo: Residual stress and texture in poly-SiC films grown by low-pressure organometallic chemical-vapor deposition, J. Appl. Phys. 87, 1748–1758 (2000)
123. J. Chen, J. Scofield, A.J. Steckl: Formation of SiC SOI structures by direct growth on insulating substrates, J. Electrochem. Soc. 147, 3845–3849 (2000)
124. K. Murooka, I. Higashikawa, Y. Gomei: Improvement of the Young's modulus of SiC film by low pressure chemical vapor deposition with B_2H_6 gas, Appl. Phys. Lett. 69, 37–39 (1996)
125. G. Sun, J. Ning, X. Liu, Y. Zhao, J. Li, L. Wang, W. Zhao, L. Wang: Heavily doped polycrystalline 3C-SiC growth on SiO_2/Si (100) substrates for resonator applications, Mater. Sci. Forum 556–557, 179–182 (2007)
126. X. Fu, J.L. Dunning, C.A. Zorman, M. Mehregany: Measurement of residual stress and elastic modulus of polycrystalline 3C-SiC films deposited by low-pressure chemical vapor deposition, Thin Solid Films 492, 195–202 (2005)
127. S. Nagappa, M. Zupan, C.A. Zorman: Mechanical characterization of chemical-vapor-deposited polycrystalline 3C silicon carbide thin films, Scr. Mater. 59, 995–998 (2008)
128. J. Trevino, X. Fu, M. Mehregany, C. Zorman: Low-stress, heavily-doped polycrystalline silicon carbide for MEMS applications. Proceedings of the 18th International Conference on Micro Electro Mechanical Systems, Miami, FL, pp. 451–454 (2005)
129. V. Hatty, H. Kahn, J. Trevino, C.A. Zorman, M. Mehregany, R. Ballarini, A.H. Heuer: Fracture toughness of low-pressure chemical-vapor-deposited polycrystalline silicon carbide thin films, J. Appl. Phys. 99, 013517 (2006)
130. L. Cheng, M. Pan, J. Scofield, A.J. Steckl: Growth and doping of SiC thin films on low-stress, amorphous Si_3N_4/Si substrates for robust microelectromechanical systems applications, J. Electron. Mater. 31, 361–365 (2002)
131. W. Zhou, J. Yang, G. Sun, X. Liu, F. Yang, J. Li: Fracture properties of silicon carbide thin films characterized by bulge test of long membranes. Proceedings of the 3rd International Conference on Nano/Micro Engineered and Molecular Systems, Sanya, China, pp. 557–560 (2008)
132. E. Mastropaolo, R. Cheung, A. Henry, E. Janzén: Fabrication of beam resonators from hot-wall chemical vapour deposited SiC, Microelectron. Eng. 86, 1194–1196 (2009)
133. S. Noh, X. Fu, L. Chen, M. Mehregany: A study of electrical properties and microstructure of nitrogen-doped poly-SiC films deposited by LPCVD, Sens. Act. A 136, 613–617 (2007)
134. M.B.J. Wijesundara, C.R. Stoldt, C. Carraro, R.T. Howe, R. Maboudian: Nitrogen doping of polycrystalline 3C–SiC films grown by single-source chemical vapor deposition, Thin Solid Films 419, 69–75 (2002)
135. M.B.J. Wijesundara, D. Gao, C. Carraro, R.T. Howe, R. Maboudian: Nitrogen doping of polycrystalline 3C-SiC films grown using 1,3-disilabutane in a conventional LPCVD reactor, J. Crystal Growth 259, 18–25 (2003)
136. J. Zhang, R.T. Howe, R. Maboudian: Control of strain gradient in doped polycrystalline silicon carbide films through tailored doping, J. Micromech. Microeng. 16, L1–L5 (2006)
137. C.S. Roper, V. Radmilovic, R.T. Howe, R. Maboudian: Characterization of polycrystalline 3C-SiC films deposited from the precursors 1,3-disilabutane and dichlorosilane, J. Appl. Phys. 103, 084907 (2008)
138. C.S. Roper, V. Radmilovic, R.T. Howe, R. Maboudian: Effects of annealing on residual stress and strain gradient of doped polycrystalline SiC thin films, Electrochem. Solid State Lett. 11, D35–D37 (2008)
139. H.D. Espinosa, B. Peng, N. Moldovan, T.A. Friedmann, X. Xiao, D.C. Mancini, O. Auciello, J. Carlisle, C.A Zorman, M. Mehegany: Elasticity, strength, and toughness of single crystal silicon carbide, ultrananocrystalline diamond, and hydrogen-free tetrahedral amorphous carbon, Appl. Phys. Lett. 89, 073111 (2006)
140. T. Shibata, Y. Kitamoto, K. Unno, E. Makino: Micromachining of diamond film for MEMS applications, J. Microelectromech. Syst. 9, 47–51 (2000)

141. D.K. Reinhard, T.A. Grotjohn, M. Becker, M.K. Yaran, T. Schuelke, J. Asmussen: Fabrication and properties of ultranano, nano, and microcrystalline diamond membranes and sheets, J. Vac. Sci. Technol. B 22, 2811 (2004)
142. X. Xiao, B.W. Sheldon, Y. Qi, A.K. Kothari: Intrinsic stress evolution in nanocrystalline diamond thin films with deposition temperature, Appl. Phys. Lett. 92, 131908 (2008)
143. H. Li, B.W. Sheldon, A. Kothari, Z. Ban, B.L. Walden: Stress evolution in nanocrystalline diamond films produced by chemical vapor deposition, J. Appl. Phys. 100, 094309 (2006)
144. D.R. Wur, J.L. Davidson, W.P. Kang, D.L. Kinser: Polycrystalline diamond pressure sensor, J. Microelectromech. Syst. 4, 34–41 (1995)
145. A.R. Krauss, O. Auciello, D.M. Gruen, A. Jayatissa, A. Sumant, J. Tucek, D.C. Mancini, N. Moldovan, A. Erdemir, D. Ersoy, M.N. Gardos, H.G. Busmann, E.M. Meyer, Q. Ding: Ultrananocrystalline diamond thin films for MEMS and moving mechanical assembly devices, Diam. Relat. Mater. 10, 1952–1961 (2001)
146. H.D. Espinosa, B.C. Prorok, B. Peng, K.H. Kim, M. Moldovan, O. Auciello, J.A. Carlisle, D.M. Gruen, D.C. Mancini: Mechanical properties of ultrananocrystalline diamond thin films relevant to MEMS/NEMS devices, Exp. Mech. 4, 256–268 (2003)
147. H.D. Espinosa, B. Peng, B.C. Prorok, N. Moldovan, O. Auciello, J.A. Carlisle, D.M. Gruen, D.C. Mancini: Fracture strength of ultrananocrystalline diamond thin films – identification of Weibull parameters, J. Appl. Phys. 94, 6076 (2003)
148. F.J. Hernández Guillén, K. Janischowsky, W. Ebert, E. Kohn: Nanocrystalline diamond films for mechanical applications, Phys. Status Solidi A 201, 2553–2557 (2004)
149. V.P. Adiga, A.V. Sumant, S. Suresh, C. Gudeman, O. Auciello, J.A. Carlisle, R.W. Carpick: Mechanical stiffness and dissipation in ultrananocrystalline diamond microresonators, Phys. Rev. B 79, 245403 (2009)
150. S. Sahli, D.M. Aslam: Measurement of the pressure response of boron-doped CVD diamond piezoresistors as a function of resistivity and electric field, Sens. Act. A 69, 27–32 (1998)
151. S. Sahli S, D.M. Aslam: Ultra-high sensitivity intra-grain poly-diamond piezoresistors, Sens. Act. A 71, 193–197 (1998)
152. H. Bjorkman, P. Rangsten, P. Hollman, K. Hjort: Diamond replicas from microstructured silicon masters, Sens. Act. 73, 24–29 (1999)
153. M. Aslam, D. Schulz: Technology of diamond microelectromechanical systems. Proceedings of the 8th International Conference on Solid State Sensors and Actuators, Eurosensors IX, Stockholm, Sweden, pp. 222–224 (1995)
154. R. Ramesham: Fabrication of diamond microstructures for microelectromechanical systems (MEMS) by a surface micromachining process, Thin Solid Films 340, 1–6 (1999)
155. Y. Yang, X. Wang, C. Ren, J. Xie, P. Lu, W. Wang: Diamond surface micromachining technology, Diam. Relat. Mater. 8, 1834–1837 (1999)
156. X.D. Wang, G.D. Hong, J. Zhang, B.L. Lin, H.Q. Gong, W.Y. Wang: Precise patterning of diamond films for MEMS applications, J. Mater. Process. Technol. 127, 230–233 (2002)
157. J. Wang, J.E. Butler, D.S.Y. Hsu, C.T.C. Nguyen: CVD polycrystalline diamond high-Q micromechanical resonators. Proceedings of the 15th International Conference on Microelectromechanical Systems, Las Vegas, NV, pp. 657–660 (2002)
158. J. Wang, J.E. Butler, T. Feygelson, C.T.C. Nguyen: 1.51 GHz nanocrystalline diamond micromechanical disk resonator with material mismatched isolating support. Proceedings of the 17th International Conference on Microelectromechanical Systems, Maastricht, the Netherlands, pp. 641–644 (2004)
159. N. Sepulveda, D. Aslam, J.P. Sullivan: Polycrystalline diamond MEMS resonator technology for sensor applications, Diam. Relat. Mater. 15, 398–403 (2006)
160. O. Auciello, J. Birrell, J.A. Carlisle, J. Geri, X. Xiao, B. Peng, H.D. Espinosa: Materials science and fabrication processes for a new MEMS technology based on ultrananocrystalline diamond thin film, J. Phys. Condens. Matter 16, R539–R552 (2004)
161. X. Xiao, J. Birrell, J.E. Gerbi, O. Auciello, J.A. Carlisle: Low temperature growth of ultrananocrystalline diamond, J. Appl. Phys. 96, 2232–2239 (2004)

162. W. Yang, O. Auciello, J.E. Butler, W. Cai, J.A. Carlisle, J.E. Gerbi, D.M. Gruen, T. Knickerbocker, T.L. Lasseter, J.N. Russel, L.M. Smith, J. Hamers: DNA-modified nanocrystalline diamond thin films as stable, biologically active substrates, Nat. Mater. 1, 253–257 (2002)
163. J.J. Bellante, H. Kahn, R. Ballarini, C.A. Zorman, M. Mehregany, A.H. Heuer: Fracture toughness of polycrystalline silicon carbide thin films, Appl. Phys. Lett. 86, 071920 (2005)
164. G.-S. Chung, K.-B. Han: H_2 carrier gas dependence of Young's modulus and hardness of chemical vapor deposited polycrystalline 3C-SiC thin films, Microelectron. J. 39, 1413–1415 (2008)
165. S. Roy, C. Zorman, M. Mehregany, R. DeAnna, C. Deeb: The mechanical properties of polycrystalline 3C-SiC films grown on polysilicon substrates by atmospheric pressure chemical-vapor deposition, J. Appl. Phys. 99, 044108 (2006)
166. J. Gaspar, T. Adrega, V. Chu, J.P. Conde: Thin-film paddle microresonators with high quality factors fabricated at temperatures below 110°C. Proceedings of the 18th International Conference on Microelectromechanical Systems, Miami, FL, pp. 125–128 (2005)
167. S.B. Patil, V. Chu, J.P. Conde: Surface micromachining of a thin film microresonator using dry decomposition of a polymer sacrificial layer, J. Vac. Sci. Technol. B25, 455–458 (2007)
168. S. Chang, S. Sivoththaman: A tunable RF MEMS inductor on silicon incorporating an amorphous silicon bimorph in a low-temperature process, IEEE Electron Dev. Lett. 27, 905–907 (2006)
169. S. Chang, S. Sivoththaman: Development of a low temperature MEMS process with a PECVD amorphous silicon structural layer, J. Micromech. Microeng. 16, 1307–1313 (2006)
170. P. Alpuim, V. Chu, J.P. Conde: Amorphous and microcrystalline silicon films grown at low temperatures by radio-frequency and hot-wire chemical vapor deposition, J. Appl. Phys. 86, 3812–3821 (1999)
171. S.B. Patil, V. Chu, J.P. Conde: Comparison of the mechanical and resonance properties of thin film silicon MEMS fabricated at 110 and 250°C, J. Micromech. Microeng. 19, 025018 (2009)
172. C.-K. Chung, M.-Q. Tsai, P.-H. Tsai, C. Lee: Fabrication and characterization of amorphous Si films by PECVD for MEMS, J. Micromech. Microeng. 15, 136–142 (2005)
173. S. Chang, W. Eaton, J. Fulmer, C. Gonzalez, B. Underwood: Micromechanical structures in amorphous silicon. Technical Digest, International Conference on Solid State Sensors and Actuators, San Francisco, CA, pp. 751–754 (1991)
174. A. Tarraf, J. Daleiden, S. Irmer, D. Prasai, H. Hillmer: Stress investigation of PECVD dielectric layers for advanced optical MEMS, J. Micromech. Microeng. 14, 317–323 (2004)
175. X. Zhang, K.-S. Chen, R. Ghodssi, A.A. Ayon, S.M. Spearing: Residual stress and fracture in thick tetraethylorthosilicate (TEOS) and silane-based PECVD oxide films, Sens. Act. A 91, 373–380 (2001)
176. B.A. Walmsley, Y.L. Liu, X.Z. Hu, M.B. Bush, J.M. Dell, L. Faraone: Poisson's ratio of low-temperature PECVD silicon nitride thin films, J. Microelectromech. Syst. 16, 622–627 (2007)
177. M.-C. Jo, S.-K. Park, S.-J. Park: A study on resistance of PECVD silicon nitride thin film to thermal stress-induced cracking, Appl. Surf. Sci. 140, 12–18 (1999)
178. C. Iliescu, F.E.H. Tay, J. Wei: Low stress PECVD-SiN_x layers at high deposition rates using high power and high frequency for MEMS applications, J. Micromech. Microeng. 16, 869–874 (2006)
179. M. Martyniuk, J. Antoszewski, C.A. Musca, J.M. Dell, L. Faraone: Dielectric thin films for MEMS-based optical sensors, Microelectron. Reliab. 47, 733–738 (2007)
180. H. Huang, K.J. Winchester, A. Suvorova, B.R. Lawne, Y. Liud, X.Z. Hud, J.M. Dell, L. Faraone: Effect of deposition conditions on mechanical properties of low-temperature PECVD silicon nitride films, Mater. Sci. Eng. A 435–436, 453–459 (2006)
181. E. Cianci, A. Coppa, V. Foglietti: Young's modulus and residual stress of RF PECVD silicon nitride for MEMS free-standing membrane, Microelectron. Eng. 84, 1296–1299 (2007)

182. W. Zhou, J. Yang, Y. Li, A. Ji, F. Yang, Y. Yu: Bulge testing and fracture properties of plasma-enhanced chemical vapor deposited silicon nitride thin films, Thin Solid Films 517, 1989–1994 (2009)
183. T. Kramer, O. Paul: Surface micromachined ring test structures to determine mechanical properties of compressive thin films, Sens. Act. A 92, 292–298 (2001)
184. M. Gromova, A. Mehta, K. Baert, A. Witvrouw: Characterization and strain gradient optimization of PECVD poly-SiGe layers for MEMS applications, Sens. Act. A 130–131, 403–410 (2006)
185. S. Kannan, C. Taylor, D. Allred: PECVD growth of Si_x:Ge_{1-x} films for high speed devices and MEMS, J. Non-Crystalline Solids 352, 1272–1274 (2006)
186. M. Gromova, K. Baert, C. van Hoof, A. Mehta, A. Witvrouw: The novel use of low temperature hydrogenated microcrystalline silicon germanium (μcSiGe:H) for MEMS applications, Microelectron. Eng. 76, 266–271 (2004)
187. C. Rusu, S. Sedky, B. Parmentier, A. Verbist, O. Richard, B. Brijs, L. Geenen, A. Witvrouw, F. Larmer, F. Fischer, S. Kronmuller, V. Leca, B. Otter: New low-stress PECVD poly-SiGe Layers for MEMS, J. Microelectromech. Syst. 12, 816–825 (2003)
188. A. Mehta, M. Gromova, C. Rusu, R. Olivier, K. Baert, C. van Hoof, A. Witvrouw: Novel high growth rate processes for depositing poly-sige structural layers at CMOS compatible temperatures. Proceedings of the 17th International Conference on Micro Electro Mechanical Systems, Maastricht, The Netherlands, pp. 721–724 (2004)
189. A. Molfese, A. Mehta, A. Witvrouw: Determination of stress profile and optimization of stress gradient in PECVD poly-SiGe films, Sens. Act. A 118, 313–321 (2005)
190. A. Mehta, M. Gromova, P. Czarnecki, K. Baert, A. Witvrouw: Optimisation of PECVD poly-SiGe layers for MEMS post-processing on top of CMOS. Technical Digest, 13th International Conference on Solid-State Sensors, Actuators and Microsystems, Seoul, Korea, pp. 1326–1329 (2005)
191. S. Sedky, M. Gromova, T. van der Donck, J.P. Celis, A. Witvrouw: Characterization of KrF excimer laser annealed PECVD Si_xGe_{1-x} for MEMS post-processing, Sens. Act. A 127, 316–323 (2006)
192. P.M. Sarro: Silicon carbide as a new MEMS technology, Sens. Act. 82, 210–218 (2000)
193. A. Klumpp, U. Schaber, H.L. Offereins, K. Kuhl, H. Sandmaier: Amorphous silicon carbide and its application in silicon micromachining, Sens. Act. A 41–42, 310–316 (1994)
194. U. Schmid, M. Eickhoff, C. Richter, G. Krötz, D. Schmitt-Landsiedel: Etching characteristics and mechanical properties of a-SiC:H thin films, Sens. Act. A 94: 87–94 (2001)
195. H. Zhang, H. Guo, Y. Wang, G. Zhang, Z. Li: Study on a PECVD SiC-coated pressure sensor, J. Micromech. Microeng. 17, 426–431 (2007)
196. G. Rehder, M.N.P. Carreño: Thermally actuated a-SiC:H MEMS fabricated by a PECVD process, J. Non-Crystalline Solids 352, 1822–1828 (2006)
197. G. Rehder, M.N.P. Carreño: PECVD a-SiC:H Young's modulus obtained by MEMS resonant frequency. J. Non-Crystalline Solids 354, 2359–2364 (2008)
198. A.F. Flannery, N. Mourlas, C.W. Storment, S. Tsai, S.H. Tan, J. Heck, D. Monk, T. Kim, B. Gogoi, G.T.A. Kovacs: PECVD silicon carbide as a mechanically resistant material for micromachined transducers, Sens. Act. A 70, 48–55 (1998)
199. L.S. Pakula, H. Yang, H.T.M. Pham, P.J. French, P.M. Sarro: Fabrication of a CMOS compatible pressure sensor for harsh environments, J. Micromech. Microeng. 14, 1478–1483 (2004)
200. P.M. Sarro, C.R. deBoer, E. Korkmaz, J.M.W. Laros: Low-stress PECVD SiC thin films for IC-compatible microstructures, Sens. Act. A 67, 175–180 (1998)
201. C. Iliescu, B. Chen, D.P. Poenar, Y.Y. Lee: PECVD amorphous silicon carbide membranes for cell culturing, Sens. Act. B 129, 404–411 (2008)
202. C. Iliescu, B. Chen, J. Wei, A.J. Pang: Characterisation of silicon carbide films deposited by plasma-enhanced chemical vapour deposition, Thin Solid Films 516, 5189–5193 (2008)

203. J. Du, C.A. Zorman: Low temperature a-SiC/Si direct bonding technology for MEMS/NEMS. Technical Digest of the 14th International Conference on Solid State Sensors, Actuators and Microsystems, Lyon, France, pp. 2075–2078 (2007)
204. A. Bagolini, L. Pakula, T.L.M. Scholtes, H.T.M. Pham, P.J. French, P.M. Sarro: Polyimide sacrificial layer and novel materials for post processing surface micromachining, J. Micromech. Microeng. 12, 385–389 (2002)
205. S.A. Smallwood, K.C. Eapen, S.T. Patton, J.S. Zabinski: Performance results of MEMS coated with a conformal DLC, Wear 260, 1179–1189 (2006)
206. J.K. Luo, Y.Q. Fu, H.R Le, J.A. Williams, S.M. Spearing, W.I. Milne: Diamond and diamond-like carbon MEMS, J. Micromech. Microeng. 17, S147–S163 (2007)
207. S.-J. Cho, K.-R. Lee, K.Y. Eun, J.H. Jeong, D. Kwon: A method of determining the elastic properties of diamond-like carbon films. Diam. Relat. Mater. 8, 1067–1072 (1999)
208. S.-J. Cho, K.-R. Lee, K.Y. Eun. J.H. Han, D.H. Ko: Determination of elastic modulus and Poisson's ratio of diamond-like carbon films, Thin Solid Films 332, 207–210 (1998)
209. B. Zhou, L. Wang, N. Mehta, S. Morshed, A. Erdemir, O. Eryilmaz, B.C. Prorok: The mechanical properties of freestanding near-frictionless carbon films relevant to MEMS, J. Micromech. Microeng. 16, 1374–1381 (2006)
210. P. Gennissen, M. Bartek, P.J. French, P.M. Sarro: Bipolar-compatible epitaxial poly for smart sensors: stress minimization and applications, Sens. Act. A62, 636–645 (1997)
211. P. Lange, M. Kirsten, W. Riethmuller, B. Wenk, G. Zwicker, J.R. Morante, F. Ericson, J.A. Schweitz: Thick polycrystalline silicon for surface-micromechanical applications: Deposition, structuring, and mechanical characterization, Sens. Act. A54, 674–678 (1996)
212. S. Greek, F. Ericson, S. Johansson, M. Furtsch, A. Rump: Mechanical characterization of thick polysilicon films: Young's modulus and fracture strength evaluated with microstructures, J. Micromech. Microeng. 9, 245–251 (1999)
213. M. Kirsten, B. Wenk, F. Ericson, J.A. Schweitz, W. Reithmuller, P. Lang: Deposition of thick doped polysilicon films with low stress in an epitaxial reactor for surface micromachining applications, Thin Solid Films 259, 181–187 (1995)
214. S. Greek, F. Ericson, S. Johansson, J.A. Schweitz: In situ tensile strength measurement and Weibull analysis of thick film and thin film micromachined polysilicon structures, Thin Solid Films 292, 247–254 (1997)
215. O. De Sagazan, M. Denoual, P. Guil, D. Gaudin, O. Bonnaud: Microelectromechanical systems fast fabrication by selective thick polysilicon growth in epitaxial reactor, Microsyst. Technol. 12, 953–958 (2006)
216. M. Furtsch, M. Offenberg, A. Vila, A. Comet, J.R. Morante: Texture and stress profile in thick polysilicon films suitable for fabrication of microstructures, Thin Solid Films 296, 177–180 (1997)
217. M. Eickhoff, H. Moller, G. Kroetz, J. von Berg, R. Ziermann: A high temperature pressure sensor prepared by selective deposition of cubic silicon carbide on SOI substrates. Sens. Act. 74, 56–59 (1999)
218. G. Krotz, H. Moller, M. Eickhoff, S. Zappe, R. Ziermann, E. Obermeier, J. Stoemenos: Heteroepitaxial growth of 3C-SiC on SOI for sensor applications, Mater. Sci. Eng. B 61, 516–521 (1999)
219. D. Young, J.D. Du, C.A. Zorman, W.H. Ko: High-temperature single crystal 3C-SiC capacitive pressure sensor, IEEE Sens. J. 4, 464–470 (2004)
220. N. Moronuki, M. Kojima, A. Kakuta: Single-crystal SiC thin-film produced by epitaxial growth and its application to micro-mechanical devices, Thin Solid Films 516, 5344–5348 (2008)
221. M. Pozzi, M. Hassan, A.J. Harris, J.S. Burdess, L. Jiang, K.K. Lee, R. Cheung, G.J. Phelps, N.G. Wright, C.A. Zorman, M. Mehregany: Mechanical properties of a 3C-SiC film between room temperature and 600°C, J. Phys. D: Appl. Phys. 40, 3335–3342 (2007)
222. C.M Su, M. Wuttig, A. Fekade, M. Spencer: Elastic and anelastic properties of chemical vapor deposited epitaxial 3C-SiC, J. Appl. Phys. 77, 5611–5615 (1995)

223. K.M. Jackson, J. Dunning, C.A. Zorman, M. Mehregany, W.N. Sharpe Jr.: Mechanical properties of epitaxial 3C silicon carbide thin films, J. Microelectromech. Syst. 14, 664–672 (2005)
224. C. Gourbeyre, T. Chassagne, M. Le Berre, G. Ferro, E. Gautier, Y. Monteil, D. Barbier: Correlation between epitaxial growth conditions of 3C-SiC thin films on Si and mechanical behavior of 3C-SiC self-suspended membranes, Sens. Act. A 99, 31–34 (2002)
225. J.S. Mitchell, C.A. Zorman, T. Kicher, S. Roy, M. Mehregany: Examination of bulge test for determining residual stress, Young's modulus and Poisson's ratio of 3C-SiC thin films, J. Aerosp. Eng. 16, 46–54 (2003)
226. A.A. Volinsk, G. Kravchenko, P. Waters, J.D. Reddy, C. Locke, C. Frewin, S.E. Saddow: Residual stress in CVD-grown 3C-SiC films on Si substrates, Mater. Res. Soc. Symp. Proc. 1069: 1069-D03-05 (2008)
227. Ch. Forster, V. Cimalla, K. Bruchner, M. Hein, J. Pezoldt, O. Ambacher: Microelectromechanical systems based on 3C-SiC/Si heterostructures, Mater. Sci. Eng. C 25, 804–808 (2005)
228. K. Hjort, J. Soderkvist, J.A. Schweitz: Galium arsenide as a mechanical material, J. Micromech. Microeng. 4, 1–13 (1994)
229. Y. Uenishi, H. Tanaka, H. Ukita: Characterization of AlGaAs microstructure fabricated by AlGaAs/GaAs micromachining, IEEE Trans. Electron Dev. 41, 1778–1783 (1994)
230. M.W. Pruessner, T.T. King, D.P. Kelly, R. Grover, L.C. Calhoun, R. Ghodssi: Mechanical property measurement of InP-based MEMS for optical communications, Sens. Act. A 105, 190–200 (2003)
231. J. Arokiaraj, S. Tripathy, S. Vicknesh, A. Ramam: Realization of freestanding InP membranes on Si by low-temperature wafer bonding and stress analysis using micro-Raman spectroscopy, Appl. Phys. Lett. 88, 221901 (2006)
232. M.A. Shah, P. Jisheng, V. Shanmugan, R. Akkipeddi: Fabrication of moisture-desensitized freestanding structures from InP for photonic-MEMS applications, J. Electrochem. Soc. 153, G7–G11 (2006)
233. T. Kusserow, N. Dharmarasu, H. Hillmer, T. Nakamura, T. Hayakawa, B. Vengatesan: Tailored stress in InP/GaInAs layers for InP/air-gap DBR-Filters with photonic crystals. IEEE/LEOS International Conference on Optical MEMS Applications, Big Sky, MT, pp. 88–89 (2006)
234. C.J. Tay, C. Quan, M. Gopal, L. Shen, R. Akkipeddi: Nanoindentation techniques in the measurement of mechanical properties of InP-based free-standing MEMS structures, J. Micromech. Microeng. 18, 025015 (2008)
235. E. Sillero, D. López-Romero, A. Bengoechea, M.A. Sánchez-García, F. Calle: Fabrication and stress relief modelling of GaN based MEMS test structures grown by MBE on Si(111), Phys. Status Solidi C 5, 1974–1976 (2008)
236. M.A. Shah, S. Vicknesh, L.S. Wang, J. Arokiaraj, A. Ramam, S.J. Chua, S. Tripathy: Fabrication of freestanding GaN micromechanical structures on silicon-on-insulator substrates, Electrochem. Solid State Lett. 8, G275–G279 (2005)
237. S. Tripathy, V.K.X. Lin, S. Vicknesh, S.J. Chua: Micro-Raman probing of residual stress in freestanding GaN-based micromechanical structures fabricated by a dry release technique, J. Appl. Phys. 101, 063525 (2007)
238. K. Hjort: Sacrificial etching of III-V compounds for micromechanical devices, J. Micromech. Microeng. 6, 370–365 (1996)
239. E. Peiner, K. Fricke, I. Behrens, A. Bakin, A. Schlachetzki: Hetero-micromachining of epitaxial III/V compound semiconductors, Sens. Act. A 85, 324–329 (2000)
240. K. Fricke, E. Peiner, M. Chahoud, A. Schlachetzki: Fracture properties of InP microcantilevers by hetero-micromachining, Sens. Act. A 76, 395–402 (1999)
241. H. Yamaguchi, R. Dreyfus, S. Miyashita, Y. Hirayama: Fabrication and elastic properties of InAs freestanding structures based on InAs/GaAs(111) heteroepitaxial systems, Physica E 13, 1163–1167 (2002)

242. H. Yamaguchi, S. Miyashita, Y. Hirayama: Mechanical and piezoresistive properties of InAs/AlGaSb cantilevers, Appl. Surf. Sci. 237, 645–649 (2004)
243. K. Deng, K.P. Kumar, L. Li, D.L. Devoe: Piezoelectric disk resonators based on epitaxial AlGaAs films, J. Microelectromech. Syst. 16, 155–162 (2007)
244. T. Abe, M.L. Reed: Low strain sputtered polysilicon for micromechanical structures. Proceedings of the 9th International Workshop on Micro Electro Mechanical Systems, San Diego, CA, pp. 258–262 (1996)
245. K.A. Honer, G.T.A. Kovacs: Integration of sputtered silicon microstructures with prefabricated CMOS circuitry, Sens. Act. A 91, 392–403 (2001)
246. P. Pal, S. Chandra: RF sputtered silicon for MEMS, J. Micromech. Microeng. 15, 1536–1546 (2005)
247. N. Ledermann, J. Baborowski, J.P. Muralt, N. Xantopoulos, J.M. Tellenbach: Sputtered silicon carbide thin films as protective coating for MEMS applications, Surf. Coatings Technol. 125, 246–250 (2000)
248. S. Inoue, T. Namazu, H. Tawa, M. Niibe, K. Koterazawa: Stress control of a-SiC films deposited by dual source dc magnetron sputtering, Vacuum 80, 744–747 (2006)
249. V. Bhatt, S. Chandra: Silicon dioxide films by RF sputtering for microelectronic and MEMS, J. Micromech. Microeng. 17, 1066–1077 (2007)
250. E. Peiner, A. Tibrewala, R. Bandorf, H. Luthje, L. Doering, W. Limmer: Diamond-like carbon for MEMS, J. Micromech. Microeng. 17, S83–S90 (2007)
251. J.P. Sullivan, T.A. Friedmann, K. Hjort: Diamond and amorphous carbon MEMS, MRS Bull. 26, 309–311 (2001)
252. T.A. Friedmann, J.P. Sullivan, J.A. Knapp, D.R. Tallant, D.M. Follstaedt, D.L. Medlin, P.B. Mirkarimi: Thick stress-free amorphous-tetrahedral carbon films with hardness near that of diamond. Appl. Phys. Lett. 71, 3820–3822 (1997)
253. S. Cho, I. Chasiotis, T.A. Friedmann, J.P. Sullivan: Young's modulus, Poisson's ratio and failure properties of tetrahedral amorphous diamond-like carbon for MEMS devices, J. Micromech. Microeng. 15, 728–735 (2005)
254. N.D. Hoivik, J.W. Elam, R.J. Linderman, V.M. Bright, S.M. George, Y.C. Lee: Atomic layer deposited protective coatings for micro-electromechanical systems, Sens. Act. A 103, 100–108 (2003)
255. W.S. Yang, S.W. Kang: Comparative study on chemical stability of dielectric oxide films under HF wet and vapor etching for radiofrequency microelectromechanical system application, Thin Solid Films 500, 231–236 (2006)
256. T.M. Mayer, J.W. Elam, S.M. George, P.G. Kotula, R.S. Goeke: Atomic-layer deposition of wear-resistant coatings for microelectromechanical devices, Appl. Phys. Lett. 82, 2883–2885 (2003)
257. T.W. Scharf, S.V. Prasad, M.T. Dugger, P.G. Kotula, R.S. Goeke, R.K. Grubbs: Growth, structure, and tribological behavior of atomic layer-deposited tungsten disulphide solid lubricant coatings with applications to MEMS, Acta Mater 54, 4731–4743 (2006)
258. C.F. Herrmann, F.W. DelRio, D.C. Miller, S.M. George, V.M. Bright, J.L. Ebel, R.E. Strawser, R. Cortez, K.D. Leedy: Alternative dielectric films for rf MEMS capacitive switches deposited using atomic layer deposited Al_2O_3/ZnO alloys, Sens. Act. A 135, 262–272 (2007)
259. Y.-J. Chang, J.M. Gray, A. Imtiaz, D.S. Seghete, T.M. Wallis, S.M. George, P. Kabos, C.T. Rogers, V.M. Bright: Micromachined resonators of high Q-factor based on atomic layer deposited alumina, Sens. Act. A 154, 229–237 (2009)
260. M.K. Tripp, C. Stampfer, D.C. Miller, T. Helbling, C.F. Herrmann, C. Hierold, K. Gall, S.M. George, V.M. Bright: The mechanical properties of atomic layer deposited alumina for use in micro- and nano-electromechanical systems, Sens. Act. A 130–131, 419–429 (2006)
261. M.M. Rahman, R. Tero, T. Urisu: Shrinking of spin-on-glass films induced by synchrotron radiation and its application to three dimensional microfabrications, Jpn. J. Appl. Phys. 43, 3941–3944 (2004)

262. A. Yasseen, J.D. Cawley, M. Mehregany: Thick glass film technology for polysilicon surface micromachining, J. Microelectromech. Syst. 8, 172–179 (1999)
263. R. Liu, M.J. Vasile, D.J. Beebe: The fabrication of nonplanar spin-on glass microstructures, J. Microelectromech. Syst. 8, 146–151 (1999)
264. L.A. Liew, W. Zhang, V.M. Bright, A. Linan, M.L. Dunn, R. Raj: Fabrication of SiCN ceramic MEMS using injectable polymer-precursor technique, Sens. Act. A 89, 64–70 (2001)

Chapter 3
Additive Processes for Metals

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Abstract Metals are vital building blocks for MEMS. Pure metals and metal alloys are employed in microsystem design to achieve a wide array of functionality. Common examples include electrical conductors, mechanical structures, magnetic elements, thermal conductors, optical reflectors, and more. In this chapter, additive processes for metals are discussed in the context of their application in MEMS. Particular attention is paid to MEMS-centric processing technologies, where thick metal layers are often required. Basic guidelines are given for material selection, and fabrication recipes are provided as a starting point for process development.

3.1 Introduction

From the Bronze Age through the Iron Age, and even into modern times, metals have fueled technological growth and played a key role in shaping society. All but 25 of the 120 elements on the periodic table are considered metals, and many are naturally abundant on earth. Elemental metals are generally known to exhibit high electrical conductivity, high thermal conductivity, relatively high physical density, and good mechanical ductility. In addition, metals can be combined with each other or with nonmetals to form innumerable metal alloy combinations with diverse electrical, mechanical, magnetic, thermal, and optical material properties. The availability, adaptability, and functionality of metals make them one of the most widely used engineering materials, not only at the macroscale, but also for microscale applications.

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3.1.1 Overview

Metals are widely used for MEMS in many different functional roles. Metals are ubiquitously used as electrical interconnections for their high electrical conductivity. Metals also exhibit advantageous mechanical properties, so they are commonly employed as mechanical elements, both rigid structures and flexures. Metals are also good thermal conductors, and thus attractive for thermal applications. Certain metals exhibit ferromagnetic behavior and can be used to create or guide magnetic fields. For optical applications, metals are used to provide reflective, mirrorlike surfaces. Metal coatings are also used to encapsulate other materials, for example, to prevent oxidation or create hermetic seals, and thin interfacial metal layers act to enhance adhesion or prevent diffusion.

Material selection usually begins by identifying and prioritizing the desired material properties. For example, if a microstructure is intended as a mechanically strong electrical conductor, one may begin by searching for materials with high electrical conductivity and high elastic modulus. Fortunately, bulk metals and metal alloys have been widely studied for hundreds of years, and much of what is known about bulk material properties largely applies at the microscale. With the emergence of microelectronics, MEMS, and nanotechnology, there is also a growing wealth of knowledge about unique material behavior at the micro- and nanoscale.

Once a specific metal or class of metals is identified, the next step is to determine how to fabricate and integrate the material into a microdevice. Although bulk machining of metals is usually a top-down process (e.g. physical milling of a bulk piece of metal), micromachining of metals is usually bottom-up (atom-by-atom, layer-by-layer deposition). Herein lies a major complication. For macroscale applications, individual components are usually fabricated separately and then assembled together. The individual system components can be machined independently of one another. In MEMS fabrication, this is usually not the case; devices are manufactured in a sequential integrated fashion by selectively adding and subtracting layers on a planar substrate. This manufacturing approach places limitations on materials and structure geometries. Furthermore, microfabrication creates a complex interplay between the fabrication process and the resulting material properties. These topics are further discussed throughout this chapter.

Methods for metal deposition can be categorized into three groups: physical vapor deposition (PVD), chemical vapor deposition (CVD), and electrochemical deposition (ECD). For MEMS, PVD and ECD are more commonly used, and thus are the primary focus of this chapter. Although CVD finds widespread usage in semiconductor devices and integrated circuits for conformal deposition of thin metal films, it is not as popular for MEMS fabrication because of film thickness limitations and process complexity.[1]

The remainder of Section 3.1 discusses general tradeoffs for the various fabrication approaches available for depositing metals and metal alloys. Section 3.2

[1] See Chapter 2 (specifically Section 2.3) for general information on CVD.

provides a more detailed discussion of PVD methods for metals, including evaporation, sputtering, and pulsed-laser deposition. Section 3.3 describes ECD methods, including both electroplating and electroless plating. Section 3.4 describes LIGA and UV-LIGA processes, a key technological advancement in the history of MEMS. Finally, Section 3.5 presents material properties and process selection guidelines for metals.

3.1.2 Fabrication Tradeoffs

There are many fabrication-related tradeoffs that must be considered for micromachining of metals. The final material properties of a metal are often highly dependent on the film thickness, deposition method, and specific processing conditions. This creates interesting design/fabrication/integration challenges and compromises. In addition, because of these geometrical and process dependencies, the material properties for metal films reported in the literature vary widely. Thus, although basic starting recipes may be found (and many are provided below), some process development is usually required for fine-tuning of the metal properties to meet a specific need.

In addition to differing material properties, various fabrication methods yield different microstructural features and process integration issues. For example, evaporation usually results in poor step-coverage but high film purity. Sputtering, on the other hand, can provide good sidewall coverage, but with lower film purity. PLD often affords high deposition rates, but is usually limited in deposition area. In contrast to these PVD methods, electroplating and electroless plating rely on chemically "growing" the metals. This enables selective deposition (e.g. using photoresist masks) only where needed, thus avoiding additional process steps and time required for film patterning via post-deposition chemical etching[2] or liftoff.[3] In addition, the material waste (overage) associated with PVD can have significant cost implications, especially for thick layers of expensive precious metals.

The required film thickness also affects fabrication process selection. For example, thinner metal films may be used as coatings or as interfacial layers. In contrast, to better conduct heat or to provide heftier mechanical structures, thicker metal films may be required. Evaporation and electroless plating are better suited for thinner films (e.g. less than 1 μm), whereas thicker films demand the faster deposition rates afforded by sputtering, PLD, or electroplating. For commercial manufacturing, there are also numerous tradeoffs involving cost, throughput, reliability, and repeatability.

The deposition of alloys raises additional issues. Different alloy ratios are often required to enhance a material property such as electrical resistance, mechanical hardness, magnetic permeability, and the like. In cases where a very specific alloy

[2] See Chapters 7 and 8 for more information on chemical etching.

[3] See Chapter 9 (specifically Section 9.2.5.5) for more information regarding liftoff.

ratio is required, stoichiometric control is a major consideration. Reliably maintaining a specific alloy ratio over long periods of time is critical for repeatable, large-scale manufacturing. In addition to repeatability and control, there is another important fabrication-related aspect for alloys: the ability (or inability) to vary the alloy ratio. This is especially important for process development and for fine-tuning of alloy composition. Moreover, deposition methods that permit on-the-fly alloy control can be used to create graded alloys, multilayers, or other complex structures.

The different metal deposition methods offer varying degrees of alloy control. Evaporation of alloys is often discouraged because of the disparate and highly temperature-dependent vapor pressures of different metal constituents. This makes control of alloys difficult with conventional evaporation systems. In contrast, sputtering and PLD permit deposition of many different alloys with fairly repeatable alloy control, but adjusting the alloy ratio requires changing the metal target. This can create time-consuming and costly process development cycles. For electroplating, the alloy ratio can sometimes be readily adjusted by varying the electroplating current density without strong influence on the properties of the deposit. Unfortunately, the alloy ratio may also be sensitive to other process conditions such as pH, temperature, or stirring, so repeatability is sometimes difficult. Electroless plating is less commonly used for alloy deposition because of the complex interdependent factors that determine the composition. See Table 3.1 for a general summary.

Table 3.1 General tradeoffs for metal deposition

Fabrication process	Deposition rate	Deposition area	Film purity	Alloy control	Equipment complexity
Evaporation	Slow	Very large	High	Poor	Moderate
Sputtering	Moderate	Large	Moderate	Good	High
PLD	Moderate	Small	High	Good	High
Electroplating	Fast	Large	Moderate	Fair	Low
Electroless plating	Moderate	Large	Moderate	Fair	Very low

3.2 Physical Vapor Deposition

Physical vapor deposition (PVD) methods rely on the physical transfer of metal atoms from a metal source to the wafer substrate, unlike chemical methods, which employ a chemical reaction. Different physical phenomena can be used to drive the process, as described below.

3.2.1 Evaporation

Evaporative deposition, or more commonly just "evaporation," is a fairly straightforward method for metal deposition. The basic concept is to heat a metal sufficiently to create a vapor, which diffuses and recondenses in solid form on other surfaces.

This process is usually performed in high-vacuum conditions (below 10^{-5} torr) so as to limit gaseous molecular scattering and to create a high-purity process environment. Note that, although the metal to be evaporated is obviously very hot, the wafer substrate usually remains at room temperature, unless intentionally heated or cooled. Also, because of the very low chamber pressures, the metal vapor tends to follow a straight path, leading to very directional deposition and poor sidewall coverage.

A typical system comprises a process chamber, a vacuum system, and a metal heating system, as shown in Fig. 3.1. Wafers are usually mounted upside down on a hemispherical chamber ceiling, which may include a planetary system to rotate the wafers for improved uniformity. The metal to be deposited – known as the "charge" – is placed in metal "boat" or ceramic crucible. The chamber is then closed and evacuated to a base pressure of 10^{-6} torr or lower. Then, the metal is heated usually to 500–2500°C (depending on the metal) to increase the vapor pressure. After a warm-up period, a physical shutter is used to precisely start and end the deposition onto the wafers. A quartz crystal microbalance (QCM) mounted inside the chamber monitors the deposition, and can provide feedback signals for automated control.

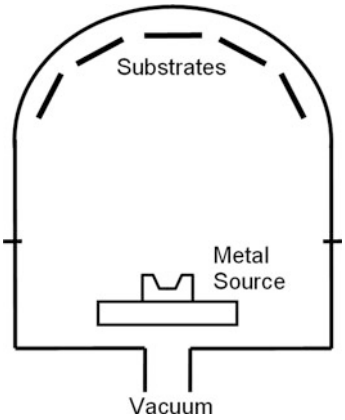


Fig. 3.1 Schematic of evaporation system

3.2.1.1 Thermal Evaporation

The simplest evaporation systems use joule heating to heat the metal charge. The dissipative heat can be created by direct conduction currents or magnetic-field-induced eddy currents. In the simpler conductively heated systems, high currents are passed through wound coils or a small metal boat (usually tungsten), inside of which sits the charge. The resistive heating of the boat facilitates deposition of relatively low-melting-point metals such as Ag, Al, and Au.

Evaporation of higher-melting-point refractory metals such as Ta, W, Mo, and Ti is challenging because these require very high temperatures to achieve reasonable vapor pressures and deposition rates [1]. Because of this, the use of metal boats and direct conductive heating may not be permissible. Instead inductive heating can be used where the metal sits in a ceramic crucible that is surrounded by a coil. RF

excitation of the coil is used to induce eddy currents in the metal. This approach permits a wider range of metals, but the crucible itself may become very hot, which can result in contamination.

3.2.1.2 E-Beam Evaporation

Another configuration for evaporation uses a directed electron beam to bombard the metal charge. The electron beam source is usually underneath the metal charge. Strong magnetic fields are used to steer the electron beam in a 270° circular arc to impinge on the charge. Although more complicated, the advantage of this approach is that the electron beam heats a central portion of the charge: the outer area of the charge and crucible remain at lower temperatures, so as to minimize contamination.

3.2.1.3 Issues with Alloys

Evaporation of alloys with precise alloy composition can be quite challenging. The basic problem is that evaporation relies on heating to increase the vapor pressure and thus control deposition rate. The vapor pressure and deposition rate of an elemental metal are usually very sensitive to temperature, and different metals require vastly different temperature ranges for evaporation. For single-element deposition, precise control of the deposition rate is relatively unimportant, so long as the final film thickness is controlled. This is easily accomplished using a QCM to stop the deposition process at the predetermined film thickness.

Consider, however, deposition of a binary alloy. In a single-source system, a metal alloy can be used as the charge, but at a given temperature, the two metals in the alloy will evaporate at different rates, resulting in a different alloy ratio in the deposited layer. Attempts can be made to compensate for this, but impracticably precise temperature control may be required. Another approach is to coevaporate different metals from independently heated crucibles. This allows independent control of the evaporation rates, but because of the temperature sensitivity of the evaporation process, and the inability to monitor the independent evaporation rates easily, precise alloy control remains very challenging. One alternative is to create a multilayer stack by alternating deposition of the constituent elements. After deposition, a heat treatment can be used to interdiffuse the metals to form the desired alloy. This approach, however, is more complicated, more time-consuming, and requires a substrate that can withstand the high-temperature postdeposition heat treatment.

It should be noted that graded alloys or multilayers can be easily achieved using a multisource evaporation system. However, because of the difficulty of alloy control, evaporation is better suited for pure metals or for metal alloys where precise composition is not necessary.

3.2.2 Sputtering

Sputtering is a physical process or phenomenon, where accelerated ions, usually Ar^+, knock out atoms in a solid target by bombardment in a potential gradient

environment. During the bombardment, momentum exchange occurs between the ions and the atoms of the surface of the target. The energized atoms are volatile and spread out as a vapor to land on the vicinity surface and the sample substrate. The sputtering process requires a vacuum environment, which is prepared by pumping out a stainless steel chamber enclosing the anode, the cathode, the target, the substrate, and so on. The chamber is evacuated to a base pressure of 10^{-6} torr or lower. Then a bombardment gas, usually Ar, is introduced to the chamber and maintained around 1–10 mtorr level. The Ar gas is ionized into Ar^+ by applying bias voltage between the anode and the cathode. Depending on the voltage waveforms used, the sputtering process is categorized as either direct current (DC) sputtering or radio frequency (RF) sputtering, as shown in Fig. 3.2.

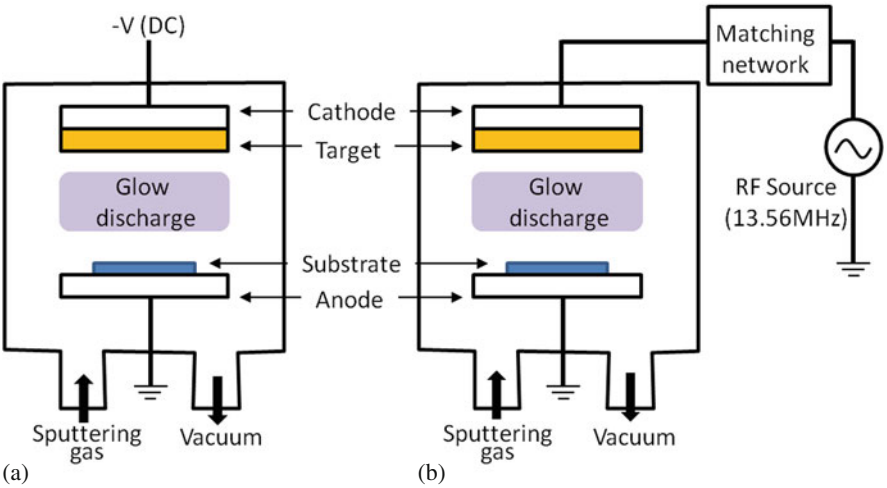


Fig. 3.2 Schematics of (**a**) DC and (**b**) RF sputtering systems

To obtain uniform thickness of a thin-film metal layer, mechanical movement such as rotation of the substrate holder can be used during the sputtering process. The rotational speed of the stage ranges from 10 to 30 rpm. The deposition rate is a function of many parameters including target-to-substrate distance, ion energy, the mass of the ion species, the mass of the target material, and the like [2].

3.2.2.1 DC Sputtering

For the sputtering of electrically conductive materials such as Al, Ti, Cr, Cu, Ag, Au, Pt, and W, a DC power source is used to energize the Ar^+ ions to bombard the target material placed on the cathode. The DC sputtering system, as depicted in Fig. 3.2a, consists of the DC power supply, cathode, a metal target attached to the cathode, Ar^+ plasma generated by high-voltage application, and an anode on which a sample wafer can be placed. The negatively biased metal target is bombarded by argon ions from the plasma, ejecting one or more metal atoms. Some of these ejected atoms are

transported and deposited on the substrate wafers. The deposition rate is increased as the sputtering power is increased, however, too much power causes damage on the substrate. To counteract this effect, magnetron sputtering has been introduced to increase the deposition rate. A magnet placed behind the target creates a field that guides electron movement near the target, causing more efficient ionization of Ar without excessively high voltages.

3.2.2.2 RF Sputtering

As an alternative to the DC supply, RF power systems can be used, as shown in Fig. 3.2b. The RF sputtering system also requires a DC bias voltage to generate plasma. After plasma is generated, however, the major driving force acting on the argon ions is exerted by the alternating current source. Typically the 13.56 MHz industry, science, and medicine (ISM) frequency band is used. Because alternating currents can flow across dielectric materials, RF sputtering systems can deposit not only electrically conducting materials, such as metals, but also dielectric materials, such as SiO_2, Si_3N_4, and glass, which are not achievable with DC sputtering due to charging effects. Also, by reversing the electrical connections, the substrate can be bombarded as opposed to the metal target. This process is often used to clean the substrate surface before depositing the target material.

3.2.2.3 Step Coverage

In contrast to the evaporation process, sputtering provides reasonably conformal coatings on uneven surfaces. This is particularly useful for the metallization of three-dimensional (3-D) MEMS structures as well as the metal interconnect of integrated circuits. The step-coverage of a sputtered thin film in a via hole has been calculated [3, 4], where the profile shows a high deposition rate on the top surface and a low deposition rate on the sidewall. As a result, the sidewall thickness tapers down toward the bottom. For a very high aspect ratio, the bottom portion may not have sufficient metal coverage due to limited mass transfer into the narrow entrance of the via hole and the higher pressure environment in the chamber. This effect is depicted in Fig. 3.3. This kind of poor coverage is more significant in high-aspect-ratio vias or trenches as compared to high-aspect-ratio pillars or walls.

The step coverage can be improved by substrate heating to enhance surface diffusion or by applying an RF bias to the wafers to introduce surface bombardment resulting in redeposition on the sidewalls [1]. The heating approach may be applicable to the metal interconnect process for ICs, where the insulating layer is a temperature-tolerant material such as SiO_2, however, it may not be directly applicable for the metallization of 3-D MEMS structures where the structural material is often a temperature-intolerant polymer. Step-coverage of thin films for very high-aspect-ratio MEMS structures remains a challenging area. Alternatively, electroless plating may be used for the thin film metallization of such high-aspect-ratio polymeric structures.

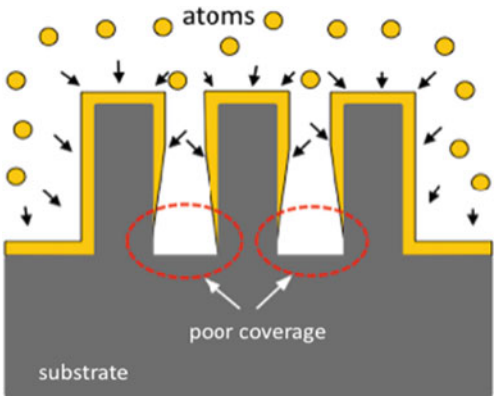


Fig. 3.3 Sputtered metal deposition in a densely placed high-aspect-ratio structure

3.2.2.4 Other Issues in Sputtering

One concern in thin-film deposition using sputtering (or evaporation) on a thick 3-D polymeric layer is that the residual solvent or moisture tends to degas under high vacuum conditions, resulting in poor adhesion between the polymer and thin-film metal layer. To prevent degassing effects, an additional hardbake step is recommended before the sputtering or evaporation process can be used.

One feature found in many sputtering systems is the ability to "clean" the substrate before the metal deposition by sputter etching. This cleaning step can improve adhesion of the metal. Sputter etching can be implemented either by reversing the electrical connections or by placing negative bias on the substrate with respect to the plasma, resulting in increasing ion bombardment on the substrate. Increasing the incident ion energy increases the adatom (Ar ion) mobility, which can aid in cleaning the deep sidewalls of a 3-D structure, thereby improving step-coverage in deep-etched features [5]. However, high sputter etch rates may cause substrate damage.

Although sputtering of alloy is commonplace, there are several important issues and approaches. In sputtering, the deposited film composition is usually fairly close to that of the bulk target, so alloys can be rather easily obtained. However, different elements in the target alloy may exhibit different sputter yields, causing composition variation. To achieve better control of stoichiometry, a multiple target system may be used, where the power of each target can be individually controlled to alter the final composition of the alloy layer. Also, by using a composite target with different regions of concentration or by changing electrical properties of the plasma, the composition of the deposited layer can be controlled [6].

Moreover, sputtered compounds can intentionally have a very different composition from the sputter target by adding reactive gaseous precursors during the deposition. Reactive sputtering is a process in which the normally inert sputter gas is replaced by an inert/reactive mixture [1]. For example, TiN, one of the most popular diffusion barrier layers in IC fabrication, can be deposited using reactive sputtering. By controlling the partial pressure of nitrogen in the sputtering system, the composition of TiN can be controlled.

Stress is also an important issue for sputtered films. A thin film deposited on a substrate is subjected to either tensile or compressive stress as influenced by the base layer and deposition conditions. One component of the stress – known as extrinsic stress – is due to thermal expansion mismatch of the film with the substrate. This stress may be significant if the wafer temperature varies (intentionally or unintentionally) from room temperature during the film deposition. In addition, large intrinsic stresses may also occur depending on deposition rate, film thickness, and the background chamber environment. In many cases, efforts are made to minimize these stresses. Alternatively, for MEMS devices, these stresses can be put to good use to realize devices such as bimorph actuators or stress-engineered 3-D structures [7, 8].

3.2.3 Pulsed Laser Deposition

Pulsed laser deposition (PLD) is another method for depositing metals, although much less often used for MEMS. As shown in Fig. 3.4, the system uses a high-energy laser beam (typically 10^8 W/cm^2) to strike a metal target within a vacuum chamber. The laser beam melts, evaporates, and ionizes a region of the target. This ablation process creates a vapor plume that transfers material to the sample wafer.

One major advantage of PLD for MEMS applications is precise stoichiometry/composition control and relatively fast deposition rates. Ideally the deposited material possesses the same chemical composition as the metal target. High quality crystalline deposits are also possible with substrate heating. The biggest drawback is that most PLD systems can only provide uniform deposition over a small surface area, sometimes only about one square centimeter. This decreases the utility of PLD for volume manufacturing. Despite this drawback, PLD finds application where

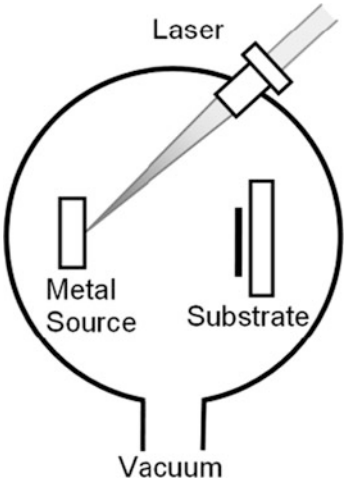


Fig. 3.4 Schematic of pulsed laser deposition system

precise stoichiometric control is paramount, especially for complex multielement materials. For metallic systems, this alloy control is beneficial for realizing high-performance magnetic materials and superconductors. PLD also finds widespread application for many other complex nonmetallic films, such as oxides, nitrides, and semiconductors.

The exact process and resulting film composition and structure are dependent on the laser parameters, chamber pressure/atmosphere, sample temperature, and sample surface quality. The complex physical and chemical interactions are the subject of ongoing research.

3.3 Electrochemical Deposition

Electrochemical deposition involves the reduction of metal ions from aqueous, organic, or fused-salt electrolytes. The reduction of metal ions M^{z+} in aqueous solution is represented by

$$M^{z+}\ \text{(metal ion in solution)} + z\,e^{-}\ \text{(electrons)} \rightarrow M\ \text{(metal deposit)}$$

Two processes can be used to provide the electrons for the reduction reaction: (1) electroplating (or electrodeposition), where an external power supply provides the electrons, or (2) electroless deposition, where a reducing agent provides the electrons.

In MEMS electrochemical deposition is commonly used to deposit surface coatings, or in the case of electroforming, for producing an entire microstructure or device. In electroforming, microstructured molds of different materials (e.g., polymers/resist, silicon) are electrochemically filled with metals such as nickel, copper, gold, or various metal alloys. More details can be found in Section 3.4.

3.3.1 Electroplating

The material properties of electroplated metals or alloys are strongly influenced by the chemistry of the electrolyte (e.g., type and concentration of ions, pH, type of additives), the physical parameters of the process (e.g., temperature, fluidics, current), and the property of the substrate (surface quality, shape). Depending on the metal to be plated and/or on the shape of the desired microstructures, the electroplating process has to be adapted to the specific application. The basics of electrochemical deposition can be found in several excellent books (e.g., [9–11]) and are summarized in this section. In addition, starting recipes are provided for some of the most common electroplated metals for MEMS: nickel, copper, gold, and some nickel alloys.

3.3.1.1 Electrochemical Reactions

The general setup and operation of an electrochemical deposition cell are shown in Fig. 3.5. Two electrodes are immersed into an electrolyte. By applying an electric

current, reduction (electron uptake) takes place at the cathode, and oxidation (electron liberation) occurs at the anode. In the case of electroplating, the substrate serves as the cathode, and metal ions are reduced to form a solid lattice. The anode can be soluble, meaning it is dissolved via oxidation during the electroplating process. The two partial reactions are expressed by the following equations.

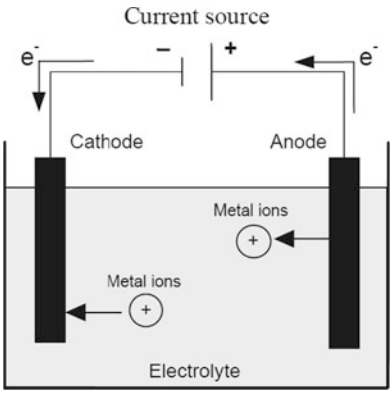


Fig. 3.5 Schematic of a general electrochemical deposition cell (using soluble anode)

Reduction (cathode):	$M^{z+} + z\,e^- \rightarrow M$ Deposition of metal
Oxidation (anode):	$M \rightarrow M^{z+} + z\,e^-$ Dissolution of metal (for a soluble anode)

The steady oxidation of the anode (a metal to be deposited) ensures a constant replenishment of metal ions in the electrolyte. Sometimes inert anodes such as platinum are used, for example, in gold electroplating. In this case, replenishment of metallic ions in the electrolyte is solely provided by manual addition of metal salts to the plating bath.

The theoretically deposited mass m_{theo} can be calculated from the electrochemical Faraday's law as

$$m_{\text{theo}} = \frac{M^* I^* t}{z^* F} \tag{3.1}$$

where M = Molar mass the deposited metal; I = Current; t = Time; z = Valency; F = Faraday constant.

Other reactions also can occur due to decomposition of water. By the oxidation of water, oxygen gas can be produced at the anode. By the reduction of water, hydrogen gas can be released at the cathode. Other components of the electrolyte can also react at the electrodes. The overall current is thus distributed to these different reactions.

The percentage of the total current associated with the reduction of metal is defined as the cathodic current efficiency γ and can be calculated by the quotient of the effective deposited mass m_{eff} and the theoretical deposited mass m_{theo},

$$\gamma = \frac{m_{\text{eff}}}{m_{\text{theo}}}. \tag{3.2}$$

If hydrogen production at the cathode cannot be suppressed, it usually severely reduces the current efficiency of the deposition process. Another adverse effect is the rise of the pH at the electrode surface, which leads to the buildup and incorporation of metal hydroxides into the deposits, leading to a brittle deposit. The accumulation of hydrogen bubbles, which adhere on the surface, can also cause pores in the deposit.

3.3.1.2 Deposition Process

In the bulk electrolyte, cations are enclosed in a complex shell. This complex shell consists of water molecules (hydration shell) or other complexing agents such as sulfite or cyanide. Before applying a current, the ion concentration is homogeneous at the electrode surface and in the bulk solution. When applying a current, the metal ion is consumed at the electrode, and this depletion region extends farther away into the bulk as the deposition proceeds.

Movement of the complexed metal ions in the electrolyte is governed by three different mass transport mechanisms: migration, convection, and diffusion. In most deposition processes the conductivity of the electrolyte is relatively high, and the applied potentials are moderate. As a consequence, most of the electrical field drops across the electrical double layer in front of the electrodes, and field-induced migration is minimal. Therefore the predominant transport mechanisms are usually convection (due to stirring or agitation), which dominates in the bulk electrolyte, and diffusion, which dominates near the surface of the electrodes.

The reduction of the metal ions at the cathode is very complex and can be divided into four parts: (1) diffusion of the solvated or complexed metal ions from the bulk solution to the electrode surface, (2) dehydration and transport of the cations through the electric double layer, (3) cationic reaction at the solution–solid interface (ion uptake and electron transfer), and (4) surface migration and incorporation of the adsorbed metal atoms into the metal lattice. Figure 3.6 depicts the overall process.

The ion diffusion is described as follows. The region immediately next to the cathode is characterized by a fictitious Nernst diffusion layer, where the gradient of ion concentration is assumed constant, as shown in Fig. 3.7. The thickness of this layer δ is strongly influenced by convection (agitation) in the electrolyte, but is typically on the order of tens to hundreds of micrometers. In stirred electrolytes the thickness of the diffusion layer will be determined by this forced convection, whereas in unstirred electrolyte baths the diffusion layer increases with time.

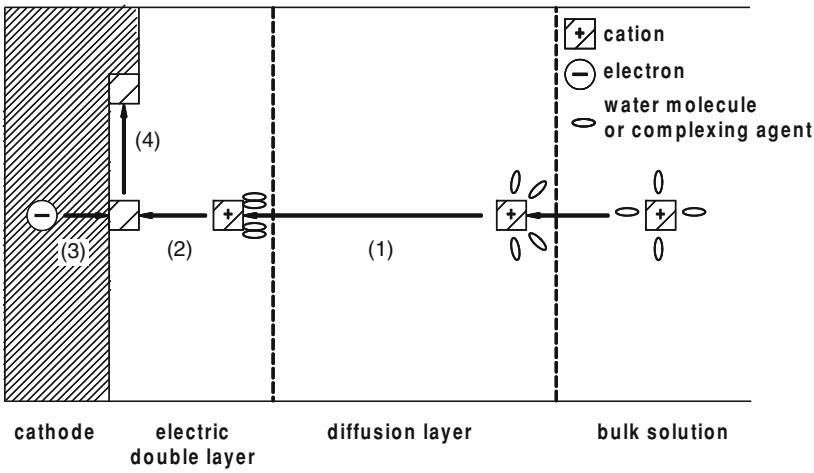


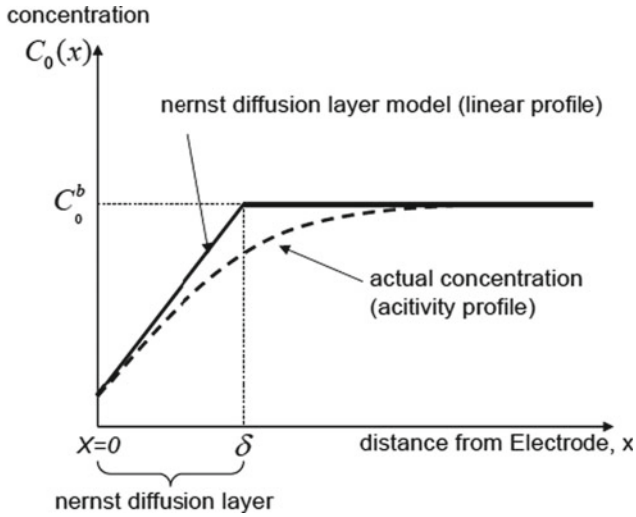
Fig. 3.6 Schematic diagram of the electrochemical deposition process

The deposition rate can be enhanced by increasing the current density, up until the ion concentration at the cathode approaches zero. The current density at which this occurs is called the limiting current density. The limiting current density (and hence maximum deposition rate) can generally be increased by increasing the cation concentration; by increasing the temperature, thus increasing the diffusion coefficient; and by increasing the convection (e.g., stirring the solution), resulting in a smaller diffusion layer. Modifying the electrolyte chemistry, especially via complexing agents, can also influence the limiting current density.

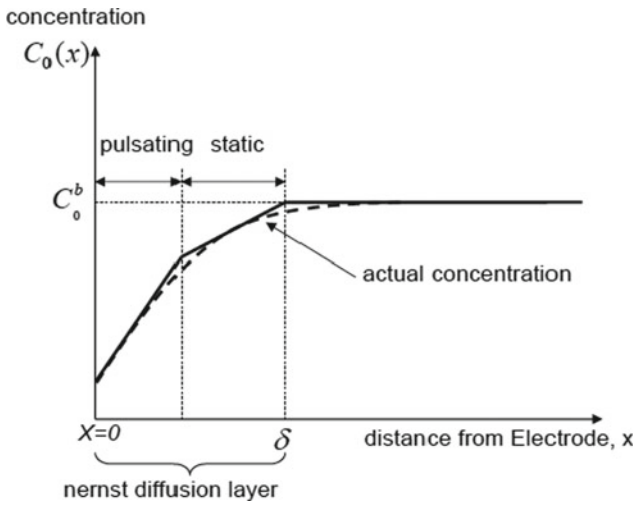
In the case of pulse-plating, the pulse current density is limited by the depletion of ions in the pulsation layer, whereas the average current density is limited by the concentration gradient in the outer stationary diffusion layer. Thus two diffusion layers can be defined: a pulsation layer in the immediate vicinity of the cathode and a stationary layer up to the point where the mass transfer is controlled by convection.

Once the cations reach the cathode surface by means of mass transfer, there is another barrier to overcome before they lose charge and are incorporated into the crystal lattice. That barrier is called the electric double layer. The simplest model of the double layer structure is given by the Helmholtz model, as depicted in Fig. 3.8. The double layer represents an organized arrangement of positive ions from the solution to compensate for the negative charges on the surface, forming an interface region similar to a parallel plate capacitor. The thickness of this layer is on the order of a few nanometers [12]. The cations to be deposited have to penetrate through the electric double layer, where they shed their hydration (or complex) shell. Then they acquire electrons in the reduction process and become adsorbed adatoms.

The final step in the formation of a crystalline metal deposit is the incorporation of the adatoms into the lattice. The adatoms are preferentially incorporated at active lattice sites such as grain boundaries, imperfections, or pre-existing built-up adatom



(a)



(b)

Fig. 3.7 Concentration of metal ions as a function of distance from the cathode (**a**) for direct current plating and (**b**) for pulse current plating

clusters on the surface. If the adsorption of an adatom ensued away from an energetically stable position, surface diffusion may transport the adatom to another active lattice site on the surface. The process of either building new grains (nucleation) or contributing to the growth of existing grains defines the formation of metal deposits in electroplating. Additional inhibitors in a plating bath can influence this nucleation

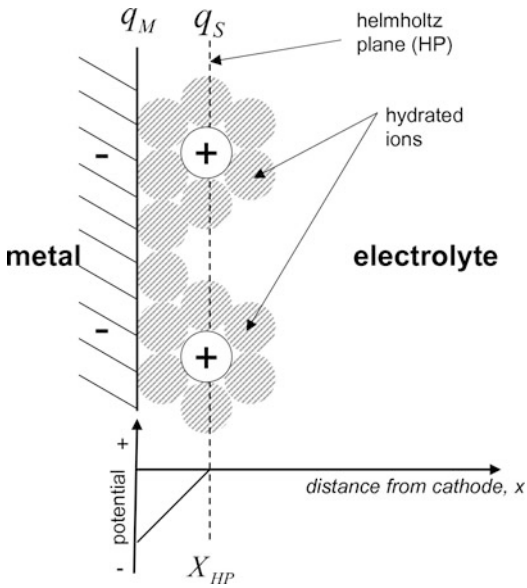


Fig. 3.8 Helmholtz model of the electric double layer. X_{HP} outer Helmholtz plane; q_M^- negative-charged metal surface; q_S positive-charged solution side of the interface

and therefore the growth processes that affect the properties of the deposit such as hardness, internal stress, and so on.

3.3.1.3 Overpotential

In the equilibrium condition (absence of external current), the potential of an electrode is denoted as E_h. As a result of a current flowing through the electrolyte the potential of the given electrode is changed to E. The difference between these two potentials is defined as overpotential

$$\eta = E - E_{\mathrm{h}} \tag{3.3}$$

The overpotential arises from the different electrochemical mechanisms associated with the reactions and movement of the ions or adatoms. The total overpotential is the sum of the individual overpotentials associated with each of these mechanisms. As a result, any one can be rate-determining for the electrodeposition. The diffusion overpotential η_{diff} arises due to mass transport through the diffusion layer. If this step is the slowest, the reaction is called diffusion-controlled. The activation overpotential η_{act} is associated with transfer of ions and electrons across the electric double layer and the transfer of the electrons. Therefore η_{act} is directly related to the electrode material. If the ion and electron transfer at the metal–solution interface is the most inhibiting step, the process is considered activation-controlled. The process by which the uncharged adatoms either form new grains or contribute to the growth of existing grains is associated with the crystallization overpotential η_{crys}. Ohmic

overpotential η_{ohm} stems from the resistivity of the electrolyte. Although the contribution of each overpotential deserves consideration, the activation overpotential or the diffusion overpotential usually dominates.

3.3.1.4 Bath Composition

Every electrolyte contains metal salts. In addition, different inorganic or organic substances are added to improve either the performance of the electrolyte solution (e.g., conductivity) or the deposit quality (e.g., hardness, internal stress). Still other additives can be used for specific purposes. For example, saccharin is used to reduce the internal stress of nickel deposits [13], bromide is used for nickel anode activation [14], and As(III)-salt is used for brightening, grain-refining, and hardening of gold deposits [15]. Table 3.2 lists some typical additives and their function.

Table 3.2 Example chemical constituents of electrolyte solutions and their function

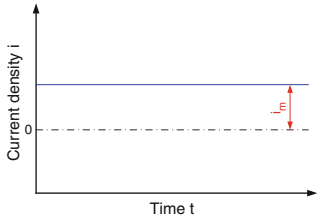
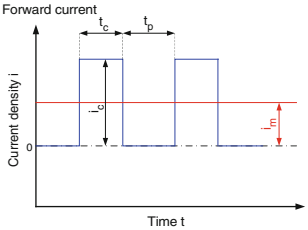
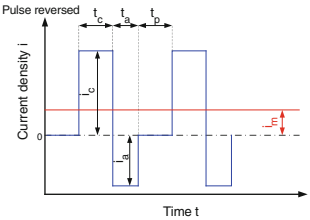
Type of substance	Function	Example
Metal salt	Provide metal ions	Ni(II)-sulfamate, Cu(II)-sulfate
Wetting agent (surfactant)	Reduce surface tension of electrolyte	Laurylsulfate, Fluorinated alkylsulfonates
Weak acid	Buffer the pH	Boric acid
Complexing agent	Stabilize electrolyte Influence selectivity of deposition process in alloy plating	1,2-Ethylendiamine Citrate
Salt	Increase conductivity of electrolyte	Sodium chloride
Brightener	Enhance or cause a bright surface of the deposit	Thiourea
Leveler	Reduce the surface roughness of the deposit	Coumarin

3.3.1.5 Current Waveform

In electroplating, besides the simple direct current, a variety of current modulations can be applied, such as triangular-, sawtooth-, or rectangular-shaped waveforms. Rectangular waveforms can be further divided into two characteristic variants: unipolar and bipolar current waveforms, both of which are commonly used. Table 3.3 illustrates the current-time-function of direct current, pulse forward current, and pulse reverse current. These current modulation schemes affect the plating mechanism and thus the chemical and microstructural properties of the deposited layer [16].

As can be seen in Table 3.3, the simplest case is the direct current mode. In contrast, the current waveform for pulsed electrodeposition (forward current) consists of cathodic pulses (t_c), separated by a current pause (t_p). Pulse reverse electrodeposition consists of a cathodic pulse (t_c), followed by an anodic pulse (t_a), where the current is reversed for a short time. In addition, the cycle can be extended

Table 3.3 Current waveforms for direct current, forward current, and pulsed reverse plating[a]

Current waveform	Mean current density
Direct current 	$i_m = i$
Forward current 	$i_m = \frac{i_c t_c}{t_c + t_p}$
Pulse reversed 	$i_m = \frac{i_c t_c - i_a t_a}{t_c + t_a + t_p}$

[a]The parameters defining a cycle are: i = current density, i_m = mean current density, i_c = cathodic current density, i_a = anodic current density, t_c = duration of the cathodic pulse, t_a = duration of the anodic pulse, t_p = duration of the pulse pause

by a pulse pause (t_p). During the cathodic pulse, metal ions are deposited on the cathode surface. Areas where field lines are concentrated are plated preferentially. Conversely, metal is preferentially removed in those areas during the anodic cycle. As shown later, the relative field strengths depend on the absolute current value. Hence, applying pulse reverse currents can result in a planarization of the deposit.

In pulse plating, a mean current density (i_m) can be defined, using the amplitudes and durations of the various pulses. This value represents the average charge density transferred during one cycle, which governs the deposition rate. Note that in order to generate the same mean current density as in the direct current case, significantly higher amplitude forward pulse current densities have to be applied.

The advantages of pulse plating have been studied extensively. Various metal alloy compositions have been optimized for morphology, magnetic properties, or mechanical properties (e.g. [17–20]). In the fabrication of printed circuit boards (PCBs), pulse reverse electroplating of copper is used in order to attain a uniform

filling of small vias and trenches. Pulse reverse methods can, to some extent, reduce the need for certain chemical additives and thus make bath control simpler.

3.3.1.6 Equipment

Various equipment can be used for electroplating, ranging from very simple to very complex. For laboratory use, the setup can be very simple, as shown in Fig. 3.9. This setup consists of a glass beaker, which contains the electrolyte solution. The electrolyte is stirred by a magnetic bar and heated by a hotplate. A temperature regulator connected to the hotplate automatically controls the temperature. A metal plate or titanium basket filled with metal pellets is used as the anode. An inert gas inlet for nitrogen or argon is sometimes used to prevent oxidation of the electrolyte. The power supply should be equipped with a pulse module to enable pulse plating if necessary. An oscilloscope may also be used to monitor the applied pulses.

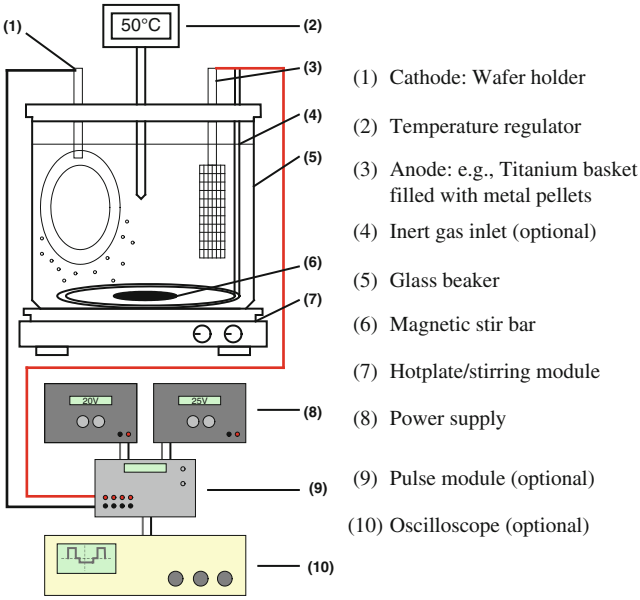


Fig. 3.9 Schematic of a laboratory-scale electroplating unit

An example of a more complex and commercially available electroplating unit is shown in Figs. 3.10 and 3.11. It holds a larger volume of electrolyte than that of a simple lab setup and includes monitors for liquid level, pH, and additives, as well as a continuous filtration and a dummy plating cell for cleaning of the electrolyte. Filtration rids the electrolyte of particles, which can interfere with the deposit. Dummy plating is used to deposit trace cation impurities on a dummy substrate before plating on the target substrate. For large-scale manufacturing, continuous filtering, salt replenishment, and pH maintenance are important issues. Also, some

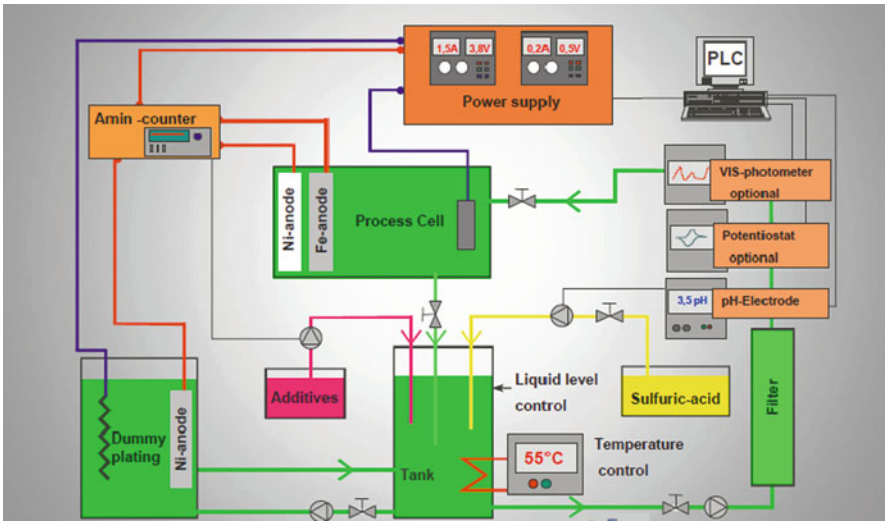
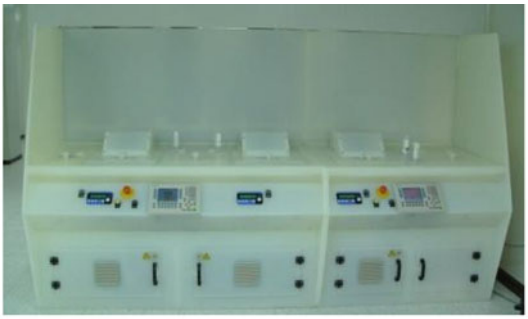
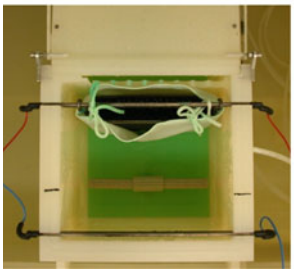


Fig. 3.10 Schematic of a commercially available Ni–Fe electroplating system (Reprinted with permission. Copyright 2009 M-O-T, Germany)



(a)



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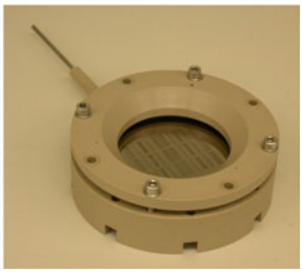

(c)

Fig. 3.11 Commercially available electroplating unit for use in a cleanroom: (**a**) plating facility for cleanroom; (**b**) process cell with anode; (**c**) holder for cathode (Si wafer) (Reprinted with permission. Copyright 2009 M-O-T, Germany)

baths may generate gaseous byproducts, so exhaust of these gases should also be considered.

3.3.1.7 Process Flow

A general overview of the electroplating process flow is shown in Fig. 3.12. The cleaning procedure has to be adapted to the substrate. Often a rinse with deionized water and a subsequent drying with nitrogen gas are sufficient for obtaining a particle-free surface. Weighing of the substrate before and after electroplating is necessary to calculate the current efficiency, which is an important value to estimate the process reproducibility. To ensure good performance and repeatability, process temperature, electrolyte circulation, and bath chemistry should be controlled accurately. Control of the pH is also crucial.

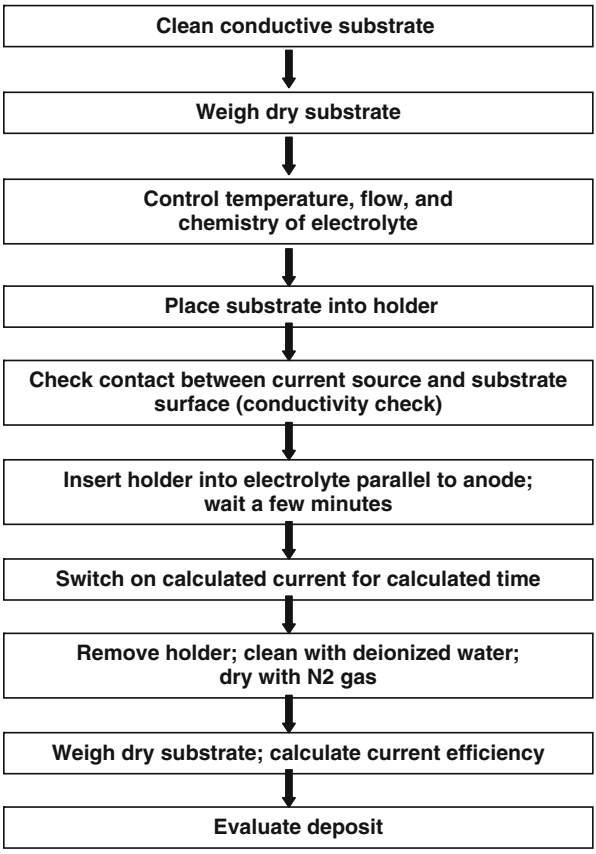

Fig. 3.12 Process flow for electroplating

3.3.1.8 Nickel

Nickel electroforming is a well-established process for fabrication of microdevices and mold inserts [13, 14, 21–24]. The standard plating baths are based on nickel sulfamate. Boric acid is used as a pH buffer, and wetting agents (surfactants) are used to enable electrolyte penetration into micropatterned structures. An unwanted side reaction is the reduction of hydrogen ions to hydrogen gas according to the following equation.

$$\text{Hydrogen formation}: \quad 2\,H^+ + 2e^- \rightarrow H_{2\,(g)}$$

As a result the current efficiency is not 100%, because some of the electrons are used to reduce the hydrogen ions instead of the metal ions. Also the concentration of hydrogen ions decreases, which changes the pH. The release of hydrogen gas can also form bubbles that cause pores in the deposit. Therefore a pH-buffering agent (e.g., boric acid) and a surfactant to enable gaseous hydrogen to escape during electroforming are crucial for the nickel electrolyte.

The electrolyte formulation and operation parameters can be modified for specific fabrication environments or according to the desired properties of the deposit. Some electrolytes contain additional additives such as stress reducers (e.g., saccharin). To enhance the electrical conductivity of the electrolyte and the solubility of the anode, chloride or bromide is used. Also the current density and current waveform are modified to vary the Young's modulus or hardness of the deposit [25].

Normally sulfur-depolarized nickel pellets are used as the anode material, but a high-purity nickel plate may also be used. A large surface area compared to the cathode and the generally good solubility of nickel result in a low anodic overpotential for most nickel electrolytes. Two typical nickel sulfamate electrolytes suitable for microfabrication are listed in Table 3.4.

Table 3.4 Example nickel sulfamate electrolytes used for microfabrication

Bath constituents and parameters	1	2
Nickel sulfamate ($Ni(NH_2SO_3)_2 \cdot 4H_2O$) (g/L)	105–110	80
Nickel(II)-bromide ($NiBr_2 \cdot 3H_2O$) (g/L)	0–5	
Boric acid (H_3BO_3) (mL/L)	40	30
Perfluorinated alkylsulfate (2 % solution) (wetting agent) (mL/L)	10	
Additive K (wetting agent) (mL/L)		5
Saccharin ($C_7H_4NNaO_3S \cdot 2H_2O$) (mg/L)	0–20	
pH	3.8	3.2
Temperature (°C)	50	40
Cathodic current density (A/dm^2)	1.0	0.1–2
Anode material	S-Ni pellets in a Ti basket	
Deposition rate	10 μm/h	
References	[13]	[14]

3.3.1.9 Copper

Copper electroplating is used for manufacturing of microdevices and for auxiliary or sacrificial layers [13, 26]. The most common bath is an acidic sulfate-based electrolyte, which can be used at room temperature and is easy to maintain. For a good quality of deposit, organic chemicals are used as leveling agents, but this makes the maintenance of the electrolyte more complicated. Alternatively, copper fluoroborate is used as the Cu salt [27]. For details see Table 3.5. For formation of integrated circuit interconnects, a different copper plating process is used. Three or four component additive mixtures in the electrolyte combined with pulse plating facilitate the superfilling of via holes and trench lines during the plating process. For further details refer to [28].

Table 3.5 Example copper electrolytes used for microfabrication

Bath constituents and parameters	Copper sulfate-based	Copper fluoroborate-based
Copper (II)-sulfate ($CuSO_4 \cdot 5H_2O$) (g/L)	15–25	
Copper (II)-fluoroborate ($Cu(BF_4)_2$) (g/L)		60
Sulfuric acid (H_2SO_4, 98%) (mL/L)	200–250	
Fluoroboric acid (HBF_4) (mL/L)		13
Boric acid (H_3BO_3) (mL/L)		12
Sodium chloride (NaCl) (g/L)	0.06–0.1	
Wetting agent (mL/L)		3
Cuprostar LP1 (leveler) (mL/L)	5	
pH		0.7–1.0
Temperature (°C)	20–25	20–25
Cathodic current density (A/dm^2)	1–4	6–12
Anode material	Phosphorus depolarized copper	Copper (99.9% Cu)
Deposition rate (μm/h)	12.5–50	
References	[13]	[27]

3.3.1.10 Gold

Gold has some outstanding properties, including very high conductivity, high ductility, excellent corrosion resistance, and good biocompatibility. Gold microstructures are used as metallic parts in microoptics, microfluidics, and micromechanics; for mask absorber structures in LIGA-technology; and for the fabrication of electrical contacts in the electronic industry.

Two kinds of gold are used in plating: soft gold (pure gold) and hard gold (gold alloy). Soft gold is used for metalizing bonding pads and for fabricating microbumps on silicon IC chips and ceramic packaging boards. Hard gold is used as a contact material on electrical connectors, printed circuit boards, and mechanical relays. For

hard gold, alloying metals such as Co, Ni, or W are used. Further aspects of gold plating processes in the electronic industry are reviewed by [29].

For electrolytic gold plating, three different types of baths are commonly used: sulfite-based electrolytes with a neutral or alkaline pH; thiosulfate-sulfite-based electrolytes with a weak acidity; or cyanide-based electrolytes with a range of pH from weakly acidic to strongly basic. Noncyanide baths are preferred because they are non-toxic and more compatible with conventional positive photoresists. Table 3.6 shows an overview of gold electrolytes suitable for microfabrication. In Table 3.7 some sulfite-based electrolytes are described. In all cases, a platinated titanium mesh is used as an insoluble anode. Specific skills are needed for mixing the chemicals to obtain a stable electrolyte. The authors recommend purchasing a complete electrolyte solution from a commercial vendor.

Table 3.6 Comparison of gold electrolytes suitable for microfabrication

Bath type	Gold complex	Current densities (A/dm^2)	Advantages/disadvantages	References
Sulfite-based	$[Au(SO_3)_2]^{3-}$	0.1–0.4	High current efficiency Very sensitive to process parameters	[30– 32]
Thiosulfate-sulfite-based	$[Au(S_2O_3)_3]^{3-}$ $[Au(SO_3)_2]^{3-}$	0.5	Good bath stability High internal stress of deposit	[29, 33, 34]
Cyanide-based	$[Au(CN)_2]^-$	0.2–0.5	Good bath stability High toxicity Instability of some resists (tend to delaminate from the substrate) Low current efficiency	[35]

Table 3.7 Overview of sulfite-based electrolytes: composition, process parameters, and applications

Application	X-ray masks	Microdevices	Microbumps
Metal salt (mol/L)	0.126	0.061–0.126	0.05
Complexing agent for metal cation	Sulfite	Sulfite	Sulfite Sulfate Chloride
Other additives	EDTA; 1,2-Ethylendiamin	EDTA 1,2-Ethylendiamin Brightener (also As(III))	EDTA As(III)
pH	7	7–9.5	9.0±0.2
Temperature (°C)	55 ± 2	28–70	
Current density (A/dm^2)	0.1–0.2	0.1–0.6	0.25–0.3
References	[32]	[32]	[15]

3.3.1.11 Nickel Alloys

The rapid development of the field of microsystems has generated new applications, which in turn require materials to meet new performance demands. In this regard, electroplated alloy materials can cover a wide spectrum of different properties depending on their composition. Plating of alloys is generally more complicated than plating of single-element metals because multiple metal reductions must occur in parallel. These reduction reactions often interact with each other, creating complex electrochemical processes.

Plating of Ni alloys in general is described in [9, 12, 36]. In [37] the effect of pulse plating on the deposit quality of alloys is described in detail. In microfabrication, nickel–iron (Ni–Fe) alloys are well known for their versatility, making them suitable for micromechanical and magnetic applications [38–44]. Also some investigations on the electroplating of Ni–Co–Fe for magnetic MEMS application are described in the literature [45–47].

Ni alloys feature a number of superior material properties compared to pure nickel. Such alloys usually exhibit increased hardness and lower brittleness and can, most notably, withstand static and dynamic strains. The latter enables an improved fatigue resistance which is an important characteristic concerning the production of movable parts such as micro gear wheels or switching devices. Moreover, magnetic properties of Ni–Fe alloys are characterized by a lower coercivity and much higher permeability compared to nickel.

Independent of specific application requirements, uniform alloy composition is a common requirement for reproducible material properties. Hardness and thus wear/corrosion resistance, residual stresses, ductility, porosity, and surface roughness, as well as magnetic properties are important factors that determine the device durability. Those properties are dictated by a number of variables during the electrochemical process, such as Ni:Fe ion ratio of electrolyte, additives, bulk pH-value, temperature, agitation, and current waveform.

In the past, reports on various approaches have delved into the control of certain layer properties of microdevices including material composition and metallurgical structure by varying electrolyte formulation and process parameters [44, 48–53]. In recent years, the influence of pulse plating on material properties and composition of Ni–Fe alloys for MEMS have been investigated [e.g., 47, 54–57].

In an acid Ni–Fe electrolyte the metal ions are usually provided by chloride or sulphate metal salts whereby a soluble nickel anode can act as an additional nickel ion source. The organic boric acid is an important additive as it prevents the hydrogen evolution at the cathode by buffering the pH and thus increases cathodic current efficiency and enables a wider current density range. In addition to acting as a buffer agent, the boric acid may also alter the composition of the Ni–Fe alloy. Another additive is citrate, which is a complexing agent for the Fe^{2+} ions and thus hinders the formation of unwanted Fe^{3+} ions. Citrate also shifts the Fe overpotential to more negative values due to the higher stability of complexed ions. Furthermore, a wetting agent such as sodium dodecylsulfate (SDS) can be added to ensure complete

wetting of the cathode. Saccharin is effective as a stress reliever. The decrease in the residual stress can be obtained by increasing the saccharin content of an electrolyte.

In Table 3.8 some recipes for sulfate-based electrolytes are summarized. The electroplated deposits have an iron content of 10–35%. In the maintenance of Ni–Fe electrolytes, control of the concentration of the electrolyte composition is crucial. To prevent Fe^{3+} formation, the electrolyte should be percolated by an inert gas (nitrogen or argon). Another option to keep oxygen out is to maintain a protective layer of argon gas over the electrolyte.

Table 3.8 Some sulfate and sulfate-chloride based Ni–Fe electrolytes for microfabrication

	Sulfate-based		Sulfate-chloride based
Bath constituents and parameters	1	2	3
Nickel sulfate ($NiSO_4 \cdot 7H_2O$) (g/L)	50	45	
Nickel chloride ($NiCl_2 \cdot 6H_2O$) (g/L)			44
Iron sulfate ($FeSO_4 \cdot 7H_2O$) (g/L)	3	3.5	
Iron chloride ($FeCl_2 \cdot 6H_2O$) (g/L)			1.1
Boric acid (H_3BO_3) (g/L)	25	25	35
Saccharin($C_7H_4NNaO_3S.2H_2O$) (g/L)	1	1	1.5
Sodium citrate ($Na_3(C_6H_5O_7) \cdot 2H_2O$) (g/L)	28		
Sodium-dodecyl-sulfate ($NaC_{12}H_{25}SO_4$) (g/L)	0.5	0.5	0.4
pH	3.5	2.8	2.5
Temperature (°C)	50	50	35
Current density (A/dm^2)	2–4	0.5	0.6
Thickness of electroplated micro structures reported (μm)	500	80	2
References	[57]	[50]	[48, 49]

3.3.2 Electroless Plating

Electroless plating requires no external source of electrical current. The term "electroless plating" is generally used to describe three fundamentally different plating processes: galvanic displacement, substrate-catalyzed processes, and autocatalytic processes. Galvanic displacement induces electron exchange on the surface of the substrate in the electrolyte, resulting in the reduction of metal ions. The substrate-catalyzed process modifies the surface to make it more reactive for oxidation and reduction. In these first two processes, the plating reaction should cease when the substrate is covered completely with metal, whereas in the autocatalytic process a metal salt and a reducing agent in an aqueous solution react continuously in the presence of a catalyst, making this technique more suitable for thick layers of metal. Chemical reducing agents often employed are hydrazine, sodium hypophosphite, sodium borohydride, amine boranes, titanium chloride, and formaldehyde.

A general reaction in electroless plating is described as:

$$M^{z+}\ \text{(Metal ion)} + z\,e^{-}\text{(suppliex by reducing agent)} \xrightarrow{\text{catalytic surface}} M\ \text{(deposit)}$$

This reaction can occur only on a catalytic surface; once deposition is initiated, the deposited metal must be self-catalytic to enable continued deposition.

Not all metals show self-catalytic functionality, and thus the kinds of metal for electroless plating are limited. Since Brenner and Riddell [58] first reported nickel electroless plating in an autocatalytic sense, electroless plating has continuously advanced, and now many useful metals are plated electrolessly. Those materials include nickel, cobalt, palladium, platinum, copper, gold, silver, and certain alloys. Various bath chemistries are available for each metal, each with different metal salts, reducing agents, and complexing agents. Some of the electroless plating baths and conditions for nickel, copper, and gold are introduced in the following sections.

Electroless plating is useful for metal deposition on nonconducting surfaces such as polymers or inorganic layers. However, because the physical and chemical properties of metals and polymeric or inorganic materials are quite different, the adhesion between two materials is often very poor and the plated metals tend to peel off. To improve adhesion and to increase the number of catalytic sites on the surface, a sample needs to go through surface treatment by physical/chemical etching processes and surface catalysis prior to immersing in the electroless plating bath.

A brief procedure flow is shown in Fig. 3.13. The surface modification includes nanoscopic surface roughing using chemical wet/dry etching (e.g., reactive ion etching) to increase the interfacial surface area for better adhesion. Then the sample is catalyzed. One popular catalyzing procedure uses a surface treatment with mechanically compliant tin, followed by the major catalytic compound palladium. In order to provide uniform catalytic sites on the surface and provide a kinetic energy during the metal reduction on the surface, both the catalysis and electroless plating steps are performed in ultrasonic environment [59, 60].

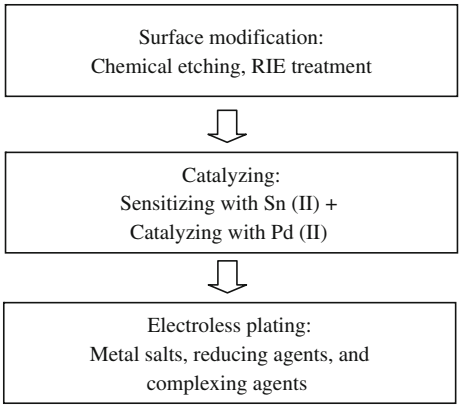

Fig. 3.13 An example of a procedure for electroless plating

3.3.2.1 Nickel

Electroless nickel plating is one of the most popular catalytic electroless processes in use today. It is commonly used in engineering coating applications for wear resistance, hardness, and corrosion protection. It is also used in the electronics industry on PCBs as a coating with an overlay of gold to prevent corrosion. The concept and basic composition has not changed much since the inception of the process [58]. The electroless nickel plating bath consists of a source of nickel ions (salts), a reducing agent, complexing agents, and some additives.

Although many nickel salts such as nickel sulfate, nickel chloride, and nickel acetate are available, nickel sulfate is preferred because of its low corrosiveness and low cost. To enhance chemical reduction of nickel at the cathode, a reducing agent is used such as sodium hypophosphite (NaH_2PO_2 H_2O), sodium borohydride ($NaBH_4$), and dimethylamine borane (DMAB). Complexing agents are used for exerting a buffering action to prevent the pH change, preventing the precipitation of nickel salts, and enhancing stable metal reduction. Note that because there are several agents inserted in the bath, nickel from electroless plating is not usually pure but contains other components such as phosphorus or boron.

Table 3.9 shows some bath compositions for electroless nickel deposition with hypophosphite reducing agent (columns 1–4), borohydride reducing agent (columns 5–6), and dimethylamine borane reducing agent (columns 7–8) [61].

A step-by-step procedure for nickel electroless plating with a hypophosphite reducing agent is given below and in Table 3.10 [9, 62], which essentially follows the recipe of Table 3.9 (column 1) except for the amount of hydroxyacetic acid of 30.9 g/L and the process temperature of 65°C. With this recipe, a deposition rate of approximately 70 nm/min (4.2 μm/h) is obtained on a printed circuit board and a Si substrate. The equipment necessary for electroless nickel plating is shown in Fig. 3.14, consisting of an Sn sensitizing bath, a Pd activation bath, an electroless nickel bath, and an ultrasonic bath.

Bath Preparation

1. Mix 10 g of $SnCl_2$ and 10 g of HCl. Take 0.375 mL of the solution and mix it with 120 mL of deionized water to prepare the Sn(II) solution.
2. Mix 10 g of Pd and 10 g of HCl. Take 0.5 mL of the solution and mix it with 100 mL of deionized water to prepare the Pd(II) solution.
3. Measure 129.62 g $NiCl_2$, 105.97 g $NaH_2PO_2{\cdot}H_2O$, and 61.8 g $HOCH_2COOH$ into a 1 L beaker. Fill the beaker with deionized water to 1 L. Mix using a motorized mechanical propeller for at least 2 h. (Note that a magnetic stirring bar is not recommended because the bath contains ferromagnetic Ni.) This stock solution can be stored for a month or two without noticeable degradation.
4. Add NH_4OH to obtain a pH level of 4–6. Mix well for 2 h in a similar way to that described above. This pH adjustment should be performed immediately before performing electroless plating.

Table 3.9 Example baths for electroless nickel deposition using various hypophosphite reducing agents

	Hypophosphite reducing agent				Borohydride reducing agent		Dimethylamine borane reducing agent	
Bath constituents and parameters	1	2	3	4	5	6	7	8
Nickel chloride ($NiCl_2 \cdot 6H_2O$) (g/L)	30	30	30		20	24	170	
Nickel sulfate ($NiSO_4 \cdot 6H_2O$) (g/L)				25				30
Sodium hypophosphite ($NaH_2PO_2 \cdot H_2O$) (g/L)	10	10	10	25				
Hydroxyacetic acid ($HOCH_2COOH$) (g/L)	35							
Sodium citrate ($Na_3C_6H_5O_7 \cdot 2H_2O$) (g/L)		12.6	84					
Sodium acetate ($NaC_2H_3O_2$) (g/L)		5						
Sodium borohydride ($NaBH_4$) (g/L)					0.67	0.4		
Ethylenediamine ($C_2H_4(NH_2)_2$) (g/L)					44			
Sodium hydroxide (NaOH) (g/L)					40			
Ammonium hydroxide (NH_4OH, 28% NH_3) (mL/L)						120		
Dimethylamine borane ($(CH_3)_2NHBH_3$) (g/L)							37	3.5
Malonic acid ($C_3H_2O_4Na_2$, disodium salt) (g/L)								34
Ammonium chloride (NH_4Cl) (g/L)			50					
Boric acid (H_3BO) (g/L)							25	
Sodium pyrophosphate ($Na_4P_2O_7 \cdot 10H_2O$) (g/L)				50				
Base for neutralizing	NaOH	NaOH	NH_4OH	NH_4OH	NaOH	NH_4OH	NaOH	NH_4OH
pH	4–6	4–6	8–10	10–11	11	11	4.25	5.5
Temperature (°C)	90–100	90–100	95	70	97	60	18	77
Deposition rate (μm/h)	15	7	6.5	15	8.8	1.3	2.3	21
References	[62]	[63]	[58]	[64]	[65]	[65]	[66]	[67]

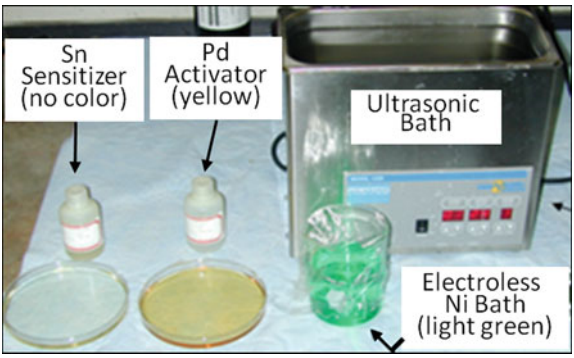

Fig. 3.14 Preparation of electroless nickel plating

Electroless Nickel Plating Procedure

1. Rinse a substrate in acetone, then methanol, then deionized water, and then sensitize it in the Sn(II) solution for 2 min.
2. Rinse the sample in deionized water for 30 s.
3. Catalyze the sample in the prepared Pd(II) solution for 2 min.
4. Rinse the sample in deionized water for 30 s.
5. Submerge the sample in the prepared electroplating bath at 65°C in an ultrasonic environment.

Table 3.10 Ingredients of electroless nickel bath with hypophosphite reducing agent [9]

Bath constituents and parameters	Molarity (mol)	Molecular weight	Mass (g/L)
Nickel chloride ($NiCl_2 \cdot 6H_2O$)	0.23	129.62	30
Sodium hypophosphate ($NaH_2PO_2 \cdot H_2O$)	0.09	105.97	10
Hydroxyacetic acid ($HOCH_2COOH$)	0.5	61.8	30.90
pH	4–6 (using NH_4OH or NaOH for adjustment)		
Temperature	65°C		

3.3.2.2 Copper

Some electroless copper plating recipes use formaldehyde or its derivatives as a reducing agent. However, such plating baths produce toxic formaldehyde vapor during the process and require high pH (~12.5). An alternative bath uses hypophosphite as the reducing agent. Table 3.11 shows some bath compositions for electroless copper deposition with formaldehyde reducing agent (columns 1–3) and hypophosphite reducing agent (column 4) [61, 68].

Table 3.11 Example baths for electroless copper deposition using formaldehyde reducing agent and hypophosphite reducing agent

	Formaldehyde reducing agent			Hypophosphite reducing agent
Bath constituents and parameters	1	2	3	4
Copper sulfate ($CuSO_4 \cdot 5H_2O$) (g/L)	3.6	30	10	3.83
Nickel sulfate ($NiSO_4 \cdot 6H_2O$) (g/L)				0.53
Boric acid (H_3BO_3) (g/L)				30.9
Sodium hypophosphite ($NaH_2PO_2 \cdot H_2O$) (g/L)				28.6
Sodium potassium tartrate ($KNaC_4H_4O_6 \cdot 4H_2O$) (g/L)	25	99		
Sodium hydroxide (NaOH) (g/L)	3.8	50	10	
Sodium carbonate (Na_2CO_3) (g/L)		32		
Formaldehyde (HCOOH (37%)) (g/L)	10	29	20.3	
Sodium citrate ($Na_3C_6H_5O_7 \cdot 2H_2O$) (g/L)				15.3
Methyldichlorosilane (CH_3Cl_2SiH) (g/L)			0.25	
Ethylenediaminetetraacetic acid (EDTA) tetrasodium (N,N′-1,2-Ethanediylbis[*N*-(carboxymethyl)glycene] tetrasodium) (g/L)			20	
Temperature (°C)	22	25	63	65
Deposition rate (μm/h)	0.5	2.5	6.3	8.5
References	[69]	[70]	[71]	[68]

The hypophosphite reduced electroless copper plating has advantages including bath stability, no toxic gas generation, and operation in a lower pH environment. However, because the deposited copper cannot catalyze the oxidation of hypophosphite, the bath needs a small amount of nickel for continuous plating and boric acid for a high plating rate, resulting in impure copper deposition.

A step-by-step procedure for copper electroless plating with a hypophosphite reducing agent [68] is given below as an example.

Bath Preparation

1. Mix 10 g of $SnCl_2$ and 10 g of HCl. Take 0.375 mL of the solution and mix it with 120 mL of deionized water to prepare the Sn(II) solution.
2. Mix 10 g of Pd and 10 g of HCl. Take 0.5 mL of the solution and mix it with 100 mL of deionized water to prepare the Pd(II) solution.
3. Mix the electroless copper plating bath with hypophosphite reducing agent following Table 3.11 (column 4).
4. Adjust the pH with either KOH or NaOH pellets to the desired pH level (Here it is 9–9.5).

Note that all ingredients are mixed and dissolved in water together. The mixture after step 3 can have a shelf life of about a month, but the mixture after step 4 tends

to plate a thin copper layer on the container wall in a few days. The pH adjustment should be done right before electroless plating is performed. The solution should have a clean blue color.

Electroless Copper Plating Procedure

1. Rinse substrate in acetone, then methanol, and then deionized water, and then sensitize it in the prepared Sn(II) solution for 2 min.
2. Rinse the substrate in deionized water for 30 s.
3. Catalyze the substrate in the prepared Pd(II) solution for 2 min.
4. Rinse the substrate in deionized water for 30 s.
5. Submerge the substrate in the prepared electroless plating bath.

3.3.2.3 Gold

Because of its high chemical stability and mechanical ductility, gold becomes an indispensable material in the electronics industry. Despite its importance, electroless gold plating [29] has been underdeveloped compared with electroless nickel or copper. Useful electroless gold plating using borohydride or amine borane as the reducing agent has been reported [72, 73]. A typical bath composition is shown in Table 3.12.

Table 3.12 Ingredients of electroless gold bath with borohydride reducing agent [73]

Bath constituents and parameters	Molarity (mol)	Molecular weight	Mass (g/L)
Potassium gold cyanide ($KAu(CN)_2$)	0.02	290	5.8
Potassium cyanide (KCN)	0.2	65	13
Potassium hydroxide (KOH)	0.2	56	11.2
Potassium borohydride (KBH_4)	0.4	54	21.6
Temperature	75°C		
Deposition rate	0.7–3.5 μm/h (with stirring)		

Bath Preparation (2.5× Concentration) [67]

1. Dissolve 28 g KOH and 32.5 g KCN in about 500 mL of deionized water.
2. Add 54 g KBH_4 and stir until dissolution.
3. Dissolve 14.4 g $KAu(CN)_2$ in about 250 mL deionized water.
4. Mix the above two solutions, and dilute to 1 L.
5. Filter through Whatman 41 filter paper or equivalent.
6. Dilute 1 volume of this solution with 1.5 volumes of deionized water to make a 2.5× bath.

3.3.3 Comparison of Electroplating and Electroless Plating

Ni, Cu, and Au microstructures can all be fabricated by electroplating or electroless plating. Compared to electroplating, electroless plating contains the following characteristics and advantages [61].

1. No power supply and electrical contact is necessary.
2. Deposition may occur on a nonconducting surface.
3. More uniform deposition can be formed on three-dimensional geometry without electric field influence.
4. Deposits are often less porous.

There are disadvantages of electroless plating too. Often the electroless baths require higher temperatures and have a relatively short lifetime. Electroless plating is also prone to poor adhesion. Care should be taken when storing electroless plating baths. A container made of plastic or glass is often found to be covered with electroless plated metal after being stored on the shelf for a while. Also, for electroless plating, the deposition rate is relatively slow, and metal layers thicker than a few micrometers are not recommended. In addition, electroless plating metal in selected regions can sometimes be quite challenging. For example, selective deposition on a metal surface is fairly easy, but selective coating a polymer on SiO_2 is not very effective (the bath will likely deposit on both the polymer and SiO_2 surfaces).

Costs of electroplating and electroless plating are fairly similar. The electroless plating process requires a chemical reducing agent for metal ions to be converted into the elemental conformation, therefore it is considered as a more expensive process from the material cost point of view. However, this chemical cost is offset by the advantage of not requiring equipment such as power supplies or switching circuits for advanced current control.

There are clearly pros and cons associated with both electroplating and electroless plating. In situations where either electroplating or electroless plating could theoretically be used, the decision for one or the other is often dependent on many process integration issues. In general, electroless plating can be considered as a complement to electroplating rather than a "competitor."

3.4 LIGA and UV-LIGA Processes

One of the most distinctive MEMS processes is the construction of thick and high-aspect-ratio three-dimensional (3-D) microstructures. High aspect ratio is modestly defined as a height to width ratio of 2 to 1 or greater. Fabrication of these structures often relies on X-ray or UV lithography of thick polymer layers.[4] The patterned

[4] See Chapter 9 for more information on lithography.

polymeric structures can be used directly as a MEMS device or used as a mold for metal electrodeposition. In this section, two fabrication approaches for achieving high-aspect-ratio 3-D electroformed metallic structures are described: one with X-ray lithography (LIGA), and the other with UV lithography (UV-LIGA or LIGA-Like).[5]

3.4.1 Process Explanation

Both LIGA and UV-LIGA processes share common fabrication steps except for the initial step of polymeric mold fabrication. A general fabrication procedure for both processes is described in this section.

Because these are surface micromachining processes, there is no strict criterion for substrate selection. A variety of substrates such as Si, glass, ceramic, and printed wiring board are available, however, an oxidized Si substrate is used as an example here (Fig. 3.15). An electrical seed layer typically consisting of Ti/Cu or Cr/Cu is deposited on the substrate using either sputtering or evaporation. Cu does

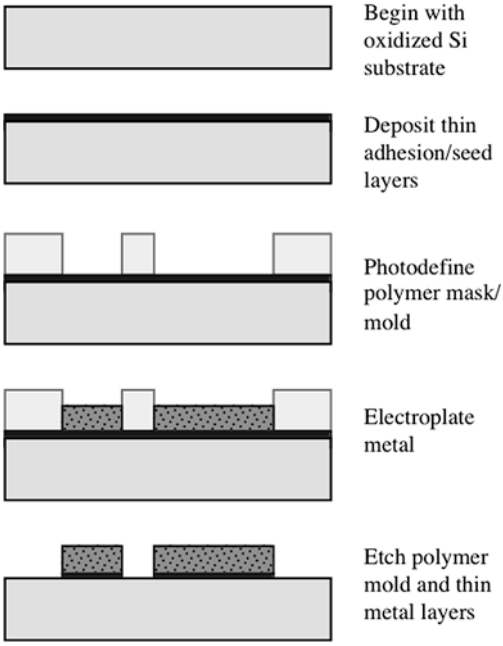

Fig. 3.15 Basic electroplating process to form single-layer metal structures

[5]The German acronym "LIGA" refers to a three-step process: X-ray-*Li*thography, Electroplating (german: *Galvanik*), Polymer Replication (German: *Abformung*). Nowadays, "LIGA" is commonly used in reference to the two-step process of lithography and electroplating (excluding the polymer replication step).

not stick well to most substrates so Ti or Cr is employed as an adhesion layer (see Section 3.5.1). Typical thicknesses of Ti (or Cr) and Cu are 10–30 nm and 100–300 nm, respectively. After the seed layer deposition, a thick polymer layer is coated, soft-baked, and lithographically patterned to form a micromold for a subsequent electroplating. LIGA typically uses polymethylmethacrylate (PMMA) or SU-8 (an epoxy-based polymer) for X-ray lithography, whereas UV-LIGA uses various UV-sensitive photoresists including DNQ-novolak-based photoresist, SU-8, polyimide, and others.

With the photoresist mold in place, the substrate is then electroplated. The electroplated metal fills the mold confined by the sidewalls. Usually the electroplating is stopped before it reaches the top of the mold. But sometimes it is electroplated over the mold to form "mushroom"-type structures for some applications. After electroplating, the polymer mold is removed using a solvent and/or plasma etching. The electroplated structures are still electrically connected to each other through the seed layer. The Cu and Ti seed layers are then sequentially time etched to isolate the electroplated structures electrically and complete the process.

With the introduction in the 1990s of UV photopatternable high-aspect-ratio polymers such as SU-8, high-quality sidewall and high-aspect-ratio molds could be fabricated using UV lithography, as compared to X-ray lithography. The electroforming process using UV-patterned molds and subsequent electroplating has been called UV-LIGA, LIGA-like, or often "poor man's LIGA."

The UV-LIGA process does not provide the extreme aspect ratios possible with X-ray LIGA, but is sufficiently suitable for many applications. A good guideline is that an aspect ratio of 6:1 can be fabricated by UV-LIGA. It is also restricted to a maximum resist height of 800 μm or so. Also submicron pattern dimensions may not be effectively produced because of the wavelength of the UV source, for example, i-line ($\lambda = 365$ nm). However, in addition to low cost in equipment, the process has other advantages such as batch processability, manufacturability, and relative simplicity, providing an affordable system set for laboratory and industrial usage.

3.4.2 Electroplating in LIGA and UV-LIGA Microstructures

The height and surface profile of high-aspect-ratio electrodeposited metal structures and the homogeneity of their thickness distribution are influenced by various factors, which can interfere with each other. The main factors and important effects are explained in this section.

The deposition rate is proportional to the current density. Therefore a higher current density results in a thicker deposit. The distribution of the current density is associated with the distribution of the electric field lines (primary current distribution). Because the metal surface is highly conductive, the field lines are normal to the electrode surface. If the anode has a larger area than the cathode, the field line density and current density are higher at the edge of the substrate, which causes a

thicker deposit at the edge of the substrate ("macro bathtub effect"). If the cathode surface is patterned with resist structures, the electric field lines bend, and a current concentration occurs at the edge of the structures [74, 75]. Therefore the electroplated layer is usually thicker near the edges of the electroplated features ("micro bathtub effect") and sometimes higher in narrow structures than in wide structures, as shown in Fig. 3.16.

Another consideration for electroplating in high-aspect-ratio features is that the transport mechanism of the metal ions depends on feature size and depth. As a result, the electroplating rate may vary during the plating process [76]. Figure 3.17 shows three different states that occur in filling a mold structure by electroplating. At the beginning of the deposition, the process is highly diffusion limited. As the plated layer grows and the trenches begin to fill, the diffusion limitations begin to wane. At an intermediate filling, the penetration range of the convection is reached. This depends on the lateral size of the structure itself. In the case of structures with sufficiently wide lateral dimensions, the flow velocity in the plating bath reduces the extension of the diffusion layer, as described in Section 3.3.1.2. Very high-aspect-ratio structures therefore show a reduced plating rate in the beginning of plating. In this case, the electroplated layer would be thinner in narrow structures, as compared to wider structures.

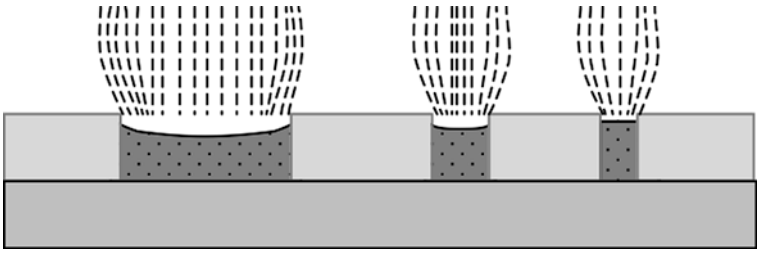

Fig. 3.16 Schematic of electrical field line distribution using resist-patterned substrates. The field line density is higher within narrow structures and at the edge of wide structures, which affects the height and surface profile of the electroplated microstructures

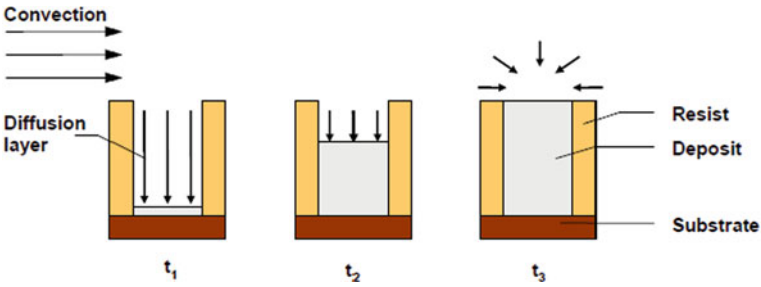

Fig. 3.17 Schematic of the diminishing influence of diffusion during metal growth. The diffusion layer thickness depends on process progress and on the penetration range of convection. At t_3, the deposition rate is improved due to spherical diffusion

All these effects cause inhomogeneous deposition rates over the substrate as well as within the features. To minimize these unwanted effects and improve the plating uniformity, some rules are given in the following.

1) Use a shield or a wafer holder to homogenize the electrical field at the macroscopic scale.
2) Use dummy plating areas over the whole substrate to promote a homogenous current distribution.
3) Use microstructured dummy areas that surround the functional features.
4) Use moderate flow to get similar heights of diffusion layers.
5) Use moderate current density to avoid insufficient supply of ions at the bottom of the microstructure.
6) Limit the deposition height to be about 2/3 of the mold height (see Fig. 3.17 for t_2).

More rules for LIGA design can be found in [77].

To show the potential of the LIGA techniques, one example is given. Figure 3.18 shows (a) a SU-8 resist mold and (b) the replicated Ni–Fe structure. The electroplating produces the exact negative of the structural details and the sidewall roughness of the resist mold. In Fig. 3.19 a commercially available micro gear system is shown. Crucial features for this application are the high aspect ratio in combination with the parallel sidewalls of the resist structure, which is typical for LIGA. Other applications of LIGA are described in [78, 79].

3.4.3 Multilevel Metal Structures

Often multiple metal levels and vias are necessary to enable complex wiring interconnections or complex mechanical microstructures. Multilevel fabrication can be achieved by extending the previously described process (see Section 3.4.1) using multiple masking and electroplating steps. For wire connections, an interlayer dielectric material must be selected to electrically insulate the metal layers from each other to avoid unexpected short circuits. Considering that the top surface of the first metal layer may be fairly rough (typical of many electroplated metals), the dielectric must be able to conformally and completely coat the top and side surfaces of the lower metal layer. Even the smallest pinhole defect in the interlayer dielectric can cause the electrical insulation to fail. Commonly used interlayer dielectric materials include PECVD or sputtered oxide/nitride, spin-on glass, or a chemically stable spin-coated polymer such as polyimide or SU-8. The intended temperature of operation must also be considered, because polymer dielectrics may not be suitable at a 100°C or more.

A fabrication process for achieving a two-layer metal structure is shown in Fig. 3.20. The process begins by depositing the first metal layer as described in Fig. 3.15. The interlayer dielectric is deposited and vias are opened to provide

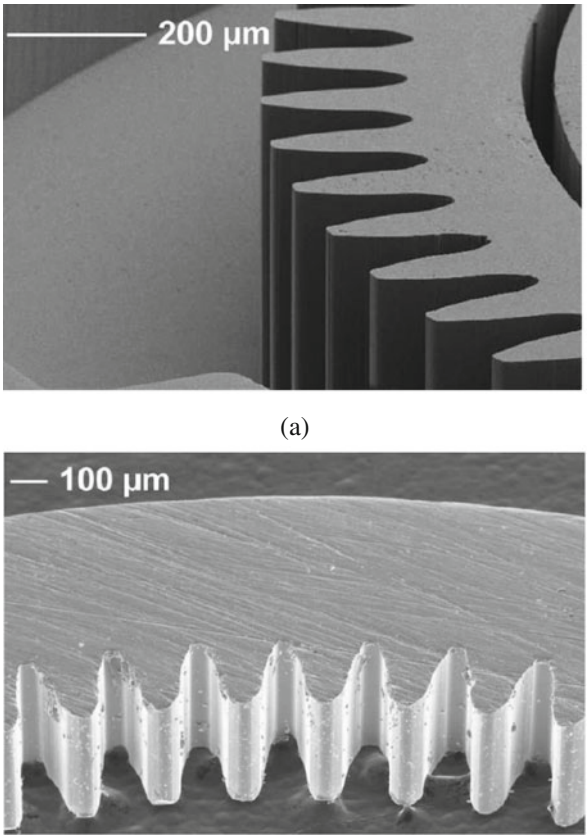

Fig. 3.18 SEM micrograph of high-aspect-ratio microstructures: (**a**) SU-8 resist mold; (**b**) electroplated Ni–Fe [57] (Reprinted with permission. Copyright 2008 Springer Europe)

interconnects between the two metal layers. For many films, this step requires the patterning of a photoresist mask and a subsequent etch. In contrast, the use of a photosensitive polymer dielectric offers the opportunity for simple one-step photodefinition.

After the interlayer dielectric is formed, a new adhesion/seed layer is required, because a conductive electrical surface is needed for electroplating. In order to provide sufficient step-coverage over the topography created by the first metal layer, sputtering is the preferred method. It should be noted that adhesion of the metal to a polymer interlayer dielectric can be quite low. If necessary, adhesion promoters may be used to improve adhesion of the metal (see Section 3.5.1).

After the seed layer deposition, a polymer mold is photodefined to create the pattern for the second metal layer, and the metal is subsequently electrodeposited to the desired thickness. Afterwards, the polymer mold and thin metal layers are etched away. If necessary a passivation layer can be deposited on top of the second metal layer for protection from the environment. Also with the right selection of materials,

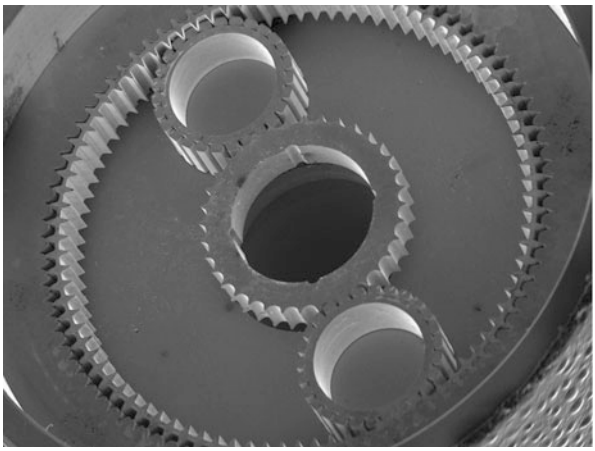

Fig. 3.19 Ni–Fe microplanetary gear system; structure height = axial length : 1 mm, diameter 8 mm (Reprinted with Permission. Copyright 2009 Micromotion GmbH, Germany)

the interlayer dielectric can be selectively etched away to create "free-standing" bridge segments that are isolated by air [80–82].

In addition to the planar metal layers, some MEMS devices creatively employ high-aspect-ratio vertical via structures for mechanical or electrical functionality. For example, metal vias are used for vertical interconnects in MEMS packaging applications [83] and for electrical passive components in RF MEMS [84]. Fabrication of vias with high aspect ratios is often desired, and various methods for achieving such structures are shown in Fig. 3.21.

The different characteristics of these approaches are summarized in Table 3.13 and described as follows. First is the damascene process, used extensively in silicon VLSI processing [85]. In damascene, an oxide mold is used, and conformal seed layers are sputtered, followed by copper electrodeposition. Excess copper protruding from the molds is removed by chemical mechanical polishing (CMP),[6] leaving copper only in the via or trench. The interdielectric oxide layers bounding the copper are intended to remain at the end of the process, serving as an electrical insulator and mechanical supporting layer for the subsequent processes.

For 3-D polymeric-mold-based processes such as LIGA or UV-LIGA, CMP may damage the softer polymer mold material resulting in uneven surface morphology. To avoid polishing steps, several alternatives have been explored. The plate-through-mold approach uses seed layers deposited before the molds. The plating time is proportional to the depth of the mold, and the mold often must be removed after the plating, which lengthens the process time further. Moreover, removal of some polymeric molds such as polyimide or SU-8 often relies on expensive (and relatively slow) dry etching processes.

[6]See Chapter 13 (specifically Section 13.7) for more information on CMP.

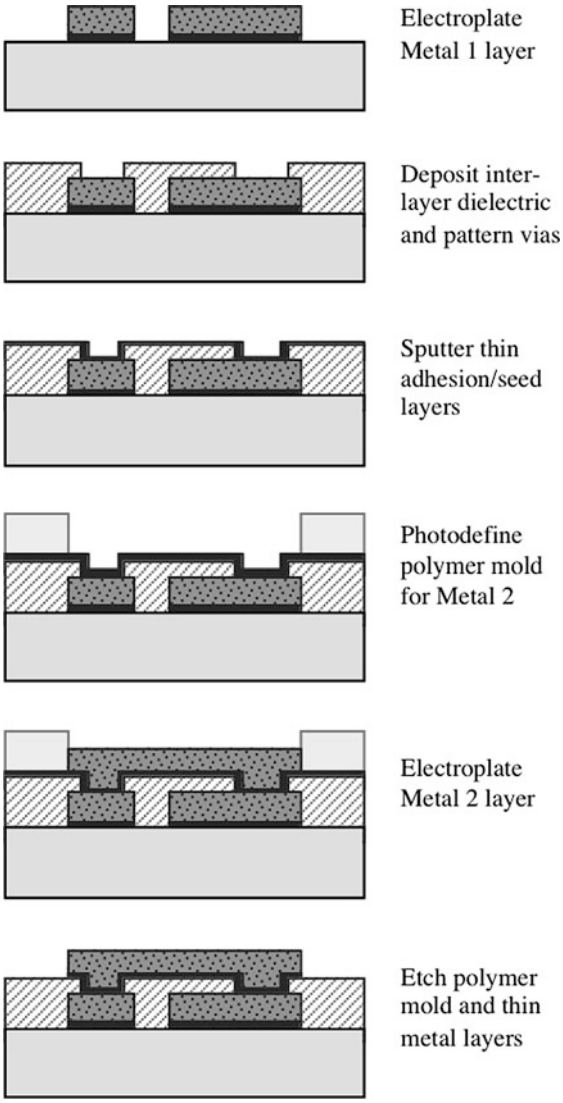

Fig. 3.20 Electroplating process to form multilayer conductive layers

Another approach – a wet etch back process – has also been used for high-aspect-ratio via connections with polymer molds [86]. This process is similar to damascene, except that a wet chemical etch is used to etch back protruding copper, as opposed to CMP. Although suitable for polymer molds, planarity is problematic.

An embedded conductor fabrication (as previously described in Fig. 3.20) uses mold formation and a combination of two simultaneous plating processes: a conformal plating process through nonremovable lower via mold and a conventional

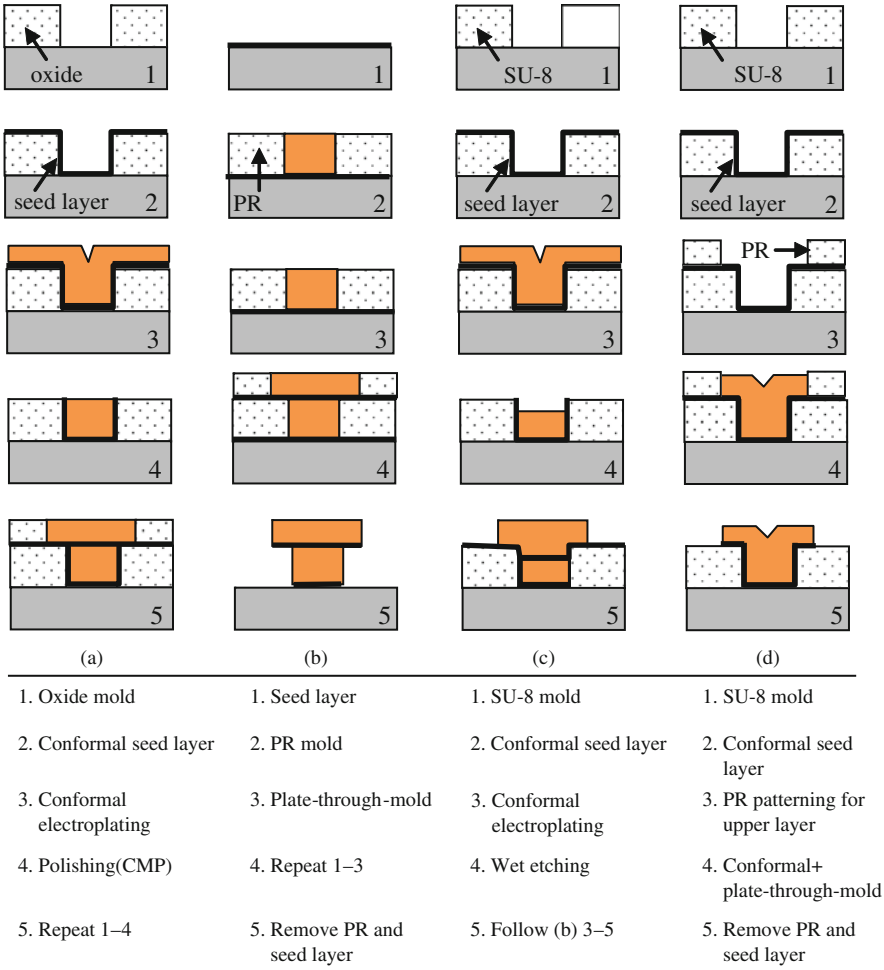

Fig. 3.21 Fabrication process comparison for one via and one upper conducting layer configuration: (**a**) damascene process; (**b**) conventional plate-through-mold process; (**c**) conformal plating process with etch back; (**d**) conformal plating without etch back [84] (Reprinted with permission. Copyright 2005 IOP)

plate-through-mold process through a removable upper conductor mold [84]. The vias are embedded in the mold from which they are formed: the mold is not removed after the structures are completed. This eliminates a long etching step for the mold removal, which simplifies and shortens the process. Also, the conformal plating makes the via fill time independent of the via height. At the end of the process, the conductors are embedded in the mold, resulting in good mechanical strength for subsequent process or packaging steps. The low-temperature polymeric process also facilitates post-CMOS compatibility if necessary.

Table 3.13 Various processes for multilayer conductor layers with vias [84]

	Damascene	Conventional plate-through-mold process	Conformal plating process with etch back	Conformal plating process without etch back
Mold material	Oxide (ceramic)	Polymer (organic)	Polymer (organic)	Polymer (organic)
Mold removal	No	Yes	No	No
Metal deposition time	Short	Long	Short	Short
Number of plating per two layers	2	2	2	1
Excess metal removal	Polishing(CMP)	No	Chemical etching	No
Mold erosion or metal dishing	Susceptible during CMP	N/A	Metal dishing during etch-back	N/A
Metal source usage	Noneconomical	Economical	Noneconomical	Economical
Device packaging	Injection molding	Polymer or cavity packaging	Injection molding	Injection molding
Applications	IC interconnect	MEMS actuator, RF passives, interconnect, power devices	MEMS interconnect, RF passives, power devices	MEMS interconnect, RF passives, power devices
References	[85]	[80]	[86]	[84]

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3.5 Materials Properties and Process Selection Guidelines for Metals

This section provides general guidelines for the selection of metals for use in MEMS. It also provides relevant material properties and application issues relating to adhesion, electrical, mechanical, thermal, and magnetic aspects.

3.5.1 Adhesion

Regardless of the intended functional application, adhesion of any metal to a particular substrate is critical to ensure successful microfabrication and long-term reliability. Adhesion depends on many factors, including type of substrate, roughness of the substrate, deposition methods, thickness of the film, and so on. The adhesion is determined by the interfacial energies of the interface, which may be metal–metal, metal–dielectric, or metal–polymer. Delamination occurs when the intrinsic and extrinsic stress in the deposited metal films overcomes the interfacial energy. Generally, cracking is caused by tensile stress, and peeloff by compressive stress.

Intrinsic stress is the result of crystallographic defects in the film, and extrinsic stress is due to the thermal expansion mismatch between the film and substrate [87]. For most MEMS applications, the extrinsic stress plays a major role. However, intrinsic stress can also be problematic. For example, stress accumulates with increasingly thick electroplated films, so this stress often limits how thick an electrodeposited layer may become.

Table 3.14 qualitatively summarizes the adhesion of various metals to different materials. Many metals, especially noble metals, do not adhere very well to common MEMS substrates such as Si, SiO_2, or glass. Often, however, thin layers of interfacial materials can be used to improve adhesion. The most widely used adhesion enhancing layers are Ti and Cr (as well as Ta and W) with thickness of 5–20 nm, usually sputtered or evaporated.

The reason for this enhancement is as follows [91]. These adhesion-promoting metals all readily oxidize, in contrast to noble metals such as Au, Ag, and Pt. Thus,

Table 3.14 Qualitative adhesion of thin film metals to different substrates

	Si [87]	SiO_2 [87]	Polyimide [88, 89]	PDMS [90]
Al	Moderate	Good	Moderate	–
Au	Moderate	Poor	Poor	Poor
Cr	Good	Good	Good	Good
Cu	Moderate	Poor	Poor	Poor
Ni	Moderate	Good	Poor	–
Pt	Moderate	Good	–	Poor
Ta	Good	–	Good	–
Ti	Good	Good	Good	Good

when an adhesion-promoting metal is deposited onto a substrate such as SiO_2, glass, or even a "clean" Si wafer with just monolayers of native oxide, chemical bonding occurs between the metal and the substrate by partial oxidation of a very thin interfacial layer of the metal. That oxide formation results in covalent bonding between the adhesion-promoting metal and the substrate. A metal deposited on top of this adhesion layer metal can interdiffuse with the adhesion-promoting metal and thus provide strong bonding of the top metal. For this mechanism to occur, the adhesion-promoting layer must not be exposed to air before depositing the second metal layer on top. If the top surface of the adhesion layer is air oxidized, it can no longer interdiffuse with the top metal, hence the bond between the two metals will be very weak and adhesion poor.

Many MEMS applications employ metals deposited on polymers. Metal/polymer interfacial issues are much more complex, with adhesion dependent on the concentration of functional groups on the polymer surface and the bond strength between the metal atoms and these functional groups [92]. The metal diffusion depth into a polymer has been found to inversely correlate with adhesion, that is, lower diffusion corresponding to stronger adhesion [89]. Other environmental and processing factors also play a role, as described below.

For polyimide, the adhesion of thin-film metals is generally good. Cu and Ni weakly bind to polyimide, Cr bonds strongly, and Al is somewhere in between [89]. In order to improve adhesion, an interfacial layer such as Ta can be used [93]. Or prior to deposition of metal, the polyimide surface can be modified by oxygen plasma, argon sputtering, or chemical etching (KOH) to enhance adhesion [88]. Note, however, metal–polyimide adhesion may deteriorate with exposure to high temperatures or high humidity [88].

PDMS has very low surface energy, so that when metals are deposited on top of it, wavelet morphology may occur on the PDMS surface [90]. This deformation may cause discontinuities or rupture of thin metal lines. Nevertheless, the adhesion of Ti and Cr on PDMS is good, so these are often used as an adhesion layer between PDMS and other metals such as Au and Pt. In addition, it is reported that the adhesion of metal with PDMS can be enhanced by plasma-treating the PDMS surface [92].

3.5.2 Electrical Properties

Metals are widely used in MEMS for electrical properties. Many pure metals are highly conductive, exhibit good adhesion to MEMS substrates, and good stability. Electrical interconnections (wires) are the most obvious and widespread electrical application for metals. Here, the most important parameter is the electrical resistivity (or inversely, conductivity). However, there are many other factors when considering selection of an appropriate metal for electrical applications. Table 3.15 summarizes some of these parameters, which are further discussed below.

The effect of skin depth must be considered for metals that will conduct high-frequency AC currents. The "skin effect" is the tendency for currents to be forced to

Table 3.15 Electrical properties of metals[a]

	Electrical resistivity (μΩ cm) [94]	Temperature coefficient of resistance (10^{-3} K^{-1}) [95]	Solderable [96]	Wire bondable [97, 98]	Self-passivating oxide [99]
Ag	1.62	3.8	Yes	Al	No
Al	2.71	3.6	Difficult	Au, Al	Yes
Au	2.26	8.3	Yes	Au, Al	–
Cr	12.6	3.0	No	No	Yes
Cu	1.71	3.9	Yes	Au[b]	No
Ni	7.12	6.9	No	No	Yes
Pt	10.7	3.9	Yes	Al	–
Ta	13.4	–	Yes	Al	Yes
Ti	39.0	–	No	No	Yes
W	5.39	4.5	No	No	–

[a]Electrical resistivity at 25°C; TCR values at 20°C
[b]Difficult, and reliability uncertain

the surface of a conductor, thus making the wire appear more resistive with increasing frequency. For this reason, increasing the cross-sectional area of a metal much beyond the skin depth does not result in lower resistance for an AC signal. The skin depths of most metals are only tens of micrometers above 1 MHz (e.g., the skin depth of Cu at 1 MHz is ~65 μm [100]). Most metals have a relative permeability of approximately unity, however, Ni and other ferromagnetic metals can have large permeabilities, leading to even smaller skin depths.

Most conductive materials also exhibit a change in resistance with temperature. The percentage resistance change per degree Celsius is referred to as the temperature coefficient of resistance (TCR) and is specified at a standard temperature. Most metals have a positive TCR, meaning that the resistance increases with temperature. The TCR is an important design consideration when metal structures are subjected to high/low temperatures or thermal cycling, especially for resistive-based sensors where unpredictable changes in interconnect resistance may affect the overall sensor performance. Metallic structures may also be specifically designed to take advantage of the TCR for sensing as a resistive temperature detector (RTD). In particular, Pt has a stable TCR over a wide temperature range, relatively high baseline resistivity, and good thermal stability, making it an ideal choice for use as an RTD.

Thermal and chemical stability are also critical to the long-term functioning of metals. Oxidation will occur on the surface of most metals in the presence of air. The impact of this oxidized layer will vary from metal to metal, and thus so too does the treatment necessary to prevent corrosion. Noble metals such as Au and Pt group metals do not readily form oxides, whereas some metals such as Al, Ti, and Cr form a thin, self-passivating oxidized layer that serves to protect the bulk of the metal from further oxidation [101]. The oxide layers of other metals such as Cu do not protect the bulk and thus have the possibility of total corrosion. Such metals must be passivated with a stable material if they are to be exposed to the atmosphere or harsh

conditions for long periods of time. Also, when creating contacts to these metals in successive metallization steps, the oxide should be removed immediately prior to the contact being made. Sputtering tools often feature an argon sample sputtering that can etch away the oxidized layer by ion milling. This is particularly useful, as the freshly cleaned metal surface is kept in an inert environment until sputtering the next metal.

Another important design aspect that can be easily overlooked is external connections. Most MEMS devices use bond pads on the chip surface for external electrical connections. These metal surfaces are exposed to the ambient environment, and subject to oxidation/corrosion, so exposed metals should exhibit self-passivating oxidation characteristics. It is also often desired to have metals that are easily solderable and/or wire bondable to facilitate device packaging.

3.5.3 Mechanical Properties

Although not as widespread as silicon or polysilicon, metals are also widely used for micromechanical elements such as beams, diaphragms, springs, hinges, and so on. The functionality and reliability of any mechanical structure depends heavily on the mechanical properties, requiring knowledge of elasticity, inelastic response, ultimate strength, and fatigue. For several reasons, however, mechanical properties of deposited films are one of the most problematic issues in MEMS designs.

First, the properties of microfabricated thin films can differ greatly from the bulk properties. Second, the mechanical properties of a material depend on both purity and microstructure, which for thin films can be very sensitive to film thickness and deposition conditions. Because of the planar fabrication processes used for MEMS, many films may be transversely isotropic (different properties in-plane versus out-of-plane). For these reasons, although general guidance can be obtained by examining bulk isotropic properties, these numbers are likely not replicated in thin films. And because of the process sensitivities described above, tight process control is very important for obtaining repeatable material properties.

Another complication is that there are numerous techniques used to directly or indirectly measure mechanical properties, including tension/compression tests, bending tests, indentation tests, dynamic tests, passive strain sensors, and others [102, 103]. Some of these methods are prone to large inaccuracies, and/or are only suited for extracting certain mechanical characteristics [104]. As a result, multiple test methodologies with different test structures may be necessary to measure all important mechanical properties.

Electroplated Ni and Ni alloys – used in LIGA-based fabrication – are the most widely studied metals for their micromechanical properties. Here, the electroplating conditions play an important role in the microstructure and thus mechanical properties. As compared to bulk Ni, electroplated Ni films generally show a slightly lower modulus, but much higher yield strength [103]. The elasticity of thin-film Al, Cu,

Table 3.16 Mechanical properties of bulk metals commonly used in MEMS [105]

Material	Density (kg m^{-3})	Young's modulus (GPa)	Poisson's ratio (Unitless)
Ag	10500	83	0.37
Al	2700	70	0.35
Au	19280	78	0.44
Cr	7190	279	0.21
Cu	8960	130	0.34
Ni	8910	200	0.31
Pt	21440	168	0.38
Ta	16650	186	0.34
Ti	4510	116	0.32
W	19250	411	0.28

and Au usually matches their bulk properties, but like Ni, their ultimate strength is usually higher [103].

The bulk mechanical properties for the most common metals used in MEMS are tabulated in Table 3.16. These values provide the designer a starting point from which to work. For design and fabrication, more specific information is required. The reader is encouraged to find the appropriate literature but cautioned not to assume identical results will be achieved, even if carefully recreating the process steps and conditions. A film deposited in one system may differ from a film deposited under identical conditions in a different system.

3.5.4 Thermal Properties

Metals are also widely used for thermal applications. They are often used as heat spreaders or thermal conductors, because most metals exhibit high thermal conductivity. They are also commonly employed in thermal bimorph actuators, where two materials with differing thermal coefficients of expansion (TCEs) are used to form a thermal actuator. Table 3.17 summarizes the bulk thermal properties of commonly used metals for MEMS.

Most metals tend to exhibit larger TCEs than semiconductors or dielectrics, thus enabling highly mismatched bimorph structures such as Al with SiO_2. For these actuators, the metal may also be used as a heater so that the actuation control is via electrical current. The converse side of this is that thermal mismatch can also create significant problems, such as thermally induced stress. This can be problematic, especially in packaging of mechanical systems.

Although metals generally have fairly high melting points, care must be exercised when considering high-temperature applications. Melting is usually not a concern, but, rather, diffusion or oxidation because many metals exhibit high diffusivity and propensity for oxidation. Special care, such as diffusion barriers or passivation layers, may be required to mitigate these surface interactions.

Table 3.17 Thermal properties of bulk metals commonly used in MEMS[a] [105]

Material	Thermal coefficient of expansion (10^{-6} K^{-1})	Thermal conductivity (W m^{-1} K^{-1})	Specific heat capacity (J kg^{-1} K^{-1})	Melting point (K)
Ag	18.9	429	235	1235
Al	23.1	237	897	933
Au	14.2	317	129	1337
Cr	4.9	93.7	450	2180
Cu	16.5	401	384	1358
Ni	13.4	90.7	445	1728
Pt	8.8	71.6	133	2041
Ta	6.3	57.5	140	3290
Ti	8.6	21.9	522	1941
W	4.5	174	132	3695

[a]Thermal conductivity at 27°C; specific heat capacity at constant pressure at 25°C

3.5.5 Magnetic Properties

Various metal alloys are known to exhibit strong ferromagnetic behavior. These magnetically responsive materials are usually categorized as either soft or hard magnets. Hard magnetic materials exhibit a strong magnetization in the absence of an external magnetic field. Therefore, they can provide a source of magnetic field without any external power. Conversely, soft magnetic materials retain little remanent magnetization, but they can be easily magnetized in the presence of a small magnetic field. Soft and hard magnetic materials are often used together to guide and concentrate magnetic fields in specific regions.

Magnetic materials for MEMS are used in various ways. Soft magnetic materials can be used with electroplated metal coils to form on-chip inductors and transformers. More complex devices such as actuators, motors, generators, or energy harvesters can also be built using hard and/or soft magnets. These structures capitalize on the same electromechanical phenomena employed in large-scale electric machines. The magnetostrictive (magnetic field-induced strain) properties of certain alloys can also be used for direct magnetomechanical coupling. Deposition of

Table 3.18 Summary of typical properties for soft magnetic electroplated alloys [40]

Material	Saturation flux density (T)	Easy-axis coercivity (Oe)	Resistivity (μΩ·cm)	Magnetostriction (ppm)	Film stress (MPa)
$Ni_{80}Fe_{20}$	1.0	0.2	20	< –3	100
$Ni_{45}Fe_{55}$	1.7	0.5	40	+20	160
Co–Fe–Cu	1.8–2.0	< 1		± 3	
Co–Ni–Fe	2.0–2.2	< 2	30	+3.5	115
$Ni_{20}Fe_{80}$	2.2	2.5	35	+25	240
Co–Fe	2.4–2.5	5–10		+45	845

Table 3.19 Select examples of hard magnetic films[a] [106]

Alloy	Deposition method	Integration notes	Thickness (μm)	Intrinsic coercivity H_{ci}(kA/m)	Remanence Br (T)	Energy product $(BH)_{max}$ (kJ/m^3)
Co–Ni–P	Plated	None	1–52	55–105[a]	0.06–0.1	1.3–1.8
Co–Ni–Mn–P	Plated	None	10–45	70–100	0.2–0.3	14
Co–Ni–Mn–P	Plated	0.2 T field	25	40–210	0.06–0.2	0.6–10
Co–Pt–P	Plated	(110) Si	2	370	0.6	52
Co–Pt–P	Plated	(110) Si substrate	8	330	1.0	69
FePt – $L1_0$	Sputtered	600°C anneal	6–7	446	–	124
FePt – $L1_0$	PLD	Small area	19–26	600	1.4	12–105
CoPt – $L1_0$	Plated	700°C anneal	10–16	800	0.37	–
Sm–Co	Sputtered	560°C anneal; glass/alumina substrate	3–50	1200	0.7–0.75	75–90
Sm–Co	Sputtered	400°C dep.; 750°C anneal	5	1035	0.8	140
Nd–Fe–B	Sputtered	500°C dep.; 750°C anneal	5	1280	1.4	400
Nd–Fe–B	PLD	650°C anneal; Small area	120	1000	0.55	77

[a]Coercivity H_c values, not intrinsic coercivity H_{ci}

magnetic alloy films is typically achieved via electroplating, sputtering, or PLD, inasmuch as good alloy control is necessary.

Selection of magnetic materials is very complex. Unfortunately, there is no universal "one-size-fits-all" perfect material for either soft or hard magnets. Rather, there are different microfabrication methods and different alloy combinations, each with advantages and disadvantages [40, 106]. For example, the higher saturation flux density soft magnetic alloys tend to have larger coercivities, and thus may not be suitable for high-frequency applications because of excessive hysteresis core losses. As another example, very high-performance hard magnets are possible, but they require high-temperature annealing, perhaps eliminating them from consideration because of process integration concerns. A thorough treatment of the design and selection of magnetic materials is beyond the scope of this chapter, but the information below provides a starting point for initial evaluation.

Soft magnetic metals are usually Ni, Fe, and Co metals and their alloys, such as Ni–Fe, Co–Fe, and Co–Ni–Fe. The properties required for soft magnetic materials are high-saturation flux density, high permeability, low coercivity, and high resistivity. In addition, low magnetostriction, low film stress, and good corrosion resistance are also desired. Table 3.18 lists typical soft magnetic electroplated alloys and their properties. $Ni_{80}Fe_{20}$ is the most widely used because of its good magnetic performance and relatively easy and reliable fabrication.

Hard magnetic metals include some transition metal alloys (e.g., Co–Ni–P, Co–P, Fe–Pt, and Co–Pt) and iron/cobalt-rich rare-earth intermetallics (e.g., $SmCo_5$, Sm_2Co_{17}, $Nd_2Fe_{14}B$). Hard magnets generally serve as a source of magnetic field, therefore the performance required for hard magnets are high energy density, high coercivity, and high remanence, as well as good thermal and chemical stability. Table 3.19 summarizes selected hard magnetic metal alloys. Co–Ni alloys are the most widely explored. They can be easily electroplated at low temperatures, but the magnetic properties are fairly weak. Electroplated Co-rich Co–Pt alloys (Co content approximately 80%) have also been developed with better performance. Equiatomic CoPt and FePt alloys have also been demonstrated with even better performance, but high-temperature annealing is required to induce an ordered $L1_0$ phase. Sputtered rare-earth alloys of Sm–Co or Nd–Fe–B offer the strongest properties (as in bulk), but these all require high-temperature deposition or annealing.

References

1. S.A. Campbell: Fabrication Engineering at the Micro- and Nanoscale, Ch. 12 (Oxford University Press, New York, NY, 2008)
2. S.P. Murarka: Chapter 9. Metallization in VLSI Technology (2nd Edition), S.M. Sze (Ed.), McGraw-Hill, New York, NY, 375–421 (1988)
3. R.J. Gnaedinger: Some calculations of the thickness distribution of films deposited from large area sputtering sources, J. Vac. Sci. Technol. 6, 355–362 (1969)
4. I.A. Blech, H.A. Vander Plas: Step coverage simulation and measurements in a DC planar magnetron sputtering systems, J. Appl. Phys. 54, 3489–3496 (1983)
5. Y.H. Park, F.T. Zold, J.F. Smith: Influences of DC bias on aluminum films prepared with a high rate magnetron sputtering cathode, Thin Solid Films 129, 309–314 (1985)

6. S. Kobayashi, M. Sakata, K. Abe, T. Kamei, O. Kasahara, H. Ohgishi, K. Nakata: High rate deposition of $MoSi_2$ films by selective co-sputtering, Thin Solid Films 118, 129–138 (1984)
7. D.H. Weon, J.I. Kim, S. Mohamadi: Design of high-Q 3-D integrated inductors for high frequency applications, Analog Integr. Circuits Signal Process. 50, 89–93 (2007)
8. M. Ataka, A. Omodaka, N. Takeshima, H. Fujita: Fabrication and operation of polyimide bimorph actuators for a ciliary motion system, J. Microelectromech. Syst. 2, 146–150 (1993)
9. M. Schlesinger, M. Paunovic: Modern Electroplating (Wiley, New York, NY, 2000)
10. D.R. Crow: Principles and Applications of Electrochemistry (Stanley Thornes (Publishers) Ltd., Cheltenham, 1998)
11. M. Paunovic, M. Schlesinger: Fundamentals of Electrochemical Deposition (Wiley, New York, NY, 1998)
12. D. Landolt: Electrochemical and materials science aspects of alloy deposition, Electrochim. Acta 39, 1075–1090 (1994)
13. H. Löwe, W. Ehrfeld, J. Schiewe: Micro-Electroforming of Miniaturized Devices for Chemical Applications, In J.W. Schultze et al. (Eds.): Electrochemical Microsystem Technologies, pp. 245–268 (Taylor & Francis, New York, NY, 2002)
14. T. Fritz: Charakterisierung galvanisch abgeschiedener Nickel- und Nickelwolframschichten für mikrotechnische Anwendungen, Dissertation D82 RWTH Aachen (2002)
15. A. Gemmler, W. Keller, H. Richter, H. Ruess: Mikrostrukturen- Prozesswissen erlaubt höchste Präzision (English: Micro devices – process models for high precision), Metalloberfläche 47, 461–468 (1993)
16. J.C. Puippe: Theory and Practice of Pulse Plating (American Electroplaters and Surface Finishers Society, Orlando, FL, 1986)
17. R.K. Sharma, A.C. Rastog, K. Jain, G. Singh: Microstructural investigations on CdTe thin films electrodeposited using high current pulses, Physica B 366, 80–88 (2005)
18. W. Wang, F.Y. Hou, H. Wang, H.T. Guo: Fabrication and characterization of Ni–ZrO2 composite nano-coatings by pulse electrodeposition, Scr. Mater. 53, 613–618 (2005)
19. M.V. Rastei, S. Colis, J.P. Bucher: Growth control of homogeneous pulsed electrodeposited Co thin films on n-doped Si(111) substrates, Chem. Phys. Lett. 417, 217–221 (2005)
20. F. Lallemand, L. Ricq, E. Deschaseau, L. De Vettor, P. Bercot: Electrodeposition of cobalt-iron alloys in pulsed current from electrolytes containing organic additives, Surf. Coat. Technol. 197, 10–17 (2005)
21. E. Becker, W. Ehrfeld, P. Hagmann, A. Maner, D. Münchmeyer: Fabrication of microstructures with high aspect ratios and great structural heights by synchrotron radiation lithography, galvanoforming, and plastic molding (LIGA process), Microelectron. Eng. 35, 35–56 (1986)
22. S. Harsch, W. Ehrfeld, A. Maner: Untersuchungen zur Hrestellung von Mikrostrukturen großer Strukturhöhe durch Galvanoformung in Nickelsulfamatelektrolyten, Reserach Centre Karlsruhe, Germany, Report No. 4455 (1988)
23. W. Stark, M. Saumer, B. Matthis: Nickelsulfamat-Elektrolyte für die Mikrogalvanoformung, Galvanotechnik 86, 1107–111 (1996)
24. M. Guttmann, J. Schulz, V. Saile: Lithographic Fabrication of Mold Inserts, In H. Baltes, O. Brand, G.K. Fedder, C. Hierold, J. Korvink, O. Tabata (Eds.): Advanced Micro and Nanosystems, Vol. 3: Microengineering of Metals and Ceramics, Ch. 8, pp. 187–219 (Wiley-VCH, Weinheim, 2005)
25. T. Fritz, M. Griepentrog, W. Mokwa, U. Schnakenberg: Determination of Young's modulus of electroplated nickel, Electrochim. Acta 48, 3029–3035 (2003)
26. W. Bacher, K. Bade, K. Leyendecker, W. Menz, W. Stark, A. Thommes: Electrodeposition of Microstructures, In N. Masuko, T. Osaka, Y. Ito (Eds.): Electrochemical Technology, Ch. 9, pp. 159–189 (Gordon and Breach, Kodansha, 1996)
27. R. Ruprecht, W. Bacher: Mikrogalvanoformung für die Weltraumforschung – Herstellen von Infrarotfiltern (English: Micro-galvanoforming for space research – production of infra-red filters), Metalloberfläche 45, 531–534 (1991)

28. P.M. Vereecken, R.A. Binstead, H. Deligianni, P.C. Andricacos: The chemistry of additives in damascene copper plating, IBM J. Res. Dev. 49, 1–18 (2005)
29. T. Osaka, Y. Okinaka, J. Sasano, M. Kato: Development of new electrolytic and electroless gold plating processes for electronics applications, Sci. Technol. Adv. Mater. 7, 425–437 (2006)
30. H. Honma, K. Hagiwara: Fabrication of gold bumps using gold sulfite plating, J. Electrochem. Soc. 142, 81–87 (1995)
31. J.J. Kelly, N. Yang, T. Headley, J. Hachmann: Experimental study of the microstructure and stress of electroplated gold for microsystem applications, J. Electrochem. Soc. 150, C445–C450 (2003)
32. N. Dambrowsky, J. Schulz: Gold plating in microsystem technology – challenges by new applications (original: Goldgalvanik in der Mikrosystemtechnik – Herausforderungen durch neue Anwendungen), Scientific Report FZKA 7308, Forschungszentrum Karlsruhe GmbH, Karlsruhe (2007)
33. M.J. Liew, S. Roy, K. Scott: Development of a non-toxic electrolyte for soft gold electrodeposition: An overview of work at University of Newcastle upon Tyre, Green Chem. 5, 376–381 (2003)
34. Y. Okinaka, M. Hoshino: Some recent topics in gold plating for electronics applications, Gold Bull. 31, 3–13 (1998)
35. A. Maner, W. Ehrfeld, R. Schwarz: Electroforming of absorber patterns of gold on masks for X-ray lithography, Galvanotechnik 79, 1101–1106 (1988)
36. A. Brenner: Electrodeposition of Alloys: Principles and Practice, Volumes I and II (Academic, New York, NY, 1963)
37. D. Landolt, A. Marlot: Microstructure and composition of pulse-plated metals and alloys, Surf. Coat. Technol. 169–170, 8–13 (2003)
38. P.C. Andricacos, L.T. Romankiw: Magnetically Soft Materials in Data Storage: Their Properties and Electrochemistry, In H. Gerischer, C.W. Tobias (Eds.): Advances in Electrochemical Science and Engineering, pp. 230–321 (VCH, Weinheim, 1994)
39. T. Budde, M. Föhse, B. Majjer, H. Lüthje, G. Bräuer, H.H. Gatzen: An investigation on technologies to fabricate magnetic microcomponents for miniaturized actuator systems, Microsyst. Technol. 10, 237–240 (2004)
40. E.I. Cooper, C. Bonhôte, J. Heidmann, Y. Hsu, P. Kern, J.W. Lam, M. Ramasubramanian, N. Robertson, L.T. Romankiw, H. Xu: Recent developments in high-moment electroplated materials for recording heads, IBM J. Res. Dev. 49, 103–126 (2005)
41. M. Föhse: Entwurf und Fertigung eines linearen elektromagnetischen Mikromotors nach dem Synchronprinzip, Dissertation, Universität Hannover (2005)
42. U. Kirsch, R. Degen: Hochpräzise und wirtschaftlich – Die Galvanoformung als hochpräzises Verfahren zur Abformung von Mikrozahnrädern, Metalloberfläche 61, 33–35 (2007)
43. T. Kohlmeier, V. Seidemann, S. Büttgenbach, H.H. Gatzen: An investigation on technologies to fabricate microcoils for miniaturized actuator systems, Microsyst. Technol. 10, 175–185 (2004)
44. S. Roy, A. Connell, A. Ludwig, N. Wang, T. O'Donnell, M. Brunet, P. McCloskey, C. Ómathúna, A. Barman, R.J. Hicken: Pulse reverse plating for integrated magnetics on Si, J. Magn. Magn. Mater. 290–291, 1524–1527 (2005)
45. Y. Sverdlow, Y. Rosenberg, Y.I. Rozenberg, R. Zmood, R. Erlich, S. Natan, Y. Shacham-Diamand: The electrodeposition of cobalt-nickel-iron high aspect ratio thick film structures for magnetic MEMS applications, Microelectron. Eng. 76, 258–265 (2004)
46. F.E. Rasmussen, J.T. Ravnkilde, P.T. Tang, O. Hansen, S. Bouwstra: Electroplating and characterization of cobalt-nickel-iron and nickel-iron for magnetic microsystems applications, Sens. Act. A Phys. 92, 242–248 (2001)
47. P.T. Tang: Pulse reversal plating of nickel and nickel alloys for MEMS. Proceedings SUR/FIN, Nashville, June 25–28, pp. 224–232 (2001)

48. J.O. Dukovic: Current Distribution and Shape Change in Electrodeposition of Thin Films for Microelectronic Fabrication, In H. Gerischer, C.W. Tobias (Eds.) Advances in Electrochemical Science and Engineering, pp. 117–157 (Verlag Chemie, Weinheim, 1994)
49. L.T. Romankiw, D.A. Herman, Proceedings of the Fourth International Symposium on Magnetic Materials, Processes and Devices, pp. 626–636 (The Electrochemical Society, Pennington, NJ, 1995)
50. A. Thommes, W. Stark, W. Bacher: Die galvanische Abscheidung von Eisen-Nickel in LIGA-Mikrostrukturen. Scientific Reports, Research Centre Karlsruhe FZKA 5586 (1995)
51. S. Abel: Charakterisierung von Materialien zur Fertigung elektromagnetischer Mikroaktoren in LIGA Technik. Dissertation, University of Kaiserslautern, Germany (1996)
52. S.D. Leith, S. Ramli, D.T. Schwartz: Characterization of Ni_xFe_{1-x} ($0.10<x<0.95$) electrodeposition from a family of sulfamate-chloride electrolytes, J. Electrochem. Soc. 146, 1421–1435 (1999)
53. U. Kirsch: Elektrochemische Abscheidung von spannungsarmen Nickel-Eisen-Legierungschichten und ihre Eigenschaften für Bauteile der Mikrosystemtechnik, Dissertation, University of Freiburg (Klaus Bielefeld Verlag, Friedland, 2000)
54. D.L. Grimmet, M. Schwartz, K. Nobe: Pulsed electrodeposition of iron-nickel alloys, J. Electrochem. Soc. 134, 3414–3418 (1990)
55. C. Müller, M. Sarret, T. Andreu: ZnMn alloys obtained using pulse, reverse and superimposed current modulations, Electrochim. Acta 48, 2397–2404 (2003)
56. J.Y. Fei, G.D. Wilcox: Electrodeposition of Zn–Co alloys with pulse containing reverse current, Electrochim. Acta 50, 2693–2698 (2005)
57. F. Giro, K. Bedner, C. Dhum, J.E. Hoffmann, S.P. Heussler, J. Linke, U. Kirsch, M. Moser, M. Saumer: Pulsed electrodeposition of high aspect-ratio NiFe assemblies and its influence on spatial alloy composition, Microsyst. Technol. 14, 1111–1115 (2008)
58. A. Brenner, G.E. Riddell: Nickel plating on steel by chemical reduction, United States Bureau of Standards, J. Res. 37, 31–34 (1946)
59. J.G. Jin, S.K Lee, Y.H Kim: Adhesion improvement of electroless plated Ni layer by ultrasonic agitation during zincating process, Thin Solid Films 466, 272–278 (2004)
60. F. Touyeras, J.Y. Hihn, X. Bourgoin, B. Jacques, L. Hallez, V. Branger: Effects of ultrasonic irradiation on the properties of coatings obtained by electroless plating and electro plating, Ultrasonics Sonochem. 12, 13–19 (2004)
61. F.A. Lowenheim (Ed.): Modern Electroplating, 3rd edn, Ch. 31 (Wiley, New York, NY, 1974)
62. A. Brenner, G. Riddell: Deposition of nickel and cobalt by chemical reduction, United States Bureau of Standards, J. Res. 39, 385–395 (1947)
63. A. Brenner: Electroless plating comes of age, Metal Finish. 52, 61–68 (1954)
64. N. Feldstein, T.S. Lancsek: Selective electroless plating by selective deactivation, RCA Rev. 31, 439–442 (1970)
65. T. Berzins: Alloy and Composite Metal Plate, U.S. Patent 3,045,334 (1962)
66. R.M. Hoke: Chemical Plating of Metal-Boron Alloys, U.S. Patent 2,990,296 (1961)
67. G.O. Mallory, J.B. Hajdu (Eds.): Electroless Plating Fundamentals and Applications, American Electroplaters and Surface Finishers Society (Noyes Publications/William Andrew Publishing, LLC, New York, NY, 1990)
68. A. Hung, K.-M. Chen: Mechanism of hypophosphite-reduced electroless copper, J. Electrochem. Soc. 136, 72–75 (1989)
69. P. Fintschenko, E.C. Groshart: Electroless copper plating, Metal Finish. 68, 85–87 (1970)
70. A.E. Cahill: Surface catalyzed reduction of copper, Proc. Am. Electroplaters' Soc. 44, 130 (1957)
71. O.B. Dutkewych, Electroless Copper Plating, U.S. Patent 3,475,186 (1969)
72. Y. Okinaka, In G.O. Mallory, J.B. Hajdu (Eds.), Electroless Plating of Gold and Gold Alloys, Ch. 11, American Electroplaters and Surface Finishers Society (Noyer Publications/William Andrew Publishing, New York, NY, 1990)
73. J.F. McCormack: Autocatalytic Gold Plating Solutions, U.S. Patent 3,589,916 (1971)

74. S. Mehdizadeh, J.O. Dukovic, P.C. Andricacos, L.T. Romankiw: The influence of lithographic patterning on current distribution: A model for microfabrication by electrodeposition, J. Electrochem. Soc. 139, 78–91 (1992)
75. J.K. Luo, D.P. Chu, A.J. Feewitt, S.M. Spearing, N.A. Fleck, W.I Milne: Uniformity control of Ni thin film microstructures deposited by through mask plating, J. Electrochem. Soc. 152, C36–C41 (2005)
76. K. Leyendecker: Untersuchungen zum Stofftransport bei der Galvanoformung von LIGA-Mikrostrukturen, Dissertation, Universität Karlsruhe (1995)
77. U. Gengenbach, I. Sieber, U. Wallrabe: Design for LIGA and Safe Manufacturing, In O. Brand, G. Fedder, C. Hierold, J. Korvink, O. Tabata (Eds.): Advanced Micro & Nanosystems, Vol. 7: LIGA and Its Applications, pp. 143–188 (Wiley-VCH, Weinheim, 2009)
78. V. Saile, U. Wallrabe, O. Tabata: LIGA and Its Applications (Wiley-VCH, Weinheim, 2009)
79. W. Menz, J. Mohr, O. Paul: Microsystem Technology, Ch. 7: The LIGA Process, p. 289 (Wiley VCH, Weinheim, 2001)
80. Y.J. Kim, M.G. Allen: Surface micromachined solenoid inductors for high frequency applications, IEEE Trans. Compon. Packaging Manuf. Technol. C 21, 26–33 (1998)
81. J.Y. Park, M.G. Allen: High Q spiral-type microinductors on silicon substrates, IEEE Trans. Magn. 135, 3544–3546 (1999)
82. J.-B. Yoon, C.H. Han, E. Yoon, C.K. Kim: Monolithic high-Q overhang inductors fabricated on silicon and glass substrates. Technical Digest of IEEE International Electron Devices Meeting, Dec. 5–8, 1999, pp. 753–756 (1999)
83. B. Morgan, X. Hua, T. Iguchi, T. Tomioka, G.S. Oehrlein, R. Ghodssi: Substrate interconnect technologies for 3-D MEMS packaging, Microelectron. Eng. 81, 106–116 (2005)
84. Y.K. Yoon, M.G. Allen: Embedded conductor technology for micromachined RF elements, J. Micromech. Microeng. 15, 1317–1326 (2005)
85. P. Gwynne: Back to the future: Copper comes of age, IBM Res. 35, 17–21 (1997)
86. F. Cros, K. Kim, M.G. Allen: A single-mask process for micromachined magnetic devices. Proceedings of the Solid State Sensor and Actuator Workshop (Hilton Head Island, SC), pp. 138–141 (1997)
87. J.A. Thornton, D.W. Hoffman: Stress-related effect in thin films, Thin Solid Films 171, 5–31 (1989)
88. M.K. Ghosh, K.L. Mittal (Eds.): Polyimides: Fundamentals and Applications, Ch. 20–21 (Marcel Dekker, New York, NY, 1996)
89. F.K. LeGoues, B.D. Silverman, P.S. Ho: The microstructure of metal-polyimide interfaces, J. Vac. Sci. Technol. A 6, 2200–2204 (1988)
90. N. Bowden, S. Brittain, A.G. Evans, J.W. Hutchinson, G.M. Whitesides: Spontaneous formation of ordered structures in thin films of metals supported on an elastomeric polymer, Nature 393, 146–149 (1998)
91. G. Jia, M.J. Madou: MEMS Fabrication, In M. Gad-el-Hak (Ed.): The MEMS Handbook, 2nd edn, Vol. 2: MEMS Design and Fabrication, pp. 3–114 (CRC Press/Taylor and Francis, Boca Raton, FL, 2006)
92. K.L. Mittal (Ed.): Adhesion Aspects of Thin Films, Vol. 2, p. 125 (VSP, Utrecht, 2005)
93. C.K. Hu, M.B. Small, F. Kaufman, D.J. Pearson, In S.S. Wong, S. Furuka (Eds.): Tungsten and Other Advanced Metals for VLSI/ULSI Applications, p. 369 (Materials Research Society, Pittsburgh, PA, 1989)
94. D.R. Lide (Ed.): CRC Handbook of Chemistry and Physics, 90th edn (CRC Press/Taylor and Francis, Boca Raton, FL, 2008). Internet Version available: http://www.hbcpnetbase.com/
95. G.T.A. Kovacs: Micromachined Transducers Sourcebook, p. 561 (McGraw Hill, Boston, MA, 2006).
96. J.R. Davis (Ed.): Base-Metal Selection, In Metals Handbook Desk Edition, 2nd edn (ASM International, Materials Park, OH, 1998)

97. S.K. Prasad: Advanced Wirebond Interconnection Technology (Kluwer, Bangalore, 2004)
98. G.G. Harman: Wire Bonding in Microelectronics, 2nd edn (McGraw Hill, New York, NY, 1997)
99. S.D. Cramer, B.S. Covino (Eds.): ASM Handbook, Vol. 13B: Corrosion: Materials (ASM International, 2005)
100. D. Jiles: Introduction to Magnetism and Magnetic Materials, 2nd edn, Ch. 2, 4 (CRC Press/Taylor and Francis, Boca Raton, FL, 1998)
101. T.W. Swaddle: Inorganic Chemistry: An Industrial and Environmental Perspective, p. 104 (Academic, San Diego, CA, 1997)
102. T. Yi, C.J. Kim: Measurement of mechanical properties of MEMS materials, Measurement Sci. Technol. 10, 706–717 (1999)
103. W.N. Sharpe: Mechanical Properties of MEMS Materials, In M. Gad-el-Hak (Ed.): The MEMS Handbook, 2nd edn, Vol. 1: MEMS Introduction and Fundamentals, Ch. 3 (CRC Press/Taylor & Francis, Boca Raton, FL, 2006)
104. V.T. Srikar, S.M. Spearing: A critical review of microscale mechanical testing methods used in the design of microelectromechanical systems, Exp. Mech. 43, 238–247 (2006)
105. M. Winter: WebElements: the periodic table on the web (2009). Available at http://www.webelements.com/ (Accessed July 1, 2010)
106. D.P. Arnold, N. Wang: Permanent magnets for MEMS. J. Microelectromech. Syst. 18, 1255–1266 (2009)

Chapter 4
Additive Processes for Polymeric Materials

Ellis Meng, Xin Zhang, and William Benard

Abstract Polymers are an increasingly important MEMS material. They are available in diverse forms and possess material properties not found in more traditional microfabrication materials originating from the integrated circuit industry. These include, for example, improved fracture strength, low Young's modulus, and high elongation. Many polymers also exhibit biocompatibility and chemical inertness which are desirable in challenging biological or chemical applications. Furthermore, low material and processing costs present interesting possibilities in MEMS both in terms of fabrication of novel research devices and mass production of inexpensive products. A variety of traditional and nontraditional processing approaches exists to manipulate polymeric materials as substrates, coatings, and sacrificial or structural layers in MEMS devices. A wide variety of polymer types and classifications exists (e.g., elastomers, epoxies, conductive polymers, hydrogels, thermosets, thermoplastics, etc.); it is the combination of material properties, processing conditions, and intended use (e.g., substrate, coating, sacrificial layer, or structural layer) that govern the selection of appropriate polymer type for a particular application. Several common MEMS polymer materials and their fabrication processes are reviewed here. The reader is also referred to Chapters 7, 8, and 9 for more in-depth discussions on wet/dry etching and lithography processes.

4.1 SU-8

Thick polymer structures with high aspect ratios can be produced in SU-8 polymer without requiring more expensive techniques such as X-ray lithography and deep reactive ion etching. SU-8 was developed and patented (U.S. patent 4882245) by IBM [1]. The original formulation consisted of EPON SU-8 resin (from Shell

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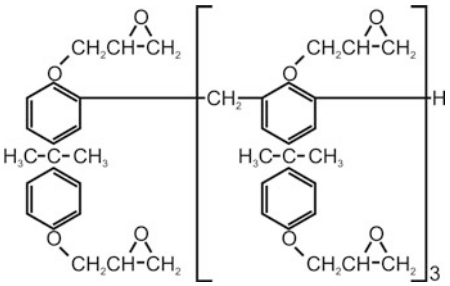

Fig. 4.1 Chemical structure of SU-8 which is a glycidyl ether of bisphenol-A novolac (Adapted from [5])

Chemicals), gamma-butyrolactone (GBL) solvent, and triaryl sulfonium salts as a photosensitizer (5–10% by weight) [1–3]. The high functionality of the epoxy (eight reactive epoxy groups per monomer unit) gives rise to the polymer name and also affords improved sensitivity over other formulations (Fig. 4.1) [4]. Subsequent SU-8 chemistries utilized other solvent formulation including methyl iso-butyl ketone (MIBK) and propylene glycol methyl ether acetate (PGMEA) [4]. In 1996, MicroChem Corporation (Newton, MA) commercialized SU-8 offering the product line NANO^{TM} XP SU-8 which was then followed by the SU-8 2000 and 3000 lines. These new formulations address some coating and adhesion issues encountered in the original formulation. For example, SU-8 2000 was formulated with cyclopentanone (C_5H_8O) solvent, which according to MicroChem, offers improved coating and adhesion properties.

SU-8 is a negative, near-UV resist, and a thermoset polymer. Although first used in 1997 as a replacement for X-ray lithography in the LIGA process (a German acronym for *Lithographie Galvanoformung und Abformung*) [6], SU-8 is an extensively employed MEMS material and was reviewed in [7].

A typical SU-8 lithography process includes the following step sequence.

- Spin coating
- Softbaking (extraction of solvent)
- UV exposure
- Post/hard baking (cross-link polymer)
- Development (may be enhanced with ultrasonic/megasonic bath or by spray)

Softbaking conveniently enables SU-8 films to self-planarize and smooth any edge bead build-up [3]. SU-8 possesses a high solids content (72–85% by weight) and low absorbance in the near-UV spectrum (~46% at 365 nm) which enables thick structures of a few hundred microns (over 500 μm with a single spin) [2, 4]. Thicker structures can be created with multiple layers; just two layers of SU-8 can produce 1.2 mm thick structures with an aspect ratio of 18 [3]. By repeating lithography steps, it is even possible to build open multilevel SU-8 structures [8–11]. When individual layer thicknesses greater than 1 mm are desired, it is advantageous to use a single constant volume injection step over multiple spin coating steps. SU-8 is

dispensed over a defined area and spread manually (at 80°C) to produce films up to 1.5 mm thick [12]. Thicker layers are limited by resist overflow at substrate edges. Six-layer SU-8 tissue engineering scaffolds have been reported [11].

UV exposure triggers generation of a strong acid that initiates the cross-linking process [13, 14]. Inclined or inclined/rotated lithography enable the production of three-dimensional structures using just a single layer of SU-8 and one mask [15]. Reflected UV energy can also be recovered to produce exotic structures. Three-dimensional structures can also be produced by exposing (with or without rotation) in multiple directions through a UV-transparent substrate (e.g., glass, sapphire, or quartz; Fig. 4.2) [16]. In addition to standard near-UV lithography, it is also possible to employ SU-8 as an X-ray resist. In fact, SU-8 possesses greater sensitivity and shorter exposure times compared to standard polymethylmethacrylate (PMMA) resists. Aspects ratios of up to 100:1 have been reported [17–19].

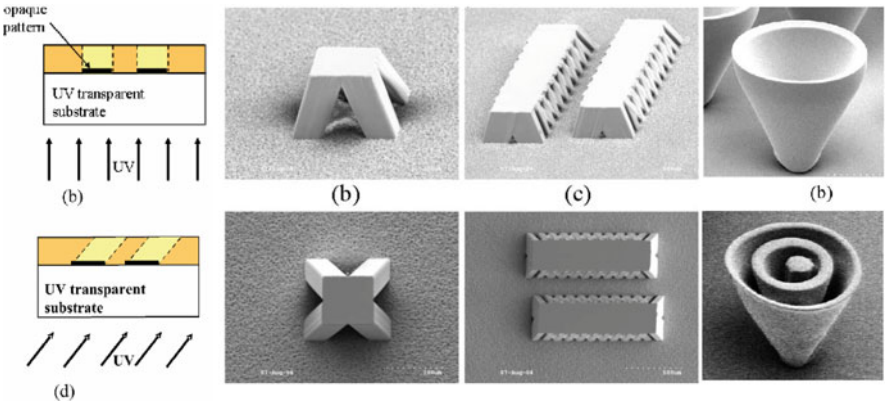

Fig. 4.2 (**a**) Backside exposure through a UV-transparent substrate. (**b**) Three-dimensional SU-8 structures produced by multidirectional and rotational back-side inclined lithography (Original figures used with permission from IEEE, copyright 2006 [16])

The postbaking step completes cross-linking of the UV-exposed polymer. SU-8 exhibits a high degree of cross-linking that enhances its physical properties but also induces stress on films and structures. Stress in SU-8 and methods to reduce its effects are discussed in detail in the "Lessons Learned" section below. Finally, SU-8 is usually developed in PGMEA.

4.1.1 Material Properties

SU-8 is well known to possess excellent thermal and chemical stability as a result of the aromatic nature of the resin and high degree of cross-linking [6, 20]. In particular, its chemical stability facilitates its application as an electroplating mold and as an etch mask, especially for prolonged plasma etching [4]. Its mechanical strength allows it to be a planarization layer in chemical mechanical polishing applications

[21]. However, it is well documented that the properties of SU-8 can vary widely with processing conditions [22, 23]. Further control of SU-8 properties is achieved by the addition of functional materials to the resist; tuning of electrical [24, 25], magnetic [26], optical [27, 28], and mechanical [29–31] properties was reported by several groups.

Bare SU-8 surfaces are hydrophobic and possess low surface energy (~73–80° and 45 mJ/m^2, respectively [32]) which limits their usefulness in microfluidics and as substrates for cell culture. Several surface modification techniques have been suggested to obtain hydrophilic SU-8 surfaces required for various applications. To facilitate filling of microchannels, an ethanolamine treatment was used [33]. Protein immobilization or cell attachment was promoted by grafting various polymers (polyethylene glycol (PEG), polyacrylic acid, and polyacylamide) to SU-8 via cerium(IV) ammonium nitrate [34]. Hydrogels grafted to SU-8 improved surface wettability and integration of bioanalytical functional layers such as enzymes and antibodies [35]. PEG has also been attached covalently to SU-8 surfaces [36]. By modifying PEG concentration or molecular weight, protein adsorption and cell attachment can be tuned. PEG as a MEMS material is discussed later in this chapter.

In addition to the aforementioned wet surface modification methods, hydrophilic SU-8 surfaces were also demonstrated using dry techniques. Hot wire chemical vapor deposition of amine groups facilitated immobilization of antibodies onto SU-8 cantilevers [37]. Oxygen plasma reduced the contact angle to 21° to facilitate filling of microchannels [38, 39]; argon plasma oxidized and roughened SU-8 surfaces (contact angle reduced to 29°) [32]. In contrast, efforts to render SU-8 superhydrophobic with low hysteresis using an excimer laser technique were reported (165°) [40]. It is also possible to increase the hydrophobicity of SU-8 simply by increasing the density of patterns on a surface (contact angle up to 147°) [41].

The versatility of SU-8 as a MEMS material has led to its extensive application in microfluidics and biomedical devices. However, SU-8 is not a USP Class VI material and the manufacturer (MicroChem) prohibits its use in implantable devices. Even so, initial studies indicate acceptable chemical compatibility and biocompatibility [42]. SU-8 coupons implanted in rats resulted in reduced biofouling in comparison to other common MEMS materials [43].

4.1.2 Processing Variations

4.1.2.1 Partial Exposure

By using multiple exposure wavelengths (313 and 365 nm), multiple exposure depths are possible in SU-8. Thus, multilevel structures are achievable with only a single spin coat [44]. This method was improved by adding antireflection coatings to the substrate to reduce unwanted reflections and achieve more accurate control of feature dimensions [45]. Layers that partially absorb UV exposure (SU-8 mixed with positive resist) have been successfully employed to produce multilevel

SU-8 structures [27]. Embedded metal masks have also been used in a similar manner [46]. Absorbing layers were particularly useful in the creation of embedded microchannels.

4.1.2.2 Direct Writing

Intricate structures having fine nanometer-scale dimensions have been produced by direct writing with e-beam writing [47]. Nd:YAG lasers and proton beams have also been explored for creating embedded microchannels and cantilever structures [48–50]. By combining UV lithography with stereolithography, three-dimensional SU-8 structures were fabricated [51, 52].

4.1.2.3 Removal of SU-8

Chemical removal of SU-8 occurs through crazing, peeling, delamination, or cracking but not through dissolution. Dissolution remains difficult due to the high cross-link density of the polymer. Chemistries suitable for removing SU-8 include:

- Hot *N*-methyl-2-pyrrolidone (NMP) [6, 53]
- H_2SO_4 [54]
- H_2SO_4/H_2O_2 [53]
- Fuming HNO_3 [53]
- NANO™ RemoverPG and Omnicoat™ (MicroChem Corporation, Newton, MA) [55]
- ACT-1(Air Products and Chemicals, Inc., Allentown, PA) (dimethylacetamide and monoethanolamine) [55]
- QZ3322 (Arch Chemicals, Norwalk, CT) (ethanolamine and tetrahydro-2-furanmethanol) [55]
- MS-111 (Miller-Stephenson, Danbury, CT) (methylene chloride, phenol, and organic acids) [56]
- Magnastrip (Inland Technologies, Tacoma, WA) (NMP-based) (70°C) [56]
- RS-120 (Cyantek, Fremont, CA) (sulfolane-based) (100–120°C) [56]
- Molten salt bath (Kolene® No. 5 and Kolene® No. 10, Kolene Corporation, Detroit, MI) (350°C) [56]

Note that although MS-111 is more effective than NMP in removing SU-8, it is rather toxic. Instead, Magnastrip and RS-120, which are less toxic, can be used [56].

Other SU-8 removal methods include pyrolysis, plasma etching, laser ablation, and water jet machining:

- Pyrolysis in O_2 or air (300–1000°C) [54, 56–58]
- O_2 and O_2/CF_4 plasma etching (0.9 μm/min for O_2 and 1.27 μm/min for O_2/CF_4) [6, 53, 59, 60]
- O_2/CF_4 downstream chemical etching (2.1 and 10 μm/min at 185 and 275°C, respectively) [56]

- O_2/SF_6 plasma etching (1.2–2 μm/min and improved sidewall angle but decreased etch rate with the addition of Ar) [61]
- Excimer laser ablation (248 nm KrF laser) [62]
- Water jet machining [63]

4.1.2.4 Release of SU-8

SU-8 release allows liftoff of electroplating molds and the formation of free-standing structures. The following techniques have been investigated for SU-8 release:

- NANO™ RemoverPG (80°C) [64]
- Thin metal sacrificial layer and wet chemical etching (SiO_2 [26], Al [3, 65], Ti [66], Cu [67, 68], Cr [69–71], Cr/Au/Cr [72]) (for release of 1–2 mm structures)
- Thick films (electroplated Cu [73], polystyrene [74], positive photoresist [66, 75], low temperature oxide [76], thermal oxide [13], whole Pyrex wafers [13], other oxides [77–79], polysilicon [80], whole Si wafers [81]) (for release of structures >2 mm)
- Peeling of SU-8 from release layer with poor adhesion to SU-8 (release layers include: spin on Teflon™ [82], plasma-deposited fluorocarbon [83], polyimide [20, 23, 84, 85], polyethylene terephthalate (PET) [86], self-assembled monolayers (SAMs) [77, 87, 88]) [70]
- Ultrasonic agitation of SU-8 on oxidized substrate [10]

4.1.2.5 Bonding

SU-8 can be joined to other polymers either through adhesive bonding or by lamination processes. Adhesives compatible with SU-8 include epoxy resin [89], UV curable epoxies [9, 12, 90], polymethylmethacrylate (PMMA) [91–93], and polydimethylsiloxane (PDMS) [94]. Lamination is achieved by using Riston (DuPont, Research Park Triangle, NC) (50°C) [95], benzocyclobutene (BCB) (Dow Chemical, Midland, MI) (pressure for 2 h and 200°C) [95], and GHQ120 crystal clear laminating film (GMP, Germany) (120–125°C) [94].

In addition, SU-8 itself is also widely used as an adhesive agent to join individual coupons, dies, and wafers together. SU-8 can be used in a variety of different states to achieve effective bonds including wet [96], softbaked [10], and semisolid [20]. Wafer-level bonding can be achieved with or without commercial wafer-bonding tools by controlling the vacuum level, pressure, and temperature [97–101]. In addition, there are several reports of achieving wafer-level bonding with very thin SU-8 layers [94, 102–105]. Special structures such as moats around channels prevent the reflow of uncross-linked SU-8 from filling channels and other gaps [101]. Also, conversion of the SU-8 surface to a hydrophilic one can promote bonding [39, 94]. For example, hydrophilic SU-8 (obtained by adding surfactant (10–40% trisiloxane alkoxylate, Silwet∗618, GE)) can be bonded to glass, Si, and PDMS without the application of pressure [106].

4.1.2.6 Transfer

An alternative route to the fabrication of multilayered or even free-standing structures in SU-8 combines bonding with transfer of SU-8 films. Flexible carrier substrates support the SU-8 during transfer and are then peeled off. Multilayer transfer has been demonstrated [84]. Carrier substrates used include Riston [8], polyimide [20, 84, 85], and PET [86, 107].

4.1.2.7 SU-8 as an Etch Mask

SU-8's excellent chemical resistance enables its use as an etch mask in both wet and dry processes:

- HF etching of glass [54]
- Electrochemical etching of nanoporous and macroporous Si [108]
- Reactive ion etching of Si in $SF_6/CBrF_3$ and $SF_6/CHF_3/O_2$ [2, 5]
- Plasma etching processes involving SF_6/O_2 [5] and CHF_3/Ar [109] etch chemistries

4.1.3 Lessons Learned

The many processing challenges encountered when using SU-8 are the focus of several process optimization articles [14, 22, 54, 110–113]. Dimensional accuracy and sidewall profile are linked to exposure. Thicker films require longer wavelengths for uniform exposure [113]. A "T-topping" phenomenon where the sidewall profile has a T-shape from the higher adsorption of shorter wavelengths is associated with using broadband UV sources. This effect is eliminated by applying a filter in the exposure path that removes wavelengths below 350 nm [44]. Aspect ratios can be increased by using megasonic agitation during development (up to 100:1, standard lithography) [114]. Megasonic development also decreases the overall development time.

Large stress gradients in SU-8 structures are often accompanied by out-of-plane curvature or fracture (Fig. 4.3) [115]. SU-8 films undergo a high degree of cross-linking during the postbake step. Although the cross-link density imparts many desirable physical properties, it also leads to brittleness and significant shrinkage (~7.5%) [8, 70]. If SU-8 is spun on an Si substrate, the fourfold difference in the coefficients of thermal expansion (CTE) of the two materials also results in high residual stress (16–19 MPa tensile stress [116]). At the very least, bowing of the substrate results [2, 3, 53] and in the worst case, there is delamination of the SU-8 [70].

Stress reduction in SU-8 films is achieved through a variety of processing modifications. A low-speed spin coating process followed by a polymer relaxation

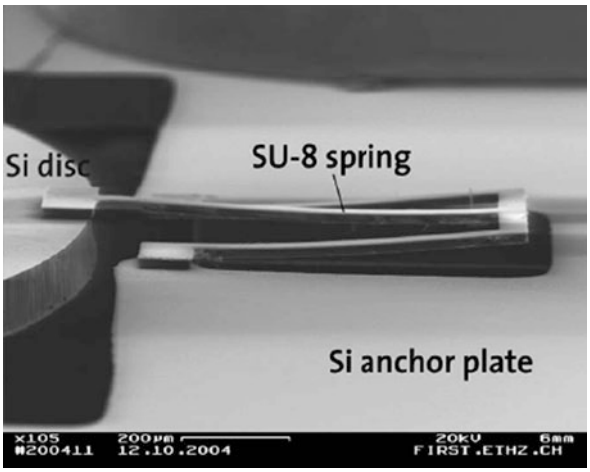

Fig. 4.3 Out-of-plane bending in a free-standing SU-8 spring element (Reprinted from [115] with permission from Elsevier, copyright 2006)

period prior to softbaking was found to reduce stress [14]. The curvature of SU-8 parts can be either positive, negative, or near-zero simply by optimizing exposure and postbaking steps [110, 117]. Both of these parameters follow similar trends: increasing the duration of exposure or postbake temperature increases the glass transition temperature as well as the cross-link density [23, 110]. Controlled temperature ramping at slow rates and multistep baking reduces thermal shock [14, 73]. It is noted that postbake steps carried out in vacuum environments may relieve stress [70].

Stress is further minimized during the design process. Large patterns should be divided into smaller areas to reduce thermal shrinkage-induced stress [9, 12, 73, 105]. For example, microchannels should be designed with thin walls and support posts [105]. Structures such as expandable fences and circular geometries may guide and distribute intrinsic stress [73].

Two additional stress-reduction strategies include modifying the SU-8 formulation (the addition of silica nanoparticles [29] or direct modification of the resist chemistry [118]) or the use of CTE matching layers or stress barrier layers. Multiple polymer matching layers have proved effective (Parylene C [119], PMMA, polyetheretherketone (PEEK) [20], and adhesive PET [86]) [53, 77]. Metal layers serve dual roles as a stress barrier and compensator [14, 78].

The use of intermediate layers may also promote adhesion of SU-8. SU-8 adhesion is gained by using adhesion promoter on substrates such as glass, Al, Cu, and Cr [55, 70]. SU-8 does, however, exhibit good adhesion on Au and Si without the use of adhesion promoters [6]. Examples of adhesion promoters include metal, thin SU-8 layers, and silanes (3-aminopropyltriethoxysilane (APTES), (for glass and Al), and AP300 (Silicon Resources, Chandler, AZ) (for stainless steel)) [55, 70, 105]. Reducing exposure dose and softbake time have been shown to improve adhesion but compromise aspect ratio [55].

4.1.4 Examples of SU-8 Application

SU-8 is a versatile material for the fabrication of microfluidic and lab-on-a-chip devices using a variety of different processing methods [120]. A diverse range of methods exist to produce simple or complex microfluidic channels and cavities [13, 45, 46, 48, 54, 65, 84, 86, 95, 98, 102, 105, 106, 121–123]. Microreactors are conveniently formed by defining cavities bounded by SU-8 walls [89, 90, 124]. Soft Parylene microchannel access ports are strengthened by patterning SU-8 supports [125, 126] or by defining anchors to secure PDMS septa for needle-based access to channels [119]. Other microfluidic structures produced with SU-8 include micromixers [10], microfluidic oscillators [93], nozzles [100], needles [127, 128], and check valves [67, 73].

4.2 PDMS

Polydimethylsiloxane (PDMS) is a commercially available cleanroom compatible silicon-based organic polymer. PDMS has a repeating unit of $(CH_3)_2SiO$ [129] as shown in Fig. 4.4. The properties of PDMS are attributed to and can be explained by the molecular structure. For example, the relatively low density and high diffusivity of gases are primarily the consequence of the larger Si–O and Si–C bond lengths compared to the C–C bond length, and the very low glass transition temperature and deformability are mostly related to the polymer chains packing and the amount of so-called "free volume." The solidification (curing) of PDMS is rationalized by an organometallic cross-linking reaction, as illustrated in Fig. 4.5. Notice that the siloxane base oligomers contain vinyl groups. The cross-linking oligomers contain at least three silicon hydride bonds each. The platinum-based curing agent catalyzes the addition of the Si–H bond across the vinyl groups, forming $Si–CH_2–CH_2–Si$ linkages. The multiple reaction sites on both the base and cross-linking oligomers allow for three-dimensional cross-linking. If the ratio of curing agent to base is increased, a harder, more cross-linked elastomer results. Heating the prepolymer also accelerates the cross-linking reaction.

Thanks to the unique properties and simple processing, PDMS is currently used, for instance, as the mechanical interconnection layer between two silicon wafers, as

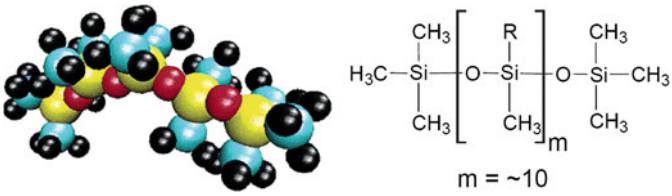

Fig. 4.4 The molecular structure of PDMS (R = CH_3 in the structure shown here for PDMS) (Used with permission from [134], copyright 1999, Division of Chemical Education, Inc.)

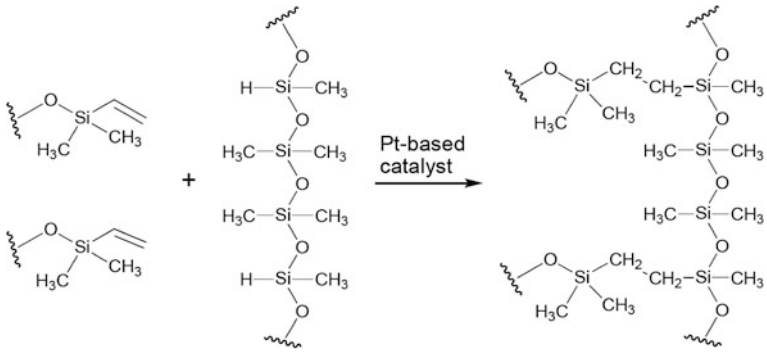

Fig. 4.5 Three dimensional cross-linking of PDMS. Used with permission from [134], copyright 1999, Division of Chemical Education, Inc.)

ion-selective membranes on ISFETs [130], and as the spring material in accelerometers [131]. It can be used as the top elastomer on a tactile sensor [132] without influencing the sensitivity of the device and a flexible encapsulation material in order to mechanically and chemically decouple sensors from their environment [133]. Furthermore, PDMS is used in sensors with integrated electronics due to its low-curing temperature.

4.2.1 Material Properties

This polymer is optically transparent with a UV cutoff of 240 nm, allowing for optical detection from 240 to 1000 nm. Some physical and chemical attributes of PDMS are (compared to other polymers) a low glass transition temperature ($T_g \sim -125°C$) [135], a unique flexibility (the shear modulus, G, may vary between 100 kPa and 3 MPa) [135], a very low loss tangent ($\tan\delta << 0.001$) [136], small temperature variations of the physical constants (except for the thermal expansivity, $\alpha \sim 20 \times 10^{-5} K^{-1}$ [137]), a high dielectric strength ($\sim$14 V μm^{-1}) [137], a high permeability to water vapor, gases, and nonpolar organic solvents [138], an impermeability to liquid water, a high compressibility, usability over a wide temperature range (at least from $-100°C$ up to $+100°C$) [139], a low chemical reactivity, and a nontoxic nature. Some typical material properties of PDMS are listed in Table 4.1.

PDMS is a viscoelastic material [146–148], and its mechanical properties change with loading frequencies [149, 150], and elapsed time durations [151, 152]. Although traditionally the viscoelastic properties have been neglected, recent advancements in material characterization have shown that ignoring the time- and frequency-dependent characteristics of PDMS results in errors in cellular force measurements, and erroneous interpretation of the measurement data of biological mechanisms. Hence, a more accurate model was determined through a material

Table 4.1 Typical material properties of PDMS

Property	Value
Glass transition temperature (T_g) [135]	$\approx -125°C$
Mass density [140]	0.97 kg/m^3
Young's modulus	360–3000 kPa
Poisson ratio [140]	0.5
Tensile or fracture strength [140]	2.24 MPa
Specific heat [140]	1.46 kJ/kg K
Thermal conductivity [140]	0.15 W/m K
Dielectric constant [140]	2.3–2.8
Index of refraction [140]	1.4
Electrical conductivity [140]	$4 \times 10^{13}\,\Omega$m
Magnetic permeability [140]	$0.6 \times 105\,\text{cm}^3/\text{g}$
Wet etching method [141]	Tetrabutylammonium fluoride ($C_{16}H_{36}FN$) + *n*-methyl-2-pyrrolidinone (C_5H_9NO) 3:1
Plasma etching method [141]	CF_4+O_2
Adhesion to silicon dioxide [142]	Excellent
Biocompatibility [143–145]	Nonirritating to skin, no adverse effect on rabbits and mice, only mild inflammatory reaction when implanted

characterization on PDMS materials for biological applications. Lin et al. determined the viscoelastic constitutive law of PDMS materials and developed a more appropriate model for cellular traction force measurement using the punch test system and finite element analysis (FEA), respectively [153]. Using the viscoelastic FEA model in dimensionless form (i.e., a dimensionless deflection $X^* = X/L$ and a dimensionless loading $P^* = P/P_0$, where L is the beam length and P_0 is the cellular force calculated by the small deflection beam theory), the mechanical forces generated by different loading rates could be determined (Fig. 4.6). The application of viscoelastic material characterization is not limited to the cellular traction force measurement and the results of their research are applicable to the analysis of other soft polymer materials at micro- and nanoscales (e.g., PMMA, in the above case, its glass transition temperature; and polyurethane, PU) [154] commonly used in biomedical industries, as well as biodegradable polymers (e.g., polybutylene succinate/adipate, PBD/SA) [155], soft lithography materials, and flexible electronic device materials [156].

4.2.2 Processing Techniques

The most commonly used fabrication technique for PDMS specimens is soft lithography which can duplicate inverted structures from a rigid mold [157]. PDMS can be easily molded to form and replicate features sized less than 0.1 μm. Because of its low surface energy, it can be lifted easily from molds and reversibly sealed to other materials without requiring intensive expertise. This ease of handling ensures rapid

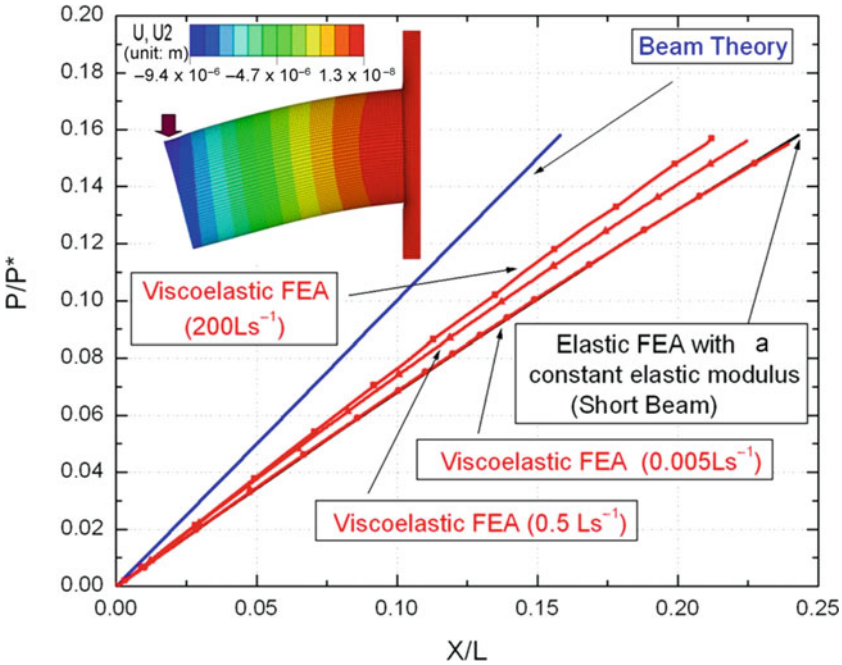

Fig. 4.6 Dimensionless form of force-displacement relationships for PDMS microcantilever shown by: (1) small deflection beam theory, (2) the elastic FEA model for short beams, and (3) the viscoelastic FEA model with different loading rates (Reprinted with permission from [153], copyright 2008, American Institute of Physics)

adoption of PDMS in biological research laboratories. An example of the PDMS structure is given below [144]. First, the base PDMS prepolymer and the curing agent are mixed with a ratio of 10:1 and then the mixture is stirred thoroughly for uniformity. The PDMS mixture is placed in a vacuum for 5 min to get rid of the air bubbles introduced during stirring. The PDMS mixture is then poured on top of the substrate, and spun at a low rate (about 500 rpm) to create a flat surface. Afterwards, the stack is placed on top of a hotplate for initial thermal curing (or "precuring") at 65°C (Fig. 4.7a). The curing time is carefully controlled so that the PDMS mixture does not fully cross-link. At the completion of the precuring, the molded pattern is slightly dipped onto the PDMS mixture and a light weight (e.g., 15 g) is applied on top (Fig. 4.7b). The substrate is put back into the vacuum for 5 min (Fig. 4.7c). Upon returning to atmospheric pressure (Fig. 4.7d) the PDMS mixture is thermally cured at 65°C for a second time (Fig. 4.7e). Following removal of the master template, the PDMS specimens, with various aspect ratios, are formed on the base substrate (Fig. 4.7f).

An alternative approach to PDMS fabrication is to make the PDMS prepolymer sensitive to ultraviolet (UV) wavelengths, and then it can be directly photopatternable. Several companies have commercialized photosensitive silicon containing polymers: WL-5000 silicones by Dow Corning for electronic packaging

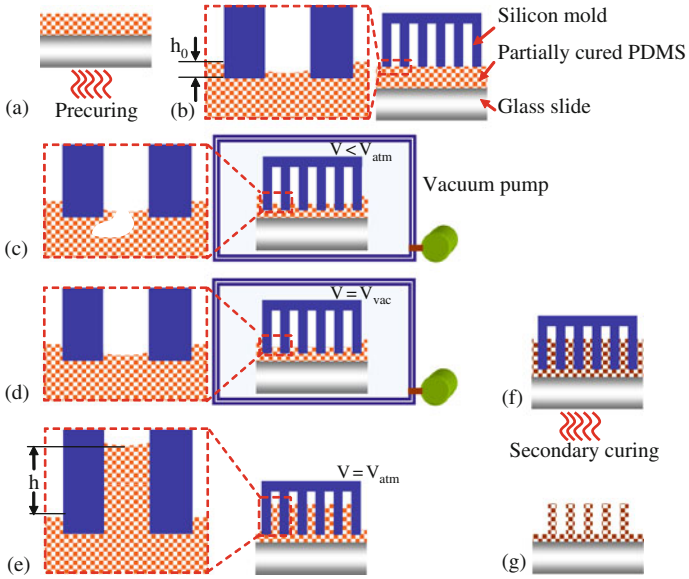

Fig. 4.7 Illustration of pressure-assisted micromolding: (**a**) PDMS prepolymer is precured on a glass slide. (**b**) The mold is slightly dipped into partially cured prepolymer. (**c**) Trapped air expands and some escapes with a certain vacuum level. (**d**) Trapped air reaches the equilibrium. (**e**) The polymer is raised when increasing the chamber pressure. (**f**) Secondary curing is conducted. (**g**) Cantilevers with various aspect ratios are formed after the removal of the master mold [144] (Reprinted with permission, copyright 2005, American Institute of Physics)

applications [158], cyclotene photosensitive resins from Dow Chemical (derived from benzocyclobutene (BCB) monomers) as dielectrics [159], and inorganic–organic hybrid polymers (ORMOCER) [160] for optical applications developed at Fraunhofer Institute and commercialized by Micro Resist. However, these new materials have different chemical nature and softness compared to the vinyl copolymers or pure PDMS polymers used in lithography thus far. Recently there have been some reports on photosensitive polymers by introducing photoinitiators, such as 2,2-dimethoxy-2-phenyl acetophenone (DMAP) [161] and benzophenone [162]. The application to PDMS has also been reported [163, 164]. The photodefinable mixture of PDMS and a photoinitiator, which eliminates the need of a master mold and the compatibility issues related to molding, provides a more efficient way of rapid prototyping polymer-based MEMS devices.

4.2.3 Biological Application Guide

Generally speaking, the biocompatible nature, rheological property, surface chemistry, and insulative property made PDMS a versatile material choice in biological applications as a functional, structural, and transfer material.

4.2.3.1 Stamp Material for Protein Transfer: Microcontact Printing

The microcontact printing (μCP) technique was first introduced by Kumar and Whitesides and coworkers at Harvard University in 1993, for patterning self-assembled monolayers (SAMs) of alkanethiols onto gold substrates [165]. The concept of μCP is straightforward: This technique is similar to flexography [166] which was adapted from the paper printing industry: alkanethiol "ink" was transferred to a gold "paper" by a prepatterned PDMS "stamp". Since then, the concept has been widely used for patterning substrates with biomolecules that enable future cell attachment and growth [167]. This includes, for example, folding of proteins and t-RNAs [168], formation of the DNA double-helix [169], and formation of the cell membranes from phospholipids [170]. First, the PDMS stamp is fabricated by the replica process from the PDMS prepolymer and mold (Section 5.2.2). Certain types of biomolecules are attached to a PDMS stamp pattern (Fig. 4.8a) and then transferred to a chemically activated substrate by direct contact of the substrate with the stamp (Fig. 4.8b). Unstamped regions are chemically treated with cell adhesion inhibitor (Fig. 4.8c), such as albumin, polyethylene glycol, or pluronic [171, 172]. However, biomolecules will remain in the stamped regions and allow cells to attach (Fig. 4.8d).

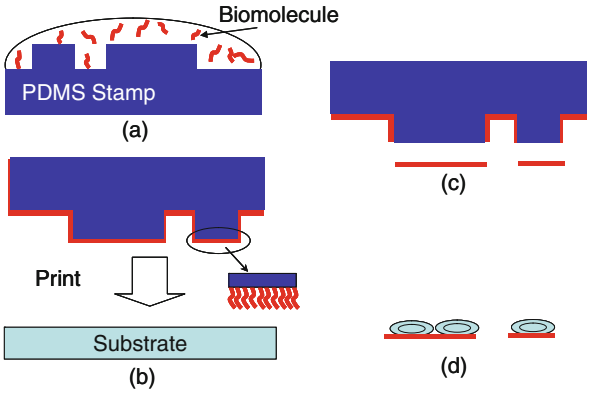

Fig. 4.8 The PDMS stamp transfers the biomolecule "ink" to a substrate upon brief contact: (**a**) Biomolecules are attached to a PDMS stamp. (**b**) Transfer to a chemically activated substrate by direct contact of the substrate with the stamp. (**c**) Unstamped regions are chemically treated with cell adhesion inhibitor. (**d**) Cells to attach to the biomolecules

4.2.3.2 Microfluidic Devices

Microfluidic devices have provided extraordinary advantages for biochemical analysis or synthesis. The basic concept of the microfluidic device is the integration of various chemical operations involved in conventional analytical processes done in a laboratory, such as mixing, reaction, and separation, into a miniaturized flow system. Ever-increasing attention has been garnered by microfluidic devices due to the extraordinary advantages of parallelization, automation, integration of sample preparation, low cost, short analysis time, and high sensitivity on separation and detection [173, 174].

PDMS has become a prime candidate as the building material of microfluidic devices for a variety of reasons. PDMS is much less expensive, easy to fabricate and bond with external components (e.g., glass, silicon, and other PDMS), has a variable thickness, and is less fragile compared to silicon and glass. Soft lithography techniques in PDMS have made the fabrication of microfluidic prototype devices with much shorter time and convenience than using silicon fabrication technology. Valves, mixers, and pumps can be easily fabricated and molded based on soft lithography procedures described in Section 4.2.2. The sealing of PDMS with other materials can be achieved either reversibly (e.g., van der Waals contact of PDMS-PDMS or PDMS-glass) or irreversibly (with the assistance of plasma oxidation or bonding of precured PDMS to a fully cured PDMS).

The physical properties of PDMS also make it favorable candidate as the functioning material for microfluidic devices. With its optical transparency for wavelengths ranging from 235 nm to near-infrared, PDMS enables optical detection over the entire visible spectrum, which is particularly attractive for the fabrication of microfluidic devices with an integrated optical detection or actuation system as shown in Fig. 4.9 [175].

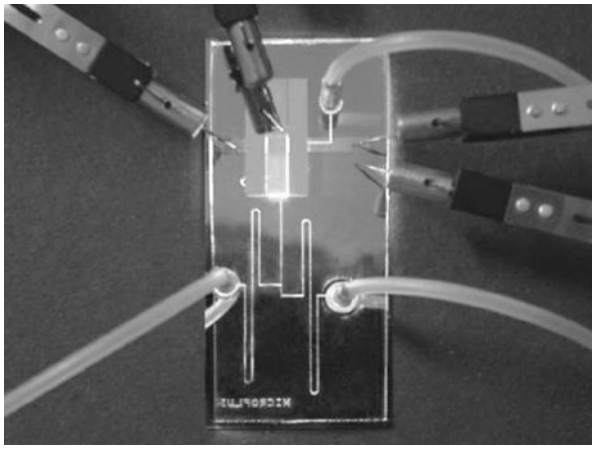

Fig. 4.9 The experimental setup for fluorescence detection. Green light is emitted across a microfluidic channel filled with phosphate-buffered saline (PBS) (Reprinted from [175], copyright 2006, IEEE)

PDMS is attractive for microfluidic applications because it is waterproof and has high gas permeability. These properties enable the inexpensive PDMS membrane to function without the integration of an electrostatic or electromagnetic flow control system. Many researchers have turned to PDMS microvalves and micropumps, along with pumps that rely on the gas permeability of PDMS, to produce fluid movement. For example, a thin membrane can be placed between a control channel layer and a flow channel layer. Fluid flow is triggered from the application of pressure across the thin PDMS membrane and the fluid flow can be controlled bidirectionally (Fig. 4.10) [176–178].

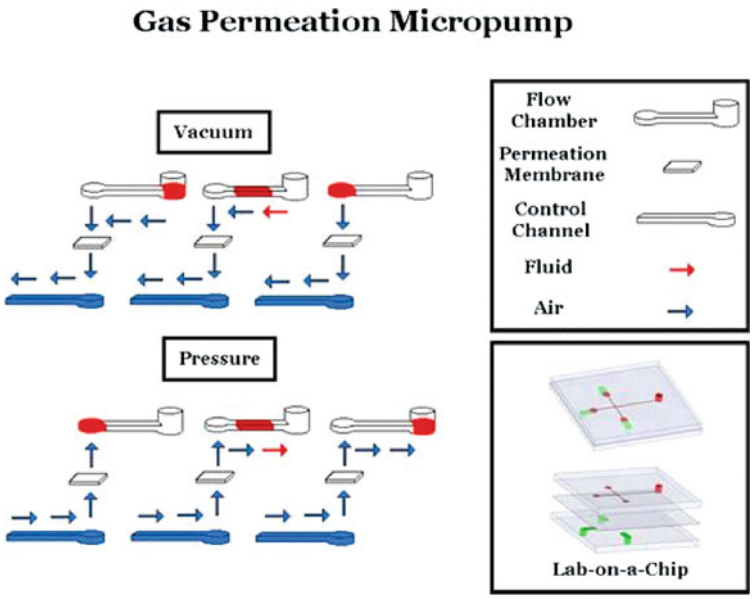

Fig. 4.10 Diagram of PDMS-based permeation pump mechanism within a microfluidic device (Reprinted with permission from [178], IOP)

The elastic property of PDMS also allows integration of microfludic devices with PDMS-based biomicroactuators that provide energy to drive both the solid microstructures and the fluid in the microchip. The low elastic modulus of PDMS enables bending of a PDMS micropost by the force exerted from a single cardiac myocyte. Unlike conventional microactuators, for example, PDMS-based cardiomyocyte biomicroactuators do not need an outside electrical power supply or stimulus. Because of their intrinsic cellular behavior, these biomicroactuators are gaining popularity as an energy source for biochemical reactors and biosensors [179]. Tanaka et al. presented the working principles of a PDMS-based cardiomyocyte biomicroactuator that uses PDMS micropillars driven repetitively by spontaneously pulsating cardiomyocytes as shown in Fig. 4.11. Both fluid and solid microstructures were successfully actuated utilizing the chemical energy of glucose which is subsequently converted into mechanical energy by cardiomyocytes. This prototype demonstrated the future potential of self-actuated and energy efficient microtransducers for in vivo applications [180].

4.2.4 Case Study

In this section, we give an example of PDMS being employed as a flexible material choice for a mechanical sensor for single-cell biomechano analysis. In recent efforts to measure the cellular traction forces of living cells, researchers developed

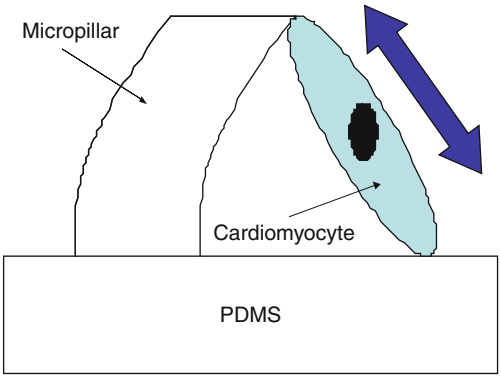

Fig. 4.11 Actuating principles of PDMS micropillars coupled to and powered by cultured cardiomyocyte

a technique that uses polymer micropillar arrays as extracellular matrices that cells can grow on, as shown in Fig. 4.12. Instead of measuring the cell reaction forces directly, this approach measures the deflection first and converts the deflections into reaction forces using appropriate mechanics of the mechanical sensor [144, 153, 181–185].

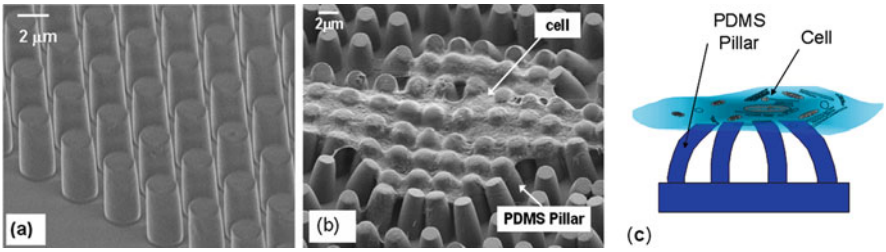

Fig. 4.12 (**a**) A SEM image of micropillar array of cellular traction force measurement system; (**b**) SEM image showing a smooth muscle cell cultured by on a PDMS micropillar array; and (**c**) schematic view of pillar bending during the cell contraction (Reprinted with permission from [153]. Copyright 2008, American Institute of Physics)

The low elastic modulus and flexible molding properties render PDMS an ideal material choice as mechanical sensors for cellular mechanics study [144, 153, 181–188]. Some of its unique advantages over other materials include (1) low stiffness allowing for the measurement of mechanical forces of cells in the piconewtons to micronewtons level; (2) ability to operate in biological environments, such as cultivated liquid or normal saline; and (3) a good biological compatibility, so that cells can survive on PDMS for a long period of time. The highly compliant and biocompatible PDMS meets all the required material characteristics as biomechanosensors. This is because the mechanical forces studied in cellular mechanics have considerable variation. For example, the forces generated by fibroblasts are on the order of hundreds of nN [181]; and the contractile forces of cardiac myocytes are measured in μN [182], whereas the forces generated by single filament, myosin, and

Table 4.2 Spring constant and probing range for microstructures with various geometries

Geometry		Spring constant		Probing forces on
D (μm)	H (μm)	(nN/μm)	Sensitivity (nN)	the order of
2	4	62.64	12.56	Over a hundred nN
2	6	10.20	2.04	Tens of nN
2	8	4.00	0.80	A few nN
2	12	1.36	0.27	Sub nN
8	24	58.15	11.63	Over a hundred nN

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kinesin are only 5–7 pN [189]. Taking advantage of the rheological properties of PDMS, cantilevers made of PDMS with varying mechanical stiffness are conveniently fabricated and tuned with desired aspect ratios [144]. Table 4.2 shows PDMS cantilevers with various aspect ratios replicated from a single silicon mold. Figure 4.13 illustrates the probing range with different geometry parameters [144]. Based on the adjusted spring constants, cantilevers with appropriate geometries for the measurements were selected.

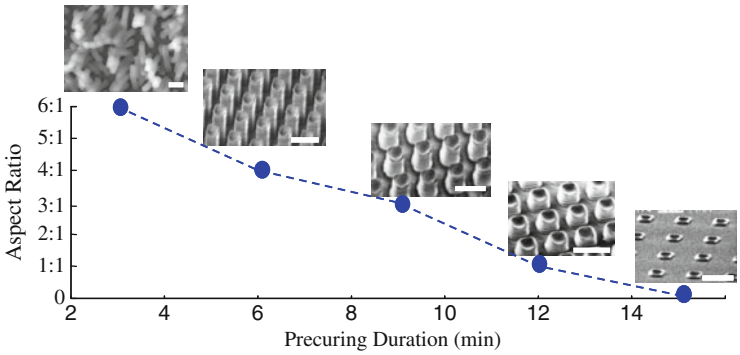


Fig. 4.13 PDMS cantilevers with various aspect ratios were replicated from a single silicon mold. Note that the cantilevers with aspect ratios 6:1 or higher collapse due to the low elastic modulus. *Spacebars* indicate 5 μm (Reprinted with permission from [144], copyright 2005, American Institute of Physics)

Here, the force measurement in isolated cardiomyocytes was demonstrated. Considering that the contraction force of cardiomyocytes is about a few nN, and the lateral dimension is about 20 μm by 100 μm, cantilevers with aspect ratios of 2:1 were manufactured and employed in cardiomyocyte force measurements. The resulting cantilever was 4 μm tall. The diameter of the root surface was 2.5 μm, and the diameter of the top surface was 2 μm with lateral penetration less than 0.1 mm. The spring constant in the presence of small deflection was derived as 62.64 nN/μm.

In order to perform monitoring of cell morphology and mechanical forces, the cells need to be viable on the stage of an optical microscope for a period of time

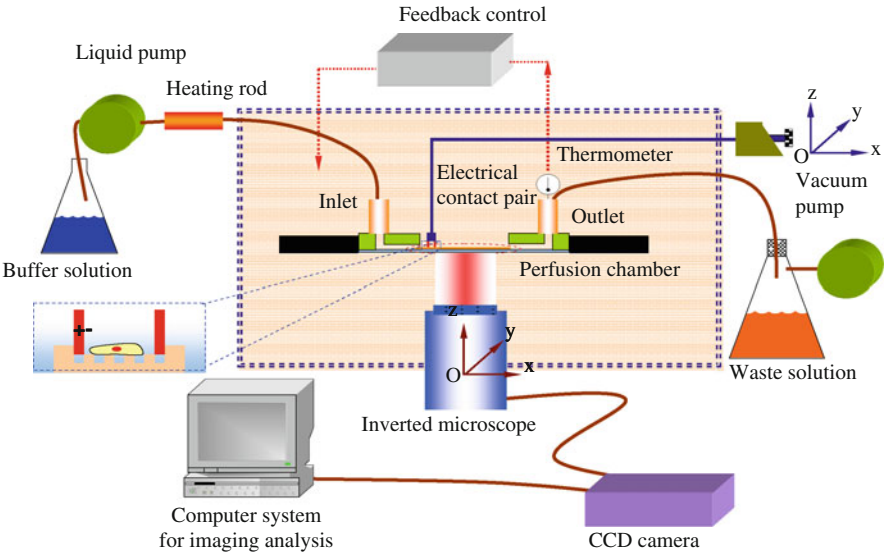


Fig. 4.14 Schematic of the in-situ force probing system for living cells (Reprinted with permission from [182], copyright 2006, Elsevier B.V.)

(preferably for a couple of hours). The experimental setup includes a perfusion chamber, temperature control components, fluidic connections, electrical connections, and image acquisition and analysis systems as shown in Fig. 4.14. The deflection of the pillars was measured by an inverted phase-contrast microscope and background noise was removed using MATLAB. A displacement map was calculated using the differences in pillar top positions (Fig. 4.15) [182]. Given that the magnitude of force exerted by the myocyte is dependent on the number and the alignment of the sarcomeres (the contractile unit of the myocyte), the vector component along the length of the sarcomeres is expected to be greater than the vector component transverse to the length of the sarcomeres. This conforms to the

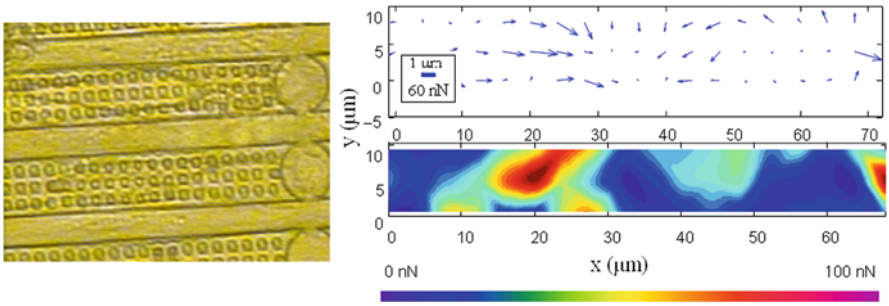


Fig. 4.15 The deformation vector maps and corresponding force vector maps obtained at systole of a single myocyte (Reprinted with permission from [182], copyright 2006, Elsevier B.V.)

physiological behavior of cardiomyocytes [182]. The amplitude of the force variation is a direct index of myocardial performance, which directly affects the blood pressure and pumping volume between the diastole and systole stages.

4.3 Polyimide

Polyimides have long been used in the microelectronics industry as both an insulator and packaging material. In particular, polyimides have been employed extensively as a planarization layer in forming multilevel interconnects [190–192] and for forming multichip modules [193]. Since the synthesis of the first aromatic forms of polyimide in 1908, advances in polyimide chemistry have led to its availability in a variety of forms including bulk (film or tapes with pressure-sensitive adhesive) or spin-on versions (photodefinable and nonphotodefinable) [194]. These are commercially available from HD MicroSystems (Parlin, NJ) and DuPont (Wilmington, DE). Polyimides were first introduced to MEMS as a flexible substrate material for sensor arrays [195] and multielectrode arrays [196, 197], both biomedical applications. Earlier reviews of polyimide in MEMS include [198, 199].

Polyimides may possess either an aliphatic (linear) or aromatic (cyclic) chemical structure and exhibit either thermoset or thermoplastic behavior (Fig. 4.16) [194]. To obtain the final chemical structure of polyimide, a polyamic acid precursor is imidized by baking at elevated temperatures (~300–500°C) [192, 195]. Polyamic acid is soluble in polar inorganic solvents (NMP, dimethyl formamide (DMF) and dimethylsulfoxide (DMSO)). The imidization process removes this solvent and in aromatic versions, closes the ring structure [200].

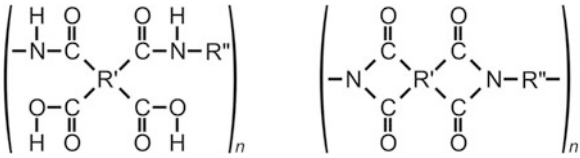


Fig. 4.16 Chemical structure of polyamic acid (*left*) and polyimide (*right*) in which the R′ and R″ may be aliphatic or aromatic (Adapted from [192])

4.3.1 Material Properties

Early applications of polyimide as a MEMS material capitalized on its low Young's modulus and ability to serve as a flexible substrate with potential biocompatibility and biostability for in vivo biomedical applications [195–197]. Its inertness [201] and low cytotoxicity [202] have been demonstrated in preliminary studies. Biocompatibility of polyimide-supported implantable microelectrodes has been demonstrated [203], however, many manufacturers expressly prohibit the use of their polyimides in implantable devices. Furthermore, polyimide is stiffer in comparison to other thin-film polymers (such as Parylene and PDMS) and has led to damage of delicate neural tissues [204, 205].

Other notable features of polyimides include high glass transition temperature, high thermal and chemical stability, low dielectric constant, high mechanical strength, low moisture absorption, and high solvent resistance [194, 199, 206]. This combination of features has led to the use of polyimides as replacements for ceramics [194], as chemically resistant electroplating masks [207], and as sacrificial layers [208]. Further review of the electrical and mechanical properties are available in [200, 209] and modification of electrical properties through the addition of graphite particles is described in [210]. Chemical modification of polyimide chemistry yields photosensitive versions having negative properties [207], however, these suffer from significant shrinkage during the imidization process. Thus, etching of standard nonphotodefinable polyimides yields higher resolutions [200, 207].

4.3.2 Processing Variations

4.3.2.1 Removal of Polyimide

Chemical removal of both cured and uncured polyimides is possible although wet removal of cured polyimides is difficult.

- Cured polyimides: hot bases and strong acids [200], H_2SO_4/H_2O_2 (selective over silicon nitride and oxide) [211].
- Uncured polyimides: bulk removal potassium hydroxide (KOH) (5–30%) [199, 207, 212, 213] and selective removal in KOH with photoresist mask [200].
- Dry etching is more effective for removing polyimide, including when used as a sacrificial layer [208, 214].
- Chemistries: O_2 plasma [215] or $O_2 + CF_4$, CHF_3, or SF_6 plasmas [199, 216–221].
- Etch masks: Al [199, 201, 208, 217, 219, 221–223], Cr/Au [218], PECVD silicon nitride [224], oxide [208], SiC [208].

Process optimization (gas concentration, plasma power, and ambient pressure) enables control of etched sidewall angles [220, 225–227] and high aspect ratios are possible with an electron–cyclotron resonance source [228]. Uncured polyimides may also be removed by dry etching [199].

Alternative dry removal processes include focused ion beam (FIB) [217] and excimer laser machining [213, 229–232].

4.3.2.2 Release of Polyimide

The simplest release technique is to peel polyimide away from Si wafers [201, 223, 233, 234]. Flexible electrode arrays are released from substrate carriers in this manner (Fig. 4.17). A number of sacrificial materials have also been used to promote release:

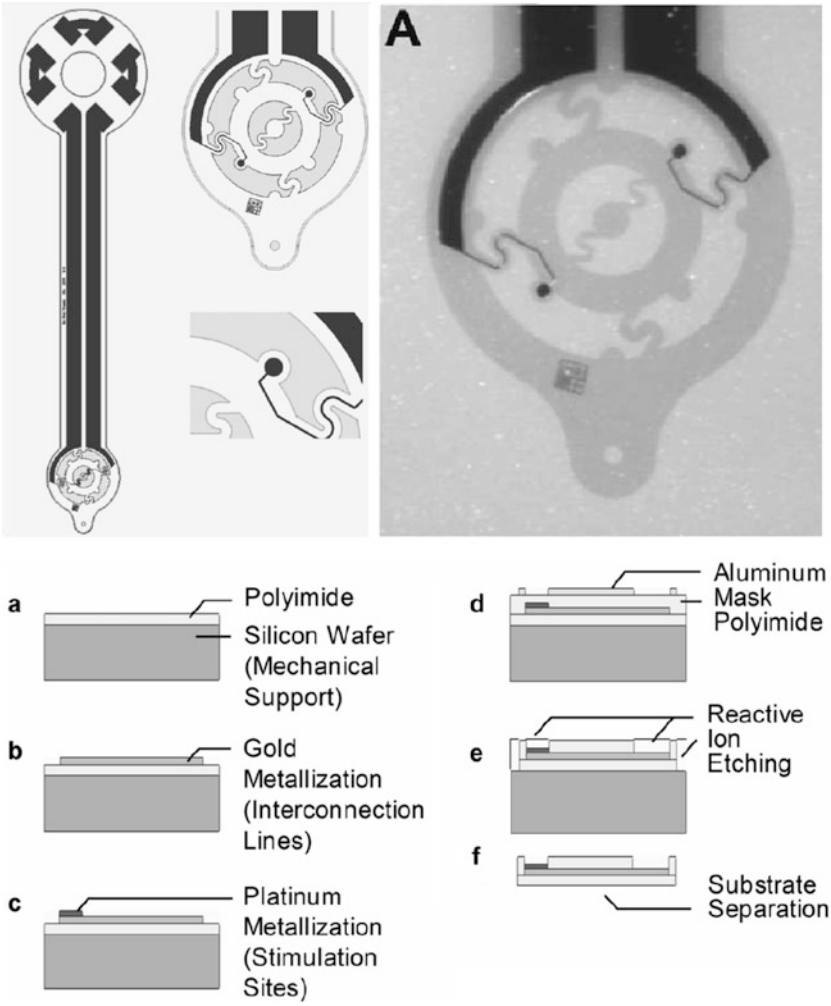


Fig. 4.17 (**a**) Layout with detail of a flexible retinal prosthesis on a polyimide substrate. (**b**) Close-up photograph of electrodes on the polyimide support freed by peeling off from a silicon carrier wafer. (**c**) Fabrication process for the retinal prosthesis (PI 2611, HD Microsystems) (Original figures reprinted from [234] with permission, copyright 2007, IEEE)

- Si substrates (undercut using HF:HNO_3 (hydrofluoric acid:nitric acid) (1:1) etch) [196]
- Oxide layers (dissolve in HF); if OH terminated (oxidized Si or Pyrex wafers), then hot wafer followed by buffered HF [202, 235]
- Al (wet release with a mixture of phosphoric–acetic–nitric acids and water [215, 236, 237] or anodic dissolution in neutral sodium chloride [65, 238])
- Thick electroplated Cu (dissolve in ferric chloride) [218]

- Cr ($HCl:H_2O$ 1:1 etch) [207]
- Ti (removal in dilute HF) [239, 240]
- Thermal decomposition of polymers (polycarbonates [65] and polynorbonenes [206]) (300°C and 370–425°C, respectively)

4.3.2.3 Bonding

Several bonding processes have been developed that utilize polyimide as an adhesive layer:

- RF dielectric heating of spin-on polyimide films to join Si pieces (1–4 bar clamping pressure, RF level of 500 W at 14 MHz, and 165–180 V_{rms}) [241]
- Electrostatic bonding of fully cured and chemical mechanical polished polyimide (350°C, 1 kg/cm^2 clamping pressure, and 100 V) (Fig. 4.18) [242]

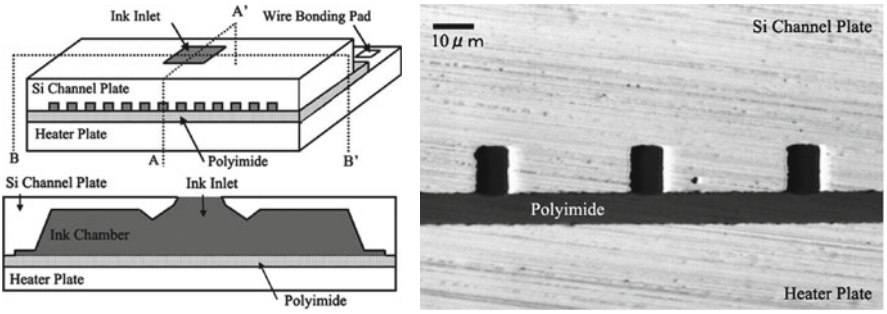


Fig. 4.18 (**a**) Schematic views of a thermal inkjet printhead assembled by polyimide bonding. (**b**) Photograph of assembled nozzle orifice showing polyimide adhesive layer (Duramide 7520, Arch Chemicals Inc.) (Original figures reprinted with permission from [242], copyright 2004, IEEE)

4.3.3 Lessons Learned

As in many MEMS polymers, adequate adhesion of polyimide to various substrates can be elusive. Although adhesion to Cr is excellent, adhesion to other substrates (such as Si, Si-derivatives, Al, and Cu) requires silane adhesion promoters [243]. Reactive ion etching in an oxygen plasma roughens polyimide surfaces to enable bonding to metals [244] and other polyimide layers [202].

Significant thermally induced dimensional changes in polyimide structures inevitably follow the imidization process. Shrinkage as high as 40–50% has been reported [202]. Although some applications may resort to using uncured films to avoid thermal shrinkage, most processes must account for this effect in the design. Below, a case study is presented that utilizes thermal shrinkage to fabricate out-of-plane structures.

4.3.4 Case Study

Thermal shrinkage due to imidization can also be used to one's advantage; hinge structures take advantage of the shrinkage for out-of-plane and self-assembly [245–247]. V-groove trenches were etched in Si and then filled with polyimide. This forms a polyimide joint that undergoes thermal shrinkage upon curing and results in the bending of attached structures (Fig. 4.19). By using multiple V-groove joints, it is possible to create bends of up to 200°. These polyimide joint actuators attached to Si legs were assembled into microrobotic conveyors [247]. In contrast, out-of-plane assembly of polyimide hinged structures was achieved manually [248, 249] or electrostatically [250, 251].

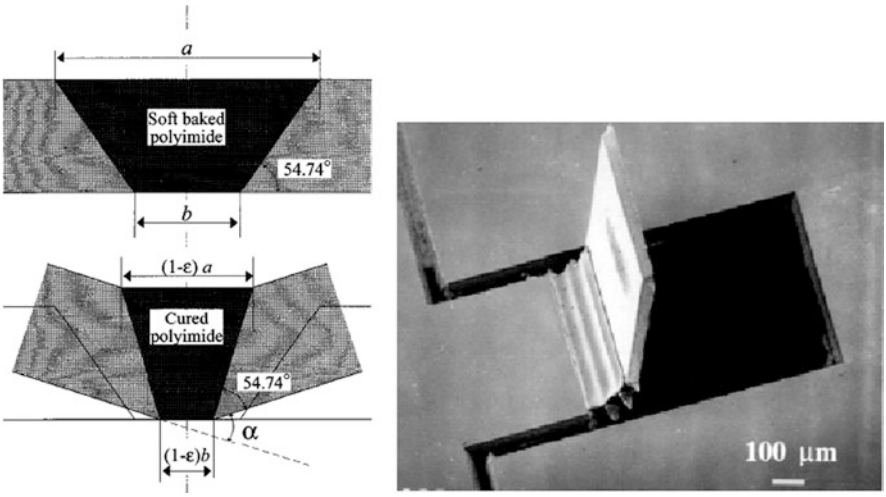


Fig. 4.19 (**a**) Principle of forming a polyimide V-groove joint by virtue or thermal shrinkage. (**b**) Out-of-plane assembly with a three V-groove joint (HTR-3 200, OCG) (Original figure from [246], used with permission of Institute of Physics Publishing Ltd.)

4.4 Hydrogels

4.4.1 Gelatin

Gelatin is well known as a both an edible dessert and binder for photographic films. It is an organic polymer that is arises from thermal denaturation or physical and chemical degradation of collagen; but unlike collagen, it does not exist naturally. The degradation process unfolds the triple helix structure characteristic of collagen and results in dissociated, unraveled, and disordered polypeptide chains [252, 253]. Cooling the gelatin allows partial recovery of the triple helix structure, albeit only in small regions, due to the random recombination of polypeptide

chains. At this point, gelatin becomes a thermoreversible gel [253–258]. Depending on the nature of the solidification process, gelatin can exhibit a wide range of physicomechanical properties; this is linked to the conformation of its constituent macromolecules (either collagen-like in helical format or having a coiled structure). Gelatin is less expensive than collagen but possesses similarities in its amino acid composition, structure, and properties [259]. Gelatin also possesses unique properties not found in collagen. It is edible, biodegradable, biocompatible, and nonimmunogenic [253].

The two types that are available, A and B, are differentiated by the method in which they are produced. Type A is produced by acid-treatment of the precursor whereas in contrast, Type B involves an alkaline treatment. These types are further categorized by the Bloom number which is a measure of the gelatin's mechanical strength. In the solid state, gelatin can be brittle at low humidity and high temperatures [259]. This property arises from its rigid chain structure. Gelatin is typically hydrophilic and can change properties depending on its water content. It conveniently has a low melting point (<100°C) [260] and is readily dissolved in warm water.

Gelatin is rendered photosensitive by the addition of a suitable photosensitizer. Examples of photosensitizers include potassium dichromate ($K_2Cr_2O_7$) and ammonium dichromate ($(NH_4)_2Cr_2O_7$) [260, 261]. Photosensitized gelatin is a negative tone resist that cross-links after exposure to UV; uncross-linked gelatin is simply removed by dissolution in warm water (~50°C). Gelatin solutions are spin processed up to concentrations of ~10% after which point an infrared heater is required [260]. Cross-linking imparts resistance to acids and bases. Gelatin is also cross-linked by applying glutaraldehyde (Fig. 4.20) [262–264]. Glutaraldehyde, however, is cytotoxic [258, 265, 266]. Other cross-linking agents, some less toxic, include formaldehyde, carbodiimide [267], dextran dialdehyde [268], and genipin [269]. Enzymatically cross-linked gelatins are biocompatible [270, 271]; transglutaminase is a naturally occurring enzyme capable of cross-linking gelatin [272]. A detailed protocol of microchannel fabrication using transglutaminase cross-linked gelatin is described in [273].

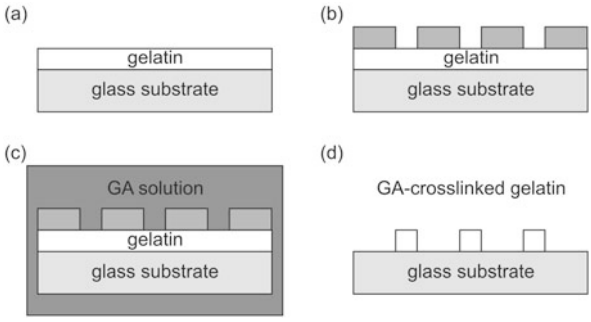


Fig. 4.20 Selective cross-linking of gelatin with glutaraldehyde (After [263])

Photolithographically defined gelatin has been used as a physical mask for sandblasting with Al_2O_3 particles [274] and its permeability enables grayscale masking during a thru-gelatin Cu electroplating process [261]. Gelatin is also resistant to plasma etching but develops surface roughness during the plasma exposure (0.1 μm/min, 400 W, O_2/SF_6) [260]. Alternatively, gelatin can be removed by enzyme digestion (proteinase K) [275]. Although the etch rate is slow (~50 nm/min in 1 mg/ml proteinase K solution), this offers new possibilities for the use of unphotosensitized gelatin as a sacrificial material. Here, photoresist was used as a masking material but suffers from poor adhesion to the underlying gelatin [260]. Fabrication of epoxy microchannels was performed using a gelatin sacrificial layer [276].

The thermoresponsive nature of gelatin allows its use as a "thermoresist." Gelatin films were patterned after contact with a heated stamp (50°C) and subsequently used as a mask to allow selective conjugation of molecules to underlying chitosan [262]. Following conjugation, gelatin was removed either with warm water or by digestion with a protease.

Immersion in water results in swelling and significant dimensional changes (up to twice the original geometry) [253]. Rinsing in ethanol or acetone extracts absorbed water but excessive extraction may induce cracks or delamination [260].

Gelatin adheres reversibly with PDMS [272] and adheres well with glass [260]. Adhesion to Parylene C was promoted by a brief plasma roughening step (1 min, 100 W, O_2/CF_4).

Release of gelatin from patterned Si is achieved by soaking Si surfaces for several hours in a 50% wt hexamethyldisilazane (HMDS) solution in hexane and appropriate thermal processing (30% wt gelatin (type B, calf bone derived, 200 Bloom), 25°C for 2 h followed by rapid air cooling at 5°C and 12 h of settling time). Although sealing to PDMS is reversible, PDMS molds treated with Pluronic® F127 (BASF Corporation) are nonadherent to gelatin [277, 278] and molded gelatin patterns are removed by warming (25°C) and flushing with 1% bovine serum albumin (BSA).

4.4.2 Chitosan

Like gelatin, chitosan is also a naturally occurring polymer. Chitosan is an *N*-deacetylated derivative of chitin which is commonly obtained from crustacean shells (Fig. 4.21). The natural origins of both materials impart a host of biomedically favorable properties such as nonimmunogenicity, biocompatibility, and nontoxicity. However, in contrast to highly insoluble chitin, chitosan is also biodegradable. In addition, chitosan has the ability to form gels, has optical clarity, is antimicrobial, and has been found to be conducive to the wound healing process. Unlike most natural polysaccharides which are neutral or acidic, chitosan is highly basic. Chitosan is a well-known biomedical material with applications in controlled drug delivery, sutures, contact lenses, and medical coatings [279].

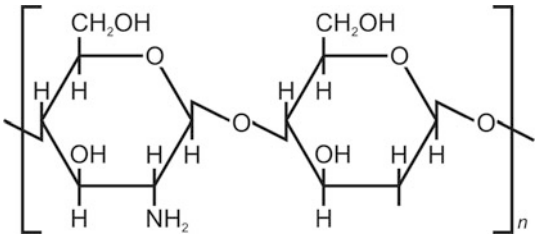


Fig. 4.21 Chemical structure of chitosan (Modified from [279])

Chitosan is produced by the deacetylation of chitin in 40% sodium hydroxide at 120°C for 1–3 h. This process typically yields 70% deacetylated chitosan. In this form, chitosan can be dissolved in dilute acids (such as acetic and formic); its solubility is pH-dependent [262]. Chitosan films were spin-casted from acidic solutions (typically 1–2% w/w). For example, contact lenses were spin-casted from squid pen chitosan [279]. Above a pH of 6.5 or in neutral conditions, chitosan is rendered insoluble [262, 280, 281]. Exposure of chitosan films to strong bases results in delamination (e.g., 1 M NaOH for 30 min) [262]. Chitosan solutions, mixed with hydroxyapatite (a bioceramic), can also be dispensed to create three-dimensional scaffolds with a feature resolution of ~200 μm [282].

In acidic solutions, chitosan is positively charged whereas it is negatively charged in basic solutions. This property enables the electrodeposition of several μm thick chitosan films onto the negative electrode. Plating was performed at a pH of 5 using a 1% w/v chitosan cationic polyelectrolyte solution [280, 283].

Chitosan can be selectively cross-linked by using naturally occurring phenol reactions such as anodic catechol oxidation. Cross-linking occurs through electrochemical oxidation only at patterned anodes [284]. Other chitosan biofabrication techniques are reviewed in [285]. Chitosan can also be rendered photosensitive [286]; following UV exposure, uncross-linked chitosan is rinsed away in phosphate-buffered saline (PBS). Although this process can achieve features down to 100 μm, the process is carried out while chitosan is in the solution state [287]. By adding a layer of PMMA between the photoresist and the underlying chitosan, the chitosan is protected from the photoresist developer and photopatterning is possible [288]. In the process shown below (Fig. 4.22), photolithography is performed and then the PMMA/chitosan layer is etched using the photoresist mask by reactive ion etching in an oxygen plasma (70 W, 50 sccm, 40 mtorr, 20°C substrate cooling, bias for vertical sidewalls, selectivity to photoresist of 1:1.65). Following patterning, it is also possible to undercut and release the chitosan structure by gas phase etching of the silicon substrate in XeF_2. The mechanical properties of both hydrated and dehydrated chitosan structures prepared using the process were also characterized [288].

Thermal imprinting of structures in chitosan films is accomplished by using soft PDMS stamps. In earlier work, glycerol was added to chitosan as a plasticizer to increase chain mobility and facilitate imprinting [289]. Glycerol addition lowered the modulus of the resulting film and enhanced transfer of thick structures.

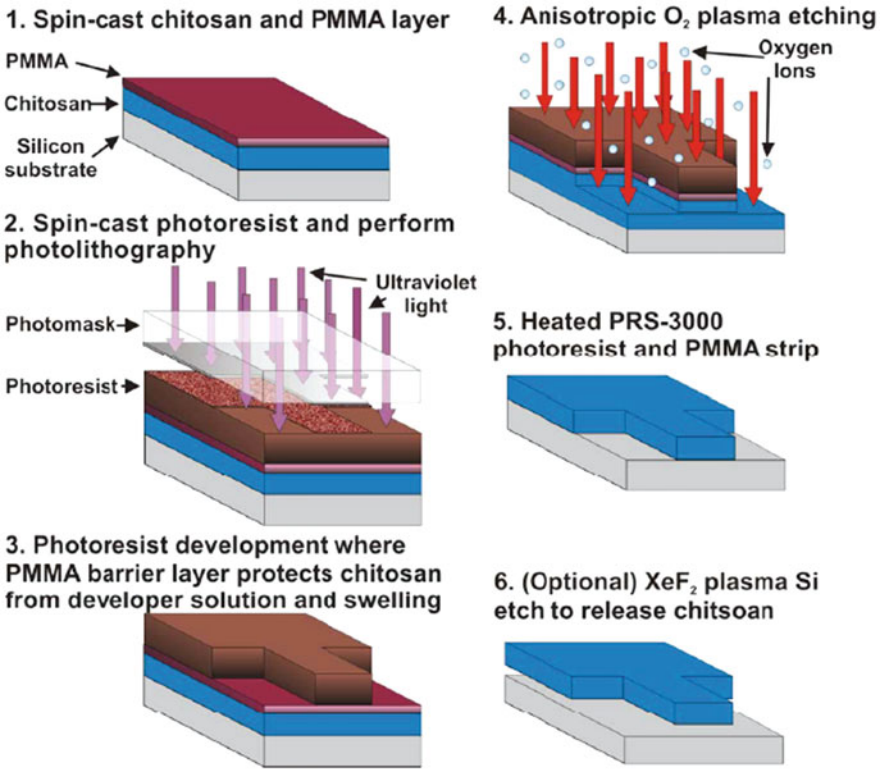


Fig. 4.22 Fabrication of chitosan structures by photolithographic techniques (Original figure reprinted with permission from [288], copyright 2008, IEEE)

Imprinting of 280 nm wide and 12 nm tall lines was achieved under low pressure and temperature conditions (25 kPa and 80°C with 1:1 glycerol-to-chitosan ratio (1.0 wt%)). Later, this process was simplified; plasticizers were omitted by directly imprinting wet chitosan films [290]. PDMS stamps were used specifically to allow for solvent evaporation through the stamp. Imprinting of nm features was performed at 5–25 psi and 90°C. PDMS stamps were easily released from chitosan structures without any prior surface treatment.

4.4.3 Polyethylene Glycol

Poly(ethylene glycol) (PEG) is a linear or branched polyether having the following structure: HO-$(CH_2CH_2O)_n CH_2CH_2$-OH [291]. This neutral hydrogel, also referred to as carbowax, possesses hydroxyl groups at either end and is available in many molecular weights. This Food and Drug Administration (FDA) approved

polymer is nontoxic, nonimmunogenic, and nonantigenic. Films of PEG act as biological passivation layers inasmuch as they can be applied to surfaces to reduce protein adsorption [292].

PEG is soluble in water and most organic solvents, allowing it to be applied to substrates from solution [293–297]. In surface modification applications, PEG has been applied by physical adsorption [298–303], covalent bonding (grafting or chemical coupling) [293, 296, 304–309], and self-assembly [310]. However, solution-based deposition techniques are not suitable for producing uniform, conformal, and ultrathin PEG films on surfaces. Dry vapor deposition approaches are available using ethylene oxide with a gas catalyst (boron trifluoride) for deposition on surfaces or within microchannels [291, 292, 311, 312]. Prior to deposition, surfaces (silicon or glass) are cleaned in piranha and silanized (3-aminopropyltrimethoxysilane (3-APTMS)).

Photosensitive PEG (negative photoresist) is possible by addition of a photoinitiator. PEG, PEG-diacyrlate (PEG-DA), PEG-methacrylate, PEG-dimethacrylate (PEG-DM), PEG-disilane, and PEG-tetraacrylate (PEG-TA) of varying molecular weights where modified with 2,2-dimethoxy-2-phenyl acetophenone (DMPA), 2-hydroxy-2-methyl propiophenone, and Irgacure 2959 photoinitiators. Solutions are spin-coated on substrates and then UV-exposed to cross-link the material [161, 310, 313–317]. Development is performed in water, solvent, or supercritical CO_2 [313, 315, 318]. PEG-DA and PEG-DM are preferred for short exposure times and low viscosity [317–319]. In addition, lower molecular weight formulations exhibit improved mechanical strength and less swelling when immersed in aqueous solutions [314, 317]. Irgacure 2959 photoinitiator is somewhat cytocompatible and has been used with PEG-DA (MW = 1000 Da) solutions to form a precursor used in three-dimensional stereolithographically defined tissue engineering scaffolds [316]. In this application, 20 or 30% (w/v) PEG-DA was required to form a gel following cross-linking by laser exposure (HeCd laser, 325 nm, 40 mW, 250 μm spot diameter). When using 15% (w/v) or less, a mechanically weak paste resulted.

Alternatively, PEG is either a masking material or a sacrificial layer with nm resolution when deposited by dip pen lithography [320]. Patterns were written on Au surfaces from 5 mg/ml acetonitrile solutions of PEG (MW = 2000 Da). When using the PEG as a masking material, the Au was selectively etched in 20 mM thiourea and 30 mM iron nitrate nonahydrate. To use the PEG patterns as a sacrificial layer, the masked surface was first selectively passivated with 1 mM 1-octadecanethiol (ODT). Following removal of the PEG by dichloromethane, Au features were etched using the same chemistry previously mentioned.

PEG may be selectively removed by oxygen plasma etching [321] or selectively deposited by screen printing [322]. For example, PEG (MW = 8000 Da) was screen printed by heating to 80°C and squeegeeing (Teflon blade) through an Al screen (2 kPa pressure and 8 ft/min speed). Deposited patterns were reflowed at 65°C to smooth the surface. These patterns formed sites for thermopneumatic actuation following deposition of Parylene to complete the chamber. Used in this manner, PEG may produce up to 30% volume change [322].

Stamping of patterns using a PDMS stamp is possible; a variation on this technique uses a PDMS mold and photosensitized PEG-DM in a capillary force lithography method [323, 324] for creating PEG structures for cell culture applications [314, 318]. However, PDMS molds were too soft; the tendency of features to deform, buckle, or collapse prevented creation of sub-100 nm features [325]. By replacing the PDMS mold with poly(urethane acrylate) (PUA), features down to 50 nm were reported [326–328]. It is necessary to treat PUA molds with 1% amorphous fluropolymer (Dupont Teflon AF2400) to facilitate mold release.

4.4.4 Case Studies

PEG may be used as either a sacrificial or structural material in conjunction with microfluidic channels. For example, although PEG is relatively soft, it is an excellent sacrificial material for temporarily increasing the stiffness of thin-walled Parylene microchannels [329]. This microfluidic neural probe must sustain 1 mN of force during the insertion process into the brain. As fabricated, the hollow probes would buckle below 1 mN (Fig. 4.23). By pulling PEG (MW $= 2700 - 3500$ Da) into the channel by suction and then cooling, the PEG-stiffened probes were successfully inserted (buckled at >12 mN). Following insertion, the PEG was dissolved upon contact with the physiological saline (~200 s to dissolve 7×10^6 μm^3 in the microchannel).

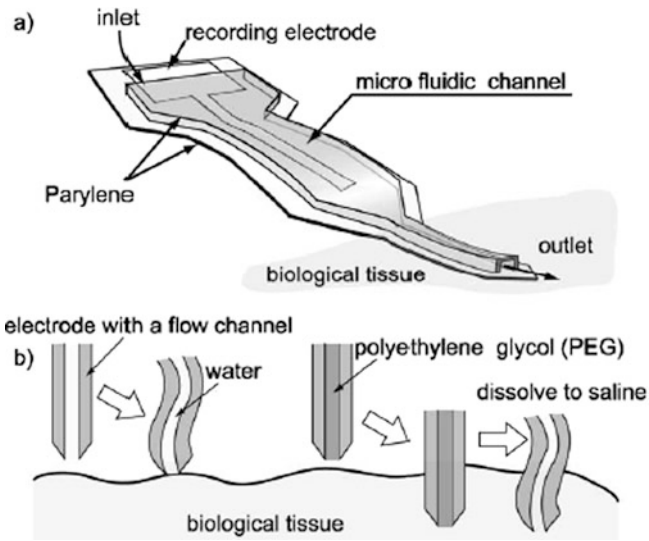


Fig. 4.23 PEG used as a sacrificial material to temporarily stiffen a fluidic probe for insertion into biological tissue. (**a**) The fluidic probe and (**b**) comparison of a hollow probe and PEG-filled probe during insertion into biological tissue (Reproduced from [329] by permission of The Royal Society of Chemistry)

PEG microchannels were directly formed without using a sacrificial layer by combining photosensitized PEG and irreversible UV sealing [317]. Two halves of the channel were formed from either low molecular weight PEG-DA or PEG-DM with 1 wt% UV initiator (DMPA). PEG was dispensed onto a silicon master mold and covered with a thin polyethylene terephthalate (PET) film for support. Following UV exposure, cross-linked films were demolded and fluidic access holes were drilled. Then the molded half was brought into contact with another supported PEG film (10^3 Pa pressure) and exposed to UV for a few minutes to irreversibly cross-link the contacted surfaces.

4.5 Parylene

Poly (*p*-xylylene) is the chemical name for the trademarked Parylene family of polymers offered by Specialty Coating Systems (Indianapolis, IL), the sole licensee of the original Union Carbide invention. Several alternatives to Parylene exist commercially that form in poly (*p*-xylylene) but differ in the synthesis path of the starting dimer (di-para-xylylene). However, only the Specialty Coating Systems version is currently approved by the FDA. Parylene is a USP (United States Pharmacopeia) Class VI material suitable for long-term implant and thus is well known historically in the medical industry as a biocompatible coating [330]. Many have examined its biocompatibility from different perspectives [42, 331–338]; its biostability, low cytotoxicity, and resistance against hydrolytic degradation are crucial attributes in Parylene's popularity as a biomedical material [42, 339, 340]. Poly (*p*-xylylene)s were reviewed in [341] and a brief review of their use in MEMS applications is found in [342].

Swarc synthesized the first Parylene (type N) in 1947 but development of a suitable deposition process delayed commercial introduction of the material until 1965; key enablers include the development of a stable dimer precursor and vapor deposition polymerization process by Gorham at Union Carbide [343–345]. Over 20 types of poly (*p*-xylylene) were synthesized, but only 4 are available as Parylene (types N, C, D, and HT) and 2 additional types are available as diX A and AM (Kishimoto Sangyo Co., Ltd., Japan). The chemical structure and defining features of each type are given below (Fig. 4.24 and Table 4.3). The type predominantly used in MEMS is Parylene C which is the focus of this section.

Parylene physical vapor deposition is performed in a vacuum and starts with the granular dimer which is loaded into a vaporizer (Fig. 4.25). The process parameters described here are standard for Parylene C. The temperature is ramped to 150°C, at which point the dimer vaporizes. Next, the dimer is pyrolyzed to cleave the dimer into the monomer radical para-xylylene (650°C). In the deposition chamber (25°C), the monomer adsorbs to all exposed surfaces and polymerizes at the rate of ~5 μm/h for Parylene C. Recently, a process was developed to directly deposit Parylene as a nanostructured thin-film by modifying the sample mounting apparatus in the deposition chamber [347–349].

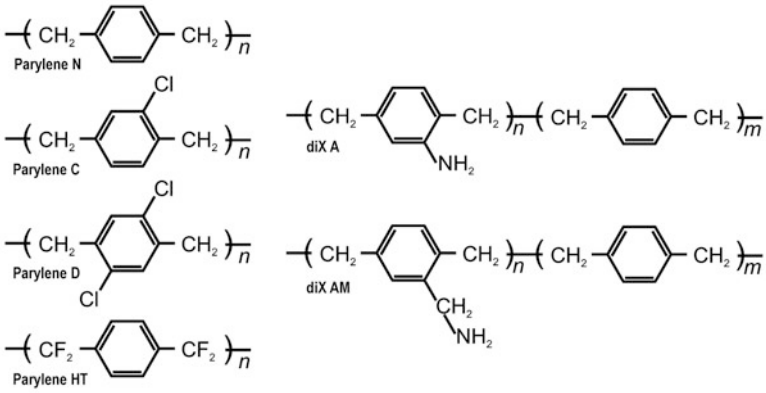


Fig. 4.24 Chemical structure of poly (*p*-xylylene)s (Original figure from [346], used with permission of Institute of Physics Publishing Ltd. 2008)

Table 4.3 Comparison of parylene types and their key features

Parylene type	Key features
N	High crevice penetration, lubricity, excellent electrical properties
C	Low permeability barrier, excellent combination of electrical and mechanical properties
D	High thermal stability
HT	Superior thermal, barrier, and electrical properties
A and AM	Amino group convenient for bonding to biomolecules

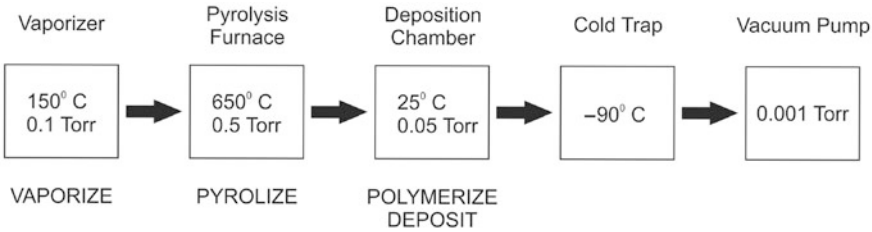


Fig. 4.25 Summary of deposition process (After [350])

4.5.1 Material Properties

Parylene is chemically inert, coats surfaces conformally, and is an excellent polymer barrier [339]. Historically, it has been used as a medical coating, an insulator

for implantable neural wire probes [351–354], an interlayer dielectric [355], and was later introduced to the MEMS community in 1997 as a coating material for fluidic interconnects [356]. Parylene has gained popularity as a standard MEMS material for its deposition method (vacuum-based), pinhole-free deposition, low process temperature, transparency, and compatibility with microfabrication processes [342]. Since its introduction to MEMS, Parylene was explored as a structural material [357] in a wide variety of MEMS applications [123, 204, 205, 329, 358–370]. Parylene in carbonized/pyrolyzed [371–373] and ion-implanted [374] forms have also found applications in MEMS as a sacrificial and sensing material. Further modification of Parylene surfaces has been demonstrated, especially for biological/biomedical applications [375–377].

4.5.2 Processing Techniques

Parylene is resistant to removal by solvents below its melting temperature. Only chloronaphthalene or benzoyl benzoate above 150°C are effective [378]. Liftoff is not possible due to the conformal structure obtained during the deposition process.

Physical processes are best for removing Parylene. Plasma processes effectively remove both Parylene N and C; the removal mechanism is discussed in [379, 380]. Plasma etching [335, 346, 358, 377], reactive ion etching [346, 355, 381], reactive ion beam etching [382], high-density plasma etching [383], and Bosch-like switched chemistry etching [346, 384, 385] have all been demonstrated. Oxide and metal masks may redeposit during the etch process and result in rough surfaces or the formation of micrograss [346, 355, 381]. Spin-on glass, nitride, and sputtered *a*-Si are also mediocre masking materials [346, 383]. Photoresist masks are preferred, however, the etch rate is comparable to that of Parylene and thus exhibits low selectivity [346]. SU-8 masks exhibit higher selectivity although its removal after etching was not required in the single study to date [386]. Anisotropic sidewall profiles are possible by using high-density plasma and switched chemistry etching [346, 383–385].

Other methods to remove Parylene include ultraviolet laser ablation [353, 354] and manual removal [352]. Release agents (such as 2% Micro® lab cleaning solution, International Product Corp.) applied to surfaces allows Parylene to be peeled away after deposition. Peeling of Parylene without damage to the film was also demonstrated on Si surfaces having a native oxide layer; immersion in water can facilitate the release [204]. Photoresist sacrificial layers are practical for the release of smaller Parylene structures [361]. As removal can pose fabrication challenges in some applications, alternative patterning methods were investigated. Selective deposition of Parylene is achieved by controlling substrate temperature [387]. This technique exploits the phenomenon that deposition thickness is a function of substrate temperature; heating the substrate (70°C) selectively limits Parylene deposition to cooler regions [388, 389].

Parylene's thermoplastic nature also enables thermal imprint patterning (Ni molds at 250°C) [390]. Micromolding combined with thermocompression bonding has been used to form channels [370, 391]. Other modes of Parylene-to-Parylene and Parylene-to-substrate bonding were also developed [392, 393].

4.5.3 Lessons Learned

Adhesion to most substrates (such as silicon) requires pretreatment with adhesion promotion A-174 (gamma-methacryloxypropyltrimethoxysilane) prior to deposition. However, A-174 is incompatible with common positive photoresists causing dissolution of photoresist patterns during the adhesion promotion process. It is suggested that a short oxygen plasma treatment can promote Parylene-to-Parylene adhesion by roughening the surface [358]. To further improve Parylene-to-Parylene adhesion, especially in wet biomedical applications, thermal annealing was performed (2 days at 200°C in vacuum) [204]. Robust Parylene-to-substrate adhesion was promoted by surface roughening with BrF_3 or XeF_2 gas phase etching [358, 394, 395] of Si or by anchoring Parylene to the substrate by deposition into etched trenches [366, 396–398].

4.5.4 Case Study

Implantable microelectrode arrays and telemetry coils were fabricated using single- and dual-layer Parylene/metal processes to realize an intraocular retinal prosthesis (Fig. 4.26) [204, 205, 399]. Parylene was selected over other polymers for its flexibility, process compatibility, and biocompatibility. Fabricated electrode arrays and coils, however, cannot tolerate accelerated lifetime testing due to water infiltration between the Parylene-to-Parylene interface. Thermal annealing was found to

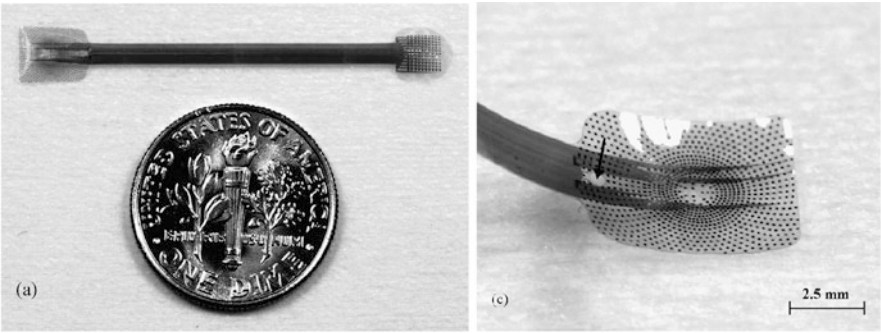


Fig. 4.26 Parylene multielectrode array with biomimetic arrangement of electrodes. The close-up shows an array that has been annealed and heat formed to match the curvature of the retina (Reprinted from [204] with permission from Elsevier, copyright 2006)

improve Parylene-to-Parylene adhesion (200°C, 2 days, vacuum with nitrogen backfill) and provide an extrapolated mean time to failure exceeding 20 years following accelerated lifetime testing [399]. As the interface between the Parylene array and the tissue is curved, thermoforming of the thin-film devices was performed using aluminum molds to impart an anatomically matched curvature to the array portion. In electronic neuroprostheses, it is desirable to fabricate electrodes using materials with high charger delivery capacity. Ir is thus preferred over Pt. However, the high melting temperature of Ir results in cracking of films deposited in Parylene C. In this case, Parylene HT, which has greater thermal stability, was used to successfully fabricate Parylene HT–Ir electrode arrays [204].

4.6 Conductive Polymers

Polymers are usually considered as solely having plastic properties. They are excellent insulators and have been extensively used as coatings to protect electrical wires from short-circuits. However, Alan J. Heeger, Alan G. MacDiarmid, and Hideki Shirakawa changed this view with their discovery of a new class of conducting polymers in 1974 for which they were awarded the Nobel Prize in Chemistry in 2000. Although this class of polymer is in its infancy, their potential applications have significant implications.

Polyacetylene was the first conducting polymer. The key feature of the polymer is that it consists of alternating single and double bonds, called conjugated double bonds along the backbone of the polymer chain [231] (Fig. 4.27). The π-electron in a double bond has less energy and can be delocalized.

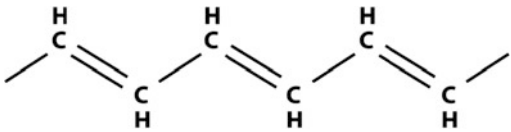


Fig. 4.27 Polyacetylene structure

However, it is not enough to have conjugated double bonds. To become electrically conducting, the polymer has to be disturbed: either by removing electrons from (oxidation), or inserting them into (reduction), the material. The process is known as doping. In the doped state, the polymer can achieve conductivity even comparable to metals, which is an increase of about 13 orders of magnitude compared to common nonconducting polymers [400] (Fig. 4.28).

Although featuring the highest conductivity among other conducting polymers, polyacetylene is not stable, which limits its use. In the next three decades following the development of polyacetylene, a wide range of derivatives were developed, such as polypyrrole, polythiophene, and polyaniline [402] (Fig. 4.29).

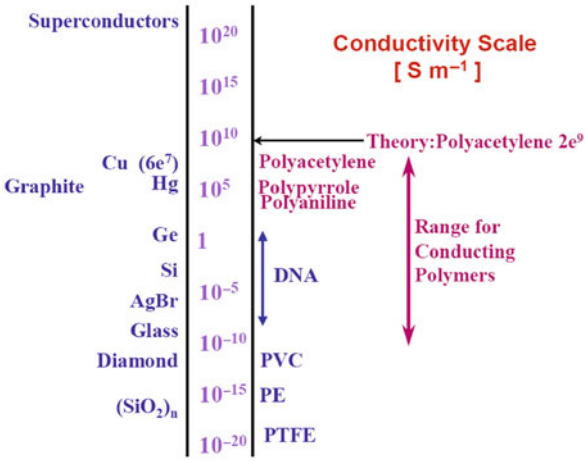


Fig. 4.28 Conductivities of conducting polymers relative to other common polymers and inorganic materials. PE is polyethylene, PVC is polyvinylchloride and PTFE is polytetrafluoroethylene, also known as Teflon©. The upper limits in conductivity for the conducting polymers polyaniline, polypyrrole, and polyacetylene are shown (Reprinted from [401] with permission of, the MIT Technology Licensing Office)

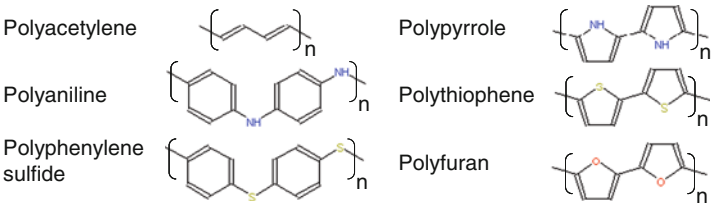


Fig. 4.29 Types of conducting polymers (Reprinted from [402] with permission from ASME)

4.6.1 Material Properties

Some of the properties of conducting polymers can be controlled by changing the redox state. By an electrochemical process, electrons can be added to or removed from the polymer via an electrode, thereby changing the oxidation state. More important, this change is reversible through chemical or electrochemical means. For example, the conductivity can be switched by 13 orders of magnitude, an effect used in organic transistors. Optical absorption, permeability, hydrophobicity, stored charge, and volume all change in a controllable manner. This enables devices such as chemical sensors, filters, capacitors, and batteries [403].

Here, we focus on the actuator applications of conducting polymer, where the volume change relies on the ion and solvent migrations [404–407]. By applying a positive potential, electrons are removed from the polymer via an electrode and the polymer is oxidized. To compensate, oppositely charged ions are incorporated

into the polymer from the supporting electrolyte and thus the volume expands. The polymer can be reversibly reduced to neutral state by applying a more negative potential and allowing the polymer to shrink to the original volume.

Although electrostatic and piezoelectric materials have major technological importance for the direct conversion of electrical energy to mechanical energy in actuators, conducting polymers, as an alternative, could provide a similar function in a manner analogous to natural muscle. Key features include:

1. Large strain (2∼20%)
2. High stress (100 times greater than muscle)
3. Low actuation voltage (∼1 V or less)
4. Can be positioned continuously between minimum and maximum values
5. Can be kept in a fixed position without consuming additional power; consumes current only when switching states
6. Can operate in liquid electrolytes, including body fluids

However, conducting polymer-based actuators have a low actuation rate and low conversion efficiency of electrical energy to mechanical energy. These can be improved through miniaturization (fabrication of conducting polymer-based devices on a smaller scale). Miniaturization could lead to improvements in conductivity and electroactivity [408]. Higher conductivity is important, but reducing resistive loss is the key requirement. One attractive feature of miniaturization is the possibility of having highly ordered and less defective material to contribute to high conductivity. In addition, the efficiency of the electroactive process through a redox cycle can be improved because the surface area to volume ratio is higher, providing a large interface between the electrode and electrolyte. This can increase the rate-limiting ion diffusion process, and reduce the double-layer capacitance and the RC time constant.

4.6.2 Actuation Mechanism and Theories

During the last few decades, researchers have proposed many models to describe the actuation mechanism of conducting polymer actuators. The complex nature of the actuation mechanism involves a large number of electrical, chemical, and mechanical variables, some of which are interrelated. Madden, Madden, and Hunter described the actuation of a free-standing polypyrrole film as a simple elastic mechanical model superimposed with the electrochemically generated strain that is assumed to be directly proportional to the charge density [409]. Della Santa, De Rossi, and Mazzoldi investigated the modeling and characterization of a muscle-like conducting polymer axial/linear actuator operating in an electrolytic cell [410]. Their model utilized simple lumped parameters identified using force and length change data. Based on the beam-bending model, Pei and Inganaes developed a mathematical model for a bilayer strip made of a gold-coated polyethylene layer

and a polypyrrole layer [411]. It was concluded that the actuation consisted of a fast cation insertion for volume expansion and a subsequent slow salt draining process for phase relaxation. Alici et al. developed a mathematical model of a strip-type polypyrrole/PVDF/polypyrrole trilayer actuator operated in air, using a similar beam-bending method [412]. The static characteristics of the actuator were analyzed and verified by experiments, such as the relationship among the input voltage, output deflection, and force.

4.6.3 Applications

4.6.3.1 Actuators

Conducting polymer actuators are commonly fabricated in two forms: linear and bilayer bending actuators. For linear actuators, Hara et al. built a polypyrrole–zigzag metal wire composite linear actuator and showed an enhanced electrochemical strain up to 21.4% [413]. Spinks et al. developed a helix tube polypyrrole linear actuator for a Braille display screen [414]. The bilayer actuator is a simple mechanical amplification structure that can convert a small linear strain into a large bending angle. One of the earliest demonstrations was carried out by Smela et al. with a polypyrrole/gold bilayer actuator to produce an electrically controlled micro finger [415]. This actuator, however, could only be used in a liquid electrolyte.

A further improvement was made by Kaneto et al. to enable the actuator to operate in air [416]. They used an insulating paper soaked with the electrolyte or a solid polymer electrolyte sandwiched between the two conducting polymer layers. This type of actuator has some limitations: either the ionic conductivity in solid polymer electrolyte is very low at room temperature, or the solvent in the solvent-swollen gel, typically water, will evaporate in the long run.

A promising approach to dry actuators has become feasible with the synthesis of new molecules called ionic liquids. These materials are salts that are liquid at room temperature; they typically consist of nitrogen-containing organic cations, such as 1-butyl-3-methyl imidazolium, and inorganic anions (Fig. 4.30) [417]. Furthermore, some ionic liquid relatives are plastic solids at room temperature, yet still maintain a reasonable conductivity, whereas others can be transformed into soft elastomeric solids at room temperature by the addition of small amounts (~5%) of a suitable polymer. These materials have only recently been applied to conducting polymer actuators, but the results are impressive: they show significantly enhanced lifetimes

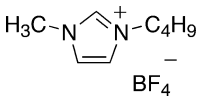


Fig. 4.30 Structure of the ionic liquid BF_4 1-butyl-3-methyl imidazolium (Reprinted from [417] with permission from Wiley-VCH)

compared to other electrolytes, as well as fast switching speeds [418]. The combination of gels with ionic liquids is therefore the next logical step in the effort to develop dry actuators.

4.6.3.2 Conducting Polymer as a Strain Gauge Material

Conducting polymers have also been reported to have a strain-sensitive effect, where the resistance changes as the gauge is stretched. The resistance change is given by:

$$\frac{\Delta R}{R_s} = G\varepsilon,$$

where R_s is the unstrained resistance of the gauge and ϵ is the strain. The factor G is known as the gauge factor of the sensor. A higher gauge factor improves the sensitivity of the strain gauge. Pure polypyrrole has been used to make strain gauges, however, the best conducting polymer strain gauges have been made by coating a flexible fabric with a layer of polypyrrole; the reported gauge factor was around 13 [419].

4.6.4 Processing Techniques

4.6.4.1 Deposition

Depositing thin, uniform polymer films by spin-coating is a widely used technique in microfabrication. This technique can be applied to photoresist, such as Shipley 1818. For metal layers, such as Cr, Au, Ti, an E-beam evaporation or thermal evaporation can be used. E-beam evaporation has a small effect on samples thus making it easier to pattern by etching or a lift-off process; thermal evaporation will raise the sample temperature thus it is not suitable for a lift-off process due to overheating of the photoresist and difficulty stripping the photoresist after evaporation.

There are many ways to deposit conducting polymers. Polyaniline can be made into powder and dissolved or dispersed in an acid solution [420]. Polythiophene can be dissolved in certain types of organic solvent by special treatment such as alkyl substitution on carbon rings [421]. Then they can be spin-cast into films onto many types of substrates. If the polymer is insoluble, such as polypyrrole, the electrochemical deposition technique is a common alternative. This process is conducted in a typical three-electrode electrochemical cell setup, which consists of a working electrode (where the conducting polymer deposits), a counterelectrode, and a reference electrode (providing precise potential control of the synthesis). The electric power can be applied by means of either potentiostatic (constant potential) [405, 422] or galvanostatic (constant current) mode [423].

4.6.4.2 Patterning

There are several ways to pattern conducting polymers. The main methods are listed as follows (Fig. 4.31) [424].

1. Patterning the electrode onto which the conducting polymer is deposited.
2. Using photoresist as a mold to template deposition.
3. Depositing the conducting polymer in the whole layer then etching it.
4. Printing the polymer (this only works with soluble conducting polymers).

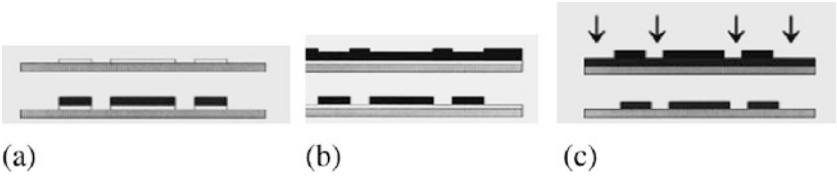


Fig. 4.31 Patterning methods: (**a**) patterned electrodes; (**b**) template deposition; and (**c**) etching (Reprinted from [424] with permission from IOP)

Patterning electrodes is the simplest way because conducting polymer will directly deposit on a substrate with no need of further patterning. The main drawback is the nonuniform film thickness; higher electric fields and reactant availability at the edges of electrodes produce thicker deposits. Also the polymer has finite lateral growth, which may bridge adjacent electrodes or make it harder to release the structure after deposition.

The second method is template deposition, using photoresist as a mold. The conducting polymer will only deposit in the opening windows, and photoresist can be subsequently removed with acetone or ethanol. This method can eliminate the lateral growth in patterned electrodes to benefit the structure release.

Conducting polymers can also be patterned by removal of unwanted material by reactive ion etching (RIE). First, the polymer is deposited on the entire surface and then the photoresist is patterned to form an etch mask. Finally, RIE is applied (usually oxygen plasma). Because oxygen will etch both the photoresist and conducting polymer, the etching process should be carefully monitored. Christophersen et al. reported that the oxygen plasma etch selectivity (ratio of etch rates) between polypyrrole and the masking 2 μm thick photoresist was 2.5:1 [425]. However, our experiments (40 sccm O_2 flow rate, 100 mtorr pressure, 300 W power) demonstrated an S1818 etch rate of 0.18 μm/min, whereas that of polypyrrole was 0.20 μm/min. Thus, this method limits the conducting polymer thickness to be less than the photoresist thickness.

4.6.4.3 Release

Microactuators require a method to partially release them from the substrate. As shown in Fig. 4.32 [424], a sacrificial layer is commonly used. But for this method,

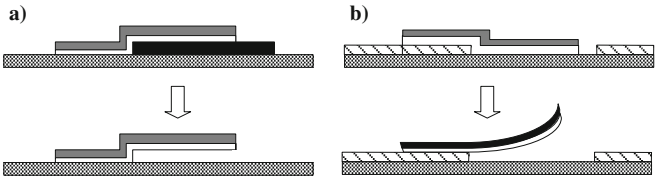


Fig. 4.32 Release methods: (**a**) sacrificial layer and (**b**) differential adhesion (Reprinted from [424] with permission from IOP)

the overhang should not be very large to avoid anchor failure during actuation. Also, the undercut release of large areas requires long etch times.

The second method uses differential adhesion. It is well known that gold adheres weakly to bare silicon, silicon dioxide, and glass. Therefore a thin layer of metal such as chromium is normally deposited first as an adhesion-promoting layer. By patterning the adhesion layer only at the anchor parts, the structure on the bare silicon can be released with the stress generated by the activated conducting polymer layer.

4.6.4.4 Process Considerations

Although there is great flexibility in fabrication techniques, conducting polymers are nevertheless sensitive to some chemicals. Therefore care must be taken to devise an appropriate process. Table 4.4 summarizes some chemical compatibilities and processes [424].

Table 4.4 Processing hazards

Damaging	Use care, test first	Harmless
Cr etchant	Acids	Au etchant
High temperatures		Hot plate at 100°C
Developer (KOH), bases	Solvents	Photoresist
Resist stripper/remover		UV light in mask aligner

Reprinted from [424] with permission from IOP

4.6.5 Case Study

In this case study, we design two structures with detailed processes based on the aforementioned fabrication techniques (Fig. 4.33). The conducting polymer we use is dodecylbenzene sulfonate (DBS^-)-doped polypyrrole. The synthesis is conducted in 0.1 M pyrrole monomer (Sigma Aldrich) and 0.1 M NaDBS (Sigma Aldrich) aqueous solution, by applying a constant potential of 0.5 V versus Ag/AgCl reference electrode.

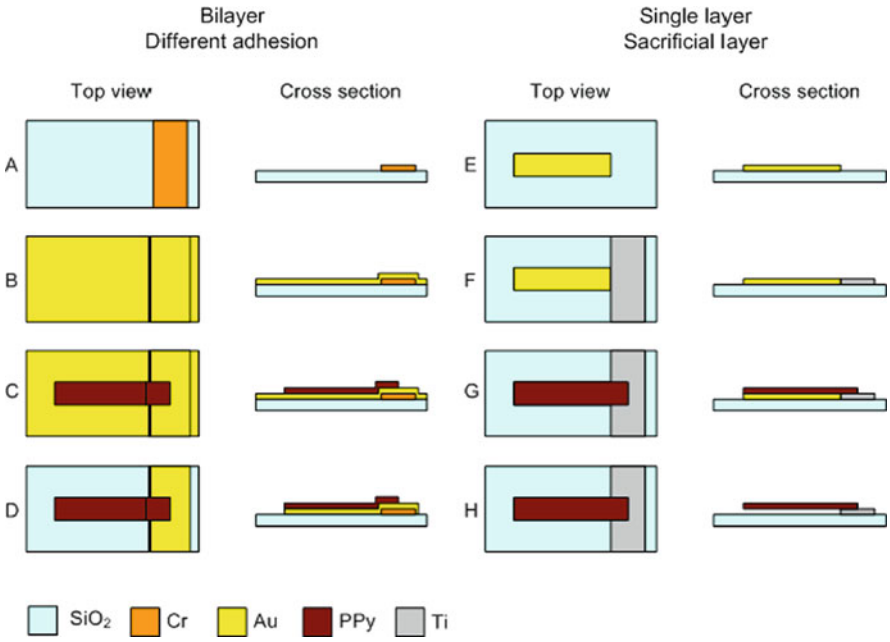
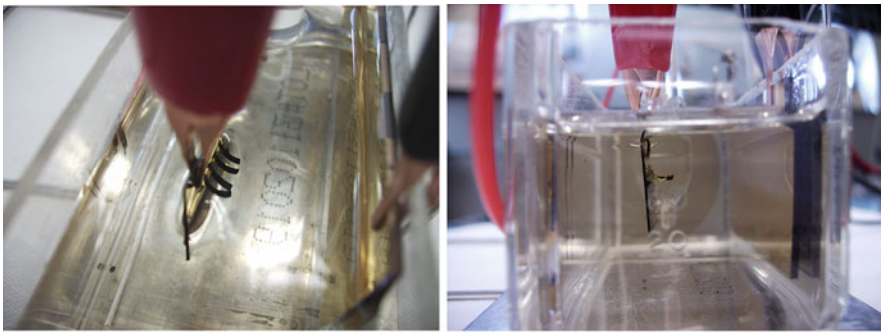


Fig. 4.33 Process flow for bilayer structure using differential adhesion method and single-layer structure using sacrificial layer method. (**a**) Deposition and patterning adhesion layer Cr (10–30 nm). (**b**) Deposition structure layer Au (100 nm). (**c**) Electrodeposition and patterning of PPy (1 μm). (**d**) Etching of the final microactuator structure by removal of the excess Au. (**e**) Deposition and patterning the sacrificial layer Au (100 nm). (**f**) Deposition and patterning the anchor layer Ti (100 nm). (**g**) Electrodeposition and patterning of the PPy (1 μm). (**h**) Etching of the final microactuator structure and underetching Au (Reprinted from [402] with permission from ASME)

The bilayer cantilever, similar to Jager et al. [422], was fabricated using the differential adhesion method. The anchor part consisted of Cr and Au, and the moving part was Au on top of glass. In our experiment, we first used the patterned electrode method to fabricate the structure on a glass slide (1 × 3 in.), but the Au part without the Cr underneath could not be released after deposition. This could be due to the lateral growth of the polymer which extends and adheres to the substrate; also the rougher glass surface could result in higher adhesion to the Au layer.

Then we switched to the photoresist template method and used polished silicon wafer as the substrate. To ensure wafer cleanliness prior to depositing the Au layer, we added a special cleaning process: piranha solution immersion (hydrogen peroxide and sulfuric acid with a volume ratio of 1:3) for 10 min. The final structure could be released immediately after final etching of Au (Fig. 4.34).

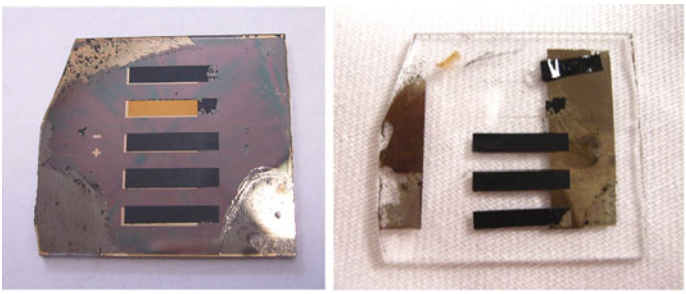
The single-layer cantilever was fabricated using the sacrificial layer method. Because the Ti etchant (Transene), which is typically hydrochloric acid, will attack Cr as well, the undercut etching of Ti will cause the whole structure to peel off from the substrate. Therefore, we used Au as the sacrificial layer and Ti as the anchor.



(a) (b)

Fig. 4.34 Bilayer structure (0.5 × 0.1 cm): (**a**) top view; (**b**) side view (Reprinted from [402] with permission from ASME)

During the synthesis, polypyrrole was first deposited on the Au layer and extended to the Ti layer after sufficient time. When the deposition was complete, the underlying Au was etched to release the cantilever, leaving only polypyrrole as the moving part (Fig. 4.35). This structure may function as a linear actuator.



(a) (b)

Fig. 4.35 Single-layer cantilever (1 × 0.2 cm): (**a**) before etching and (**b**) after etching and release (Reprinted from [402] with permission from ASME)

4.7 Other Polymers

4.7.1 Benzocyclobutene

Benzocyclobutene, or BCB, is a cross-linked aromatic polymer available in two spin-on formats: photosensitive and dry-etch (Cyclotene, Dow Chemical Company, Midland, MI). This thermoset polymer is formed from 1, 3-divinyl-1, 1, 3, 3-tetramethyldisiloxane-bisbenzocyclobutene (DVS-bis-BCB) monomer (Fig. 4.36)

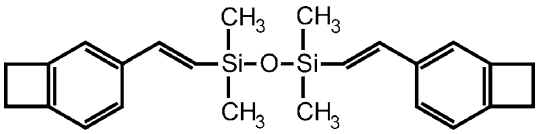


Fig. 4.36 Chemical structure of Cyclotene monomer (After [429])

[426, 427]. The dry-etch formulation consists of partially cross-linked monomer dissolved in mesitylene solvent whereas the photosensitive formulation contains an additional photosensitizer (for broadband UV sensitivity) [428].

BCB is well known as an microelectronics material (with application, e.g., as an interlevel dielectric, passivation coating, and packaging material) [430–434] and was later demonstrated as a suitable planarization material MEMS processes and packaging [435, 436]. The mechanical [437, 438], optical [439], and electrical [428] properties of BCB were characterized. Its combination of properties has led to its use as a power MEMS material for the fabrication of electrostatic micromotors [440–442]. The low moisture uptake and low dielectric constant have attracted biomedical applications [443], however BCB's biocompatibility is not fully characterized (Fig. 4.37).

The standard process features for dry-etch BCB are summarized in Table 4.5. BCB is removed by plasma processes (~0.6 μm/min in oxygen plasma) [429]. Control of the sidewall angle (vertical and sloped) was obtained by varying the process parameters in a reactive ion etching system (O_2 plasma) (Fig. 4.38) [435]. Au protects BCB during anisotropic etching of Si (in KOH) and Cr is used as an intermediate adhesion promotion layer (Fig. 4.39) [429].

Table 4.5 Standard process features for dry-etch BCB (cyclotene)

Process	Method	Details
Surface treatment	Adhesion promoter	AP3000
Deposition	Spin-coat	1–5 krpm
Soft cure	Furnace	N_2, 1 h @ 210°C
Hard cure	Furnace	N_2, 1 h @ 250°C
Etching	Plasma	O_2/CF_4 or O_2/SF_6

After [428]

Although BCB has superior planarization performance compared to polyimide, its CTE mismatch with silicon (~60 ppm/°C [432, 444] versus 2.3 ppm/°C [445]) leads to undesirable cracking. Sandwiches of polyimide–BCB–polyimide harness both the planarization capability of BCB and the mechanical/chemical strength of polyimide [435]. The mechanical robustness of BCB enables its use in chemical mechanical polishing processes as a replacement for silicon dioxide, unlike other softer polymers [446].

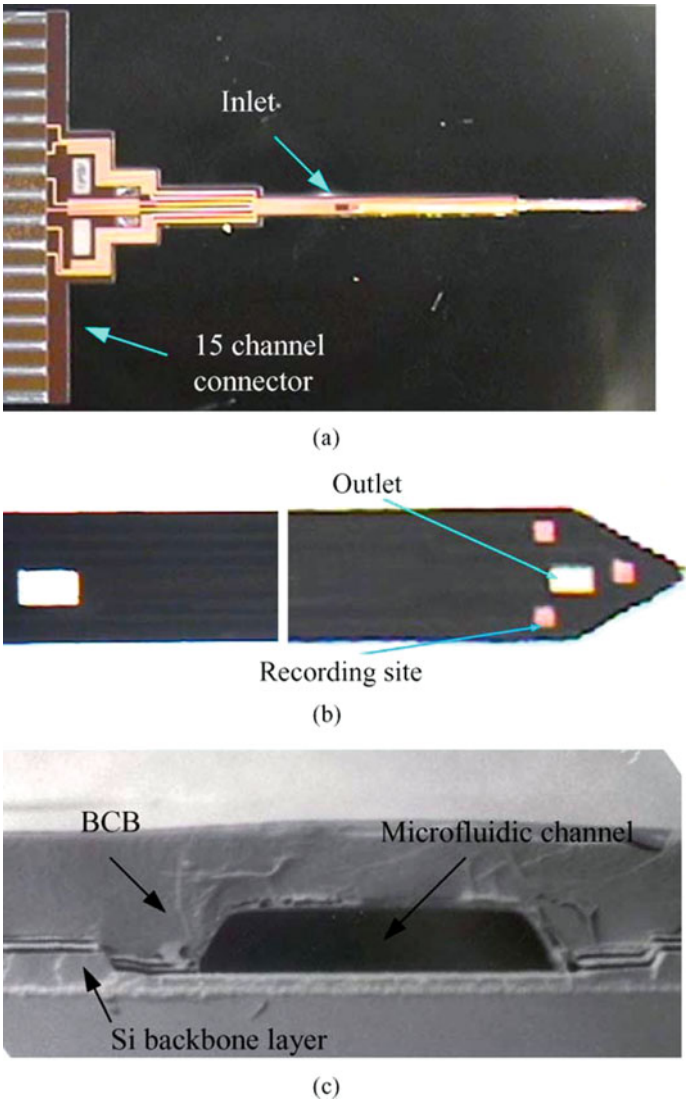


Fig. 4.37 BCB-based neural probes (three recording sites) with integrated fluidic delivery channels (40 μm × 10 μm) (Cyclotene 4026) (Reprinted from [443] with permission from Elsevier, copyright 2004)

In general, BCB exhibits poor adhesion to inorganic materials [447]. AP3000 (Dow Chemical Company) adhesion promoter enhances metal adhesion to BCB; the detailed process and a thorough review on strategies to promote BCB adhesion are given in [429]. Wafer-level packaging utilizing BCB membrane transfer bonding was demonstrated for RF devices (950 mbar pressure, 2 bar force, 250°C; ~70% yield) [448].

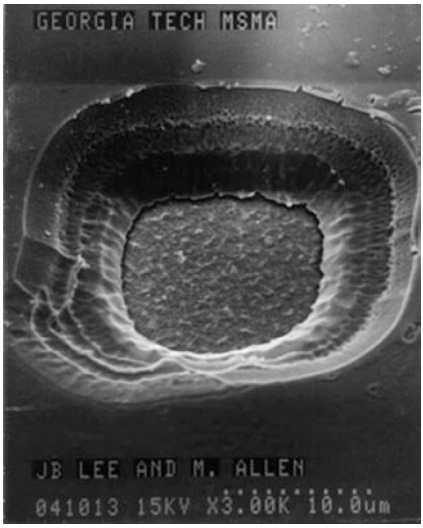


Fig. 4.38 Sloped sidewalls in a polyimide–BCB–polyimide sandwich obtained by reactive ion etching (Cyclotene 3022). Original figure from [435] used with permission of Institute of Physics Publishing Ltd

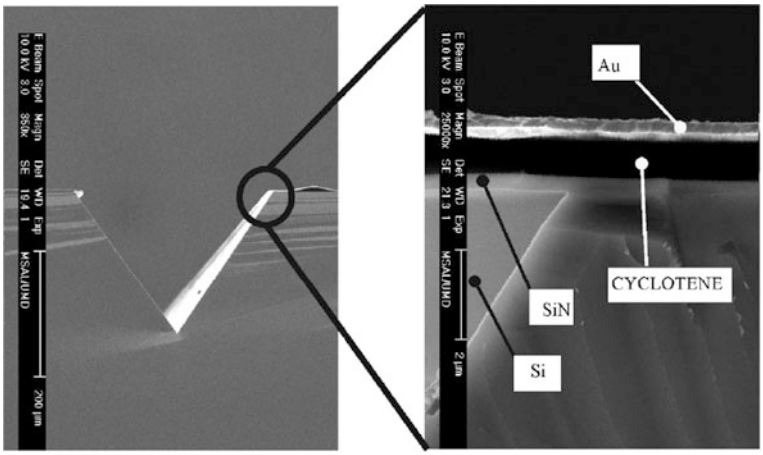


Fig. 4.39 BCB protected by Au mask for KOH etching of an underlying Si trench. Reprinted with permission from [429], copyright 2004, AVS: Science & Technology Society

4.7.2 Liquid Crystal Polymer

Liquid crystal polymers (LCP) possess a unique combination of properties exploited heavily in optical devices, especially consumer displays [449]. For example, they are birefringent and possess dielectric anisotropy. The latter property results in electric field-induced molecular alignment. Later, LCPs were investigated as a packaging material and printed circuit board (PCB) substrate [450, 451]. In the liquid phase, LCPs are isotropic. They may enter one or more liquid crystal phases that exhibit

order and symmetry. There are two mechanisms by which the material changes from the liquid to the liquid crystal phase; LCPs are either (1) thermotropic with thermally driven transitions or (2) lyotropic in which the polymer can self-assemble in response to solvent concentration [449]. We focus on thermotropic LCPs here which are available commercially in thin sheet/film format (either single- or multilayer).

This thermoplastic polymer contains a network of interlinked rigid and flexible monomers, the alignment of which can be tuned by application of shear flow when heated and maintained following cooling [452]. LCPs are excellent moisture and vapor barriers and chemically resistant over a broad temperature range [451]. The chemical compatibility is investigated for various acids, bases, and solvents in [452] and has enabled exploration of LCPs as substrates for supporting underwater and marine sensors [453]. Flow, tactile, and pressure sensors have also been demonstrated for use in dry environments [452, 454].

LCP films may be processed using standard microfabrication techniques. Prior to lithography, it is necessary to apply a rigid supporting substrate [452]. Removal of LCP is achieved by laser machining [455–457] or oxygen plasma etching. An Al mask was using in oxygen plasma reaction ion etching to remove LCP film (Vectra A-950) at a rate of ~0.22–0.27 μm/min (350 W, 500 mT). Films can also be patterned by mechanical punching [454]. LCP films can be bonded by thermal lamination (260–270°C) [452] or thermocompression bonding (400 lb load on a hydraulic press at 275°C, 30 min) [454].

4.8 Polymers for Embossing and Molding

4.8.1 Technical Overview

Hot embossing is the process whereby a pattern is impressed in a material that has been softened by the application of heat. The materials most commonly embossed for MEMS applications are thermoplastics, which are plastics that soften when heated, eventually melt, and solidify again when cooled. This approach is not limited to plastics; more exotic materials such as chalcogenide glasses are embossed to make lenses and waveguides, and microscale features have been embossed in bulk metallic glasses [458]. Hot embossing is typically used in conjunction with injection molding as a process to make mold inserts. Many of the polymers described in this section are not only used in hot embossing but also in complementary polymer fabrication techniques such as injection molding and compression molding. These complementary molding processes are briefly summarized here; for further information on specific mold-making processes, the reader is directed to the references [459–462].

Injection molding is appropriate for both thermoplastics and thermosets. Unlike thermoplastic materials, thermosetting plastics do not soften when heated. Instead, they are only workable prior to being cured. The curing process produces irreversible cross-links that impart strength to the final material. Polymers are formed

by injecting by force a liquid polymer into a structured mold cavity. The final polymer part takes on the shape of the mold cavity. Overall, this versatile process lends itself to the production of polymer parts having complex shapes and in high volume. Specialized equipment is required to perform the polymer injection and subsequent molding process.

Compression molding shares similarities with injection molding in that a polymer is forced against a mold cavity in order to take on its shape. Here, polymer granules are placed into a mold and forced against it, typically using a combination of heat and pressure (usually with a hydraulic ram). This simple process is low cost and does not require expensive tooling. However, compression molding is not suitable for forming plastics into complex shapes as in injection molding but instead is used for predominantly flat or moderately curved parts. A variety of polymers may be used, however, compression molding is usually performed on thermosets.

The basic process parameters of hot embossing are temperature, time, and force. The substrate is heated until it begins to soften (step A in Fig. 4.40). Ideally when embossing is initiated the material is pliable, but not yet bordering on becoming liquid. The softening point or glass transition temperature (T_g) is the temperature when the amorphous component of the material is transitioning between its glassy (brittle) and rubbery (pliable) states. The magnitude of the effect is dependent on the ratio of amorphous and crystalline components of the material. The ideal embossing temperature is not only dependent on the material being embossed, but also mold features. Different feature and substrate geometries will pattern more accurately with different polymer viscosities. If the material is too viscous it may adhere to the mold and make demolding difficult. This is a primary mode of mold wear.

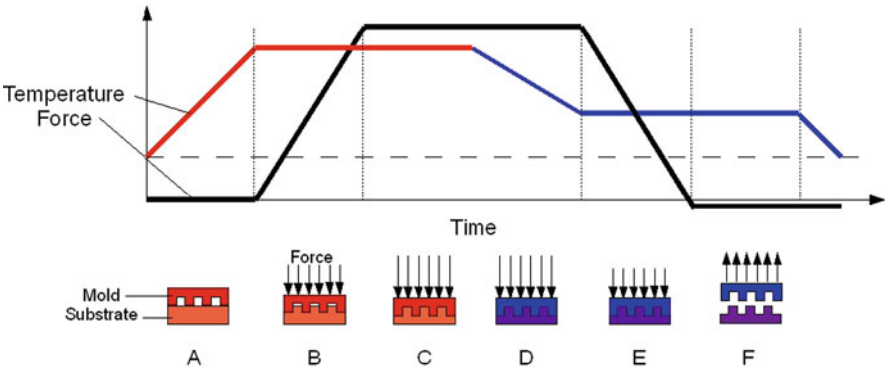


Fig. 4.40 Process profile time, temperature, and force

Force is applied to force between the mold and plastic (Fig. 4.40, step B). The force is maintained for the "embossing hold time" to allow the plastic adequate time to flow into the mold (Fig. 4.40, step C). Once the mold has been impressed in the plastic to the desired depth, both the mold and plastic are cooled below the glass transition temperature (Fig. 4.40, step D) to increase the rigidity of the newly created features such that they will maintain their shape during the demolding process

(Fig. 4.40, step F). Some shrinkage of the new features relative to the mold can assist demolding. Careful selection of temperature ramp rates and good uniformity control help minimize stress in the final part.

The force ramp times (Fig. 4.40, steps B and E) are relatively short, so the time to emboss is dominated by the temperature ramp times and the hold time. The ramp times are determined by the thermal mass of the tooling, the heaters and chillers available, and the controllers. Ideally the ramp times are short, the main constraints being reproducible performance while maintaining temperature uniformity between mold and material being molded. The ideal emboss hold time is usually considered to be the minimum time necessary for the plastic to flow and fill the mold as desired. Additional time may be necessary to buffer for variability, but excessive hold times can result in excellent bonding of the substrate to the mold.

The force required for embossing is determined by the mold flow resistance and viscosity of the material being molded. The mold flow resistance is a function of the amount of area to be pressed into the substrate, as well as the size of features in the mold that need to be filled. For instance, a mold used to fabricate narrow pillars of plastic will require more force than one used to fabricate narrow holes. A good indicator of high flow resistance is if not only the area pressed into the substrate is high, but also the length of the perimeter that encompasses that area is also high.

It is useful to evacuate the embossing chamber to reduce problems associated with air trapped between the mold and substrate; however, the vacuum levels necessary are not very difficult to achieve (on the order of 1 mT).

The primary components of embossing are: the substrate embossed, the embossing machine, and the mold insert or tool.

4.8.2 Substrate Material Selection

The selection of material to be embossed will be driven by the requirements of the device to be fabricated. Material properties commonly of interest are: mechanical strength and durability, optical transmission, fluorescence, water uptake, chemical resistance, electrical properties, and UV stability. If multiple candidate materials are suitable for the device, ease of fabrication and material cost may also factor in.

Fabrication cost is driven primarily by tool time. Because the tool time required per part is dominated by the heating and cooling times, the selection of a material with lower T_g will cost less to emboss. A material that is easy to emboss can improve mold lifetime and thus reduce cost.

4.8.2.1 Polymethylmethacrylate

Polymethylmethacrylate (PMMA) is relatively easy to emboss. It has good flow properties, with a relatively low T_g. The mechanical properties at room temperature are suitable for a wide variety of applications; however, the material is brittle and may crack if subject to impact. It has good UV resistance, and as such is commonly used in outdoor applications. Chemical resistance is not especially good; it is

attacked by most solvents and does not hold up well to strong bases, but it is widely used in microfluidic devices due to its low fluorescence over a broad spectrum.

4.8.2.2 Polycarbonate

Polycarbonate (PC) has excellent mechanical properties, as is demonstrated by the fact that it is widely used as bulletproof glass. These properties translate to devices fabricated on the microscale, with very high strains displayed before failure. It also has a relatively high T_g and heat deflection temperature, and thus is mechanically stable to higher temperatures than PMMA. It displays poor resistance to most solvents, and absorbs water (0.25–0.35%). Polycarbonate fluoresces (excitation wavelength 250 nm) which limits its compatibility with many biological assays.

4.8.2.3 Polytetrafluoroethylene

Polytetrafluoroethylene (PTFE) is of interest for applications where excellent chemical resistance is required. It is a semicrystalline thermoplastic, so even though the T_g is quite low (in many cases below the operational temperature), the embossing temperature will need to be much higher, closer to the melting temperature. PTFE has several potentially useful physical properties including low friction, low adhesion, hydrophobicity, is an excellent dielectric, and displays no fluorescence (although it may fluoresce as a result of radiation-induced breakdown). It displays high creep and is expensive.

4.8.2.4 Cyclic Olefin Copolymer

Cyclic olefin copolymer (COC) materials are widely used in optical devices inasmuch as they have very stable optical properties and display low fluorescence. They also have low moisture uptake (<0.01%), and consequently are popular for use in microfluidic devices, especially ones deploying optical interrogation. They have decent chemical resistance, and are compatible with alcohols and some acids. These materials display glass transition temperatures in the range of 110–150°C. The mechanical properties are reasonable, but adjusting composition to increase Young's modulus also increases brittleness.

An important consideration in material selection is the source. Depending on the process used to produce the embossed stock, the material may have internal stress, which can manifest during embossing. Also, if the material properties drift from lot to lot, so will the embossing results.

4.8.3 Tool Selection

There are several commercial tools on the market for hot embossing on the micro- and nanoscale, and many researchers have produced good results on homemade

tools. Unsurprisingly, the ideal setup is very application-dependent. Here are some basic considerations for tool selection.

1. Temperature range: determines materials the tool can emboss.
2. Force range: high force capability increases the area that can be embossed, as well as the range of acceptable mold flow resistances.
3. Fixture: for both mold and substrates; easy substitution will improve throughput.
4. Alignment capability: alignment of mold to a patterned substrate, or alignment of a lower second mold for double-sided embossing; in a tool, or external with jig transfer into a tool.
5. Heating and cooling rates, uniformity, and control stability: determines throughput and repeatability.
6. Mechanical precision: micro- versus nanoscale optimized.
7. Demolding mechanism.
8. Software: ease of process development, tracking and debugging.

Several of the tools are modified bonders, thus it may be worth considering this alternate functionality when selecting a tool. Typically this means that alignment is performed on separate platform.

4.8.4 Mold Material Selection and Fabrication

A wide variety of materials and methods can be used to fabricate molds. Primary considerations for material selection are cost, fabrication complexity (and hence turnaround time), and desired lifetime. The fabrication approach is determined by the features to be embossed, and the material preference. Here we cover some of the more common approaches for fabricating molds for embossing micro- and nanoscale features.

4.8.4.1 Silicon

Silicon is not an ideal mold material, inasmuch as for many applications it does not display good wear properties. Because it is crystalline, it is prone to fracturing and chipping. It also has a much lower thermal coefficient of expansion than some of the more ductile metals used in tool mounting hardware (i.e., steel, stainless steel, and bronze), which can complicate the fixture. However, if the embossing process itself is not especially mechanically challenging for the mold, silicon can be an excellent choice.

It is very widely used in prototyping applications due to the widely available and mature set of processes for machining, especially on the micro- and nanoscales. The maturity of silicon processing means that advanced mold pattern geometries can often be achieved in a relatively straightforward manner, with reasonable cost. Good turnaround times allow multiple design and fabrication iterations to take place in a short period of time.

The most common method of etching silicon for making molds over 4 μm deep is the Bosch process used in a deep reactive ion etching (DRIE) tool. This process is cyclic, consisting of a brief etch step followed by sidewall passivation. This cyclic process produces the characteristic sidewall texture shown in the image in Fig. 4.41. By shortening the cycles, the sidewall becomes smoother. Smoother sidewalls are normally desirable because roughness will in most cases be accurately replicated in the plastic during embossing, and can promote adhesion between the plastic and mold, making demolding more difficult. The roughness of silicon sidewalls can be reduced by repeated oxidation and strip cycles, but better options include using cryoetching and neutral loop discharge (NLD) etching instead of the Bosch process. Most dry deep silicon etch processes can be tweaked to adjust the sidewall angle. A slight taper simplifies demolding.

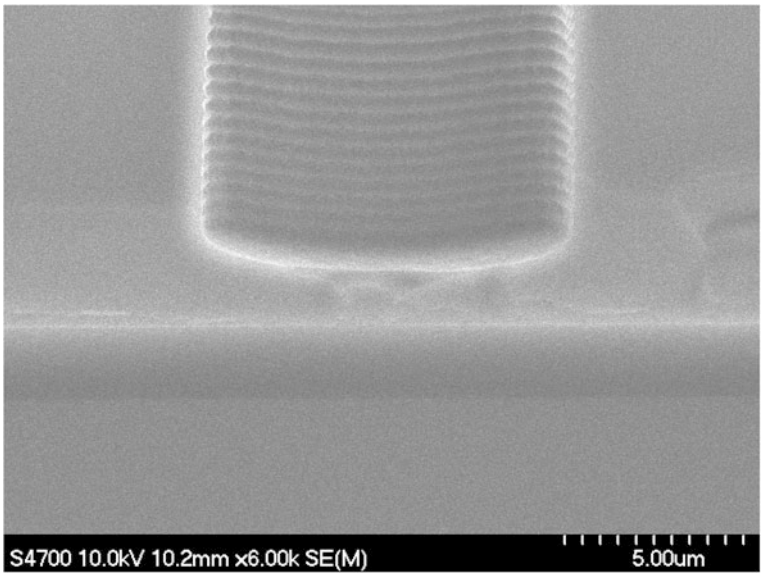


Fig. 4.41 SEM image of silicon mold sidewall etched by Bosch process DRIE

Shallow features can be etched in silicon using conventional RIE processes to produce smooth sidewalls. The geometries produced by wet anisotropic silicon etchants (such as KOH, TMAH, and EDP) are relatively easy to emboss.

4.8.4.2 Nickel

Nickel is probably the most widely used mold material for large volume applications because it displays excellent wear properties. It is also the first choice for aggressive features and embossing processes due to its high strength and toughness. Nickel can be machined using conventional milling processes, but for micro- and nanoscale

features, it is most commonly electroplated into a mold that determines the final geometry. The mold is subsequently removed.

X-ray LIGA (German acronym for *Lithographie, Galvanoformung, Abformung*, i.e., "lithography, electroplating, and molding") is the pre-eminent method for fabricating very-high-aspect-ratio nickel molds. The use of X-ray lithography to define the mold into which the nickel is electroplated, allows the definition of extremely high-aspect-ratio features with extremely smooth sidewalls (<100 nm sidewall roughness). The substrate can be scanned and tilted during the X-ray exposure to make the mold taper. This taper is transferred to the nickel during electroplating, which aids demolding. Other LIGA variations exist, including UV-LIGA in which the mold is fabricated using conventional lithography. Molds can be fabricated from materials other than photoresist, such as silicon or fused silica. It is common to take a conventional part to be duplicated in plastic and use it as the mold for electroplating. Note that this process is not straightforward if the aspect ratio of recessed areas on the plated part exceeds 1:1. See Fig. 4.42.

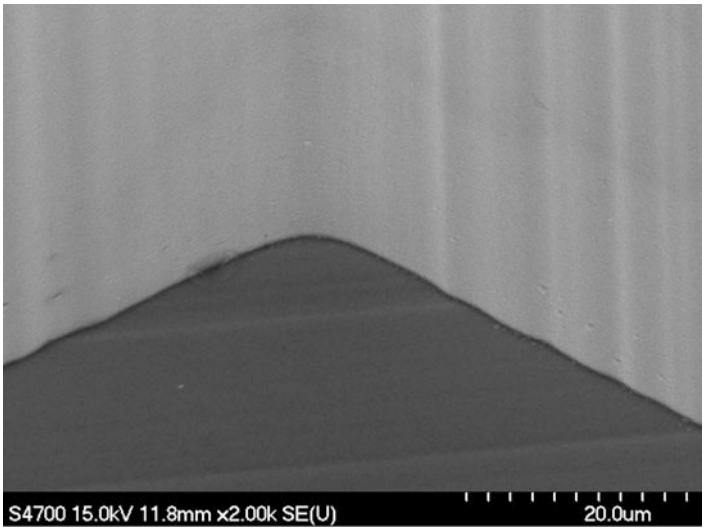


Fig. 4.42 SEM image of LIGA mold sidewall demonstrating extremely low roughness

4.8.4.3 SU-8

SU-8 is a high-contrast epoxy negative photoresist that can be coated and patterned in very thick layers. Once the material is fully cross-linked it displays excellent mechanical properties, chemical resistance, and thermal stability ($T_g = 200°C$, SU-8 3000 series [463]). Consequently, it can be a relatively rapid method of producing mold inserts. The wear properties of SU-8 are not ideal for embossing of challenging features, but for moderate features in low volumes, it can be cost effective and suitable for rapid prototyping. Grayscale lithography has been demonstrated with

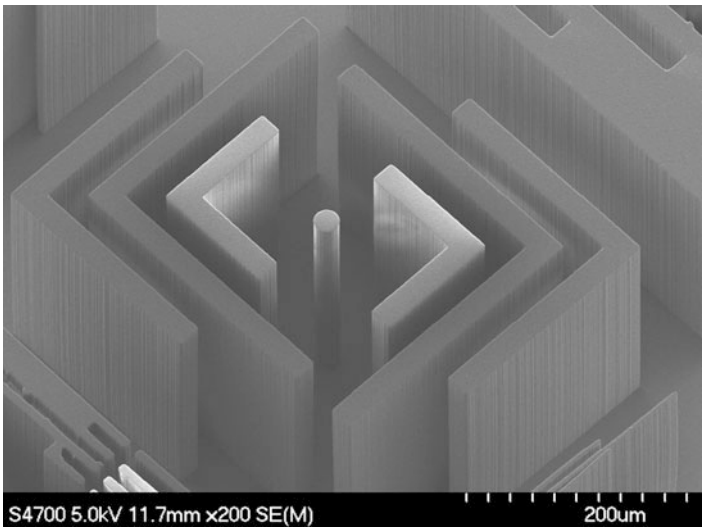


Fig. 4.43 High-aspect-ratio SU-8 features

SU-8 to fabricate 3-D microstructures [464]. A concern with the use of SU-8 mold inserts for aggressive processes is that the adhesion of the features to the substrates may be insufficient, and may deteriorate with use. See Fig. 4.43.

4.8.5 Conventional Machining of Molds

Inasmuch as the focus of this work is on micro- and nanotechnologies, we have focused on micro- and nanomachined mold inserts. Hot embossing is not a new technology; however, it has only recently become widely used on the micro- and nanoscales. Consequently there is a long history of molds fabricated using conventional machining. Conventional machining has also evolved to be able to produce a wide variety of features on the micron scale.

4.8.5.1 Milling

High-precision CNC tools can mill parts using very small diameter bits. Although the diameters of the bits might be too big to machine channels that would be considered small enough to fall into the MEMS realm, they can remove material from either side of a wall to make it narrow enough to be considered MEMS scale. This "wall" feature will form a MEMS scale channel when embossed into plastic. Inasmuch as the pattern is created one feature at a time, the cost is proportional to the size, number of features, and complexity of the mold.

4.8.5.2 Laser

Recent advances in laser and chemically assisted laser micromachining have expanded the potential application for mold insert fabrication. Historically, feature roughness has been a concern, but this is not the impediment it used to be.

4.8.5.3 Focused Ion Beam

Focused ion beam (FIB) tools have been used to structure substrates, which have been subsequently used as molds. This is a beam-based etch, therefore complex 3-D geometries can be fabricated. It also means that the cost scales linearly with the amount of material to be removed. Fine features require a finer beam, which will cost more per unit volume of material removed. This approach can provide very rapid turnaround of very small-scale features, but the cost is high.

4.8.5.4 Fixture of Molds

The effort and expense justified for the mold fixture will depend on the parameters of the process to be run, as well as the number of parts to be run. The format for the mold and the substrate will be dictated to a large degree by the embossing tool to be used; it requires due consideration when preparing to emboss. In most cases some machining will be required beyond the creation of the mold pattern in order to emboss and subsequently demold.

4.8.5.5 Release Coatings

The use of mold release agents is relatively mature in injection molding, and has direct relevance to microscale hot embossing. The mold release agent reduces or prevents adhesion between the mold and the material being embossed. This is advantageous as it reduces wear on the mold, and also reduces the possibility of fouling the mold with fragments of the embossed material.

The direct application of an off-the-shelf release agent risks distorting microscale geometries due to the granularity of the material, either forming a texture, or droplets. A custom formulation, application, or dilution may be required. It is also common to deposit a thin CVD layer of PTFE or a PTFE-like material. It is essential that the surface be very clean prior to deposition to improve adhesion of the deposited layer to the mold.

4.8.6 Process Development

There are two common philosophies for process development, both of which are predicated on the assumption that the material to be embossed is inexpensive relative

to the mold. The first approach seeks to protect the mold from mechanical damage by ensuring that the embossed material is compliant, and the force is low.

For the first-time embosser, the suggested starting temperature is in the range of 10–20°C above the material T_g. Low force and short flow time should be used. What is considered "low force" is very geometry-specific; it depends on the area of the mold and the size and flow resistance of the features, as well as the depth of the features. When in doubt start as low as in the 2–5 kN range (for low-aspect-ratio nanoscale features, this range may even be considered high). Note that molds made from standard <100> silicon substrates 100 mm in diameter and 500 μm thick are prone to crack when the force exceeds 8 kN. By keeping the flow time short, excessive substrate flow is less likely. If the mold is not filling with the substrate material, consider increasing the mold fill time before increasing the force.

The initial demold temperature should be high (i.e., 5–10°C below T_g), so that the substrate is still somewhat compliable. The demold temperature can be reduced until no evidence of feature stretching or "drawing" is evident (as can be observed in Fig. 4.44).

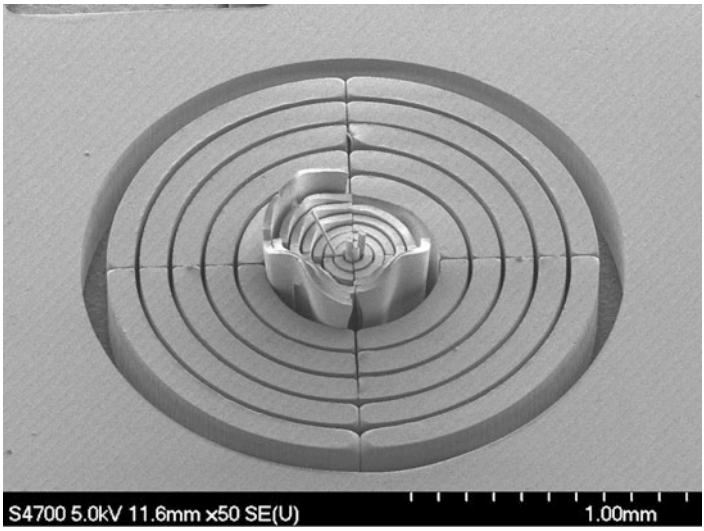


Fig. 4.44 Plastic "drawn" by the demolding step. Note that features with high perimeter-to-cross-sectional area are the worst affected

The second approach seeks to protect the mold from being "fouled" by the substrate material breaking free and staying embedded in the mold. In this case, it is better to start with low force and low temperature. This will result in the high points of the mold bearing the embossing force with little accommodation by the substrate, so it is important that the mold not have isolated high points that can be damaged. The temperature and force should be increased together until some mold fill is observed, then the focus should be on force to get good mold fill.

Fig. 4.45 Bubbles beginning to form due to high emboss temperature

The formation of bubbles in the embossed plastic (Fig. 4.45) is an indicator that the embossing temperature is high.

4.8.7 Minimum Substrate Thickness

The substrate molded has to be sufficiently rigid that the embossed features are well enough attached to the substrate that they do not adhere better to the mold and either stretch or tear free. The material needs to be mechanically sound and either thick (i.e., thick enough to be rigid with respect to the fixture and the demolding force), or bonded with good adhesion to a rigid handle layer. Similarly, it is important to make sure that the protective films often applied to plastics are removed prior to embossing because in many cases they will bond to the mold and can be very difficult to remove.

Another consideration for embossing thin plastics is the issue of flow resistance. Essentially the embossed layer is a flow channel, which can be described by Poiseuille's law:

$$R = \frac{12vl}{wh^3},$$

where: R = flow resistance, v = viscosity, l = length, w = width and h = height.

As the height of the flow channel (layer thickness) is reduced, the flow resistance increases as a function of the height cubed, so thin layers require excessive force to achieve reasonable material flow.

4.9 Materials Properties

Table 4.6 includes material properties presented in tabular format for some of the polymers discussed in this chapter. Additional property tables are found in the preceding text.

Table 4.6 Some material properties for select polymers

Property	Parylene C [465]	Polyimide [466]	SU-8	LCP (Vectra A-950) [452]	BCB (Cyclotene) [428]
Young's modulus (GPa)	2.8	1.8–8.5	0.7–5.9 [6, 22, 23, 48, 50, 63, 66, 73, 115, 467–471]		
Tensile strength (MPa)	69	100–350	15–120 [22, 23, 73, 471]	30 kpsi	85–87
Yield strength (MPa)	55 MPa				
Poisson's ratio			0.26–0.33 [22, 472]		0.34
Elongation (%)	200	10–120	1.8–24 [22, 23]		8
Cure temperature (°C)		250–375			
Melting point (°C)	290			280	
Glass transition temperature (°C)		235–400	50–240 [2, 5, 20, 22, 23, 110]		> 350
Linear coefficient of expansion	3.5×10^{-5}/°C	3–70 ppm/K	52–452 ppm/K [22, 53]	0–30 ppm/K	52 ppm/K

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References

1. J.D. Gelorme, R.J. Cox, S.A.R. Gutierrez: Photoresist composition and printed circuit boards and packages made therewith, Patent No. 4882245 (Nov. 21, 1989)
2. K.Y. Lee, N. LaBianca, S.A. Rishton et al.: Micromachining applications of a high resolution ultrathick photoresist, J. Vac. Sci. Technol. B 13, 3012–3016 (1995)

3. M. Despont, H. Lorenz, N. Fahrni et al.: High-aspect-ratio, ultrathick, negative-tone near-uv photoresist for MEMS applications. Proceedings of the IEEE Microelectromechanical Systems Conference, Nagoya, Japan, pp. 518–522 (1997)
4. J.M. Shaw, J.D. Gelorme, N.C. Labianca et al.: Negative photoresists for optical lithography, IBM J. Res. Dev. 41, 81–94 (1997)
5. N.C. LaBianca, J.D. Gelorme: High-aspect-ratio resist for thick-film applications. Proceedings of SPIE – The International Society for Optical Engineering, Santa Clara, CA, USA, pp. 846–852 (1995)
6. H. Lorenz, M. Despont, N. Fahrni et al.: SU-8: A low-cost negative resist for MEMS, J. Micromech. Microeng. 7, 121–124 (1997)
7. P. Abgrall, V. Conedera, H. Camon et al.: SU-8 as a structural material for labs-on-chips and microelectromechanical systems, Electrophoresis 28, 4539–4551 (2007)
8. L.J. Guerin, M. Bossel, M. Demierre et al.: Simple and low cost fabrication of embedded micro-channels by using a new thick-film photoplastic. Technical Digest, International Conference on Solid State Sensors and Actuators, Chicago, IL, pp. 1419–1422 (1997)
9. B. Bohl, R. Steger, R. Zengerle et al.: Multi-layer SU-8 lift-off technology for microfluidic devices, J. Micromech. Microeng. 15, 1125–1130 (2005)
10. R.J. Jackman, T.M. Floyd, R. Ghodssi et al.: Microfluidic systems with on-line UV detection fabricated in photodefinable epoxy, J. Micromech. Microeng. 11, 263–269 (2001)
11. A. Mata, A.J. Fleischman, S. Roy: Fabrication of multi-layer SU-8 microstructures, J. Micromech. Microeng. 16, 276–284 (2006)
12. C.H. Lin, G.B. Lee, B.W. Chang et al.: A new fabrication process for ultra-thick microfluidic microstructures utilizing SU-8 photoresist, J. Micromech. Microeng. 12, 590–597 (2002)
13. S. Tuomikoski, S. Franssila: Free-standing SU-8 microfluidic chips by adhesive bonding and release etching, Sens. Act. A Phys. 120, 408–415 (2005)
14. H.K. Chang, Y.K. Kim: UV-LIGA process for high aspect ratio structure using stress barrier and C-shaped etch hole, Sens. Act. A Phys. 84, 342–350 (2000)
15. M. Han, W. Lee, S.K. Lee et al.: 3D microfabrication with inclined/rotated UV lithography, Sens. Act. A Phys. 111, 14–20 (2004)
16. Y.K. Yoon, J.H. Park, M.G. Allen: Multidirectional UV lithography for complex 3-D MEMS structures, J. Microelectromech. Syst. 15, 1121–1130 (2006)
17. C. Cremers, F. Bouamrane, L. Singleton et al.: SU-8 as resist material for deep X-ray lithography, Microsyst. Technol. 7, 11–16 (2001)
18. A.L. Bogdanov, S.S. Peredkov: Use of SU-8 photoresist-for very high aspect ratio x-ray lithography, Microelectron. Eng. 53, 493–496 (2000)
19. C.G.K. Malek: SU8 resist for low-cost X-ray patterning of high-resolution, high-aspect-ratio MEMS, Microelectron. J. 33, 101–105 (2002)
20. Y.J. Song, C.S.S.R. Kumar, J. Hormes: Fabrication of an SU-8 based microfluidic reactor on a PEEK substrate sealed by a 'flexible semi-solid transfer' (FST) process, J. Micromech. Microeng. 14, 932–940 (2004)
21. C. Kourouklis, T. Kohlmeier, H.H. Gatzen: The application of chemical-mechanical polishing for planarizing a SU-8/permalloy combination used in MEMS devices, Sens. Act. A Phys. 106, 263–266 (2003)
22. R. Feng, R.J. Farris: The characterization of thermal and elastic constants for an epoxy photoresist SU8 coating, J. Mater. Sci. 37, 4795–4801 (2002)
23. R. Feng, R.J. Farris: Influence of processing conditions on the thermal and mechanical properties of SU8 negative photoresist coatings, J. Micromech. Microeng. 13, 80–88 (2003)
24. S. Jiguet, A. Bertsch, H. Hofmann et al.: SU8-silver photosensitive nanocomposite, Adv. Eng. Mater. 6, 719–724 (2004)
25. S. Jiguet, A. Bertsch, H. Hofmann et al.: Conductive SU8 photoresist for microfabrication, Adv. Funct. Mater. 15, 1511–1516 (2005)
26. N. Damean, B.A. Parviz, J.N. Lee et al.: Composite ferromagnetic photoresist for the fabrication of microelectromechanical systems, J. Micromech. Microeng. 15, 29–34 (2005)

27. I.G. Foulds, M. Parameswaran: A planar self-sacrificial multilayer SU-8-based MEMS process utilizing a UV-blocking layer for the creation of freely moving parts, J. Micromech. Microeng. 16, 2109–2115 (2006)
28. J.M. Ruano-Lopez, M. Aguirregabiria, M. Tijero et al.: A new SU-8 process to integrate buried waveguides and sealed microchannels for a Lab-on-a-Chip, Sens. Act. B Chem. 114, 542–551 (2006)
29. S. Jiguet, A. Bertsch, M. Judelewicz et al.: SU-8 nanocomposite photoresist with low stress properties for microfabrication applications, Microelectron. Eng. 83, 1966–1970 (2006)
30. S. Jiguet, M. Judelewicz, S. Mischler et al.: Effect of filler behavior on nanocomposite SU8 photoresist for moving micro-parts, Microelectron. Eng. 83, 1273–1276 (2006)
31. S. Jiguet, M. Judelewicz, S. Mischler et al.: SU-8 nanocomposite coatings with improved tribological performance for MEMS, Surf. Coatings Technol. 201, 2289–2295 (2006)
32. J. Zhang, W.X. Zhou, M.B. Chan-Park et al.: Argon plasma modification of SU-8 for very high aspect ratio and dense copper electroforming, J. Electrochem. Soc. 152, C716–C721 (2005)
33. M. Nordstrom, R. Marie, M. Calleja et al.: Rendering SU-8 hydrophilic to facilitate use in micro channel fabrication, J. Micromech. Microeng. 14, 1614–1617 (2004)
34. Y.L. Wang, J.H. Pai, H.H. Lai et al.: Surface graft polymerization of SU-8 for bio-MEMS applications, J. Micromech. Microeng. 17, 1371–1380 (2007)
35. Z. Gao, D.B. Henthorn, C.S. Kim: Enhanced wettability of a SU-8 photoresist through a photografting procedure for bioanalytical device applications, J. Micromech. Microeng. 18 (2008) (article number 045013)
36. S.L. Tao, K.C. Popat, J.J. Norman et al.: Surface modification of SU-8 for enhanced biofunctionality and nonfouling properties, Langmuir 24, 2631–2636 (2008)
37. M. Joshi, N. Kale, R. Lal et al.: A novel dry method for surface modification of SU-8 for immobilization of biomolecules in bio-MEMS, Biosens. Bioelectron. 22, 2429–2435 (2007)
38. F.G. Tseng, K.H. Lin, H.T. Hsu et al.: A surface-tension-driven fluidic network for precise enzyme batch-dispensing and glucose detection, Sens. Act. A Phys. 111, 107–117 (2004)
39. F. Walther, P. Davydovskaya, S. Zucher et al.: Stability of the hydrophilic behavior of oxygen plasma activated SU-8, J. Micromech. Microeng. 17, 524–531 (2007)
40. R.M. Wagterveld, C.W.J. Berendsen, S. Bouaidat et al.: Ultralow hysteresis superhydrophobic surfaces by excimer laser modification of SU-8, Langmuir 22, 10904–10908 (2006)
41. N.J. Shirtcliffe, S. Aqil, C. Evans et al.: The use of high aspect ratio photoresist (SU-8) for super-hydrophobic pattern prototyping, J. Micromech. Microeng. 14, 1384–1389 (2004)
42. B.A. Weisenberg, D.L. Mooradian: Hemocompatibility of materials used in microelectromechanical systems: Platelet adhesion and morphology in vitro, J. Biomed. Mater. Res. 60, 283–291 (2002)
43. G. Voskerician, M.S. Shive, R.S. Shawgo et al.: Biocompatibility and biofouling of MEMS drug delivery devices, Biomaterials 24, 1959–1967 (2003)
44. F. Ceyssens, Puers R: Creating multi-layered structures with freestanding parts in SU-8, J. Micromech. Microeng. 16, S19–S23 (2006)
45. Y.J. Chuang, F.G. Tseng, J.H. Cheng et al.: A novel fabrication method of embedded microchannels by using SU-8 thick-film photoresists, Sens. Actuators A Phys. 103, 64–69 (2003)
46. B.E.J. Alderman, C.M. Mann, D.P. Steenson et al.: Microfabrication of channels using an embedded mask in negative resist, J. Micromech. Microeng. 11, 703–705 (2001)
47. W.H. Wong, Pun EYB: Exposure characteristics and three-dimensional profiling of SU8C resist using electron beam lithography, J. Vac. Sci. Technol. B 19, 732–735 (2001)
48. H. Yu, U. Balogun, B. Li et al.: Building embedded microchannels using a single layered SU-8, and determining Young's modulus using a laser acoustic technique, J. Micromech. Microeng. 14, 1576–1584 (2004)

49. J.A. van Kan, A.A. Bettiol, B.S. Wee et al.: Proton beam micromachining: A new tool for precision three-dimensional microstructures, Sens. Act. A Phys. 92, 370–374 (2001)
50. F.E.H. Tay, J.A. van Kan, F. Watt et al.: A novel micro-machining method for the fabrication of thick-film SU-8 embedded micro-channels, J. Micromech. Microeng. 11, 27–32 (2001)
51. A. Bertsch, H. Lorenz, P. Renaud: Combining Microstereolithography and Thick Resist UV Lithography for 3D Microfabrication, pp. 18–23 (Heidelberg, Germany, 1998)
52. A. Bertsch, H. Lorenz, P. Renaud: 3D microfabrication by combining microstereolithography and thick resist UV lithography, Sens. Act. A Phys. 73, 14–23 (1999)
53. H. Lorenz, M. Despont, N. Fahrni et al.: High-aspect-ratio, ultrathick, negative-tone near-UV photoresist and its applications for MEMS, Sens. Act. A Phys. 64, 33–39 (1998)
54. J. Zhang, K.L. Tan, G.D. Hong et al.: Polymerization optimization of SU-8 photoresist and its applications in microfluidic systems and MEMS, J. Micromech. Microeng. 11, 20–26 (2001)
55. S.J. Kim, H. Yang, K. Kim et al.: Study of SU-8 to make a Ni master-mold: Adhesion, sidewall profile, and removal, Electrophoresis 27, 3284–3296 (2006)
56. P.M. Dentinger, W.M. Clift, S.H. Goods: Removal of SU-8 photoresist for thick film applications, Microelectron. Eng. 61–2, 993–1000 (2002)
57. R. Turner, Y. Desta, K. Kelly et al.: Tapered LIGA HARMs, J. Micromech. Microeng. 13, 367–372 (2003)
58. L.A. Liew, W.G. Zhang, V.M. Bright et al.: Fabrication of SiCN ceramic MEMS using injectable polymer-precursor technique, Sens. Act. A Phys. 89, 64–70 (2001)
59. R.K. Vestergaard, S. Bouwstra: Removable SU-8 mould with small feature size for electroplating compliant metal micro actuators. Technical Digest, International Conference on Solid State Sensors and Actuators, Sendai, Japan, pp. 480–483 (1999)
60. R.K. Vestergaard, S. Bouwstra: Electroplated compliant metal microactuators with small feature sizes using a removable SU-8 mould, Microsyst. Technol. 6, 214–217 (2000)
61. G. Hong, A.S. Holmes, M.E. Heaton: SU8 resist plasma etching and its optimisation, Microsyst. Technol. Micro- and Nanosyst. Inf. Storage Process. Syst. 10, 357–359 (2004)
62. M.K. Ghantasala, J.P. Hayes, E.C. Harvey et al.: Patterning, electroplating and removal of SU-8 moulds by excimer laser micromachining, J. Micromech. Microeng. 11, 133–139 (2001)
63. H. Lorenz, M. Despont, P. Vettiger et al.: Fabrication of photoplastic high-aspect ratio microparts and micromolds using SU-8 UV resist, Microsyst. Technol. 4, 143–146 (1998)
64. C.-H. Ho, K.-P. Chin, C.-R. Yang et al.: Ultrathick SU-8 mold formation and removal, and its application to the fabrication of LIGA-like micromotors with embedded roots, Sens. Act. A Phys. A102, 130–138 (2002)
65. S. Metz, S. Jiguet, A. Bertsch et al.: Polyimide and SU-8 microfluidic devices manufactured by heat-depolymerizable sacrificial material technique, Lab Chip 4, 114–120 (2004)
66. L. Dellmann, S. Roth, C. Beuret et al.: Fabrication process of high aspect ratio elastic and SU-8 structures for piezoelectric motor applications, Sens. Act. A Phys. 70, 42–47 (1998)
67. V. Seidemann, J. Rabe, M. Feldmann et al.: SU8-micromechanical structures with in situ fabricated movable parts, Microsyst. Technol. 8, 348–350 (2002)
68. J. Zou, X.F. Wang, D. Bullen et al.: A mould-and-transfer technology for fabricating scanning probe microscopy probes, J. Micromech. Microeng. 14, 204–211 (2004)
69. T.Q. Truong, N.T. Nguyen: A polymeric piezoelectric micropump based on lamination technology, J. Micromech. Microeng. 14, 632–638 (2004)
70. J.H. Daniel, B. Krusor, R.B. Apte et al.: Micro-electro-mechanical system fabrication technology applied to large area x-ray image sensor arrays, J. Vac. Sci. Technol. A 19, 1219–1223 (2001)
71. N.T. Nguyen, T.Q. Truong, K.K. Wong et al.: Micro check valves for integration into polymeric microfluidic devices, J. Micromech. Microeng. 14, 69–75 (2004)
72. A. Johansson, M. Calleja, P.A. Rasmussen et al.: SU-8 cantilever sensor system with integrated readout, Sens. Act. A Phys. 123–124, 111–115 (2005)

73. V. Seidemann, S. Butefisch, S. Buttgenbach: Fabrication and investigation of in-plane compliant SU8 structures for MEMS and their application to micro valves and micro grippers, Sens. Act. A Phys. 97–98, 457–461 (2002)
74. C. Luo, A. Govindaraju, J. Garra et al.: Releasing SU-8 structures using polystyrene as a sacrificial material, Sens. Act. A Phys. 114, 123–128 (2004)
75. J. Liu, B. Cai, J. Zhu et al.: A novel device of passive and fixed alignment of optical fiber, Microsyst. Technol. Micro Nanosyst. Inf. Storage Process. Syst. 10, 269–271 (2004)
76. P. Basset, A. Kaiser, D. Collard et al.: Process and realization of a three-dimensional gold electroplated antenna on a flexible epoxy film for wireless micromotion system, J. Vac. Sci. Technol. B 20, 1465–1470 (2002)
77. G. Kim, B. Kim, J. Brugger: All-photoplastic microstencil with self-alignment for multiple layer shadow-mask patterning, Sens. Act. A Phys. 107, 132–136 (2003)
78. V. Conedera, L. Salvagnac, N. Fabre et al.: Surface micromachining technology with two SU-8 structural layers and sol-gel, SU-8 or SiO2/sol-gel sacrificial layers, J. Micromech. Microeng. 17, N52–N57 (2007)
79. A. Liotard, F. Zamkotsian, V. Conedera et al.: Polymer-based micro deformable mirror for adaptive optics. Proceedings of SPIE. The International Society for Optical Engineering, San Jose, CA, p. 61130 (2006)
80. S. Mouaziz, G. Boero, R.S. Popovic et al.: Polymer-based cantilevers with integrated electrodes, J. Microelectromech. Syst. 15, 890–895 (2006)
81. N.T. Nguyen, S.S. Ho, C.L.N. Low: A polymeric microgripper with integrated thermal actuators, J. Micromech. Microeng. 14, 969–974 (2004)
82. M.C. Cheng, A.P. Gadre, J.A. Garra et al.: Dry release of polymer structures with anti-sticking layer, J. Vac. Sci. Technol. A 22, 837–841 (2004)
83. D. Haefliger, A. Boisen: Three-dimensional microfabrication in negative resist using printed masks, J. Micromech. Microeng. 16, 951–957 (2006)
84. M. Agirregabiria, F.J. Blanco, J. Berganzo et al.: Fabrication of SU-8 multilayer microstructures based on successive CMOS compatible adhesive bonding and releasing steps, Lab Chip 5, 545–552 (2005)
85. Z.C. Peng, Z.G. Ling, M. Tondra et al.: CMOS compatible integration of three-dimensional microfluidic systems based on low-temperature transfer of SU-8 films, J. Microelectromech. Syst. 15, 708–716 (2006)
86. P. Abgrall, C. Lattes, V. Conederal et al.: A novel fabrication method of flexible and monolithic 3D microfluidic structures using lamination of SU-8 films, J. Micromech. Microeng. 16, 113–121 (2006)
87. B.J. Kim, M. Liebau, J. Huskens et al.: A self-assembled monolayer-assisted surface microfabrication and release technique, Microelectron. Eng. 57–58, 755–760 (2001)
88. G.M. Kim, B. Kim, M. Liebau et al.: Surface modification with self-assembled monolayers for nanoscale replication of photoplastic MEMS, J. Microelectromech. Syst. 11, 175–181 (2002)
89. D.J. Strike, G.C. Fiaccabrino, M. Koudelka-Hep et al.: Enzymatic microreactor using Si, glass and EPON SU-8, Biomed. Microdev. 2, 175 (2000)
90. J. West, B. Karamata, B. Lillis et al.: Application of magnetohydrodynamic actuation to continuous flow chemistry, Lab Chip 2, 224–230 (2002)
91. Gersborg-M. Hansen, A. Kristensen: Optofluidic third order distributed feedback dye laser, Appl. Phys. Lett. 89 (2006) (article number 103518)
92. B. Bilenberg, T. Nielsen, B. Clausen et al.: PMMA to SU-8 bonding for polymer based lab-on-a-chip systems with integrated optics, J. Micromech. Microeng. 14, 814–818 (2004)
93. E.W. Simoes, R. Furlan, R.E.B. Leminski et al.: Microfluidic oscillator for gas flow control and measurement, Flow Meas. Instrum. 16, 7–12 (2005)
94. K.B. Mogensen, J. El-Ali, A. Wolff et al.: Integration of polymer waveguides for optical detection in microfabricated chemical analysis systems, Appl. Opt. 42, 4072–4079 (2003)
95. Y.M. Huang, M. Uppalapati, W.O. Hancock et al.: Microfabricated capped channels for biomolecular motor-based transport, IEEE Trans. Adv. Packaging 28, 564–570 (2005)

96. S. Arscott, P. Mounaix, D. Lippens: Substrate transfer process for InP-based heterostructure barrier varactor devices, J. Vac. Sci. Technol. B 18, 150–155 (2000)
97. C.T. Pan, H. Yang, S.C. Shen et al.: A low-temperature wafer bonding technique using patternable materials, J. Micromech. Microeng. 12, 611–615 (2002)
98. F.J. Blanco, M. Agirregabiria, J. Garcia et al.: Novel three-dimensional embedded SU-8 microchannels fabricated using a low temperature full wafer adhesive bonding, J. Micromech. Microeng. 14, 1047–1056 (2004)
99. P. Svasek, E. Svasek, B. Lendl et al.: Fabrication of miniaturized fluidic devices using SU-8 based lithography and low temperature wafer bonding, Sens. Act. A Phys. 115, 591–599 (2004)
100. S. Li, C.B. Freidhoff, R.M. Young et al.: Fabrication of micronozzles using low-temperature wafer-level bonding with SU-8, J. Micromech. Microeng. 13, 732–738 (2003)
101. S. Tuomikoski, S. Franssila: Wafer-level bonding of MEMS structures with SU-8 epoxy photoresist, Phys. Scr. T114, 223–226 (2004)
102. A. Heeren, C.P. Luo, G. Roth et al.: Diffusion along microfluidic channels, Microelectron. Eng. 83, 1669–1672 (2006)
103. L. Cui, T. Zhang, H. Morgan: Optical particle detection integrated in a dielectrophoretic lab-on-a-chip, J. Micromech. Microeng. 12, 7–12 (2002)
104. B. Helbo, A. Kristensen, A. Menon: A micro-cavity fluidic dye laser, J. Micromech. Microeng. 13, 307–311 (2003)
105. J. Carlier, S. Arscott, V. Thomy et al.: Integrated microfluidics based on multi-layered SU-8 for mass spectrometry analysis, J. Micromech. Microeng. 14, 619–624 (2004)
106. Y.T. Chen, D. Lee: A bonding technique using hydrophilic SU-8, J. Micromech. Microeng. 17, 1978–1984 (2007)
107. S. Charlot, A.M. Gue, J. Tasselli et al.: A low cost and hybrid technology for integrating silicon sensors or actuators in polymer microfluidic systems, J. Micromech. Microeng. 18 (2008) (article number 017003)
108. J.D.L. Shapley, D.A. Barrow: Novel patterning method for the electrochemical production of etched silicon, Thin Solid Films 388, 134–137 (2001)
109. M. Aktary, M.O. Jensen, K.L. Westra et al.: High-resolution pattern generation using the epoxy novolak SU-8 2000 resist by electron beam lithography, J. Vac. Sci. Technol. B 21, L5–L7 (2003)
110. J. Zhang, M.B. Chan-Park, S.R. Conner: Effect of exposure dose on the replication fidelity and profile of very high aspect ratio microchannels in SU-8, Lab Chip 4, 646–653 (2004)
111. M. Gaudet, J.C. Camart, L. Buchaillot et al.: Variation of absorption coefficient and determination of critical dose of SU-8 at 365 nm, Appl. Phys. Lett. 88 (2006) (article number 024107)
112. B. Eyre, J. Blosiu, D. Wiberg: Taguchi optimization for the processing of epon SU-8 resist. Proceedings of the IEEE Microelectromechanical Systems Conference, Heidelberg, Germany, pp. 218–222 (1998)
113. Ling Z-G, K. Lian, L. Jian: Improved patterning quality of SU-8 microstructures by optimizing the exposure parameters. Proceedings of SPIE – The International Society for Optical Engineering, Santa Clara, CA, pp. 1019–1027 (2000)
114. J.D. Williams, W. Wang: Using megasonic development of SU-8 to yield ultra-high aspect ratio microstructures with UV lithography, Microsyst. Technol. Micro Nanosyst. Inf. Storage Process. Syst. 10, 694–698 (2004)
115. D. Bachmann, B. Schoberle, S. Kuhne et al.: Fabrication and characterization of folded SU-8 suspensions for MEMS applications, Sens. Act. A Phys. 130, 379–386 (2006)
116. H. Lorenz, M. Laudon, P. Renaud: Mechanical characterization of a new high-aspect-ratio near UV-photoresist, Microelectron. Eng. 41–42, 371–374 (1998)
117. D. Sameoto, S.H. Tsang, I.G. Foulds et al.: Control of the out-of-plane curvature in SU-8 compliant microstructures by exposure dose and baking times, J. Micromech. Microeng. 17, 1093–1098 (2007)

118. R. Ruhmann, G. Ahrens, A. Schuetz et al.: Reduction of internal stress in a SU-8-like negative tone photoresist for MEMS applications by chemical modification. Proceedings of SPIE – The International Society for Optical Engineering, Santa Clara, CA, pp. 502–510 (2001)
119. R. Lo, E. Meng: Integrated and reusable in-plane microfluidic interconnects, Sens. Act. B: Chem. 132, 531–539 (2008)
120. P. Abgrall, A.M. Gue: Lab-on-chip technologies: making a microfluidic network and coupling it into a complete microsystem – a review, J. Micromech. Microeng. 17, R15–R49 (2007)
121. P. Mali, A. Sarkar, R. Lal: Facile fabrication of microfluidic systems using electron beam lithography, Lab Chip 6, 310–315 (2006)
122. J. Xie, Q. He, Y.-C. Tai et al.: Integrated electrospray chip for mass spectrometry. MicroTAS, Nara, Japan, pp. 709–711 (2002)
123. P.Y. Li, J. Shih, R. Lo et al.: An electrochemical intraocular drug delivery device, Sens. Act. A Phys. 143, 41–48 (2008)
124. E. L'Hostis, P.E. Michel, G.C. Fiaccabrino et al.: Microreactor and electrochemical detectors fabricated using Si and EPON SU-8, Sens. Act. B Chem. 64, 156–162 (2000)
125. S. Matsumoto, Y.C. Tai: A nL/min-scale valveless flow regulator for integrated micro chemical devices, JSME Int. J. Ser. B – Fluids Therm. Eng. 47, 528–533 (2004)
126. L.-Y. Chang, P.-Y. Li, L. Zhao et al.: Integrated flow sensing for focal biochemical stimulation. Proceedings of the 3rd IEEE International Conference on Nano/Micro Engineered and Molecular Systems, NEMS, Sanya, China, pp. 921–926 (2008)
127. J.H. Park, Y.K. Yoon, S.O. Choi et al.: Tapered conical polymer microneedles fabricated using an integrated lens technique for transdermal drug delivery, IEEE Trans. Biomed. Eng. 54, 903–913 (2007)
128. S. Rajaraman, S.O. Choi, R.H. Shafer et al.: Microfabrication technologies for a coupled three-dimensional microelectrode, microfluidic array, J. Micromech. Microeng. 17, 163–171 (2007)
129. R.R. LeVier, M.C. Harrison, R.R. Cook et al.: What is silicone? J. Clin. Epidemiol. 48, 513–517 (1995)
130. M.M.G. Antonisse, J.F.J. Engbersen, D.N. Reinhoudt: Nitrate and Bicarbonate Selective CHEMFETs. Proceedings of the 8th International Conference on Solid-State Sensors and Actuators, and Eurosensors IX. Transducers, Stockholm, Sweden, pp. 867–869 (1995)
131. J.C. Lotters, W. Olthuis, P.H. Veltink et al.: Polydimethylsiloxane as an elastic material applied in a capacitive accelerometer, J. Micromech. Microeng. 6, 52–54 (1996)
132. Z. Chu: Flexible package for a tactile sensor array. Proceedings of the 1996 National Sensor Conference, Delft, The Netherlands (1996)
133. R.E.G.V. Hal: Advanced Packaging of ISFETs, Design, Encapsulation and Bonding, University of Twente (1994)
134. D.J. Campbell, K.J. Beckman, C.E. Calderon et al.: Replication and compression of bulk surface structures with polydimethylsiloxane elastomer, J. Chem. Educ. 75, 537–541 (1999)
135. S.J. Clarson, J.A. Semlyen: Siloxane Polymers (Prentice Hall, Englewood Cliffs, NJ, 1993)
136. J.C. Lotters, W. Olthuis, P.H. Veltink et al.: The mechanical properties of the rubber elastic polymer polydimethylsiloxane for sensor applications, J. Micromech. Microeng. 7, 145–147 (1997)
137. ABCR: Research Chemicals and Metals Catalogue (ABCR, Karlsruhe, Germany, 1994)
138. J.C. Salamone: Polymeric Materials Encyclopedia (CRC Press, Rochester, NY, 1996)
139. D.W. van Krevelen, P.J. Hoftyzer: Properties of Polymers, Their Estimation and Correlation with Chemical Structure (Elsevier Scientific, Amsterdam, 1976)
140. J.E. Mark: Polymer Data Handbook (Oxford University Press, New York, NY, 1999)
141. J. Garra, T. Long, J. Currie et al.: Dry etching of polydimethylsiloxane for microfluidic systems, J. Vac. Sci. Technol. A Vac. Surf. Films 20, 975–982 (2002)

142. D. Armani, C. Liu, N. Aluru: Re-configurable fluid circuits by PDMS elastomer micromachining. Proceedings of IEEE, Micro Electro Mechanical Systems, Orlando, FL (1999)
143. M.C. Belanger, Y. Marois: Hemocompatibility, biocompatibility, inflammatory and in vivo studies of primary reference materials low-density polyethylene and polydimethylsiloxane: A review, J. Biomed. Mater. Res. 58, 467–477 (2001)
144. Y. Zhao, X. Zhang: Adaptation of flexible polymer fabrication to cellular mechanics study, Appl. Phys. Lett. 87 (2005) (article number 14410)
145. L.J. Lee: Polymer nanoengineering for biomedical applications, Ann. Biomed. Eng. 34, 75–88 (2006)
146. A. Mata, A.J. Fleischman, S. Roy: Characterization of polydimethylsiloxane (PDMS) properties for biomedical micro/nanosystems, Biomed. Microdev. 7, 281–293 (2005)
147. M.R. VanLandingham, N.K. Chang, P.L. Drzal et al.: Viscoelastic characterization of polymers using instrumented indentation. I. Quasi-static testing, J. Polym. Sci. B Polym. Phys. 43, 1794–1811 (2005)
148. C.C. White, M.R. Vanlandingham, P.L. Drzal et al.: Viscoelastic characterization of polymers using instrumented indentation. II. Dynamic testing, J. Polym. Sci. B Polym. Phys. 43, 1812–1824 (2005)
149. K.P. Menard: Dynamic Mechanical Analysis (CRC Press, Boca Raton, FL, 1999)
150. A. Chakravartula, K. Komvopoulos: Viscoelastic properties of polymer surfaces investigated by nanoscale dynamic mechanical analysis, Appl. Phys. Lett. 88 (2006) (article number 131901)
151. L. Cheng, X. Xia, W. Yu et al.: Flat-punch indentation of viscoelastic material, J. Polym. Sci. B Polym. Phys. 38, 10–22 (2000)
152. W.G. Knauss, W. Zhu: Nonlinearly viscoelastic behavior of polycarbonate. I. Response under pure shear, Mech. Time-Depend. Mater. 6, 231–269 (2002)
153. I.K. Lin, Y.M. Liao, Y. Liu et al.: Viscoelastic mechanical behavior of soft microcantilever-based force sensors, Appl. Phys. Lett. 93 (2008) (article number 251907)
154. M. Akay, S.N. Rollins, E. Riordan: Mechanical-behavior of sequential polyurethane poly(methyl methacrylate) interpenetrating polymer networks, Polymer 29, 37–42 (1988)
155. M. Wollerdorfer, H. Bader: Influence of natural fibres on the mechanical properties of biodegradable polymers, Ind. Crops Prod. 8, 105–112 (1998)
156. L.A. Majewski, M. Grell, S.D. Ogier et al.: A novel gate insulator for flexible electronics, Org. Electron. 4, 27–32 (2003)
157. Y.N. Xia, J.J. McClelland, R. Gupta et al.: Replica molding using polymeric materials: A practical step toward nanomanufacturing, Adv. Mater. 9, 147–149 (1997)
158. Patternable Silicones for Electronics, Product Data Sheet, Dow Corning, http://www.dowcorning.com/content/etronics/etronicspattern/
159. Product information for Cyclotene, Dow Chemical, http://www.dow.com/cyclotene/index.htm
160. W.S. Kim, R. Houbertz, T.H. Lee et al.: Effect of photoinitiator on photopolymerization of inorganic-organic hybrid polymers (ORMOCER (R)), J. Polym. Sci. B Polym. Phys. 42, 1979–1986 (2004)
161. J.H. Ward, R. Bashir, N.A. Peppas: Micropatterning of biomedical polymer surfaces by novel UV polymerization techniques, J. Biomed. Mater. Res. 56, 351–360 (2001)
162. A.A.S. Bhagat, P. Jothimuthu, I. Papautsky: Photodefinable polydimethylsiloxane (PDMS) for rapid lab-on-a-chip prototyping, Lab Chip 7, 1192–1197 (2007)
163. H.L. Cong, T.R. Pan: Photopatternable conductive PDMS materials for microfabrication, Adv. Funct. Mater. 18, 1912–1921 (2008)
164. K. Tsougeni, A. Tserepi, E. Gogolides: Photosensitive poly(dimethylsiloxane) materials for microfluidic applications, Microelectron. Eng. 84, 1104–1108 (2007)
165. A. Kumar, G.M. Whitesides: Features of gold having micrometer to centimeter dimensions can be formed through a combination of stamping with an elastomeric stamp and an alkanethiol ink followed by chemical etching, Appl. Phys. Lett. 63, 2002–2004 (1993)

166. R.E. Kirk, D.F. Othmer, J.I. Kroschwitz et al.: Encyclopedia of Chemical Technology (Wiley, New York, NY, 2007)
167. T.E. Creighton: Proteins: Structures and Molecular Properties (W.H. Freeman, New York, NY, 1993)
168. Y.N. Xia, G.M. Whitesides: Soft lithography, Angew. Chem. Int. Ed. 37, 551–575 (1998)
169. W. Sanger: Principles of Nucleic Acid Structure (Springer, New York, NY, 1986)
170. H. Ringsdorf, B. Schlarb, J. Venzmer: Molecular architecture and function of polymeric oriented systems – models for the study of organization, surface recognition, and dynamics of biomembranes, Angew. Chem. Int. Ed. Engl. 27, 113–158 (1988)
171. B.C. Wheeler, J.M. Corey, G.J. Brewer et al.: Microcontact printing for precise control of nerve cell growth in culture, J. Biomech. Eng. Trans. ASME 121, 73–78 (1999)
172. A. Bernard, J.P. Renault, B. Michel et al.: Microcontact printing of proteins, Adv. Mater. 12, 1067–1070 (2000)
173. D.J. Beebe, G.A. Mensing, Walker GM: Physics and applications of microfluidics in biology, Annu. Rev. Biomed. Eng. 4, 261–286 (2002)
174. S.C. Jakeway, A.J. de Mello, E.L. Russell: Miniaturized total analysis systems for biological analysis, Fresenius J. Anal. Chem. 366, 525–539 (2000)
175. Y.H. Kim, K.S. Shin, J.Y. Kang et al.: Poly(dimethylsiloxane)-based packaging technique for microchip fluorescence detection system applications, J. Microelectromech. Syst. 15, 1152–1158 (2006)
176. K. Hosokawa, K. Sato, N. Ichikawa et al.: Power-free poly(dimethylsiloxane) microfluidic devices for gold nanoparticle-based DNA analysis, Lab Chip 4, 181–185 (2004)
177. D.A. Bartholomeusz, R.W. Boutte, J.D. Andrade: Xurography: Rapid prototyping of microstructures using a cutting plotter, J. Microelectromech. Syst. 14, 1364–1374 (2005)
178. M.A. Eddings, B.K. Gale: A PDMS-based gas permeation pump for on-chip fluid handling in microfluidic devices, J. Micromech. Microeng. 16, 2396–2402 (2006)
179. K. Morishima, Y. Tanaka, K. Sato et al.: Bioactuated microsystem using cultured cardiomyocytes. Proceedings of the MicroTotal Analysis Systems, Squaw Valley, CA, pp. 1125–1128 (2003)
180. Y. Tanaka, K. Morishima, T. Shimizu et al.: Demonstration of a PDMS-based bio-microactuator using cultured cardiomyocytes to drive polymer micropillars, Lab Chip 6, 230–235 (2006)
181. Y. Zhao, C.C. Lim, D.B. Sawyer et al.: Cellular force measurements using single-spaced polymeric microstructures: Isolating cells from base substrate, J. Micromech. Microeng. 15, 1649–1656 (2005)
182. Y. Zhao, C.C. Lim, D.B. Sawyer et al.: Microchip for subcellular mechanics study in living cells, Sens. Act. B Chem. 114, 1108–1115 (2006)
183. M.T. Yang, N.J. Sniadecki, C.S. Chen: Geometric considerations of micro- to nanoscale elastomeric post arrays to study cellular traction forces, Adv. Mater. 19, 3119–3123 (2007)
184. J.L. Tan, J. Tien, D.M. Pirone et al.: Cells lying on a bed of microneedles: An approach to isolate mechanical force, Proc. Natl Acad. Sci. USA. 100, 1484–1489 (2003)
185. I.K. Lin, Y.M. Liao, K.S. Chen et al.: Viscoelastic characterization of soft micropillars for cellular mechanics study. 12th International Conference on Miniaturized Systems for Chemistry and Life Sciences, San Diego, CA (2008)
186. M.S. Kolodney, R,B, Wysolmerski: Isometric contraction by fibroblasts and endothelial-cells in tissue-culture – a quantitative study, J. Cell Biol. 117, 73–82 (1992)
187. O. Cazorla, Y.M. Wu, T.C. Irving et al.: Titin-based modulation of calcium sensitivity of active tension in mouse skinned cardiac myocytes, Circ. Res. 88, 1028–1035 (2001)
188. K. Visscher, M.J. Schnitzer, S.M. Block: Single kinesin molecules studied with a molecular force clamp, Nature 400, 184–189 (1999)
189. L.H. Opie: The Heart Physiology: From Cell to Circulation (Lippincott-Raven, Philadelphia, PA, 1998)

190. K. Sato, S. Harada, A. Saiki et al.: Novel planar multilevel interconnection technology utilizing polyimide. IEEE Transactions on Parts Hybrids and Packaging PHP9, pp. 176–180 (1973)
191. K. Mukai, A. Saiki, K. Yamanaka et al.: Planar multilevel interconnection technology employing a polyimide, IEEE J. Solid-State Circuits 13, 462–467 (1978)
192. A.M. Wilson: Polyimide insulators for multilevel interconnections, Thin Solid Films 83, 145–163 (1981)
193. S. Sasaki, T. Kon, T. Ohsaki et al.: A new multichip module using a copper polyimide multilayer substrate, IEEE Trans. Compon. Hybrids Manuf. Technol. 12, 658–662 (1989)
194. M. Gad-el-Hak: MEMS: Design and Fabrication (CRC/Taylor & Francis, Boca Raton, FL, 2006)
195. P.W. Barth, S.L. Bernard, J.B. Angell: Flexible circuit and sensor arrays fabricated by monolithic silicon technology, IEEE Trans. Electron Dev. 32, 1202–1205 (1985)
196. S.A. Shamma-Donoghue, G.A. May, N.E. Cotter et al.: Thin-film multielectrode arrays for a cochlear prosthesis, IEEE Trans. Electron Dev. 29, 136–144 (1982)
197. R.L. White, L.A. Roberts, O. Kwon et al.: Thin-film electrodes for an artificial ear, J. Vac. Sci. Technol. A Vac. Surf. Films 1, 287–295 (1983)
198. A.B. Frazier: Recent applications of polyimide to micromachining technology, IEEE Trans. Ind. Electron. 42, 442–448 (1995)
199. A.B. Frazier, C.H. Ahn, M.G. Allen: Development of micromachined devices using polyimide-based processes, Sens. Act. A Phys. 45, 47–55 (1994)
200. M. Pedersen, W. Olthuis, P. Bergveld: High-performance condenser microphone with fully integrated CMOS amplifier and DC-DC voltage converter, J. Microelectromech. Syst. 7, 387–394 (1998)
201. T. Stieglitz: Flexible biomedical microdevices with double-sided electrode arrangements for neural applications, Sens. Act. A Phys. 90, 203–211 (2001)
202. P.J. Rousche, D.S. Pellinen, D.P. Pivin et al.: Flexible polyimide-based intracortical electrode arrays with bioactive capability, IEEE Trans. Biomed. Eng. 48, 361–371 (2001)
203. N. Lago, K. Yoshida, K.P. Koch et al.: Assessment of biocompatibility of chronically implanted polyimide and platinum intrafascicular electrodes, IEEE Trans. Biomed. Eng. 54, 281–290 (2007)
204. D.C. Rodger, A.J. Fong, L. Wen et al.: Flexible parylene-based multielectrode array technology for high-density neural stimulation and recording, Sens. Act. B Chem. 132, 449–460 (2008)
205. D.C. Rodger, J.D. Weiland, M.S. Humayun et al.: Scalable high lead-count parylene package for retinal prostheses, Sens. Act. B Chem. 117, 107–114 (2006)
206. D. Bhusari, H.A. Reed, M. Wedlake et al.: Fabrication of air-channel structures for microfluidic, microelectromechanical, and microelectronic applications, J. Microelectromech. Syst. 10, 400–408 (2001)
207. A.B. Frazier, M.G. Allen: Metallic microstructures fabricated using photosensitive polyimide electroplating molds, J. Microelectromech. Syst. 2, 87–94 (1993)
208. A. Bagolini, L. Pakula, T.L.M. Scholtes et al.: Polyimide sacrificial layer and novel materials for post-processing surface micromachining, J. Micromech. Microeng. 12, 385–389 (2002)
209. Y.J. Kim, M.G. Allen: In situ measurement of mechanical properties of polyimide films using micromachined resonant string structures, IEEE Trans. Compon. Packaging Technol. 22, 282–290 (1999)
210. A.B. Frazier, M.G. Allen: Piezoresistive graphite polyimide thin-films for micromachining applications, J. Appl. Phys. 73, 4428–4433 (1993)
211. D. Memmi, V. Foglietti, E. Cianci et al.: Fabrication of capacitive micromechanical ultrasonic transducers by low-temperature process, Sens. Act. A Phys. 99, 85–91 (2002)
212. M. Eray, N.S. Dogan, L.J. Liu et al.: Highly stable bilayer-lipid membranes (blms) formed on microfabricated polyimide apertures, Biosens. Bioelectron. 9, 343–351 (1994)
213. K. Minami, H. Morishita, M. Esashi: A bellows-shape electrostatic microactuator, Sens. Act. A Phys. 72, 269–276 (1999)

214. L.S. Pakula, H. Yang, H.T.M. Pham et al.: Fabrication of a CMOS compatible pressure sensor for harsh environments, J. Micromech. Microeng. 14, 1478–1483 (2004)
215. M.A. Schmidt, R.T. Howe, S.D. Senturia et al.: Design and calibration of a microfabricated floating-element shear-stress sensor, IEEE Trans. Electron Dev. 35, 750–757 (1988)
216. P.J. Schubert, J.H. Nevin: A polyimide-based capacitive humidity sensor, IEEE Trans. Electron Dev. 32, 1220–1223 (1985)
217. R. Selvaraj, H.T. Lin, J.F. McDonald: Integrated optical wave-guides in polyimide for wafer scale integration, J. Lightw. Technol. 6, 1034–1044 (1988)
218. Y.W. Kim, M.G. Allen: Single-layer and multilayer surface-micromachined platforms using electroplated sacrificial layers, Sens. Act. A Phys. 35, 61–68 (1992)
219. T. Stieglitz, H. Beutel, J.U. Meyer: A flexible, light-weight multichannel sieve electrode with integrated cables for interfacing regenerating peripheral nerves, Sens. Act. A Phys. 60, 240–243 (1997)
220. G. Turban, M. Rapeaux: Dry etching of polyimide in O2-Cf4 and O2-Sf6 plasmas, J. Electrochem. Soc. 130, 2231–2236 (1983)
221. U. Buder, J.P. von Klitzing, E. Obermeier: Reactive ion etching for bulk structuring of polyimide, Sens. Act. A Phys. 132, 393–399 (2006)
222. C.H. Ahn, Y.J. Kim, M.G. Allen: A Fully Integrated planar toroidal inductor with a micromachined nickel iron magnetic bar, IEEE Trans. Compon. Packaging Manuf. Technol. A 17, 463–469 (1994)
223. T. Stieglitz, H.H. Ruf, M. Gross et al.: A biohybrid system to interface peripheral nerves after traumatic lesions: Design of a high channel sieve electrode, Biosens. Bioelectron. 17, 685–696 (2002)
224. J.W. Suh, S.F. Glander, R.B. Darling et al.: Organic thermal and electrostatic ciliary microactuator array for object manipulation, Sens. Act. A Phys. 58, 51–60 (1997)
225. C.W. Jurgensen, E.S.G. Shaqfeh: Factors controlling the etching rate and etching profile in the O-2 reactive ion etching pattern transfer step in multilevel lithography, Polym. Eng. Sci. 29, 878–881 (1989)
226. J.K. Singh, A. Roybardhan, H.S. Kothari et al.: Dependence of process parameters on planarization isolation and etching of sloped vias in polyimides for GaAs ICs, Proc. IEEE 75, 850–852 (1987)
227. F.D. Egitto, F. Emmi, R.S. Horwath et al.: Plasma-etching of organic materials.1. Polyimide in O2-Cf4, J. Vac. Sci. Technol. B 3, 893–904 (1985)
228. W.H. Juan, S.W. Pang: High-aspect-ratio polyimide etching using an oxygen plasma generated by electron-cyclotron-resonance source, J. Vac. Sci. Technol. B 12, 422–426 (1994)
229. R. Pethig, J.P.H. Burt, A. Parton et al.: Development of biofactory-on-a-chip technology using excimer laser micromachining, J. Micromech. Microeng. 8, 57–63 (1998)
230. P.M. Martin, D.W. Matson, W.D. Bennett et al.: Laminated plastic microfluidic components for biological and chemical systems, J. Vac. Sci. Technol. A Vac. Surf. Films 17, 2264–2269 (1999)
231. C.T. Pan: Perpendicular magnetic anisotropic field for polyimide-based microactuator with excimer laser ablation, Sens. Act. A Phys. 113, 240–247 (2004)
232. A. Schwarz, J.S. Rossier, E. Roulet et al.: Micropatterning of biomolecules on polymer substrates, Langmuir 14, 5526–5531 (1998)
233. M. Gross, D. Altpeter, T. Stieglitz et al.: Micromachining of flexible neural implants with low-ohmic wire traces using electroplating, Sens. Act. A Phys. 96, 105–110 (2002)
234. T. Schanze, L. Hesse, C. Lau et al.: An optically powered single-channel stimulation implant as test-system for chronic biocompatibility and biostability of miniaturized retinal vision prostheses, IEEE Trans. Biomed. Eng. 54, 983–992 (2007)
235. J. Engel, J. Chen, C. Liu: Development of polyimide flexible tactile sensor skin, J. Micromech. Microeng. 13, 359–366 (2003)

236. M. Pedersen, M.G.H. Meijerink, W. Olthuis et al.: An IC-compatible polyimide pressure sensor with capacitive readout, Sens. Act. A Phys. 63, 163–168 (1997)
237. M. Pedersen, W. Olthuis, P. Bergveld: A silicon condenser microphone with polyimide diaphragm and backplate, Sens. Act. A Phys. 63, 97–104 (1997)
238. S. Metz, A. Bertsch, D. Bertrand et al.: Flexible polyimide probes with microelectrodes and embedded microfluidic channels for simultaneous drug delivery and multi-channel monitoring of bioelectric activity, Biosens. Bioelectron. 19, 1309–1318 (2004)
239. M.H. Li, J.J. Wu, Y.B. Gianchandani: Surface micromachined polyimide scanning thermocouple probes, J. Microelectromech. Syst. 10, 3–9 (2001)
240. S. McNamara, A.S. Basu, J. Lee et al.: Ultracompliant thermal probe array for scanning non-planar surfaces without force feedback, J. Micromech. Microeng. 15, 237–243 (2005)
241. A. Bayrashev, B. Ziaie: Silicon wafer bonding through RF dielectric heating, Sens. Act. A Phys. 103, 16–22 (2003)
242. R. Nayve, M. Fujii, A. Fukugawa et al.: High-resolution long-array thermal ink jet printhead fabricated by anisotropic wet etching and deep Si RIE, J. Microelectromech. Syst. 13, 814–821 (2004)
243. M. Pedersen, W. Olthuis, P. Bergveld: Development and fabrication of capacitive sensors in polyimide, Sens. Mater. 10, 1–20 (1998)
244. Y. Nakamura, Y. Suzuki, Y. Watanabe: Effect of oxygen plasma etching on adhesion between polyimide films and metal, Thin Solid Films 291, 367–369 (1996)
245. K. Suzuki, H. Yamada, H. Miura et al.: Self-assembly of three dimensional micro mechanisms using thermal shrinkage of polyimide, Microsyst. Technol. Micro Nanosyst. Inf. Storage Process. Syst. 13, 1047–1053 (2007)
246. T. Ebefors, E. Kalvesten, G. Stemme: New small radius joints based on thermal shrinkage of polyimide in V-grooves for robust self-assembly 3D microstructures, J. Micromech. Microeng. 8, 188–194 (1998)
247. T. Ebefors, J.U. Mattsson, E. Kalvesten et al.: A robust micro conveyer realized by arrayed polyimide joint actuators, J. Micromech. Microeng. 10, 337–349 (2000)
248. M. Gel, I. Shimoyama: Parallel-plate electrostatic actuation with vertical hinges, J. Micromech. Microeng. 11, 555–560 (2001)
249. M. Gel, S. Takeuchi, I. Shimoyama: Fabrication method for out-of-plane, micro-coil by surface micromachining, Sens. Act. A Phys. 97–98, 702–708 (2002)
250. H. Miyajima, N. Asaoka, M. Arima et al.: A durable, shock-resistant electromagnetic optical scanner with polyimide-based hinges, J. Microelectromech. Syst. 10, 418–424 (2001)
251. J. Chen, C. Liu: Development and characterization of surface micromachined, out-of-plane hot-wire anemometer, J. Microelectromech. Syst. 12, 979–988 (2003)
252. T.E. Creighton: Proteins: Structures and Molecular Properties (W.H. Freeman, New York, NY, 1993)
253. A. Veis: The Macromolecular Chemistry of Gelatin (Academic, New York, NY, 1964)
254. M. Djabourov, J. Leblond, P. Papon: Gelation of aqueous gelatin solutions. 1. Structural investigation, J. Phys. 49, 319–332 (1988)
255. C. Michon, G. Cuvelier, P. Relkin et al.: Influence of thermal history on the stability of gelatin gels, Int. J. Biol. Macromol. 20, 259–264 (1997)
256. J.Y. Chatellier, D. Durand, J.R. Emery: Critical helix content in gelatin gels, Int. J. Biol. Macromol. 7, 311–314 (1985)
257. I. Pezron, M. Djabourov, J. Leblond: Conformation of gelatin chains in aqueous-solutions. 1. A light and small-angle neutron-scattering study, Polymer 32, 3201–3210 (1991)
258. A. Bigi, G. Cojazzi, S. Panzavolta et al.: Mechanical and thermal properties of gelatin films at different degrees of glutaraldehyde crosslinking, Biomaterials 22, 763–768 (2001)
259. P.V. Kozlov, G.I. Burdygina: The structure and properties of solid gelatin and the principles of their modification, Polymer 24, 651–666 (1983)
260. L.J. Yang, W.Z. Lin, T.J. Yao et al.: Photo-patternable gelatin as protection layers in low-temperature surface micromachinings, Sens. Act. A Phys. 103, 284–290 (2003)

261. J.C. Angus, U. Landau, S.H. Liao et al.: Controlled electroplating through gelatin films, J. Electrochem. Soc. 133, 1152–1160 (1986)
262. R. Fernandes, H.M. Yi, L.Q. Wu et al.: Thermo-biolithography: A technique for patterning nucleic acids and proteins, Langmuir 20, 906–913 (2004)
263. L.J. Yang, Y.C. Ou: The micro patterning of glutaraldehyde (GA)-crosslinked gelatin and its application to cell-culture, Lab Chip 5, 979–984 (2005)
264. P.M. Neumann, B. Zur, Y. Ehrenreich: Gelatin-based sprayable foam as a skin substitute, J. Biomed. Mater. Res. 15, 9–18 (1981)
265. L.H.H. Olde Damink, P.J. Dijkstra, M.J.A. Vanluyn et al.: Glutaraldehyde as a cross-linking agent for collagen-based biomaterials, J. Mater. Sci. Mater. Med. 6, 460–472 (1995)
266. D.P. Speer, M. Chvapil, C.D. Eskelson et al.: Biological effects of residual glutaraldehyde in glutaraldehyde-tanned collagen biomaterials, J. Biomed. Mater. Res. 14, 753–764 (1980)
267. Y.S. Choi, S.R. Hong, Y.M. Lee et al.: Studies on gelatin-containing artificial skin: II. Preparation and characterization of cross-linked gelatin-hyaluronate sponge, J. Biomed. Mater. Res. 48, 631–639 (1999)
268. J.P. Draye, B. Delaey, A. Van de Voorde et al.: In vitro and in vivo biocompatibility of dextran dialdehyde cross-linked gelatin hydrogel films, Biomaterials 19, 1677–1687 (1998)
269. W.H. Chang, Y. Chang, P.H. Lai et al.: A genipin-crosslinked gelatin membrane as wound-dressing material: in vitro and in vivo studies, J. Biomater. Sci. Polym. Ed. 14, 481–495 (2003)
270. L.T. Lim, Y. Mine, M.A. Tung: Barrier and tensile properties of transglutaminase cross-linked gelatin films as affected by relative humidity, temperature, and glycerol content, J. Food Sci. 64, 616–622 (1999)
271. A. Mizuno, M. Mitsuiki, M. Motoki: Effect of transglutaminase treatment on the glass transition of soy protein, J. Agric. Food Chem. 48, 3286–3291 (2000)
272. A. Paguirigan, D.J. Beebe: Gelatin based microfluidic devices for cell culture, Lab Chip 6, 407–413 (2006)
273. A.L. Paguirigan, D.J. Beebe: Protocol for the fabrication of enzymatically crosslinked gelatin microchannels for microfluidic cell culture, Nat. Protocols 2, 1782–1788 (2007)
274. WA Little: Microminiature refrigeration, Rev. Sci. Instrum. 55, 661–680 (1984)
275. E. Ermantraut, K. Wohlfart, W. Tichelaar: Perforated support foils with pre-defined hole size, shape and arrangement, Ultramicroscopy 74, 75–81 (1998)
276. R. Delille, M.G. Urdaneta, S.J. Moseley et al.: Benchtop polymer MEMS, J. Microelectromech. Syst. 15, 1108–1120 (2006)
277. J.L. Tan, W. Liu, C.M. Nelson et al.: Simple approach to micropattern cells on common culture substrates by tuning substrate wettability, Tissue Eng. 10, 865–872 (2004)
278. M.D. Tang, A.P. Golden, J. Tien: Molding of three-dimensional microstructures of gels, J. Am. Chem. Soc. 125, 12988–12989 (2003)
279. M. Kumar: A review of chitin and chitosan applications, React. Funct. Polym. 46, 1–27 (2000)
280. L.Q. Wu, A.P. Gadre, H.M. Yi et al.: Voltage-dependent assembly of the polysaccharide chitosan onto an electrode surface, Langmuir 18, 8620–8625 (2002)
281. L.Q. Wu, H.M. Yi, S. Li et al.: Spatially selective deposition of a reactive polysaccharide layer onto a patterned template, Langmuir 19, 519–524 (2003)
282. T.H. Ang, F.S.A. Sultana, D.W. Hutmacher et al.: Fabrication of 3D chitosan-hydroxyapatite scaffolds using a robotic dispensing system, Mater. Sci. Eng. C Biomim. Supramol. Syst. 20, 35–42 (2002)
283. S.T. Koev, M.A. Powers, H. Yi et al.: Mechano-transduction of DNA hybridization and dopamine oxidation through electrodeposited chitosan network, Lab Chip 7, 103–111 (2007)
284. L.Q. Wu, M.K. McDermott, C. Zhu et al.: Mimicking biological phenol reaction cascades to confer mechanical function, Adv. Funct. Mater. 16, 1967–1974 (2006)
285. H.M. Yi, L.Q. Wu, W.E. Bentley et al.: Biofabrication with chitosan, Biomacromolecules 6, 2881–2894 (2005)

286. K. Ono, Y. Saito, H. Yura et al.: Photocrosslinkable chitosan as a biological adhesive, J. Biomed. Mater. Res. 49, 289–295 (2000)
287. J.M. Karp, Y. Yeo, W.L. Geng et al.: A photolithographic method to create cellular micropatterns, Biomaterials 27, 4755–4764 (2006)
288. J.C. Cheng, A.P. Pisano: Photolithographic process for integration of the biopolymer chitosan into micro/nano structures, J. Microelectromech. Syst. 17, 402–409 (2008)
289. L. Tan, Y.P. Kong, S.W. Pang et al.: Imprinting of polymer at low temperature and pressure, J. Vac. Sci. Technol. B 22, 2486–2492 (2004)
290. I. Park, J. Cheng, A.P. Pisano et al.: Low temperature, low pressure nanoimprinting of chitosan as a biomaterial for bionanotechnology applications, Appl. Phys. Lett. 90 (2007) (article number 093902)
291. K.C. Popat, T.A. Desai: Poly(ethylene glycol) interfaces: An approach for enhanced performance of microfluidic systems, Biosens. Bioelectron. 19, 1037–1044 (2004)
292. K.C. Popat, R.W. Johnson, T.A. Desai: Characterization of vapor deposited poly (ethylene glycol) films on silicon surfaces for surface modification of microfluidic systems, J. Vac. Sci. Technol. B 21, 645–654 (2003)
293. M.Q. Zhang, T. Desai, M. Ferrari: Proteins and cells on PEG immobilized silicon surfaces, Biomaterials 19, 953–960 (1998)
294. S. Sharma, R.W. Johnson, T.A. Desai: Ultrathin poly(ethylene glycol) films for silicon-based microdevices, Appl. Surf. Sci. 206, 218–229 (2003)
295. J.H. Lee, H.B. Lee, J.D. Andrade: Blood compatibility of polyethylene oxide surfaces, Prog. Polym. Sci. 20, 1043–1079 (1995)
296. J.M. Harris: Poly(ethylene glycol) Chemistry: Biotechnical and Biomedical Applications (Plenum Press, New York, NY, 1992)
297. M. Zhang, M. Ferrari: Hemocompatible polyethylene glycol films on silicon, Biomed. Microdev. 1, 81–89 (1998)
298. M. Amiji, K. Park: Prevention of protein adsorption and platelet-adhesion on surfaces by peo ppo peo triblock copolymers, Biomaterials 13, 682–692 (1992)
299. D. Gingell, N. Owens, P. Hodge et al.: Adsorption of a novel fluorescent derivative of a poly(ethylene oxide)/poly(butylene oxide) block-copolymer on octadecyl glass studied by total internal-reflection fluorescence and interferometry, J. Biomed. Mater. Res. 28, 505–513 (1994)
300. C. Maechlingstrasser, P. Dejardin, J.C. Galin et al.: Preadsorption of polymers on glass and silica to reduce fibrinogen adsorption, J. Biomed. Mater. Res. 23, 1385–1393 (1989)
301. D. Gingell, N. Owens: Inhibition of platelet spreading from plasma onto glass by an adsorbed layer of a novel fluorescent-labeled poly(ethylene oxide)/poly(butylene oxide) block-copolymer – characteristics of the exclusion zone probed by means of polystyrene beads and macromolecules, J Biomed. Mater. Res. 28, 491–503 (1994)
302. D.W. Grainger, C. Nojiri, T. Okano et al.: Invitro and exvivo platelet interactions with hydrophilic hydrophobic poly(ethylene oxide)-polystyrene multiblock copolymers, J. Biomed. Mater. Res. 23, 979–1005 (1989)
303. N.F. Owens, D. Gingell, P.R. Rutter: Inhibition of cell-adhesion by a synthetic-polymer adsorbed to glass shown under defined hydrodynamic stress, J. Cell Sci. 87, 667–675 (1987)
304. M.B. Stark, K. Holmberg: Covalent immobilization of lipase in organic-solvents, Biotechnol. Bioeng. 34, 942–950 (1989)
305. Y.C. Tseng, K. Park: Synthesis of photoreactive poly(ethylene glycol) and its application to the prevention of surface-induced platelet activation, J. Biomed. Mater. Res. 26, 373–391 (1992)
306. M. Amiji, K. Park: Surface modification by radiation-induced grafting of Peo/Ppo/Peo triblock copolymers, J. Colloid Interface Sci. 155, 251–255 (1993)
307. K. Emoto, J.M. Harris, J.M. VanAlstine: Grafting poly(ethylene glycol) epoxide to amino-derivatized quartz: Effect of temperature and pH on grafting density, Anal. Chem. 68, 3751–3757 (1996)

308. K.R. Kamath, M.J. Danilich, R.E. Marchant et al.: Platelet interactions with plasma-polymerized ethylene oxide and N-vinyl-2-pyrrolidone films and linear poly(ethylene oxide) layer, J. Biomater. Sci. Polym. Ed. 7, 977–988 (1996)
309. Y.C. Tseng, T. McPherson, C.S. Yuan et al.: Grafting of ethylene glycol-butadiene block-copolymers onto dimethyl-dichlorosilane-coated glass by gamma-irradiation, Biomaterials 16, 963–972 (1995)
310. D. Irimia, J.O.M. Karlsson: Kinetics and mechanism of intercellular ice propagation in a micropatterned tissue construct, Biophys. J. 82, 1858–1868 (2002)
311. Y.C. Wang, M. Ferrari: Surface modification of micromachined silicon filters, J. Mater. Sci. 35, 4923–4930 (2000)
312. K.C. Popat, R.W. Robert, T.A. Desai: Characterization of vapor deposited thin silane films on silicon substrates for biomedical microdevices, Surf. Coat. Technol. 154, 253–261 (2002)
313. A. Revzin, R.G. Tompkins, M. Toner: Surface engineering with poly(ethylene glycol) photolithography to create high-density cell arrays on glass, Langmuir 19, 9855–9862 (2003)
314. A. Khademhosseini, J. Yeh, S. Jon et al.: Molded polyethylene glycol microstructures for capturing cells within microfluidic channels, Lab Chip 4, 425–430 (2004)
315. A. Revzin, R.J. Russell, V.K. Yadavalli et al.: Fabrication of poly(ethylene glycol) hydrogel microstructures using photolithography, Langmuir 17, 5440–5447 (2001)
316. K. Arcaute, B.K. Mann, R.B. Wicker: Stereolithography of three-dimensional bioactive poly(ethylene glycol) constructs with encapsulated cells, Ann. Biomed. Eng. 34, 1429–1441 (2006)
317. P. Kim, H.E. Jeong, A. Khademhosseini et al.: Fabrication of non-biofouling polyethylene glycol micro- and nanochannels by ultraviolet-assisted irreversible sealing, Lab Chip 6, 1432–1437 (2006)
318. K.Y. Suh, J. Seong, A. Khademhosseini et al.: A simple soft lithographic route to fabrication of poly(ethylene glycol) microstructures for protein and cell patterning, Biomaterials 25, 557–563 (2004)
319. A. Khademhosseini, S. Jon, K.Y. Suh et al.: Direct patterning of protein- and cell-resistant polymeric monolayers and microstructures, Adv. Mater. 15, 1995–2000 (2003)
320. R.G. Sanedrin, L. Huang, J.W. Jang et al.: Polyethylene glycol as a novel resist and sacrificial material for generating positive and negative nanostructures, Small 4, 920–924 (2008)
321. A. Tourovskaia, T. Barber, B.T. Wickes et al.: Micropatterns of chemisorbed cell adhesion-repellent films using oxygen plasma etching and elastomeric masks, Langmuir 19, 4754–4764 (2003)
322. P. Sethu, C.H. Mastrangelo: Polyethylene glycol (PEG)-based actuator for nozzle-diffuser pumps in plastic microfluidic systems, Sens. Act. A Phys. 104, 283–289 (2003)
323. K.Y. Suh, Y.S. Kim, H.H. Lee: Capillary force lithography, Adv. Mater. 13, 1386–1389 (2001)
324. Y.S. Kim, K.Y. Suh, H.H. Lee: Fabrication of three-dimensional microstructures by soft molding, Appl. Phys. Lett. 79, 2285–2287 (2001)
325. P. Kim, D.H. Kim, B. Kim et al.: Fabrication of nanostructures of polyethylene glycol for applications to protein adsorption and cell adhesion, Nanotechnology 16, 2420–2426 (2005)
326. Y.S. Kim, H.H. Lee, P.T. Hammond: High density nanostructure transfer in soft molding using polyurethane acrylate molds and polyelectrolyte multilayers, Nanotechnology 14, 1140–1144 (2003)
327. S.J. Choi, P.J. Yoo, S.J. Baek et al.: An ultraviolet-curable mold for sub-100-nm lithography, J. Am. Chem. Soc. 126, 7744–7745 (2004)
328. P.J. Yoo, S.J. Choi, J.H. Kim et al.: Unconventional patterning with a modulus-tunable mold: From imprinting to microcontact printing, Chem. Mater. 16, 5000–5005 (2004)
329. S. Takeuchi, D. Ziegler, Y. Yoshida et al.: Parylene flexible neural probes integrated with microfluidic channels, Lab Chip 5, 519–523 (2005)

330. L. Wolgemuth: Crystal-clear coating covers components, Med. Des. 6, 48–51 (2006)
331. S.G. Eskin, C.D. Armeniades, J.T. Lie et al.: Growth of cultured calf aortic smooth-muscle cells on cardiovascular prosthetic materials, J. Biomed. Mater. Res. 10, 113–122 (1976)
332. A.W. Hahn, D.H. York, M.F. Nichols et al.: Biocompatibility of glow-discharge-polymerized films and vacuum-deposited parylene, Appl. Polym. Symp. 55–64 (1984)
333. G.E. Loeb, A.E. Walker, S. Uematsu et al.: Histological reaction to various conductive and dielectric films chronically implanted in subdural space, J. Biomed. Mater. Res. 11, 195–210 (1977)
334. Y. Kanda, R. Aoshima, A. Takada: Blood compatibility of components and materials in silicon integrated-circuits, Electron. Lett. 17, 558–559 (1981)
335. B.P. Levy, S.L. Campbell, T.L. Rose: Definition of the geometric area of a microelectrode tip by plasma-etching of parylene, IEEE Trans. Biomed. Eng. 33, 1046–1049 (1986)
336. J. Lahann, D. Klee, H. Thelen et al.: Improvement of haemocompatibility of metallic stents by polymer coating, J. Mater. Sci. Mater. Med. 10, 443–448 (1999)
337. T.Y. Chang, V.G. Yadav, S. De Leo et al.: Cell and protein compatibility of parylene-C surfaces, Langmuir 23, 11718–11725 (2007)
338. N. Stark: Literature review: biological safety of parylene C. http://www.devicelink.com/mpb/archive/96/03/004.html (1996) (accessed on 4-25-2003)
339. J.I. Kroschwitz: Kirk-Othmer Encyclopedia of Chemical Technology (Wiley, New York, NY, 1998)
340. J. Lahann: Vapor-based polymer coatings for potential biomedical applications, Polym. Int. 55, 1361–1370 (2006)
341. M. Gazicki-Lipman: Vapor deposition polymerization of para-xylylene derivatives – mechanism and applications, J. Vac. Soc. Jpn. 50, 601–608 (2007)
342. Y.C. Tai: Parylene for MEMS applications, Abstracts of Papers of the American Chemical Society, New York, p. U360 (2003)
343. W.F. Gorham: A new general synthetic method for preparation of linear poly-p-xylylenes, J. Polym. Sci., Polym. Chem. Ed. 4, 3027–3039 (1966)
344. Specialty Coating Systems: Parylene Knowledge > Discovery/History. http://www.scscoatings.com/parylene_knowledge/history.aspx (accessed on 9-9-2008)
345. M. Szwarc: Some remarks on the CH2=benzene=CH2 molecule, Discuss. Faraday Soc. 2, 46–49 (1947)
346. E. Meng, P.Y. Li, Y.C. Tai: Plasma removal of parylene c, J. Micromech. Microeng. 18, 045004 (2008)
347. M.C. Demirel: Emergent properties of spatially organized poly(p-xylylene) films fabricated by vapor deposition, Colloids Surf. A Physicochem. Eng. Asp. 321, 121–124 (2008)
348. M.C. Demirel, E. So, T.M. Ritty et al.: Fibroblast cell attachment and growth on nano-engineered sculptured thin films, J. Biomed. Mater. Res. B Appl. Biomater. 81B, 219–223 (2007)
349. S. Pursel, M.W. Horn, M.C. Demirel et al.: Growth of sculptured polymer submicronwire assemblies by vapor deposition, Polymer 46, 9544–9548 (2005)
350. Specialty Coating Systems, PDS 2010 Labcoter Manual
351. G.E. Loeb, M.J. Bak, M. Salcman et al.: Parylene as a chronically stable, reproducible microelectrode insulator, IEEE Trans. Biomed. Eng. 24, 121–128 (1977)
352. H. Lerner, R.T. Zahradnik, M. Buchbinder: Miniature implantable tantalum tantalum oxide stimulating electrodes, IEEE Trans. Biomed. Eng. 29, 290–292 (1982)
353. G.E. Loeb, R.A. Peck, J. Martyniuk: Toward the ultimate metal microelectrode, J. Neurosci. Methods 63, 175–183 (1995)
354. E.M. Schmidt, M.J. Bak, P. Christensen: Laser exposure of Parylene-C insulated microelectrodes, J. Neurosci. Methods 62, 89–92 (1995)
355. N. Majid, S. Dabral, J.F. Mcdonald: The parylene-aluminum multilayer interconnection system for wafer scale integration and wafer scale hybrid packaging, J. Electron. Mater. 18, 301–311 (1989)

356. P.F. Man, D.K. Jones, C.H. Mastrangelo: Microfluidic Plastic Interconnects for Multi-bioanalysis Chip Modules, Bellingham WA, WA 98227-0010, United States, pp. 196–200 (1997)
357. C.Y. Shih, T.A. Harder, Y.C. Tai: Yield strength of thin-film parylene-C, Microsyst. Technol. Micro Nanosyst. Inf. Storage Process. Syst. 10, 407–411 (2004)
358. X.Q. Wang, Q. Lin, Y.C. Tai: A parylene micro check valve. Proceedings of the IEEE Microelectromechanical Systems Conference, Orlando, FL, pp. 177–182 (1999)
359. J. Xie, Y.N. Miao, J. Shih et al.: Microfluidic platform for liquid chromatography-tandem mass spectrometry analyses of complex peptide mixtures, Anal. Chem. 77, 6947–6953 (2005)
360. X. Yang, J.M. Yang, Y.C. Tai et al.: Micromachined membrane particle filters, Sens. Act. A 73, 184–191 (1999)
361. T.J. Yao, X. Yang, Y.C. Tai: BrF3 dry release technology for large freestanding parylene microstructures and electrostatic actuators, Sens. Act. A Phys. 97–98, 771–775 (2002).
362. E.T. Carlen, C.H. Mastrangelo: Electrothermally activated paraffin microactuators, J. Microelectromech. Syst. 11, 165–174 (2002)
363. E. Meng, P.Y. Li, Y.C. Tai: A biocompatible parylene MEMS thermal flow sensing array, Sens. Act. A Phys. 144, 18–28 (2008)
364. P.J. Chen, D.C. Rodger, R. Agrawal et al.: Implantable micromechanical parylene-based pressure sensors for unpowered intraocular pressure sensing, J. Micromech. Microeng. 17, 1931–1938 (2007)
365. P.J. Chen, D.C. Rodger, E.M. Meng et al.: Surface-micromachined parylene dual valves for on-chip unpowered microflow regulation, J. Microelectromech. Syst. 16, 223–231 (2007)
366. A. Tooker, E. Meng, J. Erickson et al.: Biocompatible parylene neurocages, IEEE Eng. Med. Biol. Mag. 24, 30–33 (2005)
367. T. Stanczyk, B. Ilic, P.J. Hesketh et al.: A microfabricated electrochemical actuator for large displacements, J. Microelectromech. Syst. 9, 314–320 (2000)
368. P.J. Chen, D.C. Rodger, M.S. Humayun et al.: Floating-disk parylene microvalves for self-pressure-regulating flow controls, J. Microelectromech. Syst. 17, 1352–1361 (2008)
369. P.J. Chen, D.C. Rodger, S. Saati et al.: Microfabricated implantable parylene-based wireless passive intraocular pressure sensors, J. Microelectromech. Syst. 17, 1342–1351 (2008)
370. H.S. Noh, P.J. Hesketh, G.C. Frye-Mason: Parylene gas chromatographic column for rapid thermal cycling, J. Microelectromech. Syst. 11, 718–725 (2002)
371. E.E. Hui, C.G. Keller, R.T. Howe: Carbonized Parylene as a Conformal Sacrifical Layer, 1998 Solid-State Sensor and Actuator Workshop, Hilton Head, SC, pp. 256–260 (1998)
372. S. Konishi, M. Liger, T.A. Harder et al.: Parylene-pyrolyzed carbon for MEMS applications. Proceedings of the IEEE Microelectromechanical Systems Conference, Maastricht, The Netherlands, pp. 161–164 (2004)
373. M. Liger, S. Konishi, Y.-C. Tai: Uncooled all-parylene bolometer. Proceedings of the IEEE Microelectromechanical Systems Conference, Maastricht, The Netherlands, pp. 593–596 (2004)
374. Y. Mizuno, M. Liger, Y.-C. Tai: Nanofluidic Flowmeter Using Carbon Sensing Element. Proceedings of the IEEE Microelectromechanical Systems Conference, Maastricht, The Netherlands, pp. 322–325 (2004)
375. M. Herrera-Alonso, T.J. McCarthy: Chemical surface modification of poly(p-xylylene) thin films, Langmuir 20, 9184–9189 (2004)
376. J. Lahann, D. Klee, H. Thelen et al.: Improvement of haemocompatibility of metallic stents by polymer coating, J. Mater. Sci.-Mater. M. 10, 443–448 (1999)
377. T.E. Nowlin, D.F. Smith Jr: Surface Characterization of plasma-treated poly-p-xylylene films, J. Appl. Polym. Sci. 25, 1619–1632 (1980)
378. Specialty Coating Systems: Solvent Resistance of Parylene (2001)
379. R.R.A. Callahan, K.G. Pruden, G.B. Raupp et al.: Downstream oxygen etching characteristics of polymers, J. Vac. Sci. Technol. B 21, 1496–1500 (2003)

380. R.R.A. Callahan, G.B. Raupp, S.P. Beaudoin: Effects of gas pressure and substrate temperature on the etching of parylene-N using a remote microwave oxygen plasma, J. Vac. Sci. Technol. B 19, 725–731 (2001)
381. J.T.C. Yeh, K.R. Grebe: Patterning of poly-para-xylylenes by reactive ion etching, J. Vac. Sci. Technol. A 1, 604–608 (1983)
382. B. Ratier, Y.S. Jeong, A. Moliton et al.: Vapor deposition polymerization and reactive ion beam etching of poly(*p*-xylylene) films for waveguide applications, Opt. Mater. 12, 229–233 (1999)
383. T.E.F.M. Standaert, P.J. Matsuo, X. Li et al.: High-density plasma patterning of low dielectric constant polymers: A comparison between polytetrafluoroethylene, parylene-N, and poly(arylene ether), J. Vac. Sci. Technol. A 19, 435–446 (2001)
384. S. Selvarasah, S.H. Chao, C.L. Chen et al.: A reusable high aspect ratio parylene-C shadow mask technology for diverse micropatterning applications, Sens. Act. A Phys. 145, 306–315 (2008)
385. D. Wright, B. Rajalingam, S. Selvarasah et al.: Generation of static and dynamic patterned co-cultures using microfabricated parylene-C stencils, Lab Chip 7, 1272–1279 (2007)
386. S. Miserendino, Y.C. Tai: Photodefinable silicone MEMS gaskets and O-rings for modular microfluidic systems. Proceedings of the IEEE Microelectromechanical Systems Conference, Kobe, Japan, pp. 369–372 (2007)
387. R. Sabeti, E.M. Charlson, E.J. Charlson: Selective deposition of parylene, Polym. Commun. 30, 166–169 (1989)
388. M. Gazicki, G. Surendran, W. James et al.: Polymerization of para-xylylene derivatives (parylene polymerization) 2. Heat-effects during deposition of parylene-C at different temperatures, J. Polym. Sci. A Polym. Chem. 23, 2255–2277 (1985)
389. P. Kramer, A.K. Sharma, E.E. Hennecke et al.: Polymerization of para-xylylene derivatives (parylene polymerization) 1. Deposition kinetics for parylene-n and parylene-c, J. Polym. Sci., Polym. Chem. Ed. 22, 475–491 (1984)
390. S.W. Youn, H. Goto, M. Takahashi et al.: Thermal imprint process of parylene for MEMS applications, Key Eng. Mater. 340–341, 931–936 (2007)
391. H.S. Noh, Y. Huang, P.J. Hesketh: Parylene micromolding, a rapid and low-cost fabrication method for parylene microchannel, Sens. Act. B Chem. 102, 78–85 (2004)
392. H. Kim, K. Najafi: Characterization of low-temperature wafer bonding using thin-film Parylene, J. Microelectromech. Syst. 14, 1347–1355 (2005)
393. H.S. Noh, K.S. Moon, A. Cannon et al.: Wafer bonding using microwave heating of parylene intermediate layers, J. Micromech. Microeng. 14, 625–631 (2004)
394. X.Q. Wang, X. Yang, K. Walsh et al.: Gas-phase silicon etching with bromine trifluoride, Technical Digest. International Conference on Solid-State Sensors and Actuators, Chicago, IL, pp. 1505–1508 (1997)
395. L. Licklider, X.Q. Wang, A. Desai et al.: A micromachined chip-based electrospray source for mass spectrometry, Anal. Chem. 72, 367–375 (2000)
396. M. Liger, D.C. Rodger, Y.C. Tai: Robust parylene-to-silicon mechanical anchoring. Proceedings of the IEEE Microelectromechanical Systems Conference, Kyoto, Japan, pp. 602–605 (2003)
397. C.Y. Shih, Y. Chen, Y.C. Tai: Parylene-strengthened thermal isolation technology for microfluidic system-on-chip applications, Sens. Act. A Phys. 126, 270–276 (2006)
398. J. Erickson, A. Tooker, Y.C. Tai et al.: Caged neuron MEA: A system for long-term investigation of cultured neural network connectivity, J. Neurosci. Meth. 175, 1–16 (2008)
399. W. Li, D.C. Rodger, E. Meng et al.: Flexible parylene packaged intraocular coil for retinal prostheses. Proceedings of 2006 International Conference on Microtechnologies in Medicine and Biology, Okinawa, Japan, pp. 105–108 (2006)

400. E.T.T. Jones, O.M. Chyan, M.S. Wrighton: Preparation and characterization of molecule-based transistors with a 50-nm source-drain separation with use of shadow deposition techniques – toward faster, more sensitive molecule-based devices, J. Am. Chem. Soc. 109, 5526–5528 (1987)
401. J. Madden: Conducting polymer actuators, Massachusetts Institute of Technology (2000)
402. P. Du, X. Lin, X. Zhang: Development of conducting polymer micro cantilever for conductivity measurement, Proceeding of ASME International Mechanical Engineering Congress and Exposition (IMECE '08), Boston, MA, 67986 (2008)
403. T.A. Skotheim, R.L. Elsenbaumer, J.R. Reynolds: Handbook of Conducting Polymers (CRC Press, Boca Raton, FL, 1998)
404. R.H. Baughman: Conducting polymer artificial muscles, Synth. Met. 78, 339–353 (1996)
405. T.F. Otero, H. Grande, J. Rodríuez: Reversible electrochemical reactions in conducting polymers: A molecular approach to artificial muscles, J. Phys. Org. Chem. 9, 381–386 (1996)
406. E. Smela: Conjugated polymer actuators, MRS Bull. 33, 197–204 (2008)
407. J.D.W. Madden, N.A. Vandesteeg, P.A. Anquetil et al.: Artificial muscle technology: Physical principles and naval prospects, IEEE J. Ocean. Eng. 29, 706–728 (2004)
408. G.M. Spinks, E. Smela: Conjugated Polymers for Microelectromechanical and Other Microdevices. In Conjugated Polymers: Processing and Applications (Skotheim, T.A., Reynolds, J. (Eds.) CRC Press, Boca Raton, FL, 2006)
409. J.D.W. Madden, P.G.A. Madden, I.W. Hunter: Polypyrrole actuators: Modeling and performance. Proceedings of the SPIE – International Society of Optical Engineering, Newport Beach, CA, pp. 72–83 (2001)
410. A. Della Santa, D. De Rossi, A. Mazzoldi: Characterization and modelling of a conducting polymer muscle-like linear actuator, Smart Mater. Struct. 6, 23–34 (1997)
411. Q. Pei, O. Inganaes: Electrochemical applications of the bending beam method. 1. Mass transport and volume changes in polypyrrole during redox, J. Phys. Chem. 96, 10507–10514 (1992)
412. G. Alici, B. Mui, C. Cook: Bending modeling and its experimental verification for conducting polymer actuators dedicated to manipulation applications, Sens. Act. A Phys. 126, 396–404 (2006)
413. S. Hara, T. Zama, A. Ametani et al.: Enhancement in electrochemical strain of a polypyrrole-metal composite film actuator, J. Mater. Chem. 14, 2724–2725 (2004)
414. G.M. Spinks, et al.: Ionic liquids and polypyrrole helix tubes: bringing the electronic Braille screen closer to reality. In Smart Structures and Materials 2003: Electroactive Polymer Actuators and Devices (EAPAD), San Diego, CA, pp. 372–380 (2003)
415. E. Smela, O. Inganas, I. Lundstrom: Controlled folding of Micrometer-size structures, Science 268, 1735–1738 (1995)
416. K. Kaneto, M. Kaneko, Y. Min et al.: Artificial muscle – Electromechanical actuators using polyaniline films, Synth. Met. 71, 2211–2212 (1995)
417. E. Smela: Conjugated polymer actuators for biomedical applications, Adv. Mater. 15, 481–494 (2003)
418. W. Lu, A.G. Fadeev, B. Qi et al.: Use of ionic liquids for pi-conjugated polymer electrochemical devices, Science 297, 983–987 (2002)
419. Geoffrey M. Spinks, G.G. Wallace, L. Liu et al.: Conducting polymers electromechanical actuators and strain sensors, Macromol. Symp. 192, 161–170 (2003)
420. D. Chinn, J. Janata: SPIN-cast thin-films of polyaniline, Thin Solid Films 252, 145–151 (1994)
421. R.L. Elsenbaumer, K.Y. Jen, R. Oboodi: Processible and environmentally stable conducting polymers, Synth. Met. 15, 169–174 (1986)
422. E.W.H. Jager, E. Smela, O. Inganas: Microfabricating conjugated polymer actuators, Science 290, 1540–1545 (2000)

423. S. Maw, E. Smela, K. Yoshida et al.: The effects of varying deposition current density on bending behaviour in PPy(DBS)-actuated bending beams, Sens. Act. A Phys. 89, 175–184 (2001)
424. E. Smela: Microfabrication of PPy microactuators and other conjugated polymer devices, J. Micromech. Microeng. 1–18 (1999)
425. M. Christophersen, B. Shapiro, E. Smela: Characterization and modeling of PPy bilayer microactuators: Part 1. Curvature, Sens. Act. B Chem. 115, 596–609 (2006)
426. N.H. Hendricks: Low dielectric constant materials for IC intermetal dielectric applications: A status report on the leading candidates. Proceedings of the Materials Research Society Symposium, Boston, MA, pp. 3–14 (1997)
427. M.E. Mills, P. Townsend, D. Castillo et al.: Benzocyclobutene (DVS-BCB) polymer as an interlayer dielectric (ILD) material, Microelectron. Eng. 33, 327–334 (1997)
428. A. Modafe, N. Ghalichechian, B. Kleber et al.: Electrical characterization of benzocyclobutene polymers for electric micromachines, IEEE Trans. Device Mater. Reliab. 4, 495–508 (2004)
429. N. Ghalichechian, A. Modafe, R. Ghodssi et al.: Integration of benzocyclobutene polymers and silicon micromachined structures using anisotropic wet etching, J. Vac. Sci. Technol. B 22, 2439–2447 (2004)
430. P.B. Chinoy, J. Tajadod: Processing and microwave characterization of multilevel interconnects using benzocyclobutene dielectric, IEEE Trans. Compon. Hybrids Manuf. Technol. 16, 714–719 (1993)
431. A.J.G. Strandjord, R.H. Heistand, J.N. Bremmer et al.: Photosensitive-BCB on laminate technology (MCM-LD). Proceedings – Electronic Components and Technology Conference, Washington, DC, pp. 374–386 (1994)
432. D. Burdeaux, P. Townsend, J. Carr et al.: Benzocyclobutene (Bcb) dielectrics for the fabrication of high-density, thin-film multichip modules, J. Electron. Mater. 19, 1357–1364 (1990)
433. L.A. Keser, R. Bajaj, T. Fang: Redistribution and bumping of a high I/O device for flip chip assembly, IEEE Trans. Adv. Packaging 23, 3–8 (2000)
434. D.T. Price, R.J. Gutmann, S.P. Murarka: Damascene copper interconnects with polymer ILDs, Thin Solid Films 308, 523–528 (1997)
435. J.B. Lee, J. English, C.H. Ahn et al.: Planarization techniques for vertically integrated metallic MEMS on silicon foundry circuits, J. Micromech. Microeng. 7, 44–54 (1997)
436. R. Carrillo-Ramirez, R.W. Jackson: A technique for interconnecting millimeter wave integrated circuits using BCB and bump bonds, IEEE Microwave Wireless Compon. Lett. 13, 196–198 (2003)
437. J. Im, E.O. Shaffer, R. Peters et al.: Physical and mechanical properties determination of photo-BCB-based thin films. Proceedings of the International Symposium on Microelectronics, Minneapolis, MN, pp. 168–175 (1996)
438. J.-h. Im, E.O. Shaffer Ii, T. Stokich Jr et al.: On the mechanical reliability of Photo-BCB-based thin film dielectric polymer for electronic packaging applications, J. Electron. Packaging, Trans. ASME 122, 28–33 (2000)
439. J.T. Beechinor, E. McGlynn, M. Oreilly et al.: Optical characterisation of thin film benzocyclobutene (BCB) based polymers, Microelectron. Eng. 33, 363–368 (1997)
440. A. Modafe, N. Ghalichechian, A. Frey et al.: Microball-bearing-supported electrostatic micromachines with polymer dielectric films for electromechanical power conversion, J. Micromech. Microeng. 16, S182–S190 (2006)
441. N. Ghalichechian, A. Modafe, M.I. Beyaz et al.: Design, fabrication, and characterization of a rotary micromotor supported on microball bearings, J. Microelectromech. Syst. 17, 632–642 (2008)
442. N. Ghalichechian, A. Modafe, J.H. Lang et al.: Dynamic characterization of a linear electrostatic micromotor supported on microball bearings, Sens. Act. A Phys. 136, 496–503 (2007)

443. K. Lee, J.P. He, R. Clement et al.: Biocompatible benzocyclobutene (BCB)-based neural implants with micro-fluidic channel, Biosens. Bioelectron. 20, 404–407 (2004)
444. P.E. Garrou, R.H. Heistand, M.G. Dibbs et al.: Rapid thermal curing of Bcb dielectric, IEEE Trans. Compon. Hybrids Manuf. Technol. 16, 46–52 (1993)
445. J. Bryzek, K. Petersen, W. McCulley: Micromachines on the March, IEEE Spectrum 31, 20–31 (1994)
446. A. Modafe, N. Ghalichechian, M. Powers et al.: Embedded benzocyclobutene in silicon: An integrated fabrication process for electrical and thermal isolation in MEMS, Microelectron. Eng. 82, 154–167 (2005)
447. S.Y. Kook, J.M. Snodgrass, A. Kirtikar et al.: Adhesion and reliability of polymer/inorganic interfaces, J. Electron. Packaging 120, 328–335 (1998)
448. S. Seok, N. Rolland, P.A. Rolland: Packaging methodology for RF devices using a BCB membrane transfer technique, J. Micromech. Microeng. 16, 2384–2388 (2006)
449. S.J. Woltman, G.D. Jay, G.P. Crawford: Liquid-crystal materials find a new order in biomedical applications, Nat. Mater. 6, 929–938 (2007)
450. C.G.L. Khoo, B. Brox, R. Norrhede et al.: Effect of copper lamination on the rheological and copper adhesion properties of a thermotropic liquid crystalline polymer used in PCB applications, IEEE Trans. Compon., Packaging, Manuf. Technol. C: Manuf. 20, 219–226 (1997)
451. E.C. Culbertson: New laminate material for high performance PCBs: liquid crystal polymer copper clad films. Proceedings Electronic Components and Technology Conference, Las Vegas, NV, pp. 520–523 (1995)
452. X.F. Wang, J. Engel, C. Liu: Liquid crystal polymer (LCP) for MEMS: Processes and applications, J. Micromech. Microeng. 13, 628–633 (2003)
453. H.A. Broadbent, S.Z. Ivanov, D.P. Fries: Fabrication of a LCP-based conductivity cell and resistive temperature device via PCB MEMS technology, J. Micromech. Microeng. 17, 722–729 (2007)
454. J.N. Palasagaram, R. Ramadoss: MEMS-capacitive pressure sensor fabricated using printed-circuit-processing techniques, IEEE Sens. J. 6, 1374–1375 (2006)
455. Z. Illyefalvi-Vitez: Laser processing of adhesives and polymeric materials for micro-electronics packaging applications. Proceedings International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing, Espoo, Finland, pp. 289–295 (2000)
456. E.E. Guzzo, J.S. Preston: Laser-ablation as a processing technique for metallic and polymer layered structures, IEEE Trans. Semicond. Manuf. 7, 73–78 (1994)
457. B. Gu, J.M. Morrison: Cost effective small via generation – the laser solution. Proceedings of the IEEE Multi-Chip Module Conference, Santa Cruz, CA, pp. 212–216 (1995)
458. J. Schroers, Q. Pham, A. Desai: Thermoplastic forming of bulk metallic glass – A technology for MEMS and microstructure fabrication, J. Microelectromech. Syst. 16, 240–247 (2007)
459. D.M. Bryce: Plastic Injection Molding: Manufacturing Startup and Management (Society of Manufacturing Engineers, Dearborn, MI, 1999)
460. D.V. Rosato, D.V. Rosato, M.G. Rosato: Injection Molding Handbook (Kluwer, Boston, MA, 2000)
461. B.A. Davis: Compression Molding (Hanser Publishers, Munich, Cincinnati Hanser Gardner Publications, 2003)
462. A.I. Isayev: Injection and Compression Molding Fundamentals (Dekker, New York, NY, 1987)
463. MicroChem Corporation. http://www.microchem.com/ (accessed on 9-9-2008)
464. V. Kudryashov, X.C. Yuan, W.C. Cheong et al.: Grey scale structures formation in SU-8 with e-beam and UV, Microelectron Eng. 67–68, 306–311 (2003)
465. Specialty Coating Systems. http://www.scscoatings.com/ (accessed on 9-9-2008)
466. HD MicroSystems, Polyimides for Microelectronics Product Selector Guide
467. G. Genolet, M. Despont, P. Vettiger et al.: All-photoplastic, soft cantilever cassette probe for scanning force microscopy, J. Vac. Sci. Technol. B 18, 617–620 (2000)

468. H.S. Khoo, K.K. Liu, F.G. Tseng: Mechanical strength and interfacial failure analysis of cantilevered SU-8 microposts, J. Micromech. Microeng. 13, 822–831 (2003)
469. K. Lian, Z.-g. Ling, C. Liu: Thermal stability of SU-8 Fabricated microstructures as a function of photo initiator and exposure doses. Proceedings of SPIE – The International Society for Optical Engineering, San Jose, CA, pp. 208–212 (2003)
470. M. Hopcroft, T. Kramer, G. Kim et al.: Micromechanical testing of SU-8 cantilevers, Fatigue Fract. Eng. Mater. Struct. 28, 735–742 (2005)
471. J.P.F. Spratley, M.C.L. Ward, P.S. Hall: Bending characteristics of SU-8, Micro Nano Lett. 2, 20–23 (2007)
472. C. Luo, T.W. Schneider, R.C. White et al.: A simple deflection-testing method to determine Poisson's ratio for MEMS applications, J. Micromech. Microeng. 13, 129–133 (2003)

Chapter 5
Additive Processes for Piezoelectric Materials: Piezoelectric MEMS

Ronald G. Polcawich and Jeffrey S. Pulskamp

Abstract Piezoelectricity has been underutilized in the MEMS world. Fabrication process compatibility, complexity, and the limited availability of repeatable and reliable piezoelectric thin films have limited the incorporation of piezoelectric thin films in MEMS. Advances in materials processing and a move toward system-in-package (SIP) concepts have pushed piezoelectric thin film devices toward mainstream acceptance. The advances in piezoelectric aluminum (AlN) thin films for film bulk acoustic resonators (FBAR) [1] have encouraged using piezoelectric transduction as an alternative to electrostatic actuation in RF (radio frequency) MEMS applications. The FBAR devices have tremendous performance advantages and smaller size over conventional bulk-machined quartz surface acoustic wave devices (SAWs) making them ideal for cellular phones. To date, FBAR devices have exceeded the performance of electrostatically driven MEMS resonator and filters operating in cellular phone frequency bands (nominally 0.7–6 GHz). In addition to FBAR technology, piezoelectric actuation/sensing is being examined for a host of applications including RF MEMS, small-scale robotics, resonant mass sensors, and energy harvesting [2, 3]. This chapter focuses on materials selection, material processing, and integration of piezoelectric thin films with conventional MEMS fabrication processes. The first sections introduce the reader to the fundamentals of both ferroelectricity and piezoelectricity. The remainder of the chapter addresses processing of the key ferroelectric and piezoelectric materials, namely lead zirconate titanate (PZT), AlN, and zinc oxide (ZnO).

5.1 Introduction to Piezoelectric Thin Films

Piezoelectric materials enable direct electromechanical coupling either with the development of an electric charge under an applied external stress or the generation

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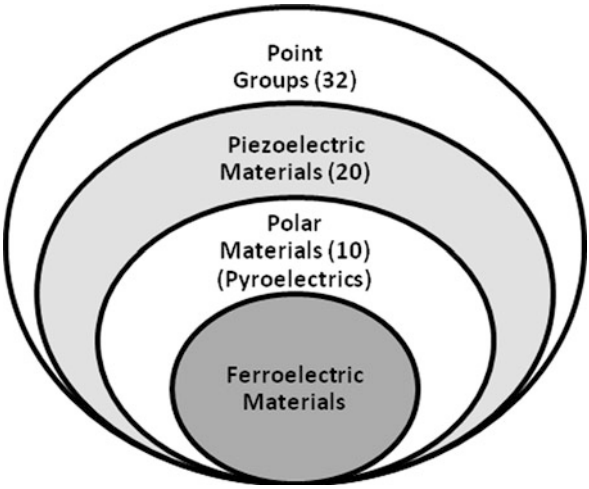


Fig. 5.1 The relationship of piezoelectric materials, polar materials, and ferroelectric materials relative to the 32 crystal point groups

of strain proportional to an applied electric field. This unique material property is limited to a small subset of materials. Examination of the 32 point groups shows that only 20 point groups allow piezoelectricity; see Fig. 5.1 [4]. Of these 20, ten of the point groups can be classified as polar materials in which an electric dipole moment can be present in the absence of an electric field (i.e., spontaneous polarization). The spontaneous polarization also changes with temperature enabling pyroelectricity. In addition, there is a special class of materials in which the spontaneous polarization can be permanently reoriented between crystallographically defined states by applying an electric field. This is the key parameter that distinguishes ferroelectric materials such as (PZT) from strictly polar materials (i.e., quartz, AlN, and ZnO).

The most commonly utilized piezoelectric material is α-quartz because of its stable piezoelectric characteristics and its extremely low acoustic losses [5]. In addition, zero-temperature coefficient properties can be achieved in certain orientations or cuts of quartz, which are extremely important for military and aerospace applications. Quartz-based devices can be found in military and aerospace, research and metrology, industrial, consumer, and automotive applications. Of the variety of applications in which quartz is of use, resonators using both bulk and surface waves are in high demand for everything from low-cost timing devices to high-precision oscillators for global positioning systems. The global market for quartz timekeeping devices is in excess of a billion US dollars (USD) [5]. In contrast to quartz, lead zirconate titanate (PZT) ceramics are used in a variety of actuator applications including positioning actuators, ultrasonic transducers, and inkjet printers to name a few. The extremely large piezoelectric coefficients of PZT make it nearly ideal for these applications. Continued use of piezoelectric materials is expected to increase as the need for increased miniaturization and integration of sensor and actuators continues to be required.

5.1.1 Direct and Converse Piezoelectricity

Piezoelectricity is comprised of two electromechanical responses, a direct effect and a converse effect. The direct effect refers to the generation of charge under the application of an applied stress and is governed by Equation (5.1) where the induced electric displacement (D_i) is proportional to the piezoelectric coefficient (d_{ijk}) and the applied stress (T_{jk}). The converse effect refers to the generation of strain under an applied electric field and is governed by Equation (5.2), where the induced strain (x_{jk}) is proportional to the piezoelectric coefficient and electric field (E_i).

$$D_i = d_{ijk} T_{jk} \tag{5.1}$$

$$x_{jk} = d_{ijk} E_i \tag{5.2}$$

In applications, the direct effect can be used for sensing and energy harvesting in which applied stresses are used to generate surface charges on the piezoelectric (see Fig. 5.2). For actuators, an applied electric field generates a strain in the piezoelectric layer producing flexure in unimorph cantilevers (see Fig. 5.3). The tensor notation for the aforementioned relationships can be simplified using matrix notation where the subscripts i, j, and k having values 1–3 are replaced with the subscripts p and q with values of 1–6 [6]. As a result, d_{ijk} is transformed to d_{ip}. The d_{ip} (strain) and e_{iq} (stress) piezoelectric coefficients are the most useful for thin film sensor and actuator applications and are related by the elastic constant, c^{E}_{pq}, Equation (5.3).

$$e_{iq} = d_{ip} c^{\mathrm{E}}_{pq} \tag{5.3}$$

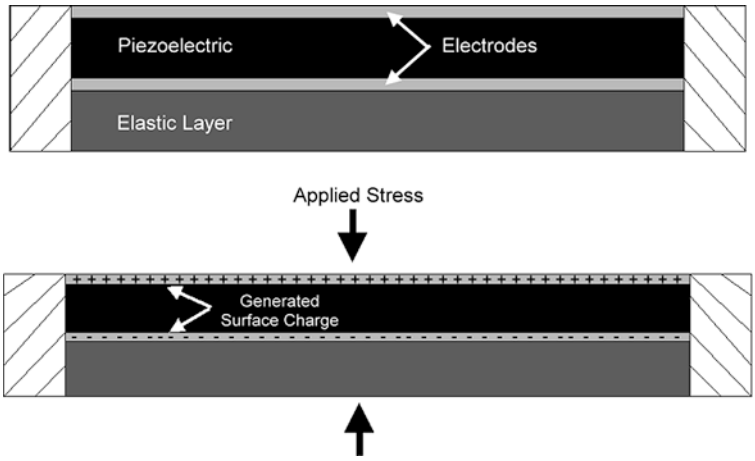


Fig. 5.2 The direct piezoelectric effect applied to a piezoelectric unimorph membrane

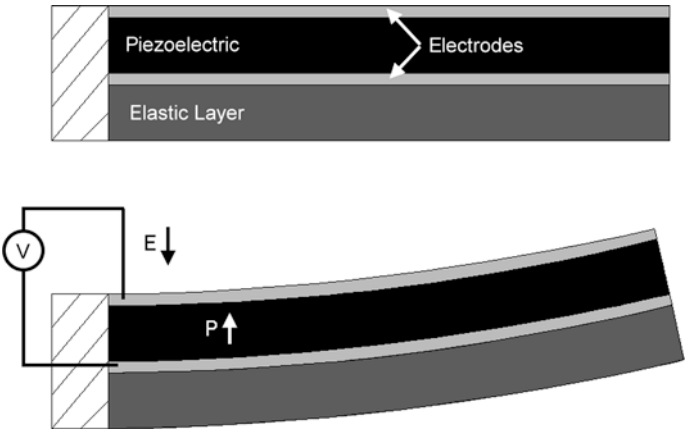


Fig. 5.3 The converse piezoelectric effect applied to a unimorph cantilever

For thin-film composites where the piezoelectric layer is rigidly attached to a supporting elastic layer (i.e., thin film or substrate), the out-of-plane stress X_3 is generally set to zero and the longitudinal strain x_3 varies from a combination of the piezoelectric effect and elastic coupling from the Poisson effect. As a result, an effective thin-film piezoelectric coefficient, $e_{31,f}$, can be related to the common piezoelectric coefficients, d_{31} and e_{31} (see Equation (5.4)) by compensating for the clamping effect experienced by piezoelectric thin films in composite structures [7–9].

$$e_{31,f} = e_{31} - \frac{c_{31}^{E} e_{33}}{c_{33}^{E}} = \frac{d_{31}}{\left(s_{11}^{E} + s_{12}^{E}\right)} \tag{5.4}$$

5.1.2 Materials – Ferroelectrics and Nonferroelectrics

Pure polar materials such as AlN and ZnO do not permit the polarization vector to change orientations relative to the crystal lattice. The polar direction is crystallographically defined along the *c*-axis of the Wurtzite crystal structure (see Fig. 5.4). In addition, these purely polar compounds do not undergo structural phase transitions that lead to the large dielectric and piezoelectric properties near the Curie temperature T_c that is observed in ferroelectric materials. Key advantages of the purely polar materials that are discussed in subsequent sections include the nearly constant ratio of the dielectric constant and piezoelectric coefficient which is extremely important for sensing applications, process compatibility with conventional complex metal-oxide semiconductor (CMOS) processing, absence of depoling or aging of the piezoelectric coefficient, and high acoustic velocities.

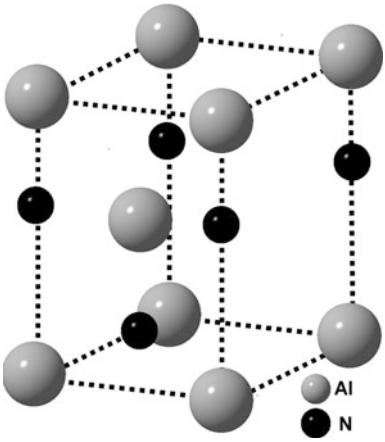


Fig. 5.4 Wurtzite crystal structure of AlN

The identification of ferroelectric behavior in Rochelle salt (potassium sodium tartrate) in 1920 led to numerous research initiatives on this subject. Over the past 80-plus years, considerable progress has been made in topics such as phenomenology, the basis of ferroelectricity, and the development of useful devices. This section reviews some of the fundamental aspects of ferroelectricity.

As stated above, a ferroelectric material is one in which a spontaneous electric dipole moment can be reoriented between crystallographically defined stable states by a realizable electric field (i.e., before dielectric breakdown occurs) [10]. In the perovskite structure, ABO_3 (see Fig. 5.5), where, in general, A is a divalent ion and B is a tetravalent ion, the cubic lattice can undergo distortions at temperatures below the Curie temperature. These distortions result in a shift of the octahedrally coordinated cation from the center of the unit cell. Consequently, a dipole moment is created between the center of negative charge created by the oxygen octahedra and the center of positive charge resulting from the cation sublattice. For lead zirconate titanate ($Pb(Zr_xTi_{1-x})O_3$), the shift in position of the A-site, Pb^{+2} ions, as well as the B-site Zr^{+4} and Ti^{+4} ions contribute to the dipole properties (see Fig. 5.6) [11].

In perovskites, the development of the dipole commonly occurs at a phase transition from a nonpolar paraelectric state to a polar ferroelectric state. In many instances the transition at the Curie temperature (T_c) is associated with a structural change from a centrosymmetric cubic phase to a noncentrosymmetric distorted phase. Additional transition temperatures can exist between two noncentrosymmetric distorted phases (e.g., tetragonal to orthorhombic or orthorhombic to rhombohedral). Figure 5.7 illustrates the lattice distortions that yield the observed structural changes in barium titanate ($BaTiO_3$). Expansion of the cubic unit cell along the [001] direction results in a tetragonal structure whereas an expansion along the [011] results in an orthorhombic structure and an expansion along the [111] direction results in a rhombohedral structure [13].

The polarization generated at T_c can be permanently reoriented into different equilibrium states with an applied electric field, leading to the most recognizable

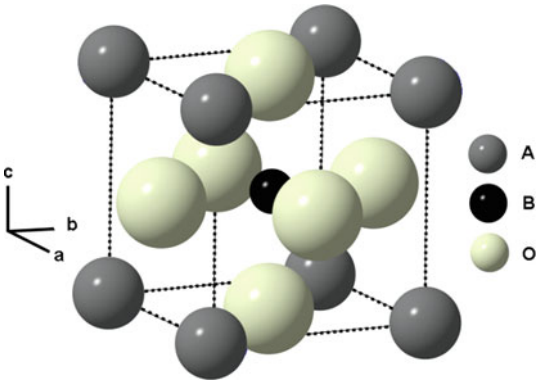


Fig. 5.5 Representation of the cubic (Pm3m) prototype structure of perovskite ABO_3 structure

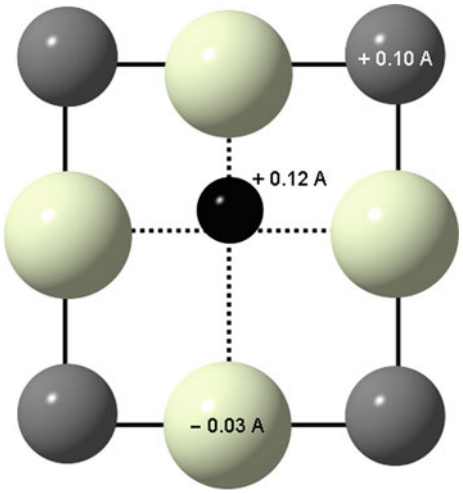


Fig. 5.6 Tetragonal distortion resulting in a positive shift of the A (0.10 Å) and B (+0.12 Å) ions and a slight negative shift of the oxygen ion (–0.03 Å) for $BaTiO_3$ (values taken from [12])

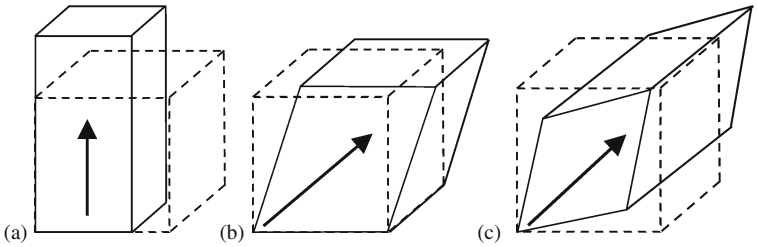


Fig. 5.7 Lattice distortions that occur upon cooling below T_c in perovskites: (**a**) in the tetragonal phase P_s develops along [001] of the original cubic structure, (**b**) in the orthorhombic phase P_s occurs along [011], and (**c**) in the rhombohedral phase P_s develops along [111]. The *dotted cubes* are for the cubic prototype; the *solid lines* show the distorted unit cells of the ferroelectric phases

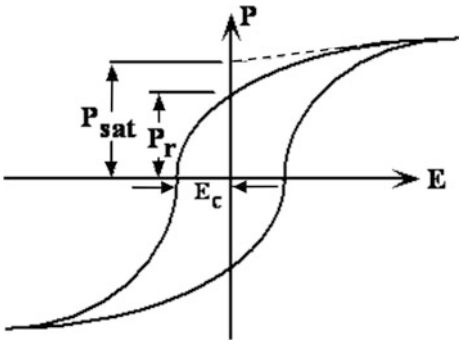


Fig. 5.8 Schematic of the polarization electric field hysteresis loop illustrating the saturation polarization (P_{sat}), remanent polarization (P_r), and coercive field (E_c)

aspect of ferroelectricity: the polarization versus electric field hysteresis loop (see Fig. 5.8). This loop results from the change in net polarization of the material as the amplitude and direction of the applied electric field are changed. The polarization electric field hysteresis loop is a fundamental aspect of ferroelectricity and illustrates the reorientability of the dipole.

The saturation polarization P_{sat} is defined as the linear extrapolation of the high field polarization to zero field and approximates the maximal amount of dipole alignment achieved at zero electric field. The remnant polarization P_r is the retained polarization at zero electric field. For an ideal material, the two remnant polarization values are equal but with opposite signs. The coercive field E_c is the electric field that results in a net zero polarization and has both a positive and negative value corresponding to each location the loop crosses the field axis.

Upon cooling below T_c, a spontaneous polarization develops in each unit cell of the material. All adjacent cells polarized in the same direction (or at least nearly so) comprise a domain. Domains form both to minimize depolarization energy and stresses [13]. These domains have polarization orientations that are dictated by the prototype unit cell and the symmetry elements lost at the phase transformation. For PZT, which can possess either a tetragonal, rhombohedral, or monoclinic ferroelectric phase depending on the Zr:Ti ratio, the polarization direction is along the original <001>, <110>, or <111> axes of the cubic prototype, respectively (see Fig. 5.9) [13, 14]. Tetragonally distorted PZT possesses six equivalent polarization directions, whereas rhombohedral distortions have eight equivalent directions. Domain boundaries (walls) form between adjacent domains of differing polarization directions. These domain walls lie on specific crystallographic planes that minimize the strain across the wall. Tetragonally distorted perovskites possess 90° and 180° domain walls, and rhombohedral perovskites have 71°, 109°, and 180° domain walls [12].

Most ferroelectrics possess a very high relative permittivity (ε_r) or dielectric constant (K). The dielectric constant is defined as the ratio of the material permittivity (ε) to the permittivity of free space (ε_o),

$$\varepsilon_r = K\frac{\varepsilon}{\varepsilon_o} \tag{5.5}$$

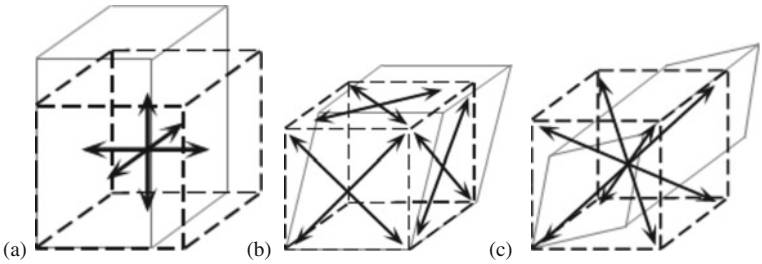


Fig. 5.9 Possible polarization directions relative to the cubic prototype for (**a**) tetragonal perovskite with 6 equivalent <001> directions, (**b**) orthorhombic distortion with 12 equivalent <110> directions, or (**c**) rhombohedral with 8 equivalent <111> directions

Under AC electrical fields, the dielectric constant can be described as a complex number with in-phase and out-of-phase components with respect to the applied voltage. The out-of-phase component is primarily due to dielectric absorption, resistive leakage, and domain wall motion. The dielectric loss, represented as D or tan δ, is the ratio of the out-of-phase and in-phase components [12]. These two parameters are important for determining a material's usefulness as a capacitor (i.e., its ability to store electric charge).

Most solid solutions between $PbZrO_3$ and $PbTiO_3$ possess ferroelectricity and show excellent piezoelectric properties. By varying the Zr^{+4}/Ti^{+4} ratio, both the ferroelectric and piezoelectric properties can be altered significantly. The phase diagram in Fig. 5.10 illustrates the structural changes that occur as a result of composition variations. Substitutions of Zr^{+4} for Ti^{+4} in $PbTiO_3$ reduce the tetragonal distortion and at sufficiently high concentrations cause the structure to transform into a rhombohedral configuration [13]. As seen in the phase diagram, the shift from a tetragonal to a rhombohedral structure occurs at a morphotropic phase boundary (MPB) near the Zr^{+4}/Ti^{+4} ratio of 52/48. A MPB denotes an abrupt structure change with composition at a constant temperature [12]. From phase equilibrium, the MPB is required to be a two-phase mixture of the tetragonal and rhombohedral structures. The presence of both of these structures in this region gives the material an

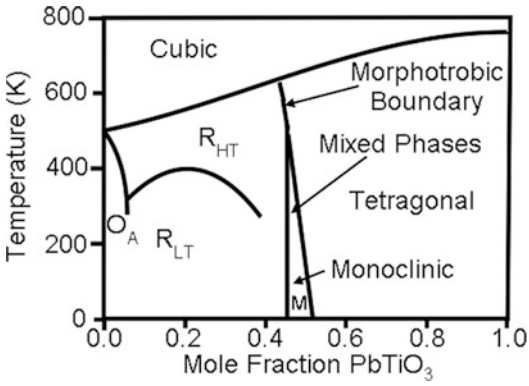


Fig. 5.10 Phase diagram for the lead zirconate–lead titanate solid solution [14] (Reprinted with permission. Copyright 2000 American Physical Society)

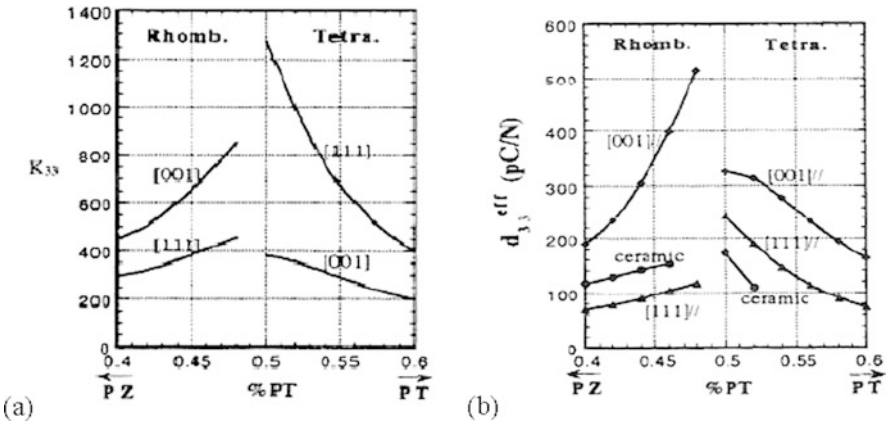


Fig. 5.11 Variation in relative permittivity (K_{33}) and the effective piezoelectric coefficient (d_{33}) as a function of the Zr/Ti ratio and orientation for bulk PZT [15] (Reprinted with permission. Copyright 1998 American Institute of Physics)

increased number of polarization directions. For MPB compositions, the high polarizability results in extremely large dielectric and piezoelectric properties, as seen in Fig. 5.11 [15]. The presence of such large piezoelectric properties near the MPB enables PZT to be an extremely attractive candidate for piezoelectric devices.

5.1.3 Fundamental Design Equations and Models

5.1.3.1 Linear Constitutive Equations of Piezoelectricity

As described in Section 5.1.1, piezoelectricity exhibits the dual electromechanical responses of electric displacement and strain defined by the direct and indirect effects, respectively. The linear piezoelectric constitutive equations for isothermal conditions, utilizing the contracted matrix notation, are defined by

$$D_i = d_{ij}T_j + \varepsilon_{ij}^T E_j \tag{5.6}$$

$$x_{ij} = s_{jk}^{\mathrm{E}} T_k + d_{kj}E_k \tag{5.7}.$$

The constitutive equation for the direct effect, Equation (5.6), defines the electric displacement in terms of the piezoelectric strain coefficient (d_{ij}), the stress (T_{jk}), the permittivity as measured at constant stress (ε_i^T), and the electric field (E_j). For non-piezoelectric materials (i.e., $d_{ij} = 0$), Equation (5.6) reduces to Maxwell's equation relating electric displacement and field. The constitutive equation for the indirect effect, Equation (5.7), defines the generated strain in terms of the piezoelectric strain coefficient (d_{kj}), the electric field (E_k), the stress (T_{kl}), and the elastic compliance as measured at constant electric field (s_{jk}^E). For non-piezoelectric materials (i.e., $d_{kj} = 0$), Equation (5.7) reduces to the generalized Hooke's law for linear elastic materials.

The second term on the right-hand side of Equation (5.7), is the piezoelectrically induced strain in a mechanically free structure and is commonly referred to as the free or actuation strain. For in-plane isotropic piezoelectric materials (PZT, AlN, ZnO), with the compressed matrix notation described above, these may be expressed as

$$\begin{pmatrix} D_1 \\ D_2 \\ D_3 \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & 0 \\ d_{31} & d_{32} & d_{33} & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{pmatrix} + \begin{pmatrix} \varepsilon_{11}^T & 0 & 0 \\ 0 & \varepsilon_{22}^T & 0 \\ 0 & 0 & \varepsilon_{33}^T \end{pmatrix} \begin{pmatrix} E_1 \\ E_2 \\ E_3 \end{pmatrix} \tag{5.8}$$

$$\begin{pmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{pmatrix} = \begin{pmatrix} s_{11} & s_{12} & s_{13} & 0 & 0 & 0 \\ s_{12} & s_{22} & s_{23} & 0 & 0 & 0 \\ s_{13} & s_{23} & s_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{66} \end{pmatrix} \begin{pmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{pmatrix} + \begin{pmatrix} 0 & 0 & d_{31} \\ 0 & 0 & d_{32} \\ 0 & 0 & d_{33} \\ 0 & d_{24} & 0 \\ d_{15} & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} E_1 \\ E_2 \\ E_3 \end{pmatrix} \tag{5.9}$$

5.1.3.2 Electromechanical Coupling Factors

The electromechanical coupling inherent to piezoelectricity leads to a dependence of the permittivity and elastic constants on both the electrical and mechanical boundary conditions. The permittivity and elastic compliance that appear in Equations (5.8) and (5.9) are therefore defined for particular boundary conditions. The difference between the mechanically clamped and free permittivities and the electrically short- and open-circuited elastic constants is a function of the piezoelectric material property known as the electromechanical coupling factor. It is a measure of energy transduction or more specifically, it is the square root of the ratio between stored converted energy to input energy. The coupling factor is useful for comparing various materials, under specific operating conditions, in terms of energy conversion. Equation (5.10) refers to the indirect effect and Equation (5.11) refers to the direct effect and generally these terms are identical.

$$k^2 = \frac{\text{Mechanical Stored Energy}}{\text{Electrical Input Energy}} \tag{5.10}$$

$$k^2 = \frac{\text{Electrical Stored Energy}}{\text{Mechanical Input Energy}} \tag{5.11}$$

$$k_{ij}^2 = \frac{d_{ij}^2}{\varepsilon_0 \varepsilon_i^T s_{ij}^E} \tag{5.12}$$

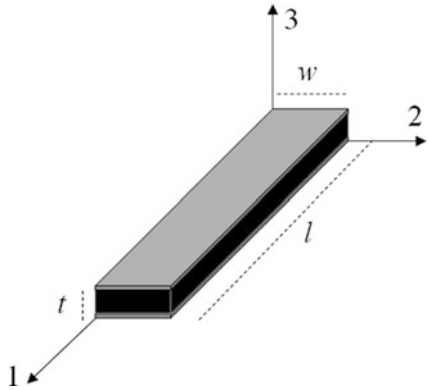


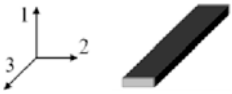
Fig. 5.12 Rectangular piezoelectric bar with parallel plate electrodes on *lw* surfaces

Equation (5.12) provides a general definition of the electromechanical coupling factor for piezoelectrics. This term depends upon those piezoelectric coefficients, permittivities, and elastic constants associated with the transduced energy terms in Equations (5.10) and (5.11) and the nature of the stress state in the material. For instance, consider the bar in Fig. 5.12 of length (l), width (w), and thickness (t). Parallel plate electrodes are placed on the two lw surfaces with the polarization directed along the 3-axis. For such a structure with only nonvanishing stresses along the 1-axis (T_1), an electromechanical coupling factor may be easily defined. The relevant electromechanical coupling factor in this case is k_{31}, referring to the use of the d_{31} piezoelectric mode. Table 5.1 defines additional coupling factors. To illustrate the relationship between Equations (5.10) and (5.12), consider the same free bar of Fig. 5.12 where a constant voltage is applied to the electrodes and the electrodes have a negligible contribution to the stiffness of the bar. The stored mechanical energy is the piezoelectric strain energy density multiplied by the volume of the material (V_p). The piezoelectric strain in this case is the free strain $d_{31}E_3$. The input electrical energy is the electrostatic energy density associated with the capacitance of the piezoelectric multiplied by the volume of the material (V_p). As expressed in Equation (5.13), this energy ratio simplifies to Equation (5.12).

$$k_{31}^2 = \frac{1/2 \frac{x_{\mathrm{avg}}^2}{s_{11}^{\mathrm{E}}} V_\mathrm{p}}{1/2 \varepsilon_\mathrm{o} \varepsilon_{33}^T E_3^2 V_\mathrm{p}} = \frac{1/2 \frac{(d_{31}E_3)^2}{s_{11}^{\mathrm{E}}} V_\mathrm{p}}{1/2 \varepsilon_\mathrm{o} \varepsilon_{33}^T E_3^2 V_\mathrm{p}} = \frac{d_{31}^2}{\varepsilon_\mathrm{o} \varepsilon_{33}^T s_{11}^{\mathrm{E}}} = \frac{d_{31}^2 Y}{\varepsilon_\mathrm{o} \varepsilon_{33}^T} \tag{5.13}$$

A distinction is necessary between the "quasi-static material" coupling factor and the "effective" coupling factor [6]. The quasi-static material coupling factor, discussed earlier, is an intensive material property that only depends upon the anisotropic material properties. The effective coupling factor is a design-specific term usually referred to in the context of resonators or resonant material property measurements. The strain field, under static or quasi-static excitation, is generally uniform. Hence for the previous example, the free strain is equal to the average strain

Table 5.1 Definition of the electromechanical coupling coefficients for elements of different geometries

Coupling factor	Resonator geometry	Boundary conditions	Value
k_{31}		T_1, x_1, x_2, x_3 nonzero	$\frac{d_{31}}{\sqrt{s_{11}^E \varepsilon_o \varepsilon_{33}^T}}$
k_{33}		T_3, x_1, x_2, x_3 nonzero	$\frac{d_{33}}{\sqrt{s_{33}^E \varepsilon_o \varepsilon_{33}^T}}$
K_{15}		T_5 & x_5 nonzero	$\frac{e_{15}}{\sqrt{c_{55}^D \varepsilon_o \varepsilon_{11}^x}}$
k_t(thickness)		x_3, T_1, T_2, T_3 nonzero	$k_{33}\sqrt{\frac{\varepsilon_0 \varepsilon_{33}^T}{c_{33}^D}}$
k_p(planar)		x_1, x_2, x_3, T_1, T_2, nonzero	$k_{31}\sqrt{\frac{2}{1+(s_{12}^E/s_{11}^E)}}$
k_{31}		x_1, x_3, T_1, T_2, nonzero	$\frac{k_{31}}{\sqrt{1-k_{31}^2}}\sqrt{\frac{1-(s_{12}^E/s_{11}^E)}{1+(s_{12}^E/s_{11}^E)}}$

that defines the strain energy density in Equation (5.13). However, under resonant conditions, the strain field is defined by the relevant vibrational modeshape and is therefore nonuniform. Thus defining the ratio of stored and input mechanical and electrical energies requires information regarding the vibrational mode in addition to the elastic, dielectric, and piezoelectric constants. A common definition of the effective coupling factor is given by Equation (5.14). This defines the effective coupling factor in terms of the resonance (f_r) and antiresonance (f_a) frequencies obtained from a one-port measurement of the admittance of a piezoelectric resonator.

$$k_{\text{eff}}^2 = \frac{f_a^2 - f_r^2}{f_a^2} \tag{5.14}$$

5.1.3.3 Influence of Boundary Conditions

As stated earlier, the electromechanical coupling inherent to piezoelectricity leads to a dependence of the permittivity and elastic constants on both the electrical and mechanical boundary conditions. For example, in the case of the direct effect, a constant external stress is applied to an equal potential electroded piezoelectric as depicted in Fig. 5.13. The external stress generates piezoelectrically induced charges

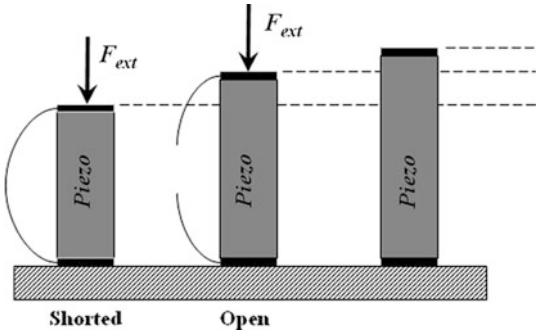


Fig. 5.13 Actuation response under different electrical boundary conditions

on the two electrodes. Under short-circuited electrodes, current is allowed to flow between the electrodes to maintain the equal potentials. Under open-circuit conditions, the charges are constrained to the electrodes and induce an internal electric field within the piezoelectric material. This field, via the indirect piezoelectric effect, actuates the material by providing stresses opposed to the externally applied stress. The material therefore requires a greater external stress for a given deformation under the open circuit condition and hence appears stiffer. Generally, only a limited number of the elastic constants will be influenced by the piezoelectric effect. These modified terms are referred to as piezoelectrically stiffened elastic constants. The permittivity has a similar response under varied mechanical boundary conditions. The ratio between the mechanically clamped and free permittivities and the electrically short- and open-circuited elastic constants are related to the electromechanical coupling factor as defined by Equations (5.15) and (5.16). In the case of high coupling factor thin-film materials like PZT, these values can differ significantly.

$$\frac{\varepsilon_{ij}^{x}}{\varepsilon_{ij}^{T}} = 1 - k_{ij}^{2} \tag{5.15}$$

$$\frac{s_{ij}^{D}}{s_{ij}^{\mathrm{E}}} = 1 - k_{ij}^{2} \tag{5.16}$$

5.1.3.4 Device Configurations

There exist a wide variety of piezoelectric devices and designs for bulk material applications. A small subset of these has been implemented in MEMS device design. Generally, MEMS devices utilize one of two operating modes, defined by the primary piezoelectric coefficients employed. The "d_{33}" mode devices feature interdigitated (IDT) coplanar electrodes that place much of the electric field in the plane and are typically constructed with the active piezoelectric film on a dielectric

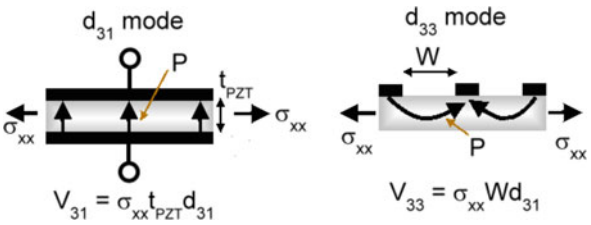


Fig. 5.14 Implementation of d_{31} and d_{33} modes of operation

layer (see Fig. 5.14). The "d_{31}" mode devices are more common and feature parallel plate electrodes that place the electric field through the film thickness (3-axis). This mode exploits the in-plane strain resulting from the d_{31} piezoelectric coefficient. In many bulk actuator designs, such as the multilayer stack actuator, the piezoelectric stress/strain can be used directly. However, given the small strains, device sizes, and process-induced variances involved, piezoelectric MEMS devices almost exclusively utilize some form of displacement amplification. The two most common generic actuator and sensor structures are the unimorph and bimorph, both employing a form of displacement amplification. The unimorph is a structure that features an electroded piezoelectric attached to a structural or elastic layer (see Fig. 5.15). Application of an electric field to the piezoelectric layer leads to flexure of the structure and applied stresses can also lead to a voltage developed across the electrodes. The bimorph (see Fig. 5.15) features two active piezoelectric layers that are operated with opposite sense strain to produce flexure and similarly may be used in sensing mode like the unimorph. Membrane structures are also quite common in piezoelectric MEMS applications and differ from their electrostatic counterparts largely in terms of the optimal electrode design to account for the induced strain nature of operation. Similar to other MEMS transduction techniques, flexural leverage has also been implemented to produce larger displacements in piezoelectric MEMS actuators. This is particularly true for the recently demonstrated in-plane actuator designs [16].

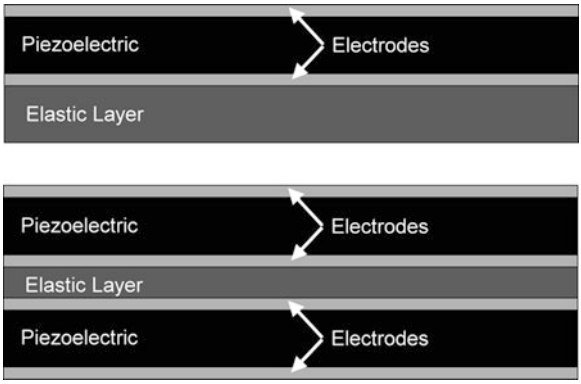


Fig. 5.15 Piezoelectric unimorph (*top*) and bimorph (*bottom*). *Note*: The bimorph can be used without the internal elastic layer and instead using a common electrode for both piezoelectric layers

5.1.3.5 Free Strain and Blocking Force

Before addressing more detailed device models, it is useful to consider the maximum possible strain, displacement, and force that can be generated by a piezoelectric actuator. The free strain Λ represents the piezoelectrically induced strain obtained in a completely mechanically free (zero force condition) material and hence is the maximum attainable strain for a given electric field. Equation (5.17) defines the free strain associated with the d_{31} mode of operation where V is the applied voltage and t_p is the thickness of the piezoelectric layer. In contrast, the term "free displacement" refers to the actuator displacement obtained when the actuator moves in the absence of external forces. The free displacement is therefore the maximum possible nonresonant static displacement for a given actuator design operating under a given electric field. The actual strain, the induced strain, in the piezoelectric layer will generally be less than the free strain due to the influence of the nonpiezoelectric components in the actuator.

$$\Lambda_{31} = d_{31}E_3 = d_{31}\frac{V}{t_\mathrm{p}} \tag{5.17}$$

The "blocking force" represents the piezoelectrically induced force obtained in a completely mechanically clamped (zero strain condition) material and hence is the maximum attainable force for a given electric field. Equation (5.18) defines the actuation force of an actuator associated with the d_{31} mode of operation where YA_p is the extensional stiffness of the piezoelectric layer, Y_p is the elastic modulus of the piezoelectric, and w is the width of the actuated section. For most MEMS structures, the appropriate d_{ij} or e_{ij} coefficient or constant is the "effective" value discussed in Section 5.1.1. This actuation force can be interpreted as the blocking force of the mechanically free piezoelectric layer only. Figure 5.16 illustrates the force-displacement response for typical actuator designs, with linear stiffness properties. For a given electric field, the force-displacement response is defined by the blocking force (zero displacement – x intercept) and the free displacement (zero force – y intercept). Points along the force-displacement curve represent the possible conditions where the actuator performs work against an external load. Increasing the electric field shifts the response up and to the right. The region below the curve defined by the maximum operating field provides the possible force-displacement responses of that particular design. Displacement amplification schemes allow the

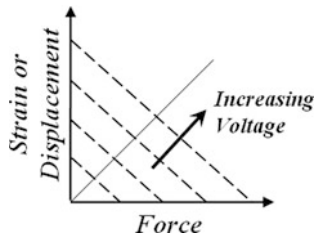


Fig. 5.16 Plot of the force/strain (displacement) relationship for a piezoelectric actuator

designer to trade force and displacement by altering the slope of the curves illustrated in Fig. 5.16. This information is useful in determining whether a given actuator design can drive a given external load.

$$F_{\text{act}} = (YA)_{\text{p}}\,\Lambda_{31} = d_{31,f}Y_{\text{p}}wV \tag{5.18}$$

5.1.3.6 Cantilever Unimorph Model

There is extensive treatment of modeling piezoelectric sensors and actuators available in the literature with varying degrees of accuracy and ease of implementation in design [17–26]. What follows is a model that approximates piezoelectric actuator response that agrees well with finite element analysis and is easily implemented for design purposes. The complexity of the differential equations describing the exact piezoelectric response limits the analytical modeling of these devices to the simplest cases. Although finite element modeling is typically employed for more complex device design, analytical models can still provide valuable design insights. As stated earlier, the unimorph is a structure that features an electroded piezoelectric attached to a structural layer. A simple unimorph actuator bends due to the piezoelectrically induced bending moment acting about its neutral axis (see Fig. 5.17). The actuation force, Equation (5.18), is the resultant of the piezoelectric stresses and acts near the midplane of the piezoelectric layer. The mechanical asymmetry of the structure about the piezoelectric layer, due to the presence of the structural layer, leads to the generation of the actuation moment. In the case of a cantilevered actuator (see Fig. 5.17) the sense of the strain within the piezoelectric layer and the relative position of the line of action of the actuation force with respect to the structure's neutral axis determine the direction of motion. Equation (5.19) defines the piezoelectric actuation moment where h is the distance between the line of action of the actuation force and the relevant neutral axis of the composite actuator.

$$M_{\text{act}} = F_{\text{act}}h = d_{31,f}Y_{\text{p}}wVh \tag{5.19}$$

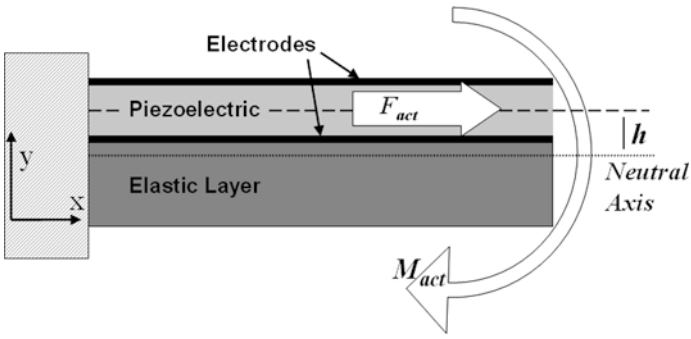


Fig. 5.17 Schematic representative of a thin film piezoelectric unimorph cantilever

Equation (5.20) defines h in terms of the location of the actuation force, y_{Fact}, and the neutral axis referenced to the same arbitrary axis. For most structures, the actuation force is assumed to act at the midplane of the piezoelectric layer.

$$h = y_{\text{Fact}} - \bar{y} \tag{5.20}$$

A convenient method for treating composite structures in flexure is the transformed section method [27]. This method converts the various dissimilar material layers of the composite to a common material with a transformed cross-section. The layers of the new cross-section have altered widths to maintain the same stiffness properties as the previous sections with the beam now of a homogeneous material. This cross-section is mechanically equivalent, in flexure, to the original composite beam but may be treated with conventional analysis. The method permits the determination of the location of the neutral axis, bending stresses, and flexural stiffness properties of the composite structure. An arbitrary material in the composite is chosen as the homogeneous material of the transformed cross-section. The cross-sectional areas of the new layers of a composite comprised of individually isotropic elastic materials are given by Equation (5.21) where w_i and t_i are the original width and thickness, respectively, of the ith layer, Y_i is the modulus of elasticity, and Y_{ref} is the modulus of the reference layer.

$$A_i = w_i t_i \frac{Y_i}{Y_{\text{ref}}} \tag{5.21}$$

The location of the bending neutral axis is given by Equation (5.22) where y_i is the distance from each layer's centroid to some arbitrary reference axis and A_{tot} is the total area of the transformed section.

$$\bar{y} = \frac{\sum A_i y_i}{A_{\text{tot}}} \tag{5.22}$$

In the case of the cantilevered actuator, the equivalent loading of the piezoelectric is that of moment applied at the end of the electroded beam. The linear free displacement of the cantilevered unimorph actuator is described, from Bernoulli–Euler beam theory, by Equation (5.23) where L is the length of the electrode, M_{act} is the bending moment acting on the actuator, and YI_c is the flexural rigidity of the composite actuator.

$$y_{\text{tip}} = \frac{M_{\text{act}} L^2}{2YI_{\text{c}}} = \frac{d_{31,f} Y_{\text{p}} w V h L^2}{2YI_{\text{c}}} \tag{5.23}$$

For many designs, the cantilevered piezoelectric actuator is capable of extremely large displacements. The dominant mechanical nonlinearity in these cases is due to the geometric (small displacement) nonlinearity. Again, for the case of the

cantilevered piezoelectric actuator with a constant end applied moment, this nonlinearity is easily described [28]. Equations (5.24) and (5.25) describe the vertical and horizontal free displacements, respectively.

$$y_{\text{tip}} = \frac{YI_{\text{c}}}{M_{\text{act}}}\left(1 - \cos\left(\frac{M_{\text{act}}L}{YI_{\text{c}}}\right)\right) \tag{5.24}$$

$$x_{\text{tip}} = L - \left(\left(\frac{YI_{\text{c}}}{M_{\text{act}}}\right)\sin\left(\frac{M_{\text{act}}L}{YI_{\text{c}}}\right)\right) \tag{5.25}$$

The flexural rigidity of the composite YI_{c} describes the bending stiffness of the actuator and is the product of the modulus of elasticity and the moment of inertia (second moment of area) of the beam with respect to the neutral axis. Employing the transformed section method and the parallel axis theorem, Equation (5.26) defines YI_{c} where I_i is the moment of inertia of the ith layer about its own centroid and d_i is the distance between the ith layer's centroid and the neutral axis [27].

$$YI_{\text{c}} = Y_{\text{ref}}\left(\sum\left(I_i + A_i d_i^2\right)\right) \tag{5.26}$$

Some problems, such as modal analysis, often require an equivalent modulus of elasticity of the composite structure. In the preceding discussion, use of the transformed section method defined the section properties in terms of an arbitrary homogeneous material. An equivalent modulus of elasticity Y_{c} is defined by Equation (5.27) which applies to structures where the separate layers behave mechanically in parallel.

$$Y_{\text{c}} = \sum\left(Y_i \frac{V_i}{V_{\text{tot}}}\right) \tag{5.27}$$

The method just described agrees well with finite element analysis. Figure 5.18 compares the results of a commercially available FEA package and the analytical model above for a d_{31} mode unimorph cantilever with a PZT active layer operating at 5 V for various ratios of piezoelectric to structural layer. The unimorph (or structure) is a silicon dioxide/platinum/PZT/platinum prismatic beam. The FEA model utilized 3-D ten-node tetrahedral structural and directly coupled field solid elements. The analytical model generally agrees within 1–3% of the finite element analysis. As discussed previously in Section 5.1.1, the film clamping effects in the majority of piezoelectric MEMS structures result in effective $d_{31,f}$ coefficients and $e_{31,f}$ constants. The 1-D analytical model described above utilizes these values directly as these terms directly relate, for example, $d_{31,f}$, the 1-axis strain response in the structure to the electric field applied along the 3-axis. However, in a 2- or 3-D FEA analysis that accommodates the full piezoelectric coefficient matrix, the actual coefficients should be specified using Equation (5.12). The method can also easily be modified to describe the response of bimorph devices.

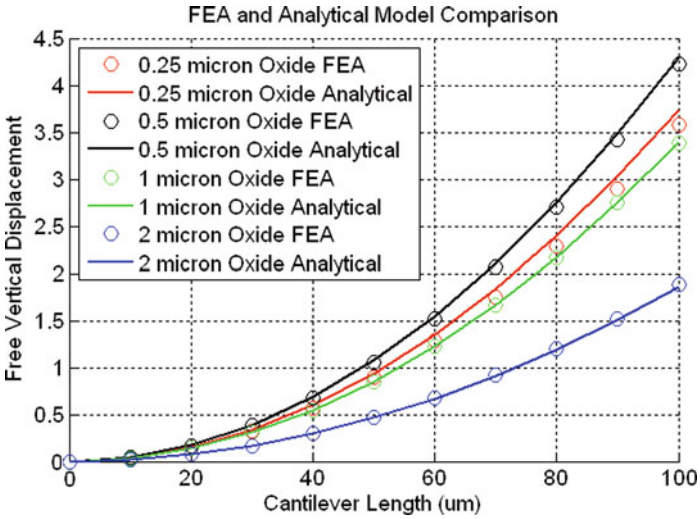


Fig. 5.18 Comparison of FEA and analytical modeling of piezoelectric unimorphs

5.1.3.7 Actuator Force Generation Against External Loads

The force exerted by a piezoelectric actuator depends upon the particular configuration used. Two general cases of interest are of a cantilever exerting a purely axial force against an external load and that of a unimorph or bimorph acting against a normal load. A symmetric composite actuator that is capable of extensional displacements only can be used to drive a MEMS flexure. In this case, the force produced by the actuator is related to the actuation force of the actuator and the ratio of the stiffnesses of the actuator and flexure. Equation (5.28) relates the force exerted by the actuator on a MEMS flexure where k_{ext} is the spring constant of the flexure and L_{act} is the dimension of the actuator along the axis of displacement. The equation illustrates the importance of the actuator stiffness when designing an actuator for driving a specific load. When the actuator is very much stiffer than the flexure, the actuator is unconstrained, the force exerted by the actuator is zero, and no work has been done on the load ($F = 0$). At the other extreme, when the flexure is much stiffer than the actuator, the actuator is completely clamped, the force exerted by the actuator is equal to the blocked force, and again no work has been done ($\Delta x = 0$).

$$F = F_{\text{act}}\left(1 - \frac{k_{\text{act}}}{k_{\text{act}} - k_{\text{ext}}}\right) = d_{31,f} Y_{\text{p}} w V \left(1 - \frac{\sum Y_i A_i}{\sum Y_i A_i - L_{\text{act}} k_{\text{ext}}}\right) \tag{5.28}$$

Similar behavior is observed for a unimorph or bimorph acting against a normal load. This scenario is encountered in most piezoelectric RF MEMS switch designs where a unimorph or bimorph actuator closes a pair of electrical contacts through vertical displacements. The PZT RF MEMS switch design of Polcawich et al. [29]

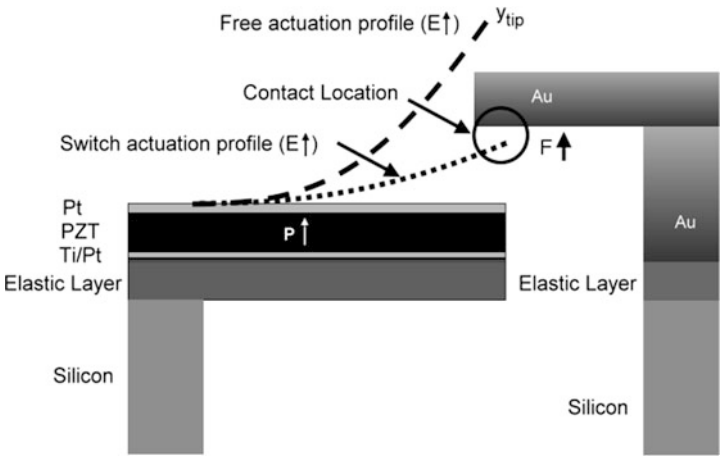


Fig. 5.19 Schematic diagram of contact loading for a piezoelectric switch actuator

features a pair of unimorph actuators mechanically coupled at their free ends to a structure containing the switch contacts. Voltage applied to the actuators vertically displaces the contacts up into a set of contact cantilevers. Figure 5.19 illustrates a simple model of this structure depicting a partially electroded cantilever unimorph with a normal contact force at the switch contact location (this assumes the contact cantilever is rigid; i.e., infinite k_{ext}) [30]. In this case, the force exerted by the actuators can be approximated by the product of the actuator stiffness and the difference between the initial gap and the free displacement. Equation (5.29) relates the force exerted by the actuator on the contact beam for the simple case where the force is exerted at the location of the end of the electrode and g_o is the initial gap between the actuator and the contact.

$$F = k_{act}\left(y_{tip} - g_o\right) = \frac{3d_{31,f}Y_p wVh}{2L_{act}} - \frac{3g_o YI_c}{L_{act}^3} \tag{5.29}$$

5.1.3.8 Piezoelectric Sensing

The preceding discussion described basic models for the behavior of piezoelectric actuators by use of the converse or indirect effect (Equations (5.6) and (5.8)). Piezoelectric materials may also be utilized for sensing and power harvesting applications. The constitutive equation for the direct effect, Equations (5.7) and (5.9), describe the dependence of the electric displacement on external stresses. Piezoelectric sensors generally measure this response either through the voltage developed on open-circuited electrodes or by the current (or charge via integration) through short-circuited electrodes with the aid of additional signal-conditioning electronics. Equation (5.30) describes the charge developed on the electrodes in terms of the electric displacement where the integration is carried out over the entire electrode area of the piezoelectric.

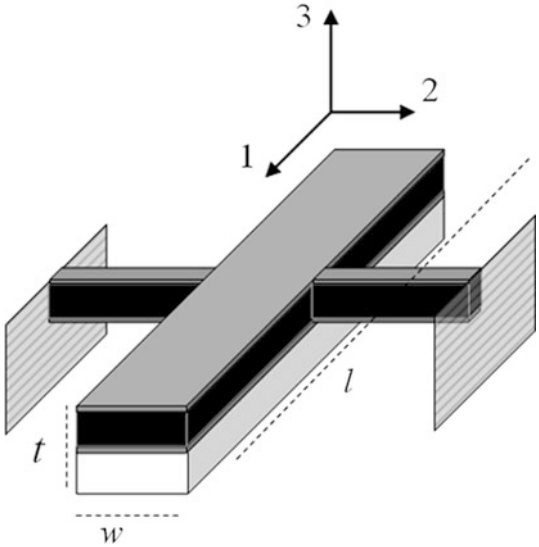


Fig. 5.20 Resonant free–free beam device

$$q = \iint [D_1 \quad D_2 \quad D_3] \begin{bmatrix} dA_1 \\ dA_2 \\ dA_3 \end{bmatrix} \tag{5.30}$$

Consider a large aspect ratio piezoelectric structure vibrating in a length extensional mode (see Fig. 5.20). Equation (5.31) describes the charge developed on the electrodes of such a structure where the only nonzero stress is along the 1-axis that is normal to the plane of the beam structure. Carrying out the integration on the second term on the right-hand side and substituting the definition from electrostatics of voltage in terms of electric field (note the negative sign), we obtain Equation (5.32). The first term is the charge due to the static capacitance of the piezoelectric sensor and the second is the piezoelectrically induced charge due to the external stress. This expression describes the essence of piezoelectric sensor operation.

$$q = -\left(\int_0^w \int_0^L (d_{31}\sigma_x)\, dxdy + \int_0^w \int_0^L \varepsilon_o \varepsilon_{33} E_3 dxdy \right) \tag{5.31}$$

$$q = C_p V - \int_0^w \int_0^L (d_{31}\sigma_x)\, dxdy \tag{5.32}$$

The open circuit voltage is obtained by setting the charge to zero and solving for the voltage across the electrodes (see Equation (5.33)). The short-circuit total

charge (integral of the current over the specified time interval) is obtained by setting the voltage to zero and solving for the charge on the electrodes (see Equation (5.34)). Piezoelectric materials have large but finite electrical resistivities that lead to leakage currents. These leakage currents prevent piezoelectrics from being used to directly sense static stress signals as the piezoelectrically generated signal typically decays rapidly. However, dynamic and resonant modes have been used to sense static stresses.

$$V_{\mathrm{oc}} = \frac{1}{C_{\mathrm{p}}} \int_0^w \int_0^L (d_{31}\sigma_x)\, dxdy \tag{5.33}$$

$$q_{\mathrm{sc}} = \int i_{\mathrm{sc}} dt = -\int_0^w \int_0^L (d_{31}\sigma_x)\, dxdy \tag{5.34}$$

5.1.3.9 Equivalent Circuit Models

It is quite common for piezoelectric devices to be used at resonance. Examples include electromechanical filters for signal processing and ubiquitous quartz crystal microbalance that exploits the large quality factor of quartz. A common technique of measuring the material properties of piezoelectrics involves measurement of the frequency response of a piezoelectric resonator [20]. For such applications, the resonator is conveniently modeled with an equivalent circuit by employing the traditional electromechanical analogy equating force with voltage and velocity with current. A number of equivalent circuits have been developed over the years for piezoelectric devices [31–34]. Perhaps the simplest and most commonly used is the so-called Butterworth–Van Dyke (BVD) model (see Fig. 5.21). In the lumped parameter one-port BVD model, the piezoelectric resonator is represented by a series RLC circuit in parallel with a "shunt" capacitance. This shunt capacitance C_{o} represents the static capacitance of the piezoelectric material between the electrodes. The RLC arm represents electromechanical equivalents of the resonator's mass (L_{m}), compliance (C_{m}), and loss (R_{m}). These are referred to as motional terms as they relate to the dynamic mechanical properties of the resonator. The BVD model is valid for isolated resonances where the circuit parameters are independent of frequency.

The electrical one-port admittance of the BVD equivalent circuit of a resonant piezoelectric device is described by Equation (5.35) where Y_m is the admittance of the motional arm and X_{m} is the motional reactance [35]. Equation (5.36) defines the motional reactance in terms of the motional inductance and motional capacitance. At resonance, the reactance associated with the motional inductance and capacitance cancel each other, giving the admittance as the inverse of the motional resistance plus the admittance of the shunt capacitance. This is typically dominated by the motional resistance term for the vibrational modes of interest.

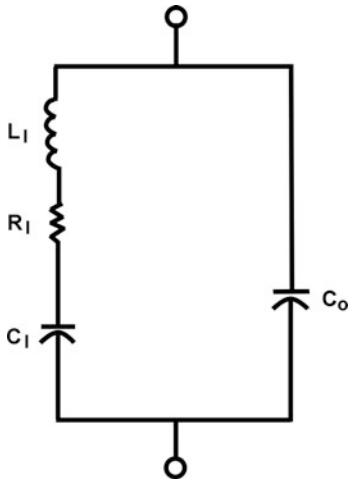


Fig. 5.21 BVD equivalent circuit representation

$$Y(\omega) = Y_{\mathrm{m}} + j\omega C_{\mathrm{o}} = \frac{R_{\mathrm{m}}}{R_{\mathrm{m}}^2 + X_{\mathrm{m}}^2} - j\frac{X_{\mathrm{m}}}{R_{\mathrm{m}}^2 + X_{\mathrm{m}}^2} + j\omega C_{\mathrm{o}} \tag{5.35}$$

$$X_{\mathrm{m}} = \omega L_{\mathrm{m}} - \frac{1}{\omega C_{\mathrm{m}}} \tag{5.36}$$

The motional circuit parameter, R_{m}, L_{m}, and C_{m} can be described in terms of the relevant mechanical quantities, the resonant mode's quality factor, and the electromechanical coupling coefficient [36]. The coupling coefficient η should not be confused with the coupling factors described earlier. These terms are sometimes used interchangeably in the literature despite their distinction. The coupling coefficient is analogous to the "turns ratio" of the effective transformer that converts quantities from the electrical to the mechanical domain and vice versa. In other words, they are the design-specific ratios of force to voltage and velocity to current. Equation (5.37) defines the motional circuit parameters for the BVD model where η is the electromechanical coupling coefficient, Q is the mode's quality factor, ω_i is the ith resonant frequency, $m_{i\mathrm{eff}}$ is the ith effective (or modal) mass, and $k_{i\mathrm{eff}}$ is the ith effective spring constant.

$$L_{\mathrm{m}} = \frac{m_{i\mathrm{eff}}}{\eta^2} \quad C_{\mathrm{m}} = \frac{\eta^2}{k_{i\mathrm{eff}}} \quad R_{\mathrm{m}} = \frac{V_{\mathrm{in}}}{I_{\mathrm{out}}} = \frac{\omega_i m_{i\mathrm{eff}}}{Q\eta^2} \tag{5.37}$$

5.1.3.10 Thin-Film Ferroelectric Nonlinearity

The constitutive equations of piezoelectricity, Equations (5.1) and (5.2), describe the *linear* response of piezoelectric materials. These, generally, can be applied successfully to polar piezoelectric thin films such as AlN and ZnO in most circumstances. However ferroelectrics such as PZT can display pronounced stress and electric

field-induced nonlinear material responses. This is particularly true for thin films and actuators. Thin films permit the application of extremely large electric fields with modest operating voltages due to the film thicknesses involved. Piezoelectric MEMS actuator applications typically drive the material well beyond the coercive field. For a half-micron thin film of PZT (52/48), for example, the coercive field corresponds to an applied voltage of about 2.5 V. Ferroelectrics even show significant nonlinearity below this field value [37]. Despite this fact it is surprising that, for both bulk material and thin film applications, the linear piezoelectric equations are often used to describe the device response. To accurately model ferroelectric MEMS device response, under high operating field (actuators) and/or bias field (sensors) conditions, these significant nonlinearities must be taken into account.

The origin of these nonlinearities in ferroelectrics is due largely to the existence of the domain structures that are absent in the polar materials. Domain wall vibration, translation, and domain switching all contribute to the nonlinear response of the elastic, dielectric, and piezoelectric properties. The study of nonlinearity in ferroelectrics is an extensive field and a review of this topic is beyond the scope of this book; for further information the readers are directed to [37–42].

At the high fields encountered in MEMS actuators, the total strain response is due to the combination of the linear response, nonlinear piezoelectricity including saturation effects, domain wall motion, and electrostriction. All dielectrics display the property of electrostriction, whereby externally applied electric fields induce a strain response that is proportional to the square of the field strength. Equation (5.38) describes the total strain response in ferroelectric materials where Q is the appropriate electrostrictive coefficient, P_s is the spontaneous polarization, E is the applied electric field, and κ is the appropriate dielectric constant. The first term defines the remnant strain. The poling process described earlier creates a macroscopically nonzero remnant polarization. The change in this value creates a semipermanent residual strain due to this poling process. This change in strain can be significant for materials such as PZT and should be accounted for in device design. The second term is equal to the linear piezoelectric coefficient (d_{ij}) multiplied by the electric field. The last term is the strain due to electrostriction. As the applied field strength increases, the electrostrictive term contributes more to the overall strain response in the material.

$$x = QP_{\mathrm{s}}^2 + 2\varepsilon_{\mathrm{o}}\kappa QP_{\mathrm{s}}E + Q\left(\varepsilon_{\mathrm{o}}\kappa E\right)^2 \tag{5.38}$$

The material responses in ferroelectrics are classified as intrinsic and extrinsic effects. Intrinsic effects are those associated with the ionic deformations of the unit cells of the crystalline material whereas extrinsic effects are those associated with changes in the domain state. At large applied stresses and electric fields, significant contributions to the total strain response (Equation (5.38)) are due to nonlinear piezoelectricity and the extrinsic response. These can be interpreted as imposing field and stress-dependent dielectric, elastic, and piezoelectric coefficients. These nonlinear material properties used for design purposes are best measured for specific materials and processing conditions. Due to these complex nonlinear effects,

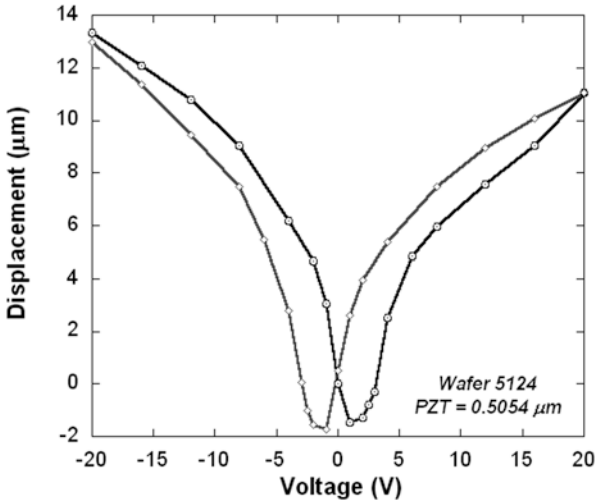


Fig. 5.22 Displacement versus voltage plot for a PZT thin-film cantilever comprised of a 0.5 μm elastic layer $(SiO_2/Si_3N_4/SiO_2)/0.1\,\mu m$ Ti/Pt bilayer, 0.505 μm PZT (52/48), and a 0.1 μm Pt top electrode. Key aspects of this diagram include the hysteretic displacement characteristics upon bipolar voltage swings. In addition, all but a small fraction of the displacement occurs in one direction

the ratio of total strain to applied electric field is referred to as the effective electroactive coefficients. These coefficients can be used with the models described above using field-dependent functions.

Perhaps the most important consequence of these nonlinear effects is the absence of a bipolar strain response when operated above the coercive field. Figure 5.22 shows voltage-displacement data from a simple unimorph PZT MEMS-actuated cantilever, illustrating the so-called butterfly loop. The plot was obtained by sweeping the actuation voltage up to a positive voltage, then reducing to zero, then sweeping down to a negative voltage, and finally returning to zero field. The extracted effective electroactive piezoelectric stress constant, $e_{31\text{eff}}$, is illustrated in Fig. 5.23 and corresponds to the displacement data in Fig. 5.22. This effective piezoelectric constant includes the small signal piezoelectric effect, electrostiction, and strain induced by large polarization charges associated with overcoming a pinched ferroelectric hysteresis loop. An additional indication of the nonlinearity within ferroelectric-based actuators is the nonlinearity in the dielectric constant κ_{33} as a function of voltage as illustrated in Fig. 5.24.

The response of the device is seen to be bipolar only in the regime between the positive and negative coercive voltages where the negative displacement reverts to a positive displacement (the "V" regions of the lower curves). It is instructive to consider the ionic deformations of the constituent unit cells of the ferroelectric material when considering this behavior. Referring to PZT tetragonal unit cell illustrated in Fig. 5.6, at small values of an applied electric field the central ion of the unit cell

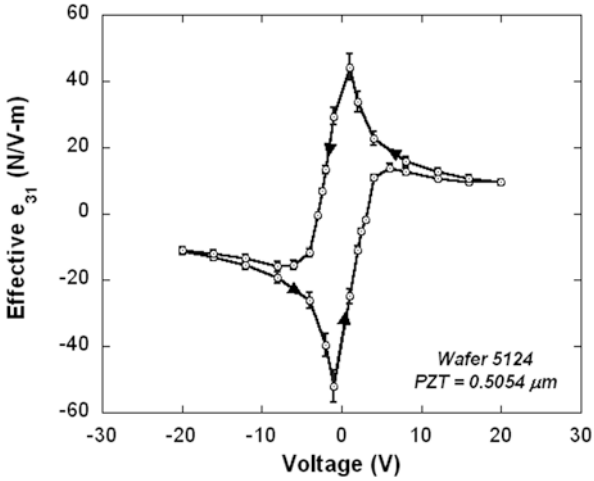


Fig. 5.23 Effective electroactive piezoelectric stress constant, $e_{31,\mathrm{eff}}$, versus voltage extracted from the displacement-voltage measurements for the PZT thin-film unimorph described in Fig. 5.22

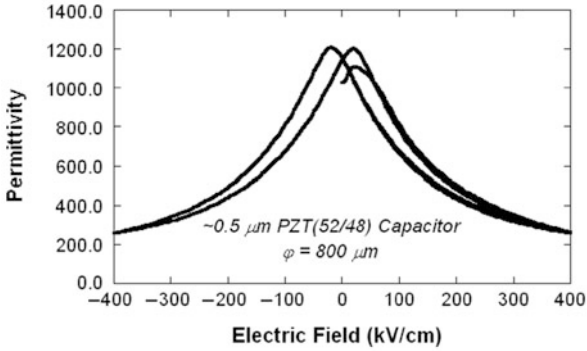


Fig. 5.24 Dielectric constant as a function of voltage for a 0.5 μm thick PZT (52/48) thin-film capacitor

displaces positively or negatively from its poled position, depending upon the polarity of the field. At small electric field values, a positive displacement of the oxygen relative to the cations creates a net elongation (*c*-axis) of the unit cell and a negative displacement creates a net contraction (*c*-axis) of the unit cell relative to the initial poled unit cell displacement.

However, for applied electric field values that exceed the value necessary to reverse the oxygen and cation sublattice displacements back to the unit cell midplane (i.e., the coercive field), the oxygen ions will continue to displace in the direction of the applied field. Once this occurs, the unit cell will no longer experience a net contraction along the *c*-axis, relative to the initial poled unit cell displacement, and instead the unit cell will experience a net elongation along the *c*-axis. This is due to the mirror symmetry of the unit cell about its midplane. Thus for large electric fields

(i.e., in excess of the coercive field) applied to the piezoelectric material, the sense of the piezoelectric strain is independent of the applied field polarity, therefore only a single sense of the piezoelectric strain is possible.

In terms of the device, the in-plane contraction of the piezoelectric material at large fields gives a negative sense to the piezoelectric actuation force. The standard configuration of the d_{31} mode MEMS unimorph, with the neutral axis below the midplane of the piezoelectric layer gives a positive sense of the moment arm. At small fields, with an applied voltage corresponding to the opposite of the original poling field (either of the lower curves in the hysteretic plot of Fig. 5.22), the actuator will deflect downward. However, as the voltage increases to a value near the coercive field, the actuator will switch directions and will then bend upward. As the field strength is increased further, the actuator will continue to bend upward. If instead, the polarity of the voltage corresponding to the original poling field is applied, the actuator will bend upward for all voltages (either of the upper curves in the hysteretic plot of Fig. 5.22). Piezoelectric MEMS devices are most often operated under unipolar conditions and hence avoid much of the hysteresis observed in Fig. 5.22.

5.1.3.11 Heat Generation

Piezoelectric devices are often limited in terms of drive amplitude and upper operating frequency by the generation of heat. Heat generation is due to the material losses in the piezoelectric. Losses in piezoelectrics are mechanical, dielectric, and electromechanical in nature. The fundamental mechanisms responsible for these losses are complex, varied, and not fully understood. However, in ferroelectrics, the nonmechanical losses are associated with domain and lattice affects, microstructural defects, and finite conductivity [43]. These losses have conventionally been described by complex representations for the permittivity, compliance, and piezoelectric material constants whereby the imaginary components refer to the losses [44]. The heat generation is largely determined by the dielectric loss with nonresonant operation. The thermal power under these conditions is given by Equation (5.39), where f is the operating frequency, Lwt_p is the volume of the active piezoelectric, and $\tan\delta$ is the dielectric loss.

$$P_{\text{therm}} = 2\pi f E_3^2 \varepsilon_{33}^T Lwt_{\text{p}} \tan\delta \tag{5.39}$$

5.1.4 Materials Selection Guide

The important piezoelectric and dielectric material properties for the three most common thin-film piezoelectrics, ZnO, AlN, and PZT are listed in Table 5.2. A few features to recognize are the effective thin-film piezoelectric coefficient, $e_{31,f}$, of these three compounds compared with that of PZT which is an order of magnitude larger than the others. Furthermore, $\varepsilon_{33,f}$ is typically greater than two orders of magnitude larger in PZT compared with ZnO and AlN.

Table 5.2 Comparison of thin-film piezoelectric materials

	ZnO	AlN	PZT
$e_{31,f}$ (C/m^2)	–0.4 → –0.8	–0.9 → –1.1	–8 → –18
$d_{33,f}$ (pC/N)	10 → 17	3.4 → 6.5	90 → 150
ε_{33}	8 → 12	10.1 → 10.7	800 → 1200
tan δ			0.02 → 0.05
Density (g/cm^3)	5.68	3.26	7.5 → 7.6
Young's Modulus (GPa)	110 → 150	260 → 380	60 → 80
Acoustic Velocity (m/s)	6.07×10^3	11.4×10^3	2.7×10^3
References	[45–50]	[45, 47, 48, 51, 52]	[45, 47, 48]

5.1.5 Applications

Piezoelectric materials offer a combination of unique advantages in MEMS for a wide range of applications. Generally, piezoelectric transduction utilizes strong electromechanical coupling that features more favorable scaling and efficiency than competing transduction approaches such as thermomechanical, electromagnetic, and electrostatics. Piezoelectric sensors typically possess high sensitivity and dynamic range and are passive devices often avoiding the need for external power. Piezoelectric actuators are capable of low voltage/high efficiency operation with large force and/or displacement generation. Although thin-film ferroelectrics can exhibit significant nonlinearities, these are generally less severe than those encountered in the more prevalent electrostatic devices. The high strong electromechanical coupling, simple geometric implementation, and high energy densities also make piezoelectric materials attractive for energy harvesting applications.

To date, piezoelectric thin films have been most successfully implemented in RF, memory, and inkjet printing applications. In addition to the commercial success of AlN film bulk acoustic resonator (FBAR) technology [1], piezoelectric thin-film RF MEMS resonators [8, 48, 53–55] have now shown good insertion loss, quality factor, and motional resistances that permit straightforward integration with standard 50Ω RF circuits. High-performance quartz-based resonators and filters are ubiquitous in RF applications, however, piezoelectric RF MEMS resonator technologies hold the promise of much greater levels of low-cost integration by allowing multiple lithographically defined frequencies on the same chip. In recent years, piezoelectric films have also been utilized in high-performance RF switches, phase shifters, and tunable capacitors [13, 29, 56–58]. Ferroelectric random access memory (FRAM), a nonvolatile memory technology typically based on PZT thin films, has been a successful commercial product since the early 1990s. The CMOS integrated technology utilizes the ferroelectric polarization reversal with applied electric bias to provide nonvolatile memory storage.

A wide array of sensors has been demonstrated with piezoelectric thin films, including acoustic microphones [59, 60], accelerometers [61–65], and ultrasound transducers [66–69]. Recent interest in wireless sensing networks and mobile technologies has motivated great attention to energy harvesting technologies. A number

of groups have demonstrated low-power but high-energy-density harvesters based on piezoelectric MEMS [70–73] using integrated proof masses and vibrational energy-scavenging designs.

In addition to RF MEMS applications, many piezoelectric MEMS actuation technologies have been developed over the past two decades including AFM cantilever devices [74], micromirror arrays [75, 76], inkjet printing devices [77], ultrasonic micromotors [78, 79], mechanical logic devices [80, 81], and small-scale robotics [16, 82–84].

5.2 Polar Materials: AlN and ZnO

This section concentrates on the purely polar compounds that have received the most interest to date for piezoelectric MEMS: AlN and ZnO. Each of these compounds has been researched for a wide variety of applications with film bulk acoustic resonators motivating much of the research. This section reviews deposition of these materials and patterning techniques, identifies device design and processing concerns, and provides examples of AlN and ZnO devices including a case study on contour-mode resonators.

5.2.1 Material Deposition

Both AlN and ZnO are primarily deposited via physical vapor deposition techniques, namely sputtering. Although metalorganic chemical vapor deposition (MOCVD) has been used for both AlN and ZnO, most MEMS applications require substantially thicker films than those typically deposited by MOCVD techniques. As a result, readers interested in information on MOCVD deposition of AlN and ZnO are directed to [85–89]. Regardless of deposition technique, *c*-axis, [0001], oriented films, and low impurity contents are required for optimal piezoelectric performance. Both the piezoelectric coefficient and the electromechanical coupling factor are affected by the quality of the piezoelectric crystalline texture [90, 91]. Figure 5.25 illustrates the trends in the longitudinal piezoelectric coefficient, $d_{33,\mathrm{f}}$, and the thickness mode coupling factor, k_{t}^2, for sputtered AlN films. Achieving highly textured [0002] AlN and ZnO films requires control of the nucleation and growth characteristics, substrate choice, surface roughness, and defect density to name a few parameters [91, 92]. Examples of successful deposition parameters for both AlN and ZnO are available in Table 5.3. In general, both ZnO and AlN thin films are deposited via reactive sputtering using magnetron sputtering with either RF or pulsed DC sources.

The choice of the substrate and/or the layer the piezoelectric material is to be deposited on, can affect the properties of the piezoelectric film greatly. For most MEMS applications, silicon is the substrate of choice and both AlN and ZnO can be

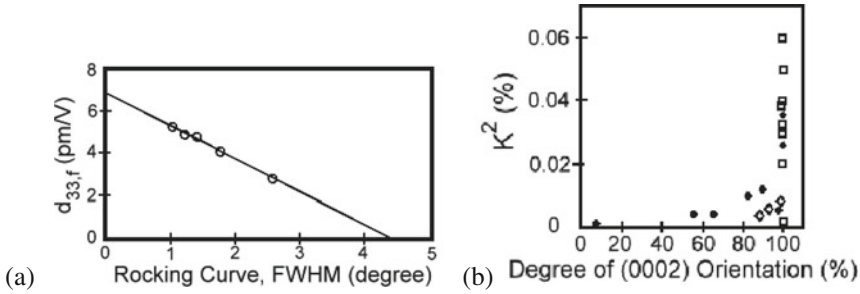


Fig. 5.25 The influence of [0002] texture on (**a**) the longitudinal piezoelectric coefficient $d_{33,f}$, [90] (Reprinted with permission. Copyright 2004 American Vacuum Society) and (**b**) the coupling factor k_t^2 for sputtered AlN thin films [91] (Reprinted with permission. Copyright 2004 Elsevier)

Table 5.3 Sputter deposition parameters for piezoelectric AlN and ZnO thin films

Sputtering parameter	AlN	AlN	AlN	AlN	ZnO	ZnO
System	RF mag	Triode	RF mag	DC pulse	RF mag	RF mag
Target	Al	Al	Al	Al	ZnO	ZnO
RF power (W)	150		200	500	80	200
Target current (A)		0.1				
Target voltage (V)		1000				
Target to substrate distance (mm)	65	40	17	80		
Pressure (Pa)	0.5	0.3	0.27	<0.67	2	0.93
Ar (sccm or %)	15.5	90%	3	0–10	50%	66%
N_2 (sccm or %)	2.5	10%	12	10–20		
O_2 (sccm or %)					50%	33%
Bias (V or W)	0 to –100 V	0 to –250 V	0 to –320 V	0 to 12 W		
Substrate temperature (°C)	RT to 800	RT to 225	RT to 80	400	RT	RT
References	[101]	[102]	[103]	[104]	[105]	[106]

deposited onto silicon. Depending on the application, additional layers (i.e., elastic layers and metal layers) may be required beneath the piezoelectric material. One common design is to use a parallel plate configuration (d_{31} mode) in which the piezoelectric is sandwiched between two conductive layers, as illustrated in Fig. 5.15. The choice of the conductive layer can directly influence the crystal texture of the piezoelectric, thereby affecting its piezoelectric properties. Common electrode materials include Ti, Pt, and Al electrodes as they have surfaces exhibiting hexagonal symmetry [93, 94, 104]. AlN deposited onto Pt has been shown to have superior performance relative to Ti and Al layers (see Fig. 5.26) [104]. Recently, there has been a push toward Mo electrodes to counter the disadvantages with Pt including its difficulty in patterning, high resistivity in ultrathin layers, and higher acoustic attenuation compared with Mo [90, 94–98]. However, Mo tends to result in broader [0002] peaks (i.e., larger full width at half maximum, FWHM, values) compared to Pt (see Fig. 5.27) [97, 98]. A comparison of the FWHM and surface

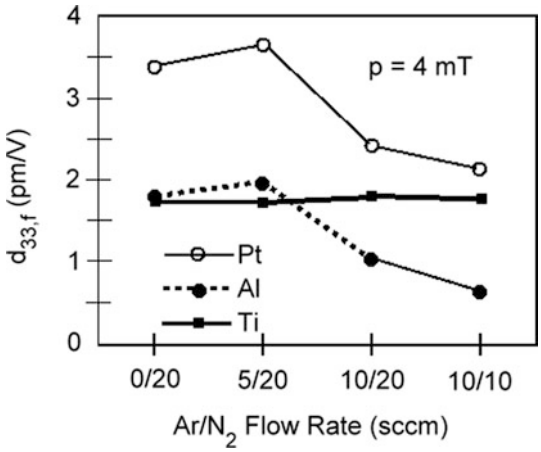


Fig. 5.26 Longitudinal piezoelectric coefficient, $d_{33,f}$, as a function of Ar/N_2 for reactively sputtered AlN deposited onto Ti, Al, or Pt electrode layers [104] (Reprinted with permission. Copyright 2001 American Vacuum Society)

roughness properties for sputtered AlN films on various substrates and thin films is listed in Table 5.4 followed by an SEM image of AlN film on Mo showing the columnar growth pattern in Fig. 5.28. Methods of improving the FWHM for AlN on Mo include the use of seed layers and buffer layers. A seed layer of Ti has been shown to yield smoother Mo films with a lower FWHM resulting in improved qualities in the sputtered AlN film (see Table 5.5) [99]. As an alternative, thin AlN buffer layers (~50 to 100 nm) have been used to improve the quality of AlN on Mo films deposited on Si substrates [100].

Similar to AlN, ZnO is primarily deposited via sputtering. A specific concern for ZnO thin films is the role of the oxygen partial pressure during sputtering. As shown

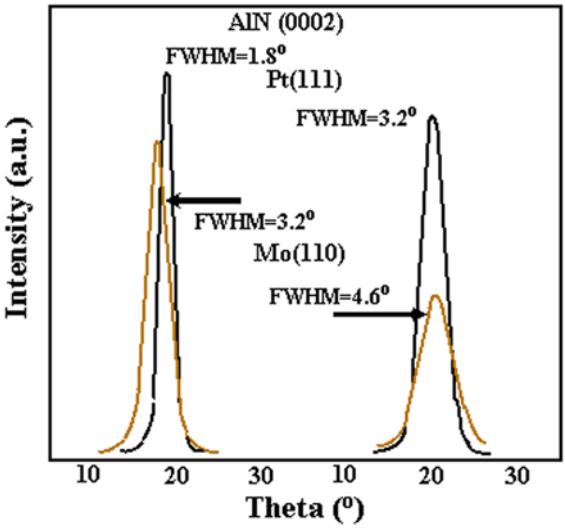


Fig. 5.27 Comparison between pulse DC sputtered AlN on Pt and Mo electrodes [97] (Reprinted with permission. Copyright 2005 IEEE)

Table 5.4 Comparison of the surface roughness (RMS) and full width at half maximum (FWHM) for sputtered AlN films on various substrates and thin films [97]

Substrate	Si	Si/Mo	Si/SiO_2	Si/Si_3N_4	$Si/SiO_2/Ti/Pt$
Substrate roughness, R_{rms}(Å)	0.94	5.10	0.91	1.27	3.49
AlN roughness, R_{rms}(Å)	12	46.3	11.4	16.0	39.7
AlN (0002), FWHM (°)	1.82	5.15	1.78	1.90	2.37

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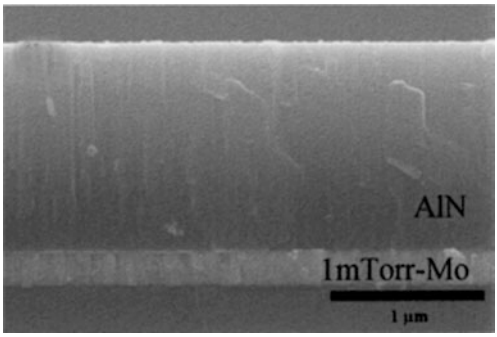

Fig. 5.28 SEM image illustrating the columnar growth and smooth texture of a sputtered AlN film deposited onto Mo on a Si substrate [96] (Reprinted with permission. Copyright 2003 American Vacuum Society)

Table 5.5 Influence of a Ti seed layer on the sputter deposition of both Mo and AlN films [99]

Substrate	Mo deposition temperature (°C)	Mo roughness, R_{rms}(Å)	Mo FWHM (°)	AlN roughness, R_{rms}(Å)	AlN FWHM (°)
No seed layer	250	3.86	6.2	12.60	3.6
Ti seed (30 nm)	250	2.75	2.1	7.44	1.7

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in Fig. 5.29a, increases in oxygen percentage in a Ar/O_2 mixture leads to decreases in the surface roughness. However, the FWHM of the [0002] peak increases. One method of achieving improvements in both the RMS roughness and FWHM is to use a two-step deposition process [105]. In the process outlined by Lin, Chen, and Kao [105], the initial step uses a high oxygen percentage (75%) to deposit a smooth starting layer of ZnO. The second deposition processes switches to a lower oxygen percentage (50%) to increase the texture quality of the film along with maintaining accurate stoichiometry. The resulting film exhibits a columnar growth pattern along with an improved surface quality (see Fig. 5.29b).

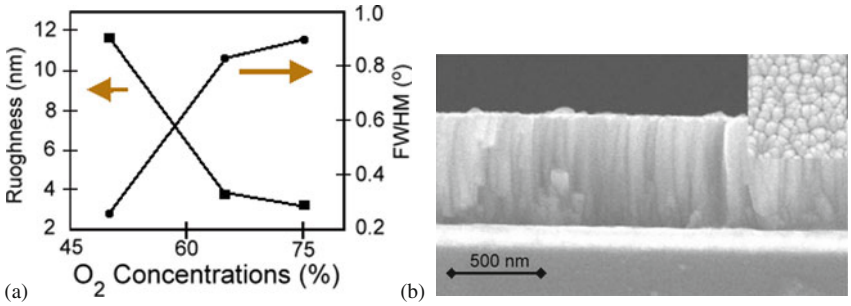


Fig. 5.29 (**a**) Influence of oxygen concentration on the texture and surface roughness of RF sputtered ZnO thin films and (**b**) an SEM image of a sputtered ZnO film deposited using a two-step process [105] (Reprinted with permission. Copyright 2007 Springer Science+Business Media)

5.2.2 Patterning Techniques

In order to enable the full integration potential of AlN and ZnO, selective patterning capabilities are required including both wet chemical and dry etch processes. A key aspect of wet chemical processes is their tendency to be very isotropic resulting in reasonably large lateral etch rates. However, under many circumstances, wet etching is preferred to avoid the physical damage and generally low selectivity of physical etch techniques. Both AlN and ZnO can be removed with wet chemical etch processes and a list of known etchants have been assembled in Table 5.6. An important characteristic about ZnO is that its material quality (texture, dielectric loss, and breakdown strength) are well known to be extremely sensitive to microfabrication processes [107]. As a result care must be taken not only to protect it during the etching process but also during the remainder of the device fabrication processes. Protection layers can include the use of silicon dioxide and silicon nitride barrier layers to name a few.

Table 5.6 Summary of wet etching techniques for AlN and ZnO thin films

Etching parameter	AlN	AlN	AlN	AlN	ZnO	ZnO
Chemical(s)	AZ400K (KOH)	KOH (10%)	TMAH	H_3PO_4 (85%)	HCl (0.1 M)	CH_3COOH: H_3PO_4:H_2O (1:1:60)
Mask	Apiezon wax	Ti	Cr			
Temperature (°C)	85	RT–85	RT	60	RT	RT
Etch rate (nm/min)	6–1000	6–1500	22	600–3000	300–1200	~800
References	[108, 109]	[109, 110]	[111]	[112, 113]	[107, 114, 115]	[107, 116]

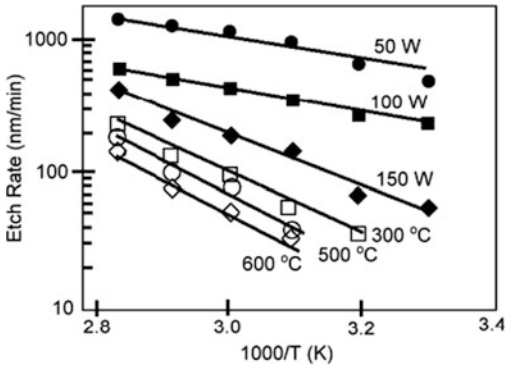


Fig. 5.30 AlN wet etch rates in 10 wt% KOH as a function of solution temperature, deposition temperature, and the deposition power of sputtered AlN [110] (Reprinted with permission. Copyright 2008 Elsevier)

The ability of etching AlN has a very strong relationship to the crystalline quality of the thin film. As discussed previously, the crystalline quality is highly dependent on the deposition parameters. Similarly, the etching rates are linked to the deposition conditions. The example in Fig. 5.30 illustrates the variance in etching conditions as a function of solution temperature, RF deposition power, and substrate deposition temperature. In addition, the lateral etch rates also vary as a function of the crystalline quality of the film (see Fig. 5.31). Another crucial point in the primary wet etch for sputtered AlN films is KOH, the main component in some photoresist developers [108, 109]. Therefore, special concern must be taken in the selection of photoresists and developers used during the microfabrication process. Similar to ZnO films, the use of barrier coatings such as silicon dioxide or silicon nitride thin films are common.

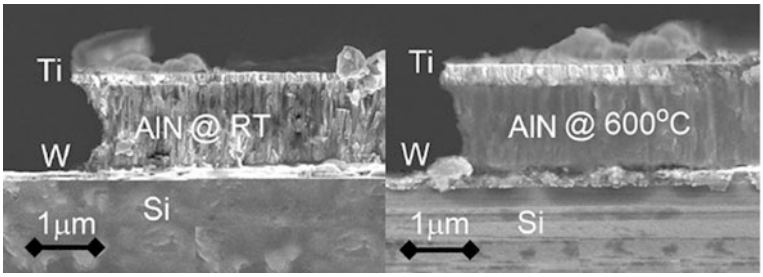


Fig. 5.31 SEM images of sputtered AlN following a wet etch in 10 wt% KOH for films deposited at RT and 600°C [110] (Reprinted with permission. Copyright 2008 Elsevier)

Physical etching of AlN and ZnO by various etching techniques is the choice for precision definition of MEMS devices. In general, chlorine plasmas are used for AlN etching and fluorine plasmas are used for ZnO. A list of common physical etch techniques for both compounds is given in Table 5.7. In contrast to wet chemical etching, physical etching leads to nearly vertical sidewalls under the appropriate etch conditions (see Fig. 5.32). For AlN, the use of hydrogen in the etch chemistries

Table 5.7 Summary of plasma etch techniques for AlN and ZnO

Etching parameter	AlN	AlN	AlN	ZnO	ZnO
System	ECR	ICP	ICP	ICP	ICP
Chemical(s)	Cl_2/H_2	Cl_2/Ar (5:1)	Cl_2 or Cl_4/H_2	C_2F_6	C_2H_6 /H_2 /Ar
RF power (W)	200	500	100–1500	700–1000	300
Bias (V or W)	–150 V	–100 to –350 V	0 to –100 V	50–200 W	
Pressure (Pa)	0.13	0.26	0.26–2	0.4–2	0.26
Etch rate (nm/min)	10–40	50–700	50–150	410	50
References	[117]	[118, 119]	[120]	[121]	[122]

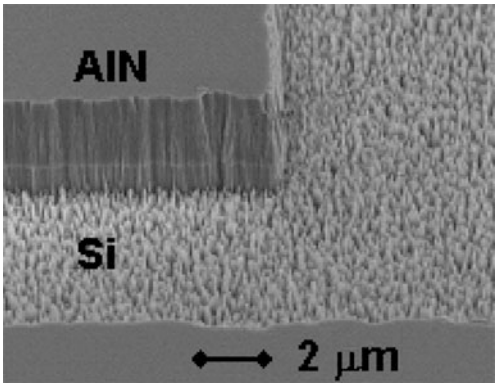


Fig. 5.32 SEM of an AlN layer etched using an ICP plasma using a Cl_2/Ar gas mixture

tends to lead to equal etching rates for the group III and group V components and leads to smoother etch surfaces [117].

5.2.3 Device-Design Concerns

Designing piezoelectric MEMS with AlN or ZnO requires attention to several key aspects that affect the overall device performance. The choice of film thickness has a direct impact on the crystalline texture and piezoelectric coefficient. The initial growth starts with epitaxial matching to the substrate or electrode surface leading to strained growth with a relatively broad FWHM. For sputtered AlN, as the film thickness increases, the alignment of the crystals improves, reducing the FWHM to near 1 degree and increasing $d_{33,f}$ toward 5 pm/V (see Figs. 5.33 and 5.34) [90, 123].

In most applications, parallel plate configurations (d_{31} mode) are utilized requiring the use of multilayer composites. As a result, control of residual stress gradients is imperative and starts with an understanding of the residual stress in the piezoelectric. Similar to the FWHM and piezoelectric coefficient, the residual stress heavily

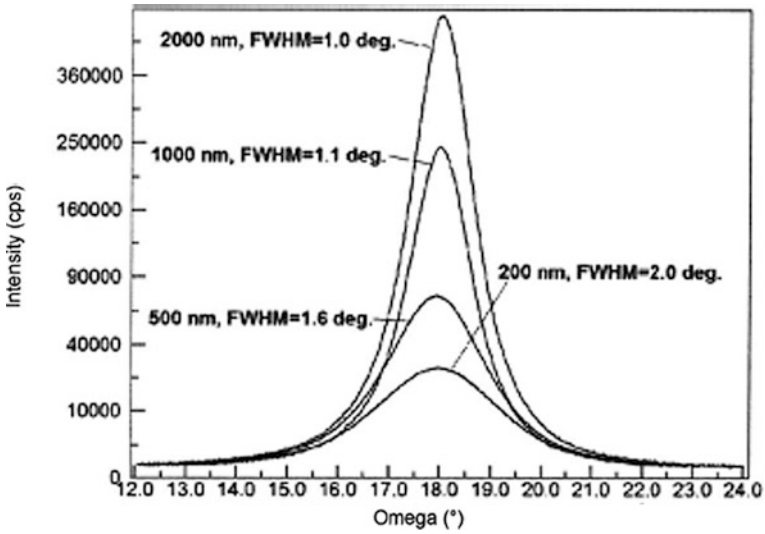


Fig. 5.33 Rocking curve FWHM and $d_{33,f}$ as a function of film thickness for sputtered AlN on Si/SiO_2/Ti/Pt [123] (Reprinted with permission. Copyright 2009 American Vacuum Society)

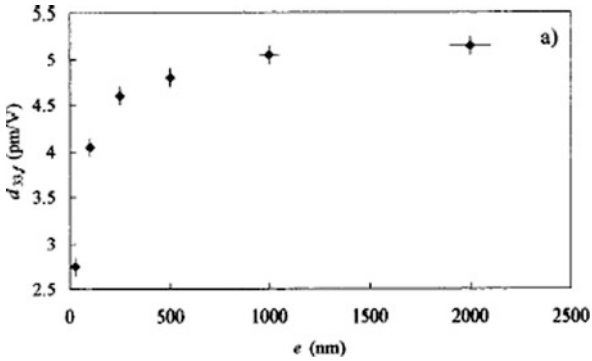


Fig. 5.34 $d_{33,f}$ as a function of film thickness for sputtered AlN on Si/SiO_2/Ti/Pt [90] (Reprinted with permission. Copyright 2004 American Vacuum Society)

depends on the film thickness, primarily a result of high interface stresses as the piezoelectric is strained to match the underlying layers. As shown in Fig. 5.35, the stress of a sputtered AlN on Pt changes from compressive to tensile with increasing thickness, for the deposition parameters in [90]. In addition to the stress being dependent on the film thickness, the deposition parameters (RF or DC bias, pressure, gas flow, and temperature) can greatly influence the residual stress [22, 101, 102, 104]. In many instances, the film stress can be controlled over a wide spectrum from compressive to tensile stress (see Fig. 5.36). In addition, the film stress and the coupling factor have been shown to be interrelated creating a more challenging situation to achieve both low stress and high piezoelectric properties (see Fig. 5.37).

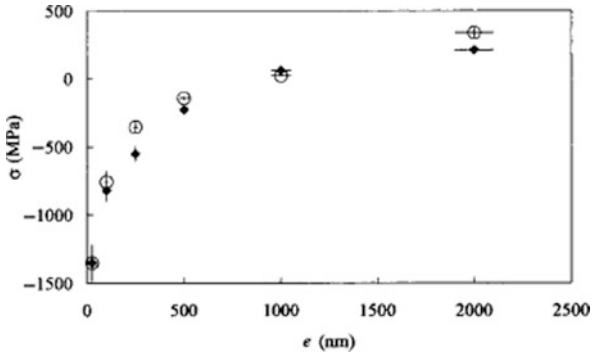


Fig. 5.35 Residual stress as a function of film thickness for a sputtered AlN film on $Si/SiO_2/Ti/Pt$ [90] (Reprinted with permission. Copyright 2004 American Vacuum Society)

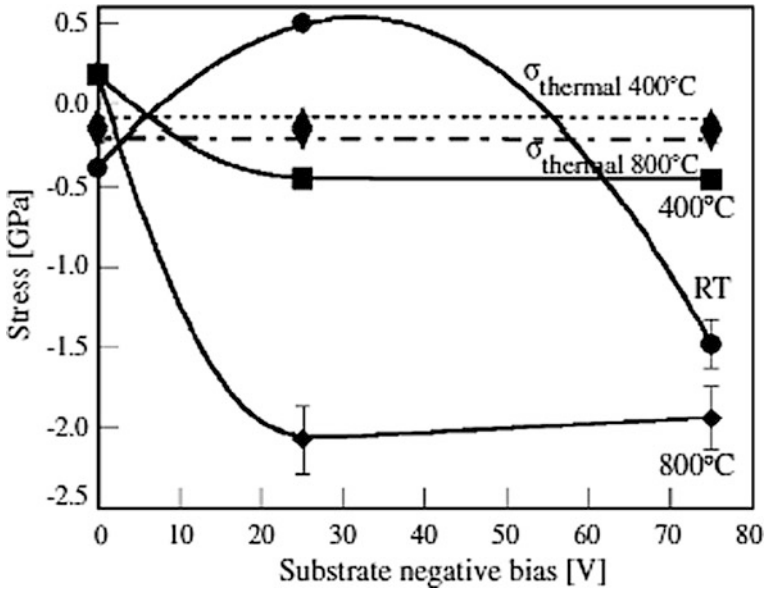


Fig. 5.36 Residual stress of AlN deposited on Si as a function of substrate bias and substrate temperature [101] (Reprinted with permission. Copyright 2006 Elsevier)

5.2.4 Device Examples

This section provides a sampling of the capabilities of polar thin films in MEMS and how they have been implemented in devices. Examples highlighting some recent successes are presented, followed by a full case study in AlN contour-mode resonators and filters.

The cell phone industry has been driving RF filter innovation in recent years, providing challenging requirements for filter selectivity, power handling, temperature insensitivity, and filter figure of merit ($k^2_{\mathrm{eff}}Q$) [124]. Film (or "free-standing") bulk

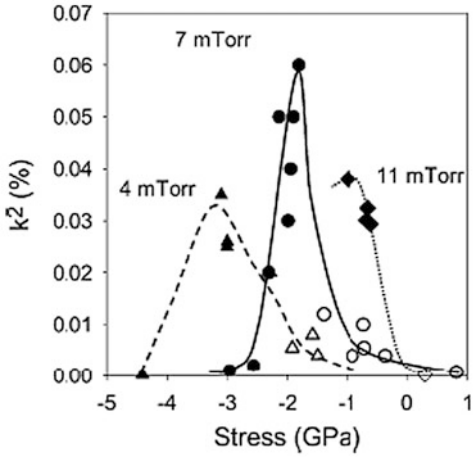


Fig. 5.37 The interplay between the electromechanical coupling factor and residual stress at different deposition pressures for sputtered AlN films on Si and Si/SiO_2 [91] (Reprinted with permission. Copyright 2004 Elsevier)

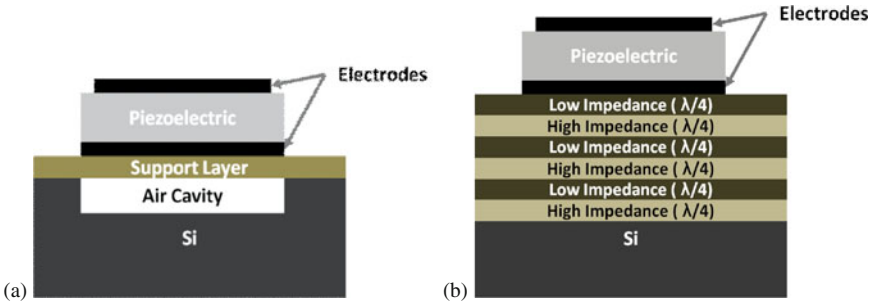
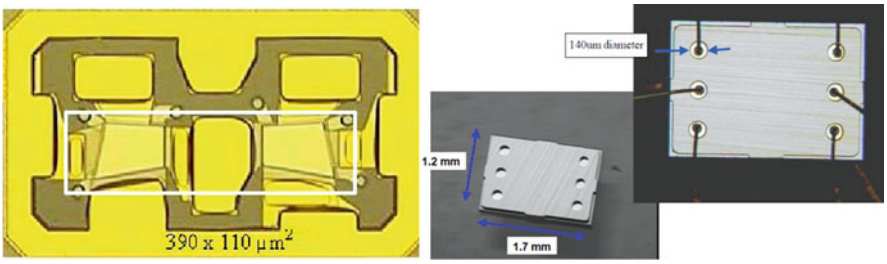


Fig. 5.38 Illustration of (**a**) film bulk acoustic resonator (FBAR) structure and (**b**) solidly mounted resonator (SMR). Both devices are typically realized with AlN thin films

acoustic resonator and filter technology now represents a significant commercial success story in RF MEMS. AlN FBAR devices feature extensional thickness-mode thin-film piezoelectric membrane resonators that are suspended above a silicon substrate (see Fig. 5.38). In addition to the free-standing FBAR structures, the solidly mounted resonator (SMR) device utilizes a series of acoustic impedance mismatch layers directly below the resonator to retain acoustic energy within the transducer.

SMR devices tend to be more robust than the FBAR but have inferior RF performance due to degradation in mechanical quality factor with enhanced acoustic energy radiation into the substrate. Both SMR and FBAR devices have a number of advantages over competing technologies such as surface acoustic wave devices (SAWs), including superior figure of merit, power handling, electrostatic discharge insensitivity, and size [125, 126]. Avago Technologies, formally Agilent's semiconductor products group, has sold hundreds of millions of FBAR-based units including



(a) (b)

Fig. 5.39 (a) Micrograph of an example FBAR filter from Avago Technologies Inc. The active filter area is indicated by the white rectangle [125] (Reprinted with permission. Copyright 2008 IEEE) and (**b**) Micrograph of singulated packaged FBAR filters from Avago [127] (Reprinted with permission. Copyright 2002 IEEE)

filters, duplexers, and multiplexers. The Avago FBAR device (see Fig. 5.39) fabrication begins with etching and backfilling portions of the silicon substrate with a sacrificial oxide [125]. Once the wafer is polished, a Mo film is deposited and patterned as an electrode. The AlN film is then sputter-deposited and patterned and followed by the deposition and patterning of the Mo top electrode. Following additional processing, the structures are released with HF. The Avago devices are hermetically sealed in a low-cost wafer-level package [127]. The patented process bonds the FBAR silicon substrate with a second silicon wafer housing vias, seals, and alignment marks. The cap wafer is subsequently thinned with conventional wafer-thinning. DRIE is then used to open access to the FBAR contacts.

Despite the advantages and success of FBAR devices, there remains a need for integrating small-scale and low-power multiple-frequency and multiple-standard RF devices [128]. Cost-effectively integrating large numbers of multiple frequency filters appears difficult for FBAR devices as they rely on extensional thickness modes to determine center frequency. In contrast, contour-mode resonators have center frequencies determined by their lithographically definable lateral dimensions. Great progress has been made during the last few years in both ZnO and AlN contour mode resonators [129–132].

High performance extensional contour mode resonators have been demonstrated in ZnO (see Fig. 5.40). Referring to the research in [129], the devices make use of high-quality single crystal silicon as the bulk of the resonator to provide low volumetric mechanical losses. Loaded quality factors in vacuum have been demonstrated with values as high as 11,800 with motional resistances of 1600 Ω. Motional resistances as low as 600 Ω have also been shown, however, with lower Qs. The resonators are fabricated with a three-mask process that begins with patterning an SOI-based single crystal silicon resonator. ZnO films are then deposited on the Cr–Au electroded resonator structures. After an Al top electrode is deposited and patterned, the ZnO is finally patterned to provide bottom electrode access.

A number of transduction techniques have been utilized in the actuation of RF MEMS switches, including electrostatic, electromagnetic, thermomechanical,

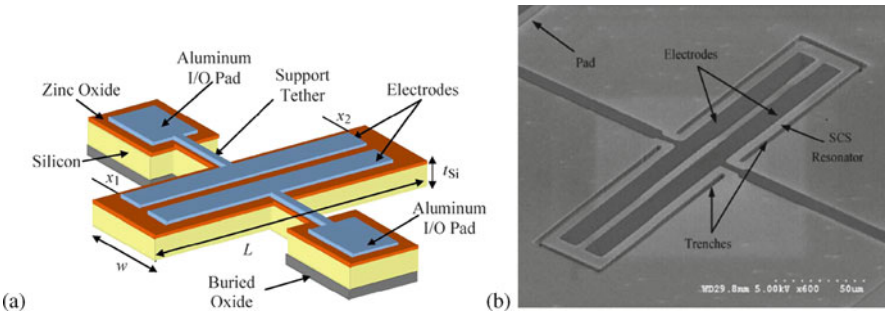


Fig. 5.40 (**a**) Illustration and (**b**) SEM of a ZnO on silicon lateral bulk acoustic resonator [129] (Reprinted with permission. Copyright 2008 IEEE)

and piezoelectric. The interest in radio and cell-phone frequency compatible AlN-based filters has motivated the development of integrated piezoelectric RF MEMS switches. AlN piezoelectric RF MEMS switches have recently been demonstrated with good RF performance at these frequencies of interest [133]. These devices feature an innovative approach to address residual stress deformation, temperature sensitivity, and the modest piezoelectric coefficients of AlN. A symmetric "dual-beam" design features pairs of actuators that experience similar residual stress and temperature-induced deformations that minimize variations in the open-state contact gap despite the mechanical fluctuations (see Fig. 5.41). The device shows immunity to residual stresses, fast switching speeds (~2 μs), moderate actuation voltage (~20 V), and good low frequency isolation (>26 dB) and insertion loss (<0.7 dB) at 2 GHz. These devices have also been successfully cofabricated on the same wafer as contour-mode AlN RF MEMS resonators. The device fabrication leverages the process used for AlN contour-mode resonators. Once these features are defined,

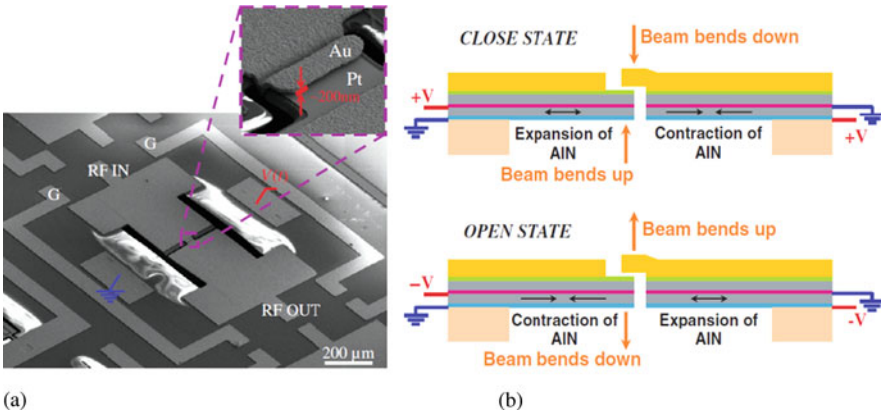


Fig. 5.41 (**a**) SEM image of AlN RF MEMS switch with inset indicating the nanogap contact location and (**b**) illustration of principle of operation of "dual-beam" architecture [133] (Reprinted with permission. Copyright 2008 Institute of Physics)

including multiple AlN and Pt electrode deposition and patterning steps, an amorphous silicon sacrificial layer is deposited and patterned with liftoff. This is followed by the deposition and patterning of a thick electroplated Au layer to provide RF transmission lines and unimorph actuator features. The switch is released using a xenon difluoride dry release to complete the process.

A number of groups are investigating mechanical logic technologies to address the limitations imposed in CMOS by gate oxide leakage. Static power consumption now rivals dynamic power consumption in CMOS and presents a significant challenge to the continued scaling of CMOS logic devices. Motivated by low-power nanomechanical logic applications, AlN nanoactuators have recently been demonstrated [134]. AlN thin films with a thickness of 100 nm were implemented in nanoscale bimorph cantilevered actuators. Displacements of 40 nm were achieved at 2 V in 18 μm long cantilever devices. The actuators were fabricated using a five-mask post-CMOS compatible process similar to the process outlined for the fabrication of the AlN RF MEMS switch discussed above. A key difference in the process, however, is the use of a focused ion beam (FIB) tool. The nearly complete suspended clamped–clamped AlN beam is severed at one anchor with the FIB to create the cantilevered device seen in Fig. 5.42.

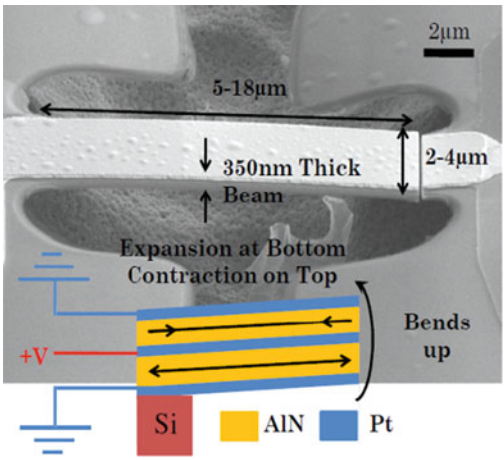


Fig. 5.42 SEM image of AlN cantilevered bimorph nanoactuator [134] (Reprinted with permission. Copyright 2008 IEEE)

5.2.5 Case Study

As discussed earlier, there is great interest in developing highly integrated multiple frequency arrays of filters and resonators for RF applications. Recent progress in both AlN contour-mode filters and RF MEMS switches suggests this technology could become a viable commercial product [128, 132, 133, 135]. The devices are generally near-symmetric Pt/AlN/Al composite structures with AlN thicknesses typically in excess of a micron [131]. The contour vibrational modes are excited

through the d_{31} coefficient in c-axis-oriented AlN films. In a typical two-port configuration, an input broadband RF signal is transduced into the mechanical domain via the converse piezoelectric effect by an input transducer. The signal is then largely filtered by the mechanical frequency response of the structure and subsequently transduced back into the electrical domain by means of the output transducer. The input transducer effectively behaves as an actuator whereas the output transducer behaves as a sensor. Different resonator geometries are utilized to achieve the best RF performance at various frequencies, including the rectangular plate geometry (~10 to ~100 MHz operation), ring resonators (~100–400 MHz), and higher-order contour-mode plate geometries (see Fig. 5.43). These devices have been demonstrated at frequencies from 20 MHz to about 700 MHz with quality factors as high as 4300 (230 MHz) and with low motional resistances ranging from 50 to 700 Ω.

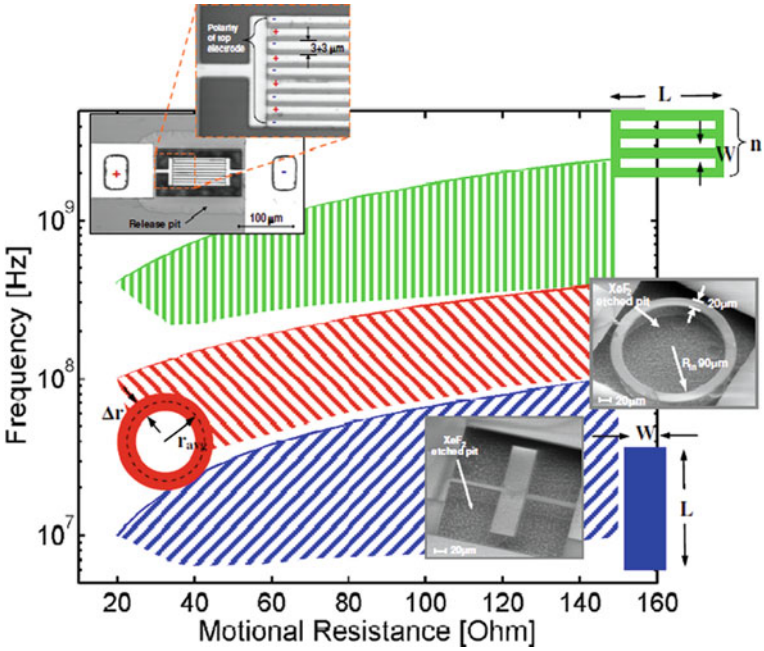


Fig. 5.43 Plot illustrating suggested geometries for AlN RF MEMS contour-mode resonators for various frequency ranges [135] (Reprinted with permission. Copyright 2006 IEEE)

These resonators have also been successfully implemented as bandpass filters [128]. Electrically coupled resonators, in a ladder configuration, have been demonstrated with rectangular plate resonators at 93 MHz and with ring resonators at 236 MHz (see Table 5.8). The filters are comprised of individual series and shunt one-port resonators configured as cascaded L networks. Within each L network, the series resonance of the series resonator is designed to coincide with the parallel resonance of the shunt resonator in order to optimally form the passband of

Table 5.8 Summary of performance of AlN contour-mode resonators [1]

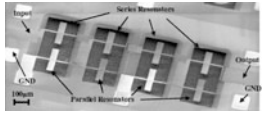
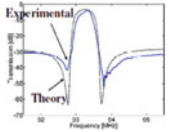
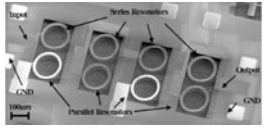
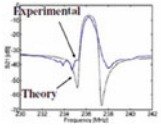
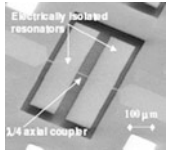
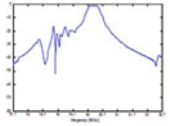
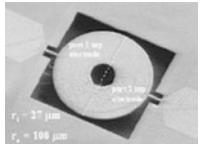
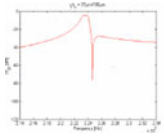
	Filter Photograph	Data	Performance
Electrically coupled ladder [9]			$f_0 \sim 93.2$ MHz $BW_{3dB} \sim 305$ kHz % $BW_{3dB} \sim 0.33\%$ $BW_{20dB} \sim 671$ kHz I.L. ~ -4 dB Rejection ~ 27 dB $R_{term} \sim 2$ kΩ
Electrically coupled ladder [9]			$f_0 \sim 236.2$ MHz $BW_{3dB} \sim 605$ kHz %$BW_{3dB} \sim 0.26\%$ $BW_{20dB} \sim 1.8$ MHz I.L. ~ -7.9 dB Rejection ~ 26 dB $R_{term} \sim 1$ kΩ

Table 5.8 (continued)

	Filter photograph	Data	Performance
Mechanically coupled array [10]			$f_0 \sim 40$ MHz $BW_{3dB} \sim 392$ kHz $\%BW_{3dB} \sim 0.98\%$ $BW_{20dB} \sim 1.1$ MHz I.L. ~ –1.5 dB Rejection ~ 20 dB $R_{term} \sim 1.5$ kΩ
Dual mode resonator [1]			$f_0 \sim 22.4$ MHz $BW_{3dB} \sim 112$ kHz $\%BW_{3dB} \sim 0.5\%$ $BW_{20dB} \sim 358$ MHz I.L. ~ –4.8 dB Rejection ~ 30 dB $R_{term} \sim 2.5$ kΩ

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the filter. The bandwidth of the filter is related to the difference between the series resonance of the shunt resonator and the parallel resonance of the series resonator. This requires a frequency shift between the two resonators, within each L network, by as much as a few percent and as little as a few tenths of a percent. Piazza, et al. [128] accomplished this by modifying the geometry of the bottom Pt electrode to affect mass loading of the composite resonators between the series and shunt devices within the filter. These devices show very good RF performance with further gains expected with optimization. The rectangular plate-based filters, featuring eight resonators, display 4 dB of insertion loss and 27 dB of out-of-band rejection at 93 MHz with 2 kΩ termination resistances. The filters based on eight ring resonators display 8 dB of insertion loss and 26 dB of out-of-band rejection at 236 MHz with 1 kΩ termination resistances.

The fabrication of these AlN contour-mode filters utilizes a four-mask CMOS compatible process (see Fig. 5.44). The process begins with the deposition of a LPCVD low-stress nitride buffer layer onto a silicon substrate. A 100 nm RF sputtered Pt bottom electrode layer is patterned by liftoff. The AlN films are deposited with a single-module Advanced Modular Sputtering (AMS, Goleta, CA) PVD sputter tool. Bottom electrode vias through the AlN film are defined with a wet etch of heated phosphoric acid. The wet etch provides a modest slope etch profile, facilitating the ensuing top electrode contact required for properly configuring the series and shunt resonators of the filter. A dry etch is used to define the top Al electrode. The AlN layer is patterned with a hard mask of low-temperature oxide and a chlorine-based dry etch. In addition, the top electrode is passivated by a ~30 nm layer of Nb during the AlN etch step. The Nb layer, remaining LTO hard mask, and the low-stress nitride layer beneath the resonators are removed during the subsequent CF_4-based dry etch. Finally, xenon difluoride is used to release the devices and to remove any remaining low-stress nitride from beneath the resonators.

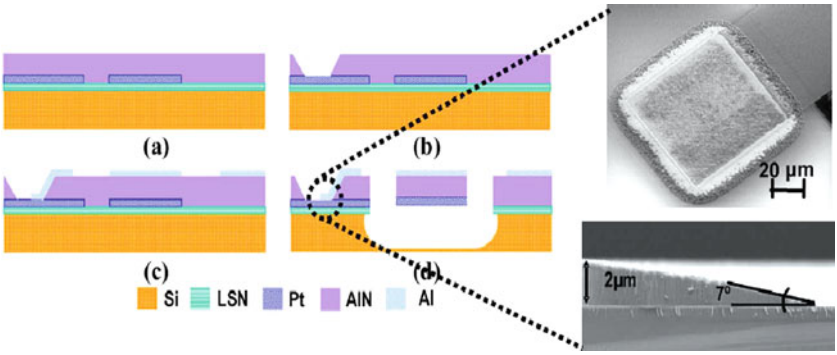

Fig. 5.44 Illustration of the fabrication process used to demonstrate AlN electrically coupled filters and images of the wet etch bottom electrode via [128] (Reprinted with permission. Copyright 2007 IEEE)

5.3 Ferroelectrics: PZT

This section concentrates on the leading ferroelectric material used in thin-film piezoelectric MEMS: lead zirconate titanate ($PbZr_xTi_{1-x}O_3$) or PZT. Possessing a piezoelectric coefficient nearly an order of magnitude larger than its nonferroelectric counterparts, PZT is the ideal candidate for devices requiring large displacements or forces. The goals of this section include an analysis of the deposition of these materials, patterning techniques, identification of device design and processing concerns, and finally a detailed subsection covering examples of PZT devices including a case study on PZT actuators for RF switching applications.

5.3.1 Material Deposition

PZT thin films have been successfully deposited by a wide variety of processes with a majority of the early development done through various sputtering techniques with a strong focus on RF or ion-beam deposition using bulk ceramic targets [136–139]. Current research efforts primarily utilize sputtering [140, 141], metal-organic-chemical vapor deposition (MOCVD) [142–144], and chemical solution deposition techniques [145–151] with many of the techniques summarized in Table 5.9. PZT deposition methods require strict control of the stoichiometry to prevent nucleation of nonferroelectric fluorite and pyrochlore structures [152, 153]. Furthermore, lead oxide (PbO) becomes highly volatile above 500°C so one must take care to provide enough excess lead to compensate for lead loss through the release of PbO during any high-temperature processing and annealing [154].

A variety of substrates can be used for PZT deposition. However, there are requirements for both the substrate and/or metallization layers. Growth of PZT is strongly nucleation controlled and with proper control of the nucleation, crystal orientation of the film can be manipulated [155, 156]. Single crystal substrates (i.e., MgO, $SrTiO_3$) can be used to nucleate epitaxial, single-crystal PZT thin films [157].

For most MEMS applications, silicon is the substrate of choice. When using Si it is important to prevent the formation of lead silicide at the substrate interface by using buffer layers and/or metal layers. In most instances, a layer of silicon dioxide is used as a buffer layer in combination with a bilayer of Ti/Pt to serve as the base electrode for the PZT deposition. With the lattice constant of platinum being close to that of PZT (2–3% mismatch for *c*-axis-oriented PZT), Pt can be an excellent template for (111) oriented PZT films as Pt tends to grow with a strong (111) texture. In order to maximize the texture within the Pt, the preferred material stack is $SiO_2/TiO_x/Pt$ [158]. The layer of TiO_x serves as a buffer layer and template that allows a higher degree of texture within the Pt. For detailed information on the method required for achieving highly textured (111) Pt, the readers are directed to [158] with one of the key figures reproduced in Fig. 5.45. Methods of manipulating the texture of the PZT away from (111) orientation when using Pt layers are discussed later within this section.

Table 5.9 Deposition methods and parameters for PZT thin films

Deposition parameter	DC sputter (reactive)	RF sputter	MOCVD	MOCVD	CSD
Target stoichiometry	Pb, Zr, Ti (3 metal targets)	$Pb_{1.20}(Zr_{0.53}Ti_{0.47})O_3$			
Excess Pb %		20			10 and 30
RF power (W)		100			
Bias (V or W)					
Pressure (Pa or T)		1–2	5 T		
Gas		O_2 (1–3 sccm)	O_2 (1 L/min)		O_2
Deposition rate (nm/min)		10–20	12		
Temperature (°C)	570 followed by post-dep RTA	550–700	550	540	RT→350 →650
References	[140]	[140, 160]	[144]	[143]	[149]

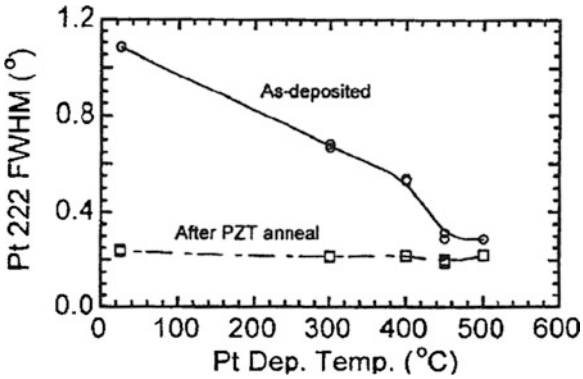

Fig. 5.45 Texture, FWHM of the sputtered Pt (222) peak, as a function deposition temperature and after thermal processing of a PZT film deposited atop the Pt film [158]

There are several metal and/or conducting oxides (i.e., Ru and RuO_2 and Ir and IrO_2) that can be used in place of Pt. These alternative electrodes can exhibit a higher resistance to Pb interdiffusion and thus provide a better barrier. Oxide electrodes are commonly used for the top electrode to reduce ferroelectric fatigue (reduction of switchable polarization with bipolar cycling). Note, ferroelectric fatigue has very little dependence on the bottom electrode material. In a vast majority of MEMS applications, bipolar switching will be avoided with typical operation relying on unipolar drive (see Section 5.1.3.10).

Sputter deposition of PZT thin films has been completed through either reactive deposition using three metal targets (Pb, Zr, and Ti) or RF sputtering using ceramic targets. In either case, PZT thin films with excellent ferroelectric and piezoelectric properties can be obtained. One challenge with sputter deposition is accurate control of the Pb and O content within the films. Lead has a higher sputter yield and higher volatility (i.e., PbO) compared to Zr and Ti. As a result, the lead loss must be compensated with either higher fluxes sputtered from pure Pb targets or excess Pb incorporated in ceramic targets. An additional item of note is the substrate temperature during deposition. The use of high temperatures during deposition results in higher Pb loss and typically requires higher excess lead content targets. If the substrate temperature can be maintained greater than 600°C, pure perovskite-phase PZT thin films can be achieved. Otherwise, a crystallization anneal is required on the sputtered film to convert the deposited layer into the desired perovskite phase.

MOCVD processes for PZT thin films have been researched as a key technology for mass production of ferroelectric random access memory (FeRAM) especially for device architectures requiring exceptional step coverage. For PiezoMEMS applications, there has been limited information reported on the piezoelectric properties MOCVD-deposited thin films. For a summary of the MOCVD deposition process readers are directed to [142, 144] for more detail.

Chemical solution deposition (CSD) methods for ferroelectric thin films have been developed based on a variety of methods (i.e., sol-gel and metallorganic decomposition) and precursors [159]. The CSD techniques can be categorized into

three main groups: sol-gel, chelating process, and metallorganic decomposition [149, 150]. The two most widely used approaches are based on a sol-gel approach using 2-methoxyethanol as a solvent and the inverted mixing order process using methanol as a solvent. Sol-gel methods have been primarily based on the research of Budd et al. in 1985 [145].

With the inverted mixing order (IMO) process, the lead, titanium, and zirconium precursors are combined in the opposite order from those developed in the original sequential addition process by Budd et al. [145, 160, 161]. In addition, the solvent used for the IMO process is methanol with slight additions of acetic acid and deionized water for additional solution stability. The use of methanol instead of 2-MOE enables a less toxic solution preparation and deposition process for the user [159].

The most heavily researched processes for the deposition of PZT films uses 2-MOE as a solvent and lead acetate trihydrate, titanium iso-propoxide, and zirconium n-propoxide as the precursors [145, 162, 163]. This process has been used to produce PZT films with the highest piezoelectric coefficients to date. A general version of the 2-MOE-based solution process flow is highlighted in Fig. 5.46. To begin, the lead precursor (lead acetate trihydrate) is dissolved in 2-MOE followed by vacuum distillation to remove the water. The dehydrated lead acetate is allowed to redissolve in a portion of the 2-MOE solvent before being mixed with the Zr and Ti precursors. Prior to being added to the lead precursor, the Zr and Ti precursors are mixed in the desired stoichiometric ratio at room temperature with 2-MOE. The combined solution is refluxed for 2–3 h at 120°C using a rotary evaporator or comparable setup. Next, the solution undergoes a short vacuum distillation to remove a small amount of reaction by-products and adjust the concentration, typically 0.4 M. The final step is to add 4 volume percent of formamide, which serves as a drying control

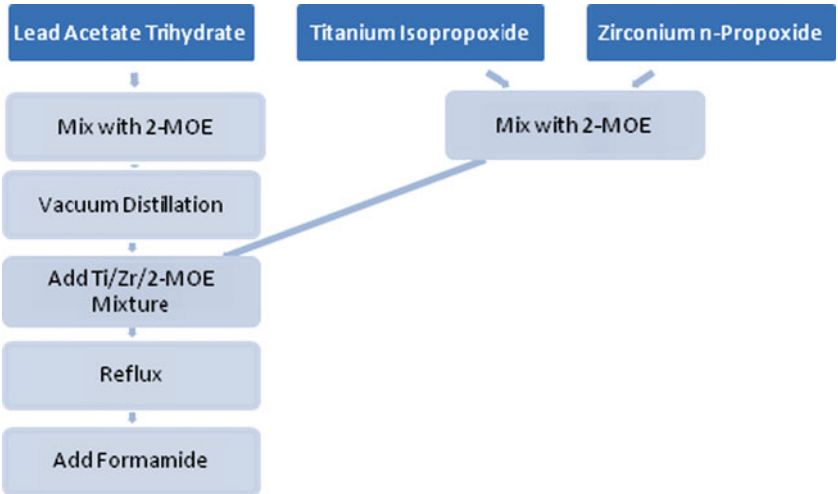

Fig. 5.46 Schematic process flow for creating a 2-MOE-based solution for PZT thin films

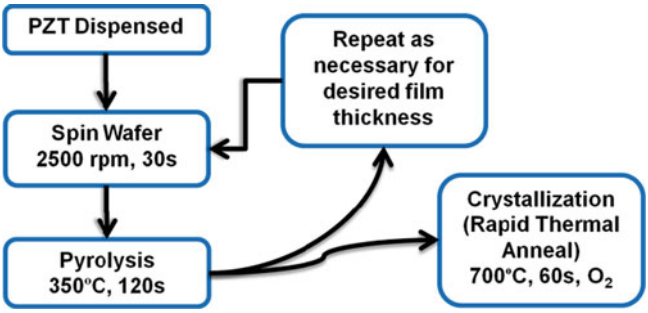

Fig. 5.47 Deposition and thermal treatment process flow for chemical solution deposition of PZT thin films based on a 2-Methoxyethanol solvent system

agent [164]. Additionally, a small percentage of acetylacetate may be added to the solution to assist in the long-term stability of the solution [165].

Regardless of the solution chemistry, the deposition processes are quite similar and graphically represented in Fig. 5.47. The only discrepancies are minor changes to the pyrolysis temperature or the crystallization temperature. The deposition begins by placing the solution into a syringe configured with a 0.1–0.2 μm PTFE (polytetrafluoroethylene) filter. The solution is statically dispensed onto the substrate and then spun to achieve a uniform film thickness across the substrate. Following the spin, the film is pyrolyzed on a hot plate to remove the volatile organics. The spin and pyrolysis steps are repeated as required (i.e., one to four layers) prior to the crystallization anneal in flowing oxygen. Using a 0.4 Molar solution, a four-layer spin process typically yields a final film thickness close to 0.25 μm. The process is continuously repeated until the desired film thickness is achieved.

Regardless of deposition method, there are several key material parameters with which to judge the quality of the PZT thin film. The first is the crystalline quality of the film via X-ray diffraction (XRD). The best quality piezoelectric films will possess a high degree of texture in the (100)/(001) orientation (see Fig. 5.48). The easiest method of assuring a high degree of (100) texture is through templating the nucleation and growth with a $PbTiO_3$ seed layer and proper attention to the amount of excess lead present during any high-temperature annealing or crystallization processes [155, 163]. An example XRD pattern of a highly textured CSD PZT thin film is shown in Fig. 5.49.

Optimizing material quality and properties requires controlling the stoichiometric gradients through the thickness of the PZT film. Figure 5.50 illustrates the importance of controlling these gradients, as these gradients represent deviations of the average properties of the film from the intended composition. As stated earlier, PZT films are strongly nucleation controlled. With heterogeneous nucleation occurring at the electrode interface, Ti rich compositions nucleate first [155]. The end result is a sawtooth Zr/Ti gradient through the PZT thickness with a Ti rich layer at the electrode interface and a Zr-rich layer at the film surface (see Fig. 5.50) [149]. To compensate for the gradient, Calame and Muralt developed a process to

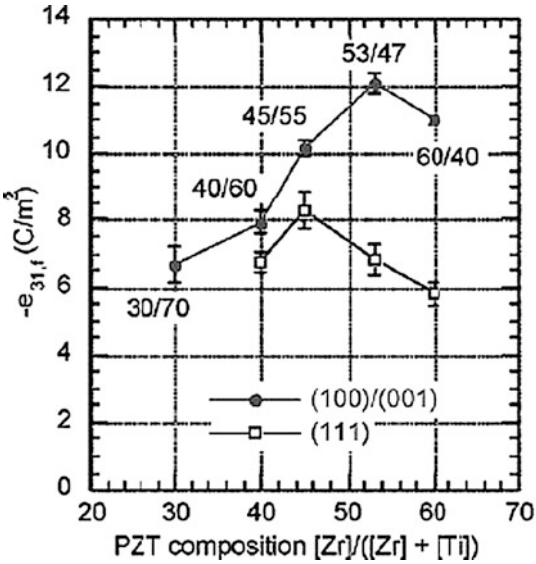

Fig. 5.48 Transverse piezoelectric stress constant, $e_{31,f}$, of a 1 μm PZT thin film as a function of Zr/Ti ratio for both (100)/(001) and (111) oriented thin films [163] (Reprinted with permission. Copyright 2003, Elsevier)

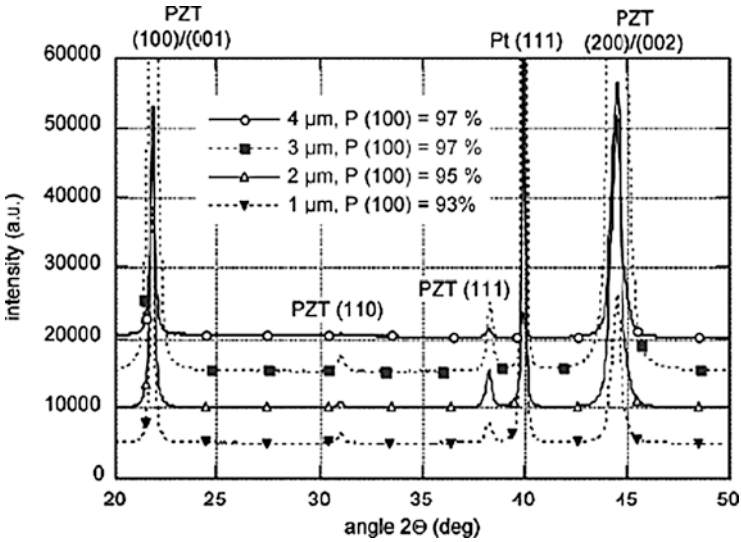

Fig. 5.49 Θ–2Θ X-ray diffraction pattern for PZT (53/47) thin films (1–4 μm) using a $PbTiO_3$ seed layer to promote a highly textured (100) orientation [163] (Reprinted with permission. Copyright 2003 Elsevier)

reduce the gradient by manipulating the stoichiometry of each of the four CSD layers (63, 58, 48, and 43% Zr content) deposited prior to the crystallization step [149]. As shown in Fig. 5.50, the average composition through the entire 2 μm thickness closely resembles the MPB desired composition of 53/47.

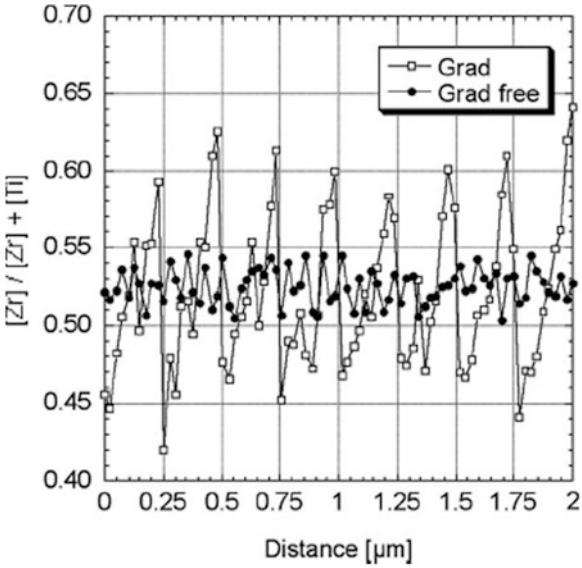

Fig. 5.50 Zr content in two different PZT (53/47) films, one with a standard 2-MOE process using a crystallization anneal every four layers and the other using an optimized process to reduce the Zr/Ti gradient in the film [149] (Reprinted with permission. Copyright 2007 American Institute of Physics)

Table 5.10 Material properties as a function of deposition method

Technique	Stoichiometry (Zr/Ti)	P_r (μC/cm^2)	E_c (kV/cm)	$e_{31,f}$ (C/m^2)	d_{33} (pC/N)	ε_{33}	tan δ	References
MOCVD	35/65	43	130					[143]
	30/70	22	65					[144]
Sputter–RF magnetron	50/50	37.4	79		100	800–1000	0.02	[140, 166]
Inverted mixing order (IMO)	53/47	26.2	43.3					[160]
2-MOE	53/47			–12.0	85	1180	0.029	[163]
				–17.7		1650	0.023	[149]

For comparison, a list of the material properties achieved for each deposition method has been compiled in Table 5.10. Note, that quite often, the ferroelectric property, namely the remnant polarization, is similar for the different techniques. However, the piezoelectric coefficients tend to be higher in the highly textured, gradient controlled CSD techniques.

5.3.2 Patterning Techniques

Patterning PZT thin films along with many other ferroelectrics remains one of the more challenging aspects of incorporating these compounds with MEMS. Not only are these compounds rather difficult to etch and pattern but contamination from the

heavy metal elements, especially lead, poses additional problems for most cleanrooms. Specific to PZT, regardless of the Zr/Ti ratio, this material can be etched with all of the common etching techniques including wet processing as well as physical and chemical etching as indicated in Table 5.11.

Table 5.11 Etch parameters for PZT thin films

Etching parameter	ECR/RIE	ICP	ICP	Wet	Ar ion mill
RF power (W)	10–200	400–800	500–800		150
Bias (V or W)	100–1000 V	100–400 V	200–350 V		36 V
Pressure (Pa or mT)	$5e^{-4}$ to 1 Pa	1–10 mT	0.1–2.0 Pa		0.7 mT
Gas(es)	CCl_4, CF_4, Ar	Cl_2/C_2F_6/Ar	BCl_3:Ar Cl_2:Ar	BOE:2HCl: $4NH_4Cl$: $4H_2O$ + $2HNO_3$:H_2O	Ar
Etch rate (nm/min)	20–95	100–180	63–193	960	25
Resist selectivity (PR/PZT)	3:1–13:1	1.5–3:1	3–6:1	1.5:1	1:1
References	[172]	[174]	[175]	[169]	[182]

Wet etching techniques remain one of the easiest solutions to patterning PZT especially when selectively stopping the etch on a platinum electrode. However, this technique is limited to larger areas (several microns to tens of microns) because most etch chemistries are highly isotropic or can even have faster lateral etch rates. Typical chemistries involve mixtures of hydrochloric (HCl) and hydrofluoric (HF) acids resulting in combinations of fluorine and chlorine containing by-products [167–169]. One of the most common chemistries with relatively high etch rate and excellent selectivity to platinum is a mixture of deionized H_2O:HCl:HF (2:1:0.05). The HCl acid is used to remove lead and titanium whereas the HF is used to remove titanium and zirconium. One problem that can occur with this etch combination occurs in films with excess lead where a white powdery lead residue remains on the wafer surface [168]. This lead-rich residue can be removed by adding small amounts of ammonium chloride and/or nitric acid to the solution [168]. Note that this etchant has a lateral etch rate nearly two to three times that of the film thickness.

Chemical and physical etching via reactive ion etching (RIE) and ion-milling can provide the necessary dimensional control necessary for creating MEMS and NEMS structures. Similar to the wet etch chemistry, reactive ion etch techniques utilize combinations of fluorine and chlorine containing compounds (such as CF_4 and CCl_4) [153, 170–172]. A major challenge with a purely chemically based RIE is the extremely low volatility of the Zr and Ti by-products, namely ZrF_4, $ZrCl_4$, TiF_4,

and $TiCl_4$. To counter, the most successful etching techniques use combinations of RF bias power in excess of 50 W, low pressures (<0.1 Pa), and elevated temperature. One technique to etch the PZT uses an electron cyclotron resonance/radio frequency (ECR/RF) reactor with 40% CCl_4, 40% CF_4, and 20% Ar gases [153]. As shown in Fig. 5.51, this technique can achieve etching rates approaching 100 nm/min using 100 W_{RF} operating at a pressure of 1 mPa. Another chemistry for RIE is outlined by the ferroelectric random access memory community using inductively coupled plasma (ICP) RIE reactors with 70% BCl_3 and 30% Ar gas [173–175]. In addition to etching PZT layers, RIE can be used to etch the electrode layers such as Pt, RuO_2, and IrO_2. In general, the leading etch chemistries use chlorine containing gases such as Cl_2, CCl_4, and BCl_3 with the etch mechanism being mostly physical in nature [153, 175–177].

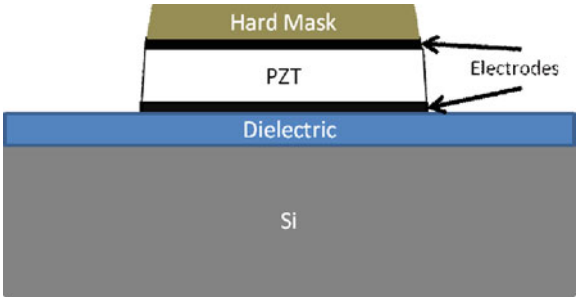

Fig. 5.51 Cross-section image/schematic of an FRAM capacitor (Ir/IrOx/PZT/IrOx/Ir) patterned using a single-layer hard etch mask of TiAlN

The two biggest challenges with a chemical RIE approach to patterning PZT are controlling re-deposition of the nonvolatile etch by-products and achieving the necessary resist selectivity. Processing at higher temperatures and using low pressures combined with high-throughput vacuum pumps increases the percentage of the by-products remaining in the gaseous phase. However, increasing the temperature causes severe resist degradation or even carbonization of the photoresist. As a result a hard mask needs to be employed. Further evidence of this is shown in Figs. 5.51 and 5.52 where resist selectivity dramatically decreases with increases in processing pressure or incident ion energy or RF bias. Resist degradation is yet another challenge with RIE etches of PZT. To preserve the resist integrity, any masking must be done with either hard-cured photoresist or hard masks to avoid degradation in soft-cured photoresist. Early work on hard masks included TiO_2 coatings with the FRAM community moving toward TiN or TiAlN coatings [178, 179]. The use of hard coatings enables a single mask layer etching process to etch the entire capacitor,electrode/PZT/electrode (see Fig. 5.53). The same process can be used for MEMS actuators. However, care must be taken to account for the elevated voltages that the actuators require compared to that of FRAM. The gap separation between the two electrode layers is defined by the PZT thickness. Because this separation can be in the range of 0.25–2 μm, breakdown across the air gap becomes a concern during device operation. For example, actuators comprised of a 0.5 μm PZT film

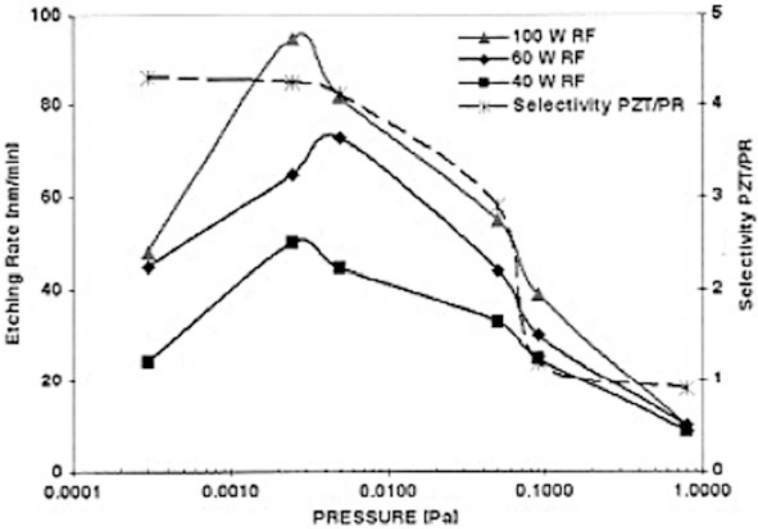

Fig. 5.52 Etching characteristics of PZT thin films as a function of RF bias power using an electron cyclotron resonance/radio frequency (ECR/RF) reactor [180] (Reprinted with permission. Copyright 2000 Taylor & Francis)

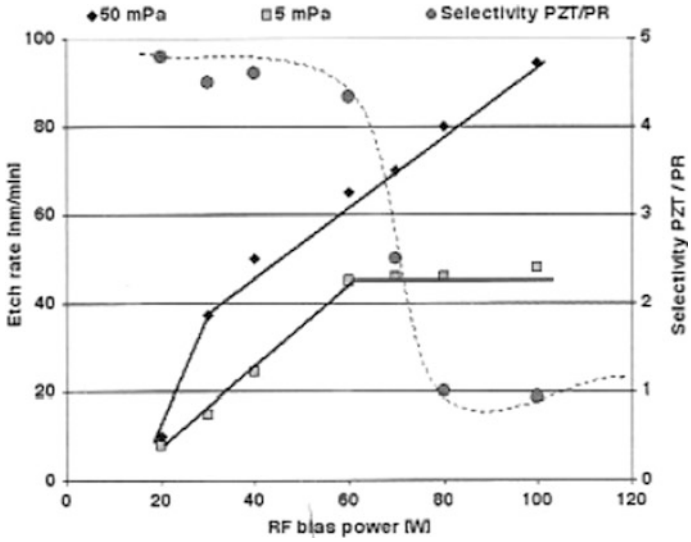

Fig. 5.53 Etching characteristics of PZT thin films as a function of processing pressure using an electron cyclotron resonance/radio frequency (ECR/RF) reactor [180] (Reprinted with permission. Copyright 2000 Taylor & Francis)

with Pt electrodes fabricated with a single etch process have breakdown voltages on the order of 10 V (~200 kV/cm). In contrast, employing a multiple step etching process to define the actuator increases the breakdown voltage for a 0.5 μm thick

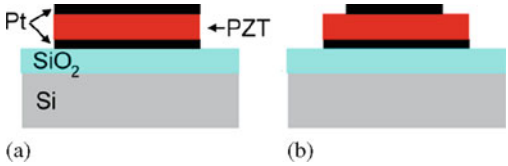

Fig. 5.54 Schematic cross section of PZT stack actuators patterned using (**a**) a single etch process and (**b**) a multiple step etch process

PZT actuators to approximately 100 V (~2000 kV/cm). This effect is primarily due to the fact that the PZT overlap required for the multistep etch/masking process increases the distance between the top and bottom electrodes (see Fig. 5.54).

The final method of patterning PZT thin films is through a physical etch using Argon ion-milling. Although this technique does not provide any significant selectivity to photoresist, PZT, or the electrode layers, it has several key advantages including the ability to etch the entire metal/PZT/metal stack and variable control of the angle of incidence [181]. For hard-to-etch compounds, especially materials with low volatility such as PZT and Pt, the accelerated Ar ions can be used to break the atomic bonds, and the variable angle control is used to push free atoms away from the wafer surface. Furthermore, the angle of incidence can be altered during the final stages of the etching to remove any re-deposited materials. Similar to the chemical-based RIE procedures, the masking material for the ion-mill must either be hardened photoresist or a hard mask as ion-damage and re-deposited heavy metal ions prevent clean removal of a soft photoresist. Although the ion-mill generally has poor selectivity and a difficulty to accurately endpoint on the desired layer, an ion-mill reactor can be configured with a secondary ion mass spectrometer (SIMS) endpoint detection system. The SIMS system analyzes the etched material as it is removed from the wafer surface and yields an accurate depiction of the depth of the current etch. An example of the endpoint detection is illustrated in Fig. 5.55 for a sample etching the top Pt electrode stopping on the PZT and for a sample etching the PZT and stopping on the bottom Pt electrode.

5.3.3 Device Design Concerns

Designing piezoelectric-based MEMS with PZT poses several challenges in the realm of device processing and electromechanical design. The processing challenges include thermal processing budget, residual stress gradients, processing induced damage, and ferroelectric domain poling. Achieving high-quality PZT thin films for piezoelectric actuators nominally requires annealing conditions with temperatures in the range of 600–750°C as previously discussed. As a result, it is imperative to thermally stabilize the underlying materials not only to ensure their compatibility with the processing temperature but also to minimize changes in residual stress. As an example, the changes in residual stress with plasma-enhanced chemical vapor deposited (PECVD) silicon dioxide (SiO_2) and a sputtered $Ti/TiO_2/Pt$ thin film on a PECVD SiO_2 are illustrated in Fig. 5.56. The first plots

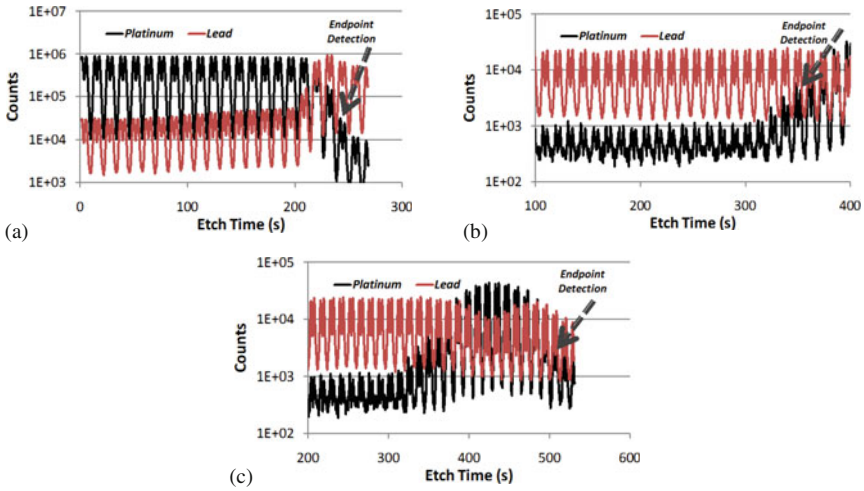

Fig. 5.55 Examples of using SIMS endpoint detection in conjunction with ion-milling of (**a**) Pt etching and stopping on a PZT thin film using the falling edge of Pt, (**b**) etching PZT and stopping on a Pt thin film using the rising edge of Pt, and (**c**) etching PZT and Ti/Pt stopping on the underlying SiO_2 using the falling edge of Pt. *Note*: the double peaks in the SIMS signal are the result from monitoring two substrates that are rotated under the beam during the etching process

compare the initial and second anneal of a PECVD SiO_2 and the next two plots compare the initial and second anneal of a Ti/TiO_2/Pt thin film. As shown, significant changes in the room temperature film stress result from the initial thermal processing whereas the stress remains stable in subsequent anneals [182].

Two important characteristics that result from the use of multilayer composite structures for a piezoelectric thin film actuator or sensor are residual stress gradients and thermally induced deformations. Each film within the composite typically has different magnitude stress values resulting primarily from the coefficient of thermal expansion mismatch with the substrate (in most cases, silicon). Table 5.12 is an example illustrating the ranges of film stress in a six-layer composite consisting of combinations of silicon dioxide, silicon nitride, a titanium/platinum bi-layer, PZT, and Pt. The stress gradient requires careful consideration in the design of piezoelectric devices. For devices requiring flat stable structures, improper design can lead to structures with drastic undesired deformations (see Fig. 5.57). Similarly, the stress gradient can be controlled to enable device specific attributes such as restoring force. Proper stress gradient control created repeatable negative curvature in a PZT actuator used to create piezoelectric switches [29, 182].

The second aspect of the multilayer stack is thermally induced deformations resulting from differences in the coefficient of thermal expansion between the layers in the composite. Using the same materials listed in Table 5.12, an example of the thermal deformations is illustrated in Fig. 5.58. As shown, deformations as large as 4 μm are observed from –50 to 100°C for an approximately 150 μm long composite

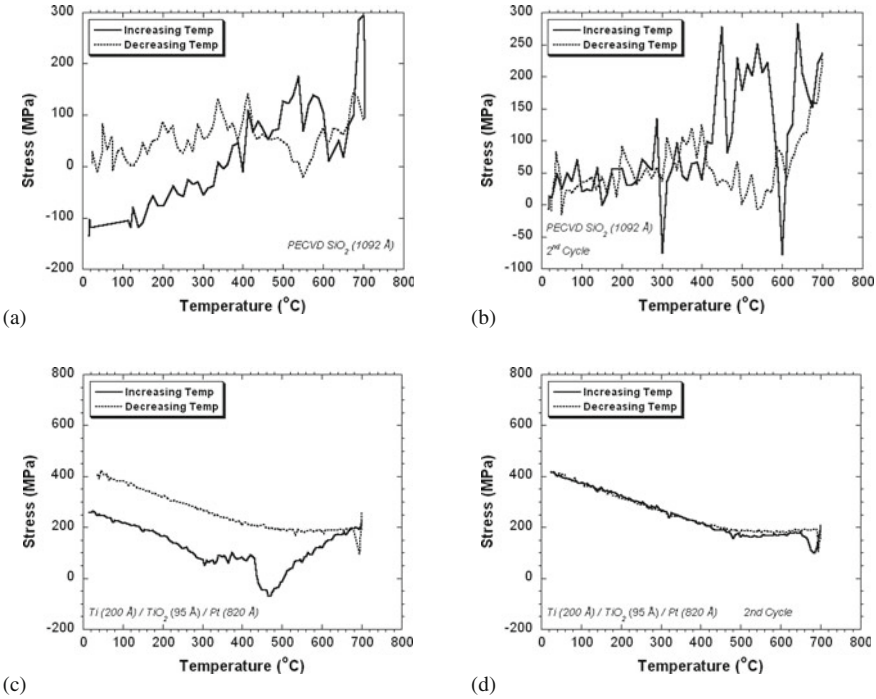

Fig. 5.56 Change in residual stress as a function of temperature for the initial and second thermal anneal for (**a**) and (**b**) PECVD SiO_2 and (**c**) and (**d**) $Ti/TiO_2/Pt$ on a thin layer of SiO_2

Table 5.12 Average residual stress measured on each of the thin films used in the composite actuator for a PZT switch [29]

Film	Nominal thickness (Å)	Stress (MPa)	Std Dev (σ)
SiO_2	1000	33.1	10
Si_3N_4	500	1100	200
SiO_2	3500	33.1	10
$Ti/TiO_2/Pt/TiO_2$	160/90/1640/10	323	83.3
PZT	5000	175	7.26
Pt	1050	76.3	16.5

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actuator comprised of a 0.5 μm elastic layer ($SiO_2/Si_3N_4/SiO_2$) and 0.5 μm PZT (52/48) thin film using Ti/Pt and Pt electrode layers.

Another area of concern for PZT-based MEMS devices is degradation in the material properties during device fabrication. The research on ferroelectric random access memory has advanced the understanding of the leading degradation mechanisms including ion damage, H_2 damage, and surface contaminants [181, 183, 184]. In many instances, the manifestation of damage in the PZT can be observed through

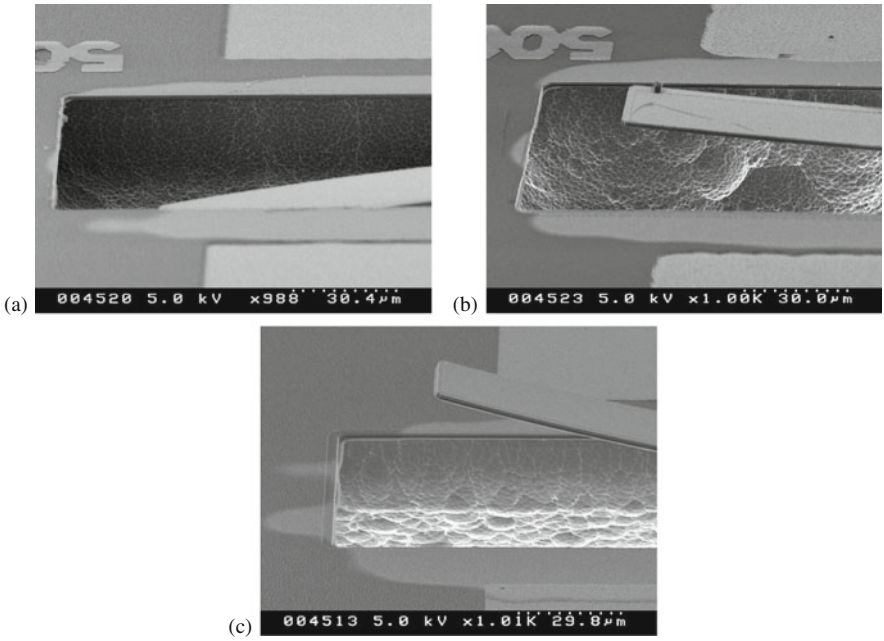


Fig. 5.57 SEM images illustrating a wide range of curvature achievable in a multilayer PZT thin film composite consisting of the layers outlined in Table 5.12. The change in curvature from (**a**) to (**c**) is achieved by simply moving the location of the high-tensile stress silicon nitride layer from near the bottom of the composite toward the center

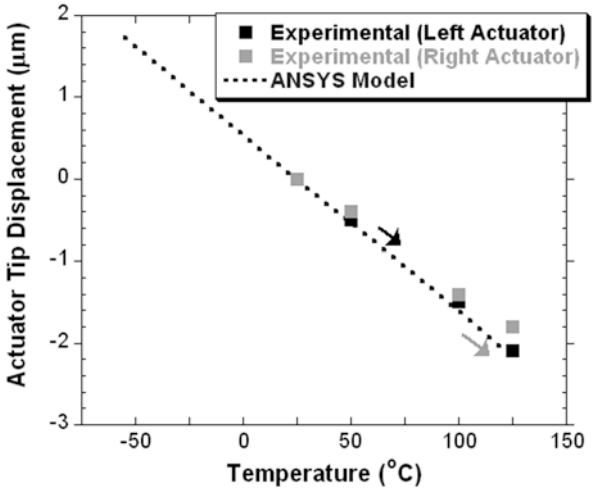


Fig. 5.58 Thermally induced deformations (experimental and finite element predictions using ANSYS) for a multilayer PZT thin film actuator consisting of $SiO_2/Si_3N_4/SiO_2/Ti/Pt/PZT/Pt$ [29] (Reprinted with permission. Copyright 2007 IEEE)

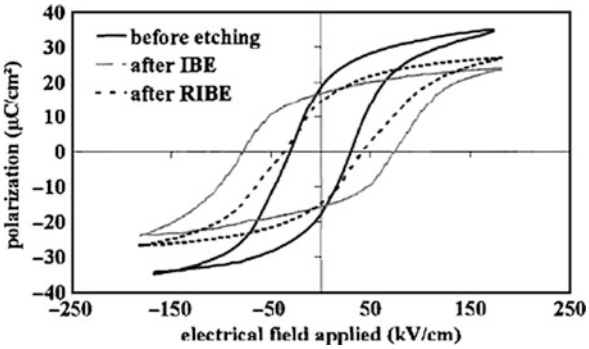


Fig. 5.59 Change in the polarization electric field hysteresis loop observed for virgin (before etching) PZT thin films, for a PZT film exposed to ion-milling (after IBE), and for a PZT film exposed to a reactive ion etch (after RIBE). For both etched samples, the testing was done after depositing and annealing a top Pt electrode layer on the etched surface [183] (Reprinted with permission. Copyright 2005 American Institute of Physics)

characterization of the ferroelectric and dielectric properties. In cases where the PZT surface is exposed to etch conditions and then electroded, reductions in the remnant polarization, increases in the coercive field, and decreases in the dielectric constant are observed resulting from the creation of a damaged surface layer lying beneath the top electrode (see Fig. 5.59) [181, 183]. The presence of the damaged surface layer is severely detrimental to the performance of the PZT and consequently the preferred process deposits and patterns the top electrode onto the as-deposited, pristine surface of the PZT film.

For piezoelectric devices patterned after the top electrode has been deposited, degradation remains a potential problem. The PZT sidewalls are damaged during the patterning process and can introduce defects into the material. More important, exposure to H_2 through contact with the hydrocarbons in photoresist and forming gas anneals introduces protons in the PZT via diffusion, adversely affecting the ferroelectric and dielectric properties through domain pinning.

Regardless of the damage created by processing, in most instances the ferroelectric and dielectric properties can be recovered using a thermal anneal. To approach full recovery, the anneal must be done above the Curie temperature of the ferroelectric. An example of how effective the recovery anneal can be is shown in Fig. 5.60. In this example, the material properties are recovered to the initial conditions using a 500°C anneal.

Another key aspect with PZT devices is the aligning of the ferroelectric domains or poling. Unlike the pure polar materials discussed previously (i.e., AlN and ZnO), the polarization in ferroelectric materials can be configured in a multitude of orientations. In order to optimize the piezoelectric coefficient of the PZT, the ferroelectric domains need to be aligned in a single preferred direction. For an actuator in a parallel plate configuration (d_{31} mode), the poling direction is along the film thickness. The most direct method of poling is the application of an electric field nominally

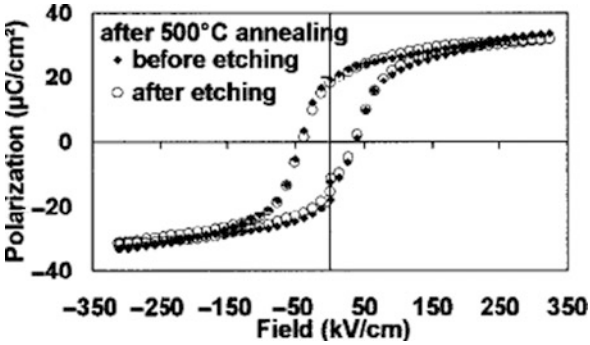


Fig. 5.60 Illustration of how high-temperature annealing can be used to recover the ferroelectric properties of PZT thin films after damage induced by the patterning process [181] (Reprinted with permission. Copyright 2002 American Institute of Physics)

3–4 times the coercive field for 10–15 min (i.e., 10–15 V for a 0.5 μm thick film). Additional techniques can be employed to further increase the piezoelectric coefficient including thermal poling and exposure to ultraviolet radiation consisting of a wavelength smaller than the absorption band gap of the material (i.e., approximately 365 nm for PZT). With thermal poling, the electric field for poling is applied and the PZT is held at temperatures approaching half of the Curie temperature or higher, nominally 125–150°C.

5.3.4 Device Examples

This section is intended to give the reader an understanding of the full capabilities of using PZT thin films for piezoelectric MEMS and how to specifically implement them in devices. Each of the main research areas of PiezoMEMS based on PZT is covered with detailed descriptions of several highlighted successful device demonstrations. In the last part of this section, a full case is undertaken for a piezoelectric RF MEMS microswitch.

In the area of sensors, PZT-based acoustic detection, infrared detectors, and energy harvesting have led the research community. As infrared detectors are based on the pyroelectric effect, or the change in polarization with temperature, and not piezoelectricity, the readers are directed to the research in [3, 185–187] for more detail. Acoustic detectors based on PZT have been demonstrated across a wide spectrum of frequencies. At low or audible frequencies, PZT thin-film-based microphones have been demonstrated with modest performance characteristics.

Another application for PZT-based acoustic sensors is nondestructive, real-time imaging using ultrasound array transducers. Thin- and thick-film PZT can be assembled to form arrays of piezoelectric micromachined ultrasonic transducers (pMUTs) [188–193]. Compared with conventional ceramic-based ultrasound systems, the

pMUTs offer the potential of smaller size systems resulting from MEMS fabrication, higher frequency for improved resolution (targeting 10–100 MHz), and better impedance matching to air and water [194]. To achieve their full potential, these arrays require a high electromechanical coupling factor enabling a large bandwidth, high efficiency, and minimal cross-element noise and high aspect ratio structures [195]. Similar to the low-frequency microphones discussed previously, membrane structures have been the typical incarnation of the pMUT. An example of such a device is in Fig. 5.61 in which a 4 μm thick PZT layer was combined with a 10 μm Si device layer to yield a transducer operating at 16.9 MHz with a quality factor Q of 25 in air and coupling factor, k^2 of 3% [195]. One limitation with conventional micromachining approaches is difficulty in achieving ultrahigh aspect ratios necessary for low MHz operation. Recent work on using spray-mist deposition of PZT solutions may be a means of achieving such technology (see [196]).

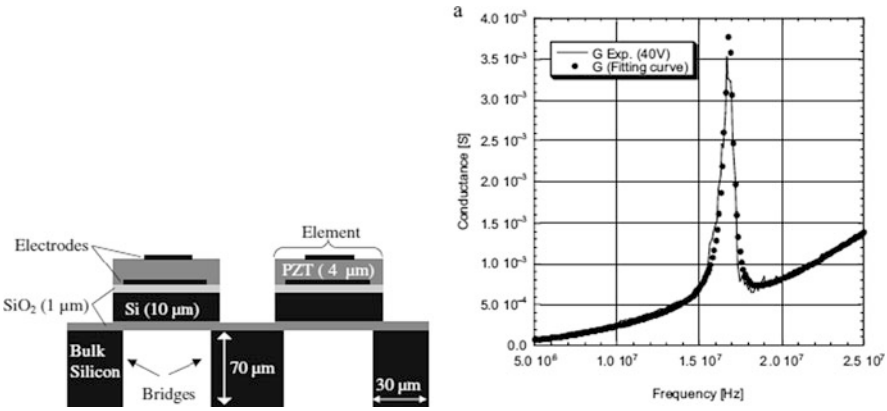


Fig. 5.61 Example of a pMUT comprised of a $Si/SiO_2/Ti/TiO_2/PZT/Cr/Au$ fabricated using Si DRIE to create the membrane [195] (Reprinted with permission. Copyright 2007 Springer Science+Business Media)

Actuation technology continues to be a strong area of development for piezoelectric MEMS including ultrasonic motors, micromirrors, RF devices, and robotics. Ultrasonic motors using thin-film PZT were investigated initially in the middle 1990s as possible replacements for actuators in wrist watches [197, 198]. For this device, a piezoelectric membrane stator is combined with a set of elastic fins on a rotor. As the resonant wave is generated within the membrane, it periodically compresses the elastic fins resulting in movement in the rotor as the elastic fins relax after contacting the membrane [199]. Similar to the previously discussed membranes, they were created using a combination of bulk and surface micromachining technologies. The device and data shown in Fig. 5.62 were from a membrane patterned using a KOH etch to create the Si membrane structure. This configuration using a 1 μm PZT film was able to achieve nearly 100 rad/s at 5 V, nearly two orders of magnitude higher velocity compared with an AlN stator of comparable frequency and a 2 μm AlN film.

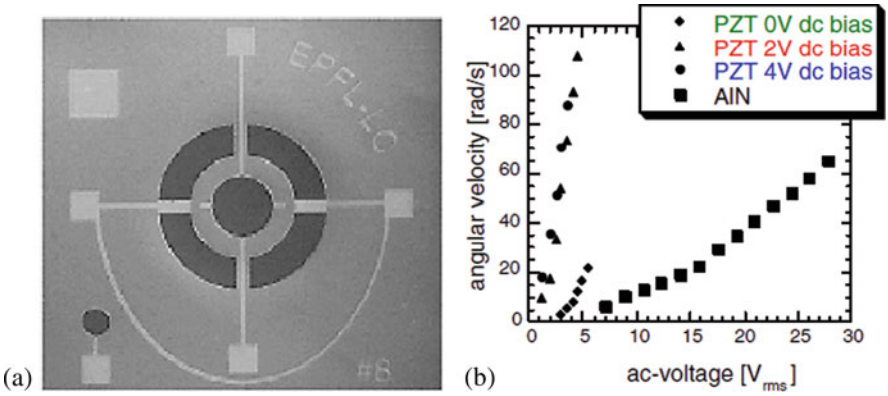


Fig. 5.62 (**a**) Optical micrograph of a PZT membrane configured for optimal vibration mode using electrode shaping to create an ultrasonic motor and (**b**) measurements of the motor angular velocity as a function of applied voltage [199] (Reprinted with permission. Copyright 2000 Institute of Physics)

Piezoelectric MEMS actuators represent a truly enabling actuator technology for millimeter-scale robotics. The actuation potential of PZT thin-film actuators is best represented in Fig. 5.63. As illustrated, PZT actuators are capable of achieving forces and displacement values in excess of other common actuation technologies for a given footprint. This particular actuator technology is being developed to enable ground mobile millimeter-scale robotics using a thin-film lateral actuation technology. This lateral actuation technology is created using manipulation of the PZT thin film relative to the neutral axis position of the beam actuator [16]. Such actuators can achieve mN force levels at micron displacements. Combining these actuators with single-crystal silicon tethers and end deflectors, it is possible to achieve in-plane rotations of 3–5° for a single element. Cascading these structures enables 45° in-plane rotations. Rotations at these levels begin to approach reasonable levels for the creation of biomimetic insect structures using a hexapod gate. Another area of interest for piezoelectric MEMS actuators is in microflight at the millimeter scale. For this application, actuators are being designed to create both the flapping and angle of attack motions used for flight by insects [84]. As shown in Fig. 5.64, wing actuators based on PZT thin films have been fabricated using a combination of surface and bulk micromachining techniques to yield wings capable of nearly 45° of total angular deflection at 5 V at a resonance frequency of 156 Hz. These wing actuators are approaching the metrics of many millimeter-scale insects for flight, including resonance frequencies in the 150–250 Hz range. Total angular deflection still requires additional research, as values in the range of 80–180° are desirable to achieve sustainable flight.

One of the key limitations of electrostatically actuated MEMS switches is the inability to combine a low actuation voltage with excellent DC and RF performance (i.e., contact force and insertion loss, respectively) and reliability. Attempts to lower the actuation voltage with electrostatic switches generally rely on reducing either

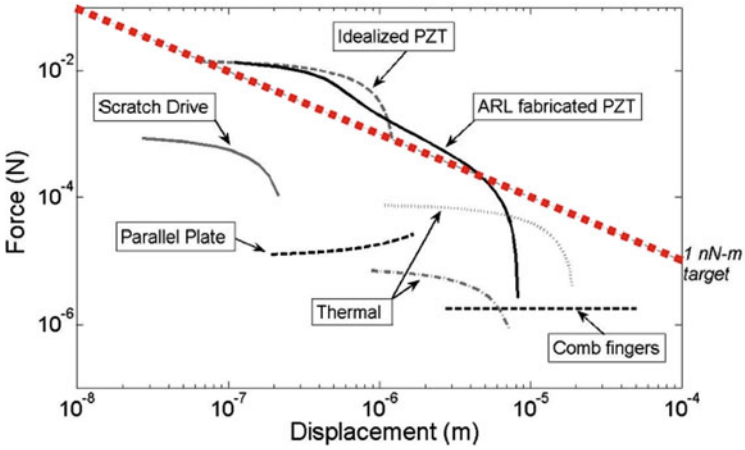
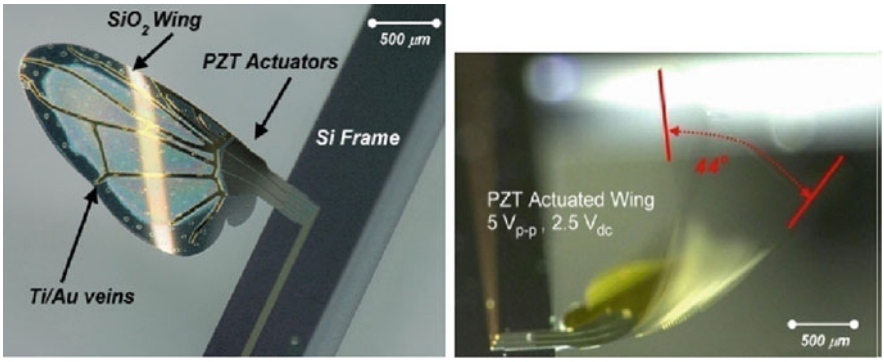


Fig. 5.63 Force-displacement plot of various actuation technologies for actuators confined to a $500 \times 500\,\mu m^2$ area. The straight line marks the target 1 nN-m minimum performance for mm-scale robotic applications [16] (Reprinted with permission. Copyright 2008 IEEE)



(a) (b)

Fig. 5.64 Images of a $PbZr_{1-x}Ti_xO_3$ (PZT) microelectromechanical systems actuated microwing (2.5 mm length) (**a**) at 0 V and (**b**) at resonance (156 Hz, 5 Vp-p), showing that resonant behavior amplifies the stroke. p-p, peak-to-peak [16] (Reprinted with permission. Copyright 2009 IEEE)

the mechanical stiffness of the released structures or the gap between the mechanical bridge/cantilever and the corresponding biasing pad [200]. Reductions in the stiffness can limit the restoring force of the switch and can lead to stiction failures [201]. Decreasing the electrode gap limits the high-frequency RF performance (in particular, the isolation in the open state for series switches) [202].

The first functioning piezoelectric MEMS DC relays were demonstrated by Gross et al. using in-plane poled PZT film actuators [203]. These devices used a cantilever beam with a supporting elastic layer, a PZT thin film as the actuator, and patterned gold structures to act as the electrodes (see Fig. 5.65). This device operated

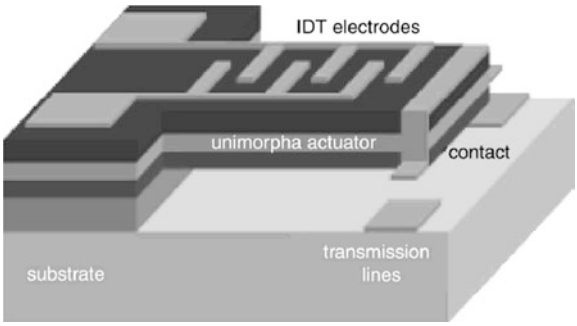


Fig. 5.65 Illustration of a thin-film PZT unimorph switch developed at Penn State University [203] (Reprinted with permission. Copyright 2003 American Institute of Physics)

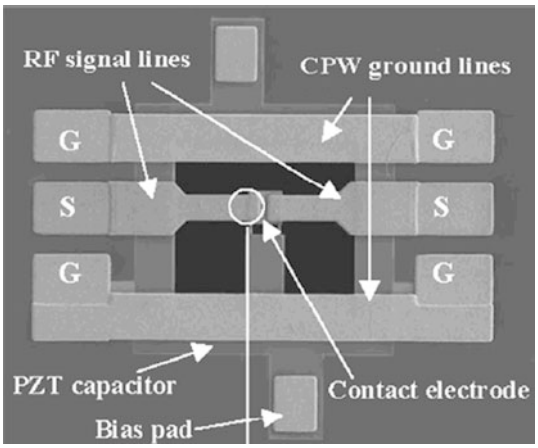


Fig. 5.66 SEM image of a bulk micromachined RF MEMS series switch using a thin-film PZT actuator to complete the signal path [204] (Reprinted with permission. Copyright 2005 IEEE)

as low as 20 V with a switching-on time as low as 2 μs. The first reported working RF MEMS switch using PZT thin films used bulk micromachining to release a unimorph actuator and a suspended transmission line [204, 205]. This design utilized a cantilever perpendicular to the wave propagation direction along the RF conductor of the coplanar waveguide (CPW). The switch operates as low as 2.5 V with an insertion loss better than 0.7 dB and isolation better than –21 dB up to 20 GHz (see Fig. 5.66).

One limitation with the RF switch actuators described above is the requirement for bulk micromachining. Surface micromachining is substantially cheaper and easier to integrate with other fabrication processes than bulk micromachining techniques [206]. The development of a surface micromachined, piezoelectric RF MEMS switch is discussed in full detail in the remainder of this section heavily leveraging the information described in [29, 182].

5.3.5 Case Study on the Design and Processing of a RF MEMS Switch Using PZT Thin-Film Actuators

The first few considerations for the design of a MEMS switch with PZT actuators are the position of the actuator relative to the microwave transmission line and the contact configuration. Referencing the description in Section 5.1.3.6, thin-film PZT generates an in-plane compressive strain at large electric field values when used in a parallel plate configuration (d_{31} mode). The resulting direction of actuation for a thin-film actuator is dictated by three main parameters, the magnitude and sense of the transverse piezoelectric stress constant, $e_{31,f}$ induced strain (force), and the position of the geometric midplane of the piezoelectric thin film relative to the composite neutral axis (moment arm). If the geometric midplane of the piezoelectric layer lies above the neutral axis, the induced piezoelectric strain will deflect the actuator up out of the wafer surface. Using this configuration, a switch can be designed with the electrical contacts of the switch residing above the actuators (see Fig. 5.67).

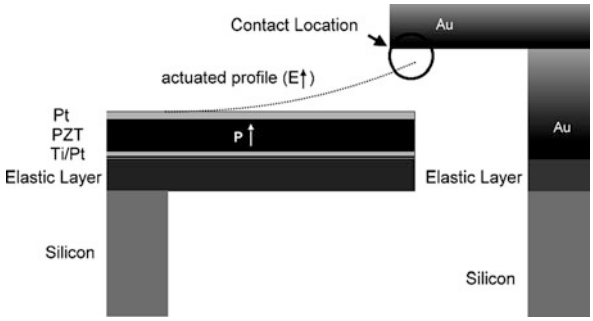


Fig. 5.67 Cross-section schematic of a PZT actuator and electrical contacts configured for use as switch

Another important consideration is that the PZT actuator is a multilayer composite comprised of at least four layers (elastic layer, metal, piezoelectric, metal) with each layer having significantly different coefficients of thermal expansion (CTE) and residual stress. The net result of such a structure is the potential for significant residual-stress-induced deformations in the unbiased actuator state and thermally induced deformations from the differences in CTE. The reader is directed to Section 5.3.3 for a description of the residual stress gradient and thermally induced stress deformations. For proper switch operation, a negative static curvature is desired and can be reproducibly fabricated using an elastic layer comprised of a three-layer composite of PECVD, SiO_2, and Si_3N_4. The negative curvature using an oxide/nitride/oxide elastic layer for the actuator not only enables switch operation with a normally open switch state but also ensures that thermally induced deformations do not cause the switch to open or close inadvertently.

With the design of the actuator complete, the RF transmission line should be designed to accommodate the actuator with minimal perturbation to the RF signal. Based on previous discussions on the piezoelectric strain generation in a parallel plate capacitor configuration, the switch contacts should be configured above the

actuators using the vertical motion generated in the actuators. The placement of the actuators requires a close interaction between the mechanical design and the high-frequency design aspects of the RF transmission line. By placing the actuators in the gaps between the RF conductor and ground planes in a coplanar waveguide (CPW) transmission line, the high dielectric constant PZT combined with the air cavity beneath the released actuator (created with a XeF_2 etch) can be compensated with minor changes in the CPW dimensions (i.e., width of the RF transmission line and RF-GND gap) so as to maintain a 50 Ω impedance in the switch (see Table 5.13 and Fig. 5.68). The two actuators residing in the RF gaps can be connected mechanically with a coupling beam containing a short section of conductor used to complete the RF circuit. Two very short cantilevered structures anchored to each section of RF conductor overhang the conductor on the mechanical coupling beam and allow the switch structure to close the series configured gap upon actuation. Another design feature is air bridges that span the RF conductor to electrically connect each of the actuators. The actuator bias lines allow the actuation voltage to be applied independently of the RF conductor. The bias air bridges spanning the RF conductor require the width of the conductor to be modified to maintain 50 Ω impedance because of the capacitive loading on the RF conductor. Thus, the RF conductor is narrowed underneath the bias air bridges and widened in the regions where the PZT actuators are located (see Fig. 5.68). It can be compensated with minor changes in the CPW gaps so as to maintain a 50 Ω impedance.

Table 5.13 Dimensional information for a PZT switch design using a CPW transmission line

Feature	Width (μm)	Length (μm)
RF conductor (outside of actuators)	75	>150
RF conductor (under air bridges)	50	10
RF gap (between actuators)	40	
RF gap (outside of actuator regions)	50	
Ground plane	440	660
PZT actuator	40	100, 125, 150
RF cantilever (in)	100	37.5
RF cantilever (out)	75	37.5
RF contact pad (in)	120	
RF contact pad (out)	77	
Bias air bridges	170	10
Ground straps	18	80

The fabrication of the PZT switch begins with the choice of an appropriate substrate for high-frequency performance and reasonable piezoelectric properties in the PZT thin film. The preferred substrate is silicon because of the wealth of knowledge regarding fabrication processes as well as previous history with processing PZT thin films on platinized silicon substrates. However, as illustrated in Fig. 5.69, a standard resistivity (1–30 Ω cm) silicon substrate has extremely poor transmission line loss at microwave frequencies. Traditional microwave substrates, alumina and sapphire [202], have transmission line losses less than 0.04 dB/wavelength (see Fig. 5.69).

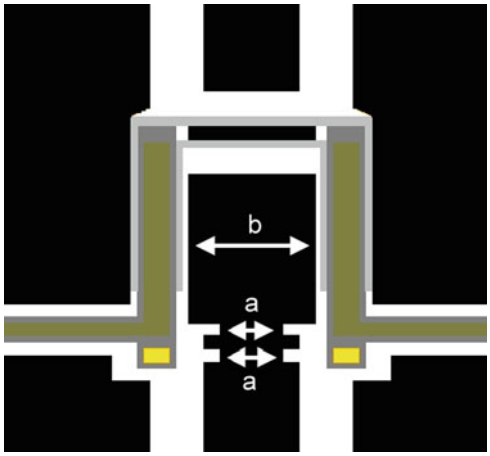


Fig. 5.68 Illustration of the RF conductor width modifications to account for (**a**) capacitive loading from the DC bias air bridges and (**b**) the changes to the capacitance within the RF gap from the air cavity underneath the actuators and CPW transmission line

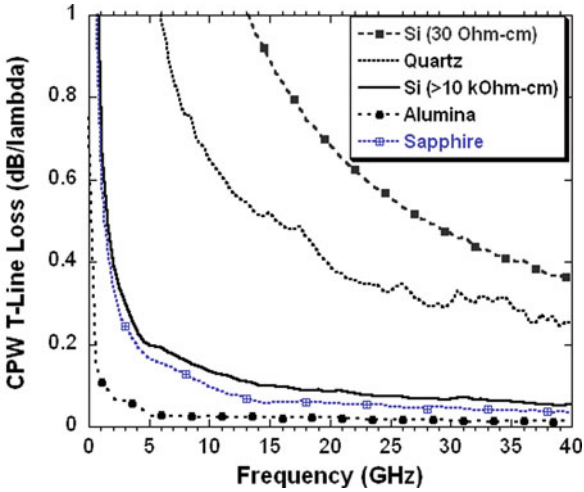


Fig. 5.69 Coplanar waveguide transmission line (T-line) loss as a function of frequency for various substrates. *Note*: The alumina is a polycrystalline substrate

Even though high-resistivity silicon is not commonly thought of as a microwave substrate, it performs quite well, with a transmission line loss of ~0.05 dB/wavelength at 40 GHz. The transmission line loss is reported as dB/wavelength and not dB/mm because the primary aim of MEMS switches is in distributed RF circuits. As a consequence, the interest is in designing the smallest low-loss circuits such as phase shifters and tunable antenna receivers. As the microwave wavelength depends on the dielectric constant of the substrate, other substrates such as quartz and fused silica usable for transmitting energy point-to-point, where dB/mm is important, require much larger circuits to maintain a particular wavelength. The result is that the line loss per wavelength increases. For the following discussion, high resistivity (>10 kΩ cm) Czochralski-grown (100) silicon substrates are selected for fabrication of a PZT switch.

Table 5.14 Plasma-enhanced chemical vapor deposition parameters for silicon dioxide and silicon nitride thin films deposited using a plasma-Therm 790

Material	SiH_4 in 5% He (sccm)	He (sccm)	N_20 (sccm)	N_2 (sccm)	NH_3 (sccm)	Pressure (mT)	Temp (ºC)	Power (W)
SiO_2	70	93	390	0	0	900	250	25
Si_3N_4	90	488	0	160	3.00	900	250	45

The next step in the actuator fabrication is deposition of the stress engineered elastic layer comprised of $SiO_2/Si_3N_4/SiO_2$. The previous discussions regarding this elastic layer combination are based on PECVD-deposited films deposited at 250°C using the deposition parameters in Table 5.14. One concern with PECVD films used in conjunction with higher temperature processing is the release of trapped hydrogen within the films, especially when using silane (SiH_4) as a precursor gas. With the CSD PZT having a thermal budget of 700°C, any trapped hydrogen within the film must be released prior to deposition of the metal and PZT layers. Following PECVD deposition, the elastic layer is annealed at 700°C in flowing N_2 (~5 sccm) for 60 s to eliminate loosely attached hydrogen ions [207–209]. The hydrogen release also results in a restructuring of the atomic bonds within the film, altering the residual stress within the PECVD films leading the values reported in Table 5.12.

Following the elastic layer, the base metal layer of $Ti/TiO_x/Pt$ is deposited, preferably using sputter deposition to achieve a high degree of (111) texture in the Pt. The details of the deposition process for achieving a highly textured Pt layer can be best described in [158]. The process begins with the deposition of Ti followed by an oxidation anneal to convert the titanium into titanium dioxide configured in the rutile crystal structure. The 820 Å Pt layer is then sputter-deposited at 500°C. With the processing temperature for the PZT being 700°C, the residual stress within the Pt should be characterized following an anneal at 700°C. The anneal results in a stress relaxation of the metal thin films, with an increase in the tensile stress of the metal layer (see Fig. 5.56). However, for device fabrication, the anneal is eliminated to ensure optimal growth of the PZT thin film without the introduction of Pt hillocks.

The planar depositions of the actuator materials are completed with the deposition of the active piezoelectric layer, PZT (52/48), followed by a sputter deposition of Pt. For the devices demonstrated in [29], a 0.5 μm thick PZT layer was deposited via sol-gel using a 2-methoxyethanol solvent-based solution. Sputtered PZT (52/48) has also successfully been used to create the same switch actuators. After the PZT, a 0.1 μm thick Pt layer is sputter-deposited at 300°C.

The next steps in the switch fabrication include actuator patterning, patterning the RF transmission lines, creation of air bridge structures, and device release and are schematically represented in Fig. 5.70. The actuator patterning begins by defining the area of the top Pt electrode regions using Ar ion-milling. Next, the PZT and bottom bilayer of Ti/Pt or TiOx/Pt are patterned with ion-milling stopping on the

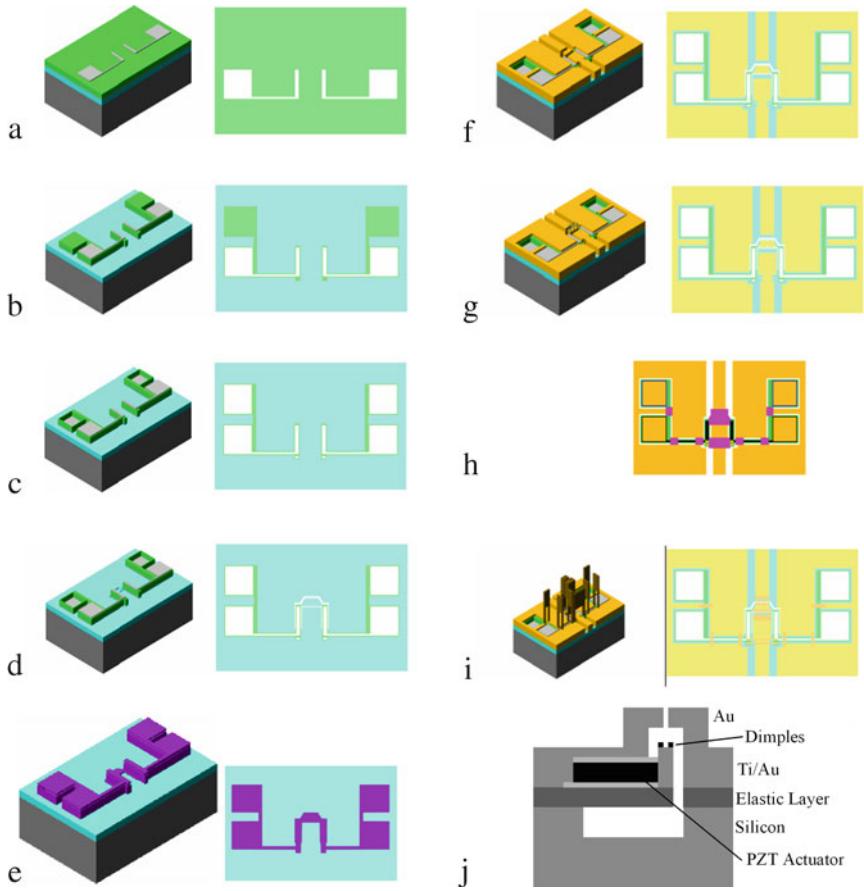


Fig. 5.70 Fabrication process flow schematic for creating a PZT actuated RF MEMS switch: (**a**) pattern top Pt, (**b**) pattern PZT and bottom Pt, (**c**) open via to bottom Pt, (**d**) open etch release trench, (**e**) thin elastic layer (pink layer is resist), (**f**) pattern CPW transmission line, (**g**) deposit contact dimple metal, (**h**) pattern sacrificial resist layer, (**i**) air bridge deposition, patterning, and O_2 release of sacrificial resist, (**j**) XeF_2 etch release of actuator [57] (Reprinted with permission. Copyright 2007 IEEE)

elastic layer with a small amount of overetch into the top of the elastic layer permitted. The opening via to contact the bottom Pt electrode is completed with either a combination of ion-milling and wet etching or simply a wet etch using a combination of H_2O:HCl:HF (2:1:0.04). The final step required for patterning the actuator is the opening of the etch trench in the elastic layer surrounding the actuator. This etch utilizes a combination of CF_4, CHF_3, and He to remove the elastic layer and provide a shallow overetch into the silicon substrate.

Prior to deposition of the RF transmission lines, the remaining elastic layer is thinned using a combination of CF_4, CHF_3, and He to remove the top layer of

silicon dioxide, silicon nitride, and 50 nm of the bottom silicon dioxide layer. As described in [29], this etch is crucial for reducing the parasitic and achieving low loss transmission lines. The transmission lines are patterned using a metal liftoff technique with evaporated Ti/Au (20/730 nm). In addition, a separate layer of Au/Pt (400/100 nm) or Au/Ru (400/100 nm) is deposited to serve as contact dimples for the switch.

The air bridge structures are created using a combination of a sacrificial photoresist layer using a mild high-temperature bake to round the corners of the resist followed by metal liftoff of an electron-beam-evaporated 2 μm Au layer. The resist is then removed using an oxygen plasma to then create the free-standing air bridge structures for the switch. Prior to the final release of the actuators, a short plasma etch using a combination of CF_4, CHF_3, and He is used to remove any oxidation on the exposed silicon surfaces. The final device (see Fig. 5.71) etch is completed using a timed XeF_2 designed to provide an approximate lateral undercut of 35 μm.

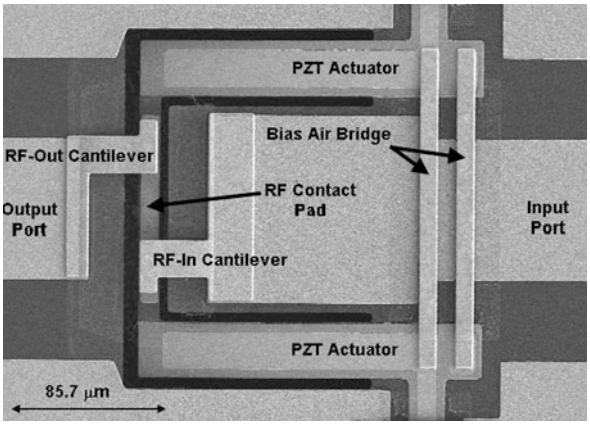


Fig. 5.71 SEM image of a PZT-actuated RF MEMS switch [57] (Reprinted with permission. Copyright 2007 IEEE)

5.4 Summary

This chapter has introduced the fundamentals of piezoelectric and ferroelectric materials, provided simple models for the response of thin film piezoelectric devices, and presented an overview of applications for these devices. The material deposition and patterning techniques for the polar piezoelectric materials, AlN and ZnO; and the ferroelectric material PZT have been reviewed. Device design considerations related to processing have also been addressed for these materials. Examples and discussions of demonstrated devices and their fabrication processes have been presented for both polar and ferroelectric materials.

The motivation to overcome the processing challenges with these materials continues to gain momentum as piezoelectric MEMS devices continue to demonstrate unique capabilities and in many cases superior device performance. Many of the

early issues with process compatibility, complexity, and film quality have been resolved. Although many technical challenges still remain, piezoelectricity is slowly becoming better utilized in the MEMS community.

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References

1. R. Ruby, P. Merchant: Micromachined Thin Film Bulk Acoustic Resonators, Proceedings of the IEEE Freq. Control, Piscataway, NJ, pp. 135–138 (1994)
2. P. Muralt, R.G. Polcawich, S. Trolier-McKinstry: Piezoelectric thin films for sensors, actuators, and energy harvesting, MRS Bull. 34, 658–664 (2009)
3. S. Tadigadapa, K. Mateti: Piezoelectric MEMS sensors: State-of-the-art and perspectives, Meas. Sci. Technol. 20, 092001 (2009)
4. J.F. Nye: Physical Properties of Crystals (Oxford University Press, New York, NY, 1990)
5. Ballato: Basic material quartz and related innovations, In Piezoelectricity: Evolution and Future of a Technology (Springer, Berlin, 2008)
6. N. Setter: ABC of Piezoelectricity and Piezoelectric Materials, In Piezoelectric Materials in Devices, pp. 1–28 (Ceramics Laboratory EPFL, Lausanne, Switzerland, 2002)
7. P. Muralt: Piezoelectric thin films for MEMS, Integr. Ferroelectr. 17, 297–307 (1997)
8. P. Muralt, A. Kholkin, M. Kohli, T. Maeder: Piezoelectric actuation of PZT thin film diaphragms at static and resonant conditions, Sens. Actuators A, 53, 397–403 (1996)
9. M. Dubois, P. Muralt: Measurement of the effective transverse piezoelectric coefficient e31,f of AlN and $Pb(Zr_xTi_{1-x}O_3)$ thin films, Sen. Actuators 77, 106–112 (1999)
10. IEEE Standard on Piezoelectricity, ANSI/IEEE Std 176 (1987)
11. W.L. Warren, J. Robertson, D. Dimos, B.A. Tuttle, G.E. Pike, D.A. Payne: Pb displacements in Pb(Zr,Ti)O3 perovskites, Phys. Rev. B 53, 3080–3087 (1996)
12. J. Moulson, J.M. Herbert, Electroceramics (Chapman and Hill, New York, NY, 1990)
13. Jaffe, W.R. Cook, H. Jaffe: Piezoelectric Ceramics (R.A.N., Marietta, OH, 1971)
14. B. Noheda, J.A. Gonzalo, L.E. Cross, R. Guo, S.E. Park, D.E. Cox, G. Shi-rane: Tetragonal-to-monoclinic phase transition in a ferroelectric perovskite: The structure of PbZr0.52Ti0.48O3, Phys Rev. B 61, 8687–8690 (2000)
15. X.-H. Du, U. Belegundu, K. Uchino: Crystal orientation dependence of piezoelectric properties of lead zirconate titanate near the morphotropic phase boundary, Appl. Phys. Lett. 72, 2421–2423 (1998)
16. K.R. Oldham, J.S. Pulskamp, R.G. Polcawich, M. Dubey: Thin-film PZT lateral actuators with extended stroke, J. MEMS 17, 890–899 (2008)
17. J.G. Smits, W. Choi: The constituent equations of piezoelectric heterogeneous bimorphs, IEEE Trans. Ultrasonics, Ferro, Freq. Control 38, 256–270 (1991)
18. H.F. Tiersten: Linear Piezoelectric Plate Vibration (Plenum Press, New York, NY, 1969)
19. W.P. Mason: Piezoelectric Crystals and Their Applications to Ultrasonics (Van Nostrand, New York, NY, 1950)
20. Ballato, J.G. Smits: Network representation for piezoelectric bimorphs, IEEE Trans. Ultrasonics, Ferro. Freq. Control 38, 595–602 (1991)
21. J.G. Smits, W. Choi, A. Ballato: Resonance and antiresonance of symmetric asymmetric cantilevered piezoelectric flexors, IEEE Trans. Ultrasonics, Ferro. Freq. Control 44, 250–258 (1997)

22. W.G. Cady: Piezoelectricity; An Introduction to the Theory and Applications of Electromechanical Phenomena in Crystals (McGraw-Hill, New York, NY, 1946)
23. D.L. DeVoe: Piezoelectric thin film micromechanical beam resonators, Sens. Actuators A 88, 263–272 (2001)
24. D.L. DeVoe, A.P. Pisano: Modeling and Optimal Design of Piezoelectric cantilever Microactuators, J. MEMS 6, 266–270 (1997)
25. M.S. Weinberg: Working equations for piezoelectric actuators and sensors, J. MEMS 8, 529–533 (1999)
26. E. Elka, D. Elata, H. Abramovich: The electromechanical response of multilayered piezoelectric structures, J. MEMS 13, 332–341 (2004)
27. J. Gere, S. Timoshenko: Mechanics of Materials, pp. 400–403 (PWS Publishing, Boston, MA, 1997)
28. J. Judy: Magnetic microactuation of polysilicon flexure structures, J. MEMS 4, 162–169 (1995)
29. R.G. Polcawich, J.S. Pulskamp, D. Judy, P. Ranade, S. Trolier-McKinstry, M. Dubey: Surface micromachined microelectromechanical ohmic series switch using thin-film piezoelectric actuators, IEEE Trans. Microwave Theory Tech 55, 2642–2654 (2007)
30. C. Fox, X. Chen, H.W. Jiang, P.B. Kirby, S. McWilliam: Development of micromachined RF switches with piezofilm actuation, Smart Structures Materials 2002, Smart Electronics, MEMS, and Nanotechnology, Vol. 4700, pp. 40–49 (San Diego, CA, 2002)
31. S. Butterworth: On electrically maintained vibrations, Proc. Phys. Soc. 27, 410–424 (1915)
32. W.G. Cady: The piezoelectric resonator, Proc. IRE 10, 83–114 (1922)
33. G. Martin: Determination of equivalent circuit constants of piezoelectric resonators of moderately low Q by absolute admittance measurements, J. Acoust. Soc. Am. 26, 413–420 (1924)
34. W.P. Mason: Electromechanical Transducers and Wave Filters, p. 399 (Van Nostrand, New York, NY, 1948)
35. Arnau: Piezoelectric Transducers and Applications (Springer, New York, NY, 2004)
36. F.D. Bannon, J.R. Clark, C.-C. Nguyen: High-Q HF microelectromechanical filters, IEEE J. Solid State Circuits 35, 512–526 (2000)
37. D. Damjanovic: Ferroelectric, dielectric and piezoelectric properties of ferroelectric thin films and ceramics, Rep. Prog. Phys. 61, 1267–1324 (1998)
38. D.A. Hall: Review: Nonlinearity in piezoelectric ceramics, J. Mater. Sci. 36, 4575–4601 (2001)
39. Q.M. Wang, Q. Zhang, B. Xu, R. Liu, L.E. Cross: Nonlinear piezoelectric behavior of ceramic bending mode actuators under strong electric fields, J. Appl. Phys. 86, 3352–3360 (1999)
40. K. Tagantsev, V.O. Sherman, K.F. Astafiev, J. Venkatesh, N. Setter: Ferroelectric materials for microwave tunable applications, J. Electroceram. 10, 1–62 (2003)
41. N. Setter et al.: Ferroelectric thin films: Review of materials, properties, and applications, J. Appl. Phys. 100, 051606 (2006)
42. G. Robert, D. Damjanovic, N. Setter: Preisach modeling of piezoelectric nonlinearity in ferroelectric ceramics, J. Appl. Phys. 89, 5067–5074 (2001)
43. K. Uchino, J. Giniewicz: Micromechatronics, pp. 242–254 (Marcel Dekker, New York, NY, 2003)
44. R. Holland: Representation of dielectric, elastic, and piezoelectric losses by complex coefficients, IEEE Trans. Sonics Ultrasonics Ultrason. SU-14, 18–20 (1967)
45. P. Muralt: PZT thin films for microsensors and actuators: Where do we stand? IEEE Trans. Ultrason. Ferro. Freq. Control 47, 903–914 (2000)
46. T.P. Alexander, T.J. Bukowski, D.R. Uhlmann, G. Teowee, K.C. McCarthy, J. Dawley, B.J.J. Zelinski: Dielectric Properties of Sol-Gel Derived ZnO Thin Films, Proceedings of the 10th IEEE International Symposium on Applications of Ferroelectrics (ISAF), East Brunswick, NJ, Vol. 2, pp. 585–588 (1996)

47. Y. Xu: Ferroelectric Materials and their Applications, pp. 61–63, 226–229 (North-Holland, Amsterdam, 1991)
48. S.V. Krishnaswamy et al.: Compact FBAR filters offer low-loss performance, Microw. RF 30, 127–136 (1991)
49. T-H. Fang, W.-J. Chang, C.-M. Lin: Nanoindentation characterization of ZnO thin films, Mater. Sci. Eng. A 452–453, 715–720 (2007)
50. P.-F. Yang, H.-C. Wen, S.-R. Jian, Y.-S. Lai, S. Wu, R.-S. Chen: Characteristics of ZnO thin films prepared by radio frequency magnetron sputtering, Microelectron. Reliab. 48, 389–394 (2008)
51. K. Tonisch et al.: Piezoelectric properties of polycrystalline AlN thin films for MEMS application, Sens. Actuators A 132, 658–663 (2006)
52. Andrei, K. Krupa, M. Jozwik, P. Delobelle, L. Hirsinger, C. Gorecki, L. Nieradko, C. Meunier: AlN as an actuation material for MEMS applications: The case of AlN driven multilayered cantilevers, Sens. Actuators A 141, 565–576 (2008)
53. K.E. Wojciechowski, R.H. Olsson III, C.D. Nordquist, M.R. Tuck: Super High Frequency Width Extensional Aluminum Nitride (AlN) MEMS Resonators, IEEE International Ultrasonics Symposium, Rome, Italy, pp. 1179–1182 (2009)
54. H. Chandrahalim, S. Bhave, R. Polcawich, J. Pulskamp, D. Judy: Influence of Silicon on Quality Factor, Motional Impedance and Tuning Range of PZT-Transduced Resonators, Solid State Sensor, Actuator and Microsystems Workshop, Hilton Head, SC, pp. 360–363 (2008)
55. J.S. Pulskamp, D.C. Judy, R.G. Polcawich, R. Kaul, H. Chandrahalim, S.A. Bhave: Monolithically Integrated PiezoMEMS SP2T Switch and Contour-Mode Filters, Proceedings of the 22nd IEEE MEMS Conference, Sorento, Italy, pp. 900–903 (2009)
56. H.C. Lee, J.H. Park, J.Y. Park, H.J. Nam, J.U. Bu: Design, fabrication, and RF performance of two different types of piezoelectrically actuated ohmic MEMS switches, J. Micromech. Microeng. 15, 2098–2104 (2005)
57. R.G. Polcawich, D. Judy, J.S. Pulskamp, S. Trolier-McKinstry, M. Dubey: Advances in Piezoelectrically Actuated RF MEMS Switches and Phase Shifters, Proceedings of IEEE International Microwave Symposium, Honolulu, HI, pp. 2083–2086 (2007)
58. D. Chung, R. Polcawich, D. Judy, J. Pulskamp, J. Papapolymerou: A SP2T and a SP4T Switch using Low Loss Piezoelectric MEMS, Proceedings of IEEE International Microwave Symposium, Atlanta, GA, pp. 100–104 (2008)
59. R. Polcawich, M. Scanlon, J. Pulskamp et. al.: Design and fabrication of a lead zirconate titanate (PZT) thin film acoustic sensor, Integr. Ferroelectr. 54, 595–606 (2003)
60. S.C. Ko, Y.C. Kim, S.S. Lee, S.H. Choi, S.R. Kim: Micromachined piezoelectric membrane acoustic device, Sens. Actuators 103, 130–134 (2003)
61. D.L. DeVoe, A.P. Pisano: Surface micromachined piezoelectric accelerometers (PiXLs), J. MEMS 10, 180–186 (2001)
62. L.P. Wang, R.A. Wolf, Y. Wang, K.K. Deng, L.C. Zou, R.J. Davis, S. Trolier-McKinstry: Design, fabrication, and measurement of high sensitivity piezoelectric microelectromechanical systems accelerometers, J. MEMS 12, 433–439 (2003)
63. S.P. Beeby, J.N. Ross, N.M. White: Design and fabrication of a micromachined silicon accelerometer with thick-film printed PZT sensors, J. Micromech. Microeng. 10, 322–328 (2000)
64. S Aoyagi et al.: Surface micromachined accelerometer using ferroelectric substrate, Sens. Actuators A 139, 88–94 (2007)
65. C.C. Hindrichsen, E.V. Thomsen, R. Lou-Moller, T. Bove: MEMS Accelerometer with Screen Printed Piezoelectric Thick Film, Proceedings of the IEEE Sensors Conference, Daegu, Korea, pp. 1477–1480 (2006)
66. G. Percin et al.: Micromachined two-dimensional array piezoelectrically actuated transducers, Appl. Phys. Lett. 72, 1397–1399 (1998)
67. B. Belgacem, F. Calame, P. Muralt: Piezoelectric micromachined ultrasonic transducers with thick PZT sol gel films, J. Electroceram. 19, 369–373 (2007)

68. Q. Wang et al.: Application of Aluminum Nitride Thin Film for Micromachined Ultrasonic Transducers, Materials Research Society Symposium Proceedings, Boston, MA, pp. 0892-FF13-01.1 (2006)
69. P. Muralt, N. Ledermann, J. Baborowski, A. Barzegar, S. Gentil, B. Belgacem, S. Petitgrand, A. Bosseboeuf, N. Setter: Piezoelectric Micromachined Ultrasonic Transducers Based on PZT Thin Films, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 52, 2276–2288 (2005)
70. R. Duggirala, R.G. Polcawich, M. Dubey, A. Lal: Radioisotope thin-film fueled microfabricated reciprocating electromechanical power generator, J. MEMS 17, 837–849 (2008)
71. R.V. Schaijk, R. Elfrink, T.M. Kamel, M. Goedbloed, Piezoelectric AlN Energy Harvester for Wireless Autonomous Transducer Solutions, IEEE Sensors, Lecce, Italy, pp. 45–48 (2008)
72. Y.B. Jeon, R. Sood, J.H. Jeong, S.G. Kim: MEMS power generator with transverse mode thin film PZT, Sens. Actuators A 122, 16–22 (2005)
73. F. Lu, H.P. Lee, S.P. Lim: Modeling and analysis of micro piezoelectric power generators for microelectromechanical systems applications, Smart Mater. Struct. 13, 57–63 (2004)
74. Y.S. Kim, H.J. Nam, S.M. Cho, J.W. Hong, D.C. Kim, J.U. Bu: PZT cantilever array integrated with piezoresistor for high speed parallel operation of AFM, Sens. Actuators A 103, 122–129 (2003)
75. J. Tsaur, L. Zhang, R. Maeda, S. Matsumoto: 2D Micro Scanner Actuated by Sol–Gel Derived Double Layered PZT, Proceedings of the IEEE Conference on MEMS 2002, Las Vegas, NV, pp. 548–551 (2002)
76. F. Filhol, E. Defay, C. Divoux, C. Zinck, M.-T. Delaye: Resonant micromirror excited by a thin-film piezoelectric actuator for fast optical beam scanning, Sens. Actuators A 123/124, 483–489 (2005)
77. E. Fujii, R. Takayama, K. Nomura, A. Murata, T. Hirasawa, A. Tomozawa, S. Fujii, T. Kamada, H. Torii: Preparation of (001)-oriented $Pb(Zr,Ti)O_3$ thin films and their piezoelectric applications, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 54, 2431 (2007)
78. P. Muralt et al.: Fabrication and characterization of PZT thin-film vibrators for micromotors, Sens. Actuators A 48, 157–165 (1995)
79. M.-A. Dubois, P. Muralt: PZT thin film actuated elastic fin micromotor, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 45, 1169–2277 (1998)
80. D. Judy, R.G. Polcawich, J. Pulskamp: Low Voltage Complementary MEMS Logic Using Piezoelectric Actuators, Solid State Sensor, Actuator and Microsystems Workshop, Hilton Head, SC, pp. 328–331 (2008)
81. D.C. Judy, J.S. Pulskamp, R.G. Polcawich, L. Currano: Piezoelectric Nanoswitch, Proceedings of the 22nd IEEE MEMS Conference, Sorento, Italy, pp. 591–594 (2009)
82. J.S. Pulskamp, R.G. Polcawich, K. Oldham: Highly Integrated Piezo-MEMS Enabled Millimeter-Scale Robotics, Proceedings of ASME IDETC/MNS, San Diego, CA (2009)
83. K. Oldham, J. Pulskamp, R. Polcawich: Thin-film piezoelectric actuators for bio-inspired micro-robotic applications, Integr. Ferroelectr. 95, 54–65 (2007)
84. J.R. Bronson, J.S. Pulskamp, R.G. Polcawich, C.M. Kroninger, E.D. Wetzel: PZT MEMS Actuated Flapping Wings for Insect-Inspired Robotics, Proceedings of the 22nd IEEE MEMS Conference, Sorento, Italy, pp. 1047–1050 (2009)
85. P. Chen et al.: Growth of high quality GaN layers with AlN buffer on Si(111) substrates, J. Cryst. Growth 225, 150–154 (2001)
86. Y. Deng et al.: Study on strain and piezoelectric polarization of AlN thin films grown on Si, J. Vac. Sci. Technol. A 23, 628–630 (2006)
87. Z. Chen, S. Newman, D. Brown et al.: High quality AlN grown on SiC by metal organic chemical vapor deposition, Appl. Phys. Lett. 93, 191906–4 (2008)
88. Dadgar et al.: A two-step metal organic vapor phase epitaxy growth method for high-quality ZnO on GaN/Al2O3 (0001), J. Cryst. Growth 267, 140–144 (2004)
89. M. Pan et al.: Metal-organic chemical vapor deposition of ZnO, J. Cryst. Growth 287, 688–693 (2006)

90. F. Martin, P. Muralt, M.A. Dubois, A. Pezous: Thickness dependence of the properties of highly c-axis textured AlN thin films, J. Vac. Sci. Technol. A 22, 361–365 (2004)
91. E. Iborra, J. Olivares, M. Clement, L. Vergara, A. Sanz-Hervás, J. San-grador: Piezoelectric properties and residual stress of sputtered AlN thin films for MEMS applications, Sens. Actuators A 115, 501–507 (2004)
92. Rodriguez-Navarro, W. Otano-Rivera, J.M. Garcia–Ruiz, R. Messier: Development of preferred orientation in polycrystalline AlN thin films deposited by RF sputtering system at low temperature, J. Mater. Res. 12, 1850–1855 (1997)
93. J.A. Ruffner et al.: Effect of substrate composition on the piezoelectric response of reactively sputtered AlN thin films, Thin Solid Films 354, 256–261 (1999)
94. M. Akiyama et al.: Influence of metal electrodes on crystal orientation of aluminum nitride thin films, Vacuum 74, 699–703 (2004)
95. M.-A. Dubois, P. Muralt, L. Sagalowicz: Aluminum nitride thin films for high frequency applications, Ferroelectrics 224, 671–678 (1999)
96. S.H. Lee, J.K. Lee, K.H. Yoon: Growth of highly c-axis textured AlN films on Mo electrodes for film bulk acoustic wave resonators, J. Vac. Sci. Technol. A 21, 1–5 (2003)
97. R. Lanz, P. Muralt: Bandpass filters for 8 GHz using solidly mounted bulk acoustic wave resonators, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 52, 936–946 (2005)
98. F. Martin, P. Muralt, M.-A. Dubois: Process optimization for the sputter deposition of molybdenum thin films as electrode for AlN thin films, J. Vac. Sci. Technol. A 24, 946–952 (2006)
99. H.-C. Lee, J.-Y. Park, K.-H. Lee, J.-U. Bu: Preparation of highly textured Mo and AlN films using a Ti seed layer for integrated high-Q film bulk acoustic resonators, J. Vac. Sci. Technol. B 22, 1127–1133 (2004)
100. T. Kamohara, M. Akiyama, N. Ueno, N. Kuwano: Improvement in crystal orientation of AlN thin films prepared on Mo electrodes using AlN interlayers, Ceram. Int. 34, 985–989 (2008)
101. F. Medjani, R. Sanjinés, G. Allidi, A. Karimi: Effect of substrate temperature and bias voltage on the crystallite orientation in RF magnetron sputtered AlN thin films, Thin Solid Films 515, 260–265 (2006)
102. B. Abdallah et al.: Deposition of AlN films by reactive sputtering: Effect of radio frequency substrate bias, Thin Solid Films 515, 7105–7108 (2007)
103. A.K. Chu, C.H. Chao, F.Z. Lee, H.L. Huang: Influences of bias voltage on the crystallographic orientation of AlN thin films prepared by long-distance magnetron sputtering, Thin Solid Films 429, 1–4 (2003)
104. M.A. Dubois, P. Muralt: Stress and piezoelectric properties of aluminum nitride thin films deposited onto metal electrodes by pulsed direct current reactive sputtering, J. Appl. Phys. 89, 6389–6395 (2001)
105. C. Lin, Y. Chen, K.-S. Kao: Two-step sputtered ZnO piezoelectric films for film bulk acoustic resonators, Appl. Phys. A 89, 475–479 (2007)
106. S.J. Chang, Y.K. Su, Y.P. Shei: High quality ZnO thin films on InP substrates prepared by radio frequency magnetron sputtering. I. Material study, J. Vac. Sci. Technol. A 13, 381–384 (1995)
107. M.J. Vellekoop, C.C.O. Visser, P.M. Sarro et al.: Compatibility of zinc oxide with silicon IC processing, Sens. Actuators A 23, 1027–1030 (1990)
108. C.B. Varlul et al.: Wet chemical etching of AlN and InAlN in KOH solutions, J. Electrochem. Soc. 143, 3681–3684 (1996)
109. D. Zhuang, J.H. Edgar: Wet etching of GaN, AlN, and SiC: A review, Mater. Sci. Eng. 48, 1–46 (2005)
110. D. Chen, J. Wang, D. Xu, Y. Zhang: The influence of the AlN film texture on the wet chemical etching, J. Microelectron. 40, 15–19 (2009)
111. S. Saravanan, E. Berenschot, G. Krijnen, M. Elwenspoek: A novel surface micromachining process to fabricate AlN unimorph suspensions and its application for RF resonators, Sens. Actuators A 130–131, 340–345 (2006)

112. T.Y. Sheng, Z.Q. Yu, G.J. Collins: Disk hydrogen plasma assisted chemical vapor deposition of aluminum nitride, Appl. Phys. Lett. 52, 576–578 (1988)
113. S.M. Tanner, V.V. Felmetsger: Microstructure and chemical wet etching characteristics of AlN films deposited by ac reactive magnetron sputtering, J. Vac. Sci. Technol. A 28, 69–76 (2010)
114. K. Kobayashi et al.: Low wet etching rates of ZnO films prepared by sputtering of mixed ZnO and AlN powder targets, Thin Solid Films 516, 4894–4898 (2008)
115. Y. Li, S.G. Tompa, S. Liang, C. Gorla, Y. Lu, J. Doyle: Transparent and Conductive Ga-Doped ZnO Films Grown by Low Pressure Metal Organic Chemical Vapor Deposition, Proceedings of the 43rd National Symposium of the American Vacuum Society, Vol. 15, pp. 1063–1068 (Philadelphia, PA, 1997)
116. D. Devoe: Piezoelectric thin film micromechanical beam resonators, Sens. Actuators A 88, 263–272 (2001)
117. S S.J. Pearton, C C.R. Abernathy et al.: Dry etching of thin-film InN, AIN and GaN, Semicond. Sci. Technol. 8, 310–312 (1993)
118. R.J. Shul, G.A. Vawter et al.: Comparison of plasma etch techniques for III-V nitrides, Solid-State Electronics Electron. 42, 2259–2267 (1998)
119. S.A. Smith et al.: High rate and selective etching of GaN, AlGaN, and AlN using an inductively coupled plasma, Appl. Phys. Lett. 71, 3631–3633 (1997)
120. H. Cho, C.B. Vartuli et al.: Comparison of inductively coupled plasma Cl2 and Cl4/H2 etching of III-nitrides, J. Vac. Sci. Technol. A 16, 1631–1635 (1998)
121. G.-K. Lee, J.-H. Moon, B.-T. Lee: Inductively coupled plasma reactive ion etching of ZnO using C2F6 and NF3-based gas mixtures, Semicond. Sci. Technol. 21, 971–974 (2006)
122. W. Lim et al.: Comparison of ZnO dry etching in high density inductively coupled CH4/H2 and C2H6/H2-based chemistries, ECS Trans. 2, 209–216 (2006)
123. V.V. Felmetsger, P.N. Laptev, S.M. Tanner: Innovative technique for tailoring intrinsic stress in reactively sputtered piezoelectric aluminum nitride films, J. Vac. Sci. Technol. A 27, 417–422 (2009)
124. R. Aigner: MEMS in RF-filter applications: thin film bulk-acoustic-wave technology, Sensors Update 12, 175–210 (2003)
125. S.R. Gilbert, R. Parker, M.K. Small, U.B. Koelle, J.D. Larson, R.C. Ruby: An Ultra-miniature, Low Cost Single Ended to Differential Filter for ISM Band Applications, Microwave Symposium Digest, 2008 IEEE MTT-S International, Atlanta, GA, pp. 839–842 (2008)
126. R. Ruby, P. Bradley, D. Clark, D. Feld, T. Jamneala, K. Wang: Acoustic FBAR for Filters, Duplexers and Front End Modules, Microwave Symposium Digest, IEEE MTT-S, Fort Worth, TX, pp. 931–934 (2004)
127. R. Ruby, A. Barfknecht, C. Han, Y. Desai, F. Geefay, G. Gan, M. Gat, T. Verhoeven: High-Q FBAR Filters in a Wafer-Level Chip-Scale Package, IEEE International Solid-State Circuits Conference, San Francisco, CA, pp. 184–187 (2002)
128. G. Piazza, P.J. Stephanou, A.P. Pisano: Single-chip multiple-frequency aln MEMS filters based on contour-mode piezoelectric resonators, J. MEMS 16, 319–328 (2007)
129. Gavin G.K. Ho et al.: Piezoelectric-on-silicon lateral bulk acoustic wave micromechanical resonators, J. MEMS 17, 512–520 (2008)
130. G. Piazza: Contour-Mode Aluminum Nitride Vibrating RF Microsystems, Proceedings of the IEEE Frequency Control, Geneva, Switzerland, pp. 1352–1355 (2007)
131. G. Piazza, P.J. Stephanou, A.P. Pisano: Piezoelectric aluminum nitride vibrating contour-mode MEMS resonators, J. MEMS 15, 1406–1418 (2006)
132. R.H. Olsson III et al.: Post-CMOS Compatible Aluminum Nitride MEMS Filters and Resonant Sensors, IEEE International Frequency Control Symposium, 2007 Joint with the 21st European Frequency and Time Forum, Geneva, Switzerland, pp. 412–419 (2007)

133. R. Mahameed et al.: Dual-beam actuation of piezoelectric AlN RF MEMS switches monolithically integrated with AlN contour-mode resonators, J. Micromech. Microeng. 18, 105011 (2008)
134. N. Sinha et al.: Ultra Thin AlN Piezoelectric Nano-actuators, Proceedings of the Transducers 2009, Denver, CO, pp. 469–472 (2009)
135. G. Piazza, P.J. Stephanou, A.P. Pisano: AlN Contour-Mode Vibrating RF MEMS for Next Generation Wireless Communications, Proceedings of the 32nd European ESSDERC Solid-State Circuits Conference, Montreux, Switzerland, pp. 62–65 (2006)
136. R.N. Castellano, L.G. Feinstein: Ion-beam deposition of thin films of ferroelectric PZT, J. Appl. Phys. 50, 4406–4411 (1979)
137. S.B. Krupanidhi et al.: RF planar magnetron sputtering and characterization of ferroelectric PZT films, J. Appl. Phys. 54, 6601–6609 (1983)
138. M. Okuyama et al.: Preparation of PbTiO3 ferroelectric thin film by RF sputtering, Jpn. J. Appl. Phys. 18, 1633–1634 (1979)
139. J. Sreenivas, M. Sayer, P. Garrett: Properties of dc magnetron sputtered PZT thin films, Thin Solid Films 172, 251–267 (1989)
140. S. Hiboux, P. Muralt, N. Setter: Orientation and composition dependence of piezoelectric dielectric properties of sputtered $Pb(Zr_xTi_{1-x})O_3$ thin films, Mater. Res. Soc. Symp. Proc. 596, 499–504 (2000)
141. Kanno, H. Kotera, K. Wasa: Measurement of transverse piezoelectric properties of PZT thin films, Sens. Actuators A 107, 68–74 (2003)
142. M. Okada et al.: Preparation of c-axis oriented PbTiO3 thin films by MOCVD, Ferroelectrics 91, 181–192 (1989)
143. H. Kuwabara, N. Menou, H. Funakubo: 1 V saturated Pb(Zr,Ti)O3 films with (111) orientation using lattice-matched (111) SrRuO3 / (111) Pt bottom electrode prepared by pulsed metal organic chemical vapor deposition, Appl. Phys. Lett. 93, 152901-1–152901-3 (2008)
144. Y. Otani, S. Okamura, T. Shiosaki: Recent developments on MOCVD of ferroelectric thin films, J. Electroceram. 13, 15–22 (2004)
145. K.D. Budd, S.K. Dey, D.A. Payne: Sol-gel processing of PT, PZ, PZT, and PLZT thin films, Br. Ceram. Proc. 36, 107 (1985)
146. G.A.M.C. Spierings, M.I.E. Ulenaers, G.L.M. Kampschoer, H.A.M. van Hal, P.K. Larsen: Preparation and ferroelectric properties of PZT by spin coating and metal organic decomposition, J. Appl. Phys. 70, 2290–2298 (1991)
147. B.A. Tuttle et al.: Microstructural evolution of PZT thin films prepared by hybrid metallorganic decomposition, J. Mater. Res. 7, 1876–1882 (1992)
148. G.A.M.C. Spierings et al.: Preparation and ferroelectric properties of PZT by spin coating and metal organic decomposition, J. Appl. Phys. 70, 2290–2298 (1991)
149. B.A. Tuttleand, R.W. Schwartz: Solution deposition of PZT ferroelectric thin films prepared by hybrid metallorganic decomposition, MRS Bull. 7, 1876–1882(1996)
150. J. W. Schwartz: Chemical solution deposition of perovskite thin films, Chem. Mater. Sci. 209, 2325–2340(1997)
151. F. Calame, P. Muralt: Growth and properties of gradient free sol-gel lead zirconate titanate thin films, Appl. Phys. Lett. 90, 062907 (2007)
152. R.D. Klissurska et al.: Effect of Nb doping on the microstructure of sol-gel derived PZT thin films, J. Am. Ceram. Soc. 78, 1513–1520 (1995)
153. P. Muralt, J. Baborowski, N. Lederman: Piezoelectric Micro-electro-mechanical Systems with $PbZr_xTi_{1-x}O_3$ Thin Films: Integration and Application Issues, Piezoelectric Materials and Devices, pp. 231–260, EPFL Swiss Federal Institute of Technology, Switzerland (2002)
154. K.H. Hartl, H. Rau: PbO vapour pressure in the Pb(Zr,Ti)O3 system, Solid State Commun. 7, 41–45 (1969)
155. P. Muralt: Texture control and seeded nucleation of nanosize structures of ferroelectric thin films, J. Appl. Phys. 100, 051605 (2006)
156. S. Trolier-McKinstry, P. Muralt: Thin film piezoelectrics for MEMS, J. Electroceram. 12, 7–17 (2004)

157. D.M. Kim, C.B. Eom, V. Nagarajan, J. Ouyang, R. Ramesh, V. Vaithyanathan, D.G. Schlom: Thickness dependence of structural and piezoelectric properties of epitaxial $Pb(Zr_{0.52}Ti_{0.48})O_3$ films on Si and $SrTiO_3$ substrates, Appl. Phys. Lett. 88, 142904-1–142904-3 (2006)
158. G. Fox, K. Suu: High temperature deposition of Pt/TiOx for bottom electrodes, US Patent 6,682,772, January 27 (2004)
159. R.W. Whatmore, Q. Zhang, Z. Huang, R.A. Dorey: Ferroelectric thin and thick films for microsystems, Mater. Sci. Semi-Solid Proc. 5, 65–76 (2003)
160. R.W. Schwartz, R.A. Assink, T.J. Headley: Spectroscopic and Microstructural Characterization of Solution Chemistry Effects in PZT Thin Film Processing, Ferroelectric Thin Films II Material Research Society Symposium Proceedings, Vol. 243, Boston, MA, pp. 245–254 (1992)
161. R.A. Assink, R.W. Schwartz: 1H and 13C NMR investigations of Pb(Zr,Ti)03 thin-film precursor solutions, Chem. Mater. 5, 511–517 (1993)
162. Q.F. Zhou, E. Hong, R. Wolf, S. Trolier-McKinstry: Dielectric and piezoelectric properties of PZT 52/48 thick films with (100) and random crystallographic orientation, Ferroelectric Thin Films IX, Material Research Society Proceedings, Vol. 655, pp. CC11.7.1–CC11.7.6 (2001)
163. N. Ledermann, P. Muralt et al.: {100}-Textured, piezoelectric $Pb(Zr_x, Ti_{1-x})O_3$ thin films for MEMS: Integration, deposition and properties, Sens. Actuators A 105, 162–170 (2003)
164. G. Orcel, L. Hench: Effect of formamide additive on the chemistry of silica-gels. Part 1. NMR of silica hydrolysis, J. Non-Cryst. Solids 79, 177–194 (1986)
165. R.W. Schwartz, R.A. Assink, D. Dimos, M.B. Sinclair, T.J. Boyle, C.D. Buchheit: Effects of Acetylacetone Additions on PZT Thin Film Processing, Ferroelectric Thin Films IV, MRS Symposium, Boston, MA, pp. 377–387 (1995)
166. K. Tsuchiya, T. Kitagawa, Y. Uetsuji, E. Nakamachi: Fabrication of smart material PZT thin films by RF magnetron sputtering method in micro actuators, JSME Int. J. 49, 201–208 (2006)
167. S. Mancha: Chemical etching of thin film PLZT, Ferroelectrics 135, 131–137 (1992)
168. R. Miller, J. Bernstein: A novel wet etch for patterning PZT thin films, Integr. Ferroelectr. 29, 225–231 (2000)
169. K. Zheng, J. Lu, J. Chu: A novel wet etching process of Pb(Zr,Ti)O3 thin films for applications in microelectromechanical system, J. Appl. Phys. 43, 3934–3937 (2004)
170. D.P. Vijay, S.uB. Desu, W. Pan: Reactive ion etching of lead zirconate titanate (PZT) thin film capacitors, J. Electrochem. Soc. 140, 2635–2539 (1993)
171. W. Pan et al.: Reactive ion etching of PZT and RuO_2 films by environ-mentally safe gases, J. Mater. Res. 9, 2976–2980 (1994)
172. J. Baborowski et al.: Mechanisms of PZT thin film etching with ECR/RF reactor, Int. Ferroelectrics 31, 261–271 (2001)
173. S.H. Joo, J.J. Lee et al.: Stacked FRAM capacitor etching process for high density application, Integr. Ferroelectr. 37, 103–111 (2001)
174. C.W. Chung: Reactive ion etching of $Pb(Zr_xTi_{1-x})O_3$ thin films in an inductively coupled plasma, J. Vac. Sci. Technol. B 16, 1894–1900 (1998)
175. S. Koo, D. Kim, K. Kim, S. Song, C. Kim: Etching properties of $Pb(Zr_xTi_{1-x})$O3lead–zirconate–titanate thin films in an inductively coupled plasma Cl2/Ar and BCl3/Ar gas chemistries, J. Vac. Sci. Technol. B 1622, 1519–1523 (2004)
176. J. Baborowski, P. Muralt, N. Lederman: Etching of platinum thin films with dual frequency ECR/RF reactor, Integr. Ferroelectr. 27, 243–256 (1999)
177. J. Baborowski et al.: Etching of RuO2 and Pt with ECR/RF reactor, Vacuum 56, 51–56 (2000)
178. C.W. Chung, I. Chung: Etch behavior of Pb(ZrxTi1-X)O3 films using a TiO2 hard, J. Electrochem. Soc. 148, C353–C356 (2001)
179. S.H. Joo, J.J. Lee, K.M. Lee. S.D. Nam, S.W. Lee, S.J. Oh, Y.T. Lee, S.O. Park, H.K. Kang, J.T. Moon: Stacked FRAM capacitor etching process for high density application, Integr. Ferroelectr. 31, 103–111 (2001)

180. J. Baborowski, P. Muralt, N. Ledermann, E. Colla, A. Seifert, S. Gentil, N. Setter: Mechanisms of Pb(Zr0.53Ti0.47)O3 thin film etching with ECR/RF reactor, Integr. Ferroelectr. 31, 261–271 (2000)
181. C. Soyer, E. Cattan, D. Rémiens, M. Guilloux-Viry: Ion beam etching of lead–zirconate–titanate thin films: Correlation between etching parameters and electrical properties evolution, J. Appl. Phys. 92, 1048–1055 (2002)
182. R.G. Polcawich: Design, fabrication, test, and evaluation of RF MEMS series switches using lead zirconate titanate (PZT) thin film actuators, Ph.D. Thesis, Pennsylvania State University (2007)
183. C. Soyer, E. Cattan, D. Rémiens: Electrical damage induced by reactive ion-beam etching of lead-zirconate-titanate thin films, J. Appl. Phys. 97, 114110–7 (2005)
184. K.R. Udayakumar, T.S. Moise, S.R. Summerfelt: Ferroelectric capacitor hydrogen barriers and methods for fabricating the same, US Patent No. 7,183,602, Feb. 27 (2007)
185. B. Willing et al.: Gas spectrometry based on pyroelectric thin film arrays integrated on silicon, Sens. Actuators A 66, 109–113 (1998)
186. B. Willing et al.: Thin film pyroelectric array as a detector for and infrared gas spectrometer, Infrared Phys. Technol. 39, 443–449 (1998)
187. M. Kohli et al.: Pyroelectric thin film sensor array, Sens. Actuators A 60, 147–153 (1997)
188. P. Muralt et al.: Piezoelectric micromachined ultrasonic transducers based on PZT thin films, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 52, 2276–2288 (2005)
189. M. Lukacs, M. Sayer, S. Foster: Single element high frequency (<50 MHz) PZT sol gel composite ultrasound transducers, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 47, 148–159 (2000)
190. F.C. Duval, R.A. Dorey, R.W. Wright, Z. Huang, R.W. Whatmore: Fabrication and modeling of high-frequency PZT composite thick film membrane resonators, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 51, 1255–1261 (2004)
191. I.G. Mina, H. Kim, I. Kim, S.K. Park, K. Choi, T.N. Jackson, R.L. Tutwiler, S. Trolier-McKinstry: High frequency piezoelectric MEMS ultrasound transducers, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 54, 2422 (2007)
192. P. Marechal, F. Levassort, J. Holc et al.: High-frequency transducers based on integrated piezoelectric thick films for medical imaging, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 53, 1524–1533 (2006)
193. Q.F. Zhou, J.M. Cannata, R.J. Meyer, D.J. Van Tol, W.J. Hughes, K.K. Shung, S. Trolier-McKinstry: Fabrication and characterization of micromachined high-frequency tonpilz transducers derived by PZT thick films, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 52, 350–357 (2005)
194. J.J. Bernstein, S.L. Finberg, K. Houston, L.C. Niles, H.D. Chen, L.E. Cross, K.K. Li, K. Udayakumar: Micromachined high frequency ferroelectric sonar transducers, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 44, 960–969 (1997)
195. B. Belgacem, F. Calame, P. Muralt: Piezoelectric micromachined ultrasonic transducers with thick PZT sol gel films, J. Electroceram. 19, 369–373 (2007)
196. S.S.N. Bharadwaja, M. Olszta, E.C. Dickey, S. Trolier-McKinstry, X. Li, T. Mayer, F. Roozeboom: Fabrication of high aspect ratio ferroelectric microtubes by vacuum infiltration using macroporous silicon templates, J. Am. Ceram. Soc. 89, 2695 (2006)
197. P. Muralt et al.: Fabrication and characterization of PZT thin-film vibrators for micromotors, Sens. Actuators A 48, 157–165 (1997)
198. M.A. Dubois, P. Muralt: PZT thin film actuated elastic fin micromotor, IEEE Trans. Ultrason. Ferroelectr. Freq. Control 45, 1169–1177 (1998)
199. P. Muralt: Ferroelectric thin films for micro-sensors and actuators: A review, J. Micromech. Microeng. 10, 136–146 (2000)
200. D. Peroulis, S.P. Pacheco, K. Sarabandi, L. Katehi: Electromechanical considerations in developing low voltage RF MEMS switches, IEEE Trans. Microw. Theory Techn. 51, 259–270 (2003)

201. S. Majumber et al.: Measurement and Modeling of Surface Micromachined, Electrostatically Actuated Microswitches, International Conference on Solid-State Sensors and Actuators, Chicago, IL, pp. 1145–1148 (1997)
202. G. Rebeiz: RF MEMS Theory, Design, and Technology (Wiley, Hoboken, NJ, 2003)
203. S.J. Gross, S. Tadigadapa, T.N. Jackson, S. Trolier-McKinstry, Q.Q. Zhang: Lead-zirconate-titanate-based piezoelectric micromachined switch, Appl. Phys. Lett. 83, 174–176 (2003)
204. H.C. Lee, J.Y. Park, J.U. Bu: Piezoelectrically actuated RF MEMS DC contact switches with low voltage operation, IEEE Microw. Wireless Comp. Lett. 15, 202–204 (2005)
205. H.C. Lee, J.H. Park, J.Y. Park, H.J. Nam, J.U. Bu: Design, fabrication, and RF performance of two different types of piezoelectrically actuated ohmic MEMS switches, J. Micromech. Microeng. 15, 2098–2104 (2005)
206. John J. Evans: DARPA, Disruptive Manufacturing Workshop (Arlington, VA, 2006)
207. M.S. Haque, H.A. Naseem, W.D. Brown: Residual stress behavior of thin plasma-enhanced chemical vapor deposited silicon dioxide films as a function of storage time, J. Appl. Phys. 81, 3129–3133 (1997)
208. E. Zakar, R. Polcawich, M. Dubey, J. Pulskamp, B. Piekarski, J. Conrad, R. Piekarz: Stress Analysis of SiO2/Ta/Pt/PZT/Pt Stack for MEMS Application, Proceedings of the 12th IEEE International Symposium on Applied Ferroelectrics, Honolulu, HI, pp. 757–759 (1999)
209. E. Zakar, M. Dubey, R. Polcawich, B. Piekarski, R. Piekarz, J. Conrad, R. Widuta: Study of PZT film stress in multilayer structures for MEMS devices, MRS Fall Symposium Proceedings, Vol. 605, pp. 287–292 (Boston, MA, 2000)

Chapter 6
Materials and Processes in Shape Memory Alloy

Takashi Mineta and Yoichi Haga

Abstract Actuators are a key factor of micro electro mechanical systems (MEMS). In particular, shape memory alloy (SMA) is an effective material for microactuators to generate large force and large displacement. In this chapter, basic properties of SMA materials, fabrication processes of bulk and thin film SMA actuators, and application devices (medical devices, fluidic devices, switches, tactile displays and cantilevers for atomic force microscopy (AFM)) are described. Microactuators of SMA have some disadvantages such as difficulty to batch fabricate and assemble, high electric power for thermal driving, and low controllability of displacement. In this chapter, integration techniques with other MEMS technologies to overcome the disadvantages of SMA actuators also are described with introductions of typical application devices.

6.1 Introduction and Principle

6.1.1 Basic Principle

Shape memory alloys (SMAs) are excellent materials for microactuators which can generate large force and large displacement. Shape memory alloy can recover its original shape after it is deformed over its elastic limit by external force. As shown in Table 6.1 compared with other types of actuators, the SMA actuators shows the highest energy density (work/unit volume), on the order of 10^7 J/m^3 [1].

The response of SMA actuators tends to be slow due to the heat capacity of the actuator, resulting in lengthy heating and cooling. Because deformation of SMA is caused by a crystalline phase transformation which occurs without any diffusion of

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Table 6.1 Work per unit volume for various microactuators

Actuator type	W/v (J/m^3)	Equation	Comments
TiNi SMA	2.5×10^7 6.0×10^6	$\sigma \cdot \varepsilon$ $\sigma \cdot \varepsilon$	Maximum one time output: $\sigma = 500$ Mpa, $\varepsilon = 5$ Thousands of cycles: $\sigma = 300$ Mpa, $\varepsilon = 2$
Solid-liquid phase change	4.7×10^6	$\frac{1}{3}(\frac{\Delta v}{v})^2 k$	k = bulk modulus = 2.2 GPa (H_2O) 8% volume change (acetamide)
Thermo-pneumatic	1.2×10^6	$\frac{F \cdot \delta}{v}$	Measured values: $F = 20$ N, $\delta = 50\,\mu$m, $v = 4$ mm $\times$ 4 mm $\times$ 50 μm
Thermal expansion	4.6×10^3	$\frac{1}{2}\frac{(E_s+E_f)}{v}(\Delta\alpha \cdot \Delta T)^2$	Ideal, nickel on silicon, s = substrate, f = film, $\Delta T = 200$ K
Electro-magnetic	4.06×10^5	$\frac{F \cdot \delta}{v}$ $F = \frac{-M_s^2 A}{2\mu}$	Ideal, variable reluctance: v = total gap volume, $M_s = 1$ V s m^{-2}
	2.8×10^4	$\frac{F \cdot \delta}{v}$	Measured values, variable reluctance: $F = 0.28$ mN, $\delta = 250\,\mu$m, $v = 100 \times 100 \times 250\,\mu$m^3
	1.6×10^3	$\frac{T}{v}$	Measured values, external field: Torque = 0.185 nN m^{-1}, $v = 400 \times 40 \times 7\,\mu$m^3
Electrostatic	1.8×10^5	$\frac{F \cdot \delta}{A \cdot \text{gap}}$ $F = \frac{\varepsilon V^2 A}{2\delta^2}$	Ideal: $V = 100$ V, δ = gap = 0.5 μm
	3.4×10^3	$\frac{F \cdot \delta}{v}$	Measured values: comb drive: $F = 0.2$ mN (60 V), $v = 2 \times 20 \times 3000\,\mu$m^3 (total gap), δ = gap = 0.5 μm
	7.0×10^3	$\frac{F \cdot \delta}{v}$	Measured values: integrated force array: v = device volume, 120 V
Piezoelectric	1.5×10^5	$\frac{1}{2}(d_{33}E)^2 E_f$	Calculated, PZT: $E_f = 60$ GPa (bulk), $d_{33} = 500$ (bulk), $E = 40$ kV cm^{-1}

Taken from a report by Krulevich et al. [1] (Reprinted with permission. Copyright ©1996 IEEE.)

substances [2], an SMA actuator can deform rapidly when it is miniaturized thus reducing its heat capacity.

6.1.2 Introduction of TiNi and TiNi-Base Ternary Alloys

The shape memory effect (SME) has been discovered in many alloys, such as TiNi-based alloys (typically Ti-50 at.%Ni), Cu-Al-Zn, Cu-Al-Ni, and Fe-Mn-Si [2]. However, only TiNi-based alloys, which were developed in 1963, have come into wide practical use in industry. Since the 1970s, TiNi alloys have been used for thermal switches, tube couplings and other applications. Thin films of TiNi-based alloy have been studied and applied for microactuators since the 1990s [3–5]. Compared with other SMA materials, TiNi SMA has advantages such as high durability for repeated actuation cycles, small thermal hysteresis, and chemical stability.

The principles of SMA materials and actuators have been published in many review articles and books [1, 2, 6, 7], and reference to these publications is very useful for understanding the principles of SMA actuators in detail. In this section, an overview of the deformation mechanism of SMA is presented as follows.

The shape memory effect based on the phase transformation of SMA can be explained as resulting from deformation of the crystalline lattice, as shown in Fig. 6.1 [2]. At high temperature, SMA has an austenitic phase, as shown in Fig. 6.1a. When it is cooled below the start temperature of martensitic transformation (M_s), the transformation of the austenitic phase into the martensitic phase is initiated. At the finish temperature of martensitic transformation (M_f), the transformation is finished completely. This is a shear deformation without diffusion of atoms, which is completed within a very short time (Fig. 6.1b). In the martensitic phase, the shear strain is compensated due to the formation of twin crystals (variant) which consist of opposing martensitic lattices. The shape of the SMA material does not change in appearance despite the change of the crystalline phase from austenite

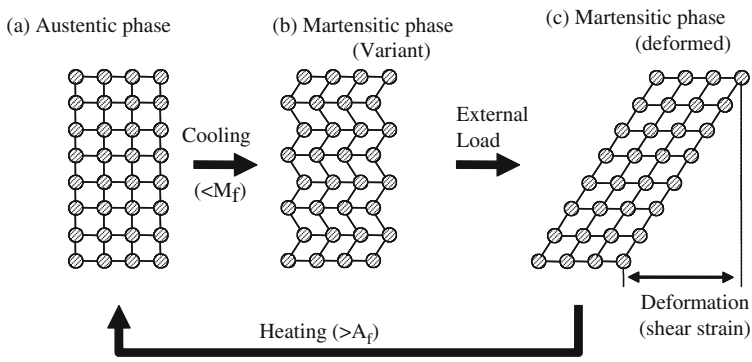

Fig. 6.1 Principle of shape memory effect based on deformation of crystalline lattice [2]

to martensite. When an exterior load is applied, the SMA material is deformed due to deformation of the twin phase as shown in Fig. 6.1c. When the SMA is heated above the reverse-martensitic phase transformation temperature (start temperature; A_s, finish temperature: A_f), the martensitic phase reverses to the austenitic phase, resulting in recovery of the original shape, as shown in Fig. 6.1a. In the case of plastic deformation of conventional metals, slip deformation caused by an exterior load results in permanent deformation which cannot be recovered after the load is released. In contrast, SMA can recover its original shape as mentioned above.

Shape memorization is achieved by thermal treatment. The SMA is clamped as the shape to be memorized during the thermal treatment. Shape memory alloys with one-way SME, which was described above, are widely used at present. Although there is another SMA type with two-way deformation, as mentioned below (Section 6.1.4), it is not always suitable for actuations with a large applied load.

Shape memory alloy goes through a phase transformation loop of stress vs. temperature under constant strain during heating and cooling, as shown in Fig. 6.2a. Another phase transformation loop of strain vs. temperature under constant stress is also useful to characterize SMA (Fig. 6.2b). In the process of cooling from high temperature, martensitic transformation starts when the SMA is cooled below M_s and is finished at M_f. In the heating process, the reverse martensitic transformation starts and is finished at A_s and A_f, respectively. In addition, a rhombohedral phase (R-phase) often appears in TiNi alloy.

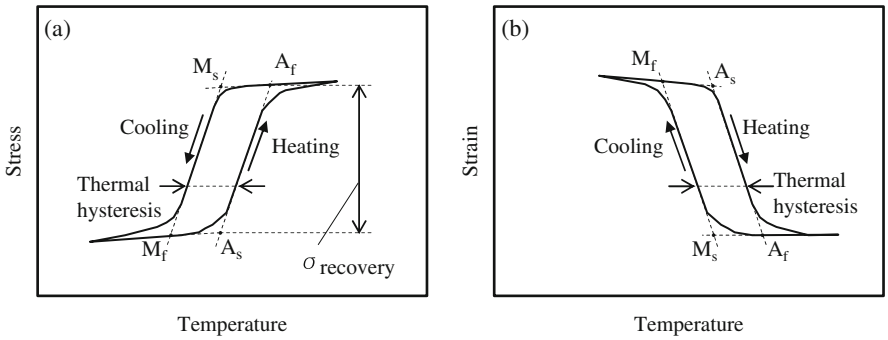

Fig. 6.2 Phase transformation loops during heating and cooling [1, 2]. (**a**) Stress vs. temperature under constant strain, (**b**) Strain vs. temperature under constant stress

Differential scanning calorimetry (DSC), by which the exothermic and endothermic heat flow can be measured during the phase transformations, is a common method for characterizing SMA. It should be noted that phase transformation temperatures are influenced by both external and intrinsic stress of the SMA. Electric resistivity change in the heating and cooling cycle is also useful for measuring the phase transformation temperatures of SMA.

6.1.3 Super-Elasticity

At constant temperature, SMA shows a force-displacement relationship which corresponds to the stress-strain relationship, as shown in Fig. 6.3a. When an external stress is applied to an SMA above its elastic limit, the SMA is pseudo-plastically deformed in the low temperature phase. Although further strain causes permanent-plastic strain, the SMA is strained reversibly (typically up to several percent) in the pseudo-plastic range. After the external force (stress) is released from the pseudo-plastic range, strain is retained. This retained strain can be recovered completely by heating above the austenitic temperature (A_f).

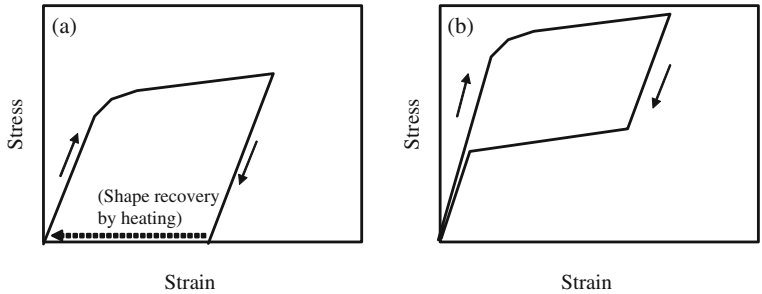

Fig. 6.3 Stress-strain behavior of SMA at constant temperature. (**a**) Shape memory effect, (**b**) super-elasticity

At temperatures higher than A_f, SMA shows super-elasticity, as shown in Fig. 6.3b. When external stress is applied to the SMA in the austenitic phase, it is deformed over its elastic limit due to the stress-induced martensitic transformation. After the external stress is released, the martensitic phase re-transforms into the high temperature phase, and then the SMA recovers its original shape by itself. The super-elastic effect enables the SMA to recover its original shape, even though it is deformed above its elastic limit, as shown in Fig. 6.3b.

Shape memory alloy materials which have a phase transformation temperature (austenitic finish temperature) below room temperature are called "super-elastic alloys". TiNi-based super-elastic alloys have been used for commercial products such as eyeglass frames, mobile phone antennas, and brassiere wire.

6.1.4 One-Way Type, Two-Way Type, All-Round-Way Type

The deformation mechanism mentioned above is usually called "one-way shape recovery". One-way SMA is deformed only once when it is heated. After the one-way SMA recovers its original shape completely by heating above A_f, it cannot be deformed without external force. In most cases at present, one-way SMA with a bias mechanism is widely used due to large force generation and small thermal hysteresis [2, 7].

The two-way shape memory effect can be obtained in TiNi alloys with control of martensitic transformation by intrinsic stress [4, 7]. By the two-way effect, TiNi alloy can be deformed to the memorized shape by heating, and then it can be deformed in another direction by cooling, resulting in reciprocatory deformation between two shapes without any external bias force [4, 7]. A particular type of the two-way effect is called "all-round type effect", which occurs in Ni-rich TiNi alloys after aging treatment under a constrained shape. Ni-rich precipitations (such as Ti_3Ni_4) provide an intrinsic stress field surrounding the TiNi parent phase [2]. Two-way SMA is suitable for simple structured actuators because reciprocatory actuation can be performed by itself without an external bias mechanism. However, there are disadvantages in two-way SMA. The shape recovery force generated by the two-way effect is much less than that by the one-way type effect. Also, two-way SMA tends to have large thermal hysteresis.

6.2 Materials Properties and Fabrication Process of SMA Actuators

Figure 6.4a shows the force generation by an SMA as a function of displacement at various temperatures. When the SMA is heated up to the A_s, the force generation is initiated. The force generation increases with increasing temperature until the SMA is heated up to the A_f. In order to design an SMA actuator accurately, it is important to comprehend the actual force-displacement property (stress-strain property) of the SMA to be used.

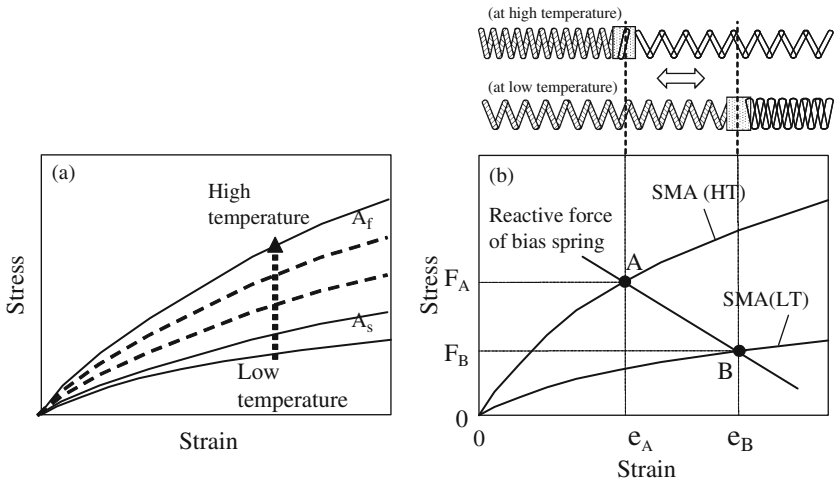

Fig. 6.4 Force-displacement curves of SMA at various temperatures (**a**), and principle of one-way SMA actuator with a bias spring (**b**)

For repeated motion, one-way type SMA should be used with a bias spring to recover the shape before the actuation, as shown in Fig. 6.4b [2]. Force-displacement curves of the SMA at low temperature and at high temperature are generally illustrated as the curves of SMA (HT) and SMA (LT) in Fig. 6.4b, respectively. At low temperature, the connection face between the SMA and the bias spring is located at the point B at which force of the SMA (LT) and reactive force of the bias spring are balanced. When the SMA is heated above A_f, the connection face moves to point A at which the force of the SMA (HT) and reactive force of the bias spring are balanced. Stroke of reciprocatory actuation ($e_B - e_A$) can be obtained by heating and cooling.

6.2.1 Bulk Material

The bulk material for SMA is mainly TiNi alloy ingots which are processed into required shapes.

Shape memory alloy wires produced by drawing are the most widely used products. Such wire comes in several diameters and can be actuated by Joule heat generated by direct flow of an electrical current into the SMA without any heater or cooler when the wire diameter of the coil is small. The direction of movement of the SMA wire is generally contractional, but bending or torsional direction is also used.

Shape memory alloy coil actuators, which are fabricated by winding SMA wire, are also commercially produced and widely used. Shape memory alloy coil can be obtained by helical cutting of an SMA tube or pipe [8]. The external diameter of the SMA coils used as actuators is generally 100–500 μm, and the wire diameter is less than 200 μm. The direction of movement is not only the contractional direction, but also the extension and torsional directions are also available. Shape memory alloy coil actuators have the advantages of flexibility and large stroke per unit length.

SMA thin plates, sheets or ribbon are fabricated by rolling. There is also a technique for lamination and rolling of thin Ti and Ni sheets and thermal diffusion [9, 10]. The thickness of the bulk thin plates is generally around 10–100 μm and the directions of movement are bending and torsional. A planar shape can be cut out for several types of fine patterning and micromachining, for example, photolithography and etching.

Shape memory alloy pipes or tubes are also fabricated by drawing. The external diameter is generally around 1–3 mm and wall thickness is around 10–100 μm.

Sintering of TiNi powder filled in a mold has also been studied for obtaining arbitrary shapes of bulk SMA (Fig. 6.5) [11].

6.2.2 Thin Film

Many TiNi-based alloy materials have been prepared by melting metallurgy. On the other hand, novel fabrication techniques for TiNi-base thin foils such as sputtering

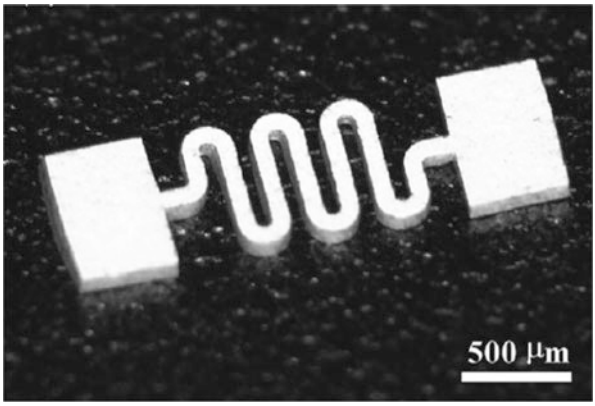

Fig. 6.5 TiNi Microspring structure [11] (Reprinted with permission. Copyright 2004 Elsevier)

[1, 3–6, 12–20], evaporation [21–23], laser ablation [24], and rapid solidification [25], have also been studied. In particular, the evolution of SMA film deposition techniques such as sputtering and evaporation are important for devices of micro electro mechanical systems (MEMS). Shape memory alloy films with high performance have been realized by film deposition techniques, for example, sputtered TiNi film can realize a shape recover force of 600 MPa and shape recovery strain of 6%, which are sufficiently practical properties [16].

6.2.2.1 Sputtering

Sputtering has been used for fabrication of TiNi-based thin films since the 1990s [1, 3–6, 12–20]. In particular, magnetron sputtering has been used most frequently. Because sputtered TiNi-base thin films tend to be amorphous, the film should be annealed above the crystallization temperature to obtain the shape memory effect.

There have been numerous reports on sputtering of TiNi-based alloy films using a single alloy target [3–5, 12–14]. In sputtering deposition using a single alloy target, the chemical composition of the target should be adjusted so that the sputtered film has a desired composition. Following are certain points which should be kept in mind when sputtering with a single alloy target. The surface of the alloy target should be carefully cleaned by pre-sputtering to remove the oxide layer on the target surface. However, lengthy pre-sputtering results in unbalance of the target composition, for example, titanium is lost during pre-sputtering due to its high sputter yield [12]. In the case of magnetron sputtering, it should also be noted that sputtering and re-sputtering of some materials onto the erosion grooves in the target cause compositional variations in the film deposited on the substrate [12].

To adjust the composition of SMA film sputtered from a single alloy target, small plates of Ti or Ni are used to partially cover an alloy target [6]. The chemical composition of the deposited film can be adjusted by changing the ratio of the areas covered by the Ti and Ni plates.

There have also been many trials to sputter from separate metal targets of titanium, nickel, and other additional elements. TiNiCu alloy films [19] and TiNi alloy films [20] have been realized by sputtering deposition with separate metal targets. When individual pure metal targets are sputtered, the substrate passes through each deposition area of the metal target rapidly. The sputtering rate of each metal is controlled by electric power individually applied to the target to control the composition of the deposited alloy. Compared to sputtering with a single alloy target, sputtering with separate multi targets is advantageous for easy adjusting the film composition, but special sputtering equipment with multi-targets is required. In sputtering with separate targets, a substrate rotating mechanism is necessary to obtain a uniform film composition.

6.2.2.2 Evaporation

It is difficult to obtain a uniform composition along film thickness by using conventional evaporation techniques. At the early stage of evaporation, Ni content tends to be higher than that of Ti because the vapor pressure of Ni is higher than that of Ti.

There is a unique deposition method termed flash-evaporation, by which small alloy pellets as the evaporation source are supplied from a storage holder to a heated tungsten boat via a guide pipe one by one [21–23]. To omit the deposition at an early stage of the evaporation, the deposition starts after a certain closed-shutter time has elapsed from the start of the pellet vaporization. The evaporation of the pellets is subsequently repeated, resulting in the deposition of a thick film with a multi-layered structure.

6.2.2.3 Non-planar Thin Film Deposition

In addition to deposition on the flat surface of substrates, there have been some studies on SMA deposition on non-planar surfaces, particularly on the cylindrical surface of a core rod or pipe. Figure 6.6 shows a tubular actuator-unit for the multi-directional bending mechanism [26]. Three meandering-shaped SMA actuators are formed in a TiNi cylindrical film with a thickness of 10 μm, which are flash-evaporated on a core Cu pipe with an outer diameter of 3 mm. The TiNi film can be uniformly deposited on a cylindrical surface of the core pipe with rotation during deposition. After the deposition, the TiNi film on the core pipe surface is patterned by electrochemical etching with a photoresist mask pattern which is formed by non-planar photolithography. After the core Cu pipe is dissolved selectively in concentrated HNO_3, a self-standing tubular TiNi actuator-unit is obtained.

Sputtering has been also used for tubular TiNi film deposition on core material. TiNi films with a thickness of 10 μm were obtained on Cu wires (50 μm in diameter) by rotating deposition [27]. TiNi crystalline grains can grow more uniformly by rotating deposition than two-step deposition on both sides of the core wire. Ion beam sputtering has also been employed [28]. By using ion beam sputtering with Ni and Ti targets, a TiNi film with a thickness of 2 μm can be deposited on a Cu shaft which is rotated during the sputtering.

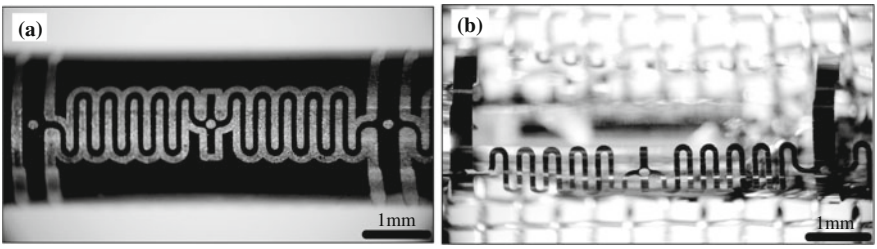

Fig. 6.6 Tubular actuator fabricated from a flash-evaporated TiNi film (10 μm) on cylindrical surface of a core Cu pipe with an outer diameter of 3 mm [26]. (Reprinted with permission. Copyright 2004 The Institute of Electrical Engineers of Japan) (**a**) Patterned by electrochemical etching with a non-planar photoresist mask, (**b**) core Cu pipe removal

Properties of tubular SMA film, in particular crystalline orientation, are not always similar to those of a film obtained by one-side deposition on a flat surface [27, 28].

6.2.3 Micromachining

TiNi alloy is a difficult material to machine, thus etching is generally used for MEMS applications. Grinding and micromilling are possible, but the optimal machining condition is limited and considerable tool wear can be expected [29]. Carbide tooling is suitable for machining.

Micromachining with a water jet requires high water pressure, which can cause undesired distortion of the SMA. A study of erosion resistance of TiNi alloy using a water jet has indicated that good erosion resistance of the TiNi alloy is due to its elastic behavior which relives local strain [30].

Laser cutting and electro-discharge machining (EDM) exhibit relatively good results. Several designs of SMA microactuators can be realized with laser machining. A Nd:YAG laser is widely used for micromachining of SMA, for example, intravascular stents or micro actuators, as shown in Fig. 6.7 [31]. A heat-affected zone (HAS) formed on the outer surface of SMA and debris and TiO_2 particles may slightly deteriorate the SME [32]. Femtosecond laser ablation allows micromachining of memorized SMA with no deterioration of its SME since the laser pulse width is very short (nanosecond order), such that heat generation is sufficiently reduced during laser machining [8, 33].

Electro-discharge machining (EDM) is an electro-thermal process by which the material is removed by electro-discharges occurring between the workpiece and tool electrode immersed in a liquid dielectric medium. In the case of micro-EDM, low-speed machining is required to obtain a smooth surface. After EDM, re-cast hard materials, the SME of which is slightly deteriorated, are observed on the EDM surfaces of TiNi SMA [34]. A disadvantage of EDM is that a starting hole is needed for the wire unless the wire starts from the side of the workpiece [35].

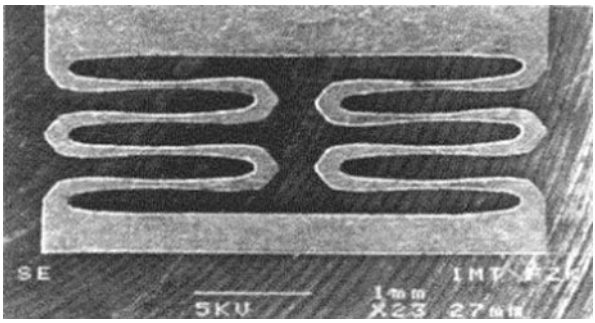

Fig. 6.7 Meandering SMA microactuator [31] (Reprinted with permission. Copyright 1998 Elsevier)

6.2.4 Etching and Lift-Off

6.2.4.1 Case and Example

Chemical Etching and Dry Etching

It is important to establish micro-patterning techniques for SMA materials to realize micro actuators with fine patterns. TiNi alloy is well known as a corrosion-resistant material in other words, it is a difficult-to-etch material. There are few chemical etching techniques; mixed solution of fluoric acid and nitric acid is known as a chemical etchant of TiNi alloy [3, 36]. There have been many reports on chemical etching of TiNi thin films in fluoric and nitric acid.

Reactive ion etching (RIE) with $SiCl_4$ as a process gas has also been attempted [36]. The etch rate of the RIE was about 10 nm/min. It is difficult to obtain a high etch rate due to the low vapor pressure of Ni compound.

Lift-Off

The lift-off process has also been attempted for patterning of deposited SMA film as shown in Fig. 6.8 [14]. On a thin evaporated film of Cr (150 nm) on an SiO_2 substrate, an 11 μm thick polyimide layer is spin-coated and cured. A second Cr film is evaporated and patterned on the polyimide layer. The polyimide layer is patterned using O_2 RIE with a Cr mask. The polyimide is slightly under-cut during the RIE to facilitate the subsequent lift-off process. A TiNi film with a thickness of 7–10 μm is deposited using DC sputtering. After the TiNi deposition, the polyimide layer is removed in hot KOH solution, resulting in the lift-off patterning. The TiNi with a narrow-pattern is released by wet etching of the sacrificial Cr layer due to the side etching of Cr.

Electrochemical Etching

Electrochemical etching is one of the most suitable methods to etch TiNi SMA with a high etch rate [37–41]. Compared to conventional chemical etching,

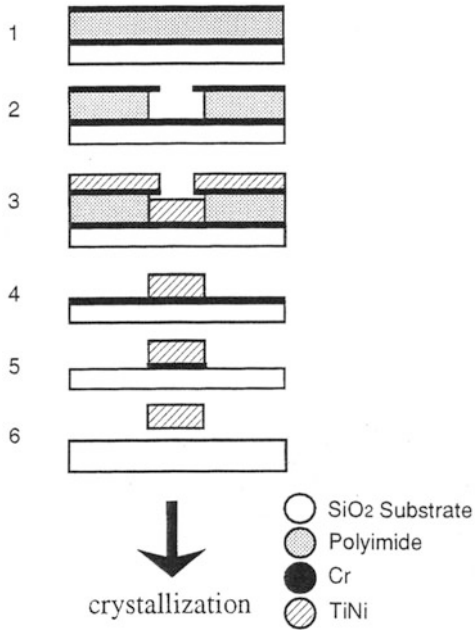

Fig. 6.8 Process chart of TiNi film sputtering and lift-off patterning. (1) Deposition of Cr/polyimide (11 μm)/Cr layers, (2) Upper Cr patterning and O_2 RIE, (3) TiNi sputtering (7–10 μm), (4) Lift-off by polyimide removal KOH solution, (5) and (6) Cr wet etching to release movable parts [14] (Reprinted with permission. Copyright 1997 The Institute of Electrical Engineers of Japan)

electrochemical etching has features including high etching rate, low side etching and a smooth etched surface [38–40]. An etch factor (etched depth/under-cut) higher than 1.5 can be obtained. Another advantage of electrochemical etching is that normal photoresist can be easily used as an etching mask. Large-scale equipment is not necessary for electrochemical etching. Electrochemical etching can be carried out using a simple setup, as shown in Fig. 6.9 [40, 41]. Shape memory alloy coated with a photoresist is used as an anode. The anode and a counter cathode, for example a stainless-steel plate, were facing each other with a gap of several tens of millimeters in the electrolyte solution. A solution of 5 vol% (about 1 mol/L) H_2SO_4-methanol has been used as an electrolyte for electrochemical etching of SMA [37, 38]. When a direct-current (DC) voltage, typically 8–10 V, is applied between the electrodes, the SMA anode is etched electrochemically. If the electrolyte solution contains water, anodic oxidation of the SMA surface occurs simultaneously, resulting in inhibition of uniform etching.

In addition to continuous voltage, pulse voltage is also useful for the electrochemical etching. The application of pulse voltage slightly suppresses under-cutting in narrow groove etching because reaction products are replaced with fresh solution when the voltage is turned off [40]. However, the etched surface tends to be rough in the case of pulse etching.

Through-layer etching is very important for the precise fabrication of micro actuators from an SMA sheet. During over-etching, the remaining SMA patterns tend to be etched non-uniformly due to imbalance of the electrolytic current distribution. The etching proceeds at the places where the current is concentrated, while it stops

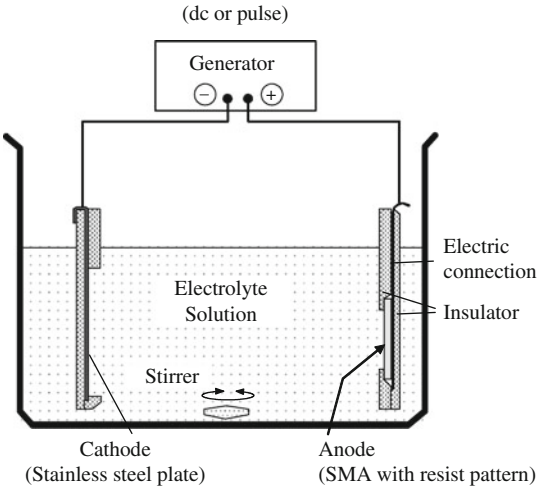

Fig. 6.9 Setup for electrochemical etching of SMA [40, 41] (Reprinted with permission. Copyright 2000 Elsevier, 2004 IOP)

at other places. In order to overcome the problem of non-uniform sheet-through etching, a conductive dummy layer of Ni or Cu, which is formed on the back side of the SMA sheet previously, is very effective in maintaining a uniform current distribution during the over-etching. The dummy layers of Ni and Cu can be easily removed in concentrated nitric acid without damage to the SMA surface [40, 41].

Figure 6.10 shows the process of fabrication of an SMA actuator from an SMA sheet by using the double-side electrochemical etching with Ni dummy layers. Double-side etching is effective to depress the side-etching. Figure 6.11 shows meandering-shaped SMA actuators fabricated from an SMA sheet by using the etching process shown in Fig. 6.10.

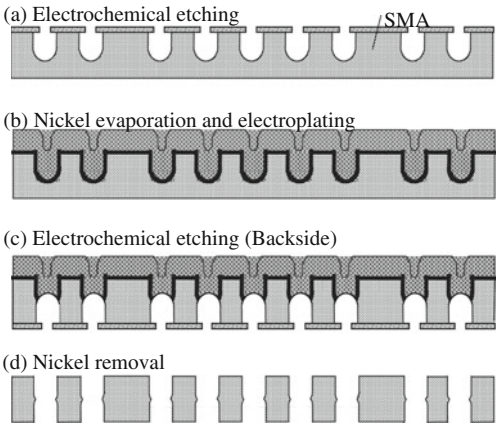

Fig. 6.10 Double-side electrochemical etching of TiNi sheet using a nickel dummy layer [40] (Reprinted with permission. Copyright 2000 Elsevier)

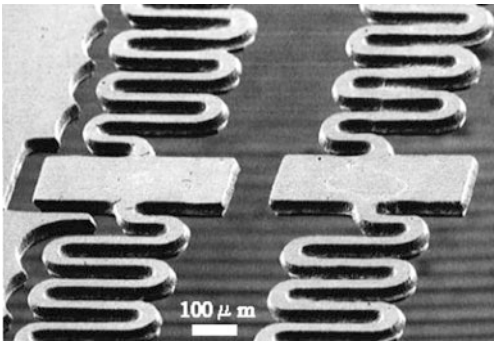

Fig. 6.11 Electrochemical etching of SMA sheet (40 μm thick, double-side etching) [40] (Reprinted with permission. Copyright 200 Elsevier)

Electrochemical etching also can be used for fabrication of non-planar SMA structures. Figure 6.12 shows a tubular SMA actuator unit for an active catheter bending mechanism, in which meandering-shaped SMA actuators are formed. An SMA tube, covered with a photoresist pattern formed by non-planar photolithography, is electrochemically etched in a cylindrical vessel with a cylindrical cathode, resulting in the fabrication of a tubular SMA actuator-unit [42].

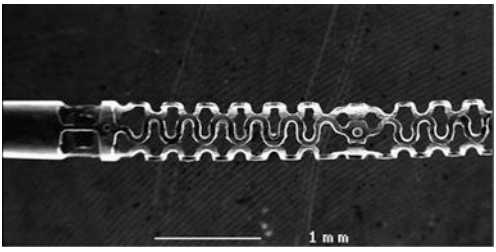

Fig. 6.12 Tubular SMA actuator-unit electrochemically etched from a SMA tube (outer/inner dia.: 600/500 μm) [42] (Reprinted with permission. Copyright © 2002 IEEE.)

A non-corrosive, non-toxic and stable electrolyte solution is required for industrial applications. Inorganic salt of LiCl, which has high solubility in alcohol [41], is useful for the electrolyte solution. In 1 mol/L LiCl-ethanol solutions, good etching with a high etch factor of 1.5 and a smooth etched surface can be carried out when LiCl is used as the electrolyte. The etch rate can be depressed less than 4 μm/min. In addition to good etching properties, the solution has other advantages, for example, it is non-corrosive, non-toxic and stable for a long term. The SMA can be etched with a smooth surface in LiCl-ethanol solution because there are no influences of other electrochemical reactions, such as anodic oxidation that tends to inhibit surface smoothing.

6.2.5 Assembly

For purposes of mechanical fixation of SMA or parts with SMA, several assembly methods, for example, mechanical fixation, adhesion, welding and soldering, are used. Electrical connections are also formed for actuation of SMA by supply of an electrical current.

6.2.5.1 Mechanical Fixation

Crimping and fastening are used for mechanical fixation of SMA. Crimping is joining two parts by deforming one or both of them to hold the other, solderless terminals made of deformable metal being used, especially in the case of SMA wires and coils. Fastening by screw bolts or other devices such as, hooks, pins, or wires, is also used to fix SMA. The advantage of this method is ease of reattachment. These mechanical fixation methods are advantageous in that they are simple and the formation of conductive connections is relatively easy. Disadvantages are the requirement of large connection areas, impreciseness of length adjustment, low productivity because of the handmade process and fracture susceptibility in the fixation area because of local deformation and local stress of SMA.

6.2.5.2 Adhesion

In the assembly of SMA parts using polymer material for intermediate adhesion, not only a nonconductive adhesion part but also a conductive adhesion part using conductive resin are employed. As the nonconductive adhesive part, epoxy resin [40] and UV curable resin [43] have been utilized. As the conductive adhesive part, epoxy resin containing silver powder [40] or UV curable conductive epoxy resin have been utilized [44].

Silane coupling agents can be used for improving adhesion between the SMA and polymer material [45].

Laser assisted deposition has been carried out for fixing an SMA coil to silicon parts for active bending catheters [44], vaporized polymer source material being selectively polymerized and deposited on the UV light-irradiated area.

A disadvantage of adhesion is that considerable time is necessary to make all connections when these connections have to be formed individually. Cyanoacrylates can be cured in a shorter time than epoxy resin but are relatively brittle. Adhesive tape (single sided or double sided) can be used for temporary fixation.

6.2.5.3 Welding

Welding of TiNi SMA to itself can be successfully performed if the heat-affected zone is minimized and welded in an inert atmosphere. Lasers such as CO_2 lasers [46], resistance welding and tungsten inert gas (TIG) welding can be used for this purpose. Several self-expanding TiNi stents have been fabricated by welding at a specific location [47]. A laser-cut patterned TiNi sheet was rolled up and welded

at a specific location in an early example. Almost all laser-cut stents are fabricated from TiNi tubes and do not require welding. Wire-based stents have been fabricated by welding TiNi wires at specific locations to form hexagonal cells, as shown in Fig. 6.13 [47].

Welding TiNi SMA to dissimilar material can be performed, for example, attachment of a radiopaque marker such as a tantalum marker to a stent (Fig. 6.14) [2, 3]. Attention should be paid to welding strength because of the brittle interface layer between TiNi and dissimilar metals.

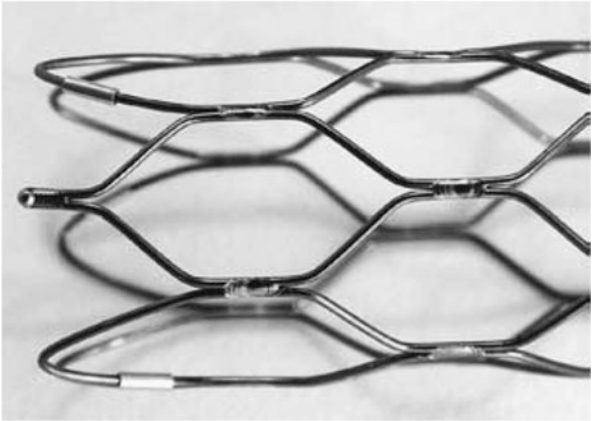

Fig. 6.13 Stent fabricated by welding TiNi wires [47] (Reprinted with permission. Copyright 2004 Springer)

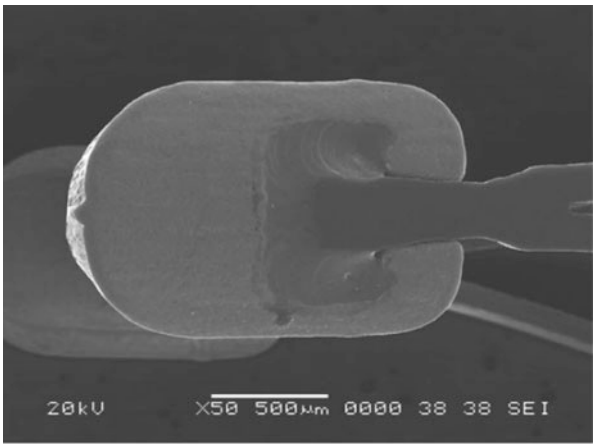

Fig. 6.14 Welded tantalum markers [47] (Reprinted with permission. Copyright 2004 Springer)

6.2.5.4 Soldering

Solder composed of fusible alloys has been successfully used for joining TiNi SMA with other materials. As the surface oxide layer of TiNi alloy prevents solder wetting, an aggressive flux (such as strong acid, aluminum paste, etc.) or ultrasonic soldering is used to remove the oxide layer. After removal of the oxide layer by the flux, standard solder such as Sn-Ag can be used. Ultrasonic soldering utilizes cavitation by ultrasonic vibration energy to remove the oxide layer, and some specially designed solder of Sn-Al is suitable for joining TiNi alloy with other materials. Soldering is useful not only for joining SMA to SMA but also for joining SMA to dissimilar material, such as stainless steel.

Plating of a solderable intermediate metal layer on the SMA surface before soldering is effective. Ni, Au or Cu are suitable for this purpose. However, adhesion between the oxide layer and the plated metal is problematic. For tight fixation of an SMA wire on a metal pattern, temporary-soldering and additional crimping of the solder by a sawtooth punch can be employed [48].

6.2.6 Materials and Processes Selection Guidance

6.2.6.1 Materials (Bulk/Thin Film)

Common Mistakes

It is important to note that mechanical and thermal properties of SMA are not independent but are related closely. For example, the limit of reversible cycles strongly depends on maximum strain.

For use in repeated actuation, an SMA actuator should be designed with consideration of fatigue. The limit of reversible cycles of actuation of TiNi SMA strongly depends on maximum strain or maximum stress which is applied to the SMA. A shape recoverable strain as high as 8% can be obtained under optimum conditions without load [49]. However, usable strain for cyclic actuation is much smaller. Table 6.2 shows typical reversible cycles of the martensitic transformation of polycrystalline TiNi SMA. The reversible actuation cycles decrease significantly with increasing maximum strain or maximum stress. The data in Table 6.2 should be considered only as a rough guideline. It is important to understand in detail the

Table 6.2 Dependence of an achievable number of repeated actuation cycles as a function of maximum strain and stress [49]

Cycles	Maximum strain (%)	Maximum stress (MPa)
100	4	275
10,000	2	140
>100,000	1	70

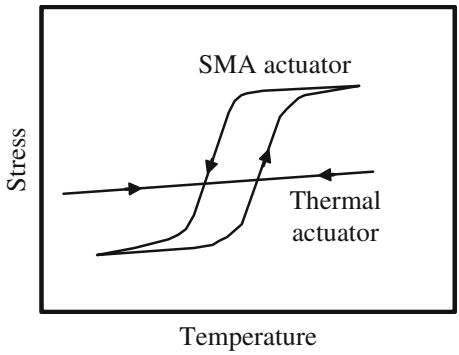

Fig. 6.15 Comparison of characteristics of SMA actuators with thermal actuators (stress vs. temperature under constant strain)

fatigue behavior of the SMA to be used. When designing SMA actuators, maximum strain or maximum stress should be determined according to the required actuation cycles.

It should be also noted that an SMA actuator is drastically deformed in a narrow temperature range. Figure 6.15 is a schematic comparison of characteristics between SMA and thermal actuators. A thermal actuator can generate actuation force linearly due to thermal expansion in a wide temperature range, in spite of small force generation. In contrast, an SMA actuator generates force drastically in the range from the start temperature to the finish temperature of phase transformation. Accurate temperature control is necessary to control the force (displacement) of the SMA actuator continuously.

Specific Features of Materials: TiNi Binary Alloys

Regarding TiNi binary alloy, it is well known that phase transformation temperatures are extremely sensitive to alloy composition [2, 21, 50]. Figure 6.16 shows an example of transformation temperature dependence on the alloy composition in flash-evaporated TiNi film [21]. The composition change of only 1 at.% causes drastic transformation temperature change greater than several tens of degrees. It is necessary to accurately control the composition of TiNi alloy to obtain transformation temperatures with high reproducibility. It should be noted that in the case of TiNi bulk alloys or sputtered alloy films, the composition dependence on transformation temperature is slightly different from the data shown in Fig. 6.16. In addition to the alloy composition, the phase transformation temperature of TiNi SMA also strongly depends on annealing temperature and annealing time. It is important to evaluate the phase transformation temperatures of the TiNi alloys to be actually used.

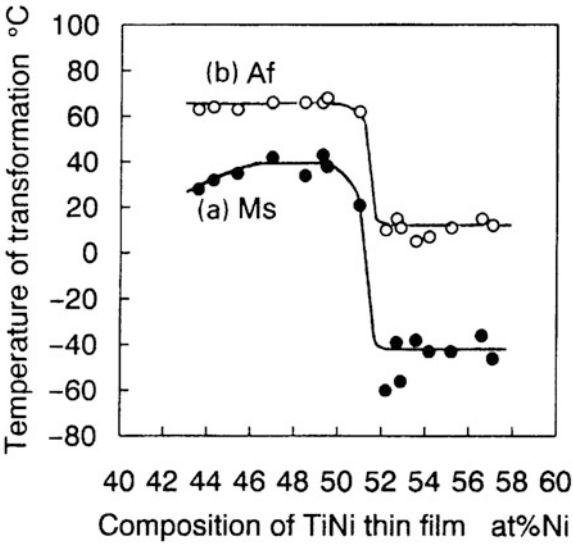

Fig. 6.16 Effect of composition of TiNi film on phase transformation temperatures [21] (Reprinted with permission. Copyright 1998 Elsevier) (Flash-evaporated TiNi film on silicon substrate, 6 μm thick, annealed at 500°C for 60 min)

TiNi Alloys with R-Phase Transformation (Low Thermal Hysterisis)

Fully annealed near-equiatomic TiNi alloys transform from the B2 parent phase directly to the monoclinic B19' phase martensitically during cooling. However, thermo-mechanically treated near-equiatomic TiNi alloys and Ni-rich alloys show two-step transformation with a rhombohedral (R) phase [51]. Typical strain and DSC curves of TiNi SMA with the R-phase transformation are shown in Fig. 6.17. When TiNi alloy is cooled from a temperature above A_f, R-phase transformation starts at R_s, which corresponds to the start temperature of actuator deformation. The first peak in the DSC curve is due to the transformation from the B2 phase to the R-phase. The second peak ranging from M_s to M_f in the DSC curve is due to transformation from the R-phase to the B19' phase.

When the SMA is re-heated from a temperature above M_s, at which the alloy is in the R-phase, only reverse-R-phase transformation (from R-phase to B2) occurs. Actuation using the R-phase and reverse-R-phase transformations of TiNi alloy is effective to obtain small thermal hysteresis.

It should be noted that the R-phase of TiNi alloys disappears at high temperature and lengthy annealing. If the R-phase is lost completely, actuation of TiNi alloy is caused by only the M-phase and reverse-M-phase transformations, resulting in large thermal hysteresis between the heating and cooling processes.

TiNi-Base Ternary Alloys

There have been many studies on TiNi-based ternary alloys in which a third element is contained to control the actuation properties such as deformation temperature and thermal hysteresis. Material properties of TiNiCu alloys (Cu is substituted for Ni)

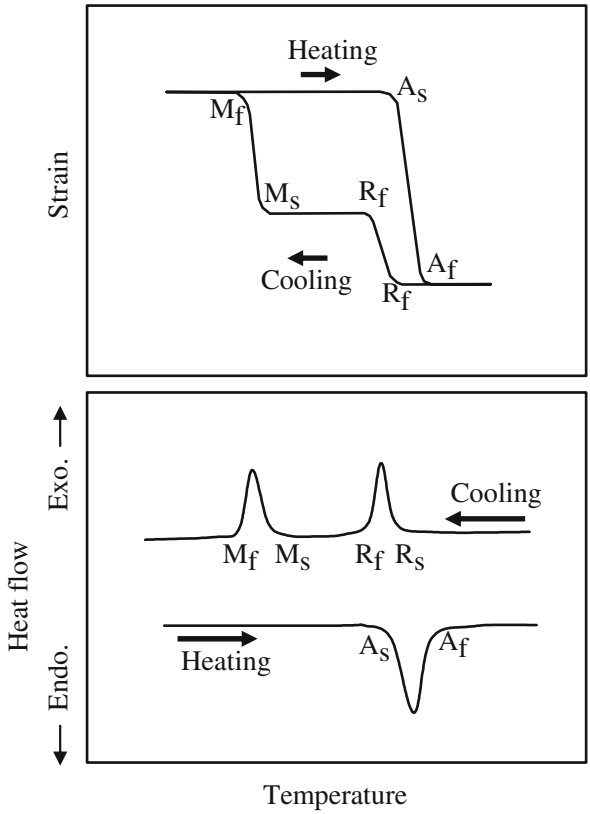

Fig. 6.17 Typical strain and DSC curves of TiNi SMA with the R-phase transformation

have been studied in many reports on bulk materials [2] and thin films [4, 52]. The addition of Cu is effective to decrease thermal hysteresis, which is the difference of phase transformation temperatures between the heating and cooling processes [53]. Small thermal hysteresis is favorable for repeated actuation in a narrow working temperature range between heating and cooling. TiNiCu bulk alloys containing 5–15 at.% Cu transform in two stages, from a cubic to an orthorhombic B19 phase, and then to a monoclinic B19' phase [2]. In the case of sputtered TiNiCu thin film, the alloy film containing 0–9.5 at.% Cu transforms in a single stage, from B2 to B19' [52]. In this region of single stage transformation, the width of thermal hysteresis of the TiNiCu thin film drastically decreases to 11 K with increasing Cu content. TiNiCu film containing 9.5 at.% Cu shows two-stage phase transformation, from B2 to B19, and then to B19'. By addition of more Cu, phase transformation becomes a single stage from B2 to B19. When Cu content is below 9.5%, a maximum reversible strain of 3.9% is obtained at a stress of 200 MPa. When Cu content is above 9.5%, maximum reversible strain decreases to 1.1% with increasing Cu content to 18 at.%. In many applications, TiNiCu alloys with Cu content from 5 to 10 at.% are used. The addition of Cu also affects the mechanical properties, for example, the elastic limit (yield stress) of martensite decreases in TiNiCu alloy. This behavior is favorable for

actuator applications. TiNiCu SMA actuators can be reset by small external force in the martensitic, resulting in large work generation [7].

The shape recovery temperature of SMA material is very important in many applications. For example, SMA with a high deformation temperature is not suitable for medical devices for use in the human body due to thermal damage. The deformation temperature of ternary alloy with added vanadium (TiNiV) tends to be lower [54]. In contrast, a high deformation temperature is favorable for exact actuation without deformation error caused by ambient temperature fluctuation. Ternary alloys with added palladium (TiNiPd) show a strong increase in transformation temperature [6, 7].

TiNb Alloys (Ni Free)

TiNi alloys have been used extensively for permanent implants (stents and other applications). Surface treatment is required to prevent corrosion. In recent years, bio-compatible SMAs without nickel content such as NbTi-based alloy have also been studied for application in medical devices for implantation in the human body because the toxicity of nickel is viewed with suspicion [55].

6.2.6.2 Process

Common Mistakes

Thin Films

As mentioned in Section 6.2.2.1 (Sputtering), it is not easy to control the chemical composition of deposited film in the case of sputtering deposition using a single alloy target. Film composition tends to differ from the composition of the target due to the sputter rate difference between Ti and Ni. Sputtering with separate targets is one solution to obtain good controllability of film composition. However, special equipment having multi-targets with individual electric power control is necessary.

To utilize the feature of large force generation, thick SMA film is required in many applications. However, it is not easy to obtain SMA film thicker than 10 μm. To obtain thick SMA film with sufficient film quality, it is important to stably control film composition. For example, in the sputtering process with an alloy target, film composition tends to change during thick film deposition due to the difference of sputter rate of Ti from Ni, as mentioned above. Figure 6.18 shows examples of thick film deposition by flash-evaporation as mentioned in Section 6.2.2.2 (Evaporation) [23]. The cross sectional views of both TiNi (Ti-45 at.%Ni) and TiNiCu (Ti-46 at.%Ni-0.5%Cu) thick films show a lamellar structure, which corresponds with the flash-evaporation cycles. Top surface roughness of the TiNi film increases with increasing film thickness due to the significant growth of crystalline grains during the thick deposition. The grain growth results in defects in grain boundary, leading to reduction of strength and flexibility of the film. In contrast, the addition of a low concentration of Cu (<3 at.%) suppresses the grain growth of the alloy film. The TiNiCu film is not fractured with a strain of 5% or larger, despite being thicker than 30 μm.

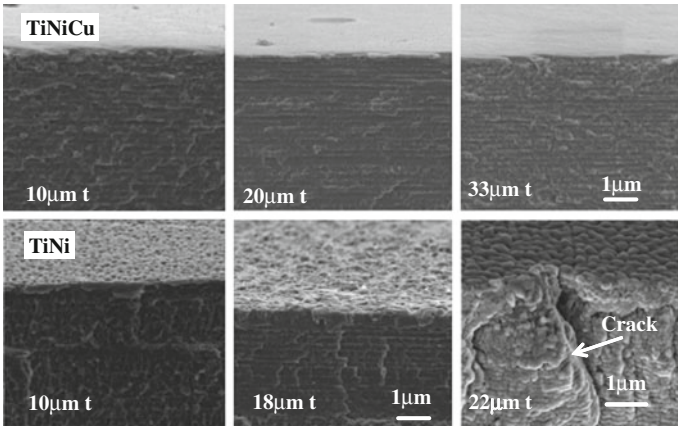

Fig. 6.18 Cross-sectional structures of flash-evaporated thick SMA films [23] (Reprinted with permission. Copyright 2009 Elsevier)

Bulk

The material of most bulk SMA is TiNi alloy. Because of the poor mechanical workability of TiNi alloy which results in high cost and defects in SMA, choice of shapes of bulk SMA is limited.

Wires are fabricated by drawing and widely available. Coils are also commercially available, but the cost of coiling is relatively high. Bulk plates of sheets fabricated by rolling are relatively thick and not suitable for fine patterning, for example, micromachining or etching after photolithography. In the case of pipes or tubes, although the cost of tube shaping is high, particular sizes of SMA tubes or pipes are widely used for stents which are fabricated by laser cutting.

Micromachining

As a micromachining method for TiNi SMA, laser cutting is practical because it is fast and allows more complex patterns [35]. To prevent deterioration due to heat generation by the laser, appropriate laser power and cutting speed should be selected. A femtosecond laser is effective to prevent heat generation, but the cost of the system is relatively high.

Etching

Oxide Film Removal

The surface of SMA materials tends to be oxidized during fabrication processes and annealing for shape memorization at high temperature. When conducting the SMA etching process, it is important to remove the oxide film on the SMA surface before etching because oxide film prevents uniform etching of the SMA substrate. Oxide

film on the TiNi alloy surface is not dissolved by a mixed solution of fluoric acid and nitric acid. However, the oxide film can be removed by lift-off as the result of TiNi substrate etching. Using an ultrasonic cleaner improves the uniform removal of the oxide film in chemical etchant because the oxide film can be removed promptly when the TiNi alloy substrate beneath the oxide film is etched. Oxide film removal is also important for complete electric contact with attached electrodes or lead wires.

Resist Selection for Chemical Etching

For patterning of TiNi alloys by chemical etching in a mixed solution of fluoric acid and nitric acid, an appropriate photoresist and baking process should be selected to obtain sufficient resistance to the etchant. Adhesion of photoresist to the SMA surface is also important. Poor adhesion causes a large under-cut, which is undesirable for accurate and fine patterning.

Electrochemical Etching (Through-Layer Etching, Resist Selection)

For through-layer patterning of TiNi alloys by electrochemical etching, the backside of the SMA layer should be protected by a conductive material layer such as Ni and Cu as mentioned in Section 6.2.4.1 to maintain uniform distribution of the electrolytic current during over-etching. The dummy layers of Ni and Cu can be removed selectively in concentrated nitric acid [40, 41].

Alcohol-based non-aqueous solutions such as H_2SO_4-methanol, LiCl-methanol, and LiCl-ethanol are useful as electrolyte solutions. Aqueous solutions are not suitable for electrochemical etching of TiNi alloys because the TiNi surface tends to be anodically oxidized during etching. A photoresist with resistance to alcohol-based solutions should be selected for the etching mask. Although many PMMA photoresists are solved in alcohol-based solutions, they are useful for the etching mask after hard baking at high temperature.

Assembly

For assembly, mechanical and adhesive fixations are simple and suitable for joining SMA to dissimilar materials. The disadvantages of mechanical fixation are a large connection area, impreciseness of length adjustment, low productivity because of the handmade process and susceptibility to fracturing in the fixation area. A disadvantage of adhesive is that it is time consuming because of the application of adhesive and the time required for curing.

Regarding the heating process for heat-curable adhesive, soldering or welding, the temperature limit and heating time in the assembly should be considered to prevent deterioration of the SME. As SMA deformed from its memorized shape tends to be restored to its memorized shape during the heating process, a certain fixation method of the SMA is required to prevent the restoration.

Oxide film on the surface of TiNi alloy should be removed to achieve uniformity of electroplating as well as sufficient solder wetting during soldering.

6.3 Applications and Devices

6.3.1 Medical

6.3.1.1 Stents

Treatment of stenosed (narrowed) lesions in the human body, for example, arterial blood vessels, using dilatation of an inflatable balloon at the tip of the catheter is an effective procedure called angioplasty.

Though the procedure is successfully performed, a high rate of restenosis occurs after 6–12 months because of neointimal growth of smooth muscle cells in the arterial blood vessels, formation of thrombi and recoiling of the vessel wall. Vascular stents, which are metal tubes with mesh-like wall, are widely used for preventing restenosis of treated blood vessels by mechanical expansion and scaffolding from inside the blood vessel after angioplasty. However, they do not reduce neointimal growth and there is still a risk of restenosis. Nonvascular stents are also used for biliary, gastrointestinal, pulmonary, and urologic stenting.

Self-expanding SMA stents (Fig. 6.19) are effective for supporting the vessel wall from inside the blood vessel and preventing migration of the stent [47]. Their transformation temperature is typically set to 30°C and the stent is superelastic at body temperature. To improve biocompatibility, for example nickel removal from the surface and corrosion resistance, electropolishing is occasionally performed. As fluoroscopic visibility of the TiNi is not sufficient, radiopaque markers made of titanium, gold or platinum-iridium are often attached to the end of the stent to facilitate placement.

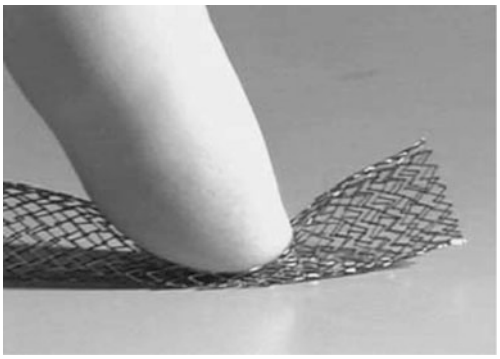

Fig. 6.19 Extreme deformation of a TiNi stent [47] (Reprinted with permission. Copyright 2004 Springer)

6.3.1.2 Endoscopes

Several flexible endoscopes are used in the esophagus, stomach, duodenum (gastrointestinal endoscopy), colon (colonoscopy), and ureter and kidney (ureteropyeloscopy). These endoscopes can be bent (deflected) by manipulation of wires from outside the human body.

To pass through the colon, which meanders with a small radius, a steerable endoscope with a diameter of 13 mm and incorporating SMA coil actuators has been developed. The SMA coil actuator contracts when heated by the application of an electrical current from outside the body. Consequently, contraction of the SMA coil bends the endoscope. The external diameter of the utilized SMA coil actuator is 1.0 mm and the diameter of its wire is 0.2 mm. Five bending segments are serially connected and controlled synchronously with an external servomotor which moves the endoscope back and forth from outside the body [56].

A steerable tip with a CMOS camera has also been developed using SMA coil actuators. The external diameter of the utilized SMA coil actuator is 0.7 mm and the diameter of its wire is 0.22 mm [57].

As shown in Fig. 6.20, a bending mechanism with a diameter of 15 mm has been developed for gastrointestinal application. This mechanism consists of a stack of elements with an SMA plate at the center of each element. When the SMA plates are actuated by the application of current, the whole structure bends in two directions like a vertebra of the human body [35].

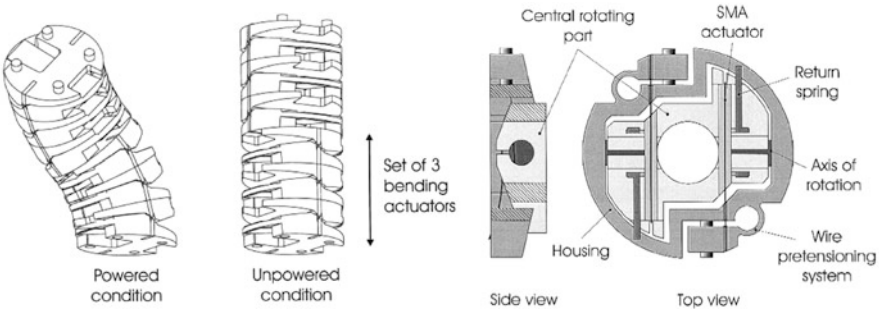

Fig. 6.20 Active bending stack mechanism using SMA plate actuators [35] (Reprinted with permission. Copyright 1999 Elsevier)

An active bending electric endoscope using SMA coil actuators with a CCD camera has been developed (Fig. 6.21). The external diameter of the fabricated endoscope is 5.5 mm, the external diameter of the utilized SMA coil actuator is 0.3 mm and the diameter of its wire is 0.075 mm [58].

6.3.1.3 Catheters

To inject contrast medium or medicine into the blood vessel or to measure blood pressure locally, a catheter, which is a hollow flexible small tube, is used. Catheter-based procedures (catheterization) enable doctors to access almost every diseased site which needs to be checked and treated via a blood vessel. Doctors control the tip of the catheter by moving its proximal part from outside of the body. Depending on blood vessel size, the catheters are approximately 0.3–3.0 mm in diameter and 1.5 m in length. As doctors must control the tip of the catheter from outside the body, operations with catheters require considerable skill, particularly when the blood vessel

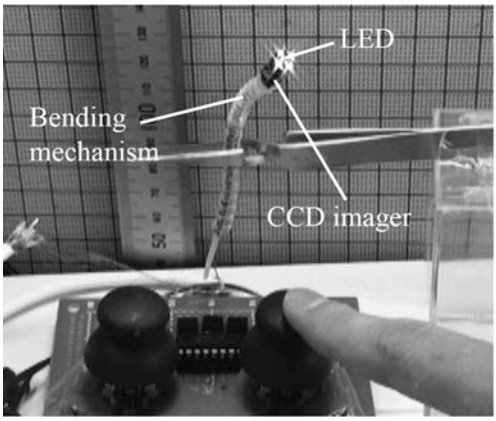

Fig. 6.21 Active bending electric endoscope using SMA coil actuators [58] (Reprinted with permission. Copyright 2000 The Institute of Electrical Engineers of Japan)

has a loop or complex configuration. Thus, there is a demand for an active catheter which moves like a snake in the blood vessel. Precise and safe manipulation of the catheter is realized if doctors can control the motion of the catheter from outside the body. As back-and-forth operation of the catheter from outside the body is relatively easy, a self-propelling mechanism is not necessarily demanded. Consequently, almost all controllable steering mechanisms are installed near the tip of the catheter. Active catheters which have micro-actuators at the tip have been developed for use in every part of the body. The tip can be controlled from outside the body and moves like a snake if many micro-actuators are distributed and properly controlled. Not only bending motion, but also torsional and precise back-and-forth motion are useful for manipulation of the tip of the catheter.

Plates or Sheets

An active catheter which has a bending mechanism realized by thin TiNi SMA plates has been developed [59, 60]. As shown in Fig. 6.22, one of the SMA plates fixed along the side of the catheter bends when the plate is heated by application of a current to restore its memorized shape. To realize precise control of bending motion by feedback control using temperature monitoring, a component which has heaters, temperature sensors and circuits on a flexible polyimide film substrate has been fabricated using MEMS technology [60]. The film components are fixed on the TiNi SMA plates placed on the sides of the catheter. To realize multi-directional bending, pairs of film components and SMA plates are fixed serially on alternating sides of the catheter. The external diameter of such a fabricated multi-joint catheter is 1 mm. The SMA plates utilized for this catheter are two directionally memorized SMAs, the shape of which is restored by cooling [60].

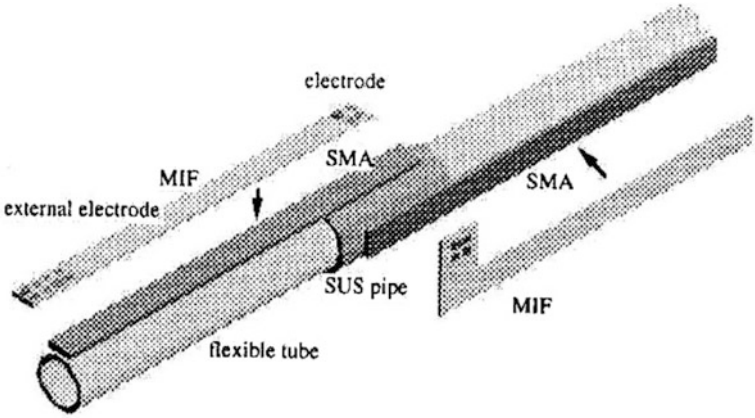

Fig. 6.22 Micro-manipulator with SMA bendable ribbons attached with MIF (Thin film heater and strain sensor) [60] (Reprinted with permission. Copyright 1996 SAGA)

Wire

Shape memory alloy wires are also utilized for active catheters as shown in Fig. 6.23 [42, 61–63]. When the SMA wires are embedded in the catheter eccentrically and heated above a certain transformation temperature by direct application of an electrical current to the SMA wire, the wire actuator bends the catheter by contraction of its length. The contraction length of the SMA wire, however, is relatively short and SMA wires fixed to the opposite side tend to restrict bending motion since the wires have to bend and stretch passively. Consequently, it is difficult to realize bending with a small radius of curvature.

Coil

Shape memory alloy micro-coil actuators are used to obtain a large bending motion and to realize multi-joint actuation as shown in Fig. 6.24. Shape memory alloy coils enable multi-directional bending with a large bending angle because the SMA coil actuators fixed at the opposite side can be passively extended. Shape memory alloy coil actuators can also be actuated by direct application of current when the wire diameter of the coil is small. Three SMA coil actuators, which are extended (from their memorized shapes) and fixed in the catheter, contract and bend in several directions. Multi-joint and multi-directional active catheters using silicon-glass link structures have been fabricated. Three SMA coil actuators are fixed between two silicon-glass link structures at intervals of 120°. Many joints are serially connected and each joint can bend in any direction. The external diameter of the fabricated catheter is 2.7 mm [44].

A major problem with active catheters which have many joints and functions is the necessity of an excessive number of lead wires to control each

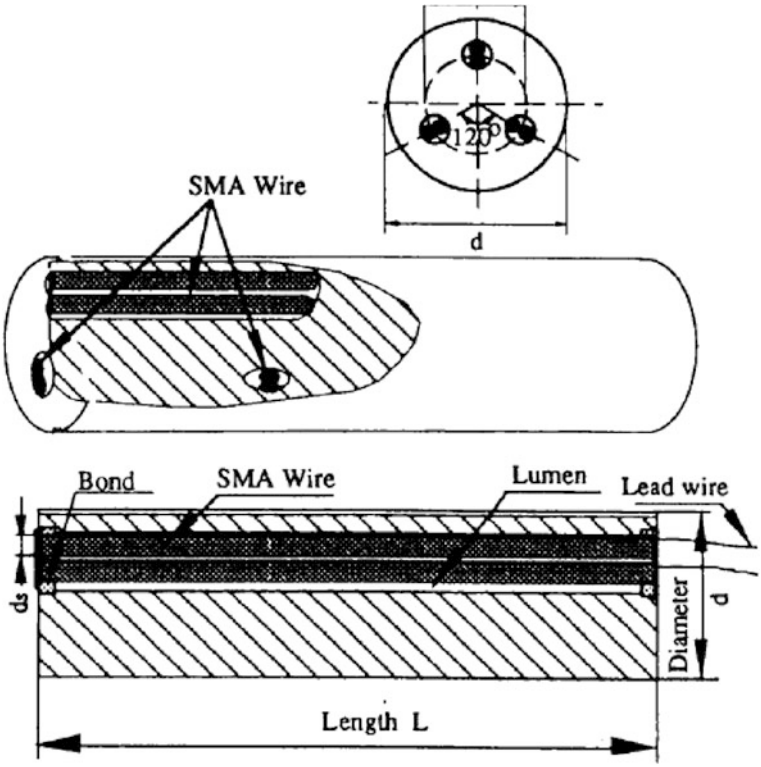

Fig. 6.23 Active bending catheter using SMA wires [62] (Reprinted with permission. Copyright © 1994 IEEE)

SMA actuator. To minimize the number of lead wires, flexible polyimide-based integrated complementary metal oxide semiconductor (CMOS) interface circuits for communication and control (C&C) have been developed and utilized in active catheters. To reduce the system size and simplify the assembly work, the C&C integrated circuit (IC) and three lead wires are fabricated on the same substrate using a CMOS-compatible polyimide-based process. The external diameter of the fabricated catheter without an outer tube is approximately 2.0 mm [64].

By locating SMA coil actuators inside the liner coil and fixing them to the liner coil directly, link structures can be eliminated and the liner coil can be used as a skeleton and a bias spring. Furthermore, every part works as a joint and hence bends more flexibly than that with links [65]. As the catheters for use in blood vessels are disposable to avoid blood infection, active catheters need to be fabricated at low cost. To solve this problem, batch assembly methods have been developed. One is silicon wafer-level batch fabrication with a silicon joint structure [66] and the other is fabrication using nickel electroplating and acrylic resin electrodeposition

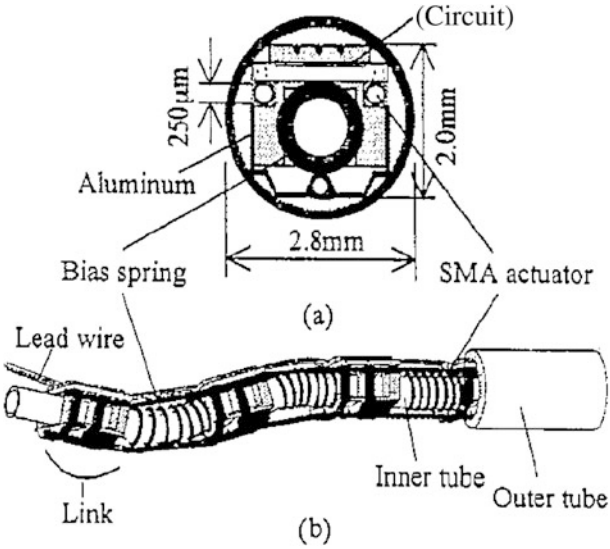

Fig. 6.24 Active bending catheter using SMA coils [44] (Reprinted with permission. Copyright 1996 Elsevier)

[67]. Fabrication using electroplating and deposition is carried out as follows. The SMA coil and metal spring are coated with polymer and the polymer is partially removed by laser ablation for partial exposure of the SMA surface and metal surface. UV curable acrylic resin is locally deposited by electroplating between the exposed SMA surface and the exposed metal surface. This novel method enables low cost batch assembly and a small external diameter.

Instead of a coil shape, flat meandering-shaped SMA actuators are also used for active catheters (Fig. 6.25). The flat shape meets both demands of small external diameter and large working channel by realizing a thin wall [68]. A batch fabrication method for flat meandering SMA actuators from an SMA (TiNi) sheet has been developed using electrochemical pulsed etching for active catheters [40]. Furthermore, to simplify the assembly process of the SMA actuators, three meandering actuators are formed in an SMA pipe using electrochemical pulsed etching. The SMA pipe is dip-coated with photoresist, which is then patterned using UV projection exposure and conventional development. This process is more suitable for mass production than laser cutting and electrodischarge machining.

Guide wires are wires which have a relatively flexible tip and are used for guidance of the catheter. An active bending guide wire has been fabricated using a flat meandering actuator (Fig. 6.26). The guide wire is bent by an electrical current supplied to the actuator because the actuator has a memorized curved shape [39].

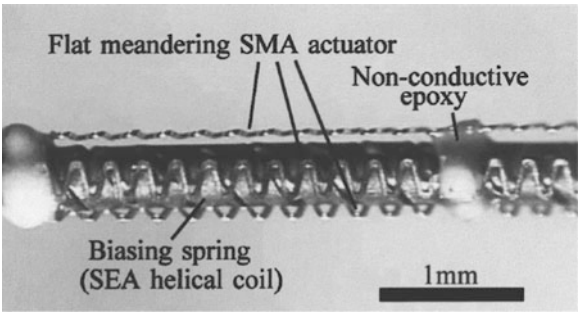

Fig. 6.25 Active bending catheter using flat meandering SMAs [40] (Reprinted with permission. Copyright 2000 Elsevier)

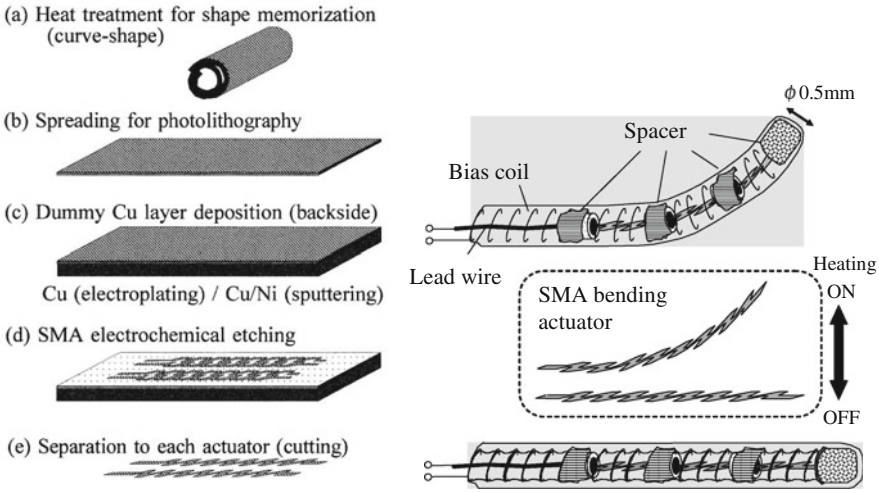

Fig. 6.26 Active guide wire using an SMA bending actuator [39] (Reprinted with permission. Copyright 2002 Elsevier)

6.3.1.4 Micro Clips and Grippers

Micro clips and grippers are typical applications of SMA micro actuators because the large deformation and large force generation of SMA material is well suited to these devices.

A micro gripper has been developed, as shown in Fig. 6.27 [1, 69].

The micro gripper consists of two micromachined (110) Si layers on which 5 μm thick TiNiCu film is sputtered. The two micromachined Si wafers are bonded by using an Au-Si eutectic bonding technique. The TiNiCu film has tensile thermal stress because it is deposited at 500°C. When the TiNiCu film is cooled, the gripper closes due to the relaxation of the thermal stress. The gripper jaws can open by shape recovery of the TiNiCu film when heated to 70°C. Opening and closing of the jaws can be repeated because the Si layer acts as a bias spring.

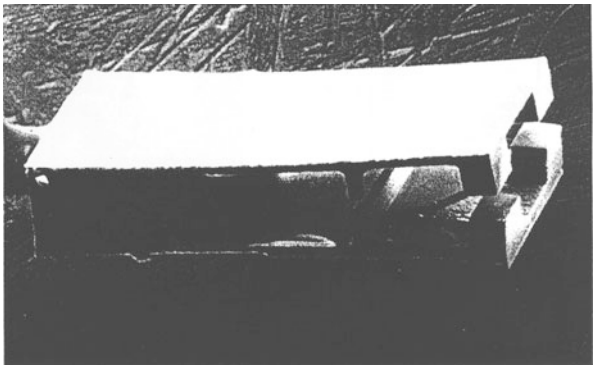

Fig. 6.27 Microgripper with sputtered TiNiCu film actuators [1] (Reprinted with permission. Copyright © 1996 IEEE)

Figure 6.28 shows a micro gripper developed by Kohl et al. [70]. The gripper mainly consists of two actuation units with a bonding pad, both of which are fabricated from a cold-rolled TiNi sheet with a thickness of 100 μm by laser cutting. Actuation unit 1 has a folded-beam structure for linear motion to close the gripping jaws. Actuation unit 2 has two circular beams. The gripper is mounted on a substrate in a pre-strained condition. By selective heating of actuation unit 1, the folded-beams recover their initial shape so that the link is pulled. Consequently, the circular beams are deformed and the gripping jaws are closed. By heating the circular beams selectively, the condition is reset, resulting in opening of the gripping jaws.

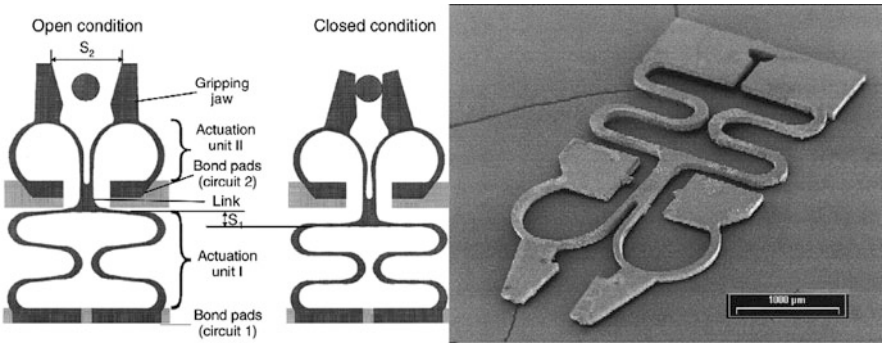

Fig. 6.28 Structure and operation principle of the SMA micro gripper [70] (Reprinted with permission. Copyright 2000 Elsevier)

Takeuchi and Shimoyama have developed an SMA micro electrode with a clipping structure for neural recording [71]. An SMA film (Ti-48 at.%Ni alloy film, 6 μm thick) is deposited by RF magnetron sputtering and patterned by HF-HNO_3

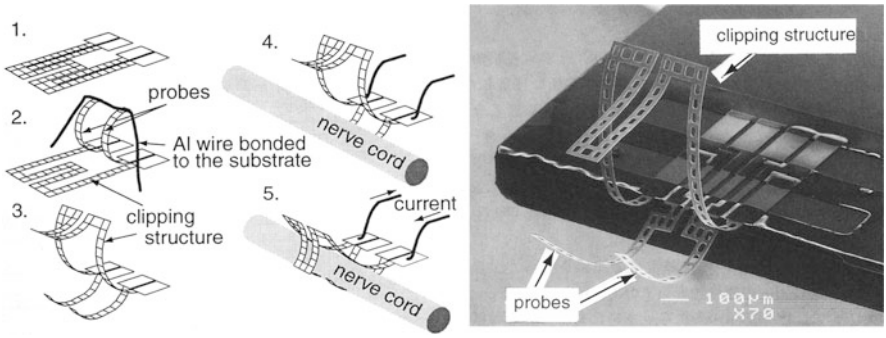

Fig. 6.29 Procedure for nerve clipping [71] (Reprinted with permission. Copyright © 1999 IEEE)

wet etching (Fig. 6.29(1)). Two beams are bent and clamped by an Al wire bonded to the substrate during heat treatment so that the curved shape is memorized (Fig. 6.29(2)). The upper and the lower beams are furthermore deformed by a micro manipulator at room temperature to form a hook structure (Fig. 6.29(3)). When the SMA arms are heated by an electric current directly for a very short time less than a second, the SMA arms recover the memorized shape, resulting in clipping of a nerve cord. The clipping force is enhanced by the 3-D structure. Consequently, the SMA clip-shaped electrode can clip a nerve cord tightly. Peak temperatures of martensitic and reverse martensitic transformation of the SMA film are 54 and 50°C, respectively. The nerve is not damaged by the thermal actuation of the SMA clip due to the short heating time. The electrical potential difference of the nerve of a living insect can be measured by using two SMA clips as electrodes.

Figure 6.30 shows a micro-vascular clip fabricated from an SMA film (11 μm thick) [72, 73]. The SMA clip is used for pulsation measurement of an artery sutured in micro-surgery to monitor obstruction of blood flow by thrombus formation. The holding mechanism consists of an outer arm and an inner cantilever to hold a blood vessel with a diameter of 1 mm. The SMA clip is fabricated from a flash-evaporated TiNiCu film with a memorized flat planar shape. Micro-heater circuits of platinum film are formed on the root and the halfway point on the outer arm with an insulator layer of polyimide film. The outer arm is bent at the root and the halfway point by external force before being attached to a blood vessel. When the SMA clip is heated at the root point locally, the outer arm closes due to deformation, resulting in the holding of a blood vessel between the outer arm and the cantilever. Thin film strain gauge circuits are also formed on the cantilever in the same platinum film layer to detect the periodical variation of the arterial pulsation. After use for pulsation monitoring, the SMA clip is heated at the halfway point so that the outer arm opens and releases the blood vessel safely. By local heating with the micro heaters, local actuation is realized, resulting in the multi-step motion.

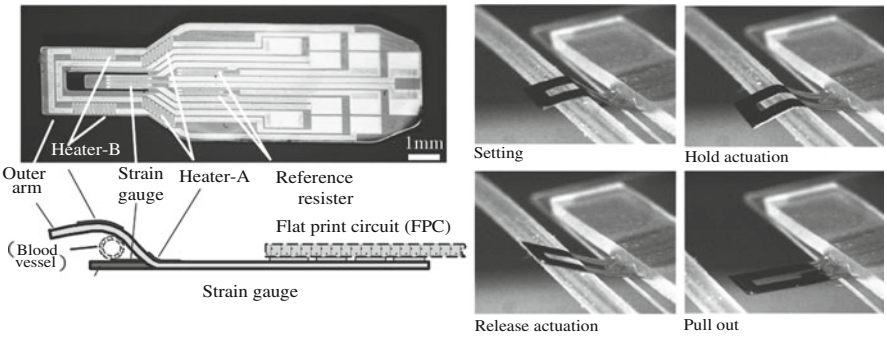

Fig. 6.30 Micro clip actuator with integrate micro heater and strain sensor [72, 73] (Reprinted with permission. Copyright 2006 Elsevier, 2008 Elsevier)

6.3.2 Fluidic Devices

Shape memory alloy has been applied for micro valves and micro pumps as a component for use in micro analysis systems. Johnson et al. have developed micro valves consisting of TiNi thin film ribbons and bulk-micromachined silicon springs [74, 75].

Kohl and his research group have been active in the development of SMA micro valves [76–79]. Shape memory alloy actuators micromachined from a TiNi thin plate (100 μm thick) by laser cutting have been used for several types of micro valves [76–78]. The operation principle, completed valve, and micromachined TiNi thin plate actuator are shown in Fig. 6.31. The micro valve is configured by an SMA actuator, a spacer and a polyimide membrane. The SMA actuator has multiple beams which can be directly heated by an electric current. In the normal condition of the unheated martensitic phase, the membrane is deflected by a pressure difference between the inlet and the outlet ports. By heating the SMA actuator above the phase transformation temperature, the flat shape is recovered and the valve is closed. The micromachined TiNi thin plate beams have a stress-optimized shape with homogeneous stress distribution. R-phase transformation of TiNi is used for the valve operation.

In addition to the micromachined SMA-thin-plate beam actuator, $Ti_{52}Ni_{48}$ and $Ti_{52}Ni_{20}Pd_{28}$ films (10 μm thick) deposited by DC-magnetron sputtering have also been used for a similar type of micro valves [79]. Figure 6.32 shows the sputtered TiNiPd thin film actuator for the micro valve. The TiNiPd film is patterned by electrochemical etching. Sharply defined edges and vertical sidewalls are obtained.

As shown in Fig. 6.33, a reciprocation micro pump with an TiNi actuator has been developed by Benart et al. [80]. To realize cyclic motion, the micro pump consists of two complementary TiNi actuators that are fabricated on silicon layers. The TiNi film is directly heated by an electrical current (0.9 A, 0.54 W). The two actuators are heated complementarily by out-of-phase currents to achieve cyclic motion.

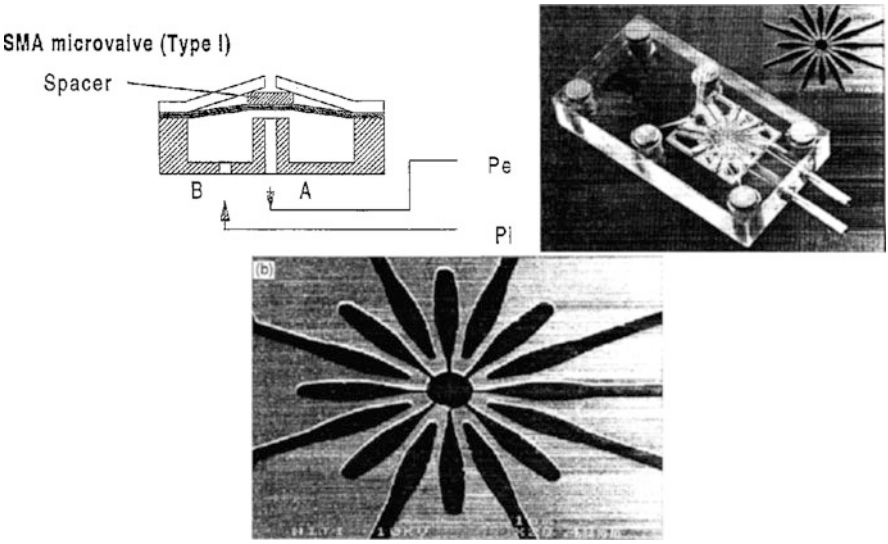

Fig. 6.31 Micro valve with stress optimized SMA actuator (micromachined SMA sheet type) [76] (Reprinted with permission. Copyright 1999 Elsevier)

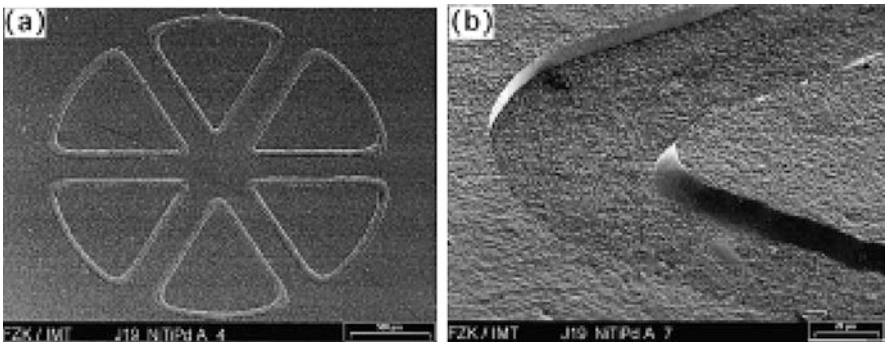

Fig. 6.32 Micro valve with SMA sputtered film [79] (Reprinted with permission. Copyright 2000 Elsevier)

Polyimide check valves are fabricated in stacked silicon layers to ensure unidirectional flow through the pump chamber. When the upper TiNi actuator is heated, the pump chamber is compressed, forcing liquid out through the right check valve (State 1); the pump chamber is expanded when the lower TiNi actuator is heated, drawing liquid in through the left check valve. The maximum pumping flow rate of water is 50 μL/min, at an excitation frequency of 0.9 Hz. At higher drive frequencies, the pumping flow rate decreases presumably due to the incomplete phase transformation of the TiNi material.

Figure 6.34 shows a micro pump which consists of two main parts, a flash-evaporated SMA film actuator and a silicon check valve [81, 82]. TiNi thin film

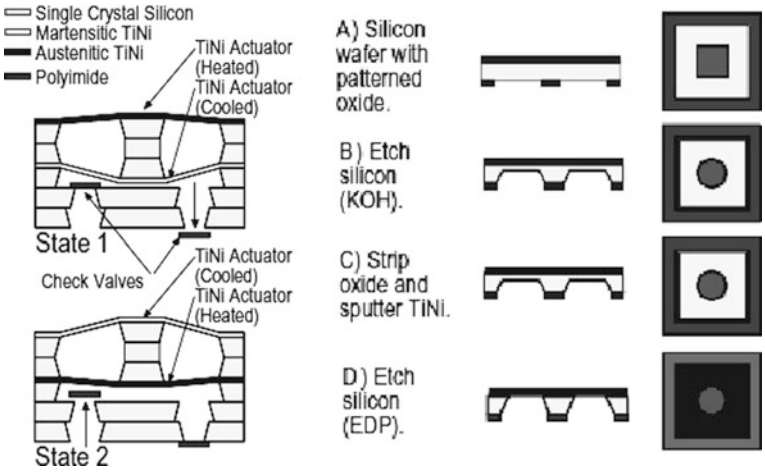

Fig. 6.33 Schematic structure and fabrication sequence of a reciprocation micro pump with two complementary TiNi actuators on silicon substrate [80] (Reprinted with permission. Copyright © 1997 IEEE)

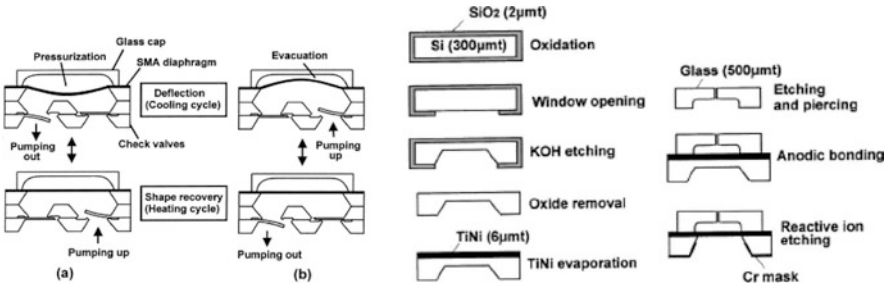

Fig. 6.34 Structure and fabrication process of micro pump with SMA film actuator [82] (Reprinted with permission. Copyright 2001 Elsevier)

with a thickness of about 6 μm was flash-evaporated onto a Si substrate, and its flat shape was memorized by heat treatment in a vacuum. A noteworthy process is the anodic bonding of the Pyrex glass cap to the TiNi film surface. Pyrex glass can be anodically bonded to TiNi film with applying DC voltage of 600 V at 300–400°C in a vacuum successfully. The micro pump is driven by thermal cycles of resistive heating and air-cooling under bias pressure applied by a nitrogen gas flow. The TiNi diaphragm of about 6 μm in thickness with a memorized flat shape is deformed when a bias pressure is applied to the chamber at room temperature. Then, when the diaphragm is directly heated up by an electric current, it recovers its initial flat shape. The check valve consists of an inlet port and an outlet port which open and close according to the movements of the TiNi diaphragm. It is easy to control the

pumping pressure by changing the bias pressure. The SMA micro pump gives a pumping rate of about 0.4 mL/cycle under a bias pressure of 100 kPa and at a back pressure of 0 kPa.

6.3.3 Optical Fiber Switch

Several optical fiber switches are widely used for telecommunication using an optical network. Mechanical 1×2 optical switches which adjust the optical axis of fibers by mechanical motion of a movable fiber have been developed using several micro actuators, including SMA actuators. The switches have advantages of low insertion loss and high cross-channel isolation because of the excellent optical property of optical fibers.

Using standard optical fibers, a mechanical 1×2 optical switch has been fabricated (Fig. 6.35) [31, 83]. A meandering SMA actuator for lateral displacement of a movable fiber has been fabricated by laser cutting of an SMA sheet. V-grooves for precise positioning of the movable fiber are fabricated by anisotropic etching of the Si substrate.

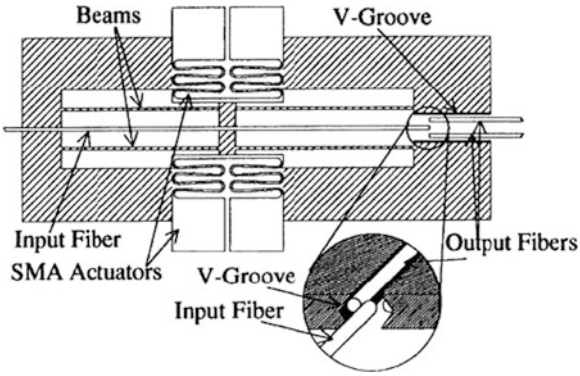

Fig. 6.35 Optical fiber switch using a flat meandering SMA actuator [31] (Reprinted with permission. Copyright 1999 The Institute of Electrical Engineers of Japan)

A mechanical 1×2 optical switch using plastic optical fibers (POF) with a relatively large core diameter have been developed (Fig. 6.36) [8]. A magnetic latch maintains the position of the movable POF on the left or right side at steady state. An SMA microcoil is fixed to a magnetic material ring and electrodes by soldering.

6.3.4 Tactile Pin Display

Tactile dynamic pin displays which depict graphic information or Braille points by bistable up-and-down motion of an array of pins to visually impaired or sightless people have been developed. The Braille points are varied arrangements of raised

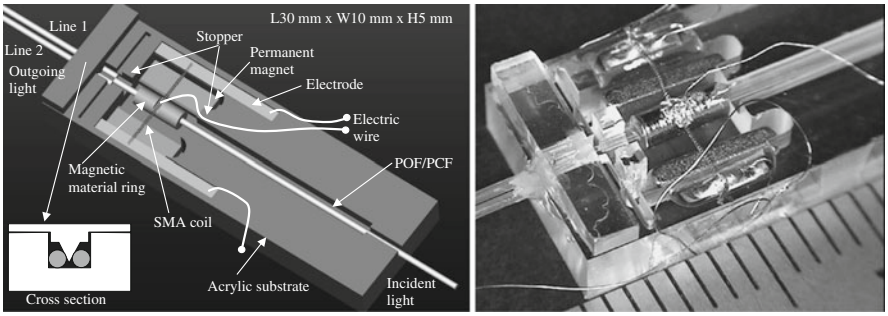

Fig. 6.36 Plastic optical fiber switch using an SMA coil actuator [91] (Reprinted with permission. Copyright © 2005 IEEE)

dots representing characters identified by touch. Generally, six raised points represent one character. An SMA actuator has advantages of noiseless actuation and a compact package with large displacement of SMA. As a disadvantage, the problem of heat generation and its accumulation caused by repeated motion and a high density of the pin array remains to be solved. Appropriate actuation of SMA should be considered for the required long service life.

Tactile pin displays using SMA wires and SMA coils have been fabricated. In the case of SMA wires, contraction of SMA wire moves individual pins and return force to restore the pin position is realized by a spring, as shown in Fig. 6.37 [84, 85] or by a rubber sheet on pin heads [86]. To improve heat dissipation, air cooling by a fan [85] or water cooling by circulation of water [86] are utilized. In the case of SMA coils, the return force to restore pin position is supplied by other SMA coils at a counter position as shown in Fig. 6.38 [8, 87]. To avoid heat accumulation, air cooling by a fan [87] or a magnetic latch mechanism (Fig. 6.38), which reduce heat generation, are utilized [8].

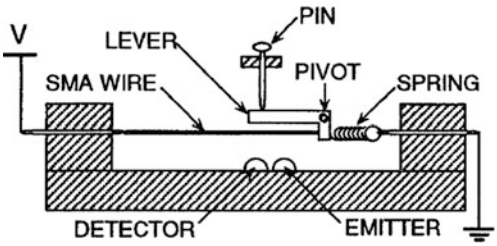

Fig. 6.37 Side view of one element of tactile display [84] (Reprinted with permission. Copyright © 1995 IEEE)

Design of a tactile pin display using an SMA sheet or plate has been proposed, and force and displacement of the actuator has been estimated. Return force to restore pin position is assumed to be served by a TiNi/SiO_2 bi-material beam

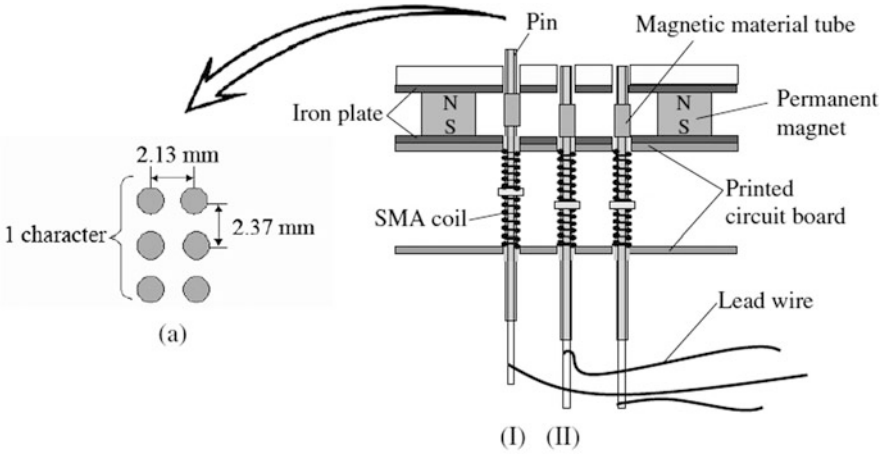

Fig. 6.38 (**a**) Braille character (Japanese standard) and (**b**) structure of dynamic Braille display [8] (Reprinted with permission. Copyright 2005 IOP)

structure [88]. Because of the large displacement of an SMA coil actuator, system size is expected to be sufficiently small for mobile use.

6.3.5 AFM Cantilever

Ti-Ni shape memory alloy sputtered film actuators have also been used for a single crystal silicon multi-probe devices for scanning probe nano-lithography [89]. The device has TiNi SMA film-actuated 8 × 8 writing probes with a cantilever (2 μm thick) and an Au film-coated tip (8 μm in height). The cantilevers and the tips are fabricated from a silicon-on-insulator (SOI) wafer consisting of a 10 μm-thick device layer and a 1 μm thick buried-oxide (BOX) layer. The TiNi SMA film is deposited by DC magnetron sputtering on the cantilever. To control the film composition, several pure Ti blocks are placed on the erosion area of a Ti-50 at%Ni alloy disk target. The sputtered TiNi film (Ni-50.2 at.%Ti) is annealed at 450°C for 1 h in a high vacuum for crystallization. After patterning the Ti-Ni film with a mixed solution of HF and HNO_3, Au film lines are formed as lead wires for direct heating of the Ti-Ni film. A polyimide film is deposited as an interlayer insulator in a cross wiring section. A thick silicon substrate layer is etched by deep reactive ion etching (DRIE) followed by removal of the remaining BOX layer from the backside. Each cantilever is deflected to the lower side due to the compressive intrinsic stress of the BOX layer, as shown in Fig. 6.39. When the SMA actuator is heated above the phase transformation temperature, it recovers the memorized flat shape as shown in Fig. 6.40. The SMA actuation mechanism yields a contact or non-contact state between the probe-tip and sample surface.

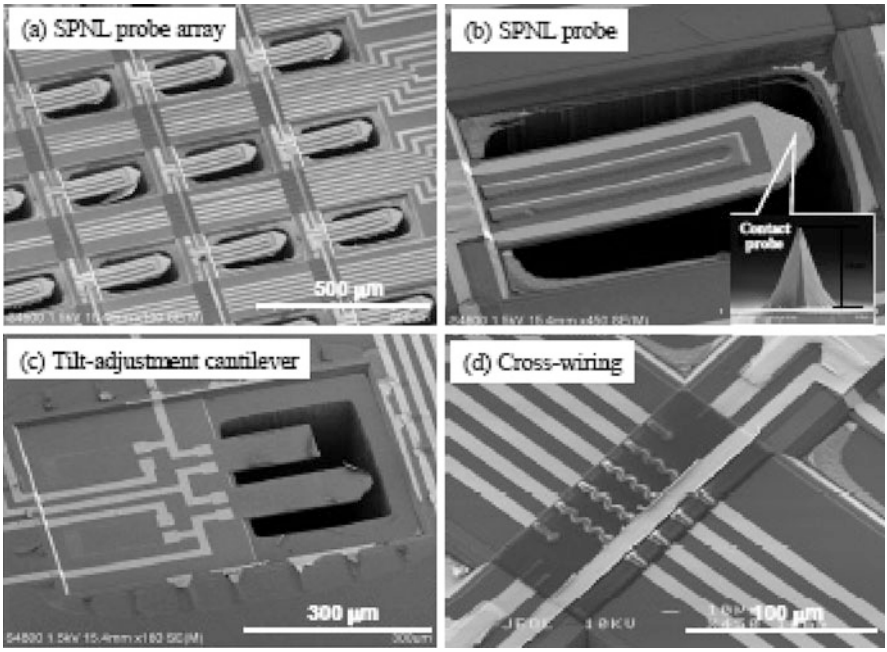

Fig. 6.39 SEM images of scanning probe nano-lithography device using Ti-Ni SMA film actuator on a silicon cantilever [89] (Reprinted with permission. Copyright © 2007 IEEE)

6.3.6 Case Studies and Lessons Learned

6.3.6.1 Designs

Shape Memory

As mentioned in Section 6.1 (Principle), "one-way shape recovery" SMA can be deformed only once. When one-way SMA is used for repeated actuation, an elastic bias spring should be added to deform the SMA [2, 7]. The two-way shape memory effect can also be realized in TiNi alloys, by which the two-way TiNi alloy actuator can be repeatedly deformed by heating and cooling without a bias mechanism [4]. Shape recovery force generated by two-way effect is much less than that of one-way type SMA. A particular "all-round type effect", which is a type of two-way effect, can also be obtained in Ni-rich TiNi alloys after aging with the shape constrained. However, it shows large thermal hysteresis at the deformation temperature.

Maximum Strain and Reversible Cycles

For SMA actuators to be used repeatedly, they should be designed with considering a fatigue as mentioned in Section 6.2.6 (Materials and Processes Selection Guidance).

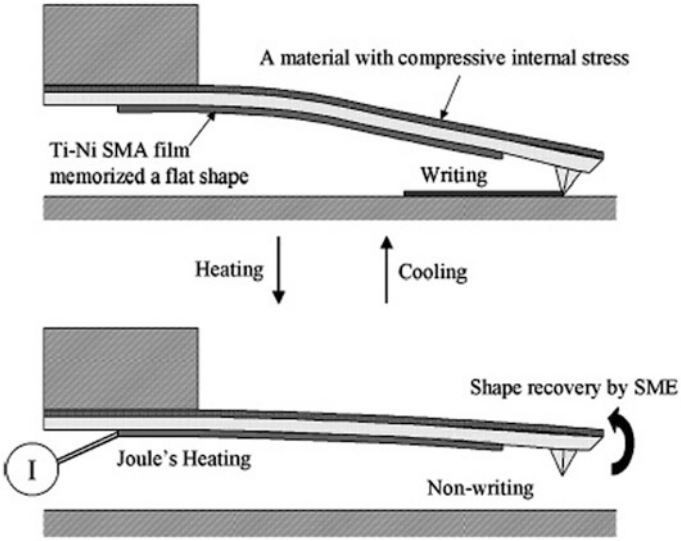

Fig. 6.40 Schematic of the actuation mechanism of cantilever of a scanning nano-lithography probe with an Ti-Ni SMA film actuator [89] (Reprinted with permission. Copyright © 2007 IEEE)

It should be noted that the limit of reversible cycles of actuation strongly depends on the maximum strain or maximum stress [49].

Latch Mechanism

In the case of bistable repeated motion, a latch mechanism is effective for low power consumption and long service life by avoiding unnecessary SMA actuation at steady state. Magnetic latch mechanisms utilize the magnetic attraction force between magnetic material and a permanent magnet. Using SMA coils and a magnetic latch mechanism, a tactile pin display [8] and an optical switch [90] have been fabricated. A bistable actuator using SMA beams and the magnetic latch mechanism has been developed for large contact force and large stroke with low power consumption [91].

6.3.6.2 Heating and Cooling

Large scale bulk SMA actuators tend to have a slow response due to the large heat capacity of the actuator itself, which results in lengthy heating and cooling cycles. As mentioned in Section 6.1.1 (Basic principle), an SMA actuator can be rapidly deformed when it is miniaturized so as to reduce its heat capacity. An SMA micro actuator can be heated above its phase transformation temperature rapidly by small thermal energy and can be rapidly cooled down by ambient air without the addition of a cooling mechanism.

Direct Heating

TiNi SMA can be actuated by Joule heat created by direct flow of an electrical current into the SMA when electrical resistance of the SMA is relatively high. The advantage of the actuation method is its simple structure without any heater or cooler. Disadvantages of direct heating are the requirement of high electrical resistance and electrical connections with low electrical resistance between the SMA and dissimilar conductive material.

Relatively high electrical resistance of SMA is required to avoid a high electrical current for actuating the SMA. Though the small or thin structure of SMA has high electrical resistance, it cannot generate high power. An array of small or thin SMA structures connected as a series circuit can solve this problem, but the structure is relatively complex.

Electrical connections with low electrical resistance between SMA and dissimilar conductive material, for example, copper as electrical lead wires, is required to avoid undesirable consumption of electrical current for heat generation at the connection. In the case of bulk SMA, assembly methods suitable for making electrical connection and for joining the SMA to dissimilar material are required, for example, mechanical fixation, conductive adhesive, soldering and welding. In the case of thin film or plate SMA, it is relatively easy to form a low resistance connection by coating a conductive metal layer on the SMA or coating an SMA layer on the conductive metal layer.

Indirect Heating

Indirect heating of an SMA actuator by additional heater lines with high resistance is advantageous for reducing the electric power needed for actuation. To realize indirect heating, it is necessary to select an appropriate mechanical design and fabrication processes of the heater and insulator so that they can deform without fracture during the SMA actuation. Figure 6.41 is a close-up view of the SMA clip actuator mentioned above [72, 73]. Micro heaters of Pt thin film (100 nm thick) are formed on an SMA thick film actuator with a polyimide insulator film (2 μm thick).

Figure 6.42 shows an indirect heating SMA coil actuator [92]. A thin Ni film (0.6 μm) on a Parylene-coated SMA coil is used as an indirect heater. The Parylene layer (1 μm thick) is an insulator between the Ni layer and the SMA surface. Parylene can be deposited uniformly in a vacuum on the entire surface of the SMA coil. A thin Ni heater layer is formed by electroless plating on the Parylene. No damage is observed in the Ni or Parylene films after 3000 cycles of prolonged experiments with applied power of 80 mW at 2% strain of SMA coil.

Control

Improvement of Displacement Accuracy

One of the disadvantages of SMA is low accuracy of displacement because of unstable heat radiation to the circumference, for example, air or solid material.

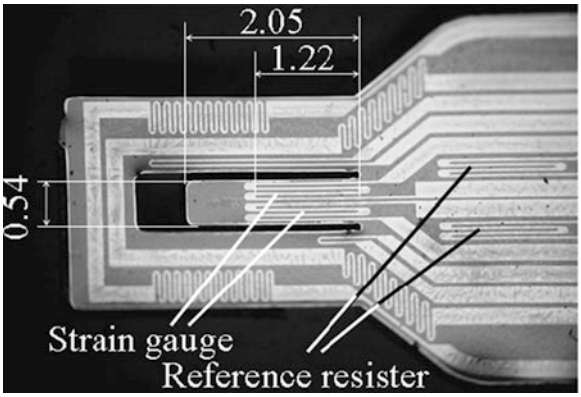

Fig. 6.41 Micro SMA clip with thin film heater lines for indirect heating [72, 73] (Reprinted with permission. Copyright 2008 Elsevier)

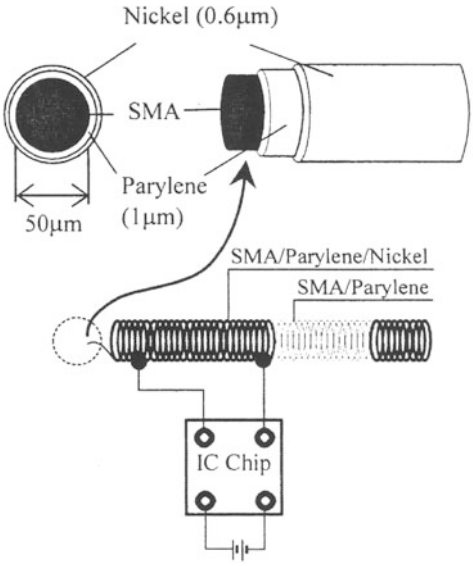

Fig. 6.42 Indirect heating SMA coil actuator [92] (Reprinted with permission. Copyright 1996 Cambridge University Press)

Additional feedback control systems are effective for improvement of the displacement accuracy. The temperature of SMA [56] or the strain of heated SMA [48] are estimated by measuring its electrical resistance. Figure 6.21 shows a micro manipulator which has SMA ribbons with a thin film strain sensor and a heater for multi-directional bending motion [60]. A Ti/Pt resister pattern on the SMA plate can measure temperature and displacement of SMA separately because the two materials have different gauge factors and temperature coefficients, as shown in Fig. 6.43 [60].

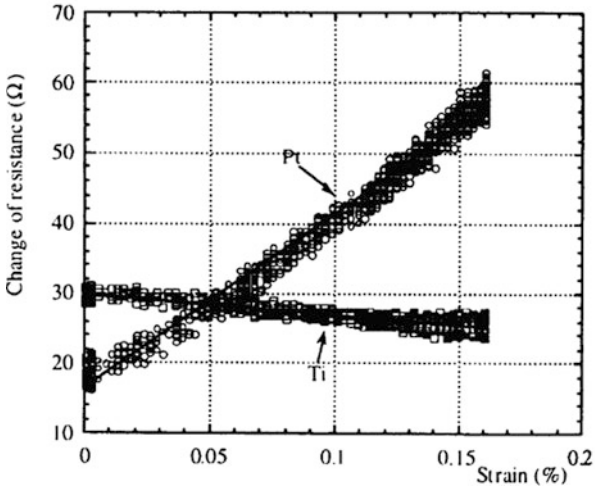

Fig. 6.43 Relation of strain and change of resistance [60] (Reprinted with permission. Copyright 1996 SAGA)

6.4 Summary

SMA materials, particularly TiNi-based alloys, have excellent mechanical properties for actuators, such as large force generation and large deformation. As introduced in this chapter, many techniques for the preparations of bulk and thin film SMA materials, micromachining and etching processes, and assembly processes have been developed by many researchers since the 1990s.

In particular, techniques for the deposition of thin film SMA have been remarkably developed. Shape memory alloy thin films with mechanical properties similar to those of bulk SMAs have been realized. Several assembly techniques, for example, mechanical fixation, adhesion, welding, and soldering have been developed and used as practical applications. Technical progress has resulted in the development of many SMA micro devices. SMA micro actuators have some disadvantages such as low displacement controllability. However, integration with other MEMS technologies, for example, micro thermal and position sensors, micro heaters, bias spring mechanism, and latch mechanism, can overcome the disadvantages of SMA actuators. Shape memory alloy actuator technologies will continue to evolve in integrated MEMS systems.

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References

1. P. Krulevitch, A.P. Lee, P.B. Ramsey, J.C. Trevino, J. Hamilton, M.A. Northrup: Thin film shape memory alloy microactuators, J. Microelectromech. Syst. 5(4), 270–281 (1996)
2. K. Otsuka C.M. Wayman: Shape Memory Materials (Cambridge University Press, Cambridge, 1998)
3. J.A. Walker, K.J. Gabriel: Thin-film processing of TiNi shape memory alloy, Sens. Actuators, A21–A23, 243–246 (1990)
4. K. Kuribayashi, M. Yoshitake, S. Ogawa: Reversible SMA Actuator for Micron Sized Robot, Proceedings of the IEEE Micro Electro Mechanical Systems. MEMS, pp. 217–221 (Napa Valley, CA, USA, 1990)
5. A.D. Johnson: Vacuum-deposited TiNi shape memory film: Characterization and applications in microdevices, J. Micromech. Microeng. 34–41 (1991)
6. S. Miyazaki, A. Ishida: Martensitic transformation and shape memory behavior in sputter-deposited TiNi-base thin films, Mater. Sci. Eng. A 273–275, 106–133 (1999)
7. M. Kohl: Shape Memory Microactuator (Springer, New York, NY, 2004)
8. Y. Haga, M. Mizushima, T. Matsunaga, M. Esashi: Medical and welfare applications of shape memory alloy microcoil actuators, Smart Mater. Struct. 14(5), S266–S272 (2005)
9. W.C. Crone, A.N. Yahya, J.H. Perepezko: Bulk shape memory NiTi with refined grain size synthesized by mechanical alloying, Mater. Sci. Forum 386–388, 597–602 (2002)
10. D. Tomus, K. Tsuchiya, T. Nagano, A. Hosokawa, T. Ohmori, M. Sasaki, Y. Todaka, M. Umemoto: Influence of heat treatment on phase transformation of Ni-rich TiNi foils produced via ultrafine laminates, Mater. Trans. 45(2), 219–224 (2004)
11. N. Miyano, K. Tagaya, K. Kawase, K. Ameyama, S. Sugiyama: Fabrication of alloy and ceramic microstructures by LIGA-MA-SPS process, Sens. Actuators A, 108(1–3), 250–257 (2003)
12. J.D. Busch, A.D. Johonson: A shape-memory properties in Ni-Ti sputter-deposited film, J. Appl. Phys. 68(12), 6224–6228 (1990)
13. A. Ishida, S. Miyazaki: Microstructure and mechanical properties of sputter-deposited Ti-Ni alloy thin films, J. Eng. Mater. Technol. 121, 3–8 (2004)
14. Y. Nakamura, S. Nakamura, L. Buchaillot, M. Ataka, H. Fujita: Tow thin film shape memory alloy microactuators, Trans. IEE Jpn. 117-E(11), 554–559 (1997)
15. S. Miyazaki, K. Nomura: Development of Perfect Shape Memory Effect in Sputter-Deposited Ti-Ni Thin Films, Proceedings of the IEEE Micro Electro Mechanical Systems (MEMS-94), Oiso, Japan, pp. 176–181 (1994)
16. S. Miyazaki, K. Nomura, A. Ishida, S. Kajiwara: J. Physique IV France 7, Colloque C5, supplement au J. Phys. III, C5-275–280 (1997)
17. A. Ishida, A. Takei, M. Sato, S. Miyazaki: Shape Memory Behavior of Ti-Ni Thin Films Annealed at Various Temperatures, Materials Research Society Symposium, Proceedings, Vol. 360, pp. 381–386 (1995)
18. A. Ishida, A. Takei, S. Miyazaki: Shape memory thin film of Ti-Ni formed by sputtering, Thin Solid Films 228, 210–214 (1993)
19. P. Krulevitch, P.B. Ramsey, D.M. Makowiecki, A.P. Lee, M.A. Northrup, G.C. Johnson: Mixed-sputter deposition of Ni-Ti-Cu shape memory films, Thin Solid Films 274, 101–105 (1996)
20. A. Ohta, S. Bhansali, I. Kishimoto, A. Umeda: Novel fabrication technique of TiNi shape memory alloy film using separate Ti and Ni targets, Sens. Actuators 86, 165–170 (2000)
21. E. Makino, M. Uenoyama, T. Shibata: Flash evaporation of TiNi shape memory thin film for microactuators, Sens. Actuators A71, 187–192 (1998)
22. T. Mineta, K. Hirota, E. Makino, T. Sugawara, S. Toh, T. Shibata: Shape memory thin film for blood vessel holding actuator of thrombus detector, Key Eng. Mater. 297–300, 244–249 (2005)

23. T. Mineta, K. Kasai, Y. Sasaki, E. Makino, T. Kawashima, T. Shibata: Flash-Evaporated TiNiCu thick film for shape memory alloy micro actuator, Microelectron. Eng. 86, 1274–1277 (2009)
24. K. Ikuta, M. Hayashi, T. Matsuura: Shape Memory Alloy Thin Film Fabricated by Laser Abration, Proceedings of the IEEE Micro Electro Mechanical System, pp. 355–360 (Oiso, Japan, 1994)
25. Y. Furuya, M. Matsumoto, H. Kimura, K. Aoki, T. Masumoto: Thermo-mechanical phase transformation of rapidly quenched Ti-Ni-Cu ribbons, Mater. Trans. JIM, 31(6), 504–508 (1990)
26. T. Mineta, M. Abe, H. Kubo, E. Makino, T. Shibata: Fabrication of TiNi 3D Micro Structures from Evaporated Thin Film Tube, Asia-Pacific Conference of Transducers and Micro-Nano Technology, pp. 322–325 (APCOT-MNT 2004 Sapporo, Japan, 2004)
27. P. John, S. Buenconsejo, K. Ito, H.Y. Kim, S. Miyazaki: High-strength superelastic Ti-Ni microtubes fabricated by sputter deposition, Acta Mater. 56(9), 2063–2072 (2008)
28. M. Komatsubara, T. Namazu, H. Nagasawa, T. Tsurui, S. Inoue: Cylindrical film deposition system for three-dimensional titanium–nickel shape memory alloy microstructure, Vacuum 83, 703–707 (2009)
29. K. Weinerta V. Petzoldt: Machining NiTi micro-parts by micro-milling, Mater. Sci. Eng. A 481–482, 672–675 (2008)
30. Y. Shida, Y. Sugimoto: Water jet erosion behaviour of Ti-Ni binary alloys, Wear 146(2), 219–228 (1991)
31. K. Hara, K. Hane, M. Sasaki, M. Kohl: Si Micromechanical Fiber-Optic Switch with Shape Memory Alloy Microactuator, Proceedings of the Solid-State Sensors and Actuators (Transducers'99), pp. 790–793 (Sendai, Japan, 1999)
32. H.C. Lin, K.M. Lin Y.C. Chen: The laser machining characteristics of TiNi shape memory alloys, High Temp. Mater. Process. 3(4), 409–420 (1999)
33. C. Li, S. Nikumb, F. Wong: An optimal process of femtosecond laser cutting of NiTi shape memory alloy for fabrication of miniature devices, Opt. Lasers Eng. 44(10), 1078–1087 (2006)
34. H.C. Lin, K.M. Lin, I.S. Cheng: The electro-discharge machining characteristics of TiNi shape memory alloys, J. Mater. Sci. 36(2), 399–404 (2001)
35. D. Reynaerts, J. Peirs, H.V. Brussel: Shape memory micro-actuation for a gastro-intestinal intervention system, Sens. Actuators A 77(2), 157–166 (1999)
36. S. Nakamura, Y. Nakamura, M. Ataka, H. Fujita: A study on patterning method of TiNi shape memory thin film, Trans. IEE Jpn. 117-E(1), 27–32 (1997)
37. D.M. Allen, T.T. Chen: The Electrochemical micromachining of microactuator devices from sputtered NiTi thin film, Electrochem. Soc. Proc. 97–95, 72–78 (1997)
38. M. Kohl, E. Quandt, A. SchBler, R. Trapp, D.M. Allen: Characterization of NiTi Shape Memory Microdevices Produced by Microstructuring of Etched Sheets or Sputter Deposited Films, Proceedings of 4th New Actuators (Actuator'94), Bremen, Germany, pp. 317–320 (1994)
39. T. Mineta, T. Mitsui, Y. Watanabe, S. Kobayashi, Y. Haga M. Esashi: An active guide wire with shape memory alloy bending actuator fabricated by room temperature process, Sens. Actuators A, 97–98C, 632–637 (2002)
40. T. Mineta, T. Mitsui, Y. Watanabe, S. Kobayashi, Y. Haga, M. Eshi: Batch fabricated flat meandering shape memory alloy actuator for active catheter, Sens. Actuators A, 88, 112–120 (2000)
41. T. Mineta: Electrochemical etching of NiTi shape memory alloy sheet using new electrolyte solutions, J. Micromech. Microeng. 14, 76–80 (2004)
42. T. Mineta, Y. Haga, M. Esashi: Electrochemical Etching of Shape Memory Alloy Using New Electrolyte Solutions, Proceedings of 15th IEEE International Micro Electro Mechanical Systems Conference (MEMS2002), pp. 376–379 (Las Vegas, NV, USA, 2002)

43. S. Ballandras, M. Calin, S. Zissi, A. Bertsch, J.C. Andre, D. Hauden: Microstereophotolithography and shape memory alloy for the fabrication of miniaturized actuators, Sens. Actuators A, 62, 741–747 (1997)
44. G. Lim, K. Park, M. Sugihara, K. Minami, M. Esashi: Future of active catheters, Sens. Actuators, A 56, 113–121 (1996)
45. N.A. Smith, G.G. Antoun, A.B. Ellis, W.C. Crone: Improved adhesion between nickel.titanium shape memory alloy and a polymer matrix via silane coupling agents, Composites A, 35, 1307–1312 (2004)
46. A. Hirose, M. Uchihara, T. Aeraki, K. Honda, M. Kondoh: Laser welding of Ti-Ni type shape memory alloy, J. Jpn. Instrum. Metals 54(3), 262–269 (in Japanese, 1990)
47. D. Stoeckel, A. Pelton, T. Duerig: Self-expanding nitinol stents: Material and design considerations, Eur. Radiol. 14(2), 292–301 (2004)
48. D. Homma, S. Uemura, F. Nakazawa: Functional Anisotropic Shape Memory Alloy Fiber and Differential Servo Actuator, Proceedings of the International Conference on Shape Memory and Superelastic Technologies, Tsukuba, pp. 463–472 (2007)
49. D. Stockel: Status and Trends in Shape Memory Technology, Proceedings of Actuators'92, pp.79–84 (Bremen, Germany, 1992)
50. T.W. Duering, K.N. Melton, D. Stockel, C.M. Wayman: Engineering Aspects of Shape Memory Alloys (Butterworth-Heinemann, London, 1990)
51. S. Miyazaki, K. Otsuka: Deformation and transition behavior associated with the r-phase in Ti-Ni alloys, Metal Trans. A 17A, 53–63 (1986)
52. S. Miyazaki, T. Hashinaga, A. Ishida: Thin Solid Films 364, 281–282 (1996)
53. T.H. Nam, T. Saburi, K. Shimizu: Cu-Content Dependence of Shape Memory Characteristics in Ti-Ni-Cu Alloys, Mater. Trans. JIM, 31, pp. 959–967 (1990)
54. H.C. Lin, K.M. Lin, S.K. Chang, C.S. Lin: A study of TiNiV ternary shape memory alloys, J. Alloys Compounds 284(1–2), 213–217 (1999)
55. E. Takahashi, T. Sakurai, S. Watanabe, N. Masahashi, S. Hanada: Effect of heat treatment and sn content on superelasticity in biocompatible TiNbSb alloys, Mater. Trans. 43, 2978–2983 (2002)
56. K. Ikuta, M. Tsukamoto, S. Hirose: Shape Memory Alloy Servo Actuator System with Electric Resistance Feedback and Application for Active Endoscope, Proceedings of the IEEE International Conference on Robotics and Automation, pp. 427–430 (Leuven, Belgium, 1998)
57. A. Menciassi, J.H. Park, S. Lee, S. Gorini, P. Dario, J.O. Park: Robotic Solutions and Mechanisms for a Semi-autonomous Endoscope, Proceedings of the 2002 IEEE/RSJ International Conference on Intelligent Robots and System, Vol. 2, pp. 1379–1384 (Lausanne, Switzerland, 2002)
58. W. Makishi, T. Matsunaga, M. Esashi, Y. Haga: Active bending electric endoscope using shape memory alloy coil actuators, Trans. IEE Jpn. 127-E(2), 75–81 (in Japanese, 2000)
59. W.C. McCoy: U.S. Patent 4 543 090 (1985)
60. S. Kaneko, S. Aramaki, K. Arai, Y. Takahashi, H. Adachi, K. Yanagisawa: Multi-Freedom Tube Type Manipulator with SMA Plate, Proceedings of the International Symposium on Microsystems, Intelligent Materials and Robots, Sendai, Japan, pp. 87–90 (1995)
61. P.W. Bremer: U.S. Patent 4 753 223 (1988)
62. T. Fukuda, S. Guo, K. Kosuge, F. Arai, M. Negoro, K. Nakabayashi: Micro Active Catheter System with Multi Degrees of Freedom, Proceedings of 1994 IEEE International Conference on Robotics and Automation, San Diego, pp. 2290–2295 (1994)
63. H. Takizawa, H. Tosaka, R. Ohta, S. Kaneko, Y. Ueda: Development of a Microfine Active Bending Catheter Equipped with MIF Tactile Sensors, Twelfth IEEE International Conference on Micro Electro Mechanical Systems (MEMS'99), Orlando, pp. 412–417 (1999)
64. K. Park, K. Minami, M. Esashi: An integrated communication and control system for a multi-link active catheter, J. Micromech. Microeng. 6, 345–351 (1996)
65. Y. Haga, Y. Tanahashi, M. Esashi: Small Diameter Active Catheter Using Shape Memory Alloy, MEMS 98 Proceedings of the IEEE International Workshop on Micro Electro Mechanical Systems, pp. 419–424 (Heidelberg, Germany, 1998)

66. T. Mineta, Y. Watanabe, S. Kobayashi, Y. Haga, M. Esashi: Active catheter using multi-link-joint structure fabricated in silicon wafer, Trans. IEE Jpn. 119-E(12), 615–619 (1999)
67. Y. Haga, S. Maeda, M. Esashi: Bending, Torsional and Extending Active Catheter Assembled Using Electroplating, Proceedings of IEEE International Micro Electro Mechanical Systems Conference (MEMS 2000), Miyazaki, pp. 181–186 (2000)
68. A. Lim, S. Lee: Thin Tube-type Bending Actuator Using Planar S-shaped Shape Memory Alloy Springs, Technical Digest of the 10th International Conference Solid-State Sensors and Actuators (Transducers'99), Sendai, Vol. 2, pp. 1894–1895 (1999)
69. A.P. Lee, D.R. Ciarlo, P.A. Krulevitch, S. Lehew, J. Trevino, M.A. Northrup: A Practical microgripper by fine alignment, eutectic bonding, and SMA actuation, Sens. Actuators A 54, 755–759 (1996)
70. M. kohl, E. Just, W. Pflenging, S. Miyazaki: SMA microgripper with integrated antagonism, Sens. Actuators A83, 208–213 (2000)
71. S. Takeuchi, I. Shimoyama: A three-dimensional shape memory alloy microelectrode with clipping structure for insect neural recording, J. Microelectromech. Syst. 9(1), 24–31 (Mar, 2000)
72. T. Sugawara, K. Hirota, M. Watanabe, T. Mineta, E. Makino, S. Toh, T. Shibata: Shape memory thin film actuator for holding a fine blood vessel, Sens. Actuators A 130–131, 461–467 (2006)
73. T. Mineta, N. Kida, S. Nomura, E. Makino, T. Sugawara, S. Toh, T. Shibata: Pulsation sensor integrated with microvascular holding actuator for thrombosis monitoring, Sens. Actuators A 143(1), 14–19 (2008)
74. J.D. Busch, A.D. Johnson: Prototype Microvalve Actuator, Proceedings of MEMS'90 (Napa Valley, CA, USA, 1990)
75. C.A. Ray, C.L. Sloan, A.D. Johnson, J.D. Busch, B.R. Petty: A silicon-based shape memory alloy microvalve, Mater. Res. Sot. Symp. Proc. 276, 161–166 (1992)
76. M. Kohl, K.D. Skrobanek, S. Miyazaki: Development of Stress-optimized Shape Memory Microvalves, Sensors and Actuators A72, 243–250 (1997)
77. K.D. Skrobanek, M. Kohl, S. Miyazaki: Stress-optimized Shape Memory Microvalves, Proceedings of the MEMS'97, pp. 256–261 (1997)
78. M. Kohl, E. Just, A. Strojek, K.D. Skrobanek, W. Pfleging, S. Miyazaki: Shape Memory Microvalves for High Pressure Applications, Proceedings of Actuators'98, pp. 473–477 (Bremen, Germany, 1998)
79. M. Kohl, D. Dittmann, E. Quandt, B. Winzek: Thin film shape memory microvalves with adjustable operation temperature, Sens. Actuators A83, 214–219 (2000)
80. W.L. Benart, H. Kahn, A.H. Heuer, M.A. Huff: A Titanium-Nickel Shape Memory Alloy Actuated Micropump, Transducers'97, pp. 361–364 (Chicago, IL, USA, 1997)
81. E. Makino, T. Mitsuya, T. Shibata: Micromachining of TiNi shape memory thin film for fabrication of micropump, Sens. Actuators 79, 251–259 (2000)
82. E. Makino, T. Mitsuya, T. Shibata: Fabrication of TiNi shape memory micropump, Sens. Actuators A 88, 256–262 (2001)
83. K. Hara, K. Hane, M. Sasaki, M. Kohl: Si Micromechanical Fiber-Optic Switch with Shape Memory Alloy Microactuator, Proceedings of the Solid-State Sensors and Actuators (Transducers'99), Sendai, pp. 790–793 (1999)
84. R.D. Howe, D.A. Kontarinis, W.J. Peine: Shape Memory Alloy Actuator Controller Design for Tactile Displays, Proceedings of the 34th Conference on Decision and Control, New Orleans, pp. 3540–3544 (1995)
85. P.M. Taylor, A. Moser, A. Creed: A sixty-four element tactile display using shape memory alloy wires, Displays 18(3), 163–168 (1998)
86. P.S. Wellman, W.J. Peine, G.E. Favalora, R.D. Howe: Mechanical Design and Control of a High-Bandwidth Shape Memory Alloy Tactile Display, 1997 International Symposium on Experimental Robotics, Barcelona, pp. 56–66 (1997)

87. R. Velazquez, E. Pissaloux, M. Hafez, J. Szewczyk: A Low-Cost Highly-Portable Tactile Display Based on Shape Memory Alloy Micro-Actuators, IEEE International Conference on Virtual Environments, Human–Computer Interfaces, and Measurement Systems (VECIMS 2005), Giardini Naxos, pp. 121–126 (2005)
88. W. Yoshikawa, A. Sasabe, K. Sugano, T. Tsuchiya, A. Ishida, O. Tabata: Design construction of beam structured vertical drive SMA thin film actuator for small tactile display, IEE J Trans. SM, 128(4), 151–160 (in Japanese, 2008)
89. Y. Okamura, T. Namazu, D. Kamoyama, N. Urushihara, T. Sasaki, T. Nagamura, Y. Isono: Ti-Ni SMA Film-Actuated 2-D Multi-Probe Array for Scanning Probe Nano-Lithography on a Wide Area, Transducers'07, pp. 2195–2198 (Lyon, France, 2007)
90. M.M.I. Bhuiyan, Y. Haga, M. Esashi: Design and characteristics of large displacement optical fiber switch, IEEE J. Quantum Electron. 41(2), 242–249 (2005)
91. J. Barth, B. Krevet, M. Kohl: A Bistable SMA Microactuator with Large Work Output, The 15th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers 2009), Denver, pp. 41–44 (2009)
92. G. Lim, K. Minami, K. Yamamoto, M. Sugihara, M. Uchiyama, M. Esashi: Multi-link Active Catheter Snake-like Motion, Robotica 14, 499–506 (1996)

Chapter 7
Dry Etching for Micromachining Applications

Srinivas Tadigadapa and Franz Lärmer

Abstract Dry etching processes provide the tools to machine precision high-aspect-ratio structures that form the basic building blocks of microelectromechanical systems. Dry etching processes consist of (1) purely chemical (spontaneous gas phase etching), (2) purely physical (ion beam etching or ion milling), and (3) a combination of both methods (reactive ion or plasma etching) for the controlled removal of desired substrate materials. Although some of the pioneering work in the field was performed as early as the 1970s and 1980s, the area of plasma etching has continued to evolve due to the continuing technological developments in high-density plasma sources, high-throughput vacuum pumps, and process control and instrumentation. Excellent reviews are currently available that provide details in various aspects of the technology and etching process development. This chapter is aimed at providing the reader with a broad understanding of the parameters that influence the results in dry etching techniques and to provide information that is useful to explore dry etching processes for the fabrication of next-generation MEMS devices. Practical recipes suitable for most commonly used plasma reactor configurations are provided and motivated in terms of the influence of the various control parameters and chemicals (gases used). Because process parameters can rarely be transferred directly across equipment or fabrication facilities, it is important to be able to tune the process parameter to specific process flow requirements and constraints. The material presented is not necessarily exhaustive, but focuses instead on practical issues to tackle for the development of dry etching processes suitable for MEMS applications across a broad range of materials.

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7.1 Dry Etching

Etching is the process of controlled removal of a desired material from a substrate via physicochemical methods. Etching can be performed either using chemicals in liquid state – defining a process commonly referred to as wet etching – or can be performed using chemicals in gaseous or plasma phase – defining the process of dry etching. Dry etching processes include plasma etching, reactive ion etching, chemically assisted ion beam etching, ion milling, and gas phase chemical etching. The chemical species used for the controlled removal of the material of interest is called an etchant. When the process of etching uses chemical species that can spontaneously react with the material to be etched and form volatile or gaseous products, the etching method is a purely chemical process governed essentially by the energetics of the reaction. However, most etching processes require additional energy to speed up the kinetics of the reaction and to engineer reactions onto pathways resulting in the formation of volatile products. This is often achieved by imparting considerable physical energy to the etchant molecules, radicals, and ions thereby resulting in a physicochemical reaction.

In the limiting case where a particular material cannot be removed easily by chemical reactions, a purely physical etching process known as ion beam etching or ion milling is used. Most dry etching processes lie in between the two extreme regions of pure chemical and pure physical etching processes. Excellent references on plasma etching for micromachining applications are available and the interested reader is referred to these for more detailed information [1–5]. A general overview on reactive ion etching can be found in [6], a review on silicon RIE is given in [7]. The capability of reactive ion etching (RIE), namely crystal orientation independent etching to realize arbitrarily shaped high-aspect-ratio microstructures, makes it an invaluable micromachining technology suitable for the micro- and nanoscale systems. Most of the present-day dry etching techniques have their origins in the classical RIE approaches developed for semiconductor manufacturing in the 1970s and 1980s [8–11]. This chapter focuses on presenting dry etching techniques from a process development perspective for a broad range of commonly encountered materials in microsystems applications.

7.1.1 Etch Metrics

Etching can be characterized by several important metrics. These metrics include etch rate, anisotropy, selectivity, etch stop, loading effects, uniformity, and so on. Figure 7.1 schematically depicts some of the important etch metrics. Briefly, the definitions can be given as follows.

Etch Rate: Defines the rate at which the exposed material is removed under given etch conditions. Etch rate is typically expressed in terms of thickness of the material removed per unit time or in the units of nm/min or μm/min. Fast etch rates are often desirable.

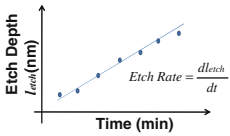
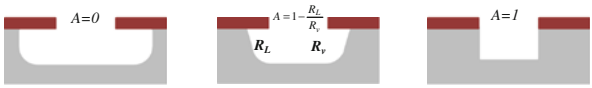
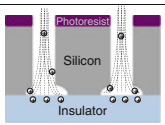
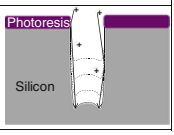
Etch Rate (R_v) (nm/min)	
Anisotropy (A)	**Perfectly Isotropic Etch** **Partially Anisotropic Etch** **Perfectly Anisotropic Etch** 
Selectivity (a:1)	Selectivity is given as a ratio: a:1,where a is the ratio of the etch rate of substrate to the etch rate of the mask.Typical selectivities in the range of 10: 1 to 100:1 are desirable.
Etch Rate Uniformity (%)	The uniformity of etch rate measured across a wafer or from wafer to wafer is given by: $Etch\ Rate\ Uniformity\ (\%) = \frac{Etch\ Rate_{Max} - Etch\ Rate_{Min}}{Etch\ Rate_{Max} + Etch\ Rate_{Min}} \times 100\%$
Notching	 Notching arises due to transient charging of exposed insulator underneath theetched layer which in turn severely affects the trajectories of energetic ions impinging on the substrate.
Microtrenching	Microtrenching describes the appearance of narrow grooves at the feet of the sidewalls in the direction of ion-bombardement. The etch profile irregularity is attributed to the forward scattering of the ions at sidewalls. 

Fig. 7.1 A brief summary of various etching metrics and parameters

Anisotropy: The degree of anisotropy (A) depends upon the etch rates in the vertical (perpendicular to the substrate surface) and the lateral (in-plane) directions. It can be mathematically expressed as

$$A = 1 - \frac{R_{\mathrm{L}}}{R_{\mathrm{V}}}, \tag{7.1}$$

where R_{V} is the vertical etch rate and R_{L} is the lateral etch rate. An ideal anisotropic etch has a value of 1 where the lateral etch rate is insignificantly small in relation to the vertical etch rate and a completely isotropic etch has an anisotropy value of 0 when the two etch rates are equal.

Selectivity: Selectivity refers to the relative etch rate of the material of interest with respect to the masking material which is typically photoresist. A high selectivity is required to achieve good masking and high fidelity pattern transfer through the process.

Etch Stop: Often etch processes need to be terminated after a defined depth is attained. Such a control on the etch depth can be achieved via timed etches or by the use of a layer of material upon which the etching process terminates. Etch stop layers allow for greater process control and compensation for nonuniformities in

etch rate across the wafer arising due to loading effects and/or equipment. A good etch stop layer must exhibit high inertness in the etch process especially in relation to the material to be etched. Typically etches are terminated on the etch stop layer using spectroscopic methods, residual gas analysis of the volatile etch products, laser interferometry, or laser reflectometry.

Etch Nonuniformity: Etch nonuniformity refers to the variation in the etch depth of features across a wafer. To ensure meaningful measurement of the nonuniformity across a wafer or from wafer to wafer, the etch depth must be measured on identical features. It is well known that the etch rate in plasma etching varies depending upon the feature width, an effect more commonly known as aspect-ratio-dependent etching (ARDE). In this effect, narrow features are found to be etched less than wider features under same plasma conditions. Compensation for the resulting nonuniformity in etch depth typically requires 20–30% overetching of wider features and the availability of an etch stop layer is vital to the success of achieving high uniformity. Etch uniformity across a wafer or from wafer to wafer is defined as:

$$\text{Etch Rate Non} - \text{Uniformity}(\%) = \left(\frac{\text{Etch Rate}_{\text{Max}} - \text{Etch Rate}_{\text{Min}}}{2 * \text{Average}}\right) \times 100\% \tag{7.2}$$

Loading Effects: The etch rate is not only a function of the gas chemistry and physical settings of the process, but also depends upon the total material (area) to be etched. In general etch rates are found to decrease as the area of material to be etched increases, especially in chemically dominant processes and is a direct consequence of the increased consumption of the etchant (reactant) species or gases. Loading effects manifest macroscopically at the wafer level when the total area of the material to be etched is changed by either increasing the number of wafers or via new mask designs. Loading effects also manifest at the microscopic level especially when etching high-aspect-ratio structures due to the local depletion of etchant molecules in etched features. Reactive ion etching lag or aspect-ratio-dependent etching describes the difference in the etch rate between large and small width features within the same wafer. These effects can also manifest across a wafer where, for example, an aluminum substrate holder is used to etch silicon in fluorine plasma. Aluminum does not react with fluorine radicals, therefore there is reduced consumption of the radicals around the periphery of the wafer from those in the middle of the wafer. This results in the well-known bullseye effect whereby features at the edges of the wafer are etched more rapidly than in the middle of the wafer. Such nonuniformity is typically compensated by overetching the substrate material onto a high selectivity etch stop layer. In general the etch rate R_n, when etching n-wafers each with an etch area A, can be written as [12, 13]

$$R_n = \frac{R_0}{1 + nkA}, \tag{7.3}$$

where R_0 is the etch rate in empty chamber, and k is a constant related to the ratio of the amount of etchant molecules consumed in etching a wafer to the amount

of etchant lost via recombination in the chamber volume/surface. As long as the volume or surface recombination of etchant molecules dominates, the loss arising due to consumption during etching can be neglected and thus loading effects are minimal. This is practically realized in large etch chambers and large flow rates. Microscopic loading is typically mitigated by performing the etches at reduced pressure and when ion bombardment or physical etch mechanisms dominate the overall character of the etch process.

Notching: The notching effect manifests as a narrow lateral opening (wedge) at the interface of the conductive material being etched and an insulating under layer. Typically, notching occurs during the overetch phase in the regions where the insulating underlayer is first exposed. In the case of silicon etching on a layer of silicon dioxide, the origin of notching is found in the local electric-field-induced trajectory bending of energetic ions that directly bombard and etch the foot of the Si sidewall. The process continues through the subsequent forward scattering or electrostatic deflection of energetic ions at the newly exposed SiO_2 surface under the notch [14].

Microtrenching: Microtrenching manifests as the appearance of rapidly etched narrow grooves at the bottom corners of etched vertical sidewalls. This enhancement in the etch rate in these corner regions is typically attributed to the preferential shallow angle forward scattering of energetic ions by the mask and etched substrate sidewall. Microtrenching is dominant in high-energy ion-bombardment-driven etching processes including ion beam etching. Although the phenomenon is observed in all kinds of substrates, charging effect in insulating substrates can also enhance the microtrenching processes. A detailed exposition on this subject can be found in [15].

7.2 Plasma Etching

Plasma etching (PE) and/or reactive ion etching (RIE) are well established process technologies in the semiconductor industry [3, 6, 7]. The classical tool is the diode reactor, as shown in Fig. 7.2. The scheme depicts the key elements of a typical plasma etching system: a number of reaction gases provided to the chamber by adjustable mass flow controllers, a grounded showerhead electrode as a gas inlet, a substrate electrode carrying the wafer, and a power supply to the substrate electrode by radio frequency (RF) via a coupling capacitor (which is mostly part of a more complex matching-unit to adapt RF impedances). Detailed descriptions of different plasma reactors and processes can be found in [16].

In RIE configuration, ions from the plasma are accelerated to high energy levels (several 100 eVs) and perpendicularly directed towards the powered substrate. In the plasma etching (PE) configuration, the showerhead is powered and the substrate electrode grounded. In this case, acceleration of ions from the plasma to the substrate is restricted to minor energy levels of only a few eVs and the directionality of the ions is lower than in RIE configuration. In the triode configuration, both the substrate electrode and the showerhead electrode are powered simultaneously,

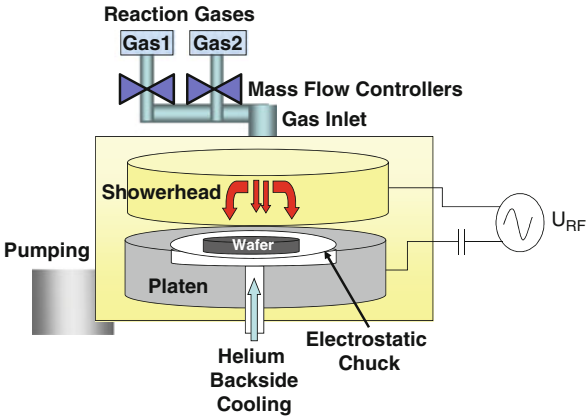


Fig. 7.2 Schematic illustration of a diode plasma or reactive ion etcher. The reactor is pumped to low-pressure conditions. Reaction gases are supplied to the chamber via the upper showerhead electrode. The lower electrode is powered by RF to drive the plasma discharge and accelerate the ions towards the substrate (RIE configuration)

either at the same or at different frequencies, see below. The goal is to generate the plasma at the desired plasma density controlled by the power level supplied to the upper electrode, and to accelerate the ions towards the substrate at the desired energy value controlled by the power level supplied to the substrate electrode, more or less independently of each other.

Radio frequencies generally used are in the low-frequency (380 kHz), mid-frequency (2 MHz), or high-frequency (13.56 MHz) regime. Typically, 13.56 MHz is used as a standard for plasma generation.

Pumping provides the low-pressure conditions in the reactor chamber needed for the electrical discharge to form between the powered and the grounded electrode, which builds up the plasma in an atmosphere of one or more compound gases, at a pressure ranging from 0.1 to 100 Pa.

The coupling capacitor allows the powered electrode to float at a DC-potential generated from the applied RF voltage and arising due to the difference in the mobilities of negative charges (electrons) and positive charges (ions) in the plasma. This is the so-called DC-bias voltage, which is responsible for energizing the ions.

7.2.1 Types of Etching

Isotropic Plasma Etching: With regard to etching, a reactive plasma consists of two relevant kinds of species: ions and radicals. The plasma is by far dominated by chemically active neutral species, the so-called radicals ($\sim 10^{19} - 10^{22}\,\mathrm{m}^{-3}$) in comparison to the electron and ion densities ($10^{15} - 10^{20}\,\mathrm{m}^{-3}$). Active radicals are created by the decomposition of gas molecules into fractional parts after collisions between gas molecules and energetic electrons in the plasma. In most cases, an electron-neutral collision breaks up the neutral molecule into neutral radicals. Being electrically uncharged, radicals reach the substrate with no or only little directionality, bond to the surface, and react readily with the material to etch, to more or less volatile compounds. If the reaction takes place instantaneously and the volatility

of the reaction products is high enough, the volatile compounds leave the etched surface quickly yielding isotropic etching behavior. This so-called chemical etch depends mainly on the properties of the materials involved, provides high selectivity, and makes it, in general, easier to find appropriate etching masks (e.g., SiO_2 for masking a Si-etch).

Fluorine radicals delivered in a plasma discharge from fluorine-rich gaseous compounds such as sulfur hexafluoride SF_6, carbon tetrafluoride CF_4, or nitrogen trifluoride NF_3, exhibit isotropic etching behavior towards silicon. Once adsorbed to the silicon surface, fluorine radicals react spontaneously with silicon atoms to form silicon fluorides SiF_x ($x = 1,2,3,4$). The reaction main products, SiF_2 and SiF_4, are volatile enough to leave the surface without a need for physical assistance, and in the process remove silicon atoms from the etched surface. Because there is no directionality contained in the mechanism, silicon etching proceeds with no preferential orientation, and the profiles are isotropic. This is an ideal behavior for underetching micromechanical structures in a so-called sacrificial etching or release-etching step, for the fabrication of free-standing and movable elements on top of a wafer. In contrast to that, etching masks such as SiO_2 or photoresist are not or only slowly attacked by fluorine radicals, without physical assistance by the energetic ions. A number of advanced micromachining technologies make use of combinations of anisotropic and subsequent isotropic silicon etching: first etch deep in the vertical direction, then protect the structures and underetch in the lateral direction [17, 18]. A well-known process example is single-crystal reactive etching and metallization (SCREAM) [19].

Plasmaless Isotropic Etching: For the purpose of silicon sacrificial etching, it is not even necessary to use a plasma source of fluorine radicals. A number of gaseous compounds are well known for the ability to etch silicon spontaneously, without a need for plasma excitation. XeF_2 [20, 21], BrF_3 [22], and ClF_3 [23] deliver fluorine radicals which once adsorbed onto the surface, lead to the spontaneous etching of the silicon. For example, XeF_2 is a white solid at room temperature and atmospheric pressure. However at ~395 Pa and room temperature the solid sublimates and in this form is able to etch silicon. Gas phase xenon difluoride isotropically etches silicon according to the chemical reaction:

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4.$$

The reaction is exothermic and may result in an increase in the local temperature, especially in thermally isolated structures. This effect is mitigated by the use of pulsed rather than continuous etch systems [24]. The absence of any liquid phase eliminates stiction-related problems. Typical etch rates greater than 1 μm/min have been reported which can be reduced by diluting XeF_2 with nitrogen. Furthermore, the etch process is a purely chemical isotropic process and requires no other form of physical energy input for it to occur. XeF_2 has very high etch-selectivity between silicon and all other known materials used in the semiconductor processes [25]. Selectivities may well exceed values of 1000 for most metals or dielectrics.

A typical XeF_2 etching process in a pulsed mode is as follows: The cycle begins by evacuating the expansion and etching chambers to a pressure of ~13.2 Pa. This allows the XeF_2 crystals to sublimate and fill the expansion chamber to a selected pressure. The etching and expansion chambers are then connected and the pressure is allowed to equilibrate to 130–400 Pa. Typically etching begins immediately and the pressure begins to rise due to an increase in the total number of moles of the gases. After a selected etch-time has passed, both chambers are again evacuated to a 13.2 Pa, held for 10 s, and the process is repeated. The advantage of pulsed systems over continuous systems is that the quantity of etchant delivered each cycle is known and can be controlled. However, it is important to note that the etch rates are dependent on the quantity of silicon present in the chamber. The presence of water vapor can also have a deleterious effect on the etch performance inasmuch as water vapor can react with XeF_2 to form HF molecules which are ineffective in etching silicon. Furthermore, the etch rate in the first few cycles can be lower than later cycles, due to the presence of native oxide on the silicon. Silicon dioxide is found to offer a good selectivity whereas nonstoichiometric silicon nitride (Si_xN_y) is found to be etched in XeF_2. Table 7.1 shows the etching rates obtained for single-crystal silicon and polysilicon for the conditions used [26].

Table 7.1 Measured etch rates in XeF_2 gas phase etching system [26]

Material	XeF_2 pressure (Pa)	N_2 pressure (Pa)	Etch time (s/cycle)	Cycle time (s)	Etch rate (nm/cycle)
Si (SC)	395	0	45	90	100
Polysilicon	395	0	45	90	2500
SiO_2	395	395–790	45	90	0.1
Si_xN_y	395	395–790	45	90	10

Figure 7.3 shows the typical silicon surface obtained after etching in XeF_2. The uniform and randomly nucleated spontaneous etching process causes the surface to roughen the longer the etching is performed. Typical RMS surface roughness values range from 100 nm to 1 μm. The process can also be controlled and slowed down by the addition of nitrogen to provide controlled thinning of silicon structures at the nanometer scale. In a recently published paper, high selectivity was demonstrated for the first time for selectively etching a SiGe sacrificial layer with respect to Si functional structures in chlorine trifluoride gas [27]. This makes any need for passivation and protection of the functional silicon during the release step obsolete. XeF_2, BrF_3, and ClF_3 react with silicon via a physisorbed surface layer.

However, in comparison to XeF_2 and BrF_3, ClF_3 shows slower reaction kinetics due to the formation of a fluorosilyl skin [28]. The hampering effect of the fluorosilyl layer is explained via a diffusion like transport of ClF_3 molecules through a fluorosilyl layer [29]. This is the basis for anisotropic etching of Si at low temperatures and the reason for the extremely high selectivity of Si over SiGe, where Ge atoms act as accelerators of the ClF_3 decomposition reaction. ClF_3 shows crystal

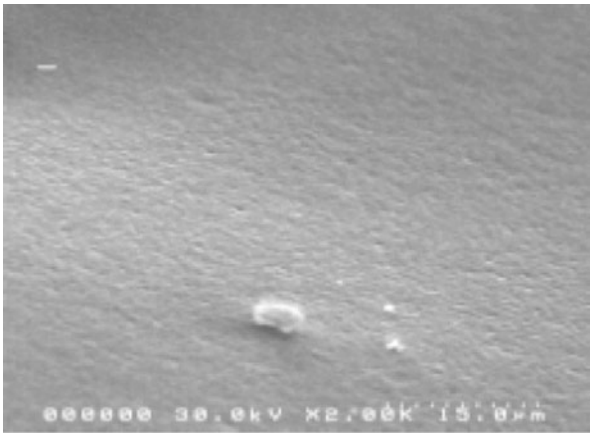


Fig. 7.3 Typical texture of the single-crystal silicon surface resulting after etching in XeF_2 gas phase etching

orientation-dependent "anisotropic" etching of silicon below 0°C. The <110> direction shows a maximum whereas <100> direction shows a minimum of the angular etch-rate distribution, with a ratio of <110>/<100> ≈ 1.5.

Anisotropic Etching: The second major species of importance in plasma etching of substrates is the positively charged ions also known as cations. Although less numerous than radicals, ions are, however, entirely responsible for any directionality and anisotropic nature of the etch. They are created during collisions of neutral gas molecules with energetic electrons in the plasma in which an electron is knocked off from the molecule and leaves behind a positive charge. Being electrically charged, ions can be accelerated towards the substrate by negatively biasing the latter with respect to the plasma potential using DC or RF voltage. This results in the ions bombarding the substrate surface in a more or less perpendicular orientation. The ions represent the directional contribution provided by the plasma, and all approaches to create anisotropic plasma etching rely on a perpendicular ion flux to the substrate. Owing to their directionality, ions do preferentially hit the bottom of a structure and only to a lesser extent their sidewalls. The incoming ions transfer their kinetic energy to the local area of impact. Although the number of ions is small compared to the number of chemically active neutral species, their energetic impact can significantly affect or drive the progress of the etching reaction locally. Ion-assisted directional etching can be caused by one or several of the following mechanisms.

(i) Induction of chemical reactions between adsorbed radicals from the plasma and the material to etch, by providing the activation energy through ion impact, especially if the reactivity of etching species with the material is low or hindered by an energy barrier.
(ii) Desorption of reaction products from the surface by the sputter action of incoming ions, especially if the volatility of the reaction products is low and the

latter stick to the material surface, forming an inhibiting film there. In this case, ion impact removes the inhibiting film of reaction products from the surface.

(iii) Desorption of other inhibiting films by the sputter action of incoming ions, for example, polymer films formed from polymerizing additives to the plasma, or films formed from nonvolatile reaction products between the material to be etched and other additives to the plasma.

Etching based on the halogens of lower reactivity such as chlorine and bromine is strongly ion-driven, which gives anisotropy to the process, however, limits achievable etch rates (typically to below 1 μm/min), etch depths (a few μms) and mask selectivities (e.g., 20–30:1 for SiO_2-hardmask). Because physical impact from the ion flow to the substrate plays a key role in the etch, selectivity as a result of individual chemical properties of the involved materials becomes less significant. Typically, there is a fundamental tradeoff between increasing the anisotropy by stronger ion bombardment on the one side, and maintaining mask selectivity sufficiently high on the other side.

7.2.2 Plasma Sources

Reactive ion etching, except in the case of gas phase chemical etching involves the use of various plasma sources into which the substrates can be introduced for etching. Depending upon the exact configuration of the electrodes and how the RF power is coupled into the chamber, plasma reactors can be classified as: (i) capacitive, (ii) inductive, and (iii) wave etchers. Furthermore, depending upon the location of the plasma with respect to the substrate, etchers can be classified as (i) plasma contact or (ii) downstream etchers. Figure 7.4 lists the major RIE systems that are briefly described next. Detailed information on plasma sources and etcher configurations can be found in [30].

Barrel Etchers: These systems are mainly used for surface treatment and were the plasma system configuration in early designs. Plasma is typically generated with RF-powered electrodes (capacitive coupling) or with a coil wrapped around the dielectric tube (inductive coupling). These systems can be used to remove photoresist residues from wafers using oxygen glow discharge. Initial experiments demonstrating CF_4-based silicon etching were performed in these systems, which resulted predominantly in isotropic etching due to the lack of directionality of the ions (See Fig. 7.4).

Capacitively Coupled RF Diode System was the work horse of the 1980s for reactive ion etching applications. The wafer is placed on the powered electrode and the best results are usually obtained at low pressures (<13.2 Pa). This approach does not allow independent control of the ion energy and the ion current at a fixed pressure and RF frequency. Typically ion energies of hundreds of eV are required to achieve the desired etch rate. A particularly effective implementation of the diode approach was the “hexode” machine developed at Bell Labs and developed to allow

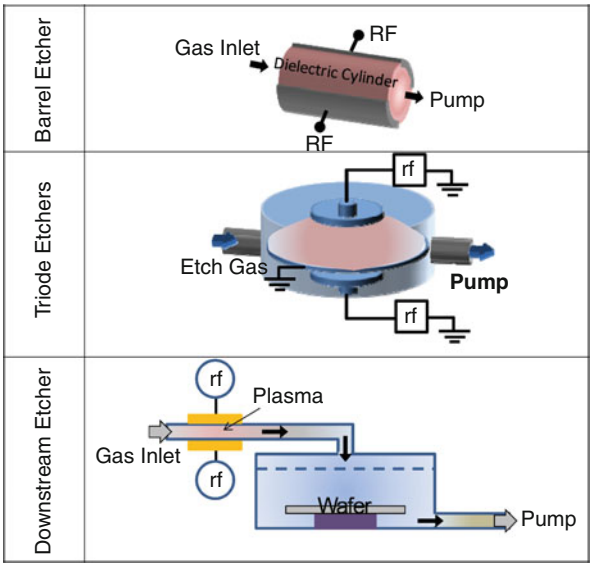


Fig. 7.4 Schematic illustration of major plasma sources and etcher configurations

etching of several wafers simultaneously. This plasma etcher configuration was a dominant batch-processing machine in the 1980s [31].

Capacitively Coupled Planar Diode and Triode Systems: The planar diode plasma configuration has been already discussed in the previous section. The triode geometry shown in Fig. 7.4 was well known in sputter deposition technology and introduced in plasma etching technology to allow independent control of ion energy and ion flux. This approach allows the ion energy to be reduced while keeping the etch rate constant by increasing the ion flux density. The wafer is placed on the lower electrode; the lower electrode power (bias power) is used to control the ion energy and the upper electrode power (source power) is used to control the ion flux. It is well known that the RF voltage needed to deliver a fixed power to the plasma decreases strongly as the frequency is increased. Thus large power can be delivered to the plasma through the high frequency (typically 13.56 MHz) without high-energy bombardment of the electrode. The ion bombardment energy at the wafer surface (lower electrode) can be controlled by a lower frequency RF power applied at the lower electrode. The term "triode" is used for this two-electrode system to recognize the fact that the grounded wall serves as a third (reference) electrode.

Chemical Downstream Etching: Figure 7.4 shows the schematic illustration of a chemical downstream etching system. In these systems, the wafer chamber is separated from the plasma source by a tube with no line-of-sight connection to the plasma source. Few ions and electrons reach the surface of the substrate and etching is carried out by the energetic neutral radicals. The process is specifically designed to minimize damage onto the surface but the etching process is isotropic

and therefore these machines are not particularly useful for high-definition pattern transfer applications.

High Density Plasma Sources: Inductively coupled plasma sources (ICP) or transformer coupled plasma sources (TCP) (see Fig. 7.5) have emerged as the most effective source technology for plasma etching and are now more or less the industry standard.

Inductively Coupled Plasma: This is generated by the inductor coil which together with a capacitor forms part of a more complex resonant LC-network

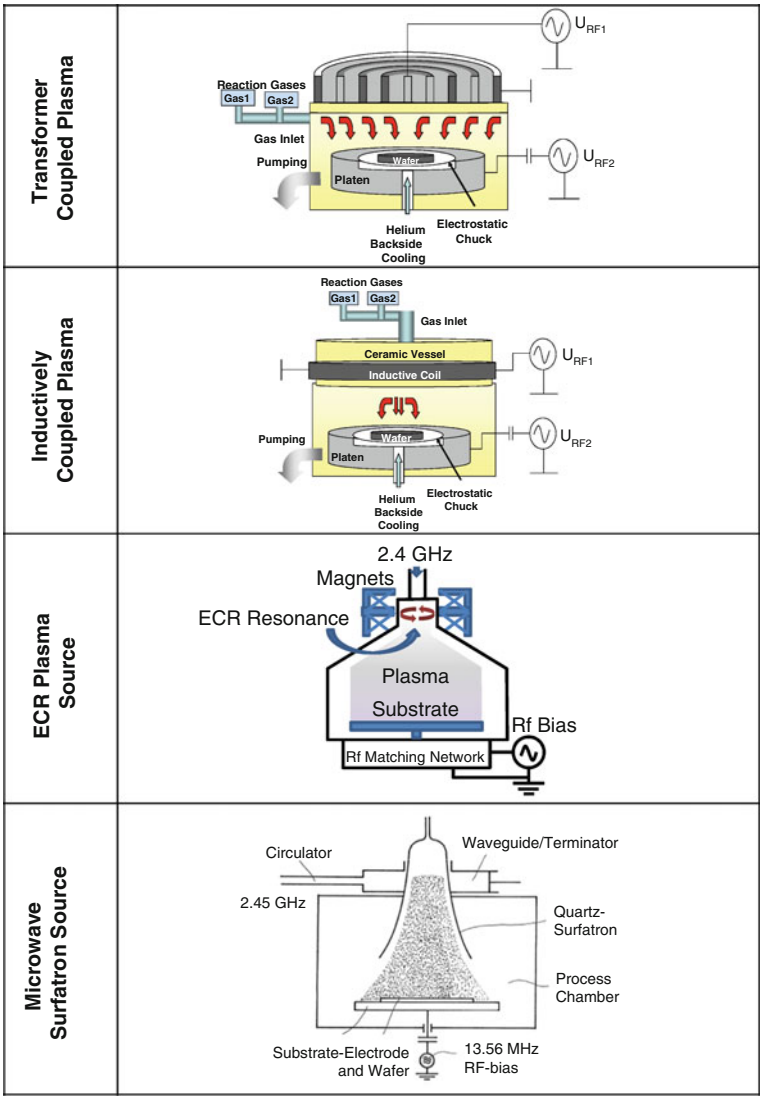


Fig. 7.5 Schematic illustration of popular high-density plasma sources

("matching unit"). The coil-and-capacitor arrangement is driven in resonance by radio frequency (RF) power. In most cases, RF frequency of 13.56 MHz is used for driving the ICP, but also 2 MHz and lower frequencies can be found in some cases. In the ICP-configuration, the coil of one or several turns, depending on the chosen frequency, is wound around a dielectric vessel. In the TCP arrangement, a flat or dome-shaped coil covers a dielectric window, which may again be flat or dome-shaped, on top of the etching chamber.

By feeding radio frequency power to the coil, a high-frequency oscillating magnetic field is generated inside the chamber, in the vicinity of the coil, with a corresponding oscillating electric field resulting from Maxwell's induction law. The electric field can excite and drive a high-density plasma within the process chamber. The plasma cannot shield itself effectively from this inner driving electric field by sheath formation, thus extremely high densities of charged particles (electrons and ions $\sim 10^{18} - 10^{20}\,\mathrm{m}^{-3}$) can be obtained by the inductive coupling technology. Electrons are heated by the RF electric field and generate the ions and chemically active species by collisions with gas molecules. However, before the plasma of charged and neutral species reaches the substrate, the hot electrons need to cool down and as a rule, the distributions of ions and neutrals requires some kind of readjustment and rearrangement, for the homogenization of etching results. Mechanical apertures [32], gas flow guides and gas flow redirectors, in combination with balanced excitation of the inductive coil [33] and magnetic lenses for plasma collimation [34], are found in this place.

Electron Cyclotron Resonance: This equipment is based on the fact that electromagnetic power can be propagated into the plasma more efficiently in the presence of a magnetic field. Typically a cyclotron resonance condition can be established when the frequency at which the electrons orbit around the magnetic field lines is equal to the frequency of the applied electric field. In most cases, microwave frequencies of 2.45 GHz or higher are used in ECR-equipment. Note that there is some confusion with the use of the term "ECR" also for magnetically enhanced RIE configurations (so-called MERIE or HRE), where plasma densities in a diode or triode reactor configuration are enhanced to some degree by the interaction with stationary or slowly varying magnetic fields.

In the ECR microwave system, the pressure should be low enough so that the electrons can undergo several orbits without colliding with gas molecules (usually less than 0.132 Pa). One of the concerns with use of ECR-sources for RIE applications is the nonvertical incidence of electrons and ions on the sample which causes some isotropic behavior in the etch profile unless additional RF biasing is applied to the substrate electrode for a more directional acceleration of the ions to the wafer. The major drawback of ECR sources is the low operating pressure window (0.0132–0.132 Pa) which limits the density of chemically active species in the plasma and in many cases the achievable etching rates for lack of reactants. At higher pressure, electron cyclotron resonance disappears and microwave excitation changes to an inefficient thermal heating of the plasma. On the other hand, in the ECR mode, the degree of ionization and ion flux to the wafer are higher than with other high-density plasma sources discussed, which makes the ECR an ideal source for strongly ion driven reactions.

Microwave Excitation: Microwaves can be used to establish glow discharges such as in ECR (see above) or surfatron sources as shown in Fig. 7.5 [35, 36]. A microwave surfatron consists of a dielectric tube or horn (in most cases made from fused silica or ceramics material) which guides the microwave field coupled into it along the border between its dielectric surface and the generated plasma. Microwave surfatron plasma excitation yields plasma properties (densities of reactive species, electrons, and ions) quite close to those from ICP sources and offers a similar process window with regard to the operating pressure and gas flow ranges. The major benefits of using microwave excitation is that available microwave power levels are virtually unlimited: magnetron tubes even for the very high power are comparatively low cost and extremely robust, and microwave configurations including magnetron, circulator, and water-load are highly resistant to damage, for example, from high reflected power situations that occur from time to time due to temporary mismatch conditions from quickly varying plasma impedances. This makes microwave excitation an economic solution for the very high power levels needed in some applications.

Table 7.2 lists a brief comparison between the various plasma sources with respect to their plasma characteristics.

Substrate Cooling and Clamping: For improved heat dissipation off the wafer, helium backside cooling is applied in most high-density plasma etching systems. Heat is generated on the wafer surface due to (i) exothermic etching reactions, (ii) flow of energetic ions to the wafer surface, and (iii) absorption of radiation power from the plasma by the wafer. Insufficient heat removal would increase the wafer temperature to values intolerable from a process standpoint (e.g., degrading the photoresist mask or sidewall passivation films). To prevent overheating, gaseous helium is used as a convective medium supplied at elevated pressure (1–2 kPa) between the wafer backside and the substrate electrode top surface. To enable backside pressurizing, the wafer needs to be tightly clamped to the substrate electrode. Clamping is often achieved through mechanical clamps in the form of springs or clamp-rings pressing onto the wafer perimeter, or by electrostatic forces exerted from an electrostatic chuck. Today electrostatic clamping is the most common way of fixing the wafer to the substrate electrode, because the clamping force is homogeneously distributed all over the wafer thus reducing the risk for wafer breakage, and edge exclusion zones caused by plasma disturbances from the mechanical clamps can be significantly reduced thus increasing usable wafer area and chip yield in production.

Many constructions of electrostatic chucks do exist. What is common to all of them is an arrangement of conducting segments put on top of an insulating disk and covered by an isolating layer. A high DC voltage of the order of kV is supplied to the conducting segments, either in a unipolar arrangement or in a bipolar arrangement (with respect to ground level).

In the unipolar arrangement, all conducting segments of the chuck are connected to the same voltage level, and electrostatic forces build up between the wafer and the E-chuck surface as soon as the high-density plasma is ignited. The conductivity of the plasma establishes a defined wafer potential, depending on RF biasing power. The difference in potentials between wafer and chuck segment electrodes is the

Table 7.2 Comparison of different plasma source types with regard to key performance parameters[a]

Plasma source	Excitation//bias frequencies	Operating pressure range (Pa)	Chemical activity	Ionization level (m^{-3})	Independent ion energy control
Barrel	RF	10−1000	Low	–	–
Diode	RF	1−100	Mid	$10^{14}-10^{16}$	No
Triode	RF//RF, LF	1−100	Mid	$10^{14}-10^{16}$	Mid
Downstream etcher	RF, μWave	10−1000	High	–	–
Microwave ECR	μWave//RF, LF	0.01−0.1	Low	$10^{19}-10^{21}$	High
Microwave surfatron	μWave//RF, LF	0.1−100 (→ atm.)	High	$10^{18}-10^{20}$	High
ICP/TCP	RF//RF, LF	0.1−100 (→ atm.)	High	$10^{18}-10^{20}$	High

[a]RF = radio frequency 27.12, 13.56, or 2 MHz; LF = low frequency 100–450 kHz; μWave = microwave frequencies 7.35, 4.9, or 2.45 GHz

source of the electrostatic clamping forces. When the plasma (and the clamping voltage) is (are) switched off, the wafer is released and can be easily removed from the substrate electrode.

In the bipolar arrangement, the voltage polarity of the segments on the E-chuck is alternating from one area to the other, for example, between +1 kV and –1 kV symmetrically. Irrespective of plasma conditions, electrostatic forces build up between the wafer (at virtual ground potential with respect to the clamping voltages) and the top surface of the E-Chuck. For declamping, in general a depolarizing voltage cycling is needed before completely switching off the clamping voltage and removal of the wafer from the electrode to overcome the holding forces of residual charges accumulated in the chuck dielectrics.

7.3 Plasma Process Parameters and Control

In general, plasma etching processes can be considered as comprising three basic unit steps namely:

(i) Adsorption and chemisorption of the reactant atoms on the surface of the substrate
(ii) Reaction and formation of a volatile reaction product having a high vapor pressure
(iii) Desorption and diffusion of the product molecules away from the substrate.

In general plasma etching processes use gases containing halogens (halogens are group VII elements, namely, fluorine, chlorine, bromine, iodine) because these elements are known to be highly electronegative and reactive. Upon reacting with the materials of interest, halogens form compounds that are known as halides. The volatility or inertness of the resulting halide is particularly significant. For the third step to be most effective, products with high vapor pressure are desired. Table 7.3 lists the boiling temperature of silane and various silicon halides. It is clear that in comparison with other halides, silicon tetrafluoride is highly volatile and likely to most easily desorb off the surface.

Table 7.3 Boiling temperature of various silicon halides and silane[a]

	Boiling temperature (°C)
SiH_4	−111.8
SiF_4	−86
$SiCl_4$	57.6
$SiBr_4$	154
SiI_4	287.5

[a]The volatility of these molecules is an important reason for the reactive etching of silicon and silicon compounds [37].
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Each of these steps plays an important role in the determination of the eventual etch rate of a given material and the rate limiting process among these limits the overall process. For example, the etching mechanism of silicon using fluorine (a halogen) can be schematically depicted as shown in Fig. 7.6. In this reaction the formation of fluorinated skin upon exposure to fluorine neutrals is an important first step. Fluorine is readily adsorbed into the first few monolayers of silicon typically forming fluorosilyl layer composed of SiF_x $(x = 1-3)$ whereas chlorine owing to its larger atomic size tends to be adsorbed mainly on the surface. The ion-bombardment step slightly enhances the final step of the reaction, the formation of volatile SiF_4 which then desorbs from the surface of the substrate. This combination of adsorption of fluorine into several monolayers of silicon as well as the greater volatility of SiF_4 in comparison to $SiCl_4$ results in a higher yield per striking ion and therefore a higher etch rate of silicon in fluorine plasmas. In fact etching of silicon in fluorine plasma proceeds fast even without ion assistance.

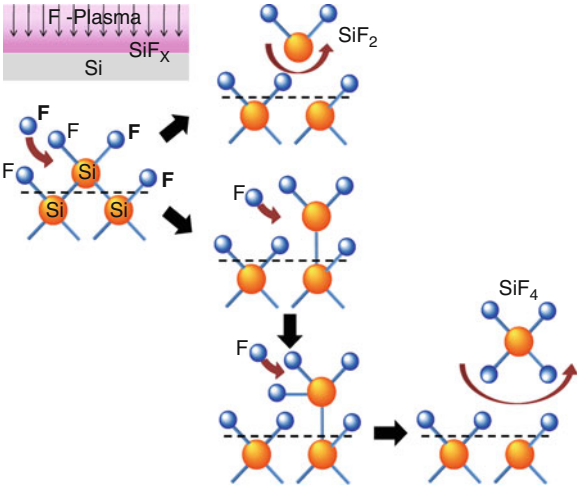

Fig. 7.6 Schematic illustration of the mechanism of plasma etching of silicon in fluorine chemistry. Few monolayers thick fluorinated skin is formed on the silicon surface which upon further attack by fluorine radicals liberates the surface silicon as SiF_2 (minor process) while the remaining surface silicon atoms proceed through various SiF_x steps until eventually liberated as SiF_4 (dominant process) [3]

7.3.1 Energy-Driven Anisotropy

In the 1970s pioneering experiments were performed by Coburn and Winters that have elucidated the role of ion bombardment on the etch rate [38]. These experiments on silicon etching used XeF_2 as the etch gas with Ar^+ as the bombarding ions. The choice of Ar^+ as the ion was to preclude any role in chemical reactions with silicon whereas XeF_2 was chosen to readily provide the atomic fluorine atoms.

Figure 7.7a shows the result of the experiment and its relevance to energy-driven anisotropy in etching. In the initial part of the experiment, the silicon wafer was exposed to XeF_2 gas only and the etch rate obtained was small. This phase essentially reflects pure chemical component of the etching. At the end of this period, the

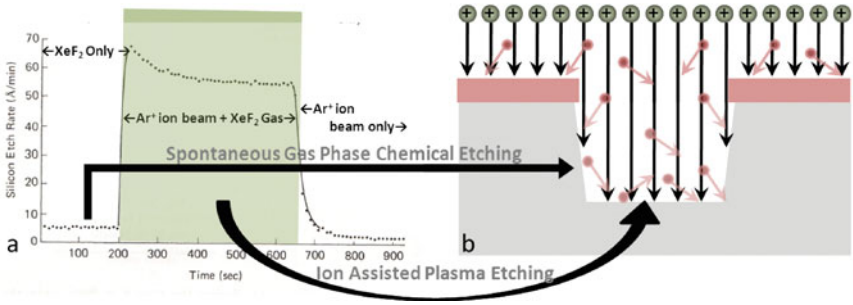

Fig. 7.7 (**a**) Silicon etch rate in three different condition [38] (Used with permission, copyright 1979, the American Institute of Physics). From the experimental results it can be clearly seen that the etch rate upon Ar^+ ion bombardment of the fluorinated silicon surface results in an etch rate that is much larger than the sum of spontaneous chemical etching in XeF_2 gas or in pure Ar^+ plasma. This difference in the etch rates can be used to achieve anisotropic etching as shown schematically in (**b**). The *solid arrows* are used to show that the etching on the sidewalls mimics spontaneous chemical etching due to the lack of ion bombardment on these surfaces whereas the bottom of the etched feature is rapidly etched due to the ion-assisted plasma process

Ar^+ ion flux is turned on and the etch rate is observed to immediately rise in this ion-assisted etching phase. At the end of this period, the XeF_2 gas supply is turned off. In the absence of atomic fluorine supply, the etch process becomes a pure physical sputtering process accomplished by the bombarding Ar^+ ions. It is clear that the etch rate during the reactive ion etching phase is much larger than the sum of pure physical and chemical etch rates. It is this observation that imparts anisotropy in the plasma etching processes. Because the sidewalls of etched features are not subjected to ion bombardment as opposed to the bottom of the etch features, the etch rates of the bottom of the wafer are significantly higher than on the sidewalls. In other words, the etch rate downwards is determined by ion-assisted chemistry whereas the sidewall etching proceeds via spontaneous reactions at much slower rates resulting in the desired anisotropy. Figure 7.7b illustrates the origin of this anisotropy schematically. Note that fluorine radicals from plasma behave differently than XeF_2, in that XeF_2 needs some activation energy to etch silicon whereas fluorine radicals do not need any such activation energy beyond the thermal energy levels.

7.3.2 Inhibitor-Driven Anisotropy

In inhibitor-driven anisotropic etches; preferential etching of the bottom of the features as opposed to the sidewalls is achieved by the formation of a protective layer on these facets during the etching process. Bombardment of the energetic ions either prevents the formation of the passivation layer or continuously removes it so as to facilitate the preferential reactive (chemical) etching of the substrate. For example, during silicon etching, introduction of hydrogen in any of the fluorocarbon etch gases (e.g., CF_4, C_2F_6, CHF_3, etc.) reduces the amount of free fluorine by

readily combining to form HF. This results in the deposition of a polymer layer (polymerization) on all the surfaces of the substrate.

However, inasmuch as the sidewalls of the etched features are not significantly bombarded by the energetic ions, the formation of fluorocarbon polymer layer protects the underlying silicon substrate whereas the polymer layer is continuously cleared by the energetic ion bombardment at the bottom thereby exposing the substrate silicon to the fluorine gas. This technique can be used to create highly anisotropic etches with aspect ratios in the range of up to 50:1. However, care must be taken so as not to compromise the critical dimension of the etched feature due to the deposition of excessive amounts of polymer layer on the sidewalls. The same concept can be extended by etching the substrates at extremely low temperatures. For example, etching silicon substrates at cryogenic temperatures of <–100°C using fluorocarbon gases, results in the formation of nonvolatile residues on the sidewalls whereas the etching of the bottom surface is driven by the continuous bombardment of the energetic ions. This method has the advantage of avoiding the formation of the passivating polymers on the sidewalls which can be very difficult to remove. However, at the cryogenic temperatures the etch process is very sensitive to any contaminants in the chamber and to the existence of native oxide layers because, at these low temperatures, the breakdown of these materials is very difficult. Figure 7.8 schematically illustrates the inhibitor-driven anisotropic etching process.

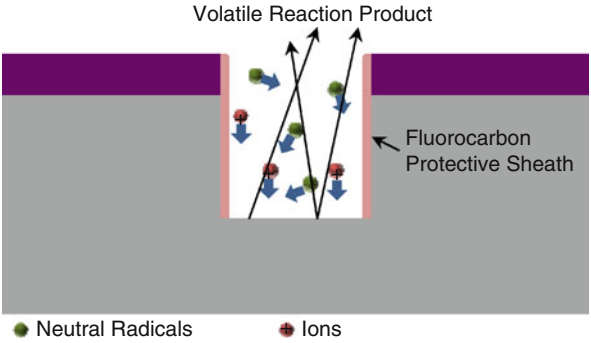

Fig. 7.8 Schematic illustration of inhibitor-driven anisotropy. Preferential buildup of protective fluorocarbon protective sheath due to the lack of ion bombardment results in enhanced etching of the bottom of the feature

7.3.3 Selectivity in Plasma Etching

In addition to etch rate and anisotropy, selectivity is a major consideration in transferring patterns into the substrate via etching processes. A large selectivity between the masking material and the etched material is desirable. This enables the achievement of high-fidelity pattern transfer which typically involves a certain amount of overetching to compensate for the nonuniformity in the etch process across a wafer.

In general, selectivity can be achieved due to differences in any of the three steps involved in plasma etching. Specifically, high selectivity can be achieved when:

(i) One of the materials in given plasma is highly inert. For example, removal of photoresist from SiO_2 surface using oxygen plasma is a very high selectivity process. This is because oxygen atoms adsorb minimally onto the oxidized surface and no reactive processes between the SiO_2 film and the oxygen plasma occur. On the other hand, oxygen plasma volatizes the photoresist via the formation of various carbon–hydrogen–oxygen reaction products which are pumped away resulting in a very high selectivity for the photoresist ashing process.
(ii) High selectivity can also be achieved due to the formation of nonvolatile products in the plasma. This situation is best illustrated when fluorine plasma is used for the removal of silicon dioxide mask layer on III-V compound semiconductors such as GaAs. Atomic fluorine upon reaction with group III elements such as Al, Ga, or In forms involatile AlF_3, GaF_3, and InF_3 which have boiling points of $\sim$1290, 1000, and >1200°C, respectively, whereas silicon dioxide can be readily etched in fluorine plasma via the formation of volatile SiF_4.
(iii) High selectivity can also be achieved if the etch rate of one of the materials in question, in the same plasma, can be comparatively retarded. For example, in fluorocarbon-based plasma etching of silicon and silicon dioxide it is well known that the net etch rate achieved for each material is the result of the competing processes of: (i) fluorine-based reactive etching and (ii) inert film formation due to the polymerization of fluorocarbon. By the appropriate addition of hydrogen into such plasma, the process can be adjusted such that for SiO_2 surface, the fluorine-based etch process slightly dominates the passivation film formation. However, for the same plasma conditions, the process is likely to be skewed towards the formation of the polymer film on silicon surfaces due to the unavailability of the surface O_2 and a difference in the sticking coefficient between the two material surfaces for the plasma gas species. These differences are typically exploited to realize selective etching of SiO_2 against silicon. However, the selectivity obtained in this case is not very high and very careful control of the etch process has to be maintained to achieve a repeatable etch selectivity.

7.4 Case Study: Etching Silicon, Silicon Dioxide, and Silicon Nitride

Etching Silicon and Its Compounds Using Halogen Chemistry: Silicon can be etched in any halogen containing gases such as F_2, CF_4, C_2F_6, C_4F_8, SF_6, CHF_3, NF_3, Cl_2, CCl_4, BCl_3, Br_2, CBr_4, and the like. As explained above, fluorine radicals spontaneously etch silicon by the formation of volatile SiF_4 product. Although

chlorine molecules dissociatively chemisorb on silicon at room temperature, they have to surmount an energy barrier of ~10 eV to attack the backbonds of the atoms on the silicon surface to form $SiCl_4$. No such energy barrier is observed for the formation of SiF_x and thus the reaction proceeds spontaneously at room temperature. Thus, bombardment of the etched surface with energetic ions is necessary to initiate the $SiCl_4$ and $SiBr_4$ formation reaction whereas ion bombardment in the case of fluorine gases slightly enhances the reaction.

Furthermore, radicals produced in the plasma from the halogens of lower reactivity, such as chlorine and bromine, react with silicon producing less volatile reaction products which stick to the surface. Thus, ion impact both activates and induces the formation of silicon chlorides or bromides from silicon depending upon the adsorbed halogen radicals, and simultaneously removes the nonvolatile (inhibitor) films of the reaction products. In particular, silicon bromides are of very low volatility and need energetic ion bombardment to assist their clearing from the silicon surface. The sidewalls of etched features typically see a very small flux of ion bombardment, thus etching in chlorine and bromine chemistries results in an energy-driven anisotropic etch. Fluorine etches tend to have a greater isotropic etch tendency and result in minimal surface damage.

The etch rate of silicon and its compounds in fluorocarbon-based plasma can be increased by the addition of O_2 which scavenges carbon away, preventing the polymerization of the unsaturated fluorocarbon species. The same effect can be achieved by the addition of chlorine gas to CF_4 and CCl_4 because chlorine acts as an effective oxidizer. However, addition of oxidizers reduces the selectivity to photoresist masks because carbon polymers are also aggressively etched through the same chemistry.

Anisotropy in Halogen Chemistry: Anisotropy in fluorine etches is usually inhibitor driven. Addition of hydrogen containing gases in fluorocarbon chemistry, leads to the depletion of fluorine radicals and therefore a reduction in the F/C ratio. An F/C ratio in the 2–3 range is required for effective inhibitor driven anisotropic etch process development [39]. Passivation of sidewalls can be enhanced via oxidation or nitridation of unbombarded silicon surfaces by addition of small amounts of oxygen or nitrogen gas to the plasma. Sidewall protection may also be improved by deposition of chlorocarbon or bromocarbon films, by the addition to the plasma of chlorocarbon or bromocarbon gases which readily polymerize upon plasma activation. Ion bombardment breaks up the passivation or protective films formed on such surfaces, that is, the structure bottom, leading to a directional and vertical etching.

High Selectivity SiO_2 Etching in Fluorocarbon Plasma: Addition of hydrogen leads to the preferential formation of the CF_x film on silicon surfaces rather than on silicon dioxide surfaces. This is because the continuous bombardment upon a SiO_2 surface causes the fluorocarbon film to volatilize via reaction with the surface oxygen in the SiO_2 layer in the form of CO, COF_2, and CO_2 products. This results in the selective formation of a protective polymer film on silicon surfaces and leads to preferential etching of SiO_2 [40–42]. Photoemission peak studies on CF_4/40% H_2 plasma-treated silicon surface shows a clear Si-C "bridging" bond peak at 284 eV [43] which is critical to the formation of the fluorocarbon film on the silicon surface.

Figure 7.9 shows the polymer film thickness and etch rates of silicon and silicon dioxide upon 0–50% H_2 addition to CF_4 plasma [43]. An increasing thickness of the fluorocarbon with increasing hydrogen concentration and a proportional decrease in the etch rate of silicon is observed, whereas the SiO_2 shows neither an enhanced formation of the fluoropolymer film nor any appreciable dependence of the resulting etch rate. Using this technique SiO_2: Si selectivity of up to 20:1 has been reported. $CF_4 - H_2$ plasma provides high selectivity between photoresist and SiO_2 films as shown in Fig. 7.10.

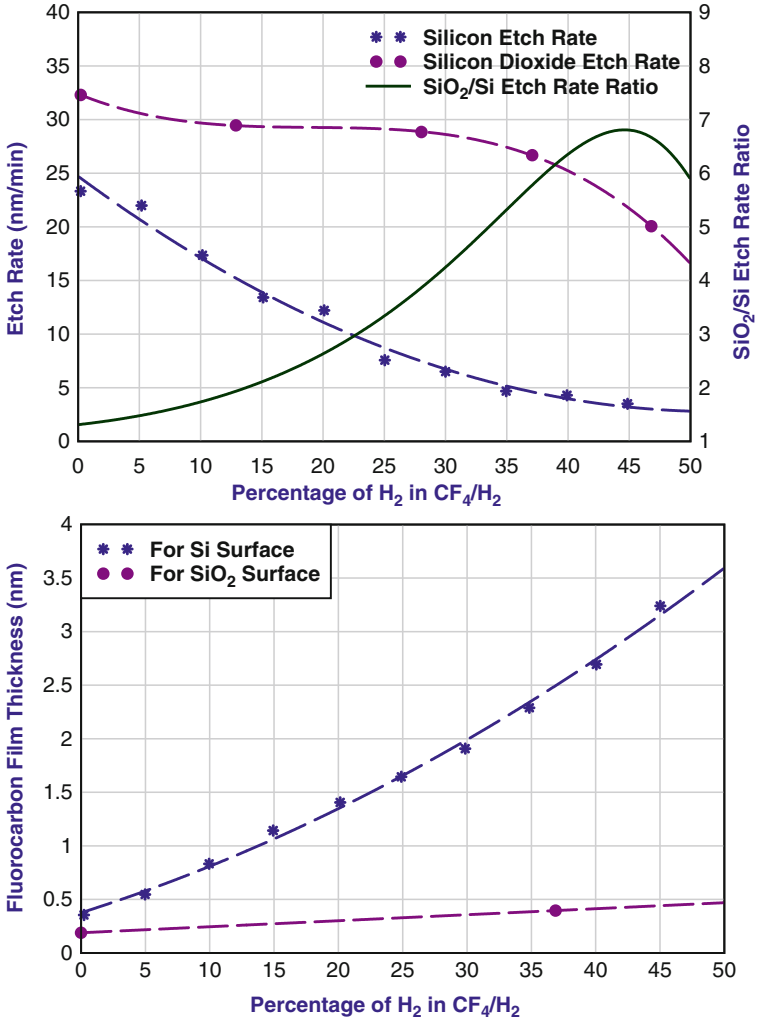

Fig. 7.9 Fluorocarbon film thickness on Si and SiO_2 measured after 5 min RIE under identical condition (*bottom*). Formation of the relatively thick layer of fluorocarbon effectively suppresses the etch rate of silicon in CF_4/H_2 (*top*) plasma providing high selectivity conditions suitable for etching SiO_2 [43] (Used with permission, copyright 1989, The Electrochemical Society)

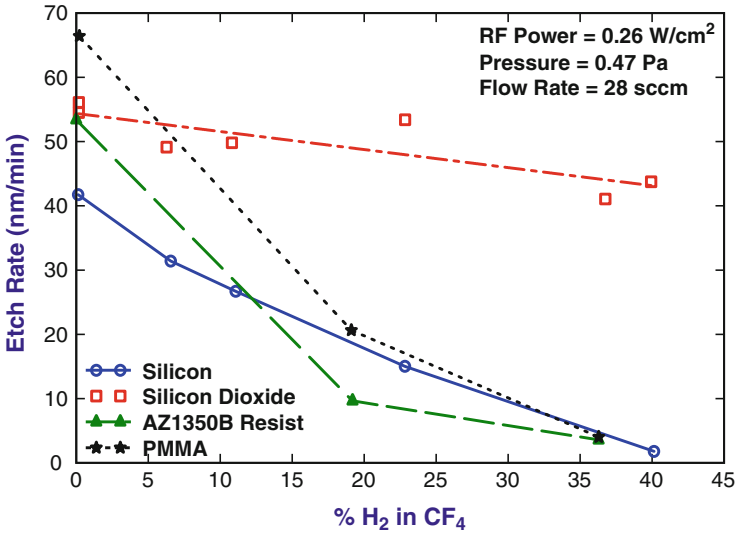

Fig. 7.10 Etch rate of photoresists, silicon, and silicon dioxide in H_2/CF_4 plasma. At high hydrogen percentage, a large value of selectivity between SiO_2 and these materials is obtained [42] (Used with permission, copyright 1979, The Electrochemical Society)

Silicon to Silicon Dioxide Etch Selectivity: Fluorine plasma naturally provides an inherent selectivity for etching silicon with respect to silicon dioxide. Flamm et al. measured the luminescence during silicon etching in fluorine plasma and concluded that fluorine atoms etch silicon at a rate ($R_{F(Si)}$)given by [44]

$$R_{F(Si)} = 2.91 \pm 0.20 \times 10^{-12}\sqrt{T}n_F e^{-0.108\,\mathrm{eV/k_BT}}, \tag{7.4}$$

where n_F is the atom concentration of fluorine given in #/cm^{-3}. The etch rate for silicon dioxide ($R_{F(SiO_2)}$) in fluorine plasma is given by the expression

$$(R_{F(SiO_2)}) = 6.14 \pm 0.49 \times 10^{-13}\sqrt{T}n_F e^{-0.163\,\mathrm{eV/k_BT}} \tag{7.5}$$

resulting in a relative Si to SiO_2 etch ratio of

$$\frac{R_{F(Si)}}{R_{F(SiO_2)}} = (4.74 \pm 0.49)e^{-0.055\,\mathrm{eV/k_BT}} \tag{7.6}$$

and ranges from a value of 41 at room temperature to 26.2 at 100°C. Etching of silicon in chlorine plasma has been presented by Schwartz et al. [7]. In general silicon etching in chlorine plasma is an ion-beam induced process and therefore results in poorer selectivity.

Addition of Inert Gases: In addition to oxidants and radical scavengers, inert gases are often added to the plasma. This is done for several reasons: (i) inert gases such as Ar stabilize the plasma because they readily donate electrons to the plasma

in contrast to the chemical species which, owing to their high electronegativity, capture available electrons needed to maintain the glow discharge; (ii) the high sputter yield of Ar^+ ions improves the ion-assisted etch rate; (iii) the directional nature of ion bombardment through the sheath improves the anisotropy of the etch; and (iv) the high thermal conductivity of inert gases such as He when added to the plasma can improve the heat transfer from the substrate wafer to the supporting chuck and plasma chamber. Of course large quantities of inert gas addition will dilute the reactive gas component and the etch process will shift towards physical sputter etching.

Recently, Yamakawa et al. [45] have demonstrated very high speed etching of silicon dioxide (BPSG) film using microwave excited nonequilibrium atmospheric pressure plasma. The authors were able to demonstrate an ultrahigh etch rate of SiO_2 (14 μm/min) and an unprecedented selectivity of 200 with respect to silicon using NF_3/He along with addition of H_2O as the etching gas. The fast etch rate can be attributed to the presence of NF_x radicals arising from the breakup of NF_3 into $NF_x^* + F^* -$ radicals. $NF_x -$ radicals (with $x > 0$) are extremely aggressive towards SiO_2 and other dielectric (and polymers) materials and etch them at extremely high speed. Addition of water vapor (H_2O) consumes the fluorine radicals by HF formation ($2F^* + H_2O \rightarrow 2HF + < O >$) whereas NF_x radicals are much less scavenged. Water vapor therefore acts as a selective fluorine radical scavenger and consequently reduces any undesirable Si-attack. However, if NF_3 is completely broken down, for example, as in high-density, high-power plasma, then the plasma primarily consists only of fluorine and nitrogen radicals. Under these conditions, a complete quenching of the fast etch rate of SiO_2 and other dielectrics has been observed. The complete breakup of NF_3 molecules under appropriate plasma conditions is also confirmed by the plasma color which changes from a deep red to a bluish color, indicating a change in preponderance from NF_x to fluorine radicals in the plasma.

Silicon Nitride Etching: Silicon nitride is readily etched in fluorine plasma and has intrinsic etch characteristics between silicon and silicon dioxide. Because silicon nitride is typically used in the LOCOS (local oxidation of silicon) process, there is often a need to etch silicon nitride over silicon dioxide and silicon with high selectivity. The intrinsic rate of etching for Si_3N_4 is about 5–10 times higher than that of SiO_2 depending upon temperature. In a CF_4/O_2 plasma the obtained Si_3N_4:SiO_2 selectivity is ~2 [46]. In general adding nitrogen to CF_4/O_2 plasma has been found to improve the selectivity of silicon nitride over silicon dioxide to 10:1.

Sanders et al. reported achieving a high selectivity of >10:1 for etching silicon nitride over silicon dioxide by the addition of CF_3Br to CF_4/O_2 plasma [46]. It is considered that this chemistry converts some of the F atoms into BrF and BrF_3 which selectively etch silicon nitride whereas silicon dioxide is not affected by the interhalogen gas species. Furthermore, Br and Cl radicals in the plasma are thought to convert the atomic oxygen (radicals) into more inert oxygen molecules. This quenching of oxygen radicals, which would otherwise oxidize the Si_xN_y surface explains the enhancement of Si_xN_y etching in comparison to SiO_2 in interhalogen gases. The highest selectivity in etching silicon nitride over silicon dioxide has been reported when using interhalogen fluoride gases such as ClF_3 and BrF_3 [47].

In summary, due to the spontaneous formation of SiF_4, silicon is more easily etched than SiO_2 which requires the etching process to be induced via ion bombardment. Addition of oxygen in RIE etch processes increases the etch rate of both Si and SiO_2. Addition of hydrogen can be used to selectively etch silicon dioxide over silicon through the formation of fluorocarbon films. Silicon nitride etches at a rate that is in between that of silicon and silicon dioxide. Highly selective etching of silicon nitride over silicon dioxide layer can be performed in 1:2 ratio NF_3/Cl_2 downstream etchers.

7.5 Case Study: High-Aspect-Ratio Silicon Etch Process

Fluorine-based plasma etching processes for silicon yield high etch rate, etch depth, and mask selectivity, and in particular enable photoresist masking with good selectivity between silicon and photomask. This is mainly due to the high chemical reactivity and spontaneous etching nature of the fluorine radicals towards silicon, and the high volatility of the silicon fluorides as reaction products. As a consequence, the etch is intrinsically isotropic. Fluorine radicals do not need ion activation to initiate or enhance their reaction with silicon, or to remove the reaction products from the silicon surface; anisotropy can only be achieved by the inclusion of sidewall passivation schemes to the process. The existing approaches to deep reactive ion etching (DRIE) of silicon are distinguished by the way sidewall passivation is achieved, the key to anisotropy and overall performance of the etch process. Cryogenic etching and the so-called "Bosch process" with alternating etch and passivation cycles are the two most well-known high-aspect-ratio silicon etch processes and are discussed in this section.

A high-density plasma tool with so-called remote or decoupled plasma is beneficial or even a must for all silicon DRIE approaches, be it cryogenic or Bosch processing. Silicon DRIE is based on the chemical activity of the plasma. Chemical activity requires both a sufficiently high concentration of passivating radicals, and a sufficiently high concentration of fluorine radicals to obtain the high etch rates. For a high density of chemically active species, a process pressure regime of typically between 1 and 10 Pa is most appropriate. Energy of the ion flux bombarding the wafer surface must be controlled independently from the plasma excitation, through substrate electrode biasing by a radio frequency or low frequency bias generator. For a good control of ion acceleration independent of plasma excitation, the plasma potential should be kept as low as possible near ground potential. The latter involves decoupling of the plasma excitation zone from the substrate region.

Traditional plasma sources for RIE fail in one or more of these requirements. Diode and triode reactors show insufficient plasma excitation density, below 10^{16} m^{-3}. Electron cyclotron resonance (ECR) sources are inappropriate for the very low pressure regime (<0.1 Pa) tolerated by the cyclotron resonance mode. ECR is a typical ion-current type of source and lacking sufficient chemical activity. Microwave surfatron sources (a tube or horn made from dielectric material, to guide the microwave field along the interface between the dielectrics and the

plasma burning inside the tube or horn, down to the process chamber, (e.g., see [48]), helicon sources, and inductively coupled plasma (ICP) sources open the pressure window up to 10 Pa and to even higher pressures. Amongst these alternatives, the ICP has emerged as the most appropriate and widespread source technology for DRIE and as the industry standard.

7.5.1 Cryogenic Dry Etching

As explained, sidewall passivation is necessary to obtain anisotropic silicon etches. One approach is to use fluorine radicals created from sulfur hexafluoride gas (SF_6) in the plasma discharge as the main etching species which would readily and isotropically remove silicon wherever it is unprotected and accessible. Oxygen radicals are created in the plasma from oxygen gas (O_2) and serve for silicon surface oxidation. Oxidation saturates dangling bonds on the silicon surface and builds up a passivating silicon oxide film, which inhibits fluorine attack of the silicon. After finding the appropriate SF_6 to O_2 flow ratio, an oxide scavenging gas such as trifluoromethane CHF_3 may be added to improve results and widen the process window to some degree (so-called "Black Silicon Method", see [49]). At room temperature, the percentage of oxygen needed to achieve anisotropic profiles is larger than 50%, which reduces both etching speed and mask selectivities considerably.

Cryogenic dry etching is a variation of the sidewall passivation technique based on surface oxidation. Lowering the wafer temperature into the cryogenic regime typically around 173 K (–100°C) by liquid nitrogen (LN_2) cooling of the substrate electrode, brings down the required oxygen amount for anisotropic etching to a few percent of the total gas flow, thus pushing up etching speed and mask selectivities drastically. In addition, the process window for achieving anisotropic etching is widened strongly.

This results from an enhancement of the chemical stability of the inhibiting silicon oxide film in a fluorine-based plasma, mainly because desorption of reaction products of silicon oxyfluoride-type from unbombarded surfaces is frozen by the low temperature. Ion bombardment of the etch floor removes the passivating film there by sputtering off most of the chemical compounds. Perfectly vertical etching in silicon can be achieved with a strong overweight of etching fluorine radicals, compared to the passivating oxygen radicals, yielding high etch rates and a relatively wide process window, in comparison to the room temperature situation.

Impressive results are achieved with cryogenic dry etching in inductively coupled plasma tools such as the Alcatel reactor, with silicon etch rates reaching 4–6 μm/min, and mask selectivities of several 100:1 for SiO_2-hardmasks [50, 51]. Use of photomasks is difficult due to cracking and delamination reasons at the low substrate temperatures, however, not impossible if special resist treatment for stress adjustment is performed before the etch. The main drawback of the cryogenic etching method is related to the low substrate temperatures needed and the critical dependence of process properties on the substrate temperature, given the strong heat impact from the plasma to the substrate and the exothermic etching reaction

between silicon and the fluorine radicals. In addition, the substrate as the coldest part in the whole reactor configuration acts as a cryopump, freezing out compounds from the plasma which act as hard-to-remove micromasks on the wafer surface. Micromasking is responsible for the formation of microneedles and micrograss on the silicon which is often observed in deep cryogenic etches as a disturbing and often unacceptable factor. Nevertheless, cryogenic dry etching is a very important silicon microstructuring technique, for example, in microoptical applications, where smooth sidewalls on a nanometer scale are of key importance.

7.5.2 Bosch Process

The etching technique described before makes use of relatively hard to remove compounds as passivating layers, in the form of silicon oxides or oxyfluorides resulting from silicon surface oxidation. Their complete removal from the etch floor without leaving micromasking residues requires energetic ion impact, eventually in combination with added scavenging agents. Excessive ion sputtering and the use of scavengers reduce the selectivity towards the masking materials. This is especially true in the case of photoresist masking. There is a tradeoff between a clean trench bottom and high mask selectivity.

A technique that avoids the formation of such hard to remove compounds is the deposition of smooth polytetrafluoroethylene (PTFE) or Teflon®-like films on the silicon surface during etching. Early published work describes the importance of the balance between etching and polymerizing species, and effects of changing this balance for both Si and SiO_2 etching [52].

Plasma polymerization can be achieved by the generation of $(CF_2)_n$-type radicals in the plasma, starting from precursor gases such as hexafluoropropene (C_3F_6) or octafluorocyclobutane (RC318®, C_4F_8), the latter being a nontoxic and stable dimer of tetrafluoroethylene (TFE, C_2F_4). The deposited smooth passivating film consists of a network of long linear $(CF_2)_n$-chains with only little cross-linking, which can be easily removed from the etch floor by low-energetic ion bombardment without leaving behind any residues. A mixture of sulfur hexafluoride gas for the fluorine radical supply and octafluorocyclobutane gas for the supply of polymer-forming radicals can be used in the plasma to achieve both passivation at the sidewall and etching at the etch floor, yielding anisotropic profiles in silicon. In addition, having fluorocarbons in the process to some extent scavenges undesired oxygen in the background gas or oxygen precipitates in Si and thus prevents the formation of hard passivation (silicon oxides) from the etched surface (floor).

However, the presence of fluorine radicals as etching species and of Teflon® film-forming monomer species together in the plasma, at the same time, leads to recombination and mutual extinction of both kinds of species. This makes the "mixed process" difficult to control for deeper etches and lowers process performance mainly with respect to etch-rate. Although, these drawbacks are somewhat mitigated using high-density ICP plasma, still the potential of the "mixed process approach" remains limited to shallow trenches with a depth on the order of 10 μm.

The recombination problem was overcome by the patented Bosch-process technology [48], which is a variation of the Teflon®-based sidewall passivation technique. Figure 7.11 illustrates the process mechanism: passivation and etching gases are introduced separately and alternately into the process chamber and the substrate to be etched is exposed to a high-density plasma, during the so-called passivation and etch cycles, respectively. In each passivation cycle, thin Teflon®-like film is deposited onto the walls of etched structures from C_4F_8-precursor species. Some scavenging of oxides from the silicon etch floor may also happen during or after the Teflon® deposition step. During the subsequent etching cycle, part of this film is removed from the coated sidewall by off-vertical ion impact and driven deeper into the trench. At the same time the trench bottom is cleared of fluorocarbon polymer and etched by fluorine radicals released from SF_6 in the plasma. Switching times between steps normally range from a few seconds up to 1 min, depending on sidewall roughness that can be tolerated. Because the passivating polymer film can be easily removed by small ion impact sputtering, mask selectivity reaches very high values, for example, 150:1 for photoresist and »300:1 for SiO_2 hard masks. If harder passivating polymers were used, more aggressive ion impact would be required and as a consequence, the selectivity towards the masking material would be reduced.

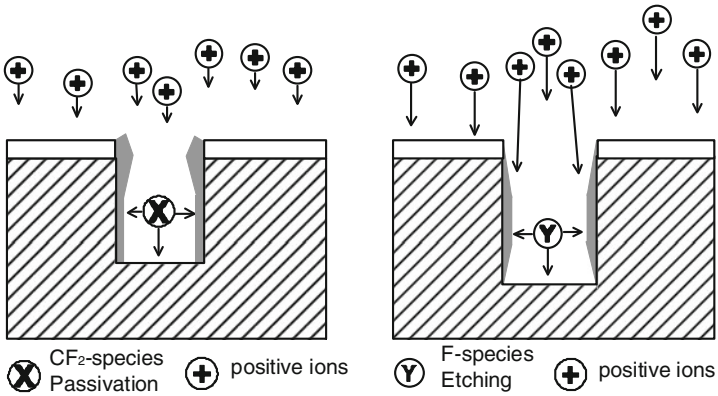

Fig. 7.11 Illustration of the basic mechanism of the Bosch process. The protecting Teflon®-like film deposited onto the structures during the passivation step is cleared from the trench floor and driven deeper into the trenches during the (intrinsically isotropic) fluorine-based etching step

Transport of the sidewall film (i.e., removal and redeposition of Teflon®-material) yields some local anisotropy of the etching steps that would otherwise be completely isotropic, in the vicinity of the sidewall, but does not adversely affect the main etching reaction away from the sidewall. Sidewall roughness is thus reduced despite the discontinuous process. Plasma polymerization is nonconformal in narrow trenches and film formation preferentially takes place at the trench opening, leaving deeper sidewall regions with less deposited passivating film, therefore the flow of polymer material along the sidewalls towards the trench floor also provides a

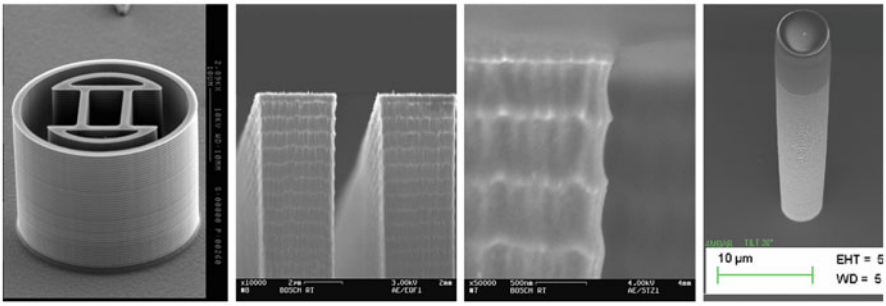

Fig. 7.12 Trench profiles and sidewall structure resulting from a typical Bosch DRIE process recipe

more uniform sidewall passivation over the trench depth. Figure 7.12 shows typical structures, profile forms, and characteristic sidewall scalloping arising from standard Bosch DRIE process recipes.

The discontinuous nature of the process overcomes a number of general problems involved with anisotropic etching.

Firstly, recombination loss of reactive species, by gas phase reactions causing their pairwise extinction, is excluded by separating them in the time domain. This is most important for the volume of the plasma source itself, where the species are generated at high concentration levels and where recombination would be strong. Outside the high-density source area, in a more diluted state, coexistence of species is easier to achieve and some mixing there, in the space between the source and the substrate, can be tolerated. For a high-density plasma source, sufficiently small in volume, switching times to below 1 s, for example, down to 100 ms are possible. Passivating and etching species remain separate in the limited volume of high-density plasma excitation, but may overlap on their way from the source to the substrate. This so-called "ultrafast gas-switching condition" yields very smooth sidewalls with hardly any remaining sidewall scalloping at all, as is depicted in the SEM pictures of Fig. 7.13.

Secondly, a vertical etching process having high mask selectivity bears an inherent risk for micromasking the trench floor. Even minor contamination on the etch surface may lead to formation of residues, microroughness, and even microneedles. Having a sidewall with a periodic nanostructure or ripple on the order of 10 nm in size is an advantage in this respect: micromasks smaller than the characteristic dimension of the scallops are undercut and extinguished from the surface, leaving back no etch residues. Only if the size of a micromask exceeds the critical dimension limit that the process can tolerate by undercutting will it cause a potential residue problem. This has to be considered in connection with the before-mentioned approach where the sidewall scalloping is practically gone: the latter process is more critical with respect to formation of microroughness, resulting from micromasking effects starting from a random distribution of incidental contaminants on the etched surface.

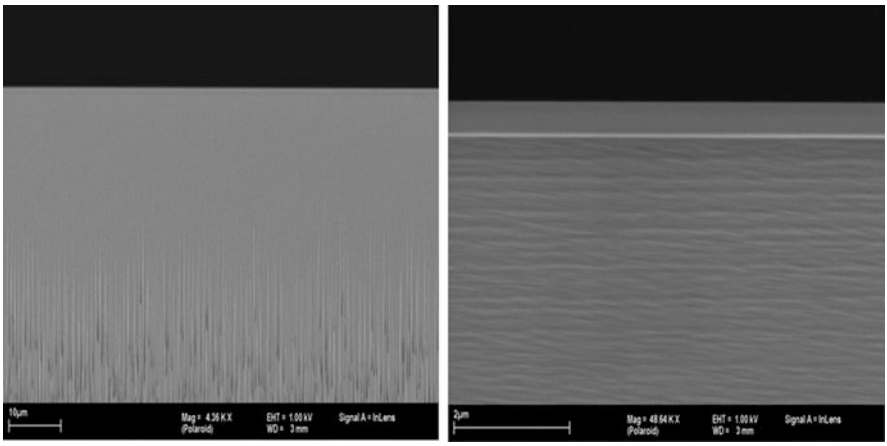

Fig. 7.13 SEM pictures of the sidewall resulting from a Bosch process using an ultrafast switching recipe: hardly any horizontal scalloping is visible at the sidewall any more. Some vertical striations are visible in the lower part of the left-hand side SEM picture, indicating the beginning of microroughness formation at the trench bottom, which also affects the sidewall

7.5.3 Understanding Trends for DRIE Recipe Development

High-Aspect-Ratio Etches: As a general observation in plasma etching processes, net etch rate decreases with rising aspect ratio of the trenches. In addition, reduced ion impact reaching the trench floor shifts the etching process towards more effective passivation with higher aspect ratios. As a consequence, profiles tend to develop positive slopes and typically trenches end up tipping when their aspect ratios begin to approach values of greater than 20:1.

Given the condition of having all trenches within a similar range of widths, adaptation of the process recipe stepwise or continuously [53, 54] helps to reduce the amount of passivation in the process and keeps the profiles straight. For example, passivation cycle time or passivation gas flow can be ramped down steadily. As an alternative, etching cycle time or etching gas flow can be ramped up steadily. Although other options including source power, bias power, or pressure ramping do exist; changing cycle times is the most obvious parameter ramping strategy, to affect the etch : deposition balance in a predictable and straightforward manner. With the use of parameter ramping, trenches of >50:1 aspect ratio can be fabricated, while keeping the sidewalls straight and vertical.

Aspect Ratio Dependent Etching – RIE Lag: Etching speed and profile evolution depend strongly on the depth : width ratio of the trench, the so-called aspect ratio. In general, the etch in narrower trenches progresses at a lower speed than in wider trenches; that is, higher-aspect-ratio trenches lag behind the lower-aspect-ratio trenches. This is partly due to the fact that the amount of ions reaching the trench floor progressively diminishes for reasons of aperture effects at the trench opening, in combination with the angular distribution of the ions. Another important aspect is transport limitations of gaseous species – radicals – in high-aspect-ratio trenches.

The amount of the lag effect is determined mainly by the mean free path of the gaseous species, that is, gas pressure.

Control of RIE Lag: RIE lag is a common and well-understood transport phenomenon in plasma etching [55]. The amount of the lag effect depends mainly on the mean free path of the gaseous species which determines their transport in etched trenches. The dependence of etch rate on the aspect ratio of the feature has been elucidated based upon a simple vacuum conductance model [56]. In addition, interaction and change of balance between etching and passivating species during transport in etched trenches is important, which is again related to mean free path and process pressure. Changes in the balance of etching and passivating species with increasing aspect ratio also affect the anisotropy and the profile. Figure 7.14 shows a characteristic example of RIE lag in high-aspect-ratio Bosch-process etches.

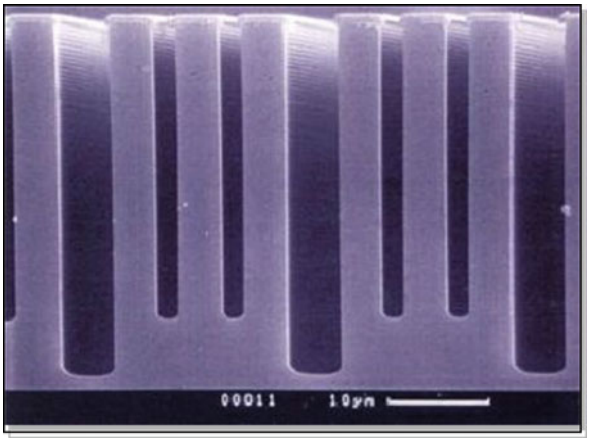

Fig. 7.14 Illustration of RIE lag effect: etch depth decreases with narrower gap sizes corresponding to higher aspect ratios

In a discontinuous process with separate etching and passivating cycles that can be controlled independently of each other, there is an individual lag effect both for the etching and for the passivating part of the overall process. For the etch step, the higher the aspect ratio of the trench the fewer fluorine radicals per time unit can reach the trench floor and etch the silicon, the size of the effect depending mainly on the etch step pressure. For the deposition step, the higher the aspect ratio of the trench the fewer polymer formers per time unit can reach the trench floor and build up an inhibiting film on the floor, the size of the effect depending again mainly on the deposition step pressure. Because a thinner inhibiting film on the etch floor boosts the rate for the subsequent etch step, this involves some compensation of the rate decrease with the aspect ratio resulting from the reduced fluorine radical supply. Deposition step lag and etching step lag can compensate each other to reach a lagfree overall process over a wide range of aspect ratios. This is achievable by individual control of the etch step and deposition step parameters; mainly by the pressure values set.

Setting the pressure higher for the individual step increases its lag effect; setting the pressure lower decreases its lag effect. Increasing deposition step pressure with

respect to etch step pressure, even to values higher than the etch step pressure, reduces the overall RIE lag of the total process and even inverts it at some stage, with higher-aspect-ratio trenches (i.e., narrower gaps), etching faster than smaller aspect ratio trenches (i.e., wider gaps). However, compensation of RIE-lag is at the expense of a reduced etch rate in the wider trenches, which approaches the low etch-rate value in the narrow trenches. On the other hand, running a deposition step pressure lower than the etch step pressure will cause a significant RIE-lag of the total process, however, at the benefit of higher overall etching rates in the wider trenches. This is the "normal" process regime which is used in most cases, in the interest of higher rates.

The stability of the polymer deposited onto the etch floor is an important weight factor in balancing etch and deposition lags, therefore the amount of achievable compensation depends also on the substrate temperature. Lowering the substrate temperature makes the floor polymer more robust and increases the weight of the deposition step in overall lag balancing. For this reason, a substrate temperature of 0°C or even lower, instead of the normal 40°C was found beneficial to achieve lagfree etching over a wide range of aspect ratios [57].

Suppression of Notching at Dielectric Interfaces: As explained at the beginning of this chapter, sidewall attach at the bottom of the etched features is observed when the etch terminates on a dielectric layer. This effect arises due to the redirection of the ions with charged dielectric at the bottom of the etch feature during the overetch phase [14, 58]. Pulsing the substrate–electrode bias power provides a mechanism for the discharging of the dielectrics during bias off-periods. Laermer et al. compared the pulsed biasing for low frequency (380 kHz) and high-frequency (13.56 MHz) carriers [59]. Notch suppression capabilities were demonstrated on high-aspect-ratio trenches (1.5 μm wide, 11 μm deep, 16% overetch on SiO_2). These results showed that pulsed LF (40 Hz, 50% duty cycle) and "double-pulsed" RF (100 kHz at 10% duty cycle + 140 Hz at 50% duty cycle) are equivalent with respect to notch suppression [59].

7.6 High-Aspect-Ratio Etching of Piezoelectric Materials

Dry etching techniques based upon the use of reactive plasma offer very attractive alternatives to the wet patterning techniques for piezoelectrics. Using a Langmuir probe, Steinbruchel made pioneering measurements for identifying the role of ions in reactive plasma etching [60]. Since then, several gas species have been used for the etching of various piezoelectric materials. In this section we present etching processes suitable for several piezoelectric materials.

7.6.1 Case Study: High-Aspect-Ratio Etching of Glass (Pyrex®) and Quartz

Silicon dioxide in its crystalline form (quartz) as well as its amorphous form (glass) is finding increasing applications in microsystems, as active resonator structure as

well as passive support and packaging components. Recently Pyrex® and quartz substrates have been etched with very high aspect ratios and very high surface smoothness using SF_6 and Ar/Xe gases [61–63]. The main difference between the etch processes developed for quartz micromachining processes and SiO_2 etch processes described in the earlier section pertain to the desired high etch rates and high-aspect-ratio etching of quartz. In this context the process relies upon ion bombardment to accelerate the etching process and fluorine-based gases are used to provide the reactive component for etching. The use of heavier Xe helps reduce the redeposition and more effectively removes any nonvolatile residues resulting in smoother surfaces with an average surface roughness of ~2 nm.

An inductively coupled plasma system is once again well suited for this application where the source generator driving the inductor coils creates the high density plasma and ion bombardment is independently controlled using a separate substrate RF generator. This enables excellent control over plasma density and kinetic energy of etchant ions. Low processing pressure and high plasma density, essentially resulting in high ionic current and greater radical flux density, improve the mass transfer rates of the reactant gases and the etch products in addition to being instrumental in the removal of nonvolatile residues. Nonvolatile residues are typically generated from the masking materials, the substrate holder, reaction chamber walls, or as reaction by-products. These result in micromasking causing high surface roughness (often referred to as grass), microtrenching, and formation of plateaulike structures. Additionally, the increased mean free path at low pressures improves the anisotropy of the etched features by minimizing the randomizing collisions between the radicals, ions, and other plasma species.

In the case of deep reactive ion etching of silicon dioxide (quartz or Pyrex®) a high Ar:SF_6 ratio is required to maintain low RMS surface roughness. Figure 7.15 shows the dependence of the etch rate and RMS surface roughness as a function of substrate RF power, chamber pressure, Ar, and SF_6 flow rate. In all cases the pressure in the chamber was maintained at 0.26 Pa throughout the flow ranges. The ICP source power was 2000 W and a substrate bias power of 475 W (Bias voltage of 80 V) was used in generating these results. From the graphs it can be seen that the best surface roughness of ~2 nm is obtained at high Ar flow rates, low chamber pressure, and high substrate power, corresponding to conditions dominated by physical sputtering of the material. The etch rate can be increased by increasing the SF_6 flow rate from 5 to 50 sccm from 0.54 to 0.74 μm/min, however, the surface roughness was found to degrade under these conditions to >100 nm. Pulse electroplated nickel was used as the etch mask layer and a selectivity of ~25:1 was obtained for SiO_2 etching under these conditions.

Figure 7.16 shows an SEM of a high-aspect-ratio feature etched in quartz using these conditions. Similar results were obtained by Li et al. while etching SiO_2 using Xe instead of Ar. The higher sputter yield of Xe gave a lower RMS surface roughness value as compared to Ar for the same mole fraction of the inert gas in SF_6. Although silicone grease or a small drop of Fomblin® oil can be used for mounting the quartz/glass substrates onto a 4 in. silicon carrier wafer, these materials cannot withstand the long process times and can leave the backside of the sample with

hard to remove, stubborn residues. Furthermore, these mounting materials do not provide a reliable and uniform thermal contact between the carrier wafer and the sample throughout the entire etch process. In order to avoid these problems, indium solder can be used for mounting the sample directly onto a silicon wafer. However, the mounting side of the SiO_2 sample needs to be coated with 20/80 nm of Cr/Au to provide a surface to which the solder can adhere. Of course if the sample is large enough it can be directly mechanically clamped or an electrostatic chuck can be used for the mounting of the sample. In all cases the backside of the chuck/substrate is cooled using helium gas maintained at the desired temperature.

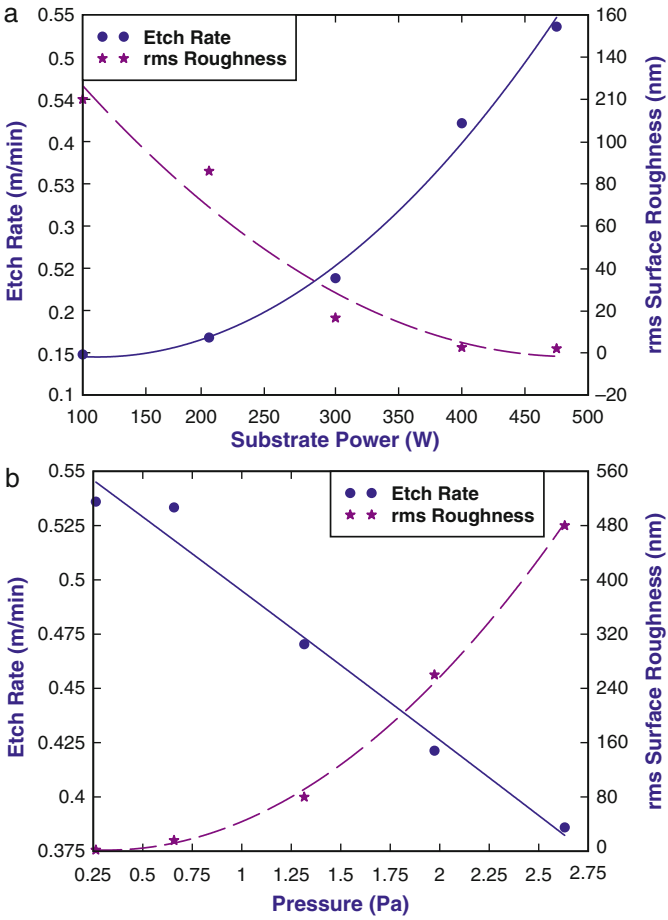

Fig. 7.15 Etch rate and surface roughness dependence of Pyrex® 7740 glass dependence as a function of: (**a**) substrate power in watts, (**b**) chamber pressure in Pa, (**c**) argon flow rate (sccm), and (**d**) SF6 flow rate (sccm). In the above graphs, all other etch parameters except the variable parameter are held constant at the following values: ICP power = 2 kW, substrate power = 475 W, chamber pressure = 0.26 Pa, argon flow rate = 50 sccm, SF6 flow rate = 5 sccm, and substrate temperature – 20°C

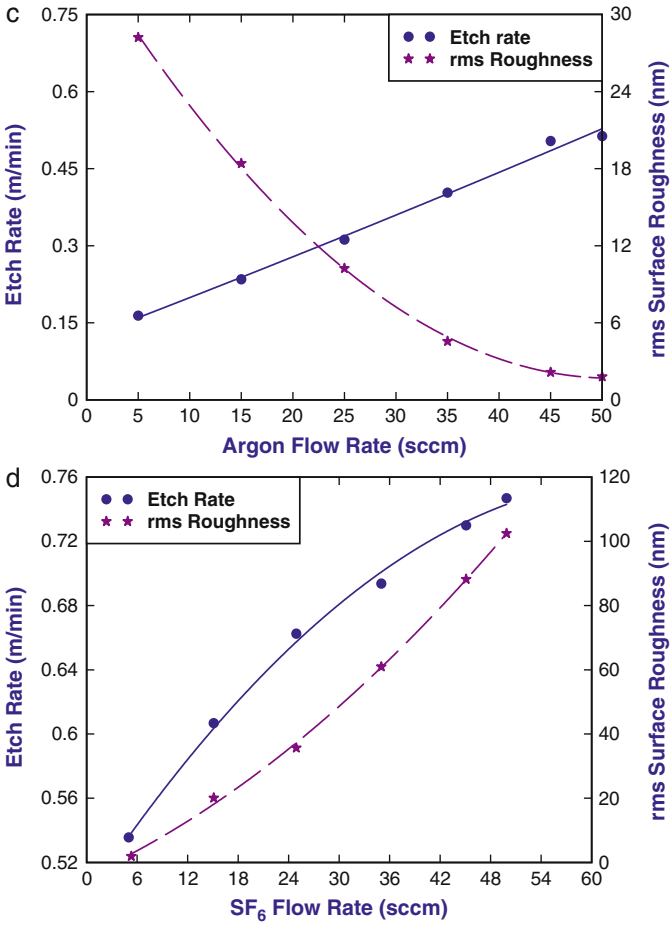

Fig. 7.15 (continued)

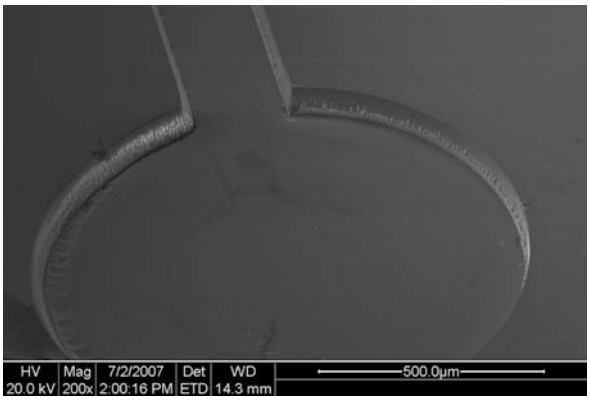

Fig. 7.16 SEM picture of a 60 μm deep etched feature in quartz. The sidewalls have been found to be roughened due to redeposition of nonvolatile etch products and mask erosion. Trenching is also observed at sharp corners in the feature, clearly indicating the dominant role of the ion-induced physical sputtering in the process [64] (Used with permission, copyright 2009, IEEE)

7.6.2 High-Aspect-Ratio Etching of Piezoelectric Materials

As seen in the case of SiO_2, most piezoelectric materials are primarily etched via physical sputtering with some assistance from chemical species in the process. The role of the chemical species is clearly observed in the comparative etching experiments of SiO_2 (quartz) and lithium niobate/tantalate [65]. In these experiments it is clearly observed that increasing the ratio of CF_4 to CHF_3 has no effect on the etch rate of lithium niobate/tantalate whereas it significantly increased the etch rate of SiO_2 where a regime of ion-enhanced chemical etching is obtained. Because the fluorides of lithium and tantalum oxide and niobium oxide are all nonvolatile, the reactive component of etching is an insignificant part of the etching process, which simply relies on the physical sputtering of the surface atoms due to the bombardment of energetic ions. Most piezoelectric etching recipes use inert gases as part of the etch gas composition [66]. This is mainly because inert gases provide plasmas with higher ion densities and ionization in comparison to the more electronegative chemical compounds (etch gases) and the higher sputter yield of inert gases is also much higher than other elements/molecules.

Figure 7.17 shows the SEM of lithium tantalate etched to a depth of ~8 μm at an etch rate of 0.2 μm/min. Surface roughness of <5 nm was obtained for this sample. The etching was performed in an inductively coupled plasma etcher with an SF_6/Ar flow rate ratio of 10/50 sccm and a substrate bias voltage of 75 V. The sample surface roughness is critically dependent on chamber pressure with low pressures offering a lower RMS surface roughness.

Aluminum nitride is typically etched using chlorine chemistries inasmuch as aluminum fluoride is an extremely stable and nonvolatile compound [67, 68]. Shul et al. have studied the comparative etching of GaN, InN, and AlN in chlorine and BCl_3 plasmas and were able to achieve etch rates of 0.23 μm/min for AlN in BCl_3 plasma with a small percentage additions of Ar/N_2 [69]. The etching characteristics of ZnO and etch selectivities of ZnO to SiO_2 in CF_4/Ar, Cl_2/Ar, and BCl_3/Ar plasma are reported by Woo et al. [70]. High etch rates of 0.12 μm/min have been reported. In several of the optimization reports of the etch processes, it was important to ensure that the photoresist mask was able to survive the piezoelectric material patterning.

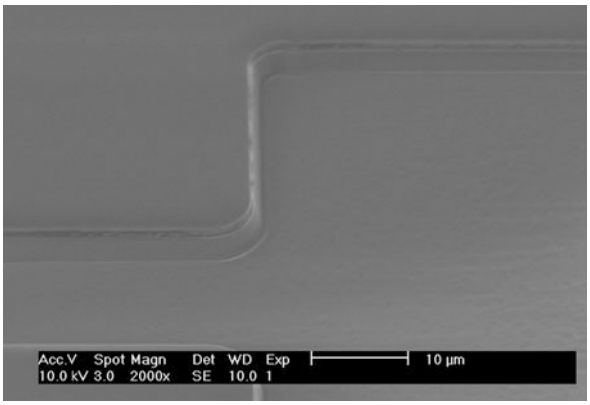

Fig. 7.17 SEM picture showing a high aspect ratio, smooth etching of lithium tantalate in 10:50 SF_6:Ar plasma. The chamber pressure was <0.66 Pa, with an ICP power of 2 kW and a substrate power of 400 W. A nickel hard mask was used to pattern the substrate

Often such optimization results in a compromise between the etch rate of the piezoelectric and mask selectivity because such etches are performed under high pressure and low substrate bias conditions. In cases where it is necessary to use a hard mask, typically electroplated nickel is used. Nickel provides a very high selectivity in fluorine plasmas where the selectivities of 20–30:1 for PZT etching have been reported [71]. PZT is typically etched in fluorine or chlorine plasma. Using SF_6 and Ar several groups have reported high-aspect-ratio etching of PZT. Using fluorine-based plasma chemistry, a maximum etch rate of 19 μm/hr for PZT-4 and 25 μm/hr for PZT-5A compositions have been reported [72]. This work also demonstrated a high-aspect-ratio etch (>5:1) on a 3 μm feature size.

Figure 7.18 shows the SEM image of the etched features for PZT. The square pillars created have a lateral dimension of 15 μm with a gap of 3 μm in between. The etched depth was ~15 μm. Almost vertical sidewalls with relatively smooth surfaces were obtained. 2–5 μm thick nickel on a Cr/Au was used as the hard mask. Selectivity of ~25:1 between the nickel hard mask and PZT was obtained. The availability of reliable, high-throughput, high-aspect-ratio micromachining processes has now created new opportunities for realizing novel MEMS devices from bulk piezoelectric materials such as quartz, lithium tantalate, aluminum nitride, PZT, and single-crystal PMN-PT. Table 7.4 summarizes the dry etching of various piezoelectric materials.

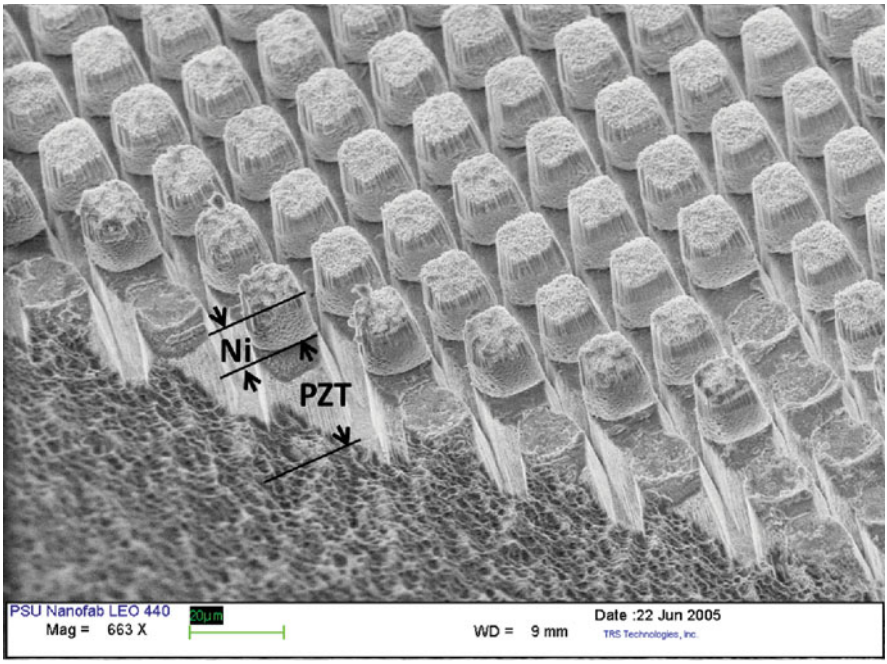

Fig. 7.18 SEM image of the etched feature in PZT ceramic substrate with a minimum feature size of 3 μm. Almost vertical sidewalls were obtained [73] (Used with permission, copyright 2009, Institute of Physics)

Table 7.4 Summary of the dry etching characteristics of various piezoelectric materials [73]

Material	Etch gas(es)	Pressure (Pa)	RF frequency (MHz)/power (W)	Etch rate (μm/min)	Comments
Quartz [74]	CF_4	355	27 MHz	4	Nonlithographic plasma confinement method was used
Quartz [61]	SF_6/Xe	0.59	13.56/90	0.4	ICP source with 150 W power was used to obtain highly smooth surface
Pyrex 7740/ quartz [63]	SF_6/Ar	0.26	13.56/475	0.54	ICP source with 2 kW power was used. Highly smooth surface with $R_a = 1.97$ nm. Similar rates were obtained for quartz etching as well
$LiNbO_3$/ $LiTaO_3$ [65]	CHF_3/CF_4	6.58	13.56/350	~0.01	Etching proceeds mainly via physical sputtering
AlN [75]	Cl_2/Ar	0.66	13.56 MHz	0.75	ICP Source with 500 W power was used. Etching proceeds by physical bombardment. No significant etching was observed below a threshold substrate voltage of −50 V. The paper also reports etching GaN and AlGaN. Another good reference is [76]
AlN [67]	BCl_3/Cl_2/Ar	0.66	13.56 MHz	0.4	
ZnO [77]	$SiCl_4$/Ar	23	13.56/0.56 W/m^2	0.027	Additional references on ZnO etching are available [70, 78]. Typically etching is found to proceed via physical bombardment
ZnO [79]	C_2H_6/H_2/Ar	0.66	13.56/300	0.05	
PZT (Bulk) [71]	SF_6	0.66	13.56/200	0.12	In [71] pure SF_6 gave the best etch rate but the angle was shallow which could be improved by Ar addition but at the cost of etch rate. The recipe used in [72] mainly uses physical sputtering, however, aspect ratios of >5:1 were obtained
PZT [80]	CF_4/80%Ar	1.97	13.56/700	0.143	
PZT [72]	SF_6:Ar::1:10	0.66	13.56/475	0.42	

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7.7 Etching of Compound Semiconductors

Almost all III-V compound semiconductors and their heterostructures can be etched in chlorine and bromine plasmas. More recently CH_4/H_2-based dry etching processes have also been explored. The three main considerations in the etching of III-V semiconductor structures include (i) smoothness of etched features inasmuch as many of these structures are used in optical devices, (ii) low damage to the semiconductor layer, and (iii) conflicting requirement of high selectivity as well as equirate etching of the heterostructure layers depending on the particular process step. Typically group V halides have very high vapor pressure and therefore are readily removed in the dry etching process. However, group III halides are not so volatile. For example, the boiling points of $AlCl_3$ is 262°C, $GaCl_2$ is 535°C, $GaCl_3$ is 201°C, InCl is 608°C, and $InCl_3$ ~600°C. Furthermore, group III fluorides are extremely stable compounds and do not volatilize readily; for example, the boiling point of AlF_3 is 1291°C, GaF_3 is ~1000°C, and InF_3 is >1200°C. Thus, purely chemical etching of GaAs can be done in chlorine plasma but the same process does not achieve good etching results for InP due to the involatility of $InCl_3$. Furthermore, the addition of fluorine to chlorine plasma can be used to obtain high selectivity during the etching of GaAs on AlGaAs. Fluorine-containing plasmas also provide a means for selectively etching silicon nitride and silicon dioxide masks on III-V compound semiconductors.

The most commonly used masking materials for etching of III–V compounds include metals such as Cr, Ni, Ti, Al, chemical vapor deposited dielectrics such as Si_3N_4, SiO_2, and novolac resin-based photoresists and electron beam photoresists. Metals exhibit the highest selectivity for these etching applications; however, the grain size of the deposited film determines the sidewall roughness and limits the achievable smoothness. The smoothest etch results have been achieved by using hardbaked, multilayer, novolac-resin-based photoresists. In general polymethyl methacrylate (PMMA) e-beam resist is found to exhibit poor etch resistance in comparison to the novolac resists. However, positive tone e-beam resists such as ZEP-520A and negative tone SAL-601 have been found to offer good etch resistance. Care has to be taken to prevent any erosion of mask which might result in roughening of the top part of the etched features.

7.7.1 Case Study: Etching of GaAs and AlGaAs

In this section, various GaAs gas chemistries are briefly reviewed. Specific advantages for each process are briefly indicated. Table 7.5 lists the etch rate of some of the commonly used masking materials in GaAs etching [81].

Reactive Etching in $SiCl_4$ Plasma: Etching at moderate pressures of 2.63–13.15 Pa is chemical in nature. Typically at moderate pressure, etching of GaAs in chlorine and bromine plasma is rapid, spontaneous, and crystallographic as seen in Fig. 7.19 [37]. The relative chemical etch rates of the various etch planes in GaAs are: $(111)_{As\text{-}rich} > (100) > (110) > (111)_{Ga\text{-}Rich}$. Silicon tetrachloride is not as

Table 7.5 Commonly used masking materials compatible with etching III–V semiconductors in chlorine plasma[a]

Material	Etch rate (nm/min)	GaAs: material etch rate ratio (selectivity)
GaAs	28.33	1
Au-Pd	2.5	11.3333
Au	1.75	16.19048
Glass (SiO_2)	0.708333	40
Cr	1.25	22.66667
Ni	0.5	56.66667
Ni-Cr	0.833333	34
AZ-1350 J (Photoresist)	2.916667	9.714286

[a]These etch rates were obtained in 90% Ar/10%BCl_3 plasma chemistry obtained in diode RIE set-up operated at 50 W RF power (300 V bias), 1.97 Pa pressure [81]. Used with permission, copyright 1987, American Vacuum Society

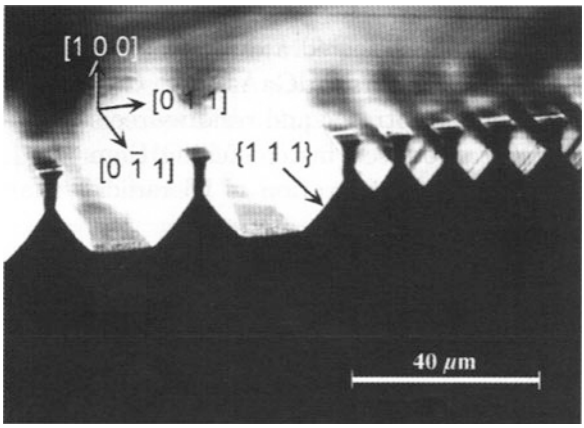

Fig. 7.19 Etch characteristics of GaAs in $SiCl_4$ reactive ion plasma (2.63 Pa, 150 W, 200 mW/cm^2). The high pressure and low power etch results in the emergence of the various crystallographic facets [37] (Used with permission, copyright 2000, Springer)

corrosive as pure Cl_2 gas and the plasma leaves no nonvolatile residues and is a clean process well suited for crystallographic dry etching.

Reactive Ion Etching in Cl_2 Plasma: Smooth and vertical trenches are obtained due to the high DC-bias ion bombardment. Aspect-ratio-dependent etch rate is clearly observed. In order to avoid any roughness or grass formation due to microloading, this etch must be performed at very low pressures in the range of 0.066–0.66 Pa. The addition of BCl_3 and Ar can result in very smooth trench formation [82]. Figure 7.20 shows an SEM picture of a high-aspect-ratio, smooth etch profile obtained in GaAs using chlorine plasma [37].

Reactive Ion Etching in $BCl_3 + Ar$ Plasma: Using this etching chemistry at low pressures and high Ar%, equirate etching of GaAs and AlGaAs can be obtained. An equi-etch rate of 280 nm/min for 50 W, 1.97 Pa, and 90% Ar has been reported [81]. Addition of 10% oxygen to this mixture provided a selectivity of ~5:1, however, at a remarkably slow etch rate of 10 nm/min for GaAs.

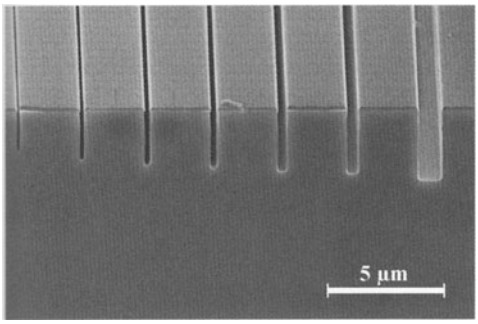

Fig. 7.20 Etch characteristics of GaAs in Cl_2 in an inductively coupled plasma reactive ion etcher (0.2 Pa, 150 W, ~500 V dc bias). Highly anisotropic etch showing width dependent etch rate is clearly observed. It is possible to obtain smooth etch morphologies using low pressures (below 0.1 Pa) range [37] (Used with permission, copyright 2000, Springer)

Reactive Ion Etching in $SiCl_4$ and SiF_4 Plasma: This etch chemistry provides a high selectivity GaAs etch against AlGaAs. The use of separate chlorine and fluorine containing gases as opposed to CCl_2F_2 (CCl_2F_2 is an ozone depleting chlorofluorocarbon the use of which currently conflicts with "Montreal Protocol".) affords greater flexibility in controlling the Cl/F ratio. In addition, no polymer formation is observed in this gas mixture. Formation of AlF_3 results in the etch stopping mechanism for AlGaAs in fluorine containing plasma. Figure 7.21 shows the selectivity of GaAs over AlGaAs as a function of the percentage of $SiCl_4$ [83]. Clearly preferential high selectivity of GaAs over AlGaAs is obtained for aluminum-rich GaAs compositions and at low $SiCl_4$ concentrations.

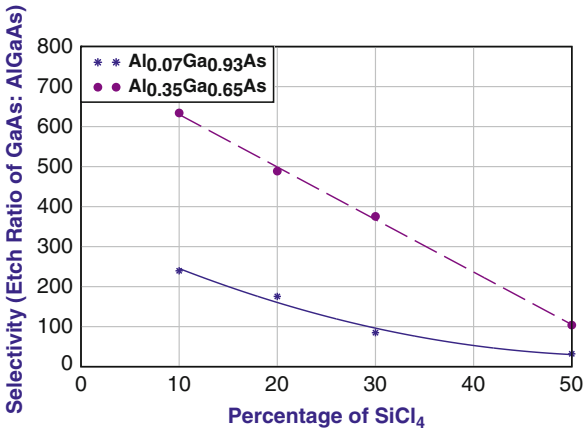

Fig. 7.21 Selectivity of GaAs over AlGaAs as a function of %$SiCl_4$ in $SiCl_4 + SiF_4$ plasma. The data were obtained for a RIE plasma at a pressure 7.89 Pa and a dc bias of −60 V and offer a selectivity in excess of 500:1 for $Al_{0.35}Ga_{0.65}As$ [83] (Used with permission, copyright 1990, American Vacuum Society)

Reactive Ion Etching in CH_4 and H_2 *Plasma:* Hydrogen–alkane mixtures can also be used to etch GaAs [84, 85]. However, the etch rates in this case are

much lower than those achieved using chlorine plasma. In general, hydrogen-based etches result in very smooth surface morphologies and are not much affected by water vapor contamination allowing for the use of nonload locked RIE machines. Furthermore, hydrogen plasma has been demonstrated to result in the least damage to the substrate [84]. The etching itself is considered to occur through the formation of AsH_3 and $(CH_3)_3Ga$ as volatile reaction products. Figure 7.22 shows the dependence of GaAs etch rate as a function of percentage of CH_4 in H_2 plasma [84].

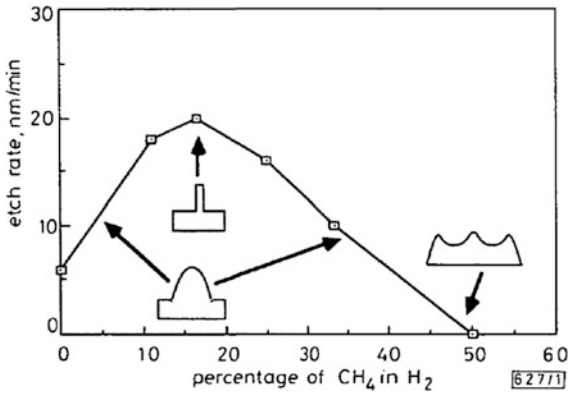

Fig. 7.22 Etch rate of GaAs as a function of $\%CH_4$ in H_2 plasma. The data were obtained for a RIE plasma at a pressure 1.84 Pa and a power density of 0.4 W/cm^2. The reduction in the etch rate with increasing methane is due to the formation of an inert polymer layer. The maximum etch rate is found to increase to a value of ~180 nm/min when the etch is performed at a pressure of 5.26 Pa and 0.75 W/cm^2 [84] (Used with permission, copyright 1987, The Institution of Engineering and Technology, IET)

7.7.2 Case Study: Etching of InP, InGaAs, InSb, and InAs

Reactive Ion Etching in Cl_2 Plasma: Indium phosphide related materials have been successfully etched using chlorine plasmas [86–88]. However, owing to the nonvolatile nature of $InCl_3$, etches performed at room temperature including ion bombardment have been found to exhibit low etch rates and rough morphologies. Etches performed at elevated temperatures of >140°C show an appreciable increase in the etch rate of >2 μm/min due to the increased volatilization of $InCl_x$. As the temperature is increased to 200–250°C, enhanced energy-driven anisotropy of the etched features has been observed. However, chemically assisted ion beam etching performed at high temperatures is prone to microloading-related roughness arising due to the sputter deposition of nonvolatile residues from hard masks, etch chamber, and substrate chuck.

Silicon dioxide and photoresist have been found to be suitable etch masks while graphite and silicon have been found to be suitable for the substrate chuck materials [89]. Ko et al. have reported the etching of smoothly etched vias in InP using

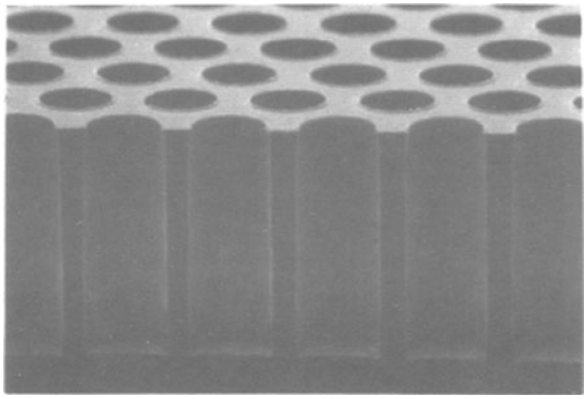

Fig. 7.23 30 μm wide, 92 μm deep via holes etched in InP using Cl_2/Ar (50% Cl_2) plasma. An ECR source driven at 500 W along with 100 W RF substrate power at 0.26 Pa and 20°C temperature was used. Local surface heating due to ion bombardment of the substrate is considered to provide the elevated temperature [90] (Used with permission, copyright 1995, The Electrochemical Society)

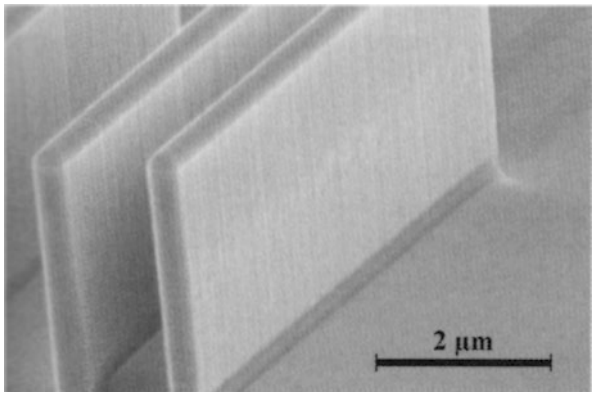

Fig. 7.24 0.4 μm wide slabs etched in InP using $Cl_2/H_2/N_2$/Ar in an ICP-RIE. A substrate temperature of 250°C, pressure of 0.26 Pa were used [37] (Used with permission, copyright 2000, Springer)

a ECR-RIE with Cl_2/Ar as the etch gases (see Fig. 7.23) [90]. A flow ratio of 2:1 of Cl_2: Ar has been found to result in very smooth etched surface morphologies. Addition of hydrogen or HCl to the plasma has been shown to improve the etched surface morphologies. The likely effect of the addition of hydrogen in chlorine plasma is the effective removal of phosphorus as PH_3. Figure 7.24 shows a very smooth and vertical etch surface obtained using $Cl_2/H_2/N_2$/Ar in an ICP-RIE [37].

Etching InP in CH_4/H_2 Plasma: Alkane–hydrogen etching of InP provides an alternative to etching using halogen gases. Although the etch rates are low in the range of 20–60 nm/min, the etch morphologies are extremely smooth and the damage due to etching is limited to less than 4 nm into the surface [91]. In alkane–hydrogen plasma, phosphorus is removed via the formation of PH_3 whereas indium is removed via the formation of $(CH_3)_3In$. Due to the high volatility of PH_3, the

etched surface is found to be In-rich. CH_4:H_2 ratio in the range of 0.1–0.4 is typically used. Higher values of CH_4 lead to polymer deposition on the surfaces.

Figure 7.25 shows the etch profile obtained in $CH_4/H_2/Ar$ RIE plasma for an InP/InGaAsP mirror. An overhang and positive etch slope can be seen due to the buildup of polymer on the sidewall of the etched feature. Cyclically alternating between O_2 plasma to clear the polymer buildup and etch step using CH_4/H_2 solves this problem at the cost of greater process complexity. Alternatively a small amount of O_2 can be continuously added to the CH_4/H_2 plasma to prevent the buildup of the polymer on the sidewalls [92]. A comparison of these methods and their advantages has been presented by Schramm et al. [93].

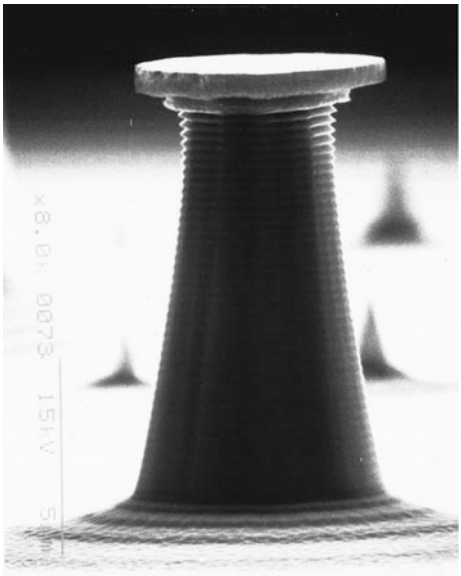

Fig. 7.25 A 45 period, gas source MBE grown InP/InGaAsP mirror etched using $CH_4/H_2/Ar$ plasma under conditions: pressure = 6.57 Pa, substrate bias = 500 V, $CH_4/H_2/Ar$: 4/20/10 sccm [93] (Used with permission, copyright 1997, The American Vacuum Society)

7.8 Case Study: Ion Beam Etching

Ion-beam etching is a purely physical, plasma-based etch process and excellent reviews are available [94, 95]. During milling, the sputtering of material occurs by momentum transfer between the impinging ions and the surface. To first order, the etch rate, *ER*, is proportional to the product of the ion flux density *F*, and the sputter yield S(θ), and can be given as [94]

$$ER(\theta, IE) \propto F\cos(\theta)S(\theta, IE),$$

where θ is the angle of incidence of the ion beam and *IE* is the energy of the ion beam. In general, sputter yield is a function of the angle of incidence, the atomic

weight and incident energy of the ions, and the target material. Most materials exhibit an increase in sputter yield with θ, up to a maximum at about 40°–60°, followed by a sharp drop. The overall increase in etch rate for oblique angles of incidence is because the increased sputter yield generally exceeds the reduction in flux density. The sputter yield also varies with ion energy exhibiting an exponential increase between 20 and 100 eV, followed by a linear increase up to about 500 eV, and finally increasing more gradually up to a saturation point above 10 keV [94].

The process is highly anisotropic so undercutting is generally not a concern, and very high resolutions with features of better than 100 Å have been demonstrated. The physical nature of the process means that all materials can be etched, allowing a single-step approach for patterning multimaterial film stacks. However, the major drawback of ion milling is the poor selectivity, and there is typically less than a tenfold difference in the etch rate between materials. The etch depth is therefore controlled by timing, or with mask layer thicknesses adjusted to compensate for the low selectivity. Table 7.6 lists the etch rates observed in milling experiments using an Oxford Series-300 dual-source etch system with a 15 cm Kaufman-type ion source. All tests were performed using argon at a pressure of 0.026–0.039 Pa. The use of oblique angle increases the etch rate as well as avoids trenching and redeposition problems.

Table 7.6 Ion-beam etch rates for some commonly ion-milled materials[a]

Material	Current density (mA/cm^2)	Voltage (V)	Angle (°)	Etch rate (nm/min)
PZT	0.42	1000	0	14
PZT	0.45	1000	45	24
Platinum	0.42	1000	0	30
Platinum	0.45	1000	45	34
Si_xN_y	0.45	1000	45	28
Zirconia	0.45	1000	45	20

[a]Milling conditions: 0.026–0.039 Pa [26]

The addition of a partial pressure of oxygen during ion-beam etching has been noticed to reduce the sputter yield of certain metals that oxidize easily [96]. Figure 7.26a shows the etch rate as a function of oxygen concentration for various materials. The effect is likely the result of competition at the surface between the chemisorption of oxygen, and the sputtering removal of both the oxygen and metal atoms. This method can be used as a means to increase the selectivity of a mask over nonreactive materials. This is well illustrated for patterning complex oxides such as lead zirconate titanate (PZT), where reactive sputtering in oxygen ambient has little effect on its milling rate, however, the ion milling etch rates of metals such as chrome, titanium, and aluminum are significantly reduced due to harder to etch metal–oxide formation (see Fig. 7.26b). Figure 7.27a shows PZT etching with nearly vertical sidewalls achieved using a titanium mask layer. Using this technique it is possible to pattern thin PZT features down to ~1 μm as shown in Fig. 7.27b.

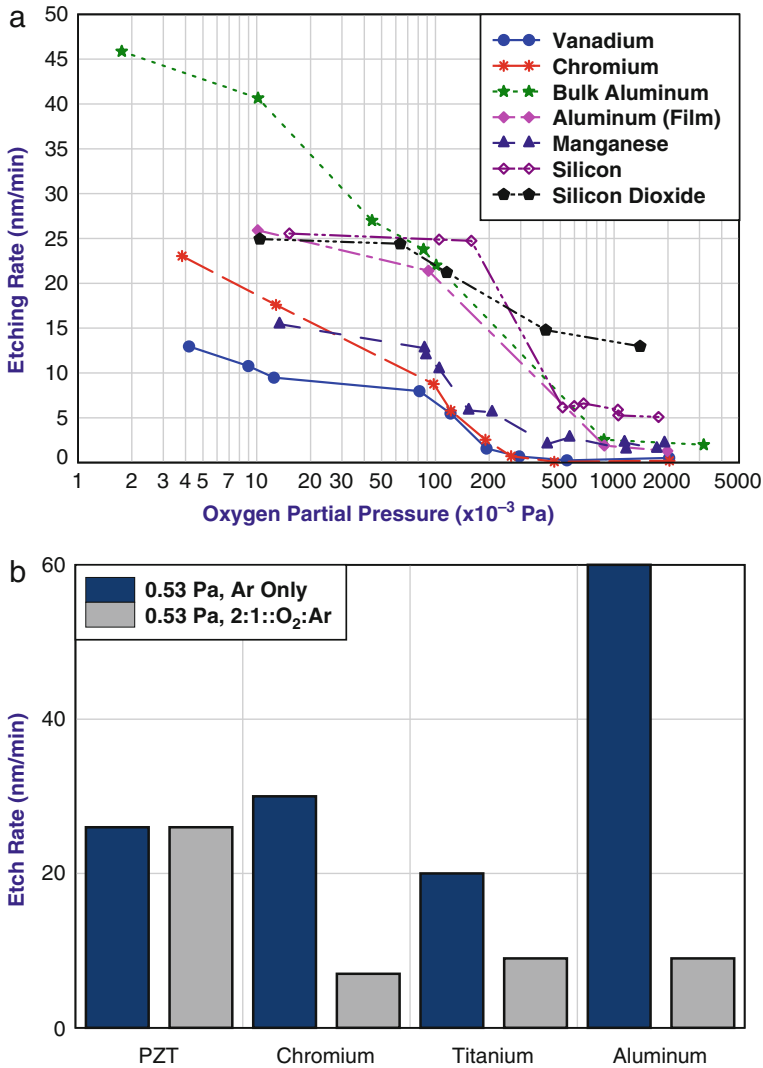

Fig. 7.26 (**a**) Etch rate of various materials with the addition of oxygen at 1 keV and 0.6 mA/cm^2 current density [96] (Used with permission, copyright 1973, Springer); (**b**) ion milling rates for sputtered metals and sol-gel deposited PZT with and with without oxygen using 0.45 mA/cm^2 current density, 1 kV acceleration potential, angle of 45° and a pressure of 0.53 Pa

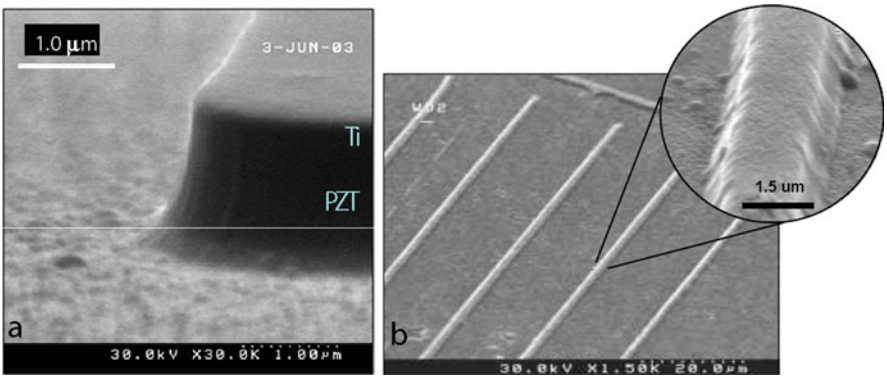

Fig. 7.27 Ion-beam etching PZT with hard masks in O_2, showing excellent resolution: (**a**) PZT patterned using titanium hard mask, and (**b**) using chromium hard mask [26]

7.9 Summary

To summarize, dry etching processes are at the heart of MEMS fabrication and materials technology. The use of plasma creates a reactive gaseous environment in which various substrate materials can be removed as volatile reaction products. Most of the etching processes are based on various halogen chemistries. The overall etch results depend upon the specific material, etch chemistry, etch equipment, and various other parameters including masking materials, history of the chamber, and so on, thus it is nearly impossible to give specific process recipes that can be reliably reproduced across various laboratories or facilities. What is important is to realize the determining factors of the overall etch characteristics in a given process. In Table 7.7, process recipes for etching various metals, semiconductors, and dielectrics are listed. These are not intended as a list of the current state-of-the-art numbers, but to provide the reader with nominal etch-related parameters to be expected on three different but typical pieces of etch equipment. Recent developments in high vacuum technology with high-throughput turbomolecular pumps, high-density and stable inductively coupled plasma sources, fast switching, precision mass flow controllers, and process control instrumentation have enabled the design and manufacturing of next-generation etching equipment. However, challenges remain in the development of high-throughput, high-definition etching processes, especially for high-aspect-ratio etching of ceramic materials such as complex oxides encountered in piezoelectric and magnetic materials, and wideband gap semiconductors. In addition, challenges lie ahead as top-down fabrication techniques are rapidly approaching the 10 nm scale with high-aspect-ratio etch requirements.

Table 7.7 Typical plasma etch recipes including gas chemistry used, etch rates obtained, and equipment type

Material	Pressure (Pa)	Source power (W)	Substrate power (W)	Gases	Etch rate (nm/min)	Comments
Metals						
Aluminum	1.32	800	175	Cl_2: 75	100	Tool: Applied Materials DPS System, Mask: PR 3012
Platinum	1.32	800	175	Cl_2: 75 sccm	100	Tool: Applied Materials DPS System, Mask: PR 3012
Chromium	10.5	75	–	Cl_2: 60 sccm, O_2: 20 sccm	10	Tool: Plasma Therm PT 720 Mask: ZEP-530 (Selectivity: PR:Cr::3:2) Note: 60% over etch recommended for small features (sub 750 nm)
Semiconductors						
Silicon	1.32	1000	150	Cl_2: 20 sccm	490–520	Tool: Applied Materials DPS System, Mask: SiO_2 Selectivity: Si:SiO_2::8:1
Silicon	1.32	175	–	Cl_2: 20 sccm	60	Tool: Plasma Therm PT 720, Mask: Cr, Selectivity: Si:Cr :: 10:1. Process relies on oxidation of chromium for good selectivity
Silicon	26.3	200	–	SF_6: 50 sccm	300–400	Tool: Plasma Therm PT 720, Mask: SiO_2, Selectivity: Si:SiO_2 :: 60:1
Gallium arsenide	0.132	200	–	Cl_2: 20 sccm	500	Tool: Plasma Therm PT 720, Mask: PR, Selectivity: GaAs:PR :: 20:1, Mask: Cr, Selectivity: GaAs:Cr :: 50:1
AlGaAs	1.32	250	–	Cl_2: 29 sccm	400	Tool: Plasma Therm PT 720, Mask: PR, Selectivity: AlGaAs:PR :: > 10:1

Table 7.7 (continued)

Material	Pressure (Pa)	Source power (W)	Substrate power (W)	Gases	Etch rate (nm/min)	Comments
Dielectrics						
Silicon dioxide	1.97	–	100	CHF_3: 75 sccm CF_4: 30 sccm	37–40	Tool: Applied Materials MERIE System, Magnetic Field: 60 gauss
Silicon dioxide	13.2	200	–	CF_4: 45 sccm O_2: 5 sccm	110	Tool: Plasma Therm PT 720 Mask: PR 1813
Silicon nitride	1.97	–	50	CHF_3: 25 sccm	10	Tool: Applied Materials MERIE System, Magnetic Field: 60 gauss
Silicon Nitride	26.3	300	–	CF_4: 40 sccm O_2: 8 sccm Ar: 7 sccm	167	Tool: Plasma Therm PT 720 Mask: PR 1813, Selectivity: < 1
Quartz	6.57	–	200	CHF_3: 45 sccm Ar: 140 sccm	46–49	Tool: Applied Materials MERIE System, Magnetic Field: 22.5 gauss, Mask: Chromium, Selectivity: Quartz:Cr :: 12:1
SilSpin®	2.63	–	25	O_2: 30 sccm CHF_3: 12 sccm	130	Tool: Applied Materials MERIE System, Magnetic Field: 45 gauss, Cathode temperature: 3°C
Polyimide	2.37	–	150	O_2: 90 sccm	682	Tool: Applied Materials MERIE System, Magnetic field: 45 gauss, Cathode temperature: 3°C, Mask: Cr or Ni Hard Mask
Polypyrrole	5.26	350	–	O_2: 30 sccm	300	Tool: Plasma Therm PT 720 Mask: PR 1813, Selectivity: Polypyrrole:PR ::1:1
Benzocyclobutene (BCB)	26.3	200	–	O_2: 45 sccm Ar: 5 sccm CF_4: 10 sccm	1000	Tool: Plasma Therm PT 720, Process used for BCB etch back

Source: The Pennsylvania State University node of the National Nanofabrication Infrastructure Network
Note: The PlasmaTherm PT-720 is a parallel plate etcher (i.e., diode type etcher), AMAT-MERIE is a magnetically enhanced reactive ion etcher and uses a magnetic field for increasing the plasma density, and AMAT-DPS is a high-density inductively coupled plasma etcher in which the plasma power and substrate power are independently controlled

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References

1. R.J. Shuhl, S.J. Pearton: Handbook of Advanced Plasma Processing Techniques, p. 653 (Springer, Heidelberg, 2000)
2. S.M. Rossnagel, W.D. Westwood, J.J. Haber: Handbook of Plasma Processing Technology: Fundamental, Etching, Deposition and Surface Interactions, p. 546 (William Andrew, New York, NY, 1991)
3. D.M. Manos, D.L. Flamm: Plasma Etching: An Introduction, p. 476 (Academic, San Diego, CA, 1989)
4. M. Elwenspoek, H.V. Jansen: Silicon Micromachining (Cambridge University Press, Cambridge, 1998)
5. M. Madou: Fundamentals of Mirofabrication (CRC Press, Boca Raton, FL, 1997)
6. G.S. Oehrlein, W.D. Westwood, J.J. Haber: Reactive Ion Etching, in Reactive Ion Etching: Handbook of Plasma Processing Technology, pp. 196–206 (Rossnagel, S.M. (Ed.) Noyes, New York, NY, 1990)
7. G.C. Schwartz, P.M. Schaible: Reactive ion etching of silicon, J. Vac. Sci. Technol. 16, 410–413 (1979)
8. X.Y. Li, P.J. French, P.M. Sarro, R.F. Wolffenbuttel: Fabrication of a Single Crystalline Silicon Capacitive Lateral Accelerometer Using Micromachining Based on Single Step Plasma Etching. Proceedings of the IEEE MEMS Conference, Amsterdam, The Netherlands, pp. 398–403, 1995.
9. B. Diem, P. Rey, S. Renard, S.V. Bosson, H. Bono, F. Michel, M.T. Delaye, G. Delapierre: SOI 'SIMOX'; from bulk to surface micromachining, a new age for silicon sensors and actuators, Sens. Actuators A Phys. 46, 8–16 (1995)
10. K.T. Sung, S.W. Pang: Etching of Si with Cl_2 using an electron cyclotron resonance source. 39th National Symposium of the American Vacuum Society, Chicago, IL, pp. 1206–1210 (1993)
11. W.H. Juan, J.W. Weigold, S.W. Pang: Dry etching and boron diffusion of heavily doped high-aspect ratio Si trenches. Micromachining and Microfabrication Process Technology II, Austin, TX, pp. 45–55 (1996)
12. C.J. Mogab: The loading effect in plasma etching, J. Electrochem. Soc. 124, 1262–1268 (1977)
13. D.L. Flamm: Introduction to Plasma Chemistry, in Plasma Etching: An Introduction, pp. 91–183 (Manos, D.M., Flamm, D.L. (Eds.) Academic, San Diego, CA, 1989)
14. G.S. Hwang, K.P. Giapis: On the origin of the notching effect during etching in uniform high density plasmas, J. Vac. Sci. Technol. B Microelectron, Nanometer Struct. 15, 70–87 (1997)
15. K.P. Giapis: Fundamentals of Plasma Process-Induced Charging and Damage, in Handbook of Advanced Plasma Processing Techniques, pp. 257–308 (Shuhl, R.J., Pearton, S.J. (Eds.) Springer, Berlin, 2000)
16. B. Chapman: Glow Discharge Processes: Sputtering and Plasma Etching (Wiley-Interscience, New York, NY, 1980)
17. M. de Boer, H. Jansen, M. Elwenspoek: The Black Silicon Method V: A Study of The Fabricating of Movable Structures for Micro Electromechanical Systems in Solid-State Sensors and Actuators, 1995 and Eurosensors IX. Transducers ′95. The 8th International Conference, pp. 565–568 (1995).

18. H. Muenzel, G. Benz, A. Schilp, F. Laermer: Processing silicon in a plasma etch system (fabrication of free-standing silicon structures) Patent DE4420962, GB2,290,413, Office, G.P., Germany (1995)
19. K.A. Shaw, Z.L. Zhang, N.C. MacDonald: SCREAM I: A single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures, Sens. Actuators A Phys. 40, 63–70 (1994)
20. D.E. Ibbotson, J.A. Mucha, D.L. Flamm, J.M. Cook: Plasmaless dry etching of silicon with fluorine-containing compounds, J. Appl. Phys. 56, 2939–2942 (1984)
21. F.I. Chang, R. Yeh, G. Lin, P.B. Chu, E. Hoffman, E.J.J. Kruglick, K.S.J. Fister, M.H. Hecht: Gas-Phase Silicon Micromachining with Xenon Difluoride. Proceedings of the SPIE, Austin, TX, 1995, Vol. 2641, pp. 117–128 (1995).
22. X.-Q. Wang, X. Yang, K. Walsh, Y.-C. Tai: Gas-Phase Silicon Etching with Bromine Trifluoride. Proceedings of the International Conference on Solid-State Sensors and Actuators - Transducers 97, Chicago, Vol. 2, p. 1505 (1997).
23. Y. Saito, O. Yamaoka, A. Yoshida: Plasmaless etching of silicon using chlorine trifluoride, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 9, 2503–2506 (1991)
24. G.T.A. Kovacs, N.I. Maluf, K.E. Petersen: Bulk micromachining of silicon, Proc. IEEE 86, 1536–1551 (1998)
25. K.R. Williams, R.S. Muller: Etch rates for micromachining processing, J. Microelectromech. Syst. 5, 256–269 (1996)
26. S.J. Gross: Micromachined switches and cantilever actuators based on piezoelectric lead zirconate titanate (PZT), Ph.D. Thesis, Electrical Engineering, The Pennsylvania State University, University Park, pp. 66–70 (2004).
27. C. Leinenbach, H. Seidel, T. Fuchs, S. Kronmueller, F. Laermer: A novel sacrificial layer technology based on highly selective etching of silicon-germanium in CLF_3 in Micro Electro Mechanical Systems, 2007. MEMS IEEE 20th International Conference, pp. 65–68 (2007).
28. A. Hoechst: Plasmaless Dry Etching of Silicon Using Chlorine Trifluoride. Investigation of Etching Mechanism and Applications in Microsystem Technologies, Ph.D. Thesis, pages 118, University of Tubingen, Germany, (2007).
29. A. Hoechst, F. Fischer, G. Kirbach, A. Urban, V. Becker, M. Irmscher, H. Sailer, D.P. Kern: Investigations on the mechanism of silicon etching with chlorine-trifluoride, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 23, 1936–1942 (2005)
30. O.A. Popov: High Density Plasma Sources (Noyce Publications, Park Ridge, NJ, 1995)
31. D.L. Flamm, K.G. Herb: Plasma Etching Technology – An Overview, in Plasma Etching: An Introduction, pp. 1–89 (Manos, D.M., Flamm, D.L. (Eds.) Academic, San Diego, CA, 1989)
32. F. Laermer, A. Schilp, K. Funk, M. Offenberg: Bosch deep silicon etching: improving uniformity and etch rate for advanced MEMS applications in Micro Electro Mechanical Systems, 1999. MEMS/99. 12th IEEE International Conference, pp. 211–216 (1999)
33. V. Becker, F. Laermer, A. Schilp, T. Beck: Plasma Etching Installation Patent 6,531,031, Office, U.S.P., US (2003)
34. K. Breitschwerdt, V. Becker, F. Laermer, A. Schilp: Device and Method for Etching a Substrate by using an Inductively Coupled Plasma Patent 6,709,546 and 7,094,706, Office, U.S.P., US (2004)
35. B. Charlet, L. Peccoud: Process for Etching with Gaseous Plasma, Patent EP-0359777, Office, E.P., France (1992)
36. B. Charlet, L. Peccoud, T. Dupeux: Microusinage du silicium dans un reacteur GIR assiste par un plasma micro-ondes. Proceedings 6th Colloque Int. sur la Pulverisation Cathodique et ses Applications, CIP 85, Nice, France, pp. 183–188 (1987).
37. C. Youtsey, I. Adesida: Plasma Processing of III-V Materials, In Handbook of Advanced Plasma Processing Techniques, pp. 459–506 (Shuhl, R.J., Pearton, S.J. (Eds.) Springer, Berlin, 2000)
38. J.W. Coburn, H.F. Winters: Ion- and electron-assisted gas-surface chemistry – An important effect in plasma etching, J. Appl. Phys. 50, 3189–3196 (1979)

39. J.W. Coburn, H.F. Winters: Plasma etching – A discussion of mechanisms, J. Vac. Sci. Technol. 16, 391–403 (1979)
40. R.A.H. Heinecke: Control of relative etch rates of SiO_2 and Si in plasma etching, Solid-State Electron. 18, 1146–1147 (1975)
41. H.W. Lehmann, R. Widmer: Profile control by reactive sputter etching, J. Vac. Sci. Technol. 15, 319–326 (1978)
42. L.M. Ephrath: Selective etching of silicon dioxide using reactive ion etching with CF_4-H_2, J. Electrochem. Soc. 126, 1419–1421 (1979)
43. G.S. Oehrlein, S.W. Robey, J.L. Lindstrom, K.K. Chan, M.A. Jaso, G.J. Scilla: Surface modifications of electronic materials induced by plasma etching, J. Electrochem. Soc. 136, 2050–2057 (1989)
44. D.L. Flamm, V.M. Donnelly, J.A. Mucha: The reaction of fluorine atoms with silicon, J. Appl. Phys. 52, 3633–3639 (1981)
45. K. Yamakawa, M. Hori, T. Goto, S. Den, T. Katagiri, H. Kano: Ultrahigh-speed etching of SiO_2 with ultrahigh selectivity over Si in microwave-excited non equilibrium atmospheric pressure plasma, Appl. Phys. Lett. 85, 549–551 (2004)
46. F.H.M. Sanders, J. Dieleman, H.J. B. Peters, J.A.M. Sanders: Selective isotropic dry etching of Si_3N_4 over SiO_2, J. Electrochem. Soc. 129, 2559–2561 (1982)
47. D.E. Ibbotson, J.A. Mucha, D.L. Flamm, J.M. Cook: Selective interhalogen etching of tantalum compounds and other semiconductor materials, Appl. Phys. Lett. 46, 794–796 (1985)
48. F. Laermer, A. Schilp: Method of Anisotropically Etching Silicon Patent 5501893, Office, U.S.P., USA (1996)
49. H. Jansen, M.d. Boer, R. Legtenberg, M. Elwenspoek: The black silicon method: A universal method for determining the parameter setting of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control, J. Micromech. Microeng. 5, 115–120 (1995)
50. J.W. Bartha, J. Greschner, M. Puech, P. Maquin: Low temperature etching of Si in high density plasma using SF_6/O_2, Microelectron. Eng. 27, 453–456 (1995)
51. M. Puech, P. Maquin: Low temperature etching of Si and PR in high density plasmas, Appl. Surf. Sci. 100–101, 579–582 (1996)
52. C.J. Mogab, A.C. Adams, D.L. Flamm: Plasma etching of Si and SiO_2 – The effect of oxygen additions to CF_4 plasmas, J. Appl. Phys. 49, 3796–3803 (1978)
53. A.M. Hynes, H. Ashraf, J.K. Bhardwaj, J. Hopkins, I. Johnston, J.N. Shepherd: Recent advances in silicon etching for MEMS using the ASE(TM) process, Sens. Actuators A Phys. 74, 13–17 (1999)
54. J. Hopkins, H. Ashraf, J.K. Bhardwaj, A.M. Hynes, I. Johnston, J.N. Shepherd: The benefits of process parameter ramping during plasma etching of high aspect ratio silicon structures. Materials Research Society Symposium Proceedings, p. 63 (1999)
55. R.A. Gottscho, C.W. Jurgensen, D.J. Vitkavage: Microscopic uniformity in plasma etching, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 10, 2133–2147 (1992)
56. J.W. Coburn, H.F. Winters: Conductance considerations in the reactive ion etching of high aspect ratio features, Appl. Phys. Lett. 55, 2730–2732 (1989)
57. V. Becker, F. Laermer, A. Schilp: Anisotropic Plasma Etching of Trenches in Silicon by control of Substrate Temperature, Patent DE 19841964, Germany (2000)
58. T. Kinoshita, M. Hane, J.P. McVittie: Notching as an example of charging in uniform high density plasmas. The 3rd International Workshop on Advanced Plasma Tools for Etching, Chemical Vapor Deposition, and Plasma Vapor Deposition: Sources, Process Control, and Diagnostics, San Jose, CA, pp. 560–565 (1996)
59. F. Laermer, A. Urban: Challenges, developments and applications of silicon deep reactive ion etching, Microelectron. Eng. 67–68, 349–355 (2003)
60. C. Steinbruchel: Langmuir probe measurements on CHF_3 and CF_4 plasmas: The role of ions in the reactive sputter etching of SiO_2 and Si, J. Electrochem. Soc. 130, 648–655 (1983)
61. L. Li, T. Abe, M. Esashi: Smooth surface glass etching by deep reactive ion etching with SF_6 and Xe gases, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 21, 2545 (2003)

62. X. Li, T. Abe, M. Esashi: Deep Reactive Ion Etching of Pyrex Glass. Proceedings of IEEE Thirteenth Annual International Conference on Micro Electro Mechanical Systems, Miyazaki, Japan, pp. 271 (2000)
63. A. Goyal, V. Hood, S. Tadigadapa: High speed anisotropic etching of Pyrex for microsystems applications, J. Non-Crystalline Solids 352, 657 (2006)
64. M.B. Pisani, P. Kao, S. Tadigadapa: Bulk acoustic wave resonators for infrared detection applications, Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International, pp. 1959–1962 (2009)
65. P.W. Leech: Reactive ion etching of piezoelectric materials in CF_4/CHF_3 plasmas, J. Vac. Sci. Technol. A Vac. Surf. Films 16, 2037–2041 (1998)
66. S.A. Campbell: The Science and Engineering of Microelectronic Fabrication (Oxford University Press, New York, NY, 2001)
67. F.A. Khan, L. Zhou, V. Kumar, I. Adesida, R. Okojie: High rate etching of AlN using $BCl_3/Cl_2/Ar$ inductively coupled plasma, Mater. Sci. Eng. B: Solid-State Mater. Adv. Technol. 95, 51–54 (2002)
68. F. Engelmark, G.F. Iriarte, I.V. Katardjiev: Selective etching of Al/AlN structures for metallization of surface acoustic wave devices, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 20, 843–848 (2002)
69. R.J. Shul, C.G. Willison, M.M. Bridges, J. Han, J.W. Lee, S.J. Pearton, C.R. Abernathy, J.D. MacKenzie, S.M. Donovan, L. Zhang, L.F. Lester: Selective inductively coupled plasma etching of group-III nitrides in Cl_2- and BCl_3-based plasmas. Papers from the 44th national symposium of the AVS, San Jose, CA, pp. 1621–1626 (1998)
70. J.C. Woo, G.H. Kim, J.G. Kim, C.I. Kim: Etching characteristic of ZnO thin films in an inductively coupled plasma, Surf. Coat. Technol. 202, 5705–5708 (2008)
71. M. Bale, R.E. Palmer: Deep plasma etching of piezoelectric PZT with SF_6, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 19, 2020–2025 (2001)
72. S.S. Subasinghe, A. Goyal, S. Tadigadapa: High aspect ratio plasma etching of bulk lead zirconate titanate. in Proceedings of SPIE: Micromachining and Microfabrication Process Technology XI vol. 6109, pp. 100–108 (Mary-Ann Maher, H.D.S., Jung-Chih Chiao (Eds.) SPIE, San Jose, CA, 2006)
73. S. Tadigadapa, K. Mateti: Piezoelectric MEMS sensors: state-of-the-art and perspectives, Meas. Sci. Technol. 20, 092001 (2009)
74. S. Schreiter, H.U. Poll: A new plasma-etching technique for micromechanical structuring of quartz, Sens. Actuators A Phys. A35, 137–141 (1992)
75. S.A. Smith, C.A. Wolden, M.D. Bremser, A.D. Hanser, R.F. Davis, W.V. Lampert: High rate and selective etching of GaN, AlGaN, and AlN using an inductively coupled plasma, Appl. Phys. Lett. 71, 3631–3633 (1997)
76. R.J. Shul, C.G. Willison, M.M. Bridges, J. Han, J.W. Lee, S.J. Pearton, C.R. Abernathy, J.D. MacKenzie, S.M. Donovan, L. Zhang, L.F. Lester: Selective inductively coupled plasma etching of group-III nitrides in Cl_2 and BCl_3-based plasmas, J. Vac. Sci. Technol. A: Vac. Surf. Films 16, 1621 (1998)
77. E. Mastropaolo, A.M. Gundlach, C. Fragkiadakis, P.B. Kirby, R. Cheung: Reactive ion etching of zinc oxide (ZnO) in $SiCl_4$ based plasmas, Electron. Lett. 43, 1467–1469 (2007)
78. W.T. Lim, L. Stafford, J.S. Wright, L.F. Vossa, R. Khanna, J.-I. Song, J.-S. Park, Y.W. Heo, J.-H. Lee, J.-J. Kim, D.P. Norton, S.J. Pearton: Comparison of plasma chemistries for the dry etching of bulk single-crystal zinc-oxide and rf-sputtered indium-zinc-oxide films, Appl. Surf. Sci. 253, 9228–9233 (2007)
79. W. Lim, L.F. Voss, R. Khanna, J. Wright, B.P. Gila, D.P. Norton, S.J. Pearton, F. Ren: Comparison of ZnO dry etching in high density inductively coupled CH_4/H_2 and C_2H_6/H_2-based chemistries, Pennington, NJ 08534-2896, United States, pp. 209–216 (2006)
80. A.M. Efremov, D.P. Kim, K.T. Kim, C.I. Kim: Etching characteristics and mechanism of $Pb(Zr,Ti)O_3$ thin films in CF_4/Ar inductively coupled plasma, Vacuum 75, 321–329 (2004)

81. A. Scherer, H.G. Craighead, E.D. Beebe: Gallium arsenide and aluminum gallium arsenide reactive ion etching in boron trichloride/argon mixtures, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 5, 1599–1605 (1987)
82. K.J. Nordheden, D.W. Ferguson, P.M. Smith: Reactive ion etching of via holes for GaAs high electron mobility transistors and monolithic microwave integrated circuits using $Cl_2/BCl_3/Ar$ gas mixtures, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 11, 1879–1883 (1993)
83. W.H. Guggina, A.A. Ketterson, E. Andideh, J. Hughes, I. Adesida, S. Caracci, J. Kolodzey: Characterization of $GaAs/Al_xGa_{1-x}As$ selective reactive ion etching in $SiCl_4/SiF_4$ plasmas. The 34th International Symposium on Electron, Ion and Photon Beams, San Antonio, TX, pp. 1956–1959 (1990)
84. R. Cheung, S. Thoms, S.P. Beamont, G. Doughty, V. Law, C.D.W. Wilkinson: Reactive ion etching of GaAs using a mixture of methane and hydrogen, Electron. Lett. 23, 857–859 (1987)
85. J. Werking, J. Schramm, C. Nguyen, E.L. Hu, H. Kroemer: Methane/hydrogen-based reactive ion etching of InAs, InP, GaAs, and GaSb, Appl. Phys. Lett. 58, 2003–2005 (1991)
86. M.A. Bosch, L.A. Coldren, E. Good: Reactive ion beam etching of InP with Cl_2, Appl. Phys. Lett. 38, 264–266 (1981)
87. C. Youtsey, I. Adesida: A comparative study of Cl_2 and HCl gases for the chemically assisted ion beam etching of InP. The 38th International Symposium on Electron, Ion, and Photon Beams, Scottsdale, AZ, pp. 2360–2365 (1995).
88. G.A. Vawter, C.I.H. Ashby: Reactive-ion-beam etching of InP in a chlorine–hydrogen mixture, The 38th International Symposium on Electron, Ion, and Photon Beams, New Orleans, LA, pp. 3374–3377 (1994)
89. C. Youtsey, R. Grundbacher, R. Panepucci, I. Adesida, C. Caneau: Characterization of chemically assisted ion beam etching of InP. The 38th International Symposium on Electron, Ion, and Photon Beams, New Orleans, LA, pp. 3317–3321 (1994)
90. K.K. Ko, S.W. Pang: High aspect ratio deep via holes in InP etched using Cl_2/Ar plasma, J. Electrochem. Soc. 142, 3945–3949 (1995)
91. U. Niggebrugge: Recent advances in dry etching processes for InP-based materials. Proceedings of the Third International Conference on Indium Phosphide and Related Materials, Cardiff, UK, pp 246–251 (1991)
92. J. Etrillard, F. Heliot, P. Ossart, M. Juhel, G. Patriarche, P. Carcenac, C. Vieu, M. Puech, P. Maquin: Sidewall and surface induced damage comparison between reactive ion etching and inductive plasma etching of InP using a $CH_4/H_2/O_2$ gas mixture. The 42nd national symposium of the American Vacuum Society, Mineapolis, MN, pp. 1056–1061 (1996)
93. J.E. Schramm, D.I. Babic, E.L. Hu, J.E. Bowers, J.L. Merz: Fabrication of high-aspect-ratio InP-based vertical-cavity laser mirrors using $CH_4/H_2/O_2/Ar$ reactive ion etching, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 15, 2031–2036 (1997)
94. R.J. Lee: Ion Beam Etching (Milling) (Elsevier, Amsterdam, 1984)
95. J.M.E. Harper: Ion Beam Etching, in Plasma Etching: An Introduction, pp. 391–423 (Manos, D.M., Flamm, D.L. (Eds.) Academic, San Diego, CA, 1989)
96. M. Cantagrel, M. Marchal: Argon ion etching in a reactive gas, J. Mater. Sci. 8, 1711–1716 (1973)

Chapter 8
MEMS Wet-Etch Processes and Procedures

David W. Burns

Abstract Wet chemical etching through openings in photoresist or hard masks underlies many process sequences for MEMS device fabrication. This chapter presents more than 800 wet-etch recipes for over 400 varieties and combinations of substrates and deposited thin films, with emphasis on processes that use laboratory chemicals often found in university and industrial cleanrooms. Over 600 citations serve as additional resources for selecting or developing etchants suitable for processing MEMS devices. Nearly 40 tables, organized internally by material then by etch components, allow quick location and comparisons among recipes. Abbreviations for target materials and etch components are standardized to aid in comparisons. Etch rates and etch selectivities over other materials are given where available. While emphasizing silicon and other popular materials in the MEMS field, III-V compounds and more exotic materials are also presented.

Topics addressed include wet-etch principles and procedures; process architectures that incorporate wet-etch sequences; evaluation and development of wet-etch procedures and equipment with emphasis on safety and an anticipation of foundry transfer; oxide, nitride, silicon, polysilicon, and germanium isotropic etching; standard metal etching; nonstandard dielectric, semiconductor and metal etching; photoresist removal and wafer cleaning sequences; silicide etching; plastic and polymer etching; anisotropic silicon etching; bulk silicon and silicon–germanium etch stops; electrochemical etching and etch stops; photoassisted etching and etch stops; thin-film etch stops; sacrificial layer removal; porous silicon formation; layer delineation for failure analysis; and defect determination. Practical examples offer some of the finer nuances in the processes and procedures related to wet chemical etching. This chapter provides a practical and valuable guide for device designers and process developers to select or develop an etch for many types of MEMS and integrated MEMS devices.

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8.1 Introduction

Few micromachined or integrated devices are developed or manufactured without some level of wet chemical processing. Whether the device is electrical, mechanical, electronic, integrated, optical, optoelectronic, biological, polymeric, microfluidic, sensor, or actuator, decisions about processing and process alternatives can have a major impact on the ultimate technical and commercial success. These devices are generally built on substrates of silicon, compound semiconductors, glass, quartz, ceramic, or plastic involving one or more layers of thin films deposited that are each patterned and etched on the substrate. The layers and deposition sequence place constraints on the process architectures and unit processes available for developing and manufacturing the device, becoming increasingly complex and interactive as the number of layers increases.

Wet etching is the systematic intentional removal of material using a liquid etchant, a process step generally preceded by the formation of an overlying photoresist mask (an exposed and developed photosensitive polymer) or a hard mask (a patterned etch-resistant material). The etch step is generally followed by a rinse step with deionized water and subsequent removal of the masking material. Wet-etch alternatives include dry etching, which uses one or more gaseous reactants at generally reduced pressures having RF-induced excitation of the reactant species and vacuum pumping for removal of the reaction products. Nonplasma dry etching, such as xenon difluoride or hydrofluoric acid vapor etching, has many of the characteristics of a wet isotropic etch and is generally performed in a confined chamber.

The creation of nearly all types of IC, MEMS, MOEMS, MST, and NEMS devices is likely to have involved some type of wet-etch procedure. Represented as steps or sequences in the overall process flow, wet etches are often incorporated for selectively removing portions of deposited thin films, stripping specific materials such as hard masks and photoresist masks, cleaning and preparing substrates for further processing, removing sacrificial layers and portions of substrates, and forming two- and three-dimensional structures. Considerations for a wet-etch sequence include etchant availability, etch selectivity, etch rate, etch isotropy, material compatibility, process compatibility, process repeatability, cost, equipment accessibility, worker safety, facilities support, and proper disposal concerns.

Although a device designer, process architect, or manufacturer may prefer a completely dry process flow when available, many of the standard process steps such as photoresist developing and wafer cleaning still remain aqueous. Wet-etch processing sequences can offer cost, speed, and performance benefits over dry-etch techniques. Dry-etch analogues may be unavailable, such as for extensive selective undercutting of microstructures or for crystal orientation-dependent etching. Dry processes may be preferred over wet processes, particularly if available in a well-equipped processing facility or if wet processes offer inadequate performance. An advantage for utilizing wet processes, however, is that devices may be developed and manufactured in a relatively low-capital, low-overhead laboratory or processing facility. Wet etching becomes particularly attractive when dry etching requires long etch times in

an expensive plasma or RIE etching system, and can be more cost and time effective when lots of 25 wafers or more are processed simultaneously.

The selection of processing sequences, whether wet or dry, is strongly driven by the availability of equipment and processes to the developer at an associated facility. The successful designer, developer, and manufacturer will nearly always use or modify processes that are on hand and avoid additional requirements unless absolutely necessary to develop new processes, install new equipment, or acquire new process capability. It is important to understand and apply both wet and dry processes where needed and to use standard processes wherever possible. Table 8.1 summarizes general considerations for comparisons between wet and dry etching.

Table 8.1 General comparisons between wet and dry etching

	Consideration	Dry etching	Wet etching
1	Etch existence	High	High
2	Etch rate	Moderate, variable	High, variable
3	Etch uniformity	Moderate, variable	Moderate, variable
4	Material selectivity	Low, variable	High with careful selection
5	Wafer throughput	Moderate	High
6	Mask selectivity	Moderate, variable	High with careful selection
7	Photoresist mask usage	High	Not usable in some cases
8	Patterned feature resolution	High	Moderate
9	Substrate backside exposure	Low	High
10	Etch reliability	High	Moderate; improves with automation
11	Etch repeatability	High	Moderate; improves with automation
12	Training and maintenance	Moderate	Low
13	Operator chemical exposure	Low	Moderate
14	Unit process cost	Moderate	Low
15	Equipment cost	High	Low
16	Facilities cost	High	Low

This chapter begins with an overview of principles and process architectures for wet etching, followed by a section on the evaluation and development of wet-etch facilities and procedures for the local and remote user. The next two sections present wet-etch processes in artificial yet practical divisions as IC-compatible materials that are generally acceptable to integrated circuit manufacturers and nonstandard materials that may require separate or dedicated equipment, facilities, postprocessing, or other special considerations. Additional sections cover anisotropic etching of silicon and etch stops, sacrificial layer removal using wet etchants, porous silicon formation, and wet etchants for layer delineation and defect determination. Further discussions of wet etching techniques and processes can be found in many excellent books and journals [1–30].

8.2 Principles and Process Architectures for Wet Etching

The triumviral sequence of deposition, pattern, and etch dominates much of semiconductor and MEMS processing, as shown in typical process or fabrication run travelers. The deposition sequence may include additive-process steps such as epitaxial growth, e-beam evaporation, sputtering, chemical vapor deposition (CVD), low-pressure CVD (LPCVD), metal-organic CVD (MOCVD), and plasma-enhanced CVD (PECVD), and alternatively include other sequences such as thermal oxidations or ion implantation. The patterning sequence generally involves spin-depositing photoresist and exposing with a contact aligner, stepper, or e-beam lithography system using a prescribed photoresist thickness and exposure time. The thickness and exposure time may be adjusted as needed to ensure adequate feature definition, particularly over large changes in film heights. The etching steps are often plasma or reactive-ion based. In situations where dry etching is not available or otherwise inadequate for a particular etch sequence, wet-etch steps can be inserted into the process flow. Selection of a particular wet- or dry-etch sequence is usually determined during the design and development of a MEMS device, although the choice may be modified when equipment is upgraded or the process is transferred to another facility.

Various process architectures are available or can be created for MEMS devices, such as fully integrated or fully custom processes, semicustom or standard MEMS processes, process variants of other established processes, and unit processes from multiple facilities, as illustrated in Fig. 8.1. Fully integrated MEMS processes can be based on established CMOS, BiCMOS, or compound semiconductor processes. Fully custom processes generally have only a few masking levels in a dedicated process used for prototypes, initial production, or high-volume devices. Semicustom processes incorporate device-specific MEMS sequences prior to or after integrated circuit processes, and may be incorporated at either the wafer or die level. Standard MEMS processes include qualified single and multilayer poly processes, metal processes, SOI or LIGA processes, and multiuser or multidevice processes. Process variants include relatively minor adjustments to an established process, such as starting material variations, small changes to film thickness or etch depths, and elimination of feature-free patterning steps from a standard process flow. For those willing to transport wafers between multiple facilities, unit process steps may be executed at one or more of the many excellent smaller facilities that have specific capabilities and expertise such as thin-film deposition, epi growth or ion implantation, patterning and etching, chemical–mechanical polishing, and backend processes such as dicing and packaging.

Fully integrated and standard MEMS processes often provide the user with few if any choices in the etchant determination, inasmuch as these processing sequences are established and qualified at a particular facility. The user may not even know or need to know details of the etch sequences. An exemplary fully integrated process has IC sequences intermingled with qualified and compatible MEMS sequences. Fully custom MEMS processes provide the widest opportunities for selection of wet- and dry-etch sequences, particularly for early-stage device development, for

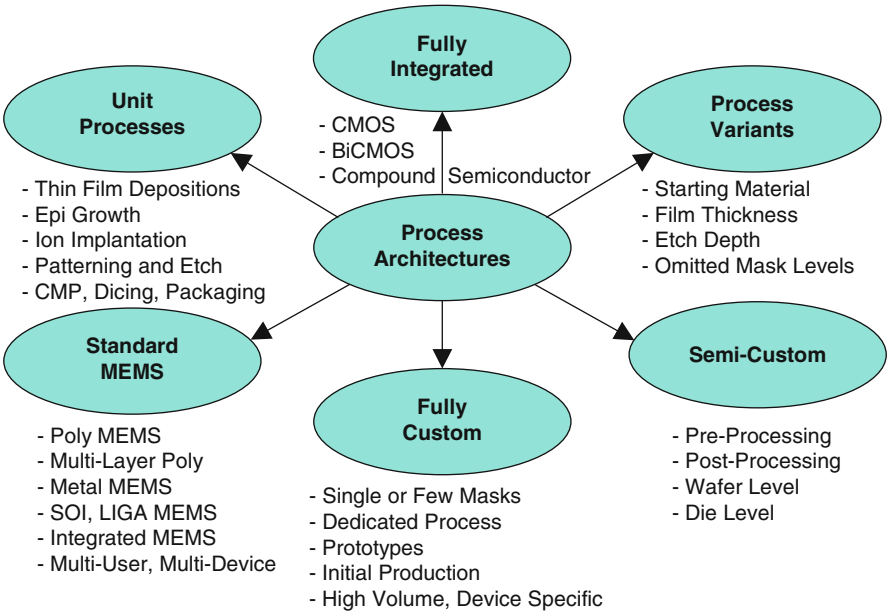

Fig. 8.1 Process architectures for MEMS devices include fully integrated processes, process variants of standard integrated circuit or MEMS processes, semicustom and fully custom processes, standard (e.g., multidevice or multiuser) MEMS processes, and unit processes. Wet-etch sequences may be predetermined by the selected process architecture, particularly for devices that can fit into standard and fully integrated processes. Special wet-etch sequences may require the selection of a process variant, semicustom, fully custom, or unit process architecture

devices requiring only a few mask sequences, and for very high-volume devices. Semicustom processes allow MEMS sequences to be placed before or more often after an established active device (i.e., CMOS) process, providing the developer the opportunity to select wet- or dry-etching sequences to meet specific device requirements. Process variants can include modifications to the etch steps to meet the requirements for thin-film etching. The user of unit processes may have the strongest say in wet process selection and execution.

A number of companies offer foundry services, comprising anywhere from single processing steps and modules to full-blown established process flows. Some of the larger foundries offering MEMS services, subject to change, are listed in the references [31]. For example, a user may submit a CAD design to an outside service, which can provide multilevel metal structures on top of a variety of substrates based on multilayer electrodeposition of materials [32]. Foundries for unit process steps may be found through online searches or conversations with industrial experts and foundry representatives.

Selection of a wet-etch unit process requires many considerations, some of which are illustrated in Fig. 8.2. After development of a general process flow for a particular device, etch sequences are evaluated as to whether they should be wet or dry.

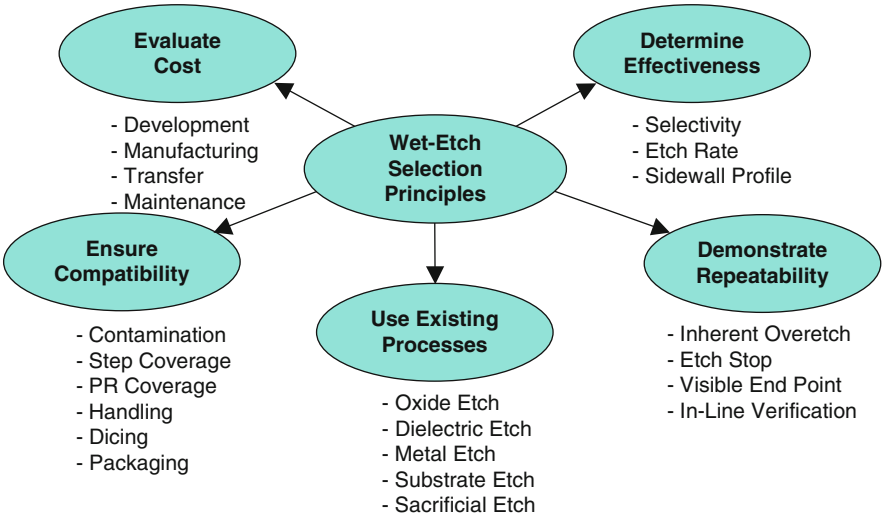

Fig. 8.2 Wet-etch selection and development principles include: determine effectiveness, demonstrate repeatability and reliability, use existing processes where possible, ensure process compatibility, and evaluate cost

The first wet-etch selection principle is to determine the effectiveness of a candidate etchant or an etch sequence based on selectivity, etch rate, and sidewall profile requirements. The selectivity must be sufficiently high to etch the desired material while having minimal impact on the masking material and any underlying films that become exposed as the etched material is clearing. When possible, the etch rate should be selected to complete the etch in about 2–5 min: long enough so that insertion and wetting effects are minimal, and short enough to keep the workflow moving adequately and keep unit costs down. Specialized etches, such as sacrificial etches or anisotropic etching of substrates, may take several hours or more.

The sidewall profile can be a significant consideration when selecting a wet etch. Wet etches, as compared to dry etches, can significantly undercut mask features. Fine features, such as adjacent lines and spaces, may completely disappear during a wet etch. Undercutting also leads to broadening of device features for dark-field masks, affecting design rules and in some cases limiting the die size. In some situations, tapered sidewalls that generally occur with wet etches can be advantageous, allowing better step coverage for subsequent film deposition and patterning.

The second wet-etch selection principle is to demonstrate repeatability, reliability, and robustness of the wet etch. For example, a finicky etch sequence requires excessive operator attention and can ruin an entire process with even slight etch variations. A good wet etch sequence has built-in overetch capability that allows overetching of 5–15% or more with minimal impact on yield or device performance. An ideal wet etch has inherent overetch capability against an etch stop and nearly infinite selectivity to other exposed materials. Highly beneficial to an etch sequence

is a visible endpoint for operator-controlled etching and in-line film-thickness verification of the etched or underlying film, which ensures that the selected material has been completely removed in the targeted areas.

Wet etches are generally sensitive to etchant temperature, etchant concentration, amount of previous use, etchant age, evaporation of the etchant or diluent in the etchant solution, etchant loading such as the number of wafers being etched and the percentage of exposed area including substrate backsides, feature size, film composition, film morphology, annealing history, surface contamination, surface residues, incubation time, stirring or agitation, and room illumination, each requiring diligent control for a reliable etch process.

Etches can be disqualified from consideration if the etchant is too slow; has insufficient selectivity to other masking materials and underlying layers; lacks uniformity; presents contamination concerns for further substrate processing; generates unwanted compounds, residues, or pitting; causes cracks, swelling, peeling, or excessive undercutting of the masking layer; or requires unwieldy storage, handling, disposal, safety, and facilities concerns. Although wet etchants may offer higher selectivity than dry etches to masking materials, they may also be appreciably more sensitive to film composition and annealing.

The third wet-etch selection principle is to use existing processes wherever possible. Processing facilities will generally have wet-etch capabilities for materials such as silicon dioxide and metals such as aluminum that can be adapted as needed to the particular film thickness of interest. Dedicated stations may be available for particular processes such as anisotropic etching of substrates. Where special etches are required, such as an extensive sacrificial etch, it is wise to adapt existing processes and equipment only as needed to achieve the desired etch characteristics. Those who have developed a customized etch to fabricate a device know the significant amount of time and effort required to develop, characterize, and qualify the specialized etch.

The fourth wet-etch principle is to ensure compatibility with other aspects of the device process and the facility where the device is to be developed. Cross-contamination into other devices, equipment, and processes via wafer routing or wafer handling in common holders and etch baths can unexpectedly have a detrimental impact on other devices. The developer needs to ensure that subsequent sequences within a given device process are compatible, considering step coverage for subsequent deposition steps and photoresist spinning, the handling of fragile devices, dicing requirements, and packaging needs.

When multiple options exist after due consideration has been given to the above principles for wet-etch selection, the next step is to consider all the costs of development, manufacturing and technology transfer, equipment and facility maintenance, and the overhead associated with floor space, process controls, and supplies. Costs are generally lowest when existing processes within a facility are used, because the expense for etching with an existing process is usually marginal or incremental and does not require additional capitalization or development efforts.

Those who have developed or are currently developing a semiconductor or MEMS device recognize the extensive interplay between process sequences and device design. If the etch sequence cannot be adjusted to achieve the desired result,

adjustments to the overall process architecture may be helpful. Alternatively, device designs can often be adjusted to accommodate undue constraints on etching or other process sequences.

8.2.1 Surface Reactions and Reactant/Product Transport

Etching systems generally comprise an etch beaker or tank sufficient in size to hold one or more wafers comfortably in an often vertical orientation, surrounded completely with liquid etchant during an etch cycle, as illustrated in Fig. 8.3. A heater, thermocouple, and agitator may be included. The tanks often have a drain facilitized into an acid/base neutralization system, a dedicated hydrofluoric acid collection system, or a solvent collection tank. Etchant may be poured into the tank from bottles of etchant or from permanently installed delivery systems with external chemical storage facilities. The etch tanks and liquid distribution systems are formed from inert materials with respect to the etchant used, such as perfluoroalkoxy (PFA), flame-retardant polypropylene (PP), high-density polyethylene (HDPE), polytetrafluoroethylene (PTFE or Teflon®), molded polyvinylidene fluoride (PVDF), or quartz [27, 33]. Stainless steel tanks are occasionally used for solvents and sometimes for KOH etchants. PFA tanks and holders may be used for KOH etching. The etch tank may be placed inside another tank or sink for safety and spillage control. To protect the operator, the tank and sink are typically exhausted

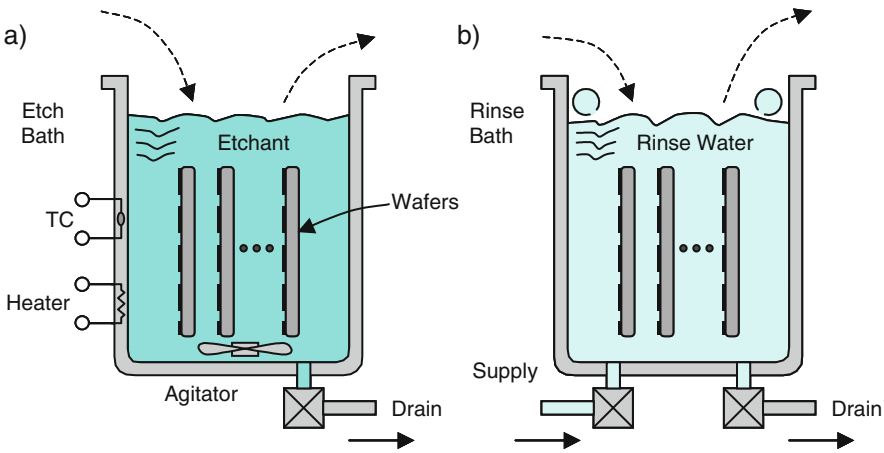

Fig. 8.3 Etch baths (**a**) for wet etchants often have a heater, a thermocouple, an agitator or stirrer, and valving to drain the etchant. A separate rinse bath (**b**) allows copious amounts of deionized water to rinse the wafers adequately prior to spin or blow-drying. A dedicated holder or cassette (not shown) of polyaryletheretherketone (PEEK) with embedded carbon fibers, polypropylene, PFA, PTFE or Teflon®, PVDF, or quartz may be used for wafer transport during etching and rinsing

with an overhead exhaust hood implemented with splashguards as part of a wet bench.

The wet bench may have timers, light and fan switches, heater controllers, alarm systems, and one or more dedicated etch baths along with rinse tanks. The rinse tanks are similarly constructed and allow for copious amounts of deionized water to spray on or bubble up past the wafers, diluting and removing the etchant from the wafers. The rinse baths may have drop doors at the bottom of the tank to rapidly remove the rinse water in multiple dump–rinse cycles. Some etch sequences require that the wafers be etched and rinsed in the same bath (i.e., dilution rinses), however, wafers are generally transported from the etch bath to the rinse bath by manual or automatic lifting. The wafer holders or cassettes must also be inert to the etchant and are usually dedicated to a particular wet bench or etch process to avoid possibilities of cross-contamination.

A generalized model for liquid-etch processes is illustrated in Fig. 8.4. Etching occurs when reactants in a liquid etchant chemically react at an exposed surface of the material being etched, with by-products dissolving back into the liquid etchant or released as a gas. The etch rate is affected by the concentration of reactants in the liquid etchant, the local transport of these reactants to the exposed surface, the reaction rate at the interface between the liquid etchant and the material being etched, the removal rate of the reaction products from the surface, and the concentration of reaction products in the etch bath.

The reactions at the liquid–solid interface can be surprisingly complex. Etching may involve a composite reduction–oxidation reaction that produces an oxide of the material being etched that is then etched to expose fresh material in a continuous manner. Secondary effects can occur and sometimes dominate, such as vapor barriers at the interface from a high-aspect-ratio feature or from nonwetting masking material. Unwanted by-products, such as a salt residue or other solid formation at the etched surface, can generate an etch barrier that slows or even stops an etch. Local evolution of gas can create a micromasking effect that slows the etch rate while bubbles stay adhered to the surface, resulting in a roughened surface and possible hillock formation. Inadvertent, localized etch rate reductions can occur with viscous or low-solubility etchants, as when a wafer is partially rinsed and then reinserted into the etch bath with insufficient agitation.

Enhancements to the etch rate are often achieved by: increasing the concentration of the reactants, performing the etch at an elevated temperature, using an agitator to assist etchant flow, changing the etch bath to get fresh etchant and expel accumulated by-products, and minimizing obstructions to the etchant that may occur with direct contact to a wafer holder or close proximity to another wafer. The rate-limiting step of the generalized model usually determines which enhancements have the most impact. Increases in the etchant temperature usually result in a faster etch, although room-temperature etching is often the most convenient and safest with reasonable etch rates obtained by careful selection of the etchant and etchant concentration.

Nearly all wet etches, including anisotropic etches, encompass some degree of undercutting when using an overlying photoresist or hard mask layer having patterned features. An ideal etch, best realized with a dry etch rather than a wet etch,

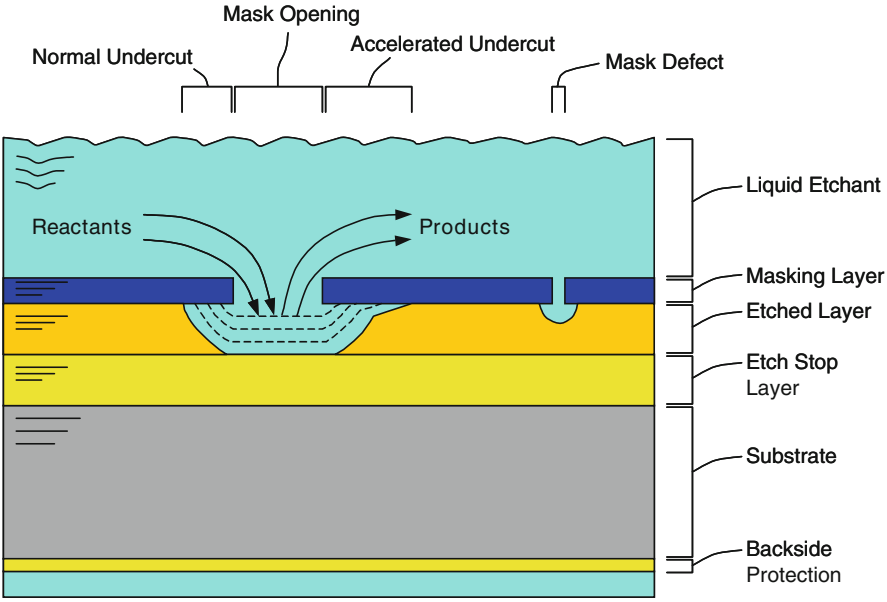

Fig. 8.4 Illustration of transport mechanisms for liquid etching of masked layers with an underlying etch stop layer. A supply of reactants in the etchant react heterogeneously with exposed portions of the etched layer resulting in one or more by-products that dissolve back into the etch liquid or egress as a gas. Insufficient reactants or an excessive concentration of products can slow the etch inordinately, particularly in tight geometries. With most thin films and amorphous materials, the reaction is isotropic, resulting in circular corners viewed from above and a generally rounded etch profile at the sidewalls from the side. As the etch front strikes an underlying etch stop layer, the reactants are less exhausted and the etch can speed up laterally, resulting in a more angular and less rounded sidewall. Masking layers with high internal stress or etched layers with a deviated morphology at the upper surface can result in appreciably accelerated etch fronts at the interface between the masking layer and the etched layer, effectively accelerating the undercutting. Defects in the masking layer can result in unwanted local etching. A dark-field masking layer is illustrated; similar concerns and phenomena occur for light-field masks though the amount of material etched is usually much greater

translates the overlying patterned mask features into the etched layer with high fidelity and minimal feature distortion. Wet etches, with their inherent property of etching any exposed surface, generally etch the sidewalls at a similar rate as the bottom. Isotropic etches produce a lateral undercut distance on the same order of magnitude as the etch depth, resulting in a curved profile having a radius approximately equal to the etch depth as shown on the left side of Fig. 8.4. Undercutting bias may be compensated with adjustments to the widths of corresponding features on the photomask or beam-writing tool. Undercutting concerns may preclude the use of wet etchants for fine features in favor of dry etching that is more vertical and has a diminished lateral etch rate. With anisotropic materials or anisotropic etchants, the sidewall profile becomes more angular. For the isotropic case, as the etchant breaks through to an underlying etch stop layer, the etchant can become less exhausted

locally and etch laterally more quickly, which tends to linearize and straighten the sidewall.

Other phenomena such as a highly tensile masking layer can cause a slight lifting of the masking layer near a feature opening, which causes the mask to peel back slightly during etching. The peeling results in accelerated undercutting at the interface and a shallow angular profile as illustrated near the center of Fig. 8.4. A compressive mask may also tend to lift via mechanical buckling as the aspect ratio (undercut distance to mask thickness) increases, which further increases the etch rate.

The lateral etch rate can be accelerated by modifying characteristics of the etched layer such as decreasing the density at the top or bottom of the film, generating a high defect density near the top surface, or locally injecting high levels of impurities. In cases where the etched feature is deep or where extensive lateral etching is desired, the etchant can become locally constrained and exhausted, decreasing the local etch rate. Defects in the masking layer, such as small particulates, can allow the etchant to creep along the particulate or move blatantly through an open mask defect to inadvertently etch the underlying material, as shown on the right side of Fig. 8.4.

8.2.2 Etchant Selectivity and Masking Considerations

A major consideration in the selection and evaluation of a wet-etch process sequence is the etch selectivity, defined as the etch rate of the etched material relative to the etch rate of the masking or underlying material. Etch selectivities of 100 or more are preferable although selectivities as low as one or less can prove adequate for thin etched layers. Etch selectivity with respect to the etch stop layer or to other layers exposed during the etch sequence may also be of consequence, although it is often of lesser concern because the underlying layer is generally exposed for only a short time during the overetch phase of the sequence. As depicted in the graphic of Fig. 8.5, a higher etch selectivity usually allows a thinner mask layer, a deeper etch, a thinner etch stop layer, and improved overetch capability.

The choice of etchant may be determined by the masking layer, and vice versa. The masking layer prevents the etchant from reaching covered surfaces and must hold up during the time for the etch. A thicker masking layer can increase the achievable etch depth. The masking layer may also etch laterally to some degree as the etch proceeds. This additional source of bias may be compensated for in the photomask design by automatically adding or subtracting a suitable amount from light or dark field mask features, respectively. Over time, the wet etchant may absorb into the masking layer, causing it to swell, crack, or possibly lift, thereby exposing the etched layer in unintended areas. Attention must be paid to the status of the films on the backside of the substrate, inasmuch as this portion as well as the sides of the substrate are generally exposed directly to the etchant. Additional protection may be

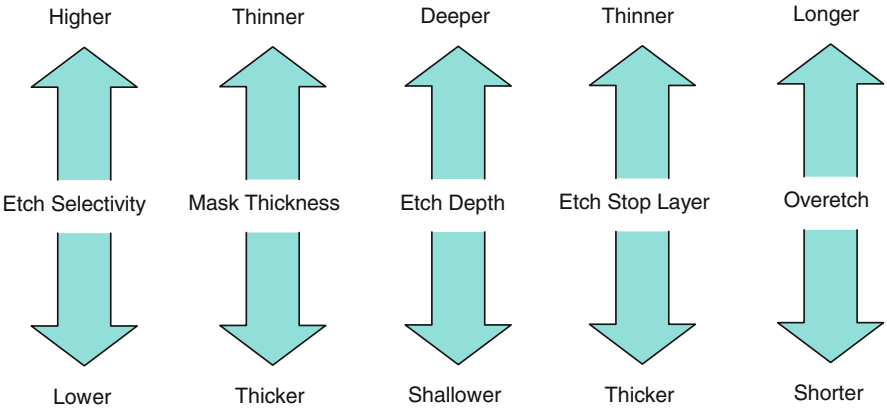

Fig. 8.5 As the selectivity of an etchant compared to an etch mask or an etch stop layer increases, the mask thickness can be thinner, the achievable etch can be deeper, the etch stop layer can be thinner, and the overetch can be longer

provided with an application of photoresist to the backside, the deposition of backside etch-resistant protection layers, or use of special fixturing that limits backside exposure during the etch step.

Many factors should be considered for the appropriate selection of an etch-resistant masking layer, as shown in Fig. 8.6. The predominant consideration is whether an existing or standard process is adequate for the device. Because of the cost and time required to set up a new etch sequence, the best approach is usually a standard photoresist-based etch sequence including steps such as spin,

Fig. 8.6 Considerations and consequences of using a hard mask or a photoresist mask shows that a PR mask is generally the mask of choice, except for situations where higher etch resistance, a deeper etch, or substrate backside protection is needed

prebake, expose, develop, postbake, etch, rinse, dry, and strip. Basic photoresist processes are generally IC compatible, offer less risk of contamination, provide better resolution, and offer improved feature size control over a hard-mask sequence that likely uses an initial photoresist patterning and etching sequence to form the hard-mask features. Photoresist masking sequences, once installed in a facility, reduce development costs for a new etchant. Photoresist processing generally provides lower unit costs, contains fewer process steps, has a shorter overall process time, provides better step coverage in most situations, and spins onto the wafer faster than coating the wafer with a thin-film deposition for use as a hard mask.

When needed, photoresist processes can often be adapted for MEMS device requirements. For example, step coverage can be improved with a thicker photoresist layer simply by slowing the spin speed or selecting a different photoresist with higher viscosity and solids content. Improved etch resistance with photoresist masks can sometimes be achieved with an elevated postbake cycle or heavy UV exposure for negative-acting resist. With careful handling and processing considerations, photoresist can be spun on the backside of a wafer to provide any needed masking or backside protection. Similarly, backside photolithography sequences can benefit from a frontside photoresist coating to provide etch resistance and scratch protection during the etch sequence.

8.2.3 Direct Etching and Liftoff Techniques

Liftoff techniques may be invoked when a difficult-to-etch material such as a noble metal or a stack of several metal layers requires patterning, and direct etching is unsuitable. Rather than spinning and patterning photoresist on top of the patterned layer and etching the layer directly, the liftoff technique first forms a patterned photoresist layer on the substrate and then the patterned layer is deposited directly on the resist such as by e-beam evaporation (see Fig. 8.7). After stripping away the photoresist using, for example, a solvent in an ultrasonic bath, selected material in contact with the substrate remains and the rest floats away or is rinsed, brushed, or blown from the substrate. The liftoff process may result in jagged edges due to thin deposited material on the photoresist sidewalls prior to liftoff. Enhanced liftoff techniques use a two-layer resist system with a relatively thin, somewhat developer-resistant upper layer above a lower layer that is less resistant. When the photoresist system is exposed and developed, small overhangs emerge over the lower layer, which subsequently shadow a sputtered or e-beam deposited film. Note that the tone of the photomask is reversed for the liftoff process (i.e., a dark field mask is needed where a light-field mask would be correct for direct etching) or negative-acting resist may be used. Alternatively, the enhanced liftoff technique can be implemented effectively with a carefully selected thin-film stack.

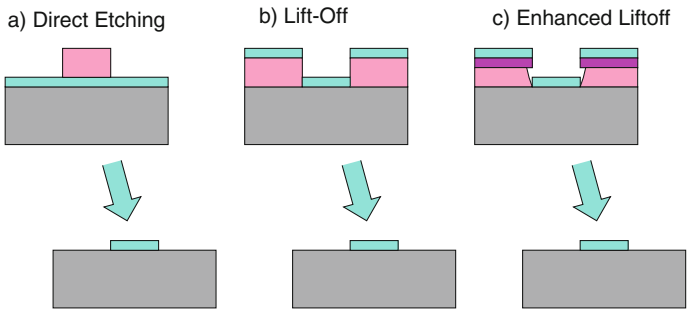

Fig. 8.7 Liftoff techniques may be used in lieu of direct etching for materials that are difficult to etch or the unavailability of etchants with adequate selectivity to other exposed materials. Conventional etching, as in (**a**), directly etches the exposed material, leaving the covered material unetched. The general lift-off process places the to-be-removed material on top of patterned photoresist and on the substrate as shown in (**b**), where the underlying photoresist is dissolved away, requiring no direct etching of the patterned material. Material codeposited on the sidewalls of the photoresist or liftoff layer can prove difficult to remove cleanly and may result in unwanted stringers and particulates. An enhanced liftoff process as in (**c**) has a composite photoresist layer wherein the thin upper resist layer is more resistant to the developer than the underlying resist layer; in this way, an overhanging region is produced to minimize sidewall deposition and improve the robustness of the etch

8.2.4 Sacrificial Layer Removal

Sacrificial layer etching presents specific challenges that are normally secondary considerations for direct wet or dry etching. Sacrificial layers are positioned underneath structural layers, where features in the sacrificial layer such as anchor openings, dimples, sidewall profiles, film thickness, and film steps shape the overlying structural layer. Selective removal of the sacrificial layer is generally accomplished with extensive lateral etching using a liquid etchant to undercut the structural layer and leave portions or more freestanding. The etchant must have extremely high selectivity to the sacrificial layer relative to the structural layer and other exposed materials for lengthy sacrificial etches. Lack of an etchant with suitable selectivity restricts the attainable undercut distance and can limit the choices of materials usable for the structural layer.

Successful sacrificial etch processes generally have inherently high overetch capability that allows the operator to ensure complete sacrificial layer removal and the designer to place features with short and long undercut times on the same device. Removal of sacrificial layers generally proceeds with relatively short downward etching followed by extensive lateral etching. Lateral etching is generally isotropic in the plane, etching in all directions equally. As described in Section 8.1, the etchant can become exhausted with insufficient reactants or become poisoned with too many etch products, either of which can reduce the local etch rate. Design features should be placed so that the undercutting frees up all portions of a structure nearly at the same time; however, a robust etchant, sacrificial layer and structural layer combination allows fidelity in the formation of structures even with vastly differing undercut

time. During the etch sequence, anchored features need to stay anchored, with the sacrificial etchant unable to separate the structural layer from the substrate. Upon completion of the etch, test structures or device features that can be inspected readily validate the etch procedure.

Enhancements can be made to the sacrificial etch process for improved performance. For example, careful selection and abidance with design rules for etch holes in the structural layer allow local access of the etchant to the sacrificial layer and reduces the time required to completely clear the sacrificial layer. The sacrificial layer itself may be selected to increase the etch rate, such as a bilayer of fast-etching, heavily doped deposited oxide over a thermally grown oxide. Wet etching in general and sacrificial layer etching in particular require consideration of the wafer backside so that any deposited films stay intact and do not flake off during the sacrificial etch process.

8.2.5 Substrate Thinning and Removal

Wet etchants are often used in the thinning or selective removal of substrate material (see Fig. 8.8), largely because of the relatively high volume of the etched material to be removed and the high density of reactants in the liquid etchant compared to reactants in a reduced-pressure plasma etching system. Uniform substrate removal or thinning combines physical grinding mechanisms with chemical etching in chemical–mechanical processes to rapidly remove material on either the backside or the frontside of a wafer. Masked features, such as holes, vias, trenches, channels, and anisotropically etched diaphragms confine the etch choice to selective wet etchants or to high etch-rate reactive ion etchers. Wafer thinning or substrate

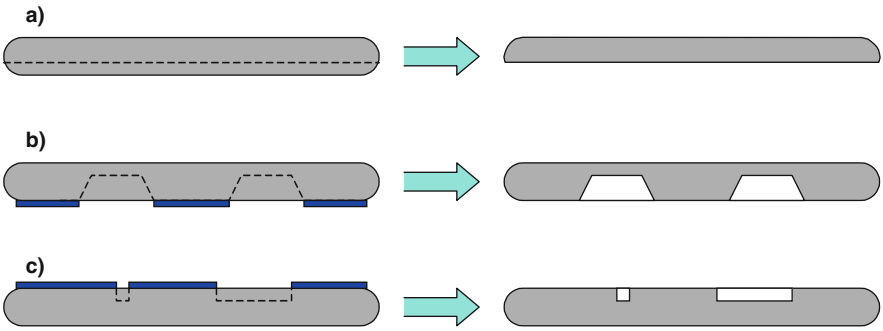

Fig. 8.8 Wet chemical etching can be used to (**a**) thin, (**b**) selectively etch from the backside, or (**c**) selectively etch substrates from the frontside. Chemical–mechanical polishing or planarization (CMP) combines mechanical grinding with chemical etching to uniformly thin the substrate backside or planarize the topside. Masked features for anisotropically etched diaphragms, through-wafer holes and vias, or topside trenches and channels require a suitable etch mask and may be wet etched or dry etched. The wafers become increasingly fragile and special care must be placed during subsequent handling and dicing

etching is generally placed near the end of the process flow, as the wafers become increasingly fragile with thinning and have higher embedded costs.

8.2.6 Impact on Process Architecture

The choice of the type of wet etch has a direct impact on the process architecture. As illustrated in Fig. 8.9, the process flow can be generalized into a series of masking sequences, each including a deposition step, a patterning step, and an etch step. Although deposition steps clearly encompass sputtered, e-beam evaporated, chemical vapor, or plasma-deposited films, also falling into this category are thermal oxidation, ion implantation, or acquisition of starting material. Patterning of photoresist with photomasks or direct-writing equipment provides a suitable mask for most etch processes, whether wet or dry. Hard masks provide increased etch resistance where needed, although they themselves are generally patterned with a photoresist sequence. During the deliberations for choosing the order and type of etching processes, each mask sequence must be considered to ensure that nonstandard materials are not included early in the process; that possible contamination from etch tanks, holders, or etchants themselves is avoided; that restricted fume hoods or other wet-etch facilities are used only after critical processing sequences have been completed; that masking materials are limited where possible to photoresist masks or to standard oxide, polysilicon, and metal layers for use as hard masks; that structural layers be limited to standard materials when contamination is a concern; that the masking material be readily stripped after etch completion; that selected film thicknesses be compatible with subsequent processing including photoresist coverage; that step coverage after a film has been etched does not generate stringers or other sources of particles; and that wafer handling not be compromised

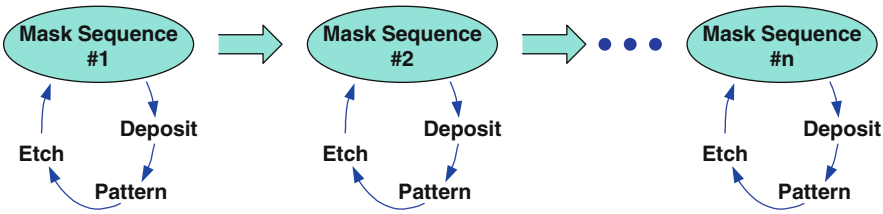

Fig. 8.9 Process flows for ICs, MEMS/NEMS, or integrated MEMS/NEMS devices can be simplified, with exceptions, into a series of masking sequences, each with a deposition step, a patterning step, and an etch step. Complex CMOS and BiCMOS processes may have two dozen or more mask sequences whereas many MEMS-only process flows have fewer than five. Each masking sequence is affected by the prior sequences and has an impact on the subsequent sequences. The order and choice for each sequence is often a part of the device design. To achieve the desired result, the process steps or the design may be varied. Decisions on the order of execution for wet-etch sequences and their associated masking and material layers must consider a number of issues including contamination, film thickness limitations, front- and backside processing requirements, and substrate handling

by creating fragile structures too early into the overall flow. This all being said, the clever device designer and process engineer can often work together and find compromises that achieve the design and production goals in a cost-effective, technically successful manner.

8.2.7 Process Development for Wet Etches

When considering development of a new wet-etching procedure: avoid it if at all possible. A new etch process can involve setting up new facilities, installing new equipment, setting up new chemical handling and safety procedures, obtaining purchasing approvals, determining chemical storage and disposal, establishing training procedures, performing operator training, providing system maintenance, and spending a large amount of characterization time with sometimes expensive wafers. Adapting an existing etch procedure, or better yet using an existing etch procedure, is a highly recommended alternative. In many established laboratories or fabrication facilities, a wide array of processes and materials for photoresist and hard masks are available for use or adaptation. Hard masks are sometimes necessary, however, it is best to consider and use a photoresist mask whenever possible.

In cases where a new etch is needed or an existing etch needs adaptation, guidelines for etching procedures and safety considerations are available from a variety of sources including handbooks, user guides, equipment manuals, manufacturer's recommendations, etchant suppliers, photoresist manufacturers, the Web, university websites, publications, and expert knowledge from an experienced user or processing expert. Appreciable effort is required to set up an etch facility with suitable services, adequate ventilation, appropriate disposal means, and controlled access. Several etch stations may be needed in a facility to accommodate the needs of different users and process flows. Facilities should provide ready access to goggles, facemasks, aprons, and spill carts with established safety procedures and chemical handling in case of spills. Wet benches are outfitted with suitable beakers, tanks, holders, and cassettes, with dedicated labware for contamination control. PFA, PTFE, or quartz labware are generally the best choice, although other materials may serve for room-temperature etchants. Etch sequences may be executed in heated tanks or in beakers on hot plates, although etch processes that run at room temperature are highly favored. Etch-process development generally requires plenty of wafers to establish etch rates of the etch layer and potential masking layers, to determine selectivity to other materials in the wafer stack, and to perform sensitivity studies with changes in etchant concentration, solution temperature, and other variables. The amount of rinsing may need to be qualified, with aqueous etchants preferred over solvents. A run-traveler template and operating procedures should be finalized and documented. Light sensitivity for the etch should be checked, and operation in a tank with a lid may be needed. Agitation capability may be desired for improved etch uniformity. Adequate removal of photoresist and hard masks must be verified.

Various test equipment can aid in the development and monitoring of wet etches, as listed in Table 8.2. The trained, unaided human eye can effectively see when an etch has been completed for many films such as shiny metal films, although it is generally unsuitable for determining adequate clearing of the film between small patterned features. By temporarily withdrawing a wafer from an etchant, an operator can look briefly at large features on the wafer topside or backside and observe interference fringes, color, or sheen changes on the wafer to determine if the etch is complete. Hydrophobicity changes may be observed as the wafer is temporarily withdrawn from the etchant. Excessive withdrawal of the wafer for inspection may slow the etch, however, and in some cases cause the etch to stop due to surface reactions that may occur when the wafer is exposed to air.

Table 8.2 Test equipment for wet-etch development

	Equipment	Advantages	Disadvantages
1	Unaided eye	Allows rapid inspection during etch No intermediate rinsing and drying steps Allows etch continuation Provides immediate verification Overetch can be timed from etch clearing Good for pilot wafer verification	Can slow etch Not applicable for many films Difficult to tell progress of an incomplete etch Requires larger features for inspection Requires manual handling Difficult to assess small features
2	Microscope	Readily available Works well for metal films and films with high visual contrast Small features can be inspected	Requires rinsing and drying before each inspection Transparent films are difficult to assess Difficult to assess very fine features
3	Microscope with depth gage	Works well for deep etches Upgrade available for most microscopes	Limited resolution due to depth of field limitations Not valid for transparent layers
4	Ellipsometer	Noncontact Provides refractive index and thickness	Difficult on small features Not suitable for metal films Limited applicability to multilayer films
5	Optical film thickness spectro-reflectometer	Noncontact Repeatable quantitative metrics Suitable for test structures Provides refractive index and thickness	Requires rinsing and drying before inspection Not suitable for metal films Limited applicability to multilayer films
6	Optical interferometric profilometer	Noncontact Wide-area 3-D step heights Suitable for test structures	Requires rinsing and drying before inspection Not suitable for transparent films
7	Mechanical profilometer	Relatively low cost Uses patterned features	Presents contamination concerns due to probe contact Requires patterned features

Table 8.2 (continued)

	Equipment	Advantages	Disadvantages
8	Depth gauge, mechanical	Low cost Re-zero to wafer reference surface	Moderate accuracy Requires large feature sizes
9	SEM	High resolution	Requires wafer fragments or cross-sectioned features Destructive
10	FIB/SEM	Accuracy In situ cross-sectioning	Requires patterned features Destructive
11	EDS, STEM, XPS, scanning Auger	Provides chemical analysis	Difficult on small features Destructive
12	AFM	Provides surface texture and small step heights	Incurs physical contact Small sample area

Viewing the wafer with an optical microscope may help determine etch completion of a patterned feature for many films, although etch rates for incompletely etched films are difficult to determine when limited to observations through the microscope. Deep etches can often be determined with a quality microscope by focusing on the substrate surface and then on the bottom of the etched feature, and calculating height differences from readings off the mechanical dials on the microscope. To improve accuracy, the z-translation stage on the microscope can be outfitted with an interferometric readout for determining distance between one in-focus surface and another, from which etch depths and etch rates can be determined.

An ellipsometer may be used effectively to determine film thickness and removal rates for single-layer and some multilayer stacks. A vertical noncontact spectrometer with a small spot size (e.g., NanoSpec [34]) is a valuable tool for determining the etch rate for most transparent and semitransparent films. A mechanical profilometer (e.g., Alpha-Step [35] or Dektak [36]) is useful for observing etch progress for metals and other films, although it requires contact on the surface with a needle point that may present contamination problems. Mechanical drop or depth gauges (e.g., Mitutoyo [37]) can be helpful for large, deeply etched structures such as anisotropically etched diaphragms.

The application of adhesive tape, a stripe from a resist pen, or a drop of photoresist on a film to be etched can sometimes provide suitable features for determining film thickness and hence the etch rate after the film has been etched, although the feature edges are often too poorly defined to provide a sufficiently sharp edge. Improvements to the edge definition can be made with use of a test or device mask on a test or run wafer. Dedicated structures for depth measurements and etch verification can be placed on the test and device wafers, and are highly recommended for process development, qualification and monitoring.

Analytical equipment such as a scanning electron microscope (SEM) is used occasionally for determining etch rates, however, it requires cross-sectioned features and is generally destructive. An etch profile may be determined by cleaving a wafer across an etch hole and then viewing and measuring etch depths in the SEM. Newer focused ion beam and scanning electron microscopy (FIB/SEM) equipment can perform the cross-sectioning in the same chamber as the inspection. XPS and other chemical-analysis techniques may also be used to determine the etch rate of some material configurations, although a large, unpatterned spot size is generally needed.

8.2.8 Additional Considerations and Alternatives

Wet-etch processes, particularly sequences that require a new setup for each use, are prone to certain difficulties such as incorrectly mixed etchant, unavailable wafer holders, temporarily unavailable services, and broken labware. Although procedures can be set up to avoid such issues, it is generally incumbent on the user to ensure that the etch process is successfully carried out. Two principles help avoid inadvertent happenings: run a pilot wafer or part of a wafer prior to the run wafer(s), and ensure test structures are located somewhere on the wafer or device so that the etch sequence can be verified immediately.

For those with limited access to unit processes such as wet etches, alternatives are provided in Table 8.3. A commercial foundry may support an entire process flow that allows the user to submit a design, and from that design the foundry processes the wafers and returns finished wafers or packaged parts to the user. Custom process flows or process variants can sometimes be made available from commercial foundries, although additional negotiating and payment may be needed for some nonrecurring engineering costs. Some foundries will perform standard unit process steps such as thin-film depositions, patterning, and wet or dry etches at a fixed cost, whereas custom unit processes may incur development costs. Industrial laboratories may offer captive processes for development and limited initial production. University facilities, such as members of the National Nanofabrication Infrastructure Network (NNIN) in the United States, may be used by qualified students and industrial users at each site, or may alternatively be accessible to remote users via a staff member or a local consultant to perform desired services [38]. Some of the university facilities accommodate and encourage industrial employees to work on-site on a fee basis. Within the university facilities, students and faculty members can design devices, develop processes, and perform research with appropriate oversight. Government laboratories and government-sponsored programs also may be available to meet user requirements. Trade groups, networks, and exchanges [39] have emerged as centers for connecting user needs for design services, unit processes, or full fabrication sequences with foundries and laboratories that cater to those needs.

Table 8.3 General comparison of wet-etch site alternatives

Facility	Mode	Advantages	Disadvantages
Commercial foundry	Standard process flow	Fixed processes Easy design variations Well-defined start times Reliable completion times Fixed pricing Ramp to manufacturing Pay for what is used	Few or no process variants Expensive for only a few wafers or devices Process IP confined to foundry Requires complete process run
	Custom process flow	Dedicated flows Inherent ramp to manufacturing	Unknown development cost
	Standard unit process	Lower cost Qualified sequences	Work accomplished at multiple facilities
	Custom unit process	Outsourced development Unit process-level qualification	Higher development costs Higher unit process costs
Industrial laboratory	Technician or operator	Fast processing In-house expertise Allows low-rate initial production	Personnel intensive Capital intensive High maintenance costs Limited ramp to production
	Engineering development	Innovative processes State-of-the-art materials Internally developed IP	Personnel intensive Capital intensive High maintenance costs Requires process transfer
University facility	Industrial user	Novel devices, new processes Self-controlled IP	Minimal infrastructure
	Embedded engineer or technician	Established facilities Direct control of personnel Very fast Simultaneous pilot and device runs	Requires personnel commitments Costly budget item

Table 8.3 (continued)

Facility	Mode	Advantages	Disadvantages
	Local consultant	Established facilities Experienced personnel Can be fast Technology transfer assistance	External expenditure Limited IP control
	Student/faculty	Established facilities Novel devices, new processes Experienced mentors Internal IP	Training required Time consumption Equipment support Equipment downtime
	Remote user	Established facilities Experienced personnel Flexible processes and materials	Can be slow No production External expenditure
Government laboratory	Internal user	Well-endowed facilities Fixed or custom processes Internal IP	Variable funding
	Remote user	Well-endowed facilities Fixed or custom processes	High costs Limited production capability

8.3 Evaluation and Development of Wet-Etch Facilities and Procedures

Wet-etch procedures present concerns common to other aspects of semiconductor and MEMS/NEMS device processing: facilities, equipment, services, wafer handling, safety procedures, and training. Additional considerations may emerge due to the presence of caustic and potentially harmful liquids, as well as the need to control their source, use, and disposition. These concerns and considerations need to be evaluated regardless of whether a wet-etch process is developed internally or provided by outside services.

8.3.1 Facility Requirements

Wet-etch capability places certain requirements on facilities, maintenance, and operating personnel. One exemplary facility may be structured as multiple laboratories with one lab dedicated to highly clean integrated circuit processing, a second lab for CMOS-compatible MEMS and related semiconductor device processing, and a general lab for exploring and developing nonstandard devices and processes. Another facility may designate specific bays to standard (e.g., silicon) IC and clean MEMS processing with other bays designated for compound semiconductor and gold-compatible processing. Another facility may separate wet-chemical processing within clean-room bays by chemical hood, with specific hoods designated, for example, for oxide etching and PR stripping, nitride etching and PR stripping, aluminum etching and PR stripping, pre-furnace wafer cleaning (nonmetal), nongold metal etching; anisotropic wafer etching; compound semiconductor etching, general etching (including gold), and solvent processing. Still other facilities may have no limitations on types of processing in cleanroom fume hoods, except for restrictions to use only preapproved chemicals and materials. Some special requirements for IC, MEMS, and NEMS wet-chemical processing are listed below with brief descriptions.

8.3.1.1 General Facilities

Gowning room – outfitted with lab coats, jump suits, smocks, bouffant caps, hoods, facial protection, safety glasses, goggles, latex and vinyl gloves, and booties

Chemical storage – cabinet with passthroughs for supplying new etchant and for storing partially empty bottles, chemical in-use labels, and material safety data sheets

Chemical disposition – temporary storage for empty and in-use bottles with access to labels for identifying chemicals and bottle contents; containment vessels for local disposition of etchants for heavy metals (e.g., gold etchant)

Cleanroom bays – set up by function and cleanliness control with local or laboratorywide air filtering and conditioning that is graded by particulate count for class 10,000 (general gowned area), class 1000 (clean assembly area), class 100 (general processing area), class 10 (lithography and wafer cleaning areas), and better

Wet-etch stations – one or more stations with fume hoods that may be dedicated for clean processing, semiclean processing, and general processing for contamination control

Acid neutralization system – automated system to collect and neutralize acid and base waste (not HF) from sinks and fume hoods before discharge

Fume scrubber – system to remove harmful vapors from hood exhaust with water dilution

Test bays and benches – contains test and characterization equipment to validate process steps and perform preliminary evaluation of devices

Facility alarms – gas, chemical, acid/base neutralizer, smoke, fire detection, and strobe alarms

Emergency exits – one or more emergency exits for fast laboratory evacuation.

8.3.1.2 Wet-Bench Services

Electricity – adequate power for lights, ventilation, alarms, hot plates, stirrers, temperature controllers, timers, and solenoids as needed for bench operation

Water supply – plumbed deionized water with suitable faucets, taps, and sprayers

Drains – plumbed with separate systems for HF acid drainage and for acid/base neutralization

Nitrogen – plumbed with hoses and nitrogen guns

Compressed air – plumbed for pneumatic actuators

Fume exhaust – adequate draw and external venting for wet benches and user safety

Emergency alarms – nearby push-button switches for laboratory alerts

PA system and phones – nearby public address system for lab announcements.

8.3.1.3 Wet-Bench Equipment

Wet bench with fume hood – flame-retardant polyvinyl chloride and polypropylene [33] wet bench for acids and stainless steel for solvents; proper exhaust and gauges; optional laminar flow and local HEPA filtration; optional deep sinks, gooseneck DI water tap, and industrial water for plenums

Etch tanks – PFA, PTFE, or quartz tanks for acids; stainless steel or polypropylene for most solvents; lids

Hot plates – integrated into etch tanks or set into sinks with temperature control; may be placed on hood work surface; optional stirrers

Rinse tanks – PFA, polypropylene, or PTFE tanks for acids; stainless steel or polypropylene for most solvents; dump rinsers or cascade rinsers for wafer cleaning

Timers and controllers – preferably built into the wet bench

Nozzles – spray nozzles for DI water and filtered blowoff guns for nitrogen

Wands – vacuum wands for individual wafer transfers

Aspirator – flexible tube and nozzle with switch for pumping acids/bases into acid neutralization system

Spin-rinse dryer – chamber that accommodates wafer cassettes; low spin speed for spraying with DI water and high spin speed with heated nitrogen for drying wafers; generally placed near the wet bench

Labware – color-coded or marked PFA, polypropylene, or PTFE cassettes, cassette handles, beakers, graduated cylinders, quartz or Teflon® holders, stirrers, thermometers, and special fixturing

Wipes – lint-free cleanroom wipes for drops, small spills, and blow-drying wafers

Bench space – sufficient room for safe transfer of wafers with adequate counter space

Floor space – sufficient room for operators and additional aisle space for safe passage

Chemical carts – pails or wheeled carts for transporting bottles

Solid waste disposal – wastebaskets for solid waste such as soiled cleanroom wipes; may be covered and vented for solvent or photoresist waste; zip-lock bags for wet cleanroom wipe disposal; dedicated containers for broken substrates and labware

Carboys – polypropylene tanks for collecting discarded solvents.

8.3.1.4 Safety

Personal protection – goggles, face shields, chemical gloves, and chemical aprons

Operating manuals – accessible from near wet bench

Safety procedures – written and accessible from near wet bench

Phones – with numbers for major emergencies and staff contact information for minor emergencies

Emergency alarms – alerts for lab personnel and for emergency response team

Emergency showers – accessible and within reach of wet bench, even with lights out

Emergency eye washes – accessible and within reach, even with lights out

First aid kits – includes tubes of calcium gluconate gel for HF exposure

Spill cart – cart with emergency equipment to contain and treat chemical spills

Materials and chemicals – procedures for chemical storage, use, disposal, and chemical control to minimize contamination risks and ensure safety.

When establishing new facilities or determining which facility to use for wet chemical etching, it is generally advisable to have all process sequences performed in the same facility. Important peripheral considerations are given to optical and e-beam lithography requirements; furnace operations; deposition and material growth processes; wet and dry etching capabilities; and inspection, test, and characterization needs. Wet-etching and wet-processing steps are prominent in most process flows. Because most devices or projects require processing steps beyond that of wet etching, the integration of all processes and wafer transport between steps requires careful consideration.

8.3.2 Wafer Handling Considerations

Wet-etch development and execution requires consideration of wafer handling. For small wafer pieces, a pair of Teflon-coated metal or plastic tweezers or an ETFE basket may suffice. Single wafers may be placed in a PFA or PTFE lollipop-style dipper holder. Multiple wafers benefit from the use of a quartz wafer holder with multiple slots, a standard polypropylene cassette, or a dedicated Teflon cassette. Vacuum wands with conductive PEEK, PFA, polyimide, PTFE, or quartz tips may be used for transferring and blow-drying wafers. Gravity or push-fed cassette-to-cassette transfers are encouraged to avoid direct handling of each wafer. Good handling procedures should prevent wafers from touching each other and minimize contact with any appliance.

Each wafer-handling apparatus is typically allocated to a particular wet bench and restricted to that location. Wet benches may have imposed restrictions to the type of substrate, such as silicon-based substrates in one hood and compound semiconductor substrates in another. For example, wet benches may be set up for extremely clean processes such as wafer cleaning before furnace or epitaxial growth operations, oxide etching and photoresist stripping, nitride etching, standard metal etching, nonstandard metal or general etching, gold-contaminated processing, anisotropic silicon etching, GaAs processing, acid etching, base processing, solvent processing, and specialty processing. In limited facilities, one or two wet benches may suffice: acid/base/alkalis and solvents, or acids and base/solvents. The processing history of the substrates may further dictate restrictions on wet bench accessibility. For example, a facility's procedures may restrict a wafer from any wet bench or equipment dedicated to clean processing for furnace operations.

Wet-etch operations should ensure that movements of all wafers, holders, and etchants be obstruction-free to help prevent wafer damage and to provide for operator safety. Provisions for hand-drying of wafers with a nitrogen gun should ensure an open, unobstructed work area away from the user so that the user may hold the wafers downward and away from the user's face. Inspection of wafers should be done with minimal movement and transport to avoid inadvertent breakage. The

wafers should be kept close to countertop surfaces at all times to minimize breakage, and wafer transfers along aisles to spin-rinse dryers or to another work station should use protective cassettes to avoid breakage.

8.3.3 Safety Concerns

Wet-etch processes have exposed fluids that, by their nature, may be caustic and potentially harmful to a user. Care always needs to be taken or a user could be exposed accidentally to an etchant at any time between the opening of an etchant bottle to the final rinsing and discarding of the etchant. Special precautions should be observed while setting up or using any wet-etch process. Those who can recall holes in clothing from sulfuric acid residues on a wet bench, infiltration of a full-shield face mask with hydrochloric–nitric acid fumes from a tube washing, the dry scent of concentrated hydrofluoric acid, or view of a hydrazine cloud from an overheated hotplate will have a healthy respect for standard, common-sense precautions when wet etching. Operator safety is paramount in performing a wet etch. If the user cannot be safe, then the etch procedure is inappropriate and should not be used. A procedure should be written up and taught for each etch sequence, explaining each apparatus and movement in detail including the order of mixing etchants, operating temperature, holders to be used, and storage or disposal of the etchants and rinse liquids.

Exposure to chemical etchants can cause burns, rashes, eye damage, lung problems, and chronic health issues. Electricity in the wet benches can create shock hazards. The invariable broken glassware and broken wafers can cause cuts to the operator and to others who unwittingly become exposed to the sharp edges if broken glass or wafers are not disposed of properly. An operator must know what to do, where to go, whom to call, and how to clean up or to get assistance in case of a spill, breakage, or incident. At least one layer of protection such as a transparent shield should be located between the user and the etchant at all times so that the user is protected against splashes of liquid or spitting of hot etchant. A practical reminder is this: always have protective clothing and eyewear on, because when accidents happen, it is too late to use any steps of precaution. Experienced users carefully step backwards from equipment while protecting their wafers, and move steadily and predictably down lab aisles.

8.3.4 Training

Training of operators and users is a requirement for safe successful execution of a wet-etch process. Training is best done with an experienced user, along with written or multimedia materials that contain all relevant procedures and precautions. Trainers should oversee a new user during at least one actual etch sequence. Experienced users should be observed by other lab users and politely corrected if

negligence occurs or proper precautions are not taken. Training needs to cover topics of equipment operation, etchant preparation, etchant disposal, wafer handling, etch steps, rinsing and drying steps, and clean-up procedures. Aspects of safety including location of eye washes, chemical showers, emergency exits, spill carts, PA system, phones, and postings of emergency numbers and contact information should also be presented to the prospective user.

8.4 IC-Compatible Materials and Wet Etching

IC-compatible materials include those materials that are used in standard sequences for integrated circuit processing. Historically, MEMS devices have been developed largely on previous-generation equipment from semiconductor facilities, which graciously gifted many academic institutions with their fully or partially depreciated equipment as new-generation equipment for larger wafers and smaller feature sizes emerged. A significant portion of the donated equipment was used to set up bipolar, p-channel, n-channel, and CMOS processes on 4 in. (100 mm) wafers at the university laboratories to fulfill the educational and research needs of circuit-design and process-engineering students. The laboratories' pilot lines were set up with adherence to cleanliness principles, particulate control, and avoidance of contaminants that reduce carrier lifetime, breakdown voltage, and threshold voltage stability of bipolar and MOS circuits. For good reason, the beliefs that cross-contamination from sources of metal such as sodium can harm the performance of integrated circuits and cause shifts over time have prevailed. Consequently, wet etchants that are considered to be electronic grade have sufficiently low values of sodium, trace concentration of metals such as lead, iron, copper, and nickel, and dopants such as phosphorus and arsenic [40].

As such, the following sections on etching processes break down materials of interest into IC-compatible materials (referred to as standard materials) and non-standard materials, separating out metals from the dielectrics and semiconductors.

8.4.1 Oxide and Dielectric Etching

One or more etch sequences of silicon dioxide occur in nearly every MEMS or IC process. Etching of oxide generally uses dry-etch sequences for fine-line semiconductor processes, however, MEMS processes often use wet oxide etches for stripping, etching largely noncritical features, opening contacts, and for extensive lateral etching to remove sacrificial layers.

Silicon dioxide, commonly referred to simply as oxide, etches well at room temperature with hydrofluoric acid (HF) mixed with water. The hydrofluoric acid reacts with the oxide to form water-soluble H_2SiF_6 and water [41]. A buffering agent such as ammonium fluoride may be included to regulate the ionic concentration of HF_2^- in the etchant and provide uniform etch rates over long periods of use [42].

Ammonium fluoride-based etches with acetic acid and ethylene glycol are used for etching oxide passivation layers deposited over pad metals such as aluminum because of reduced attack on the aluminum [43]. Oxide etch rates vary significantly with etchant concentration. Although room-temperature etch baths are prominent, temperature-controlled baths lead to more consistent etch rates and may be desirable for critical timed etches. Stirring has a minor affect on HF-based etchants, although stirring and agitation can change the effective etch rate of pad etchants for passivation oxides. Deionized water is used for rinsing, with five bath changes generally sufficient to quench the etch and to rinse the etchant from the wafer surfaces. The pH and resistivity of the rinse water may be checked or monitored to ensure adequate rinsing time and rates. Drying is typically done with a commercial spin-rinse dryer that includes high-speed axial spinning with heated nitrogen after spray rinsing.

Small features in a dark-field photoresist mask may be difficult to etch consistently with HF-based etchants due to vapor barriers from small pockets of trapped air in the patterned region or etch-resistant silicate formation on the oxide surface, although the etched film can be cleared consistently with an ammonium fluoride etchant. The oxide etch rate depends strongly on the oxide deposition process. Thermally grown oxides on silicon etch the most slowly, whereas less dense, unannealed deposited oxides etch much more quickly. Large amounts of impurities such as boron or phosphorus in the film increase the etch rate, and can be attractive for rapid undercutting of freestanding microstructures. For smaller amounts of boron (<17 molar%), the etch rate of oxide decreases [27]. Oxide damage from ion implantation can also increase the etch rate. Conversely, high temperature annealing can densify deposited films and decrease the etch rate of the densified films to nearly that of thermally grown oxide.

Large amounts of oxide can be etched in HF or buffered HF etchants, and these etchants have a relatively long shelf life in storage or in use. Glass, Pyrex® glassware, and quartz will etch in HF, therefore their use as etch beakers and wafer holders is limited, whereas beakers and holders of acid-resistant materials such as polypropylene (PP), high-density polyethylene (HDPE), polytetrafluoroethylene (PTFE or Teflon), and polyvinylidene fluoride (PVDF) [27] are prominent. Photoresist generally forms an excellent mask except for long exposure to high concentrations of unbuffered hydrofluoric acid, and polysilicon or occasionally silicon nitride layers may be used to mask an oxide etch. A dedicated chemical hood may include, for example, an etch tank for buffered HF etch, another etch tank for concentrated HF (49%), and provision for photoresist stripping. A summary of aspects and considerations for wet etching of silicon dioxide is found in Table 8.4.

Etch rates for typical silicon dioxide etchants are found in Table 8.5. The term buffered hydrofluoric acid (BHF) is used throughout this chapter to denote etchants with mixtures of hydrofluoric acid, ammonium fluoride, and water, rather than the commonly used term buffered oxide etch (BOE) inasmuch as BHF is used for etching materials other than oxide. Diluted HF etchants, or DHF, are generally followed by the portion of concentrated HF to the portion of water by volume.

Table 8.4 Oxide wet-etch sensitivities

	Variable	Effect on etch rate	Etchant	Remarks
1	Etchant concentration	High	HF-, BHF-, or NH_4F-based	Higher acid concentration increases the etch rate; increased dilution in water decreases the etch rate
2	Buffering	Moderate	BHF	NH_4F used as a buffering agent for HF-based etchants for a uniform etch rate
3	Temperature	Moderate	HF, BHF, NH_4F	Increased etchant temperature increases the etch rate
4	Stirring or agitation	None to moderate	HF, BHF, NH_4F	Stirring has little impact on HF etch rates (though may help with small patterned features); stirring or agitation increase the etch rate for NH_4F-based etchants
5	Rinse liquid	None	HF, BHF, NH_4F	Use copious amounts of DI water; spray, dump, cascade, overflow, or dilution rinse
6	Drying	None	HF, BHF, NH_4F	Use spin-rinse-dry or N_2 blow dry
7	Feature size	None to moderate	HF, BHF, NH_4F	Small features can be difficult to etch with HF-based etchants due to salt formation on the surface or vapor locks with photoresist masks; improves with NH_4F-based etchants
8	Deposition technique for oxide	High	HF, BHF, NH_4F	Thermally grown oxide normally etches the slowest; deposited oxides generally etch faster with lower deposition temperature, less annealing and decreased film density
9	Doping level in oxide	Moderate	HF, BHF, NH_4F	Doped oxide, for example, with boron or phosphorus or both, will generally etch faster
10	Annealing	Low to moderate	HF, BHF, NH_4F	Annealing can slow etch rates of LTO and other deposited oxides; minimal affect on etch rate of thermal oxide
11	Etch exhaustion	Low	HF, BHF, NH_4F	HF and BHF etchants show little etch exhaustion
12	Shelf life	Moderate to long	HF, BHF, NH_4F	HF and BHF etchants can last for months
13	Etch beakers and holders	None	HF, BHF, NH_4F	Avoid use of quartz, Pyrex, glass, or metal beakers and holders
14	Etch masks	None	HF, BHF, NH_4F	Photoresist is often used; polysilicon or silicon nitride layers can be effective

Table 8.5 Silicon dioxide etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon dioxide (SiO_2), deposited BPSG	Not specified	HCl(38%): HF(49%): H_2O 10:1:10	Room temperature; BPSG etchant; reduced attack on thermal oxides; DI water rinse [45]
2	Silicon dioxide (SiO_2), thermally grown	11	HF(49%) vapor	20°C vapor, vapor HF etchant; atmospheric pressure; 1 cm over dish of etchant; mask with Si(poly), Si_3N_4 (65:1), Si_3N_4(low-stress) (35:1); PR masks may peel; Etches Pyrex, quartz, SiO_2(LTO) (13 Å/s), SiO_2(PSG) (35 Å/s), SiO_2(PSG, annealed) (25 Å/s); Doesn't significantly etch Au, Cr, Ni, polyimide, Pt, sapphire, Si, Si(poly), W; roughens Al, Cu, Ti; avoid condensation on wafer by removing the wafer from the vapor at 15-sintervals; heat wafer for higher etch rate and higher selectivity to thermal oxide over deposited oxide [27, 28, 46]
3	Silicon dioxide (SiO_2), LPCVD LTO and PSG	13–35	HF(49%) vapor	20°C vapor; vapor HF etchant; atmospheric pressure; low end of range for undoped, annealed films; high end of range for doped, unannealed films; see remarks for thermal oxide with same etchant [27]
4	Silicon dioxide (SiO_2), thermally grown	220	HF(49%) undiluted	Room temperature; HF etchant (49 wt%); DI water rinse [47, 48]
5	Silicon dioxide (SiO_2), deposited PSG	1100–1900	HF(49%) undiluted	Room temperature; PSG etchant; annealed SiO_2 (PSG), 3–5 wt%; DI water rinse [47]
6	Silicon dioxide (SiO_2), thermally grown	380	HF(49%) undiluted	20°C; HF etchant (49 wt%); PR mask OK for short etches; PR will peel or crack for ratios stronger than 3:1 H_2O:HF(49%) [49]; mask with >4000 Å Si(poly) [50], Si_3N_4 (160:1), Si_3N_4(low-stress) (440:1), W (460:1); Etches Al, Ti; DI water rinse [27]

Table 8.5 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
7	Silicon dioxide (SiO_2), deposited	230–600	HF(49%) undiluted	20°C; HF etchant (49 wt%); low end of range for undoped, annealed films; high end of range for doped, unannealed films; see remarks for thermal oxide with same etchant [27]
8	Silicon dioxide (SiO_2), thermally grown	4	HF(49%):H_2O 1:10	20°C; DHF etchant (10:1); mask with PR, Si(poly), Si_3N_4 (20:1), Si_3N_4(low-stress) (75:1), W (>200:1); Etches AlSi (2%) (40 Å/s), Ti (180 Å/s), TiW (1 Å/s); DI water rinse [27]
9	Silicon dioxide (SiO_2), deposited	5–250	HF(49%):H_2O 1:10	20°C; DHF etchant (10:1); low end of range for undoped, annealed films; high end of range for doped, unannealed films; see remarks for thermal oxide with same etchant [27]
10	Silicon dioxide (SiO_2), thermally grown	1	HF(49%):H_2O 1:50	Room temperature; DHF etchant (50:1); mask with PR, Si(poly), Si_3N_4 (>5:1), Si_3N_4(low-stress) (>5:1); DI water rinse [51]
11	Silicon dioxide (SiO_2), deposited	1–10	HF(49%):H_2O 1:50	Room temperature; DHF etchant (50:1); low end of range for undoped, annealed films; high end of range for doped, unannealed films; see remarks for thermal oxide with same etchant [51]
12	Silicon dioxide (SiO_2), thermally grown	0.4	HF(49%):H_2O 1:100	Room temperature; DHF etchant (100:1); DI water rinse [52]
13	Silicon dioxide (SiO_2), BSG	5	HF(49%): HNO_3(70%): H_2O 1:100:100	Room temperature; R-etchant; BSG etchant; preferential to boron-doped glass; etches thermal SiO_2 at 1 Å/s; DI water rinse [8]
14	Silicon dioxide (SiO_2), PSG	550	HF(49%): HNO_3(70%): H_2O 3:2:100	Room temperature; P-etchant; PSG etchant; preferential to phosphorus-doped glass; etches thermal SiO_2 at 2 Å/s; DI water rinse [8]
15	Silicon dioxide (SiO_2)		HF(49%): HNO_3(70%): Acetic 1:3:2	Room temperature; HNA etchant; DI water rinse [53]

Table 8.5 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
16	Silicon dioxide (SiO_2), thermally grown	17	HF(49%): NH_4F (40%) 1:5	20°C; BHF etchant (5:1); mask with PR, Si(poly) (>100:1), Si_3N_4 (110:1), Si_3N_4(low-stress) (250:1), W (>50:1); Etches Ag (1 Å/s), Al (2 Å/s), AlSi (2%) (23 Å/s), Al_2O_3 (27 Å/s), Cu (1 Å/s), graphite (3 Å/s), polyimide (1 Å/s), Pyrex (7 Å/s), quartz (22 Å/s), Si_3N_4 (PECVD) (1.5–10 Å/s), SiO_2 (LTO) (20–25 Å/s), SiO_2 (PECVD) (40–80 Å/s), SiO_2 (PSG) (75–110 Å/s), Ti (fast), TiW (17 Å/s); Etches slightly Cr (0.1 Å/s), Ge(poly) (0.3 Å/s), Mo (0.1 Å/s), Ni (0.2 Å/s), NiCr (80/20) (0.2 Å/s), Parylene Type C (0.1 Å/s), Si(poly) (0.1 Å/s), SiGe(poly) (0.1 Å/s), TiN (0.4 Å/s), TiW(10/90) (0.1 Å/s), Va (0.3 Å/s), W (0.3 Å/s); Doesn't significantly etch Au, Nb, Pd, Pt, sapphire, Si, Ta; use TiN or TiW rather than Ti for adhesion layers; DI water rinse [27, 28]
17	Silicon dioxide (SiO_2), TEOS	10–80	HF(49%): NH_4F (40%) 1:7	30°C; BHF etchant (7:1) with FC-170 surfactant (1 part per 1600); etch rate decreases with annealing and dopant; DI water rinse [54]
18	Silicon dioxide (SiO_2), deposited	20–110	HF(49%): NH_4F (40%) 1:5	20°C; BHF etchant (5:1); low end of range for undoped, annealed films; high end of range for doped, unannealed films; see remarks for thermal oxide with same etchant [27]
19	Silicon dioxide (SiO_2), thermally grown	15	HF(49%): NH_4F (40%) 1:6	Room temperature; BHF etchant (6:1); mask with PR, Si(poly), Si_3N_4 (>90:1), Si_3N_4(low-stress) (>90:1); DI water rinse [51]
20	Silicon dioxide (SiO_2), deposited	25–100	HF(49%): NH_4F (40%) 1:6	Room temperature; BHF etchant (6:1); low end of range for undoped, annealed films; high end of range for doped unannealed films; see remarks for thermal oxide with same etchant [51]
21	Silicon dioxide (SiO_2), deposited on Al		NH_4F (40%): Acetic 1:1	Room temperature; reduced attack on aluminum; DI water rinse [45]

Table 8.5 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
22	Silicon dioxide (SiO_2), deposited on Al	6	NH_4F (40%):Acetic:propylene glycol:H_2O plus surfactant 13:32:6:49	20°C; Pad Etch 4 from Ashland; rate is for SiO_2 (LTO, unannealed); mask with PR, Si_3N_4 (90:1), Si_3N_4(low-stress) (>100:1), Si_3N_4 (PECVD) (25:1); Etches Pyrex (3 Å/s), quartz (5 Å/s), SiO_2 (5 Å/s), SiO_2 (PECVD, unannealed) (25 Å/s), SiO_2 (PSG, unannealed) (35 Å/s); Slightly etches Al (0.3 Å/s), AlSi (2%) (2.5 Å/s), Ti (0.3 Å/s); Doesn't significantly etch Cr, Mo, Nb, sapphire, Si, Si(poly), Ta, Va, or W; DI water rinse [28]
23	Silicon dioxide (SiO_2), thermally grown	13	Ammonium fluoride buffer, hydrofluoric acid	20°C; Transene Buffer HF Improved; PR masks; faster with deposited and doped oxides; DI water rinse [55]
24	Silicon dioxide (SiO_2), deposited on Al	67	Ammonium fluoride, glacial acetic acid, Al etch inhibitor, surfactant	22°C; Transene Silox Vapox III; mask with PR; minimal Al attack; DI water rinse [55]

The etch rate tables throughout this chapter emphasize recipes mixed from standard integrated circuit laboratory chemicals, although many other fine etchant recipes exist. The etch tables are separated into dielectrics then metals, first for materials compatible with clean IC processing and later for nonstandard materials of interest to the MEMS community. The etched material name is generally followed by its chemical symbol in parentheses for ease in searching. The particular deposition technique may also be indicated. Within each table, the etchants and etch processes are organized alphabetically first by etched material, then by etchant components, and then by etch rate for similar etchants (e.g., with different temperatures or citations). Within each etch mixture, the chemical components are generally organized alphabetically, with hydrogen peroxide, diluents such as acetic acid, and water positioned last in the component sequence. The chemical concentration in weight percent is generally listed in parentheses after the chemical symbol, except for those with 100% concentrations and solid forms. Acetic acid (>99%) is denoted simply as acetic. Organic solvents and etchants are generally denoted with an acronym such as IPA for isopropyl alcohol, EtOH for ethyl alcohol, MeOH for methyl alcohol, and KOH for potassium hydroxide. Semiconductor or reagent grade chemicals are available from a number of fine suppliers [44].

The composition ratios for chemical mixtures follow the etchant components, with numbers separated by colons to indicate the relative volumes (not weight) of each component unless otherwise indicated. The sequence of the etchant components does not imply the order in which the components should be added. For example, it is not to be inferred that water is added last (remember to add acids to water, not the other way around). Commercial etchants of particular interest with published etch rates are included, although the components of the etchant may not be fully known.

The etch rates are presented uniformly in angstroms per second (Å/s), in part to keep the etch rates of interest in the single-digit range and above. Etch rates of 1–10 Å/s are generally suitable for film thicknesses up to several thousand angstroms; etch rates of 100–1000 Å/s or more are generally suitable for extensive lateral etching or removal of significant portions of the substrate such as a backside anisotropic etch. Etch rates less than 1 Å/s are generally too slow for common use, although the information is valuable to determine the selectivity of the etchant to masking layers and other exposed layers during the etch sequence or to layers that become exposed during the overetch portion of the etch step. Notes of interest and references are included for each etchant, including etch rates and selectivities to other materials when available. The recipes are believed to be accurate, although many have not been used or confirmed by the author. Some etch rates have been rounded slightly from the literature values, and some etchant components have been tweaked to align them with commercial concentrations for standard electronics-grade reagents. The recipes and etch rates are intended to serve as a guide to wet chemical etching for a wide variety of MEMS-related materials, and a selected etchant should be verified by the user with samples under representative etching conditions prior to actual use.

Wet etching of other dielectric films such as silicon nitride have characteristics and concerns similar to those of oxide etching. Silicon nitride films, being

much harder and more chemically resistant than silicon dioxide, are best etched using plasma or reactive ion etching because the etch rates in liquid etchants are slow and the choice of suitable masking materials is limited. Etchants for silicon nitride include the family of etchants for silicon dioxide (although much slower), and phosphoric-acid based etchants with high selectivity to oxide. Phosphoric acid is generally heated to obtain reasonable etch rates. Overall etch times for silicon nitride are similar to those of oxide, because the thickness of silicon nitride films for IC or MEMS devices is often less than the oxide thickness. The deposition technique has a direct impact on the etch rates of silicon nitride, similar to its impact on oxide. Stoichiometric LPCVD silicon nitride films and stress-compensated silicon nitride films with higher silicon fractions are more resistant to etchants than the more porous PECVD or sputtered films. Etch tanks and carriers for room-temperature HF-based etches can use polypropylene, PFA or PTFE carriers and beakers. Heated phosphoric-acid based etches may use PFA, Pyrex, or quartz beakers and holders. Standard photoresist processes can provide a suitable mask for dry etching and some HF-based etching of silicon nitride, although the resist is generally not suitable for elevated-temperature phosphoric acid etching or for high HF concentrations. A pretreatment including a brief oxide etch may improve nitride etch-rate uniformity. Etch rates for silicon nitride are compiled in Table 8.6.

8.4.2 Silicon, Polysilicon, and Germanium Isotropic Etching

With single-crystal silicon wafers comprising the vast majority of substrates used for IC and MEMS processing, silicon etching has many well-established, diverse processes for removing silicon in preferential shapes and locations. Anisotropic silicon etching, a long-term standard for backside cavity and silicon diaphragm formation, has given way to vertical wall etching with deep reactive ion etching for many applications. Frontside features such as trenches and channels with aspect ratios (etch depth to etch width) greater than 1:1 are generally dry etched. Traditional mesa processes with liquid silicon etches have been upgraded to plasma processing. High removal rates with plasma torches are available for noncontact wafer thinning with argon and CF_4 at 20 μm/min [59]. Etch stop mechanisms based on electrochemistry or high boron-doped silicon have been superseded by embedded oxide etch stops with bonded wafer technology and by other methods for silicon-on-insulator formation that provide dry-etch alternatives to wet etching of silicon. The bulk thinning of wafers for flip-chip packages and chip-scale packaging remains predominantly a wet-etch process through a combination of mechanical grinding and chemical etching. Anisotropic silicon etchants that contain sodium or potassium present contamination concerns to semiconductor processes because of the potential for threshold voltage drift in MOSFETs; thus, they are considered nonstandard. Anisotropic silicon etching and silicon etch stops are discussed later in this chapter.

Table 8.6 Silicon nitride etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and References
1	Silicon nitride (Si_3N_4), LPCVD stochiometric	0.75	H_3PO_4(85%)	160°C; strip or mask with Si(poly), SiO_2 (LTO) (>20:1), SiO_2 (PSG) (2:1); Etches Al (85 Å/s), AlSi (2%) (160 Å/s), Al_2O_3 (1 Å/s), Cr (17 Å/s), PR (>20 Å/s), Si_3N_4(PECVD) (3 Å/s); Etches slightly Ge(poly) (<0.1 Å/s), Parylene Type C (0.1 Å/s), Pyrex (0.6 Å/s), quartz (<0.1 Å/s), sapphire (<0.01 Å/s), Si (<0.1 Å/s), Si(poly) (<0.1 Å/s), SiGe(poly) (<0.1 Å/s), SiO_2-thermal (<0.1 Å/s), TiW (0.4 Å/s); Doesn't significantly etch Au, Nb, Ta; heated bath with reflux; PFA tank; DI water rinse [27, 28]
2	Silicon nitride (Si_3N_4), LPCVD low stress	0.45	H_3PO_4(85%)	160°C; strip or mask with Si(poly), SiO_2 (LTO) (>13:1); SiO_2 (PSG) (1:1); see remarks for stochiometric Si_3N_4 with same etchant [27]
3	Silicon nitride (Si_3N_4), CVD	0.4–3	H_3PO_4(85%)	140–200°C; etch rate 1.6 Å/s at 180°C; mask with SiO_2(CVD) (>4:1); Etches Si (0.05 Å/s) at 180°C; use reflux system to reconstitute water vapor; DI water rinse [25]
4	Silicon nitride (Si_3N_4), PECVD high index	3.3	H_3PO_4(85%)	160°C; strip or mask with Si(poly), SiO_2 (LTO) (95:1); SiO_2 (PSG) (7:1); see remarks for stochiometric Si_3N_4 with same etchant [28]
5	Silicon nitride (Si_3N_4), LPCVD stochiometric	2.3	HF(49%) undiluted	20°C; HF etchant (49 wt%); mask with Si(poly) or PR for short times; etches SiO_2 (>300 Å/s), W (1 Å/s); DI water rinse [27]
6	Silicon nitride (Si_3N_4), LPCVD low stress	1	HF(49%) undiluted	20°C; HF etchant (49 wt%); mask with Si(poly) or PR for short times; etches SiO_2 (>300 Å/s), W (1 Å/s); DI water rinse [27]

Table 8.6 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and References
7	Silicon nitride (Si_3N_4), LPCVD stochiometric	0.2	HF(49%):H_2O 1:10	20°C; DHF etchant (10:1); mask with PR, Si(poly) or W; etches SiO_2 (>4 Å/s), TiW (1 Å/s); DI water rinse [27]
8	Silicon nitride (Si_3N_4), PECVD	1–5	HF(49%):H_2O 1:10	23°C; DHF etchant (10:1); DI water rinse [56]
9	Silicon nitride (Si_3N_4), CVD		HF(49%): HNO_3(70%) 3:10	70°C; etches Si rapidly [57]
10	Silicon nitride (Si_3N_4), LPCVD stochiometric	0.15	HF(49%): NH_4F (40%) 1:5	20°C; BHF etchant (5:1); mask with PR or Si(poly); Etches SiO_2 (>15 Å/s), Ti (fast), TiW (17 Å/s), W (<0.3 Å/s); Doesn't etch Au, Cr, Nb, Pd, Pt; nitride etch rate decreases with increasing refractive index; DI water rinse [27]
11	Silicon nitride (Si_3N_4), PECVD low index	10	HF(49%): NH_4F (40%) 1:5	20°C; BHF etchant (5:1); mask with PR or Si(poly); see remarks for stoichiometric Si_3N_4 with same etchant [28]
12	Silicon nitride (Si_3N_4), PECVD high index	1.3	HF(49%): NH_4F (40%) 1:5	20°C; BHF etchant (5:1); mask with PR or Si(poly); see remarks for stoichiometric Si_3N_4 with same etchant [28]
13	Silicon nitride (Si_3N_4), deposited	2	Ortho-phosphoric acid	180°C; Transetch-N; no PR; mask with SiO_2 (125:1); silicon selectivity (125:1); Pyrex or quartz tank; add water to replace evaporated water; DI water rinse [58]

Dry etching of polysilicon films with a photoresist mask is quite prevalent in IC and MEMS processing, in part because the thickness of the deposited polysilicon films is typically less than a few micrometers, which makes dry etching cost effective. Wet etching of polysilicon with anisotropic wet etchants provides similar results to isotropic etches, because the grain structure of polysilicon has little long-range order and only individual grains are subject to the anisotropy. Wet etching of polysilicon may be preferred over dry etching for clear-field features with small aspect ratios and wide lines, along with the need to remove the polysilicon layer concurrently from the backside of the wafer. Isotropic etchants for silicon or polysilicon include nitric acid and hydrofluoric acid mixed with water or acetic acid to reach the desired concentration [60–62]. The nitric acid reacts with the exposed silicon surface to form silicon dioxide, which is promptly etched away by the hydrofluoric acid. Ammonium fluoride can substitute for the hydrofluoric acid, because HF is formed from the nitric acid [27]. Typical masks for wet or dry etching of polysilicon include photoresist for small etch depths, and oxide, nitride, or metal for deeper etches. Typical etch chemistries and etch rates for isotropic etching of single-crystal silicon, polycrystalline silicon, and germanium are listed in Table 8.7. Some of the etchants exhibit modest anisotropy.

8.4.3 Standard Metal Etching

Thin-film metal layers serve important roles in IC and MEMS processing to help create substrate contacts, electrical interconnections, electrodes, reflective structures, and hard masks for underlying layers. Etchants for metals are generally acid-based and are available in various concentrations and mixtures. The etch rates are primarily dependent on the acid concentration, type of metal, and etch temperature, and secondarily dependent on alloy content in the metal layer, agitation, etchant exhaustion, and storage time before use, particularly if the etchant contains a decaying component such as hydrogen peroxide. PFA and polypropylene cassettes and holders are standard equipment for the handling and transport of wafers. Deionized water serves as a suitable rinse liquid in a dump rinser, followed by nitrogen blow-drying or the passing of the substrates through a spin–rinse–dry cycle. Because metals are of particular concern in shortening carrier recombination lifetimes of semiconductor components, precautions should be made to separate metal-etch facilities and the labware used for clean wafer processing.

Photoresist masks dominate metal patterning sequences, although deposited oxides, nitrides, and other metals may also serve as suitable etch masks. Verification of etch completion can often be done visually and reinforced with microscope inspection because one is able observe the dramatic shift in reflectivity when metal is removed and underlying layers become exposed. Profilometry can be used for validating etch completion by measuring step heights, however, noncontact ellipsometry or spectrometry will reveal the thickness of the underlying material to validate removal of the metal layer.

Table 8.7 Germanium, silicon, and polysilicon isotropic etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Germanium (Ge), LPCVD poly	77	H_2O_2(30%) undiluted	50°C; mask with photoresist, Si_3N_4, SiO_2 (LTO); Etches Cr (20 Å/s), TiW, W (25 Å/s); Etches slightly Al (thickens), AlSi (2%) (<0.1 Å/s), SiGe(poly) (<0.1 Å/s); Doesn't significantly etch Parylene Type C, polyimide, Pyrex, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2; DI water rinse; Doesn't significantly etch poly-SiGe with Ge fraction less than 0.7 [28, 63]
2	Germanium (Ge), (111)	5	H_2O_2(30%):H_2O 1:5	26°C; (111) surface; DI water rinse [64]
3	Germanium (Ge), (100)	40	H_3PO_4(85%): H_2O_2(30%):H_2O 1:6:3	30°C; etches Ge(110) 50 Å/s, Ge(111) 30 Å/s; DI water rinse [65]
4	Germanium (Ge), (100)	1800	HF(49%): H_2O_2(30%) 1:1	25°C; (100) direction; etches faster in (111) (3500 Å/s) and (110) directions (6500 Å/s); orientation-dependent; agitate; DI water rinse [66]
5	Germanium (Ge), (111)	4200	HF(49%): H_2O_2(30%) 2:1	25°C; Ge(111) surface; Ge(100) etches slower, Ge(110) etches faster; highly selective to silicon; DI water rinse [64, 67, 68]
6	Germanium (Ge), (111)	330	HF(49%): H_2O_2(30%):H_2O 1:2:10	25°C; Ge(111) surface; DI water rinse [67]
7	Germanium (Ge), (100)	700	HF(49%): H_2O_2(30%):H_2O 1:1:4	26°C; (100) surface; preferential etchant; fastest for (110) surface and low doping; DI water rinse [64]
8	Germanium (Ge), single-crystal	4000	HF(49%): HNO_3(70%) 1:9	Room temperature; rates are approximate; DI water rinse [69]
9	Germanium (Ge), single-crystal		HF(49%): HNO_3(70%):Acetic 3:5:3	Room temperature; HNA etchant; also CP-4A etchant; etch rate increases with CP-4 etchant (Camp #4 etchant) with ~0.5% bromine [26]); DI water rinse [70]

Table 8.7 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
10	Germanium (Ge), (100)	2100	HF(49%): HNO_3(70%):Acetic 18:8:5	Room temperature; HNA etchant; agitate to remove bubbles and reduce hillock formation; DI water rinse [71]
11	Germanium (Ge), (100)	4300	HF(49%): HNO_3(70%):Acetic 18:8:5	Room temperature; HNA etchant; agitate to remove bubbles and reduce hillock formation; DI water rinse [71]
12	Germanium (Ge)		HNO_3(70%) undiluted	Warm; DI water rinse [72]
13	Germanium (Ge), LPCVD poly	150	HNO_3(70%): NH_4F (40%):H_2O 126:5:60	20°C; mask with nitride; etches thermal oxide (1.5 Å/s), deposited oxide (2–65 Å/s); DI water rinse; see remarks for single-crystal silicon with same etchant [28]
14	Germanium (Ge), bulk	35	NH_4OH(29%): H_2O_2(30%):H_2O 1:6:48	Room temperature; DI water rinse [73]
15	Germanium (Ge)	250	Nitric, HF, and acetic	20°C; Transene RSE-563; mask with SiO_2; isotropic; DI water rinse [74]
16	Silicon (Si), single-crystal	460–830	BrF_3 vapor, reduced pressure	Room temperature; BrF_3 vapor etchant; pulsed etching; 1 min per pulse; 500 mTorr; etch selectivities >1000 for oxide, hard-baked resist, Al, Cu, Au, Ni; slightly etches Si_3N_4 (400:1 to 800:1 selectivity) [75]
17	Silicon (Si)		HF(49%): HNO_3(70%) 1:4	20°C; DI water rinse [53]
18	Silicon (Si), poly	700	HF(49%): HNO_3(70%) 1:3	Room temperature; DI water rinse [76]
19	Silicon (Si), single-crystal	40–8000	HF(49%): HNO_3(70%) 2:98 to 34:66	30°C; with stirring and sample rotation; etch rate increases with increasing HF; rate reduces with use; DI water rinse [77]

Table 8.7 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
20	Silicon (Si), poly	90	HF(49%): HNO_3(70%):H_2O 2:70:28	Room temperature; HNW etchant; DI water rinse [45]
21	Silicon (Si), single-crystal	1200–>27,000	HF(49%): HNO_3(70%):H_2O varies	25°C; HNW etchant; rate increases with agitation; rate decreases with use; substituting water for acetic acid reduces etch rate; DI water rinse [61, 78]
22	Silicon (Si), poly	25	HF(49%): HNO_3(70%):Acetic 1:20:20	Room temperature; HNA etchant; stir constantly; slightly etches oxide; mix fresh; DI water rinse [45]
23	Silicon (Si), single-crystal	5800	HF(49%): HNO_3(70%):Acetic 3:5:3	Room temperature; HNA etchant; also CP-4A etchant; fast chemical polish; DI water rinse [22]
24	Silicon (Si), single-crystal	1200–>80,000	HF(49%): HNO_3(70%):Acetic varies	25°C; HNA etchant; mask with Si_3N_4, SiO_2, black wax (room temperature), etches 600–3200 Å/s at 2:1:3 HNO_3:HF:Acetic; rate increases with agitation; rate decreases with use; rate decreases with light doping; DI water rinse [61, 78]
25	Silicon (Si), single-crystal	25	HNO_3(70%): NH_4F (40%):H_2O 126:5:60	20°C; mask with PR cautiously, SiO_2 (15:1), Si_3N_4 (750:1), Si_3N_4(low-stress) (500:1); Etches Ag (8 Å/s), Al (10 Å/s), AlSi (2%) (65 Å/s), Al_2O_3 (2–17 Å/s), Cr (1.5 Å/s), Cu (6 Å/s), Ge(poly) (150 Å/s), graphite (10 Å/s), Mo (1800 Å/s), Nb (13 Å/s), Ni (3.5 Å/s), Pyrex (20 Å/s), quartz (2 Å/s), Si_3N_4(PECVD) (2–10 Å/s), Si(poly) (15–50 Å/s), SiGe(poly) (90 Å/s), SiO_2 (LTO) (2 Å/s), SiO_2 (PECVD) (4–17 Å/s), SiO_2 (PSG) (30–65 Å/s), Ta (1 Å/s), Ti (50 Å/s), TiW (4 Å/s), Va (1600 Å/s), W (2 Å/s);

Table 8.7 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
				Etches slightly sapphire (0.1 Å/s); Doesn't significantly etch Au, Parylene Type C, Pd, polyimide; Pt, TiN; mix several hours before use; agitate for improved uniformity; etch rate decreases with use; DI water rinse [27, 28]
26	Silicon (Si), LPCVD poly	15–50	HNO_3(70%): NH_4F (40%):H_2O 126:5:60	20°C; doping-level dependent; see remarks for single-crystal silicon and same etchant [28]
27	Silicon (Si), deposited amorphous	1.2	NH_4OH(29%):H_2O 1:10	60°C; DI water rinse [79]
28	Silicon (Si), single-crystal	165	SF_6:H_2 vapor 1:1000	1060°C; SF_6 vapor etchant [80]
29	Silicon (Si), single-crystal	77	XeF_2 vapor, reduced pressure	20°C; XeF_2 vapor etchant; 2.6 Torr; mask with Al (>1000:1), PR, Si_3N_4 (35:1), Si_3N_4(low-stress) (>1000:1), SiO_2 (>1000:1); Etches Ge, Mo, poly (30 Å/s), Nb, Ta, TiW, SiGe, Ti (5 Å/s), Va, W (13 Å/s) Doesn't significantly etch Al, AlSi (2%), polyimide, quartz, SiO_2, ZnO [81]; Doesn't etch acrylic, Al, Ga, Ni, photoresist, Si_3N_4, SiC, Pt [82]; strip native oxide prior with BHF etchant (10:1); etch rate is strongly feature and load dependent [27, 28]
30	Silicon (Si), LPCVD poly	30	XeF_2 vapor, reduced pressure	Room temperature; XeF_2 vapor etchant; see remarks for single crystal silicon above [27]
31	Silicon (Si)	100	Nitric and HF	25°C; Transene RSE-200; SiO_2 mask; isotropic; DI water rinse [83]
32	Silicon–germanium (SiGe), (100), epi	17	HF(49%): H_2O_2(30%):Acetic 1:2:3	Room temperature; $Si_{0.7}Ge_{0.3}$; etches slightly Si (no Ge) ~0.02 Å/s; DI water rinse [84]

Table 8.7 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
33	Silicon–germanium (SiGe), (100), MBE	18	HF(49%): H_2O_2(30%):Acetic 1:2:3	25°C; p-type $Si_{0.6}Ge_{0.4}$; etches slightly Si (<0.02 Å/s); n-doped $Si_{0.6}Ge_{0.4}$ has faster etch rate (38 Å/s for 1×10^{18} cm^{-3} Sb); higher Ge fraction increases etch rate (860 Å/s for 100% Ge with 50,000:1 selectivity over Si); wait 100–180 min after mixing before etching; similar effects with H_2O replacing acetic acid though slower; DI water rinse [85]
34	Silicon–germanium (SiGe), (100), MBE	3.5	HF(49%): HNO_3(70%):H_2O 5:40:20	22°C; HNW etchant; $Si_{0.6}Ge_{0.4}$; etches slightly Si (0.27 Å/s); etch rates increase with higher HF or HNO_3 concentrations; etch selectivity increases with lower HNO_3 concentration; DI water rinse [86]
35	Silicon–germanium (SiGe), (100), MBE	6.8	HF(49%): HNO_3(70%):H_2O 1:350:300	22°C; HNW etchant; $Si_{0.7}Ge_{0.3}$; etches slightly Si (0.07 Å/s); substituting acetic acid for H_2O doubles etch rates for SiGe and Si while retaining 100:1 selectivity; DI water rinse [87]
36	Silicon–germanium (SiGe), LPCVD poly	90	HNO_3(70%): NH_4F (40%):H_2O 126:5:60	20°C; see remarks for single-crystal silicon and same etchant [28]
37	Silicon–germanium (SiGe), RTCVD poly	3.3	NH_4OH(29%): H_2O_2(30%):H_2O 1:1:5	75°C; $Si_{0.6}Ge_{0.4}$; etches slightly Si-poly (0.1 Å/s), SiO_2 (0.03 Å/s); n-doped $Si_{0.6}Ge_{0.4}$ increases etch rate; p-doped $Si_{0.6}Ge_{0.4}$ decreases etch rate; higher Ge fraction increases etch rate (1100 Å/s for 100% Ge-poly); DI water rinse [88]

Standard metals, as used in this chapter, include aluminum, titanium, and tungsten. Etchants with nitric and phosphoric acids convert exposed aluminum to aluminum oxide with the nitric acid, and then etch the oxide layer with the phosphoric acid. Faster etch rates are generally achieved by elevating the etchant temperature or increasing the etchant concentration. Table 8.8 contains etchants and etch rates for various standard metal layers.

8.4.4 Photoresist Removal Techniques and Wafer Cleaning Processes

Removal of patterned photoresist occurs multiple times in nearly every IC or MEMS process and often follows immediately after the etching of an underlying film. Although freshly made and premixed commercial strippers form the majority of PR stripping processes, plasma-stripping of resist in a low-pressure (e.g., 300 mTorr) oxygen plasma often presents a clean, fast, and efficient way of removing resist from the fronts and backsides of wafers with thin photoresist residue or thick, hard-baked photoresist that has been exposed to harsh etchants or high-energy plasmas.

Freshly mixed resist strippers with sulfuric acid and hydrogen peroxide (described as "piranha" by those who have experienced a drop or two of this self-heating combination on exposed skin) also provide a quick way to remove resist from wafers. Wet stripping of resists that cause effervescent bubble formation can lift and float wafers into undesirable positions, invoking the need for aggressive agitation and pre-emptive withdrawal and reinsertion of a wafer holder or cassette to knock off aggregated bubbles on wafers, particularly those wafers with thick single- or double-sided resist. Organic solvents such as acetone can effectively remove resist prior to postbaking, although they can be ineffective after hardening and exposure of the resist to plasma etching. Liftoff techniques remove the resist and undercut overlying metal films, often with ultrasonically agitated acetone in a metal tank.

Wafer cleaning cycles prior to oxidation cycles or LPCVD depositions will remove some residual resist, however, it is expected that the photoresist stripping sequence will remove all of the resist prior to wafer cleaning. PFA or quartz beakers and holders are generally used for wet stripping of resist, which can take place at elevated temperatures up to about 120°C. For elevated-temperature acidic strippers, rinsing of wafers immediately after resist removal must be done carefully to avoid spitting of the acid and water when the two meet on the hot wafer surfaces. Dump rinsing after the strip step effectively dilutes and removes the acid, base, or solvent, followed by a spin–rinse–dry cycle or use of a nitrogen gun to blow-dry the wafers. Visual validation of resist removal can be augmented with microscope inspection for residual resist that may show as thin, redeposited sheets of hardened resist on underlying wafer features.

The tables given below present relevant procedures for photoresist removal. Although not exhaustive, they provide the MEMS and integrated MEMS developer with information on common resist-related operations with chemicals commonly available in a cleanroom processing environment. Table 8.9 lists a range of wet

Table 8.8 Standard metal (Al, Ti, W) etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Aluminum (Al), deposited	870	H_2SO_4(96%): H_2O_2(30%) 56:1	120°C; high-sulfuric piranha; Etches Ag (100 Å/s), AlSi (2%) (30 Å/s), Al_2O_3 (3–15 Å/s), Cr (1–3 Å/s), Cu (15 Å/s), Mo (3 Å/s), Nb (1 Å/s), Ni (65 Å/s), NiCr (15 Å/s), polyimide (2800 Å/s), Ti (40 Å/s); Etches slightly Ge(poly) (softens), Parylene Type C (0.4 Å/s), Pt (0.5 Å/s), TiW (0.1 Å/s); Doesn't significantly etch Au, Pyrex, quartz, sapphire, Si, Si(poly), SiGe(poly), Si_3N_4, SiO_2, Ta; exothermic; add H_2O_2 immediately prior to use; DI water rinse [27, 28]
2	Aluminum (Al), deposited		H_2SO_4(96%): HCl(38%):H_2O 1:1:1	20–50°C; doesn't significantly etch Si, SiO_2; DI water rinse [45]
3	Aluminum (Al), deposited	33	H_3PO_4(85%) undiluted	50°C; etches slightly Si, SiO_2; DI water rinse [45]
4	Aluminum (Al), deposited	100	H_3PO_4(85%): H_2O_2(30%):H_2O 8:1:1	35°C; Krumm etchant; hardbake PR for improved etch resistance; etch rate increases to 120 Å/s at 50°C, 300 Å/s at 80°C; also etches GaAs; DI water rinse [26, 89]
5	Aluminum (Al)	25	H_3PO_4(85%): HNO_3(70%) 16:1	40°C; add water to reduce etch rate; agitate; DI water rinse [26]
6	Aluminum (Al), evaporated	15	H_3PO_4(85%): HNO_3(70%):H_2O 16:1:4	Room temperature; DI water rinse [90]
7	Aluminum (Al), evaporated	6	H_3PO_4(85%): HNO_3(70%):Acetic: H_2O 4:1:4:1	24°C; PAN etchant (phosphoric-acetic-nitric acids); etch rate increases with temperature; DI water rinse [91]

Table 8.8 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
8	Aluminum (Al), deposited	15–50	H_3PO_4(85%): HNO_3(70%):Acetic: H_2O 16:1:1:2	35–45°C; PAN etchant; faster etch rate with higher temperature; rate varies with Cu and Si in Al alloy; clear H_2 bubbles with agitation; DI water rinse [30]
9	Aluminum (Al), deposited on GaAs		HCl(38%):H_2O 1:2	80°C; can be used with GaAs; DI water rinse [8]
10	Aluminum (Al), sputtered	1400	HCl(38%): H_2O_2(30%):H_2O 8:1:1	30°C; etch rate increases to 1700 Å/s at 50°C; hardbake PR for improved etch resistance; DI water rinse [89]
11	Aluminum (Al), deposited	100	HCl(38%): HNO_3(70%):H_2O 3:1:2	30°C; mask with PR; Etches Ag, Au (115 Å/s), AlSi (2%), Cu (100 Å/s), Mo (110 Å/s), Ni (17 Å/s), Pd (65 Å/s); Etches slightly Al_2O_3(0.2 Å/s), SiO_2(PECVD) (0.1 Å/s), Pt (0.6 Å/s), Ta (0.3 Å/s), Ti (0.1 Å/s), TiW (0.6 Å/s), W (0.9 Å/s); Doesn't significantly etch Cr, Nb, polyimide, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2(LTO), SiO_2(PSG); water added to reduce PR attack; self-heating; DI water rinse [28]
12	Aluminum (Al)	4000–8000	HCl(38%): HNO_3(70%):H_2O 10:1:9	50°C; Al and Al alloys; DI water rinse [92]
13	Aluminum (Al), deposited	40	HF(49%):H_2O 1:10	20°C; DHF etchant (10:1); etch rate for AlSi (2%); rate drops for high HF concentrations (0.7 Å/s for HF etchant (49 wt%), 0.4 Å/s for anhydrous HF [93]); mask with PR; Etches SiO_2 (4 Å/s), SiO_2-LTO (6 Å/s), SiO_2-PSG (80–250 Å/s), Ti (180 Å/s), TiW (1 Å/s);

Table 8.8 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
				Etches slightly SiGe(poly) (<0.1 Å/s), Si_3N_4 (0.2 Å/s), Si_3N_4(low-stress) (<0.1 Å/s); Doesn't significantly etch Ag, Au, Cr, Cu, Ge(poly), Mo, Nb, Ni, NiCr, Pd, polyimide, Pt, Si, Si(poly), Ta, TiN, TiW, Va, W; DI water rinse [27]
14	Aluminum (Al), deposited on silicon	30–550	Phosphoric, nitric and acetic acids	25–75°C; 40°C typical (80 Å/s); Transene Aluminum Etchant Type A; etches faster with higher etchant temperature; mask with PR, Si_3N_4, SiO_2; Etches Cr (slightly), Cu, GaAs, Ni; Doesn't significantly etch Au, NiCr, Si, Si(poly), Ta, TaN, Ti, W; glass, Teflon or polypropylene tank; stir or agitate for faster etch rates and improved uniformity; DI water rinse [94]
15	Aluminum (Al), deposited on GaN, GaAsP, GaP, NiCr, Si, others	40–200	No nitric	25–50°C; Transene Aluminum Etchant Type D; 40°C typical (125 Å/s); use with GaAs, GaP; mask with PR, Si_3N_4, SiO_2; Etches slightly Cr and Si_3N_4; Doesn't significantly etch Au, Cu, Ni, NiCr, Si, Ta, TaN, Ti, W; glass, Teflon or polypropylene tank; etch rate varies with Al composition; DI water rinse [94]
16	Aluminum (Al), deposited	160	Phosphoric, nitric, acetic	40°C; Cyantek AL-11; agitate often; quartz tank; DI water rinse [95]
17	Titanium (Ti), deposited		H_2O_2(30%) undiluted	50–60°C; DI water rinse [45, 96]
18	Titanium (Ti), deposited		H_2SO_4(96%) undiluted	80°C; DI water rinse [45, 76]
19	Titanium (Ti), deposited		H_2SO_4(96%): H_2O_2(30%) 2:1	70°C; doesn't significantly etch $TiSi_2$; DI water rinse [97]

Table 8.8 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
20	Titanium (Ti), deposited		H_2SO_4(96%): HF(49%):H_2O 30:1:69	70°C; DI water rinse [98]
21	Titanium (Ti)		H_3PO_4(85%) undiluted	Warm; DI water rinse [96, 99]
22	Titanium (Ti)		HCl(38%) undiluted	Room temperature; DI water rinse [96]
23	Titanium (Ti), deposited	2000	HF(49%):H_2O 1:9	32°C; DHF etchant (9:1); mask with PR; DI water rinse [16, 100]
24	Titanium (Ti), deposited	180	HF(49%): H_2O_2(30%):H_2O 1:1:20	20°C; mask with PR; etch rate increases with higher HF concentration; Etches Al (25 Å/s), AlSi (2%) (40 Å/s), SiO_2 (2 Å/s), SiO_2(PSG) (35 Å/s), W (2 Å/s); Etches slightly Si(poly) (0.5 Å/s), Si(poly, n-doped) (0.2 Å/s); Doesn't significantly etch Cr, sapphire, Si, Si_3N_4 (0.1 Å/s), Si_3N_4(low-stress) (<0.1 Å/s), TiW; DI water rinse [27, 28]
25	Titanium (Ti), deposited		HF(49%): HNO_3(70%) 1:200	Room temperature; DI water rinse [45]
26	Titanium (Ti), deposited		HF(49%): HNO_3(70%):H_2O 1:1:50	Room temperature; HNW etchant; DI water rinse [45, 76]
27	Titanium (Ti), deposited	3000	HF(49%): HNO_3(70%):H_2O 1:2:7	32°C; HNW etchant; mask with PR; DI water rinse [16, 100]
28	Titanium (Ti), deposited		NH_4OH(29%): H_2O_2(30%):H_2O 1:1:5	50°C; doesn't significantly etch $TiSi_2$; DI water rinse [97, 101]

Table 8.8 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
29	Titanium (Ti), deposited	50	Hydrochloric acid, no HF	85°C; etch rate 10 Å/s at 70°C; Transene titanium etchant TFTN; mask with PR; Etches Al, Cr, GaAs, Ti; Etches slightly Cu, Ni; Doesn't significantly etch Au, Si, Si_3N_4, SiO_2, Ta, TaN, W; polyethylene or polypropylene tank; DI water rinse [102]
30	Titanium–tungsten (TiW) (90/10), sputtered	1	H_2O_2(30%) undiluted	20°C; mask with PR; Etches W (3 Å/s); Doesn't significantly etch AlSi(2%) (0.3 Å/s), Si, Si(poly), Si_3N_4, SiO_2, Ti; DI water rinse [27]
31	Titanium–tungsten (TiW), deposited	10–15	Proprietary	25–40°C; Transene Ti-tungsten TiW-30; mask with PR; Etches Cu, GaAs; Etches slightly Ni, Ti, W; Doesn't significantly etch Al, Au, Cr, Si, Si_3N_4, SiO_2, Ta, TaN; store cold; DI water rinse [103]
32	Tungsten (W), deposited	3	H_2O_2(30%) undiluted	20°C; mask with PR; Etches TiW (90:10) (1 Å/s); Etches slightly AlSi (2%) (<0.3 Å/s); Doesn't significantly etch Al, Si(poly), Si_3N_4, SiO_2, Ti; endpoint difficult with Al mask; DI water rinse [27, 45]
33	Tungsten (W), deposited	25	H_2O_2(30%) undiluted	50°C; mask with PR; Etches Cr (18 Å/s), Ge(poly) (75 Å/s), TiW; Etches slightly AlSi (2%) (<0.1 Å/s), SiGe(poly) (<0.1 Å/s); Doesn't significantly etch Al, Parylene Type C, polyimide, Pyrex, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2; consider ultrasonic to remove bubbles; DI water rinse [28]
34	Tungsten (W)		HCl(38%): HNO_3(70%) 3:1	Hot; aqua regia; DI water rinse [104]

Table 8.8 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
35	Tungsten (W)		HF(49%): HNO_3(70%) 4:1	Hot; DI water rinse [104, 105]
36	Tungsten (W), deposited		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [45, 98]
37	Tungsten (W), deposited	80–250	Ferricyanide-based	20–60°C; etches 140 Å/s at 30°C; Transene Tungsten Etch TFW; mask with PR; Etches Al, Cr, GaAs; Etches slightly Si, SiO_2; Doesn't significantly etch Au, Cu, Ni, Si_3N_4, Ta, TaN, Ti; DI water rinse [106]

Table 8.9 Photoresist removal processes

	Material	Strip rate (Å/s)	Stripper	Remarks and references
1	Organic residues	N/A	O_2 plasma	Dry etch; 0.5–10 min; plasma; 300 mT, O_2, 100–300 W; surface oxide may form [108]
2	Organic residues	N/A	O_2 RIE	Dry etch; 1–5 min; 10–50 mT, O_2, 100–400 V bias; for most stubborn films [108]
3	Organic residues	N/A	UV-Ozone	1–30 min in UV-ozone [108]
4	Photoresist (PR), spun	>20,000 varies	Acetone	20°C; etches slightly Parylene Type C (0.1 Å/s); Doesn't significantly etch Ag, Al, Al_2O_3, Au, Cr, Cu, Mo, Nb, Ni, NiCr, Pd, polyimide, Pt, Pyrex, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta, Ti, TiN, TiW, Va, W; can be heated with loosely fit lid or used ultrasonically; dissolution rate slows significantly if wafers have seen high temperatures above 130°C from postbake cycles or dry etching; for hardened resist use piranha, O_2 plasma, or a commercial stripper; chemically inert to most inorganics [27, 28]
5	Photoresist (PR), spun	varies	H_2SO_4(96%): H_2O_2 (30%) 2:1 to 4:1	90–140°C; piranha; add peroxide to sulfuric acid when mixing; DI water rinse [109]
6	Photoresist (PR), spun	varies	H_2SO_4(96%): H_2O_2(30%) 56:1	120°C; high-sulfuric piranha; Etches Ag (100 Å/s), Al (850 Å/s), AlSi (2%) (30 Å/s), Al_2O_3 (3–15 Å/s), Cr (1–3 Å/s), Cu (15 Å/s), Mo (3 Å/s), Nb (1 Å/s), Ni (65 Å/s), NiCr (15 Å/s), polyimide (2800 Å/s), Ti (40 Å/s); Etches slightly Ge(poly) (softens), Parylene Type C (0.4 Å/s), Pd (0.5 Å/s), Pt (0.5 Å/s), TiW (0.1 Å/s); Doesn't significantly etch Au, Pyrex, quartz, sapphire, Si, Si(poly), SiGe(poly), Si_3N_4, SiO_2, Ta; Heat and agitate; 5–10 min; exothermic; add H_2O_2 immediately prior to use; hydrous silicon oxide is formed on Si substrates that can be removed with DHF etchant (10:1) for 10 s; DI water rinse [27, 28]
7	Photoresist (PR), spun	>80 varies	Isopropanol (isopropyl alcohol or IPA)	20°C; strips PR less quickly than acetone or methanol; Doesn't significantly etch Ag, Al, Al_2O_3, Au, Cr, Cu, Mo, Nb, Ni, NiCr, Parylene Type C, Pd, polyimide, Pt, Pyrex, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta, Ti, TiN, TiW, Va, W [28]

Table 8.9 (continued)

	Material	Strip rate (Å/s)	Stripper	Remarks and references
8	Photoresist (PR), spun	>2500 varies	Methanol (MeOH)	20°C; strips PR less quickly than acetone, can produce residues; Doesn't significantly etch Ag, Al, Al_2O_3, Au, Cr, Cu, Mo, Nb, Ni, NiCr, Parylene Type C, Pd, polyimide, Pt, Pyrex, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta, Ti, TiN, TiW, Va, W [28]
9	Photoresist (PR), spun	varies	NH_4OH(29%): H_2O_2(30%):H_2O 1:1:5	80°C; >5 min; DI water rinse [108]
10	Photoresist (PR), spun	5 varies	O_2 plasma	Dry ashing; 20°C; descum; 51 sccm O_2 in plasma with 50 W, 300 mTorr and gap of 2.6 cm; benign to inorganics [27]
11	Photoresist (PR), spun	50	O_2 plasma	Dry ashing or stripping; 20°C; 51 sccm O_2 in plasma with 400 W, 300 mTorr and gap of 2.6 cm; etches Parylene Type C (35 Å/s), polyimide (60 Å/s); benign to inorganics [27, 28]
12	Photoresist (PR), spun	varies	O_2 plasma	Dry ashing or stripping; plasma etcher, barrel etcher or asher [110]
13	Photoresist (PR), spun	varies	AZ300T (TMAH, NMP, others)	80°C; 5 min; solvent hood; final resist strip bath; DI water rinse [111]
14	Photoresist (PR), spun	varies	EKC 830 (aminoethoxy ethanol, n-methyl pyrrolidone)	80°C; 10 min at 80°C for ~1 μm of resist; 30 min for up to 10 μm of resist; agitate 5–10 s initially and every 5 min; follow with AZ300T for 5 min at 80°C; 3 quick-dump rinses; use with ultrasonic bath for liftoff processes [111]
15	Photoresist (PR), spun	>14,000 varies	Microstrip 2001	85°C; Fujifilm Microstrip 2001; Etches polyimide (85 Å/s); Doesn't significantly etch graphite, Pyrex, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2; use with Al, Ti, W; DI water rinse [28]
16	Photoresist (PR), spun	varies	Nanostrip (sulfuric acid, peroxymonosulfuric acid, hydrogen peroxide)	20°C or higher; Cyantek Corp.; Nanostrip; >5 min per bath; multiple baths [111]

Table 8.10 Prelithography cleaning process (pre-spin)

	Material	Strip rate (Å/s)	Stripper	Remarks and references
1a	Photoresist (PR)	N/A	AZ300T (NMP + TMAH) or PRX1165 (NMP)	80°C; 10 min; continue with next step [112]
1b		N/A	Isopropyl alcohol	Room temperature; continue with next step [112]
1c		N/A	DI water	Rinse; N_2 blow dry; dehydration bake >100°C for >2 min; cool substrates before spinning [112]

Table 8.11 Prelithography cleaning process (re-spin)

	Material	Strip rate (Å/s)	Stripper	Remarks and references
1	Photoresist (PR) on wafers, not post-baked	N/A	Acetone	Apply with spray bottle of acetone about 10 s until clear while spinning wafers on coater track; acetone clears and wafers dry while still spinning [113]

and dry photoresist removal processes. Removal rates are highly subject to the type and thickness of the resist, previous baking cycles, and extent of exposure to chemical etchants. Table 8.10 provides a prelithography cleaning process for removing resist using heated commercial strippers. Table 8.11 presents a method for removing photoresist from lithographically exposed wafers that have not been postbaked to allow resist reapplication following an inadvertent or incorrect exposure step. This technique may work with negative or positive photoresist. An alternative for positive resists is to blanket expose the resist layer and develop the exposed resist in a standard developer. Table 8.12 provides a sequence of solvent soaks to remove organics including spun photoresist on wafers and dried photoresist, which may also be suitable for holder, tweezer, cassette, and vacuum wand cleaning [107]. For unbaked and prebaked photoresist, the acetone and methyl alcohol soaking steps may be reduced to 2 min each in an optional ultrasonic bath, followed by a rinse with running DI water for 30 s and drying with nitrogen [108]. Table 8.13 presents an organic contaminant removal process using solvents and cleanroom swabs. Table 8.14 describes a particulate removal process for removal of scribing dust and debris that may occur on wafers or substrate samples. Most of the time processes for removing photoresist require at least 5 min in each solution, and for many, 10 min per bath is suggested.

Wafer-cleaning processes precede nearly every furnace or deposition sequence to ensure that contaminants and residues from wet-etch steps and other processes are adequately removed from the wafers. These sequences are predominantly if

Table 8.12 Photoresist and organic removal sequence with solvents

	Material	Strip rate (Å/s)	Stripper	Remarks and references
1a	Photoresist (PR) on wafers, partial substrates, holders and tweezers	varies	Acetone	Room temperature; 10 min; AMI strip sequence; solvent hood; place substrate or tweezers in beaker with acetone and lid and place in ultrasonic cleaner with water; continue with next step [114]
1b		N/A	Methanol	Room temperature; 5 min; solvent hood; continue with next step [114]
1c		N/A	Isopropyl alcohol	Room temperature; 5 min; solvent hood; continue with next step [114]
1d		N/A	DI water	DI water rinse; 5 quick-dump rinse and spin–rinse–dry or DI water spray and N_2 blow-dry [114]

Table 8.13 Organic contaminant removal process with swabs

	Material	Strip rate (Å/s)	Stripper	Remarks and references
1a	Photoresist (PR) residue and dried resist	N/A	Acetone	Room temperature; coat wafer surface with acetone; scrub with a cleanroom swab; continue with next step [115]
1b		N/A	Isopropyl alcohol	Spray wafer with IPA from a squeeze bottle to displace acetone; blow dry with N_2 [115]

Table 8.14 Particulate removal process with surfactants

	Material	Strip rate (Å/s)	Stripper	Remarks and references
1a	Particulates on substrates (e.g., scribe dust)	N/A	Surfactant in DI water	Tergitol, soap, or similar surfactant with optional ultrasonic agitation; continue with next step [116]
1b		N/A	DI water	Running DI water rinse; 0.5 min; N_2 blow-dry [116]

not completely wet, with chemical-etch steps followed by vigorous deionized water rinsing steps and a final spin–rinse–dry cycle with hot nitrogen. Table 8.15 presents a standard RCA clean cycle (initially developed at RCA Laboratories) for silicon substrates prior to contamination-sensitive furnace and deposition operations [117–121].

Although many variations of sequences, times, temperatures, and concentrations exist, the general cleaning approach begins with a mixture of sulfuric acid

Table 8.15 RCA clean cycle for silicon substrates

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1a	Silicon (Si) substrates		NH_4OH(29%): H_2O_2(30%):H_2O 1:1:5	75°C; organic clean (a.k.a. SC-1, standard-clean #1, or RCA-1); removes insoluble organic contaminants and some metals; PR previously stripped; DI water rinse [109]
1b			HCl(38%): H_2O_2(30%):H_2O 1:1:6	75°C; ionic clean (a.k.a. SC-2, standard-clean #2, or RCA-2); removal of any ionic, alkaline and heavy metal contaminants; DI water rinse; spin–rinse–dry [109]
1c			HF(49%):H_2O 1:10	Room temperature; DHF etchant (10:1); oxide strip; removal of thin silicon dioxide layer and any metallic contaminants from previous step; DI water rinse [109]

and hydrogen peroxide at 90–120°C to remove from the wafer surfaces some of the inorganics and organics such as photoresist residue and thinly deposited oily vapors from the air. Small particles of silica and silicon, additional organics, and metal surface contaminants are removed in a second step with ammonia hydroxide and hydrogen peroxide at about 70°C, which oxidizes the wafers slightly to lift and entrain contaminants on and near the wafer surface. A hydrofluoric-acid dip at room temperature for a short time strips the thin, chemically grown oxide and allows contaminants to be dissolved or floated away. Hydrochloric acid and hydrogen peroxide at about 70°C in a fourth step clean the surface of metals and ionic contaminants. The wafers are typically rinsed with DI water in a dump rinser for 5–6 cycles between each step. Ultrasonic agitation may be applied for the ammonium hydroxide and HCl steps if available. The three peroxide steps are preheated in controlled-temperature tanks, and the chemicals are generally mixed soon before use. Note that the peroxide steps are exothermic and will cause the bath temperature to rise when mixed or refreshed. The etchants with ammonium hydroxide and HCl should be replaced on a regular basis, although the composition may be refreshed with the addition of hydrogen peroxide. After the last dump rinse, the wafers are transported into a spin–rinse–dryer where the wafers are sprayed with DI water while spinning slowly, and then blown dry with heated nitrogen gas while spinning rapidly. The wafers are transferred promptly to the corresponding furnace or deposition system for further processing.

Table 8.16 presents an alternative process sequence for wafer cleaning cycles prior to oxidation or anneal furnace operations. For furnace operations such as LPCVD poly, nitride, epi deposition, or annealing that benefit from a substrate largely clear of native oxide, the order of the HF-dip is reversed as shown in Table 8.17.

Table 8.16 Alternative clean cycle for silicon substrates (preoxidation)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1a	Silicon (Si) substrates		H_2SO_4(96%): H_2O_2(30%) 4:1	90°C; 10 min; quartz hot pot; removes trace organics; 5 QDRs; continue with next step [122]
1b			HF(49%):H_2O 1:50	Room temperature; DHF etchant (50:1); 15–30 s Teflon tank; removes thin native oxide; 5 QDRs; continue with next step [122]
1c			HCl(38%): H_2O_2(30%):H_2O 1:1:5	70°C; 10 min; quartz hot pot; removes trace metal ions; 5 QDRs; spin–rinse–dry; proceed promptly to next operation [122]

Table 8.17 Clean cycle for silicon substrates (predeposition)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1a	Silicon (Si) substrates		H_2SO_4(96%): H_2O_2(30%) 4:1	90°C; 10 min; quartz hot pot; removes trace organics; 5 QDRs; continue with next step [122]
1b			HCl(38%): H_2O_2(30%):H_2O 1:1:5	70°C; 10 min; quartz hot pot; removes trace metal ions; 5 QDRs; continue with next step [122]
1c			HF(49%):H_2O 1:50	Room temperature; DHF etchant (50:1); 15–30 s Teflon tank; removes thin native oxide; 5 QDRs; spin–rinse–dry; proceed promptly to next operation [122]

8.4.5 Examples: Wet Chemical Etching of IC-Compatible Materials

For most IC and MEMS processes, a photoresist mask will suffice for patterning sequences involving standard materials such as oxide, nitride, silicon, polysilicon, and metal, as depicted in Fig. 8.10. For cases where the film is uncommonly thick, or when the photoresist is unable to hold up to the etchant for the required time, a hard mask may be needed. A group of examples for the wet etching of standard IC-compatible materials follows. These examples and others throughout this chapter are intended to be instructive. Their accuracy should not be relied on, and their utility should be verified by the user.

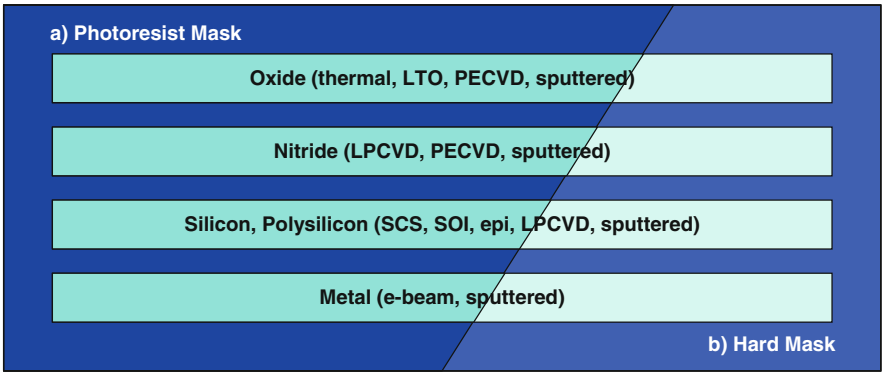

Fig. 8.10 Photoresist masks suffice for the majority of patterning and wet- or dry-etch steps for thin films of oxides, nitrides, silicon, polysilicon, and metals, although hard masks may be used in some cases. Photoresist masks are predominantly used for masking layers of modest thickness. For longer and deeper etches, a carefully selected hard mask may be preferred. Although PR masks and hard masks are options for the etching of most materials of interest, many other device and process considerations affect the selection of masks

8.4.5.1 Example 1: Wet Etch of Low-Temperature Oxide

A 6000 Å-thick unannealed, undoped oxide deposited on all exposed surfaces of a silicon wafer from the decomposition of silane and heterogeneous reaction with oxygen at about 400°C in an LPCVD system is coated with a patterned, 1.1 μm-thick photoresist mask on the topside of the wafer. BHF etchant (6:1) at room temperature etches 12 wafers in a dedicated Teflon tank and cassette at a rate of 50 Å/s. The wafers are agitated while in the etchant for the first 10 s. At 15-s intervals after 1½ min have passed, the wafers are pulled briefly out of the etchant to inspect the wafer backsides and to determine when the oxide is gone by observing whether the backsides pull hydrophobic whereby water does not wet the surface. The wafers are etched for 120 s to substantially clear the oxide and another 15 s to provide 10–15% overetch. The wafers are dump-rinsed for five cycles in DI water and then inserted into a spin–rinse dryer for a 3-min rinse with DI water at 600 RPM and a 4-min spin with heated nitrogen at 2000 RPM.

The wafers are removed from the dedicated cassette and placed into a run box. One of the wafers is inspected visually in a 10x microscope to ensure narrow features are not excessively undercut, and then measured with an optical film thickness measurement system (e.g., NanoSpec) to ensure 100% removal of the oxide by measuring the thickness of any oxide on the silicon substrate at five locations on the wafer, showing that less than 100 Å remain at all tested locations. The photoresist is stripped from the wafers in a dedicated cassette in a quartz tank for 20 min with hot piranha comprising nine parts concentrated sulfuric acid (96%) and one part hydrogen peroxide (30%) mixed 15 min earlier and heated to 120°C, with assistance from self-heating of the exothermic mixture. Goggles and a face shield, double gloves, cleanroom coat, chemical apron, head mask, and booties are worn in front

of a polypropylene chemical hood with functioning exhaust and a nearby eye wash, emergency shower, and PA system.

8.4.5.2 Example 2: Wet Etch of Silicon Nitride on Silicon

A 1200 Å-thick layer of stoichiometric LPCVD silicon nitride deposited on silicon wafers is masked with a 5000 Å-thick layer of annealed undoped LTO and placed in a Teflon cassette into hot phosphoric acid at a temperature of 160°C for 27 min (0.75 Å/s etch rate) in a quartz etch tank on a hot plate in a sink with a quartz reflux system to remove the exposed nitride features on the topside and all of the nitride on the backside of the wafers. The etch is preceded with a short dip in DHF etchant (50:1) to remove any oxide from the nitride surface for improved etch uniformity.

8.4.5.3 Example 3: Sacrificial Etch of Deposited Polysilicon Under a Structural Layer of Stress-Controlled Silicon Nitride

A 2 μm-thick layer of polysilicon is sacrificially removed from under a 10,000 Å-thick structural layer of stress-controlled silicon nitride with a 126:5:60 volumetric mixture of nitric acid (70% by weight), ammonium fluoride (40% by weight), and DI water at room temperature for 33 min to free 20 μm-wide silicon nitride features from two sides (10 μm per side at 50 Å/s etch rate), then quenched with slow and careful insertion into a DI water overflow rinse tank for 5 min followed by careful blow-drying with a nitrogen gun.

8.4.5.4 Example 4: Aluminum Etching over Patterned Nitride, Oxide, and Silicon

A wafer with a 0.5 μm-thick layer of sputter-deposited aluminum with 2% silicon over patterned layers of silicon nitride, silicon dioxide, and contact openings is etched with a photoresist mask and a commercial etchant at 40°C for 1 min (80 Å/s) with an additional 10-s overetch using plenty of agitation and temporary withdrawal of the wafer and Teflon cassette from the polypropylene etch tank several times in the first 30 s, followed by dump-rinsing and spin–rinse drying.

8.4.5.5 Example 5: Junction Depth Determination for an Integrated MEMS Device

An integrated silicon CMOS sensor die with a PECVD nitride layer over aluminum bond pads, an underlying polysilicon layer with a TiN barrier metal atop a thermal oxide layer, is placed in a Teflon die holder and initially cleaned with a surfactant (soap) in water using an ultrasonic bath for 10 min, then rinsed in running DI water directly under a tap for 0.5 min and dried with filtered nitrogen gas from a nitrogen

gun to remove loosely bound particulates. This is followed by a soak sequence of acetone, methanol, and isopropyl alcohol for 5 min each in a solvent bench and dried with filtered N_2 to remove any smudges and organic residue from die handling. The die is placed in a quartz beaker with a Teflon holder on a hot plate set in a built-in sink of a general-acid wet bench with hot phosphoric acid at 160°C for about 10 min to strip the 2000 Å-thick nitride (3.3 Å/s), followed by a 5-min DI water rinse. Any remaining aluminum pads and traces are stripped in a mixture of phosphoric acid, hydrogen peroxide, and water (8:1:1) at 35°C for about two min to clear the 1.2 μm-thick Al film (100 Å/s), and then rinsed in a beaker of DI water for 5 min. The 100 Å-thick TiN barrier metal is removed in BHF etchant (5:1) at room temperature for about 4 min (0.4 Å/s) followed by a DI water rinse in a beaker for 5 min. The 4500 Å-thick polysilicon layer is removed in about 1 min with a wet etch containing nitric acid, hydrofluoric acid, and water (50:1:20) at 25°C (90 Å/s). The oxide is stripped with BHF etchant (5:1) at room temperature for 15 min to clear the 15,000 Å-thick film (17 Å/s) using the Teflon die holder and rinsed in running DI water for 0.5 min. The junction depth is delineated with a junction-staining etch of HF(49%) and HNO_3(70%) at 200:1 for 1 min [8], followed by rinsing in running DI water for 0.5 min and blow drying with N_2 prior to microscope inspection.

8.5 Nonstandard Materials and Wet Etching

Nonstandard materials include substrates, thin films, etchants, processes, and equipment that are actually or perceptively incompatible with IC cofabrication. Cross-contamination is a major issue for any custom or semicustom MEMS process, and conflict resolution is often attained only by segregation of equipment, wafers, chemicals, and facilities. Many MEMS devices use IC processes or minor variants thereof, however, once a nonstandard sequence is reached in a standard wafer process flow, the wafers may be unable by policy to re-enter any portion of the standard flow. Of particular concern are contaminants such as sodium and lifetime killers such as gold that affect transistor performance and reliability. The seasoned MEMS device and process designer understands these limitations and generates workable solutions within facility, process, and design constraints. For example, a MEMS device may use a single nonstandard wet-etch step after the completion of a 20-mask CMOS process, and that step may be performed in a dedicated, isolated wet bench or at an outside facility to avoid conflicts with standard CMOS processing. Some MEMS process steps, such as an extended sacrificial etch step, may use the same chemicals and fume hoods as a qualified CMOS sequence, although set up in a separate etch tank in a dedicated portion of the hood. Often the MEMS steps are relegated as close to the end of a standard CMOS or bipolar process as possible, then finished in dedicated equipment.

The following sections present etch rates and processes for nonstandard materials categorized as dielectrics, conductive oxides and semiconductors, metals, silicides, plastics and polymers, and examples.

8.5.1 Nonstandard Dielectric, Semiconductor, and Metal Etching

The etch rates of nonstandard dielectrics and metals predominantly depend upon the film material, deposition technique, type and concentration of etchant, and etchant temperature. To a lesser extent, the etch rates depend upon stirring or agitation, the amount of material already etched by the etchant, and pretreatment of the patterned film such as annealing or native oxide layer removal immediately prior to etching. A variety of premixed commercial etchants and recipes for mixing an etchant from basic laboratory chemicals are available for nearly all dielectric and metal films. Etch beakers, etch tanks, and wafer holders are generally Teflon or polypropylene for room-temperature processes, with quartz or Pyrex suitable for some etchants. The etch tanks may be heated for temperature control of the etchant. Rinsing is generally accomplished with DI water in a dump-rinser followed by a cycle through a spin–rinse–dryer with hot N_2. Photoresist masks are generally the most attractive, although hard masks of a metal, oxide, or other dielectric may be desirable in some situations. Safety precautions apply to chemical handling, storage, and etching procedures alike.

Etch rates and etchants for many nonstandard dielectrics, conductive oxides, semimetals, semiconductors, and compound semiconductors are found in Table 8.18, and etch rates and etchants for nonstandard metal films are found in Table 8.19. Etch rates and etchants for standard and nonstandard metal silicides are found in Table 8.20. Silicides can be formed by depositing the base metal through a window in a masking oxide, then sintering and stripping the remaining metal with a suitable metal etchant. Silicides are resistant to most wet etchants, and dry (plasma), sputter or ion-beam etches may be used to etch them if needed. Silicides of different phases (e.g., V_3Si, V_5Si_3, and VSi_2) may have different etch rates in a given etchant, and some forms may prove insoluble whereas others etch readily. Many of the silicides can be oxidized with dry oxygen or steam at elevated temperatures and then the oxidized base metal etched accordingly [123, 124]. Reviews of silicides and silicide processing can be found in the literature [21, 97, 125–128].

8.5.2 Plastic and Polymer Etching

Wet etching of thin-film plastics and polymers is strongly dependent upon the type of polymer; the extent of cross-linking; the chain length; the solvent concentration in the polymer during etching; and the type, concentration, and temperature of the etchant. Wet etchants are generally solvent or acid-based. Solvent-based processes may use PFA, polypropylene, Pyrex, quartz, or stainless steel beakers, etch tanks, and holders with deliberation. Agitation including ultrasonic means can increase the etch or dissolution rate and uniformity. Safety measures and proper solvent disposal must be observed equally. Photoresist serves as a suitable etch mask for many polymeric layers, particularly if baked at an elevated temperature. Deposited oxide or metal may also serve as an etch mask, although the deposition processes for these

Table 8.18 Nonstandard dielectric, conductive oxide, semimetal, and semiconductor etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Aluminum antimonide (AlSb)		HCl(38%): HNO_3(70%) 1:1	25°C; DI water rinse [129]
2	Aluminum antimonide (AlSb), MBE	high	HF(49%):H_2O 1:20	Room temperature; DHF etchant (20:1); Etches GaSb; Doesn't significantly etch GaAs, InAs; DI water rinse [130]
3	Aluminum antimonide (AlSb)	5	HF(49%):H_2O: Ethanol 1:700:7000	Room temperature; etch rate decreases with distance from PMMA patterns; Doesn't significantly etch GaSb (<0.05 Å/s), InAs (<0.05 Å/s); DI water rinse [131]
4	Aluminum antimonide (AlSb)		HF(49%): H_2O_2(30%):H_2O 1:1:1	25°C; DI water rinse [129]
5	Aluminum antimonide (AlSb)		HF(49%): HNO_3(70%):Acetic 2:3:1	Room temperature; HNA etchant; faster etch rate with reduced acetic acid; DI water rinse [132]
6	Aluminum antimonide (AlSb), MBE	7	MF319 (TMAH-based developer) undiluted	Room temperature; agitate constantly; etch rate depends on thickness; Etches GaSb (3 Å/s), AlGaSb; Doesn't significantly etch InAs; DI water rinse [133]
7	Aluminum arsenide (AlAs), MBE and MOCVD	2500	HF(49%) undiluted	Room temperature; HF etchant (49 wt%); etch rate increases with increased HF concentration; 10% HF concentration recommended; Doesn't significantly etch $Al_xGa_{1-x}As$ ($x < 0.5$), GaAs; DI water rinse [134]
8	Aluminum arsenide (AlAs), MOCVD	180	HF(49%): NH_4F (40%):H_2O 1:7:200	22°C; etch rate for $Al_xGa_{1-x}As$ with $x = 1.0$ and 25:1 H_2O:BHF etchant (7:1); DI water rinse [135]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
9	Aluminum gallium arsenide (AlGaAs), MBE	22	H_2SO_4(96%): H_2O_2(30%):H_2O 1:1:50	25°C; DI water rinse [136]
10	Aluminum gallium arsenide (AlGaAs), MBE	45	H_2SO_4(96%): H_2O_2(30%):H_2O 1:4:60	Room temperature; DI water rinse [137]
11	Aluminum gallium arsenide (AlGaAs), MBE	26	H_3PO_4(85%): H_2O_2(30%):H_2O 1:1:50	25°C; DI water rinse [136]
12	Aluminum gallium arsenide (AlGaAs)	630	HF(49%):H_2O 1:6	Room temperature; DHF etchant (6:1); lateral undercut rate for $Al_{0.7}Ga_{0.3}As$; add H_2O_2 for less selectivity to GaAs; DI water rinse [138]
13	Aluminum gallium arsenide (AlGaAs), MOCVD	20	HF(49%): NH_4F (40%):H_2O 1:7:24	22°C; etch rate for $Al_xGa_{1-x}As$ with $x = 0.725$ and BHF etchant (7:1):H_2O 1:3; etch rate increases with increasing Al fraction; doesn't significantly etch $Al_xGa_{1-x}As$ with $x < 0.6$; use citric acid with H_2O_2 for Al fraction less than 0.5; DI water rinse [135]
14	Aluminum gallium arsenide (AlGaAs), MBE	40	NH_4OH(29%): H_2O_2(30%):H_2O 10:1:50	Room temperature; etch rate for $Al_{0.29}Ga_{0.71}As$; agitation with stirrer can increase etch rate $3x$; DI water rinse [137]
15	Aluminum gallium indium phosphide (AlGaInP), OMVPE	170	H_2SO_4(96%) undiluted	70°C; etch rate for $Al_{0.35}Ga_{0.15}In_{0.5}P$; slower for lower Al fractions; etchant is dopant sensitive at 60°C; DI water rinse [139]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
16	Aluminum gallium phosphide (AlGaP), MBE	1.3	H_3PO_4(85%) undiluted	Room temperature; etch rate for $Al_{0.5}Ga_{0.5}P$; DI water rinse [140]
17	Aluminum gallium phosphide (AlGaP), MBE	3	HCl(38%) undiluted	Room temperature; etch rate for $Al_{0.5}Ga_{0.5}P$; Etches InGaP (330 Å/s), AlInP (830 Å/s); DI water rinse [140]
18	Aluminum gallium phosphide (AlGaP), MBE	50	HF(49%) undiluted	25°C; HF etchant (49 wt%); etch rate for $Al_{0.5}Ga_{0.5}P$; Etches AlInP (15 Å/s); Doesn't significantly etch InGaP; DI water rinse [141]
19	Aluminum gallium indium phosphide (AlGaInP), OMVPE	380	HCl(38%):H_2O 1:1	25°C; etch rate for $Al_{0.35}Ga_{0.15}In_{0.5}P$; slower for lower Al fractions; dopant sensitive; DI water rinse [139]
20	Aluminum gallium phosphide (AlGaP), MBE	50	HCl(38%): HNO_3(70%):H_2O 1:1:1	25°C; etch rate for $Al_{0.5}Ga_{0.5}P$; mask with PR, black wax; Etches AlInP, GaAs, InGaP; decrease nitric component for higher selectivity to GaAs and lower AlGaP etch rate; decrease H_2O component for lower selectivity to GaAs and higher AlGaP etch rate; stabilize mixture 30 min before use; DI water rinse [140]
21	Aluminum gallium phosphide (AlGaP), MBE	50	HF(49%) undiluted	25°C; HF etchant (49 wt%); etch rate for $Al_{0.5}Ga_{0.5}P$; Etches AlInP (15 Å/s); Doesn't significantly etch GaAs, InGaP; DI water rinse [140]
22	Aluminum indium arsenide (AlInAs), MBE		HCl(38%):H_2O 3:1	Room temperature; DI water rinse; Doesn't significantly etch GaAsSb [142]
23	Aluminum indium nitride (AlInN), MBE	15–120	AZ400K (KOH-based PR developer) undiluted	20–80°C; etch rate for $Al_{0.81}In_{0.19}N$; DI water rinse [143]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
24	Aluminum indium phosphide (AlInP), MBE or MOCVD	35	H_2SO_4(96%) undiluted	25°C; etch rate for $Al_{0.5}In_{0.5}P$; Doesn't significantly etch InGaP, AlGaP; DI water rinse [141]
25	Aluminum indium phosphide (AlInP), OMVPE	370	H_2SO_4(96%) undiluted	70°C; etch rate for $Al_{0.5}In_{0.5}P$; DI water rinse [139]
26	Aluminum indium phosphide (AlInP), MBE or MOCVD	40	H_3PO_4(85%) undiluted	25°C; etch rate for $Al_{0.5}In_{0.5}P$; Etches slightly AlGaP (1.3 Å/s); Doesn't significantly etch InGaP, AlGaP; DI water rinse [141]
27	Aluminum indium phosphide (AlInP), MBE or MOCVD	800	HCl(38%) undiluted	25°C; etch rate for $Al_{0.5}In_{0.5}P$; Etches InGaP (330 Å/s), AlGaP (3 Å/s); DI water rinse [141]
28	Aluminum indium phosphide (AlInP), OMVPE	480	HCl(38%):H_2O 1:1	25°C; etch rate for $Al_{0.5}In_{0.5}P$; DI water rinse [139]
29	Aluminum indium phosphide (AlInP), MBE and MOCVD	100	HCl(38%):H_2O 1:5	25°C; etch rate for $Al_{0.5}In_{0.5}P$; etch rate decreases to 10 Å/s with HCl:H_2O of 1:30; Doesn't significantly etch GaAs (>600:1), InGaP (20:1); DI water rinse [144]
30	Aluminum indium phosphide (AlInP), MBE or MOCVD	600	HCl(38%): HNO_3(70%):H_2O 1:1:1	25°C; etch rate for $Al_{0.5}In_{0.5}P$; increasing HNO_3 or HCl concentration increases etch rate; decreasing HNO_3 concentration increases selectivity to GaAs; DI water rinse [141]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
31	Aluminum indium phosphide (AlInP), MBE or MOCVD	23	HNO_3(70%) undiluted	25°C; etch rate for $Al_{0.5}In_{0.5}P$; Etches InGaP (4 Å/s); Doesn't significantly etch AlGaP; DI water rinse [141]
32	Aluminum nitride (AlN), sputtered	90	AZ400K (KOH-based PR developer) undiluted	40°C; unannealed film; etch rate reduces with increased crystallinity (10*x* reduction for 1100°C anneal); resistant to most popular etchants except NaOH and KOH; DI water rinse [143, 145, 146]
33	Aluminum nitride (AlN)		H_2O undiluted	100°C; Di water rinse [21]
34	Aluminum nitride (AlN), sputtered	300–1000	H_3PO_4(85%) undiluted	80–100°C; orientation dependent; DI water rinse [147]
35	Aluminum nitride (AlN), hot pressed	1.7	HF(49%):H_2O 1:1	57°C; DHF etchant (1:1); DI water rinse [148]
36	Aluminum nitride (AlN), hot pressed	1.3	HF(49%): HNO_3(70%) 1:1	57°C; DI water rinse [148]
37	Aluminum nitride (AlN), CVD	120	HNO_3(70%) undiluted	100°C; deposition at 900°C; etch rate is 30 Å/s at 75°C and 1100 Å/s at 150°C; DI water rinse [149]
38	Aluminum oxide (Al_2O_3, alumina, sapphire)	25	H_2SO_4(96%): H_3PO_4(85%) 1:1	285°C; (0001) orientation; mask with sintered Cr–Pt–Cr; use platinum holder and flask; DI water rinse [150, 151]
39	Aluminum oxide (Al_2O_3), sputtered	3.8	H_3PO_4(85%) undiluted	50°C; as-deposited film; DI water rinse [152]
40	Aluminum oxide (Al_2O_3), CVD	4	H_3PO_4(85%) undiluted	185°C; partially crystalline film; etch rate increases with reduced crystallinity; DI water rinse [153]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
41	Aluminum oxide (Al_2O_3), CVD		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); amorphous form; also etches in BHF or hot phosphoric acid; doesn't significantly etch crystalline form; crystalline form may etch in hot phosphoric with sulfuric acid; DI water rinse [25]
42	Aluminum oxide (Al_2O_3), CVD	4	NH_4F (40%): HF(49%) 10:1	Room temperature; BHF etchant (10:1); amorphous film; etch rate reduces with crystallinity; crystalline films will not etch even in concentrated HF; DI water rinse [153]
43	Aluminum oxide (Al_2O_3, sapphire)		NH_4OH(29%): H_2O_2(30%):H_2O 1:1:3	80°C; substrate cleaning solution before metallization; follow with HCl:H_2O_2:H_2O 1:1:3 at 80°C, each for 15 min; DI water rinse [26]
44	Aluminum oxide (Al_2O_3, sapphire), deposited	2	Ortho-phosphoric acid	180°C; Transetch-N; SiO_2 mask (120:1); silicon selectivity (120:1); Pyrex or quartz tank; add water to replace evaporated water; DI water rinse [58]
45	Aluminum phosphide (AlP)		H_2O undiluted	Room temperature [154]
46	Antimony (Sb)		H_2SO_4(96%) undiluted	Hot; DI water rinse [25]
47	Antimony (Sb)		HCl(38%):H_2O 1:1	Room temperature; DI water rinse [155]
48	Antimony (Sb)		HCl(38%): H_2O_2(30%):H_2O 30:5:70	Room temperature; DI water rinse [155]
49	Antimony (Sb)		HCl(38%): HNO_3(70%) 3:1	Aqua regia; DI water rinse [25]
50	Antimony (Sb)		HCl(38%): HNO_3(70%):H_2O 1:1:1	Room temperature; DI water rinse [98]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
51	Antimony (Sb)		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [156]
52	Antimony (Sb)		HF(49%): HNO_3(70%):H_2O 2:3:5	Room temperature; HNW etchant; DI water rinse [157]
53	Antimony (Sb)	4200	HF(49%): HNO_3(70%):Acetic 1:3:12	Room temperature; HNA etchant; also Dash etchant; DI water rinse [158]
54	Arsenic (As)		HCl(38%): HF(49%):HNO_3(70%):Acetic 1:2:2:12	Room temperature; DI water rinse [159]
55	Arsenic (As)		HNO_3(70%) undiluted	DI water rinse [25]
56	Beryllium oxide (BeO, beryllia), single crystal	3	HCl(38%) undiluted	120°C; mildly anisotropic; stir or agitate; DI water rinse [160]
57	Beryllium oxide (BeO, beryllia), single crystal		H_3PO_4(85%) undiluted	175°C; also etches in HF vapor at 100°C; DI water rinse [161]
58	Boron (B)		H_2SO_4(96%): HCl(38%): HNO_3(70%):H_2O 2:5:10:50	Room temperature; DI water rinse [162]
59	Boron nitride (BN)		H_2SO_4(96%) undiluted	Boiling; DI water rinse [21]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
60	Boron nitride (BN), CVD	2.5	H_3PO_4(85%) undiluted	180°C; etches slightly in BHF (<0.2 Å/s), H_2O_2(3%) at 80°C (0.5 Å/s); DI water rinse [163]
61	Boron oxide (B_2O_3)		H_2O undiluted	Room temperature [164]
62	Cadmium oxide (CdO), thermally grown	1	HCl(38%):H_2O 1:10,000	Room temperature; 0.001 M HCl; also etches in dilute HF and H_2SO_4:H_2O_2:H_2O mixtures [165]; DI water rinse [166]
63	Cadmium tin oxide (CdO-SnO_2), (CTO), sputtered	>330	HCl(38%):H_2O 4:1	Room temperature; DI water rinse [167]
64	Cadmium selenide (CdSe), single crystal		HNO_3(70%): H_2SO_4 (18 N):Acetic: HCl(38%) 30:20:10:0.1	40°C; preferential etch; DI water rinse [168]
65	Cadmium sulphide (CdS), single crystal	350	HCl(38%):H_2O 1:2	Room temperature; etches cadmium-rich face 6x slower; DI water rinse [169]
66	Cadmium sulphide (CdS), single crystal		HNO_3(70%): Acetic:H_2O 1:6:1	25°C; DI water rinse [168]
67	Cadmium telluride (CdTe), ALE		H_3PO_4(85%): HNO_3(70%):H_2O 71:1:29	Room temperature; avoid further dilution with H_2O; can use H_2O_2 in place of HNO_3; can use acetic acid in lieu of H_3PO_4; DI water rinse [170]
68	Cadmium telluride (CdTe), single crystal	2000	HCl(38%): HNO_3(70%):H_2O 2:2:1	23°C; chemical polishing etchant; DI water rinse [171, 172]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
69	Cadmium telluride (CdTe), single crystal		HF(49%): HNO_3(70%) 1:1	25°C; also etches in concentrated hydrochloric acid; DI water rinse [168]
70	Cadmium telluride (CdTe), single crystal	560	HF(49%): H_2O_2(30%):H_2O 3:2:1	25°C; preferential etchant; DI water rinse [168, 172]
71	Cadmium telluride (CdTe), single crystal	10000	HF(49%): HNO_3(70%):Acetic 2:1:1	23°C; HNA etchant; can form pits; agitate; DI water rinse [172]
72	Cadmium telluride (CdTe), single crystal	1300	HNO_3(70%): H_2SO_4(96%): HCl(38%):Acetic 50:18:1:10	23°C; polishes; DI water rinse [172]
73	Cadmium telluride (CdTe), single crystal	580	HNO_3(70%) undiluted	23°C; can leave precipitate; DI water rinse [172]
74	Copper oxide (CuO)		HCl(38%):H_2O 1:2	Hot; little loss of Cu; DI water rinse [25]
75	Carbon (C), graphite		H_2SO_4(96%) undiluted	80°C; DI water rinse [173]
76	Carbon (C), graphite		HNO_3(70%) undiluted	Room temperature; DI water rinse [173]
77	Carbon (C), graphite		KOH(50%)	Hot; DI water rinse [173]
78	Diamond (C), SC CVD	35	O_2:Ar plasma 7 sccm:8 sccm	Dry etch; inductively coupled plasma (ICP); 2.5 mTorr; 600 W; −160 V bias [174]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
79	Fluorinated tin oxide (FTO)	40	Proprietary	40°C; Transene fluorinated tin oxide etchant FTO 100-FBA5; mask with PR; Etches Al, Cu, ITO, Ni, NiCr; strong agitation; DI water rinse [175]
80	Gallium (Ga)		HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [176]
81	Gallium (Ga)		HNO_3(70%) undiluted	Hot; DI water rinse [176]
82	Gallium antimonide (GaSb)		HCl(38%) undiluted	Hot; DI water rinse [177]
83	Gallium antimonide (GaSb)		HCl(38%): H_2O_2(30%):H_2O 1:1:2	Room temperature; DI water rinse [178]
84	Gallium antimonide (GaSb), MBE		HF(49%):H_2O 1:20	Room temperature; DHF etchant (20:1); Etches AlSb; Doesn't significantly etch GaAs, InAs; DI water rinse [130]
85	Gallium antimonide (GaSb)		HF(49%): HNO_3(70%):Acetic 1:2:1	25°C; HNA etchant; DI water rinse [129]
86	Gallium antimonide (GaSb)		HF(49%): HNO_3(70%):H_2O 1:1:1	Room temperature; HNW etchant; DI water rinse [179]
87	Gallium antimonide (GaSb)		HF(49%): HNO_3(70%):H_2O 3:7:10	Room temperature; HNW etchant; p–n junction etchant; DI water rinse [180]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
88	Gallium antimonide (GaSb), MBE	3	MF319 (TMAH-based developer) undiluted	Room temperature; also etches AlGaSb, AlSb (7 Å/s); doesn't significantly etch InAs; DI water rinse [133]
89	Gallium arsenide (GaAs)	70	H_2SO_4(96%):H_2O 5:1	Room temperature; consider citric acid and succinic acid etchants; DI water rinse [25]
90	Gallium arsenide (GaAs)	150	H_2SO_4(96%): H_2O_2(30%) 4:1	21°C; (001) surface; preferential etchant; rate increases with H_2O_2 concentration; DI water rinse [181]
91	Gallium arsenide (GaAs)	200	H_2SO_4(96%): H_2O_2(30%):H_2O 8:1:1	Room temperature; (100) face; etches (111) face more slowly; less anisotropy with higher H_2SO_4 concentrations; DI water rinse [8, 182–184]
92	Gallium arsenide (GaAs)	210	H_2SO_4(96%): H_2O_2(30%):H_2O 1:1:8	Room temperature; (100) face; DI water rinse [182]
93	Gallium arsenide (GaAs)	800	H_2SO_4(96%): H_2O_2(30%):H_2O 4:1:5	Room temperature; (100) face; preferential etchant; DI water rinse [182]
94	Gallium arsenide (GaAs)	2400	H_2SO_4(96%): H_2O_2(30%):H_2O 1:8:1	Room temperature; (100) face; etches (111) face more slowly; more anisotropy with lower H_2SO_4 concentrations; DI water rinse [182, 183]
95	Gallium arsenide (GaAs)	15	H_3PO_4(85%): H_2O_2(30%):H_2O 3:1:50	20°C; etch rate for (100) face; etch rate is less for (111) plane; higher phosphoric acid concentrations produce smoother etch; mask with PR, oxide, nitride; DI water rinse [8, 185]
96	Gallium arsenide (GaAs)	450	H_3PO_4(85%): H_2O_2(30%):H_2O 1:1:3	30°C; etch rate for (100) surface; mask with PR, oxide, nitride; DI water rinse [185]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
97	Gallium arsenide (GaAs)	300	H_3PO_4(85%): H_2O_2(30%):MeOH 1:1:3	Room temperature; direction dependent; DI water rinse [186]
98	Gallium arsenide (GaAs)	75	HCl(38%):Acetic: H_2O_2(30%) 1:2:1	20°C; etch rate decreases with acetic acid dilution; smooth surfaces; Etches $In_{0.48}Ga_{0.52}P$ (45 Å/s), InP (60 Å/s) etch rate for $In_{0.48}Ga_{0.52}P$; DI water rinse [187]
99	Gallium arsenide (GaAs)	35	HCl(38%): H_2O_2(30%):H_2O 1:4:40	Room temperature; (100) face; anisotropy increases with lower HCl concentration; DI water rinse [182]
100	Gallium arsenide (GaAs)	800	HCl(38%): H_2O_2(30%):H_2O 40:4:1	Room temperature; smooth surfaces on As and Ga faces; anisotropy decreases with higher HCl concentration; DI water rinse [182, 188]
101	Gallium arsenide (GaAs)	15–1500	HF(49%): H_2O_2(30%):H_2O varies	25°C; low H_2O_2:H_2O ratios are isotropic; high H_2O_2:H_2O ratios are preferential; DI water rinse [189]
102	Gallium arsenide (GaAs)	25	HF(49%): H_2O_2(30%):H_2O 1:16:450	25°C; DI water rinse [189]
103	Gallium arsenide (GaAs)	500	HF(49%): H_2O_2(30%):H_2O 1:2:25	Room temperature; rounds edges; DI water rinse [8, 190]
104	Gallium arsenide (GaAs)	1600	HF(49%): HNO_3(70%):H_2O 1:1:1	Room temperature; HNW etchant; (001) surface; DI water rinse [191]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
105	Gallium arsenide (GaAs)	3300	HF(49%): HNO_3(70%): Acetic:H_2O 1:3:5:5	24°C; etch rate increases to 4000 Å/s at 30°C; DI water rinse [192]
106	Gallium arsenide (GaAs)		HNO_3(70%):H_2O 1:9	Room temperature; p–n junction etchant; delineate p and n regions; DI water rinse [193]
107	Gallium arsenide (GaAs)	1200	HNO_3(70%): H_2O_2(30%) 1:1	Room temperature; (001) surface; DI water rinse [191]
108	Gallium arsenide (GaAs)	50	NH_4OH(29%): H_2O_2(30%) 1:700	Room temperature; etch rate for (111) Ga face; isotropic etchant; etch rate is similar for As(100) and As(111) faces; mask with oxide, nitride; doesn't significantly etch AlGaAs [194]; DI water rinse [8, 177, 195]
109	Gallium arsenide (GaAs)	650	NH_4OH(29%): H_2O_2(30%) 1:30	25°C; etches $Al_{0.3}Ga_{0.7}As$ (5 Å/s), $Al_{0.6}Ga_{0.4}As$ (1 Å/s); selectivity to AlGaAs increases with H_2O_2 concentrations above 20:1 and highest at 30:1; DI water rinse [196]
110	Gallium arsenide (GaAs)	20	NH_4OH(29%): H_2O_2(30%):H_2O 3:1:140	Room temperature; etch rate for n-type (100) Ga face; etch rate is 6 Å/s for Ga(111) and 33 Å/s for As(111) planes; etch rate is less for p-type; mask with oxide, nitride; DI water rinse [8, 197]
111	Gallium arsenide (GaAs)	250	NH_4OH(29%): H_2O_2(30%):H_2O 1:1:8	Room temperature; (100) surface; anisotropic; DI water rinse [198]
112	Gallium arsenide (GaAs), GaAIAs and AlGaAs	22	Citric acid, hydrogen peroxide	25°C; Transene GA Etch-300; mask with PR, SiO_2; Etches GaAlAs and AlGaAs; Pyrex, HDPE, Teflon or quartz tank; agitate for improved smoothness; store below 50°F; DI water rinse [199]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
113	Gallium arsenide antimony (GaAsSb), MBE		H_3PO_4(85%): H_2O_2(30%):H_2O 1:1:40	22°C; DI water rinse [142]
114	Gallium arsenide phosphide (GaAsP)	17	NH_4OH(29%): H_2O_2(30%):H_2O 20:7:1000	Room temperature; DI water rinse [200]
115	Gallium nitride (GaN), CVD	160	H_3PO_4(85%) undiluted	180°C; etches 30 Å/s at 50°C; DI water rinse [201]
116	Gallium nitride (GaN), deposited	1.3	Ortho-phosphoric acid	180°C; Transetch-N; SiO_2 mask (80:1); silicon selectivity (80:1); Pyrex or quartz tank; add water to replace evaporated water; DI water rinse [58]
117	Gallium phosphide (GaP)	70	H_2SO_4(96%): H_2O_2(30%):H_2O 3:1:1	60°C; etches p-type preferentially; DI water rinse [202]
118	Gallium phosphide (GaP)	2400	H_3PO_4(85%) undiluted	180°C; (111) surface; anisotropic; etches (100) face at ~120 Å/s; (111) etch rate is 800 Å/s at 150°C and 4000 Å/s at 200°C; mask with Au; DI water rinse [203]
119	Gallium phosphide (GaP)	330	HCl(38%): HNO_3(70%):H_2O 2:1:2	45°C; P(111) face; P(111) etch rate is 800 Å/s at 50°C; add HCL to water first, then HNO_3; DI water rinse [204]
120	Gallium phosphide (GaP)	80	HF(49%): H_2O_2(30%) 1:1	24°C; preferential etch rate to p-type GaP with illumination; DI water rinse [202]
121	Gallium phosphide (GaP)	580	Potassium hexacyanoferrate	80°C; Transene Gallium Phosphide Etchant; mask with Ti, SiO_2, Au or KMER; Etches SiC; Doesn't significantly etch Pd, Au or Pt; DI water rinse [205]
122	Germanium (Ge)			See Table 8.7

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
123	Germanium dioxide (GeO_2)		H_2O undiluted	Room temperature; Doesn't significantly etch GeO [206]
124	Germanium dioxide (GeO_2), CVD		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); hexagonal form; also etches in hydrochloric, phosphoric and sulfuric acids; tetragonal form is etch resistant; DI water rinse [25]
125	Germanium dioxide (GeO_2)		HF(49%):H_2O 1:4	Room temperature; DHF etchant (4:1); Etches GeO [206]
126	Germanium nitride (Ge_3N_4), CVD		HF(49%): NH_4F (40%) 1:5	Room temperature; BHF etchant (5:1); also etches in concentrated HF, nitric or hot phosphoric acids; etches slightly in sulfuric acid; DI water rinse [25]
127	Halfnium oxide (HfO_2), CVD	1	HF(49%):H_2O 1:3	25°C; DHF etchant (3:1); cracking may occur with higher HF concentration; etch rate decreases with annealing; consider CP-4A etch; DI water rinse [207]
128	Halfnium oxide (HfO_2), CVD		HF(49%): NH_4F (40%) 1:5	Room temperature; BHF etchant (5:1); also etches in concentrated HF and slightly in hot phosphoric acids; DI water rinse [25]
129	Indium aluminum arsenide (InAlAs), MBE	110	HCl(38%):H_2O 3:1	Room temperature; may have initial etch delay; lower HCl concentrations will not etch InAlAs or InGaAlAs; Etches AlGaAs, InGaAlAs (18 Å/s for AlAs mole fraction of 0.34), InP; Doesn't significantly etch GaAs, InGaAs (<0.1 Å/s), InGaAlAs (for AlAs mole fraction <0.2); DI water rinse [208]
130	Indium antiminide (InSb)		HF(49%): HNO_3(70%):H_2O 1:1:4	Room temperature; HNA etchant; DI water rinse [179]
131	Indium antiminide (InSb)	3200	HF(49%): H_2O_2(30%)H_2O 1:1:8	25°C; rate for In(111); preferential etchant; etches Sb(111) at 4800 Å/s; DI water rinse [209]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
132	Indium antiminide (InSb)	2800	HF(49%): HNO_3(70%):Acetic 1:2:1	25°C; HNA etchant; rate for In(111); similar rate for Sb(111) at this temperature only; DI water rinse [129, 210]
133	Indium antiminide (InSb)		HF(49%): HNO_3(70%):Acetic 3:5:3	Room temperature; HNA etchant; also CP-4A etchant; DI water rinse [211]
134	Indium arsenide (InAs)		HCl(38%) undiluted	Room temperature; DI water rinse [179]
135	Indium arsenide (InAs)	1400	HCl(38%) undiluted	75°C; DI water rinse [70]
136	Indium arsenide (InAs)		HF(49%): HNO_3(70%):H_2O 1:3:2	Room temperature; HNW etchant; p–n junction etchant; delineate p and n regions; DI water rinse [70]
137	Indium arsenide (InAs)		HNO_3(70%): H_2O_2(30%):H_2O 1:1:4	Room temperature; DI water rinse [179]
138	Indium arsenide phosphide (InAsP), VPE	200	H_3PO_4(85%): HCl(38%) 1:3	Room temperature; add 0–0.3 parts H_2O_2(30%) with increasing As concentration; DI water rinse [212]
139	Indium gallium antimonide (AlGaSb), sputtered		HCl(38%): H_2O_2(30%):H_2O 10:1:10	Room temperature; DI water rinse [213]
140	Indium gallium arsenide (InGaAs), MBE	22	H_2SO_4(96%): H_2O_2(30%):H_2O 1:1:50	25°C; use citric acid system for higher selectivity to AlGaAs; DI water rinse [136]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
141	Indium gallium arsenide (InGaAs), MBE	14	H_3PO_4(85%): H_2O_2(30%):H_2O 1:1:50	25°C; use citric acid system for higher selectivity to AlGaAs; DI water rinse [136]
142	Indium gallium arsenide phosphide (InGaAsP), LPE	115	H_2SO_4(96%): H_2O_2(30%):H_2O 3:1:1	20°C; etch rate is 265 Å/s at 30°C; etches InP (2 Å/s) at 20°C, (5 Å/s) at 30°C; DI water rinse [214, 215]
143	Indium gallium arsenide phosphide (InGaAsP), MOCVD	1.3	H_2SO_4(96%): HCl(38%): H_2O_2(30%):H_2O 1:1600:10:2000	23°C; similar etch rates for GaAs and InGaP; DI water rinse [216]
144	Indium gallium phosphide (InGaP), OMVPE	6	H_2SO_4(96%) undiluted	70°C; DI water rinse [139]
145	Indium gallium phosphide (InGaP), MBE	15	H_3PO_4(85%): HCl(38%):H_2O 1:1:1	25°C; etch rate increases with less water and less H_3PO_4; DI water rinse [217]
146	Indium gallium phosphide (InGaP), MOCVD	330	HCl(38%) undiluted	25°C; etch rate decreases rapidly with H_2O dilution; etch rate increases with HNO_3 addition; slow etch rate (4 Å/s) in concentrated HNO_3; selective to GaAs; DI water rinse [218]
147	Indium gallium phosphide (InGaP), MOCVD	200	HCl(38%): HNO_3(70%):H_2O 1:1:1	25°C; etch rate for $In_{0.5}Ga_{0.5}P$; increasing HNO_3 or HCl concentration increases etch rate; decreasing HNO_3 concentration increases selectivity to GaAs; DI water rinse [141]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
148	Indium gallium phosphide (InGaP), OMVPE	25	HCl(38%): H_2O_2(30%):Acetic 1:1:10	20°C; DI water rinse [187, 219]
149	Indium gallium phosphide (InGaP), OMVPE	12	HCl(38%):Acetic 1:20	20°C; etch rate for $In_{0.48}Ga_{0.52}P$; etched surface can be rough; add peroxide for smoother surfaces (although selectivity to GaAs decreases); Etches InP (65 Å/s); Doesn't significantly etch GaAs (<1 Å/s) [187]
150	Indium oxide (In_2O_3), sputtered	1.4	H_2SO_4(96%) undiluted	50°C; film doped with Sn; mask with Cr; DI water rinse [220]
151	Indium oxide (In_2O_3), CVD		HCl(38%) undiluted	Warm; Sn-doped film; DI water rinse [221]
152	Indium phosphide (InP)	3100	HCl(38%) undiluted	26°C; anisotropic; doesn't significantly etch InGaAsP; DI water rinse [215, 222, 223]
153	Indium phosphide (InP)		HCl(38%):H_2O 3:1	Room temperature; anisotropic etchant with highest etch rate in <100> directions; Etches $In_{0.52}Al_{0.48}As$ (115 Å/s); Doesn't significantly etch InGaAs; consider HCl:H_3PO_4 or HCl:H_3PO_4:Acetic etchants; does not etch in peroxide-based etchants; DI water rinse [224]
154	Indium phosphide (InP)	65	HCl(38%):Acetic 1:20	20°C; etched surface can be rough; add peroxide for smoother surfaces (though selectivity to GaAs decreases); Etches $In_{0.48}Ga_{0.52}P$ (12 Å/s); Doesn't significantly etch GaAs (<1 Å/s) [187]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
155	Indium phosphide (InP)	40	HCl(38%): H_2O_2(30%):Acetic 1:1:10	20°C; DI water rinse [187]
156	Indium phosphide (InP)	15	HCl(38%): H_2O_2(30%):H_2O 1:1:1	25°C; DI water rinse [223]
157	Indium phosphide (InP)	450	HCl(38%): H_3PO_4(85%) 1:1	35°C; (100) surface; preferential etchant; light sensitive; selective to InGaAsP; DI water rinse [225]
158	Indium phosphide (InP)	5600	HCl(38%): HNO_3(70%) 1:1	26°C; anisotropic; DI water rinse [222]
159	Indium phosphide oxide (InPO)		H_2SO_4(96%): H_2O_2(30%):H_2O 5:1:1	Cleaning cycle; DI water rinse [226]
160	Indium phosphide oxide (InPO)		HF(49%):H_2O 1:1	Room temperature; DHF etchant (1:1); also etches in HCl and H_2SO_4; DI water rinse [226, 227]
161	Indium tin oxide (ITO), sputtered	3	HCl(38%):H_2O 1:1	50°C; DI water rinse [228, 229]
162	Indium tin oxide (ITO), deposited	7	HCl(38%):H_2O 4:1	40°C; DI water rinse [167, 230]
163	Indium tin oxide (ITO), deposited	11	HCl(38%): HNO_3(70%) 3:1	40°C; aqua regia; DI water rinse [230]
164	Indium tin oxide (ITO), deposited	3.3	HCl(38%): HNO_3(70%):H_2O 50:1:25	Room temperature; DI water rinse [231]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
165	Indium tin oxide (ITO), sputtered		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); DI water rinse [232]
166	Indium tin oxide (ITO)	15–20	Proprietary	40–50°C; Transene indium tin oxide etchant TE-100; mask with PR; strong agitation; Etches Ni, Cu, NiCr and Al; DI water rinse [233]
167	Iron oxide (FeO), CVD		HCl(38%):H_2O 1:1	25–50°C; DI water rinse [234]
168	Iron oxide (FeO)		HF(49%):H_2O 1:10	Little or no loss of Fe; DHF etchant (10:1); DI water rinse [25]
169	Iron oxide (FeO)	50	Dilute acid	25°C; Transene iron oxide mask etchant, ME-10; mask with PR; etch rates dependent on thermal history of Fe_2O_3 and can become insoluble; glass or polypropylene tank; mild agitation; DI water rinse [235]
170	Lead oxide (Pb_2O_3)		HNO_3(70%) undiluted	DI water rinse [25]
171	Lead selenide (PbSe)	160–500	KOH:H_2O_2(30%): H_2O:ethylene glycol 150 g:1 mL: 180 mL:150 mL	35°C; nonstandard chemicals; etch rate increases with agitation; replenish with peroxide; DI water rinse [236]
172	Lead sulfide (PbS)		HCl(38%): HNO_3(70%):Acetic 30:10:1	50°C; rinse with 1:9 Acetic:H_2O then DI water [237]
173	Lead sulfide (PbS)		HNO_3(70%) undiluted	70°C; remove sulfur on surface with DI water rinse [237]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
174	Lead telluride (PbTe)		KOH:H_2O_2(30%): H_2O:ethylene glycol 300 g:1 mL: 330 mL:300 mL	35°C; nonstandard chemicals; DI water rinse [236]
175	Lead–zirconium–titanate (PZT), sputtered or sol-gel	500–1000	HCl(38%): HF(49%):H_2O 300:2:700	56°C; DI water rinse [238]
176	Lead–zirconium–titanate (PZT), sheet	500	HCl(38%) undiluted	60°C; etches 250 Å/s at 30°C; DI water rinse [239]
177	Lithium niobate ($LiNbO_3$)	1.3	HF(49%):H_2O 1:8	50°C; DHF etchant (8:1); rate can be increased with local ion damage; DI water rinse [240]
178	Lithium niobate ($LiNbO_3$)	20	HF(49%): HNO_3(70%) 1:2	Room temperature; proton-exchanged substrate; DI water rinse [241]
179	Lithium niobate ($LiNbO_3$)	1	HF(49%): HNO_3(70%) 1:2	Room temperature; proton-exchanged substrate; DI water rinse [241]
180	Lithium niobate ($LiNbO_3$)		HF(49%): HNO_3(70%) 1:2	110°C; DI water rinse [242]
181	Magnesium aluminum oxide ($MgAl_2O_4$, spinel)	85	H_2SO_4(96%): H_3PO_4(85%) 3:1	285°C; (110); doesn't etch significantly in HF, phosphoric or sulfuric acids; use platinum holder and flask; DI water rinse [151]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
182	Magnesium oxide (MgO), sputtered	23	Acetic:H_2O 1:100	Room temperature; etches MgO at 1 Å/s for acetic:H_2O 1:1000; PR mask; DI water rinse [243]
183	Magnesium oxide (MgO), crystalline	10	H_2SO_4(96%):H_2O 1:1	21C°; etches 420 Å/s at 77°C; DI water rinse [244]
184	Magnesium oxide (MgO), crystalline		H_2SO_4(96%): H_3PO_4(85%) 1:40	160°C; (111) surface; similar for (100) and (110) surfaces; DI water rinse [245]
185	Manganese dioxide (MnO_2)		HNO_3(70%): H_2O_2(30%):H_2O 1:1:18	Room temperature; DI water rinse [246]
186	Mercury selenide (HgSe)		HCl(38%): HNO_3(70%):H_2O 6:2:3	25°C; preferential etchant; DI water rinse [168]
187	Mercury selenide (HgSe)		HNO_3(70%): H_2SO_4(18 N): HCl(38%):Acetic 50:20:1:10	40°C; pitless polish etchant; DI water rinse [168]
188	Mercury telluride (HgTe)		HNO_3(70%): HCl(38%) 1:1	25°C; preferential etchant; DI water rinse [168]
189	Mercury telluride (HgTe)		HNO_3(70%): HCl(38%):H_2O 6:1:1	25°C; pitless polish etchant; DI water rinse [168]
190	Molybdenum trioxide (MoO_3)		NH_4OH(29%): H_2O_2(30%) 9:1	DI water rinse [25]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
191	Niobium oxide (Nb_2O_5), CVD		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); doesn't significantly etch in BHF; low etch rate in phosphoric and sulfuric acids; DI water rinse [25]
192	Pyrex (borosilicate glass, Corning 7740)	300	HF(49%):H_2O 1:1	25°C; DHF etchant (1:1); also etches in BHF; see Section 8.3.1; DI water rinse [25]
193	Quartz	50	HF(49%):H_2O 1:1	25°C; DHF etchant (1:1); also etches in BHF; see Section 8.3.1; DI water rinse [25]
194	Selenium (Se)		H_2SO_4(96%) undiluted	Hot; DI water rinse [247]
195	Silicon (Si)			See Tables 8.7 and 8.22
196	Silicon carbide (SiC), deposited		H_3PO_4(85%) undiluted	180°C; amorphous film only; use dry processes, hot gases, or molten salts with platinum containers [248, 249]
197	Silicon carbide (SiC), p^- cubic SiC deposited on Si		HCl(38%): HF(49%):H_2O 1:1:50	Electrochemical etch; room temperature; anodic etching; 2-terminal configuration; mask with PR; SS clip to sample; SS electrode in solution; current density of 96.4 mA/cm^2 [250]
198	Silicon carbide (SiC), single crystal	65	HF(49%):H_2O 1:20	Photoelectrochemical etch; DHF etchant (20:1); room temperature; n-SiC; faster anodization rate for p-SiC (360 Å/s); anodize in HF solution with light (n-type) or dark (p-type) to about 55% porosity, then oxidize in wet nitrogen at 1150°C and etch resulting oxide in HF; DI water rinse [251]
199	Silicon carbide (SiC)		HF(49%): HNO_3(70%) 6:1	60°C; slow etch rate; DI water rinse [21]
200	Silicon carbide (SiC), substrate	1.3	Potassium hexacyanoferrate	80°C; Transene gallium phosphide etchant; mask with negative PR, Ti, SiO_2, Au or KMER; Etches SiC; Doesn't significantly etch Pd, Au or Pt; DI water rinse [252]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
201	Silicon dioxide (SiO_2)			See Table 8.5
202	Silver oxide (Ag_2O)		NH_4OH(29%):H_2O 1:4	DI water rinse [25]
203	Tantalum carbide (TaC)		HF:HNO_3(70%): H_2O 1:1:1	Room temperature; HNA etchant; DI water rinse [253]
204	Tantalum nitride (TaN)		HF(49%): HNO_3(70%) 1:1	Warm; DI water rinse [21]
205	Tantalum nitride (TaN)		Hydrofluoric acid	25°C; Transene tantalum etch 111; mask with PR, Au, Si_3N_4, W; Etches Al, Cr, Cu, GaAs, Ni, Si, SiO_2, Ta_2O_5, Ti; DI water rinse [254]
206	Tantalum oxide (Ta_2O_5), CVD		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); amorphous form; medium etch rate in BHF; crystalline form doesn't significantly etch in HF, phosphoric or sulfuric acids; DI water rinse [25]
207	Tantalum oxide (Ta_2O_5)		Hydrofluoric acid	25°C; Transene tantalum etch 111; mask with Au, PR, Si_3N_4, W; Etches Al, Cr, Cu, GaAs, Ni, Si, SiO_2, TaN, Ti; DI water rinse [254]
208	Tellurium (Te)		H_2SO_4(96%) undiluted	Room temperature; DI water rinse [255]
209	Tellurium (Te)	1600	HCl(38%): HNO_3(70%):H_2O 3:1:1	Room temperature; dilute aqua regia; DI water rinse [256]
210	Tellurium (Te)		HNO_3(70%):H_2O 2:3	Room temperature; DI water rinse [25]
211	Tin oxide (SnO_2)	50	HCl(38%):H_2O 1:3 to 1:10	Electrochemical etch; room temperature; 40 mA/cm^2; mask with SiO_2; resistant to room-temperature nitric, sulfuric, hydrochloric and hydrofluoric acids; DI water rinse [257]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
212	Titanium dioxide (TiO_2), CVD		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); crystalline form; BHF okay for unannealed, amorphous films; also etches in phosphoric and sulfuric acids; DI water rinse [25]
213	Titanium nitride (TiN), reactive sputtered	10	HCl(38%): HF(49%): HNO_3(70%) 15:1:5	Room temperature; DI water rinse [258]
214	Titanium nitride (TiN), reactive sputtered	9	HF(49%): HNO_3(70%):Acetic 1:20:20	30°C; HNA etchant; DI water rinse [258]
215	Titanium nitride (TiN), sputtered		NH_4OH(29%): H_2O_2(30%):H_2O 3:1:2	Room temperature; DI water rinse [259]
216	Titanium nitride (TiN), ALD, CVD, PVD	0.1–0.3	NH_4OH(29%): H_2O_2(30%):H_2O 1:1:10	Room temperature; DI water rinse [260]
217	Titanium nitride (TiN), sputtered	4.5	NH_4OH(29%): H_2O_2(30%):H_2O 1:1:5	75°C; etches slightly CoSi (<0.1 Å/s); DI water rinse [261]
218	Vanadium oxide (V_2O_5), CVD		HF(49%):H_2O 1:9	Room temperature; DHF etchant (9:1); not all forms of VO are etched; DI water rinse [262, 263]
219	Zinc oxide (ZnO), sputtered	130	H_3PO_4(85%): Acetic:H_2O 1:100:100	20°C; etches rapidly in concentrated HCl and HNO_3; DI water rinse [264]
220	Zinc oxide (ZnO), sputtered	250	H_3PO_4(85%): Acetic:H_2O 1:1:10	20°C; DI water rinse [264]

Table 8.18 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
221	Zinc oxide (ZnO), sputtered	500	H_3PO_4(85%): Acetic:H_2O 1:1:50	Room temperature; higher lateral etch rate; DI water rinse [265]
222	Zinc oxide (ZnO), sputtered	170–230	HCl(38%):H_2O 1:40	25°C; rate sensitive to deposition conditions; DI water rinse [266]
223	Zinc oxide (ZnO), Al-doped (AZO), sputtered	100	HCl(38%): HNO_3(70%):H_2O 4:1:200	22°C; etch rate higher for unannealed films (350 Å/s); DI water rinse [267]
224	Zinc oxide (ZnO), sputtered	16–50	NH_4F (40%): HF(49%) 7:1	20°C; BHF etchant (7:1); DI water rinse [264]
225	Zinc oxide (ZnO), Al-doped (AZO), sputtered	3.6	TMAH:H_2O 2.38% TMAH	45°C; TMAH-based developer; Al<1%; DI water rinse [268]
226	Zinc selenide (ZnSe)		HCl(38%) undiluted	Hot; consider methanol-bromine etchant; DI water rinse [269]
227	Zinc sulfide (ZnS), deposited		HCl(38%):H_2O 1:4	Room temperature; doesn't significantly etch Si_3N_4; DI water rinse [270]
228	Zinc sulfide (ZnS)		HCl(38%): HNO_3(70%) 1:1	25°C; preferential etchant; DI water rinse [168]
229	Zinc telluride (ZnTe)		HCl(38%): HNO_3(70%) 1:1	25°C; preferential etchant; DI water rinse [168]
230	Zinc telluride (ZnTe)		HF(49%): HNO_3(70%)4:3	25°C; also etches in concentrated HCl; DI water rinse [70, 168]
231	Zirconium oxide (ZrO_2), CVD		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); also etches in hot phosphoric acid; DI water rinse [25]

Table 8.19 Nonstandard metal etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Aluminum (Al)			See Table 8.8
2	Beryllium (Be)		H_2SO_4(96%) undiluted	Room temperature; DI water rinse [271]
3	Beryllium (Be)		HCl(38%) undiluted	Room temperature; DI water rinse [272]
4	Beryllium (Be)		HF(49%):H_2O 1:7	Room temperature; DHF etchant (7:1); DI water rinse [273]
5	Bismuth (Bi)		H_2SO_4(96%) undiluted	Hot; DI water rinse [25]
6	Bismuth (Bi)		HCl(38%):H_2O 1:10	Room temperature; DI water rinse [98]
7	Bismuth (Bi), MBE		HCl(38%): HNO_3(70%):H_2O 1:1:1	Room temperature; DI water rinse [274]
8	Bismuth (Bi)	4200	HNO_3(70%):Acetic: H_2O 6:6:1	Room temperature; DI water rinse [275]
9	Brass (CuZn)		H_3PO_4(85%): HNO_3(70%):Acetic 1:1:4	50°C; PAN etchant; DI water rinse; see also copper [53]
10	Cadmium (Cd)		HNO_3(70%):H_2O 3:1	DI water rinse [25]
11	Cadmium (Cd)		HNO_3(70%):Acetic: H_2O_2(30%) 1:2:2	DI water rinse [26]
12	Chromium (Cr)	25	HCl(38%) undiluted	Room temperature; DI water rinse [276, 277]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
13	Chromium (Cr)		$HCl(38\%):H_2O$ 1:1 to 1:20	Room temperature; DI water rinse [26]
14	Chromium (Cr)		$HCl(38\%): H_2O_2(30\%)$ 3:1	Room temperature; DI water rinse [26, 45]
15	Chromium (Cr)		$HNO_3(70\%):H_2O$ 3:1	80°C; DI water rinse [92]
16	Chromium (Cr), deposited	25	Ceric ammonium nitrate, perchloric acid	20°C; Cyantek CR-7; mask with PR, oxide, Au, polyimide; Etches Ag (75 Å/s), Al (0.6 Å/s), Cu (45 Å/s), Ge(poly) (45 Å/s), Ti(0.3 Å/s), Va (10 Å/s); Etches slightly graphite (0.1 Å/s), Mo (0.5 Å/s), Ni (0.3 Å/s), NiCr (2 Å/s), Pyrex (roughens), quartz (<0.1 Å/s), SiGe(poly) (<0.1 Å/s), SiO_2(thermal) (<0.01 Å/s), Ta (0.1 Å/s), TiW (0.1 Å/s), W (0.5 Å/s); Doesn't significantly etch Au, Nb (roughens), nitride, oxide, Pd, poly-Si, Pt, sapphire (roughens), Si; DI water rinse [28]
17	Chromium (Cr), deposited	40	Ceric ammonium nitrate, nitric acid	40°C; Transene chromium etchant 1020; mask with PR, Au, Si_3N_4, SiO_2, Ti, W; etches Al, Cu, GaAs, Ni; glass tank; DI water rinse [278]
18	Cobalt (Co)		$H_2SO_4(96\%)$: $H_2O_2(30\%):H_2O$ 1:14:15	Room temperature; DI water rinse [279, 280]
19	Cobalt (Co), sputtered	40	$H_2SO_4(96\%)$: $H_3PO_4(85\%)$: $HNO_3(70\%)$:Acetic 1:1:3:5	40°C; doesn't significantly etch $CoSi_2$; DI water rinse [281]
20	Cobalt (Co), deposited	1.5	$HCl(38\%):H_2O$ 1:3	35°C; slows with etch time; doesn't significantly etch TiN; DI water rinse [282]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
21	Cobalt (Co), sputtered		HCl(38%): H_2O_2(30%) 3:1	Room temperature; doesn't significantly etch $CoSi_2$; DI water rinse [97, 101]
22	Cobalt (Co), deposited	13	HCl(38%): H_2O_2(30%):H_2O 1:1:100	30°C; doesn't significantly etch TiN (<0.02 Å/s); DI water rinse [282]
23	Cobalt (Co), deposited		HCl(38%): H_2O_2(30%):H_2O 3:1:3	80°C; etches cobalt oxide; doesn't significantly etch $CoSi_2$; DI water rinse [283, 284]
24	Cobalt (Co)		HNO_3(70%):Acetic 1:1	Room temperature; DI water rinse [53]
25	Cobalt (Co), evaporated		HNO_3(70%): H_2O 1:1	Room temperature; doesn't significantly etch $CoSi_2$; DI water rinse [285]
26	Cobalt (Co), MBE		HNO_3(70%): H_2O_2(30%) 1:3	Room temperature; doesn't significantly etch $CoSi_2$; DI water rinse [286]
27	Copper (Cu)	110	H_2SO_4(96%): H_2O_2(30%):H_2O 1:5:19	Also etches with H_3PO_4, HCl or HNO_3; DI water rinse [287]
28	Copper (Cu)		H_2SO_4(96%): HNO_3(70%):Acetic 2:3:3	Room temperature; etches Ni and Ni alloys at similar rate; dilute with H_2O for reduced rate; DI water rinse [288]
29	Copper (Cu), Brass (CuZn)		H_3PO_4(85%): HNO_3(70%):Acetic 55:20:25	55–80°C; PAN etchant; DI water rinse [53]
30	Copper (Cu), Cu–Al–Si Alloy (CuAlSi)		H_3PO_4(85%): HNO_3(70%):Acetic 1:1:1	60–70°C; PAN etchant; DI water rinse [53]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
31	Copper (Cu)		HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [289]
32	Copper (Cu), deposited	100	HCl(38%): HNO_3(70%):H_2O 3:1:2	30°C; dilute aqua regia; mask with PR; Etches Ag, Al (100 Å/s), AlSi(2%), Au (115 Å/s), Mo (110 Å/s), Ni (17 Å/s), Pd (65 Å/s), Pt (0.6 Å/s), W (1 Å/s); Etches slightly Al_2O_3 (0.2 Å/s), SiO_2(PECVD) (0.1 Å/s), Ta (0.3 Å/s), Ti (0.1 Å/s), TiW (0.6 Å/s); Doesn't significantly etch Cr, Nb, polyimide, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta; water added to reduce PR attack; self-heating; DI water rinse [28]
33	Copper (Cu)		HF(49%): HNO_3(70%) 1:1	Room temperature; rapid dissolution; DI water rinse [289]
34	Copper (Cu)		HNO_3(70%):H_2O 5:1	Room temperature; dilute with H_2O for slower etch; DI water rinse [98, 289]
35	Copper (Cu)		NH_4OH(29%):H_2O 1:1	Room temperature; rapid dissolution; can substitute H_2O_2 for H_2O; DI water rinse [289]
36	Copper (Cu)		NH_4OH(29%): H_2O_2(30%):H_2O 1:1:1	Room temperature; DI water rinse [290]
37	Copper (Cu)	80	Ammonium persulfate	40°C; Transene Copper Etchant APS-100; mask with PR; Etches Ni; Etches slightly W; Doesn't significantly etch Al, Au, Cr, Si, Si_3N_4, SiO_2, Ta, TaN, Ti; PVC, glass or epoxy-coated tank; continuous agitation; DI water rinse [291]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
38	Copper (Cu), deposited	480	H_3PO_4(85%): HNO_3(70%):Acetic: H_2O 16:1:1:2	50°C; Transene aluminum etchant type A; mask with PR, Si_3N_4 (>1000:1), Si_3N_4(low-stress) (>1000:1), SiO_2(LTO) (>1000:1), Ti (>1000:1); Etches Al (90 Å/s), AlSi(2%) (110 Å/s), Ge(poly) (2 Å/s), Ni (5 Å/s); Etches slightly Al_2O_3 (1–10 Å/s), sapphire (0.3 Å/s), Si(poly) (0.2 Å/s); Doesn't significantly etch Cr, quartz, Si, SiGe(poly), SiO_2; heated bath; DI water rinse [28]
39	Copper (Cu), deposited	45	Ceric ammonium nitrate, nitric acid	20°C; Cyantek CR-7; mask with Au, polyimide, PR, SiO_2; Etches Ag (75 Å/s), Al (0.6 Å/s), Cr (25 Å/s), Ge(poly) (45 Å/s), Ti(0.3 Å/s), Va (10 Å/s); Etches slightly graphite (0.1 Å/s), Mo (0.5 Å/s), Ni (0.3 Å/s), NiCr (2 Å/s), Pyrex (roughens), quartz (<0.1 Å/s), SiGe(poly) (<0.1 Å/s), SiO_2 (<0.01 Å/s), Ta (0.1 Å/s), TiW (0.1 Å/s), W (0.5 Å/s); Doesn't significantly etch Au, Nb (roughens), Pd, Si, Si(poly), Si_3N_4, SiO_2, sapphire (roughens), Pt; DI water rinse [28]
40	Dysprosium (Dy)		HNO_3(70%): Acetic 2:3	Room temperature; DI water rinse [292]
41	Erbium (Er)		H_2SO_4(96%): H_2O_2(30%) 1:1	DI water rinse [293]
42	Gold (Au), deposited	1600–2500	HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [26, 294]
43	Gold (Au), deposited	4000–8000	HCl(38%): HNO_3(70%) 3:1	32–38°C; aqua regia; DI water rinse [92]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
44	Gold (Au), deposited	115	HCl(38%): HNO_3(70%):H_2O 3:1:2	30°C; dilute aqua regia; mask with PR; Etches Ag, Al (100 Å/s), AlSi (2%), Cu (100 Å/s), Mo (110 Å/s), Ni (17 Å/s), Pd (65 Å/s), Pt (0.6 Å/s), W (1 Å/s); Etches slightly Al_2O_3 (0.2 Å/s), SiO_2(PECVD) (0.1 Å/s), Ta (0.3 Å/s), Ti (0.1 Å/s), TiW (0.6 Å/s); Doesn't significantly etch Cr, Nb, polyimide, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta; water added to reduce PR attack; self-heating; DI water rinse [28]
45	Gold (Au), deposited	165	KI:I_2:H_2O 4 g:1 g:40 mL	Room temperature; doesn't significantly etch Al; DI water rinse [22, 45]
46	Gold (Au), deposited	1270	KI:I_2:H_2O 1 g:4 g:4 mL	55°C; DI water rinse [26]
47	Gold (Au), deposited	28–150	KI, I_2	25–60°C; Transene gold etchant TFA; mask with PR; Etches Al, Cu (corrodes), GaAs; Etches Ni slightly; Doesn't significantly etch Cr, Si, Si_3N_4, SiO_2, Ta, TaN, Ti, W; glass tank; DI water rinse [295]
48	Hafnium (Hf)	1.5	H_2SO_4(96%): HNO_3(70%) 1:1	35°C; DI water rinse [296, 297]
49	Hafnium (Hf)	1	HCl(38%): HNO_3(70%) 1:1	35°C; DI water rinse [296]
50	Hafnium (Hf)		HF(49%):H_2O 1:50	Room temperature; DHF etchant (50:1); DI water rinse [16]
51	Hafnium (Hf)		HF(49%): H_2O_2(30%):H_2O 1:1:20	Room temperature; DI water rinse [98]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
52	Hafnium (Hf)		HF(49%): HNO_3(70%): H_2O_2(30%) 10:45:45	Room temperature; DI water rinse [298]
53	Indium (In)		HCl(38%) undiluted	Room temperature; heat for faster etch rate; DI water rinse [299, 300, 301]
54	Indium (In)		HCl(38%): HNO_3(70%) 3:1	40°C; aqua regia; DI water rinse [98, 300]
55	Indium (In)		HNO_3(70%):H_2O 1:1	Room temperature; DI water rinse [302]
56	Indium (In)		IPA, EtOH, then MeOH	Room temperature; DI water rinse [26]
57	Invar (FeNi)		HCl(38%): HNO_3(70%):Acetic: H_2O 2:2:5:1	Room temperature; DI water rinse [25]
58	Iridium (Ir)		HCl(38%): HNO_3(70%) 3:1	40°C; aqua regia; DI water rinse [26, 98]
59	Iron (Fe)		HCl(38%):H_2O 1:1	Room temperature; DI water rinse [98]
60	Iron (Fe)		HCl(38%): HNO_3(70%):H_2O 7:3:30	60–70°C; Di water rinse [25]
61	Iron (Fe), Steel (low-carbon)		HF(49%): H_2O_2(30%) 3:97	Room temperature; DI water rinse [53]
62	Iron (Fe), Iron–silicon alloy (FeSi)		HF(49%): H_2O_2(30%) 6:94	Room temperature; DI water rinse [53]
63	Iron (Fe), Steel (low-carbon)		HF(49%): HNO_3(70%):H_2O 7:3:30	60°C; HNW etchant; DI water rinse [53]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
64	Iron (Fe)		HNO_3(70%) undiluted	Hot; can be diluted or used at room temperature; DI water rinse [303]
65	Kovar (FeNiCo)		HCl(38%):H_2O 1:1	70°C; DI water rinse [26]
66	Kovar (FeNiCo)		HCl(38%): HNO_3(70%):Acetic 15:1:3	Room temperature; DI water rinse [26]
67	Lead (Pb)		Acetic:H_2O_2(30%) 1:4	Room temperature; DI water rinse [25]
68	Lead (Pb)		Acetic:H_2O_2(30%) 3:1	Room temperature; DI water rinse [53]
69	Lead (Pb)		Acetic:H_2O_2(30%): MeOH 2:3:5	Room temperature; DI water rinse [53]
70	Lead (Pb)		Acetic:H_2O_2(30%): H_2O 2:2:5	Room temperature; DI water rinse [98]
71	Lead (Pb)		HNO_3(70%):H_2O 3:17	Room temperature; DI water rinse [25]
72	Lithium (Li)		HNO_3(70%) undiluted	Room temperature; DI water rinse [26]
73	Lithium (Li)		MeOH undiluted	Room temperature; DI water rinse [304]
74	Magnesium (Mg)		H_2SO_4(96%): H_2O_2(30%):H_2O 15:90:10	25°C; DI water rinse [53]
75	Magnesium (Mg)		HNO_3(70%):H_2O 1:19 to 3:17	Room temperature; DI water rinse [25]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
76	Magnesium (Mg)		HNO_3(70%):MeOH 1:9	20°C; DI water rinse [53]
77	Manganese (Mn)		HCl(38%):H_2O 1:1	Room temperature; DI water rinse [25, 305]
78	Molybdenum (Mo), deposited		H_2SO_4(96%): HNO_3(70%) 1:4	Room temperature; DI water rinse [98]
79	Molybdenum (Mo), deposited	4000	H_2SO_4(96%): HNO_3(70%):H_2O 1:1:3	55°C; DI water rinse [10]
80	Molybdenum (Mo), sputtered		H_3PO_4(85%): HNO_3(70%):H_2O 5:3:2	25°C; DI water rinse [91]
81	Molybdenum (Mo), deposited	80	H_3PO_4(85%): HNO_3(70%):Acetic: H_2O 5:2:4:150	Room temperature; PAN etchant; mask with PR; DI water rinse [8, 22]
82	Molybdenum (Mo), deposited	115	H_3PO_4(85%): HNO_3(70%): Acetic:H_2O 180:11:11:150	20°C; PAN etchant; mask with PR (3:1); etches Al (3 Å/s); Doesn't significantly etch Cr, TiW; Di water rinse [28]
83	Molybdenum (Mo), deposited		HCl(38%): H_2O_2(30%) 1:1	Room temperature; DI water rinse [76]
84	Molybdenum (Mo), deposited	110	HCl(38%): HNO_3(70%):H_2O 3:1:2	30°C; dilute aqua regia; mask with PR; Etches Ag, Al (100 Å/s), AlSi(2%), Au (115 Å/s), Cu (100 Å/s), Ni (17 Å/s), Pd (65 Å/s), Pt (0.6 Å/s), W (1 Å/s);

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
				Etches slightly Al_2O_3 (0.2 Å/s), SiO_2(PECVD) (0.1 Å/s), Ta (0.3 Å/s), Ti (0.1 Å/s), TiW (0.6 Å/s); Doesn't significantly etch Cr, Nb, polyimide, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta; water added to reduce PR attack; self-heating; DI water rinse [28, 306]
85	Molybdenum (Mo)		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [307]
86	Molybdenum (Mo), deposited	55–85	Ferricyanide	30–60°C; Transene moly etch TFM; mask with negative PR, KMER, KTFR, or KPR; DI water rinse [308]
87	Molybdenum carbide (Mo_2C)		HNO_3(70%) undiluted	Room temperature; DI water rinse [26]
88	Monel (NiCuFe)		HNO_3(70%): H_2SO_4(96%):Acetic 5:2:5	Room temperature; DI water rinse [288]
89	Nichrome (NiCr), deposited		H_2SO_4(96%) undiluted	100°C; DI water rinse [76]
90	Nichrome (NiCr)		HCl(38%):H_2O 4:1	Room temperature; DI water rinse [25]
91	Nichrome (NiCr), sputtered		HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [309]
92	Nichrome (NiCr)		HCl(38%): HNO_3(70%):H_2O 1:1:3	Room temperature; DI water rinse [16]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
93	Nichrome (NiCr), sputtered (80:20)	14	Ceric ammonium nitrate	20°C; Transene nichrome etchant TFN; mask with Pr; Etches Al (8 Å/s), Cr (28 Å/s), Cu (115 Å/s), Mo (115 Å/s), Ni (2 Å/s); Doesn't significantly etch polyimide, quartz, Si, Si(poly), Si_3N_4, SiO_2; DI water rinse [28]
94	Nichrome (NiCr), evaporated	50	Ceric ammonium nitrate	40°C; Transene nichrome etchant TFN; mask with PR; Etches Al, Cr, Cu, GaAs, Ni; Doesn't significantly etch Au, Si_3N_4, SiO_2, Ti, W; DI water rinse [310]
95	Nickel (Ni), deposited	65	H_2SO_4(96%): H_2O_2(30%) 56:1	120°C; high-sulfuric piranha; Etches Ag (100 Å/s), Al(850 Å/s), AlSi(2%) (30 Å/s), Al_2O_3 (3–15 Å/s), Cr (1–3 Å/s), Cu (15 Å/s), Mo (3 Å/s), Nb (1 Å/s), NiCr (15 Å/s), polyimide (2800 Å/s), Ti (40 Å/s); Etches slightly Parylene type C (0.4 Å/s), Pt (0.5 Å/s), TiW (0.1 Å/s); Doesn't significantly etch Au, Pyrex (roughens), quartz (roughens), sapphire (roughens), Si, Si(poly), SiGe(poly), Si_3N_4, SiO_2, Ta (thickens); exothermic; add H_2O_2 immediately prior to use; DI water rinse [27, 28]
96	Nickel (Ni), deposited		H_2SO_4(96%): H_2O_2(30%) 1:4	60°C; doesn't significantly etch $NiSi_2$, Si, SiO_2; DI water rinse [311, 312]
97	Nickel (Ni)		H_2SO_4(96%): H_3PO_4(85%): HNO_3(70%):Acetic 1:1:3:5	85–95°C; DI water rinse [53]
98	Nickel (Ni)		H_2SO_4(96%): H_3PO_4(85%): HNO_3(70%):Acetic 1:1:3:5	40°C; doesn't significantly etch $NiSi_2$; DI water rinse [97]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
99	Nickel (Ni)		HCl(38%): H_2O_2(30%) 3:1	Room temperature; doesn't significantly etch $NiSi_2$; DI water rinse [97]
100	Nickel (Ni), nickel–cobalt (NiCo)		HCl(38%): HNO_3(70%):Acetic 1:80:120	20°C; DI water rinse [53, 313]
101	Nickel (Ni), deposited		HCl(38%): HNO_3(70%):H_2O 5:1:3	Room temperature; selective to $NiSi_2$; DI water rinse [314]
102	Nickel (Ni), deposited	17	HCl(38%): HNO_3(70%):H_2O 3:1:2	30°C; dilute aqua regia; mask with PR; Etches Ag, Al (100 Å/s), AlSi(2%), Au (115 Å/s), Cu (100 Å/s), Mo (110 Å/s), Pd (65 Å/s), Pt (0.6 Å/s), W (1 Å/s); Etches slightly Al_2O_3 (0.2 Å/s), SiO_2(PECVD) (0.1 Å/s), Ta (0.3 Å/s), Ti (0.1 Å/s), TiW (0.6 Å/s); Doesn't significantly etch Cr, Nb, polyimide, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta; water added to reduce PR attack; self-heating; DI water rinse [28]
103	Nickel (Ni), deposited		HF(49%): HNO_3(70%) 1:1	Room temperature; dilute with H_2O to reduce etch rate; DI water rinse [315]
104	Nickel (Ni)		HNO_3(70%) undiluted	Room temperature; dilute with H_2O to reduce etch rate; DI water rinse [12]
105	Nickel (Ni), sputtered	17	HNO_3(70%):H_2O 1:20	45°C; DI water rinse [316]
106	Nickel (Ni)		HNO_3(70%): H_2SO_4(96%):Acetic 3:2:3	Room temperature; etches Cu and Cu alloys at similar rate; dilute with H_2O for reduced rate; DI water rinse [288]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
107	Nickel (Ni)	1600	HNO_3(70%): H_2SO_4(96%): H_3PO_4(85%):Acetic 3:1:1:5	85°C; DI water rinse [317]
108	Nickel (Ni), evaporated or sputtered with Cr, Au	30	Nitric acid, potassium perfluoroalkyl sulfonate	25°C; Transene nickel etchant TFB; mask with PR; Etches Al, Cr, Cu, GaAs; Doesn't significantly etch Au, Si_3N_4, SiO_2, Ti, W; glass tank; DI water rinse [318]
109	Nickel (Ni), electroless or electroplated on GaAs or Cu	50	Nitrate-based	40°C; Transene nickel etchant TFG; mask with PR; Etches Al; Doesn't significantly etch Au, Cr, Cu, Si, Si_3N_4, SiO_2, Ti, W, GaAs, Ta, TaN; glass tank; DI water rinse [318]
110	Nickel-Phosphorus (NiP, 90:10)		H_3PO_4(85%): HNO_3(70%) 9:1	Room temperature; DI water rinse [91]
111	Niobium (Nb)	11	H_2SO_4(96%) undiluted	175°C; DI water rinse [319]
112	Niobium (Nb)		HCl(38%): HF(49%): HNO_3(70%):H_2O 2:1:2:2	Room temperature; DI water rinse [53]
113	Niobium (Nb)		HF(49%):H_2O 1:1	Room temperature; DHF etchant (1:1); DI water rinse [319]
114	Niobium (Nb)		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [98]
115	Osmium (Os)		HCl(38%): HNO_3(70%) 3:1	Warm; aqua regia; DI water rinse [320]
116	Palladium (Pd)		HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [320]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
117	Palladium (Pd), evaporated	15	HCl(38%): HNO_3(70%):Acetic 1:10:10	25°C; DI water rinse [321]
118	Palladium (Pd), deposited	65	HCl(38%): HNO_3(70%):H_2O 3:1:2	30°C; dilute aqua regia; mask with PR; Etches Ag, Al (100 Å/s), AlSi(2%), Au (115 Å/s), Cu (100 Å/s), Mo (110 Å/s), Ni (17 Å/s), Pt (0.6 Å/s), W (1 Å/s); Etches slightly Al_2O_3 (0.2 Å/s), SiO_2(PECVD) (0.1 Å/s), Ta (0.3 Å/s), Ti (0.1 Å/s), TiW (0.6 Å/s); Doesn't significantly etch Cr, Nb, polyimide, quartz, sapphire, Si, Si(poly), Si_3N_4, SiO_2, Ta; water added to reduce PR attack; self-heating; DI water rinse [28]
119	Palladium (Pd)		HNO_3(70%) undiluted	Hot; DI water rinse [320]
120	Palladium (Pd), sputtered		KI:I_2:H_2O 10 g:1 g:40 mL	Room temperature; selective to $PdSi_2$; DI water rinse [322]
121	Palladium (Pd), evaporated or sputtered	110	Ferric chloride and hydrogen chloride [323]	50°C; Transene palladium etchant TFP; mask with PR; Doesn't significantly etch Au, Ni; glass, Pyrex or PVC tank; DI water rinse [324]
122	Permalloy (NiFeMo), sputtered	65	H_2SO_4(96%): HF(49%): H_2O_2(30%):H_2O 6:1:1:22	23°C; Ni:Fe:Mo 79:16:5 wt%; DI water rinse [325]
123	Platinum (Pt)		H_2O_2(30%) undiluted	Boiling; DI water rinse [45]
124	Platinum (Pt), sputtered	5	HCl(38%): HNO_3(70%) 19:1	Boiling; hard-bake PR; DI water rinse [326]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
125	Platinum (Pt)		HCl(38%): HNO_3(70%) 8:1	70°C; DI water rinse [98]
126	Platinum (Pt), deposited		HCl(38%): HNO_3(70%):H_2O 3:1:4	45°C; dilute aqua regia; DI water rinse [327]
127	Platinum (Pt), deposited		HCl(38%): HNO_3(70%):H_2O 3:1:4	85°C; dilute aqua regia; precede with brief BHF etch; DI water rinse [328]
128	Platinum (Pt), CVD	8	HCl(38%): HNO_3(70%):H_2O 7:1:8	85°C; DI water rinse [329, 330]
129	Platinum (Pt)		HF(49%): HNO_3(70%) 4:1	Hot; DI water rinse [53]
130	Rhenium (Re)		H_2SO_4(96%) undiluted	Hot; DI water rinse [320]
131	Rhenium (Re)		HNO_3(70%):H_2O 1:1	Room temperature; DI water rinse [25]
132	Rhodium (Rh)		H_2SO_4(96%) undiluted	Hot; DI water rinse [320]
133	Rhodium (Rh)		HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [26]
134	Ruthenium (Ru)		HCl(38%): HNO_3(70%) 3:1	Warm; aqua regia; DI water rinse [320]
135	Ruthenium (Ru), evaporated or sputtered	40–50	Ceric ammonium nitrate, nitric acid	20–25°C; Transene ruthenium etchant RU-44; mask with PR; glass or polypropylene tank; DI water rinse [331]
136	Silver (Ag)		H_2SO_4(96%) undiluted	Hot; DI water rinse [320]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
137	Silver (Ag), deposited	100	H_2SO_4(96%): H_2O_2(30%) 56:1	120°C; high-sulfuric piranha; Etches Al (850 Å/s), AlSi(2%) (30 Å/s), Al_2O_3 (3–15 Å/s), Cr (1–3 Å/s), Cu (15 Å/s), Mo (3 Å/s), Nb (1 Å/s), Ni (65 Å/s), NiCr (15 Å/s), polyimide (2800 Å/s), Ti (40 Å/s); Etches slightly Parylene type C (0.4 Å/s), Pt (0.5 Å/s), TiW (0.1 Å/s); Doesn't significantly etch Au, Pyrex (roughens), quartz (roughens), sapphire (roughens), Si, Si(poly), SiGe(poly), Si_3N_4, SiO_2, Ta (thickens); exothermic; add H_2O_2 immediately prior to use; DI water rinse [27, 28]
138	Silver (Ag)		HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [320]
139	Silver (Ag)	1600	HNO_3(70%):H_2O 7:1	Room temperature; DI water rinse [332]
140	Silver (Ag)	2000–4000	HNO_3(70%):H_2O 1:1 to 1:10	40–50°C; DI water rinse [10]
141	Silver (Ag)		NH_4OH(29%): H_2O_2(30%) 1:1	Room temperature; DI water rinse [26, 45]
142	Silver (Ag)	60	NH_4OH(29%): H_2O_2(30%):Acetic 1:1:4	Room temperature; DI water rinse [8]
143	Silver (Ag), deposited	200	KI, I_2	25°C; Transene silver etchant TFS; mask with PR; Etches Al, Au, GaAs; glass tank; Doesn't significantly etch Cr, Si, Si_3N_4, SiO_2, Ta, TaN, Ti, W; agitate for higher etch rate; DI water rinse [333]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
144	Silver (Ag), deposited	75	Ceric ammonium nitrate, nitric acid	20°C; Cyantek CR-7; mask with PR; Etches Al (6 Å/s), Cr (25 Å/s), Cu (45 Å/s), Ge(poly) (45 Å/s), NiCr (2 Å/s), V (10 Å/s); Etches slightly Al_2O_3 (<0.1 Å/s), graphite (0.1 Å/s), Mo (0.5 Å/s), Ni (0.3 Å/s), quartz (0.1 Å/s), SiGe(poly) (<0.1 Å/s), SiO_2 (<0.01 Å/s), Ta (0.1 Å/s), Ti(0.3 Å/s), TiW (0.1 Å/s), W (0.5 Å/s); Doesn't significantly etch Au, Nb, Pd, polyimide, Pt, Pyrex, sapphire, Si, Si(poly), Si_3N_4, SiO_2; DI water rinse [28]
145	Steel, low-carbon		H_2SO_4(96%): H_2O_2(30%):H_2O 15:90:10	25°C; DI water rinse [53]
146	Steel, low-carbon		H_2SO_4(96%): H_3PO_4(85%): HNO_3(70%) 1:3:1	85°C; DI water rinse [53]
147	Steel, medium-carbon		HF(49%): H_2O_2(30%):H_2O 1:10:10	Room temperature; DI water rinse [53]
148	Steel, stainless (SS)		H_3PO_4(85%): HCl(38%): HNO_3(70%):Acetic 1:1:4:5	70°C; DI water rinse [53]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
149	Steel, stainless (SS)		HCl(38%): HNO_3(70%):H_2O 1:1:1	Room temperature; DI water rinse [92]
150	Tantalum (Ta)		H_2SO_4(96%): HF(49%): HNO_3(70%) 5:2:2	Room temperature; DI water rinse [334, 335]
151	Tantalum (Ta)		H_3PO_4(85%) undiluted	180°C; DI water rinse [336, 337]
152	Tantalum (Ta), PVD	0.8	HF(49%):H_2O 1:10	25°C; DI water rinse [338]
153	Tantalum (Ta)		HF(49%): HNO_3(70%) 1:2	Room temperature; add water to slow etch; DI water rinse [16]
154	Tantalum (Ta)		HF(49%): HNO_3(70%):H_2O 2:2:5	Room temperature; DI water rinse [98]
155	Tantalum (Ta), deposited	70–80	Hydrofluoric acid	25°C; Transene tantalum etch SIE-8607; mask with PR; Etches Al, Cr, Cu, GaAs, Ni, Si, SiO_2, Ta, TaN, Ta_2O_5, Ti; Doesn't significantly etch Au, Si_3N_4, W; DI water rinse [254]
156	Thorium (Th)		HCl(38%) undiluted	20°C; DI water rinse [339]
157	Thorium (Th)		HCl(38%): HNO_3(70%) 3:1	20°C; DI water rinse [339]
158	Tin (Sn)		HCl(38%) undiluted	Room temperature; DI water rinse [340]
159	Tin (Sn)		HCl(38%):H_2O 1:4	Room temperature; DI water rinse [98]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
160	Tin (Sn)		HCl(38%):HF(49%) 1:1	Room temperature; DI water rinse [98]
161	Tin (Sn)		HCl(38%): HNO_3(70%) 3:1	Room temperature; DI water rinse [26]
162	Tin (Sn), deposited		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [76]
163	Tin–nickel (SnNi), electroplated	3	HCl(38%):H_2O 1:3	25°C; Room temperature; Sn:Ni 65:35 wt%; etches SnNo 5 Å/s at 50°C, 9 Å/s at 75°C; DI water rinse [341]
164	Titanium (Ti)			See Table 8.8
165	Tungsten (W)			See Table 8.8
166	Vanadium (V), deposited		H_2SO_4(96%): HF(49%): HNO_3(70%) 5:2:2	Room temperature; DI water rinse [45]
167	Vanadium (V)		H_3PO_4(85%) undiluted	180°C; DI water rinse [342]
168	Vanadium (V)		HCl(38%): HF(49%): HNO_3(70%):H_2O 2:1:2:2	Room temperature; DI water rinse [53]
169	Vanadium (V)		HCl(38%): HNO_3(70%) 3:1	Room temperature; aqua regia; DI water rinse [26]
170	Vanadium (V), CVD		HF:HNO_3(70%) 1:10	Room temperature; DI water rinse [343]
171	Vanadium (V), CVD		HF:HNO_3(70%): H_2O 1:1:1	Room temperature; HNW etchant; DI water rinse [98]
172	Vanadium (V)		HNO_3(70%):H_2O 1:3	35°C; DI water rinse [342]

Table 8.19 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
173	Vanadium (V), deposited		NH_4OH(29%): H_2O_2(30%) 1:4	Room temperature; DI water rinse [344]
174	Yttrium (Y)		HNO_3(70%) undiluted	Room temperature; DI water rinse [345, 346]
175	Zinc (Zn)		HCl(38%):H_2O 1:1	Room temperature; DI water rinse [26]
176	Zinc (Zn)	4000	HNO_3(70%):H_2O 1:4	50°C; DI water rinse [10]
177	Zinc (Zn)		HNO_3(70%): H_2O_2(30%):Ethanol 1:1:1	Room temperature; DI water rinse [53]
178	Zirconium (Zr)		H_2SO_4(96%) undiluted	Hot; DI water rinse [347]
179	Zirconium (Zr)		HCl(38%) undiluted	Hot; DI water rinse [347]
180	Zirconium (Zr)		HCl(38%): HNO_3(70%) 3:1	60°C; aqua regia; DI water rinse [347]
181	Zirconium (Zr)		HF(49%): HNO_3(70%):H_2O 1:5:5	Room temperature; HNW etchant; can substitute H_2O_2 for H_2O; DI water rinse [348]
182	Zirconium (Zr)		HF(49%): HNO_3(70%):H_2O 1:1:50	Room temperature; HNW etchant; DI water rinse [98]

Table 8.20 Silicide etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Chrome–silicon (CrSi)	10–15	H_3PO_4(85%): HF(49%): HNO_3(70%) 60:1:5	Room temperature; DI water rinse [16]
2	Chrome–silicon (CrSi), thin film on Cu, Ni or Au	15–20	Potassium hexacyanoferrate	50°C; Transene chromium cermet etchant TFE; mask with negative PR; etches CrO; Doesn't significantly etch Au, Cu, Ni; glass tank; stirring helpful; DI water rinse [349]
3	Chromium silicide ($CrSi_2$)		H_2SO_4(96%): H_3PO_4(85%): H_2O 1:4:2	Room temperature; DI water rinse [21]
4	Chromium silicide ($CrSi_2$)		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [21]
5	Cobalt silicide ($CoSi_2$)		H_3PO_4(85%) undiluted	155°C; DI water rinse [17, 21, 125, 127, 350]
6	Cobalt silicide ($CoSi_2$), sputtered Co on Si and sintered	6	HF(49%):H_2O 1:20	Room temperature; DHF etchant (20:1); DI water rinse [351]
7	Copper–Silicon (CuSi)		H_3PO_4(85%): HCl(38%): HNO_3(70%):Acetic 1:1:3:5	70–80°C; DI water rinse [53]
8	Hafnium silicide ($HfSi_2$)		HF(49%):H_2O	Resistant to aqueous alkali and inorganic acids except HF, aqua regia and sulfuric-peroxide mixtures; DI water rinse [125, 127]

Table 8.20 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
9	Iron silicide ($FeSi_2$)		HCl(38%): HF(49%): HNO_3 (70%):H_2O 50:1:5:44	Room temperature; ternary alloys with Cr and V; DI water rinse [352]
10	Iron silicide ($FeSi_2$)		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); DI water rinse [21]
11	Iron silicide ($FeSi_2$)		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [21]
12	Magnesium silicide (Mg_2Si)		Acetic undiluted	Room temperature; DI water rinse [21]
13	Magnesium silicide (Mg_2Si)		HF(49%): HNO_3(70%) 5:1	Room temperature; DI water rinse [26]
14	Manganese silicide ($MnSi_2$)		HCl(38%): HNO_3(70%) 3:1	Room temperature; DI water rinse [21]
15	Manganese silicide ($MnSi_2$)		HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [21]
16	Molybdenum silicide ($MoSi_2$)		H_2SO_4(96%): H_3PO_4(85%):H_2O 1:4:2	Room temperature; doesn't significantly etch Mo_5Si_3; DI water rinse [21]
17	Molybdenum silicide ($MoSi_2$)	3.3	HF(49%): HNO_3(70%) 1:1	Room temperature; DI water rinse [21, 45, 127]

Table 8.20 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
18	Nickel silicide ($NiSi_2$), sintered		HF(49%):H_2O 1:10	Room temperature; DHF etchant (10:1); reduce etch rate with cathodic protection; DI water rinse [127, 353]
19	Nickel silicide ($NiSi_2$)		HF(49%): HNO_3(70%) 1:3	Room temperature; agitate ultrasonically; DI water rinse [354]
20	Nickel silicide ($NiSi_2$), sintered	6	Phosphoric, acetic, nitric and fluoroboric acids with water	Room temperature; Freckle etch, Arch Chemicals; etches silicon (100 surface at 3 Å/s), AlSi (1%) (9 Å/s); DI water rinse [355]
21	Niobium silicide ($NbSi_2$)		H_2SO_4(96%): H_3PO_4(85%):H_2O 1:4:2	Room temperature; DI water rinse [21]
22	Niobium silicide ($NbSi_2$)		HF(49%): HNO_3(70%):H_2O 4:10:86	Room temperature; HNW etchant; also Kroll's reagent; DI water rinse [356]
23	Niobium silicide ($NbSi_2$)		HF(49%): NH_4F (40%) 1:10	Room temperature; BHF etchant (10:1); DI water rinse [127]
24	Palladium silicide (Pd_2Si)		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); DI water rinse [26]
25	Palladium silicide (Pd_2Si)		HF(49%): HNO_3(70%)	Room temperature; DI water rinse [127]
26	Platinum silicide (PtSi), sintered		HCl(38%): HNO_3(70%) 3:1	85°C; aqua regia; precede with BHF etch; DI water rinse [328, 329]

Table 8.20 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
27	Platinum silicide (PtSi), sintered		HCl(38%): HNO_3(70%):H_2O 3:1:4	60°C; also etches Pt; DI water rinse [357]
28	Platinum silicide (PtSi)		HF(49%): HNO_3(70%)	Room temperature; DI water rinse [127]
29	Platinum silicide (PtSi)		HF(49%): HNO_3(70%):Acetic 1:3:4	Room temperature; HNA etchant; DI water rinse [45]
30	Rhenium silicide (ReSi)		HF(49%): HNO_3(70%):H_2O	Room temperature; HNW etchant; DI water rinse [358]
31	Rhodium silicide (RhSi), sintered		HF(49%): HNO_3(70%):Acetic 4:9:7	Room temperature; HNA etchant; etches Rh and Si; DI water rinse [359]
32	Ruthenium Silicide (Ru_2Si_3)	23	HF(49%): KOCl (11%):H_2O 1:3:50	Room temperature; nonstandard chemical; DI water rinse [360]
33	Tantalum silicide ($TaSi_2$)		H_2SO_4(96%): H_3PO_4(85%):H_2O 1:4:2	Room temperature; DI water rinse [21]
34	Tantalum silicide ($TaSi_2$), LPCVD		HF(49%) undiluted	40°C; HF etchant (49 wt%); DI water rinse [361]
35	Tantalum silicide ($TaSi_2$), LPCVD		HF(49%): HNO_3(70%) 1:25	Room temperature; also etches Si; DI water rinse [362]

Table 8.20 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
36	Tantalum silicide ($TaSi_2$), sintered	3.3	HF(49%): NH_4F (40%) 1:10	Room temperature; BHF etchant (10:1); DI water rinse [127, 363]
37	Tantalum silicide ($TaSi_2$)	50	Proprietary	20°C; Transene; DI water rinse [364]
38	Titanium silicide (Ti_2Si_3)		H_2O_2(30%) undiluted	20°C; etches Ti_2Si_3, other compositions unknown; DI water rinse [21]
39	Titanium silicide ($TiSi_2$)	25	HF(49%):H_2O 1:100	Room temperature; DHF etchant (100:1); insoluble in aqueous alkali and most inorganic acids; DI water rinse [127, 128, 365]
40	Titanium silicide ($TiSi_2$)	45	HF(49%):H_2O 1:40	Room temperature; DHF etchant (40:1); DI water rinse [128]
41	Titanium silicide ($TiSi_2$), sintered	25	HF(49%): NH_4F (40%) 1:10	Room temperature; BHF etchant (10:1); DI water rinse [363]
42	Titanium silicide ($TiSi_2$), evaporated	0.7	KOH:H_2O 500 g:1000 mL	70°C; KOH etchant (30 wt%); etches silicon (100 surface at 85 Å/s); DI water rinse [366]
43	Titanium-tungsten silicide (TiWSi), sintered		HCl(38%): HNO_3(70%) 3:1	Room temperature; $Ti_{0.3}W_{0.7}Si_2$; Di water rinse [367]
44	Tungsten silicide (WSi_2), sintered		HF(49%): HNO_3(70%):H_2O 4:10:86	Room temperature; HNW etchant; also Kroll's reagent; insoluble in aqua regia and most inorganic acids; DI water rinse [127, 365, 368, 369]
45	Tungsten silicide (WSi_2), CVD		HF(49%): HNO_3(70%):H_2O 2:60:40	Room temperature; HNW etchant; etches Si; DI water rinse [370]

Table 8.20 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
46	Tungsten silicide (WSi_2)		HNO_3(70%): NH_4F (40%) 49:1	Room temperature; DI water rinse [45]
47	Vanadium silicide (VSi_2)		HF(49%): NH_4F (40%) 1:10	Room temperature; BHF etchant (10:1); DI water rinse [127]
48	Vanadium silicide (VSi_2)		H_2SO_4(96%): H_3PO_4(85%):H_2O 1:4:2	Room temperature; DI water rinse [21]
49	Vanadium silicide (V_3Si)		HF(49%): HNO_3(70%) 1:6	Room temperature; DI water rinse [371]
50	Vanadium silicide (V_3Si)		HF(49%): HNO_3(70%): H_2O_2(30%) 1:1:4	Room temperature; DI water rinse [372]
51	Zirconium silicide ($ZrSi_2$)		HF(49%):H_2O	Room temperature; DHF etchant; DI water rinse [127]
52	Oxides of ($CoSi_2$), ($CrSi_2$), (Ir_3Si_5), ($NiSi_2$), (Ru_2Si_3), (Si), (WSi_2), thermally grown	2.5–4	HF(49%): NH_4F (40%) 1:50	Room temperature; BHF etchant (50:1); thermally grown oxides; DI water rinse [373]

masking materials are limited to low temperatures to avoid excessive cross-linking, melting, or burning of the underlying polymer. Polymers that are photosensitive such as PMMA, SU-8, photo-sensitive polyimide, BCB, and commercial photoresists may need no masking layer. Etch rates and etchants for some plastics and polymers are listed in Table 8.21. Typically, polymers may be etched in an oxygen plasma. Particularly stubborn thin materials may be sputter-etched with an argon plasma. Chemical resistance of polymers varies widely and assessments can be found in the literature [374].

8.5.3 Examples: Wet Chemical Etching of Nonstandard Materials

Plastic and polymeric thin films may be desirable in an IC or MEMS process for passivation, corrosion resistance, overmolding, chip-scale packages, chemical specificity, expansion with absorption, and relatively low elastic moduli. Modern plastics provide a wide variety of properties that can be favorably exploited for small lightweight sensors and ICs. Bio-MEMS devices utilize biocompatible polymers with relatively large feature sizes. Photoresponsive polymers can be patterned directly with submicron features and used directly or as molds for other polymer processes. Epoxies and solvent bonding techniques can be used to assemble smaller sections of a system. Traditional micromachining of silicon substrates is greatly expanded and in some cases supplanted by the use of these alternative materials in a variety of optical, electrical, chemical, and mechanical sensors and actuators. The appropriate selection of materials is governed largely by cost, performance, and availability. Several examples for wet chemical etching of nonstandard materials follow.

8.5.3.1 Example 1: BCB Patterning and Etching

Negative-acting BCB resist is equilibrated to room temperature, hand-dispensed at 100 RPM on a borosilicate glass wafer and spun at ~2500 RPM in a well-ventilated hood to produce a 5 μm-thick layer. The wafer is pretreated with an adhesion promoter before BCB application, and a Q-tip soaked with developer is placed against the wafer periphery near the end of the high-speed spin to remove excess resist. The wafer is prebaked on an in-line hot plate for 90 s at 65°C; exposed within the day to form seal-ring patterns using a contact aligner; and then puddle-developed on a wafer-track using a commercial developer until unexposed areas are cleared, rinsed with a DI water spray at 10 s at 500 RPM, spun dry at 3000 RPM for 30 s, and postbaked for 60 s at 90°C. The wafer is then diced and each cap die is flip-chip bonded to an underlying silicon RF-MEMS wafer using a 250 g force for 3 min in air at 120°C. A nonhermetic seal is made by reflowing and curing the BCB in the flip-chip assembly at 250°C for 20 min. The cap wafer may be reworked if needed using a commercial stripper at 80°C to remove the BCB after exposure and before curing (the developer may be used if the wafer has not been exposed), using the commercial stripper at 95°C for partially cured BCB, dry etching the cured film in

Table 8.21 Plastics and polymer etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Benzocyclo-butene (BCB), spun and cured		H_2SO_4(96%): H_2O_2(30%) 4:1	120°C; exothermic mixture; DI water rinse [375, 376]
2	Benzocyclo-butene (BCB), spun and cured	180	SF_6:O_2 plasma 15:95 sccm	Dry etch; cured material; 260 W, 1000 mTorr; also etches in CF_4:O_2 plasma or straight O_2 for BCB without silicon [377]
3	Cyclic olefin copolymer (COC)		Heptane undiluted	Room temperature; nonstandard solvent; DI water or isopropyl alcohol rinse [378]
4	Cyclic olefin copolymer (COC)		Hexadecane:IPA 1:12	Room temperature; nonstandard chemical; solvent bonding; isopropyl alcohol rinse [378]
5	Epoxy, aluminum-filled		H_2SO_4(96%) undiluted	Hot; DI water rinse [26]
6	Epoxy, gold-filled		HNO_3(70%): HCl(38%):H_2O 3:1:10	Room temperature; DI water rinse [26]
7	Epoxy, silver-filled		HF(49%): HNO_3(70%) 1:3	Room temperature; DI water rinse [26]
8	Fluorinated ethylene propylene (FEP, Teflon-FEP), film		THF undiluted	Warm; nonstandard solvent; surface modifier; DI water or isopropyl alcohol rinse [379]
9	Liquid crystal polymer (LCP), plastic packages		H_2SO_4(96%): HNO_3(70%) 1:9	60°C; less attack on metallurgy; rinse with acetone while part is hot; finish with DI water rinse then isopropyl alcohol with ultrasonic agitation [45]
10	Liquid crystal polymer (LCP), plastic packages		HNO_3(70%) undiluted	60–70°C; etches nonferrous metals; rinse with acetone while part is hot; finish with DI water rinse then isopropyl alcohol with ultrasonic agitation [45]

Table 8.21 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
11	Liquid crystal polymer (LCP), sheet	40	O_2 RIE	Dry etch; mask with Al; 350 W, 500 mTorr [380]
12	Novolak (PR)	80	Isopropyl alcohol undiluted	50°C; etch rate is 40 Å/s at 27°C; DI water or isopropyl alcohol rinse [381]
13	Octadecyltri-chlorosilane (OTS)		HCl(38%):H_2O 1:10	Room temperature; pretreated surface; DI water rinse [382]
14	Photoresist (PR), vexing		Air ambient	450–650°C; negative and positive resists [383, 384]
15	Photoresist (PR), vexing		H_2SO_4(96%): H_2O_2(30%) 1:1	160°C; negative and positive resists; mix fresh; DI water rinse [383]
16	Photoresist (PR), vexing		O_2 plasma	Dry ashing; negative and positive resists; removal rate increases with wafer temperature; high selectivity to SiO_2 and Si [383, 385]
17	Photoresist (PR)	50	Ozone:H_2O	95°C; ozone-rich water; add ammonium hydroxide to remove etch residues; DI water rinse [386]
18	Photoresist (PR), thick negative or positive resist	110–750	Ozone:Solvent	Room temperature; solvent selected for high ozone solubility; DI water rinse [387]
19	Polyaniline (PANI)		H_2SO_4(96%) undiluted	Room temperature; DI water rinse [388]
20	Polyaniline (PANI)		NMP undiluted	Room temperature; nonstandard solvent; DI water or isopropyl alcohol rinse [389, 390, 391, 392]
21	Polycaprolactone (PCL)		Acetone undiluted	Room temperature; also reacts with isopropyl alcohol and gold etchant (type TFA); DI water rinse [393]
22	Polycarbonate (PC), sheet film		Acetone undiluted	Room temperature; DI water rinse [394]

Table 8.21 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
23	Polycarbonate (PC)		MEK undiluted	Room temperature; nonstandard solvent; solvent bonding; DI water or isopropyl alcohol rinse [395]
24	Polydimethyl-siloxane (PDMS)		Acetone undiluted	Room temperature; swells film [396]
25	Polydimethyl-siloxane (PDMS)	55	CF_4:O_2 RIE 3:1	Dry etch; 270 W; 47 mTorr [397]
26	Polydimethyl-siloxane (PDMS)		HCl(38%):H_2O 1:5	Room temperature; surface treatment; DI water rinse [398]
27	Polydimethyl-siloxane (PDMS)	1600	TBAF:NMP 1:1	Room temperature; nonstandard chemicals; DI water rinse [399]
28	Polydimethyl-siloxane (PDMS)		TBAF:THF 1 g:1 mL	Room temperature; 1.0 M solution; non-standard chemicals; DI water rinse [400]
29	Polyester, substrate		H_2SO_4(96%): H_2O_2(30%) 7:3	90°C; surface modification; DI water rinse [401]
30	Polyethylene (PE)		H_2SO_4(96%): $K_2Cr_2O_7$: H_2O 150:7:12 by weight	70°C; chromic acid; nonstandard chemical; slightly etches polypropylene (PP); DI water rinse [402]
31	Polyethylene (PE)		H_2SO_4(96%):CrO_3: H_2O 29:29:42 by weight	75°C; chromic acid; nonstandard chemical; follow with HNO_3 at 50°C or HCl:H_2O 1:1 (6 N) at 50°C; DI water rinse [403]

Table 8.21 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
32	Polyethylene glycol (PEG)		H_2O undiluted	Room temperature; also dissolves in acetone and alcohol [404]
33	Polyethylene terephthalate, (PET), Mylar®	4200	H_2SO_4(96%): Phenol:H_2O 115:76:9 by weight	110°C; nonstandard chemical; DI water rinse [405]
34	Polyimide (PI, Kapton®), adhesive-backed tape		Acetone undiluted	Apply tape with tweezers on top of PR; peel tape off manually or soak in acetone to remove [406]
35	Polyimide (PI)	150	$CF_4/Ar/O_2$ plasma 5:10:30 sccm	Dry etch; 300 mT; 180 W; etches Si_3N_4 (9 Å/s), oxide-LTO (9 Å/s), Si (3 Å/s); doesn't significantly etch Al [45]
36	Polyimide–Kevlar (PI–Kevlar®), PCB substrates		H_2SO_4(96%) undiluted	185°C; DI water rinse [407]
37	Polyimide (PI)		H_2SO_4(96%): H_2O_2(30%) 7:1	80°C; Caro's acid; DI water rinse [45]
38	Polyimide (PI), spun	2800	H_2SO_4(96%): H_2O_2(30%) 50:1	120°C; add fresh peroxide; DI water rinse [28]
39	Polyimide (PI), spun	1	HF(49%): NH_4F (40%) 1:5	20°C; BHF etchant (5:1); DI water rinse [28]
40	Polyimide (PI)		HNO_3(70%) undiluted	60°C; DI water rinse [45]

Table 8.21 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
41	Polyimide (PI)	650	O_2 plasma	Dry etch; lateral etch rate; doesn't significantly etch SiC [408]
42	Polyimide (PI, Kapton®)	55–295	Proprietary	40–60°C; Transene Kapton polymide film etchant; mask with PR or Riston [409]
43	Polymer, residues		H_2SO_4(96%): H_2O_2(30%) 2:1 to 4:1	90–140°C; general organics; DI water rinse [109]
44	Polymer, residues		HF(49%):H_2O 1:10 to 1:200	25°C; DHF etchant; can undercut organics; DI water rinse [109, 410]
45	Polymer, residues		NH_4OH(29%): H_2O_2(30%):H_2O 1:1:5	40–75°C; general organics; DI water rinse [109]
46	Polymer, sidewall		NH_4OH(29%): H_2O_2(30%) 5:1	120°C; polymer-dependent; can etch Si; DI water rinse [411]
47	Polymer, sidewall		H_2SO_4(96%): H_2O_2(30%) 4:1	120°C; polymer-dependent; DI water rinse [411]
48	Polymethylmeth-acrylate (PMMA)		Acetone undiluted	Room temperature; may use ultrasonic agitation; DI water or isopropyl alcohol rinse [412]
49	Polymethylmeth-acrylate (PMMA)		Chloroform undiluted	Room temperature; nonstandard solvent; solvent bonding of PMMA–PMMA [413]
50	Polymethylmeth-acrylate (PMMA)		DCM undiluted	Room temperature; nonstandard solvent; DI water or isopropyl alcohol rinse [414]

Table 8.21 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
51	Polymethylmeth-acrylate (PMMA)		NMP undiluted	Room temperature; nonstandard solvent; consider MEK, THF or others [415]
52	Polyparaxylylene (Parylene C)	80	O_2 RIE 120 sccm	Dry etch; 400 W; 200 mTorr [416, 417]
53	Polypropylene (PP)	0.3	CrO_3:H_2O 600 g:1000 mL	70°C; chromic acid, 6 M solution; nonstandard chemical; DI water rinse [418]
54	Polypropylene (PP)		DCM undiluted	70°C; DI water or isopropyl alcohol rinse [419]
55	Polypropylene (PP)		HCl(38%): HNO_3(70%) 3:1	Warm; aqua regia; DI water rinse [420]
56	Polystyrene (PS), sheet film		Acetone undiluted	Room temperature; DI water rinse [394]
57	Polystyrene (PS), spun		Toluene undiluted	Room temperature; nonstandard solvent; doesn't significantly etch SU-8; DI water rinse [421]
58	Polysulfone (PSF)		NMP undiluted	Room temperature; nonstandard solvent; DI water or isopropyl alcohol rinse [422]
59	Polytetrafluoro-ethylene (PTFE, Teflon), substrate	160	Ar IBE	Ion beam etch; Ar^+ ions; 500 eV; 0.5 mA/cm^2, [423]
60	Polytetrafluoro-ethylene (PTFE, Teflon), film		Benzoin dianon: Potassium tert-butoxide:Me_2SO 0.27 g:1.0 g: 35 mL	50°C; nonstandard chemicals; surface modification; strip with $KClO_3$ in H_2SO_4; DI water or isopropyl alcohol rinse [424, 425]

Table 8.21 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
61	Polytetrafluoro-ethylene (PTFE, Teflon), sheet film		Sodium, naphthalene	50°C; FluoroEtch®, Acton Technologies; non-standard chemical; surface treatment; not for cross-linked fluoropolymers; IPA and DI water rinse [426, 427]
62	Polytetrafluoro-ethylene (PTFE, Teflon), film		THF undiluted	Warm; nonstandard solvent; surface modification; DI water or isopropyl alcohol rinse [424]
63	Polyurethane (PU)		Acetone	Room temperature; causes swelling then weight loss with 65°C bakeout [428, 429]
64	Polyvinyl chloride (PVC)		MEK undiluted	Room temperature; nonstandard solvent; DI water or isopropyl alcohol rinse [430]
65	Polyvinyl chloride (PVC)		THF undiluted	Room temperature; nonstandard solvent; DI water or isopropyl alcohol rinse [431]
66	Polyvinylidene fluoride (PVDF)		HNO_3(70%) undiluted	Elevated temperature; DI water rinse [432]
67	Polyvinylidene fluoride (PVDF)		NMP undiluted	Room temperature; nonstandard solvent; DI water or isopropyl alcohol rinse [422]
68	Residues, inorganic		H_2O undiluted	Room temperature; water-soluble inorganics such as salts, electrolytes, acidic residues, alkaline residues [45]
69	Residues, organic		H_2SO_4(96%): H_2O_2(30%) 7:3	Elevated temperature; stubborn organics; exothermic; stir and mix carefully; do not store; consider O_2 plasma; DI water rinse [45]
70	Residues, organic		Isopropyl alcohol, Acetone undiluted	Room temperature; soluble organics; DI water rinse [45]
71	Silicone, gel		Isopropyl alcohol undiluted	Room temperature; effective for silicone gels; DI water rinse [45]
72	Silicone		HNO_3(70%) undiluted	Room temperature soak; can heat to boiling for faster removal; consider commercial strippers; DI water rinse [45]

Table 8.21 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
73	Silicon rubber (RTV), encapsulant	530	TMAH (24 wt% in methanol):IPA 1:10	38°C; IPA rinse [433]
74	SU-8 (PR), spun and uncured		Acetone undiluted	Room temperature; DI water rinse [434]
75	SU-8 (PR), spun		H_2SO_4(96%): H_2O_2(30%) 50:1	60°C; DI water rinse [435]
76	SU-8 (PR), spun		Methyl chloride, phenol, and organic acids	Room temperature; Miller–Stephenson MS-111 epoxy stripping agent, nonstandard solvent; DI water rinse [436]
77	SU-8 (PR), spun	165	NMP undiluted	Hot; nonstandard solvent; DI water rinse [421]

a CF_4:O_2 (20:80) or SF_6:O_2 (10:90) plasma, or by using a piranha solution of sulfuric acid and hydrogen peroxide (4:1) at 120°C followed by a DI-water rinse and spin dry [376, 437, 438].

8.5.3.2 Example 2: COC Patterning and Solvent Bonding

A homogeneous, trilaminate microfluidic device for DNA sequencing is formed from three layers of cyclo–olefin copolymer (COC) by hot-embossing (above the glass-transition temperature) 50 μm-deep features from a 50 μm-thick, negative-tone dry-resist pattern on a 200 μm-thick PET backing sheet into a middle layer of 130 μm-thick COC. An upper layer of COC is solvent-bonded to the middle layer by pretreating the bonding surface of the upper COC film with a 1:12 mixture of hexadecane in isopropyl alcohol (IPA), removing the excess liquid, allowing the solvent mixture to dry while penetrating and plasticizing the COC surface, then warm-laminating (below the glass-transition temperature) the two layers together to form covered channels. After punching features through the two layers to access the channels, a lower layer of COC is treated with the solvent mixture in a similar manner and warm-laminated to the previously laminated middle layer to seal off one side of the access ports. A blade may be used to trim the tri-layer laminate to size, and fittings may be epoxied over the ports [378].

8.5.3.3 Example 3: LIGA Mold Removal

A 120 μm-thick layer of PMMA is cast and polymerized on a silicon wafer having a 500 Å deposited nickel seed layer on top of a 3.0 μm deposited oxide layer. The PMMA is exposed with an X-ray source using an X-ray mask, developed in a commercial developer, and plated with nickel from a nickel sulfamate plating bath. The PMMA mold is stripped in acetone, re-exposed briefly from the X-ray source without a mask, and redeveloped to remove residual PMMA. The nickel seed layer is removed in the open areas with a dilute solution of nitric acid and water (1:20) for 1 min. The sacrificial oxide layer is removed under narrower nickel features by etching in BHF etchant (5:1) for 15 min and the wafer with freestanding nickel actuator features is rinsed carefully in DI water [414, 439].

8.6 Anisotropic Silicon Etching and Silicon Etch Stops

Anisotropic etching is direction-dependent etching, stemming from crystalline characteristics of the material being etched or from induced anisotropies in the etch process itself. The effect has been studied extensively and used for a variety of MEMS devices including pressure sensors, accelerometers, angular rate sensors, microphones, microfluidic devices, inkjet nozzles, through-wafer vias, and cap wafers. Crystallographically dependent anisotropic etchants have etch rates that are dependent on the crystal orientation of the substrate or thin film. Isotropic etchants are blind to the crystallography and etch in all directions at approximately the same

rate, resulting in appreciable undercutting of a selective masking layer with a lateral distance close to the etched depth.

Anisotropic etches, with carefully aligned masking patterns, can result in minimal undercutting although the etches generally produce pronounced flanks. A single-crystal silicon substrate, with its diamond crystal lattice, provides certain planes that etch quickly and other planes that etch slowly in anisotropic etchants such as potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), ethylene-diamine pyrocatecol (EDP), ammonium hydroxide (NH_4OH), sodium hydroxide (NaOH), hydrazine (N_2H_4), and others. Surfaces with exposed {100} planes such as the topside or bottomside of a (100) wafer etch quickly in these etchants, whereas (111) sidewalls at 54.74° (the sidewalls are closer to the vertical than 45°) etch appreciably more slowly. For example, a large open-square feature in a hard mask on the wafer surface will result in a cavity with a square bottom and tapered sides whereas a small open feature result in a pointed, self-stopping inverted pyramidal cavity. Rectangular patterns produce rectangular cavity bottoms with tapered sidewalls or a v-groove trench for small geometries. Silicon wafers with (111) surfaces etch minimally and are not often used for anisotropic etching. Wafers with (110) and more exotic orientations allow trenches with nearly vertical sidewalls, however, they don't allow rectangular-bottomed cavities. Geometrical features such as exterior (concave) corners result in oddly faceted structures that may require specially configured undercutting features placed on the mask or etchant additives to achieve the desired etched shape with minimal loss of pattern fidelity. Deeply etched cavities may show pillowing effects where the anisotropic etchant etches slightly more quickly near the sides of the cavity than in the middle, resulting in a somewhat thicker center region.

The primary use of anisotropic etching is to form diaphragms, cavities, or trenches that may require significant removal of the substrate top or bottom. Etched structures such as diaphragms fabricated using a timed etch can be difficult to produce repeatedly, particularly when the final diaphragm thickness is a small fraction of the total wafer thickness. For example, a small 1% variation in the etch rate can result in a nearly 10% variation in the feature thickness when the target diaphragm thickness is 1/10 of the substrate thickness. Automatic etch stops that allow significant overetching to accommodate etch rate variations are often used to surmount this problem. Etch stops such as heavily boron-doped silicon layers or a buried oxide layer in a silicon-on-insulator (SOI) wafer are built in, and are more robust compared to electrochemical etch stops that require externally connected voltage supplies. Etch-resistant layers such as patterned oxide or silicon nitride are commonly used to transfer patterns into the substrate and to protect active devices and peripheral portions of each die during the etch sequence. Anisotropic wet etchants generally require elevated etch-bath temperatures with careful control over the etchant concentration and a watchful eye for etchant exhaustion. Although anisotropic etching remains prevalent for many devices, surface micromachining with thin-film sacrificial layers or dry etching of the substrate with high-speed deep reactive ion etchers (D-RIE) are used for many contemporary designs. The following sections

and tables provide more detailed information on etch rates for silicon with various anisotropic etchants, important types of passive and active etch stops, and a few examples.

8.6.1 Anisotropic Etching of Silicon

Anisotropic etching of silicon strongly depends upon wafer orientation and patterned features including shape, size, orientation, and corner positions. Figure 8.11 depicts several representative geometries, including a large square, a long rectangle, a small circle, and an annular square to illustrate typical cavity geometries that result in anisotropic etching of a (100) silicon wafer. Long rectangular features form trenches with elongated bottoms or self-terminating v-grooves for narrow features when aligned along a <110> direction. Features such as small squares, circles, and small mask defects tend to form self-limiting pyramidal pits. Features with exterior corners such as a square in a square result in undercutting of the internal corners as higher-order crystalline planes become exposed, each with its own chemistry-dependent etch rate that can be higher than the (100) etch rate. Area permitting, enlarged corner-compensation features can be placed on the exterior corners to produce the desired feature as the etch process reaches completion, although these approaches place additional sensitivity on the etch rate and etch time. Certain additives may also slow the etching of the higher-order planes and eliminate the need for corner compensation features. One may notice that rotational misalignment of the mask features can result in excessive sidewall undercutting. Manufactured orientation flats and notches can identify the crystal orientation to about 0.5° or so,

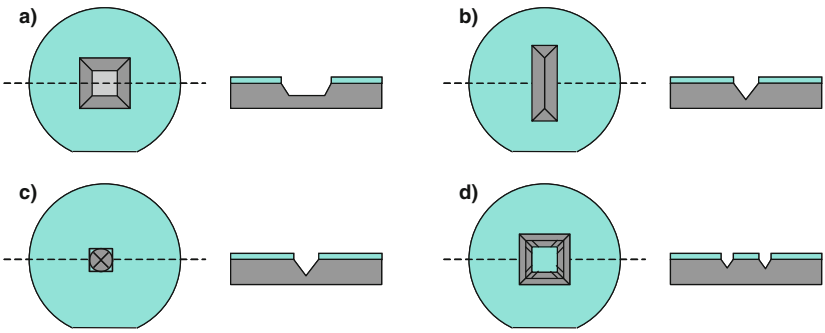

Fig. 8.11 Basic patterns in a masking layer on the surface of a (100) silicon wafer, followed by anisotropic etching into the substrate. (**a**) A large square pattern results in a smaller square-bottomed cavity with 54.736°($\cos^{-1}$(1/sqrt(3))) flanks. (**b**) A long rectangular feature results in a self-limiting trench or v-groove. (**c**) A small circular feature or mask defect results in a self-limiting pyramidal pit. (**d**) A patterned square within a square results in flanks along the outer walls and near the centers of the inner walls, whereas the corners of the inside square will preferentially undercut as higher-order planes become exposed

however, devices requiring more concise alignment may benefit from initially forming one or more long, narrow v-grooves on each wafer, then aligning to the groove edges. Devices with deep cavities may have significant projected-area loss due to the sloped sidewall flanks and the wafers may become quite fragile as they are etched, prompting special handling protocols and fixtures.

The etch rates of silicon with anisotropic etchants depend primarily upon the exposed crystal faces, etchant type, etchant temperature, and etchant concentration. To a lesser extent, the etch rate depends upon the amount of agitation or stirring, amount of exposed area, etchant exhaustion, substrate doping, and etchant additives. Approximate etch rates of several standard anisotropic etchants including KOH, TMAH, NH_4OH, EDP, and hydrazine are listed in Table 8.22. Ammonium hydroxide, although much slower than KOH or EDP etchants, is generally a standard cleanroom chemical and should be considered, particularly for etching shallower topside features. Sodium hydroxide etchants and others may present contamination concerns. Wafers etched in KOH, TMAH, or NH_4OH etchants can be cleaned sufficiently to allow continued processing in standard IC processing equipment. EDP etchants stop better than KOH on abrupt heavily doped p^{++} layers and have an appreciably higher etch selectivity to oxide, although they present some handling and discarding concerns. Most of the anisotropic silicon etchants will attack standard aluminum pads and traces, however, TMAH and NH_4OH etchants can be predoped with silicon powder or silicic acid to provide an anisotropic etchant with high resistance to standard aluminum metallurgy. Many excellent articles and summaries have been written on anisotropic etching of silicon, and the reader is encouraged to consult these publications [440–448] and books [78, 449–455] on the subject for more detailed information.

8.6.2 Heavily Doped Silicon Etch Stops

Silicon with high concentrations of substitutional elemental boron has a substantially slower etch rate in most anisotropic etchants and can be used as an effective etch stop, as illustrated in Fig. 8.12. Alkaline anisotropic etchants such as CsOH, KOH, LiOH, NaOH, and RbOH exhibit a strong reduction in the etch rate for high boron concentrations in silicon exceeding about $2 \times 10^{19}\text{cm}^{-3}$. Organic anisotropic etchants such as EDP and TMAH, ammonium-hydroxide etchants, and hydrazine etchants show similar effects. Boron concentrations in excess of $1 \times 10^{20}\text{cm}^{-3}$ can cause an etch rate reduction of 100 or more [473].

Highly doped p^{++} silicon can be formed in a silicon wafer using solid source diffusion of boron from a boron–nitride wafer at elevated temperatures, from gaseous deposition and diffusion of boron, from incorporation of high levels of boron dopant during epitaxial silicon growth, during crystal pulling of silicon from a melt with a high concentration of boron, or from a high dosage of ion-implanted boron. The heavily boron-doped silicon is under high tensile stress that may result in the formation of slip planes visible to the eye as plaid-type patterns, although germanium may be codoped with the boron to provide strain compensation and reduce slippage.

Table 8.22 Anisotropic silicon etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si), (100)	varies	Aqueous alkali (CsOH, KOH, LiOH, NaOH, RbOH)	Less commonly used anisotropic etchants except for KOH
2	Silicon (Si), (100)	140	Ethylenediamine: pyrocatechol:H_2O 680 mL:120 g: 320 mL	110°C; EPW etchant; mask with Ag, Au, Cr, Cu, Si_3N_4, SiO_2, Ta; Etches Si(110) 83 Å/s; Si(111) 8 Å/s; Doesn't significantly etch Ge, SiO_2 (0.05 Å/s); reduced etch rate for SiGe (>5% Ge); use quartz reflux system; sensitive to oxygen; reduced etch rate with high p-type doping; DI water rinse [442]
3	Silicon (Si), (100)	225	Ethylenediamine: pyrocatechol: pyrazine:H_2O 750 mL:240 g: 4.5 g:240 mL	115°C; EDP etchant, type F; less sensitive to oxygen; residues at lower temperatures; DI water rinse [456]
4	Silicon (Si), (100)	40	Ethylenediamine: pyrocatechol: pyrazine:H_2O 880 mL:140 g: 5.3 g:120 mL	75°C; EDP etchant, type S; Etches Si(110) 53 Å/s, Si(111) 0.6 Å/s, SiO_2 (0.001 Å/s); etches Si(100) 125 Å/s at 115°C, 90 Å/s at 105°C, 70 Å/s at 95°C, 13 Å/s at 50°C; Fewer residues at lower temperatures; low oxygen sensitivity; reduced etch rate with high p-type doping; stir continuously; DI water rinse [447, 456]
5	Silicon (Si), (100)	70	Ethylenediamine-based	100°C; Transene PSE-300 etchant; preferential <100> directions; negligible <111> plane; mask with SiO_2; etches Al, Cu; Doesn't significantly etch Ag, Au or Ta; use quartz flask with reflux condenser; initial dip in DHF recommended; DI water rinse [472]

Table 8.22 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
6	Silicon (Si), (100)	4.4	KOH:H_2O 250 g:1000 mL	20°C; KOH etchant (20 wt%); mask with Au/Cr, Si_3N_4, SiO_2; Etches Si(110) (6 Å/s), Si(111) (0.04 Å/s), SiO_2 (0.003 Å/s); Etch rate slows for high p-type dopant levels; rough surfaces; stir continuously; ultrasonic agitation helpful; DI water rinse [447]
7	Silicon (Si), (100)	240	KOH:H_2O 250 g:1000 mL	80°C; KOH etchant (20 wt%); mask with Si_3N_4, SiO_2 (for shallow etches); Etches Si(110) (370 Å/s), Si(111) (5 Å/s), SiO_2 (0.7 Å/s); slows for high p-type dopant levels; near highest Si etch rate with KOH concentration across temperature; rough surfaces; stir continuously; DI water rinse [447]
8	Silicon (Si), (100)	180	KOH:H_20 1:2 by weight (1 kg KOH pellets to 2 L water for 29% KOH by weight; pellets are 10–15% water)	80°C; KOH etchant (29 wt%); PR mask fails; mask with thermal SiO_2 (140:1), SiO_2(LTO) (110:1), Si_3N_4 (>1000:1), Si_3N_4(low-stress) (>1000:1), W, sandwich of SiO_2(PECVD) and Si_3N_4, Au on Cr adhesion layer; Etches Al (2000 Å/s), AlSi(2%) (fast), Al_2O_3 (130–400 Å/s), Cr (0.7 Å/s), Ge(poly) (high), Nb (0.5 Å/s), Pyrex (2 Å/s), quartz (1 Å/s), Si(poly) (110–160 Å/s), Si_3N_4(PECVD) (0.1 Å/s), SiO_2 (1.3 Å/s), SiO_2(LTO) (1.5 Å/s), SiO_2(PECVD) (1–2 Å/s), SiO_2(PSG) (6 Å/s), Ta (0.5 Å/s), Ti (softens), TiW (50 Å/s), Va (2 Å/s); Doesn't significantly etch Ag, Au, Cu, Mo, Ni, Pd, Pt, sapphire, Si_3N_4, W; dip wafers in DHF etchant prior to nitride mask deposition to remove native oxide and reduce undercutting; heat and stir or pump continuously in PFA tank with recirculating pump to reduce stratification; add IPA to improve uniformity [447]; stops on p^{++} silicon; DI water rinse [27, 28]

Table 8.22 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
9	Silicon (Si), (100)	3–510	KOH:H_2O 665 g:1000 mL	20–100°C; KOH etchant (40 wt%); mask with Si_3N_4, SiO_2 (for shallow etches); Etches Si(100) 3 Å/s at 20°C, 15 Å/s at 40°C, 55 Å/s at 60°C, 175 Å/s at 80°C, 510 Å/s at 100°C; Etches Si(110) 5 Å/s at 20°C, 22 Å/s at 40°C, 83 Å/s at 60°C, 275 Å/s at 80°C, 790 Å/s at 100°C; Etches SiO_2 0.003 Å/s at 20°C, 0.03 Å/s at 40°C, 0.2 Å/s at 60°C, 1.1 Å/s at 80°C, 5 Å/s at 100°C; Near highest SiO_2 etch rate with KOH concentration; slows for high p-type dopant levels; smoother surfaces; stir continuously; DI water rinse [447]
10	Silicon (Si), (100)	2.5–480	KOH:IPA:H_2O 250 g:200 mL:800 mL	20–100°C; KOH etchant (~20 wt%); mask with Si_3N_4, SiO_2 (for shallow etches); Etches Si(100) 2.5 Å/s at 20°C, 12 Å/s at 40°C, 47 Å/s at 60°C, 160 Å/s at 80°C, 480 Å/s at 100°C; Etches Si(110) 1.3 Å/s at 20°C, 5.5 Å/s at 40°C, 20 Å/s at 60°C, 63 Å/s at 80°C, 175 Å/s at 100°C; Etches SiO_2 0.002 Å/s at 20°C, 0.02 Å/s at 40°C, 0.1 Å/s at 60°C, 0.7 Å/s at 80°C, 3.3 Å/s at 100°C; Smoother surfaces; lower (100) and much lower (110) etch rates with IPA; reduced (100) to (111) selectivity; reduces undercutting of exterior corners; DI water rinse [447]
11	Silicon (Si), (100)	175	KOH:tert-butanol: H_2O 250 g:150 mL: 850 mL	80°C; KOH etchant (~23 wt%) (5 M) before addition of alcohol; excess alcohol may float on surface; minimal exterior corner undercutting; small hillocks; DI water rinse [457]

Table 8.22 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
12	Silicon (Si), (100)	330	N_2H_4:H_2O 1:1	100°C; hydrazine etchant (1:1); mask with SiO_2, Si_3N_4; Etches Al, Cu, polyimide, PR, Si(110) 150 Å/s, Si(111) 20 Å/s, Zn; Doesn't significantly etch Ag, Au, Ta, Ti; Smoother surfaces with increasing hydrazine concentration; reduced Si etch rate with high p-type doping; use reflux reactor; be cautious of fumes; sensitive to oxygen; dip in DHF etchant (20:1) for 20 s prior to etch; DI water rinse [445, 458, 459]
13	Silicon (Si), (100)	65	NH_4OH(29%):H_2O 1:6	75°C; ammonium hydroxide etchant (3.7 wt%); mask with Si_3N_4, SiO_2; 3:1 selectivity over (110) planes; 25:1 selectivity over (111) planes; 8000:1 selectivity over SiO_2; selectivity >8400:1 over Si_3N_4; rate slows with very high dopant concentrations; 8000:1 selectivity over 1.3×10^{20} cm^{-3} boron-doped silicon; etches Al (40 Å/s); mix fresh; agitate to reduce hillocks and surface roughness; dip first into DHF etchant; DI water rinse [460]
14	Silicon (Si), (100)	80	NH_4OH(29%):H_2O 1:2	75°C; ammonium hydroxide etchant (9 wt%); highest etch rate versus NH_4OH concentration; forms hillocks; agitate to reduce surface roughness; see remarks for 3.7 wt% etchant; etches Si (45 Å/s) at 1 wt%; DI water rinse [460]
15	Silicon (Si), (100)	200	NH_4OH(29%): H_2O_2(30%):H_2O 1000:3:2000	80°C; ammonium hydroxide etchant (2.65 M); minimal hillocks and smoother surfaces; etches slightly Si_3N_4 (<0.01 Å/s), SiO_2 (<0.01 Å/s), SiO_2(LTO) (0.03 Å/s); doesn't significantly etch Al (with at least 0.13 g Si added per liter), Au, Cr, Ta, Ti; illuminate p-type samples for smoother surfaces; see remarks for 3.7 wt% etchant; DI water rinse [461]
16	Silicon (Si), (100)	65	NH_4OH(29%):Si: H_2O 140 mL:0.1 g: 860 mL	75°C; ammonium hydroxide etchant (3.7 wt%) plus dissolved Si; doesn't significantly etch aluminum with prior dissolution of at least 0.1 g of silicon per liter of etchant; see remarks for 3.7 wt% etchant without additive; DI water rinse [460]

Table 8.22 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
17	Silicon (Si), (100)	105	TMAH (2 wt% in H_2O)	80°C; TMAH etchant (2 wt%); mask with SiO_2, Si_3N_4; etches Si(111) 2 Å/s; rough surfaces and hillocks; near highest (100):(111) selectivity; add ~5 g Si to reduce etch rate of Al; DI water rinse [462]
18	Silicon (Si), (100)	185	TMAH (4 wt% in H_2O)	90°C; TMAH etchant (4 wt%); mask with SiO_2, Si_3N_4; etches SiO_2(0.06 Å/s); rough surfaces; near peak in (100) etch rate with TMAH concentration; p-type Si etches slightly slower; DI water rinse [463]
19	Silicon (Si), (100)	100	TMAH (20 wt% in H_2O)	80°C; TMAH etchant (20 wt%); etches Si(110) 185 Å/s, Si(111) 2.8 Å/s; moderately rough surface; DI water rinse [464]
20	Silicon (Si), (100)	165	TMAH (22 wt% in H_2O)	90°C; TMAH etchant (22 wt%); mask with SiO_2, Si_3N_4; relatively smooth surfaces; etches Al (160 Å/s), Si(110) (240 Å/s), Si(111) (8 Å/s), SiO_2 (0.03 Å/s); etch rate reduces with high p-type doping; DI water rinse [465]
21	Silicon (Si), (100)	75	TMAH (25 wt% in H_2O)	80°C; TMAH etchant (25 wt%); mask with SiO_2, Si_3N_4; smoother surfaces; DI water rinse [466]
22	Silicon (Si), (100)	130	TMAH (25 wt% in H_2O)	90°C; TMAH etchant (25 wt%); etches Si(110) 250 Å/s, Si(111) 4 Å/s; smoother surface; DI water rinse [464, 467]
23	Silicon (Si), (100)	73	TMAH (10 wt%) and IPA (30 wt%) in H_2O	80°C; TMAH etchant (10 wt%) etchant with IPA; mask with SiO_2, Si_3N_4; smooth surfaces; DI water rinse [466]
24	Silicon (Si), (100)	72	TMAH (20 wt%) and IPA (10 wt%) in H_2O	80°C; TMAH etchant (20 wt%) with IPA; mask with SiO_2, Si_3N_4; smooth surfaces; similar etch rates for higher-order planes; DI water rinse [466, 468]
25	Silicon (Si), (100)	165	TMAH (22 wt% in H_2O):Si 1000 mL:75 g	90°C; TMAH etchant (22 wt%) predoped with Si; mask with SiO_2, Si_3N_4; relatively smooth surfaces; etches slightly Al (0.05 Å/s), SiO_2 (0.03 Å/s); DI water rinse [465]

Table 8.22 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
26	Silicon (Si), (100)	70	TMAH (25 wt% in H_2O):Silicic acid 1000 mL:250 g	80°C; TMAH etchant (25 wt%) with silicic acid; mask with SiO_2, Si_3N_4; etches AlSi (1%) (0.08 Å/s) (50 Å/s without additive), Si(111) 8 Å/s, SiO_2 (0.03 Å/s), Si_3N_4 (0.006 Å/s); dip in DHF etchant (100:1) for 60 s prior; can use 120 g of dissolved silicon instead of silicic acid; etch rate, surface smoothness and (100):(111) selectivity improves with addition of 5 g pyrocatechol per liter; DI water rinse [469]
27	Silicon (Si), (100)	100	TMAH (25 wt% in H_2O):Surfactant 1000 mL:5 g	90°C; TMAH etchant (25 wt%) with surfactant; etches Si(110) (17 Å/s), Si(111) (1.7 Å/s); smooth surfaces; surfactant is NCW-601A from Wako, contains 30 wt% polyoxyethylene alkyl phenyl ether; decreases (110) etch rate dramatically; replicates exterior corners fairly well; DI water rinse [470, 471]
28	Silicon (Si), (110)	1400	Alkali-based	100°C; Transene PSE-200 etchant; preferential <110> directions; negligible <111> plane; mask with SiO_2; Doesn't significantly etch Ag, Au orTa; use flask with reflux condenser; initial dip in DHF etchant recommended; DI water rinse [472]

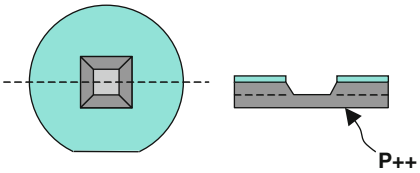

Fig. 8.12 A silicon wafer with a heavily doped boron etch stop causes the etch rate to reduce appreciably when the p^{++} layer is exposed to the etchant

Doped polysilicon films have been shown in some cases to provide an effective etch stop. Phosphorus-doped silicon shows a much smaller effect in these etchants, if at all. Table 8.23 lists typical etch rate reduction ratios for heavily doped silicon. Etch rate reductions at particular fractions and dopant levels of interest are presented. The etch rate reduction for the doped layer is the inverse of the selectivity for the etched material relative to the etch stop layer. Although the electrically active dopant level is one of the major factors in etch rate reduction, etchant type, concentration, and temperature are also important considerations.

8.6.3 Lightly Doped Silicon and Silicon–Germanium Etch Stops

Lightly doped silicon can serve as an etch stop for heavily doped silicon using particular regions of the HF–nitric–acetic acid system. Although isotropic, the etchant can effectively stop on lightly doped n-type or p-type silicon after etching a heavily doped p^+ or n^+ silicon layer. Etch stops based on high concentrations of germanium in silicon are also included here, inasmuch as the etch stop material can be lightly doped either n-type or p-type independent of the germanium level. Further remarks are found in Table 8.24.

8.6.4 Ion-Implanted Silicon Etch Stops

Ion implantation is commonly used to locally dope silicon, and heavy dosages of an implanted species can form adequately doped silicon or a silicon compound that serves as an effective etch stop for some silicon isotropic and anisotropic etchants. For example, high dosages of boron ($> 5 \times 10^{15}\,cm^2$) implanted into silicon or polysilicon and annealed can serve as an effective etch stop. The peak concentrations can be determined and etch rate ratios estimated from the highly doped boron (p^{++}) etch stop performance for various etchants (see Table 8.23). Alternatively, etch stops have been formed in silicon substrates by ion implantation of oxygen, nitrogen, or carbon, then annealed to form silicon dioxide, silicon nitride, and silicon carbide that have high selectivity to the majority of silicon etchants. Some examples are listed in Table 8.25. Although the depth of the implanted species is limited, the thickness above the implanted region can be augmented with an additional deposition of epitaxial silicon, provided that excessive dopant diffusion does not occur

Table 8.23 Heavily doped silicon etch stops and processes

	Material	Etch rate reduction	Etchant	Remarks and references
1	Silicon (Si), (100)	varies	Aqueous alkali (CsOH, KOH, LiOH, NaOH, RbOH)	Similar etch stop effects as KOH etchant [448]
2	Silicon (Si), (100)		Ethylenediamine: pyrocatechol: pyrazine:H_2O 1000 mL:160 g: 6 g:133 mL	49°C; EDP etchant, type S; p-type dopant (boron); epi-deposited samples; similar behavior for Si(110); selectivity decreases slightly with increasing etchant temperature to 110°C; similar behavior for EPW (non-catalyzed) etchant [447, 448, 456]
	<1E19 cm^{-3} (p)	1.0		
	1.7E19 cm^{-3} (p)	0.8		
	3.0E19 cm^{-3} (p)	0.5		
	4.7E19 cm^{-3} (p)	0.1		
	9.0E19 cm^{-3} (p)	0.01		
	1.0E20 cm^{-3} (p)	0.006		
3	Silicon (Si), (100)		Ethylenediamine: pyrocatechol: pyrazine:H_2O 17 mL:3 g: 0.016 g:8 mL	110°C; EDP etchant; p-type dopant; boron diffusion-doped samples; minimal effect on etch rate ratio of varying pyrazine concentration and oxygen content in etchant [474]
	<1E19 cm^{-3} (p)	1.0		
	2.0E19 cm^{-3} (p)	0.8		
	2.5E19 cm^{-3} (p)	0.5		
	4.5E19 cm^{-3} (p)	0.1		
	8.0E19 cm^{-3} (p)	0.01		
	1.0E20 cm^{-3} (p)	0.003		
	1.5E20 cm^{-3} (p)	0.0006		
4	Silicon (Si), (100)		KOH:H_2O 315 g:1000 mL	60°C; KOH etchant (24 wt%); p-type dopant; similar behavior for Si(110); selectivity decreases with increasing KOH concentration [448]
	<8E18 cm^{-3} (p)	1.0		
	1.5E19 cm^{-3} (p)	0.8		
	3.3E19 cm^{-3} (p)	0.5		
	8.0E19 cm^{-3} (p)	0.1		
	1.0E20 cm^{-3} (p)	0.06		
	1.5E20 cm^{-3} (p)	0.02		

Table 8.23 (continued)

	Material	Etch rate reduction	Etchant	Remarks and references
5	Silicon (Si), (100)		$KOH:H_2O$	21°C; KOH etchant (10 wt%); n-type dopant; modest reduction in etch rate with high P concentration [448]
	<8E18 cm^{-3} (n)	1.0	110 g:1000 mL	
	1.5E19 cm^{-3} (n)	0.8		
	6.0E19 cm^{-3} (n)	0.5		
	4.0E20 cm^{-3} (n)	0.2		
6	Silicon (Si), (100)		$N_2H_4:H_2O$	118°C; 50:50 hydrazine etchant; p-type dopant; boron solid-source diffused samples; etch rates become extremely slow above this concentration [458]
	>1.5E20 cm^{-3} (p)	slow	1:1	
7	Silicon (Si), (100)		$NH_4OH(29\%):H_2O$	75°C; 3.7 wt% NH_4OH etchant; p-type dopant; epi-deposited samples [460]
	1.3E20 cm^{-3} (p)	0.00013	1:6	
8	Silicon (Si), (100)		TMAH (25 wt% in H_2O)	80°C; TMAH etchant (25 wt%); p-dopant; boron implanted and gas-phase deposited; selectivity increases with decreasing etchant temperature; minor change in selectivity with etchant concentration [475]
	<4E18 cm^{-3} (p)	1.0		
	2.0E19 cm^{-3} (p)	0.8		
	7.0E19 cm^{-3} (p)	0.5		
	1.0E20 cm^{-3} (p)	0.3		
	2.0E20 cm^{-3} (p)	0.1		
	2.5E20 cm^{-3} (p)	0.025		
9	Silicon (Si), poly		TMAH (22 wt% in H_2O)	90°C; TMAH etchant (22 wt%); p-dopant; boron implanted at 30 keV into 2000 Å thick LPCVD polysilicon through 2000 Å silicon nitride layer, then annealed at 900°C for 30 min; etch rates are lateral through etch hole in upper nitride layer; selectivity increases with decreasing TMAH concentration; dissolve silicon to reduce etch rate of Al [465]
	<2E18 cm^{-3} (p)	1.0		
	4.0E18 cm^{-3} (p)	0.8		
	2.0E19 cm^{-3} (p)	0.5		
	1.5E20 cm^{-3} (p)	0.1		
	4.0E20 cm^{-3} (p)	0.01		

Table 8.24 Lightly doped silicon and silicon–germanium etch stops

	Material	Etch rate reduction	Etchant	Remarks and references
1	Silicon (Si), (100) >4E18 cm^{-3} (n) <1E17 cm^{-3} (n)	 1.0 <0.01	HF(49%): HNO_3 (70%):Acetic 1:3:8	22°C; HNA etchant; mask with Si_3N_4 or thick SiO_2; etches heavily doped silicon (<0.01Ω cm) 100–500 Å/s, SiO_2(5 Å/s); sensitive to agitation and defects in lightly doped material (>0.068 Ω cm); DI water rinse [62, 444, 446, 449]
2	Silicon (Si), (100) >9E18 cm^{-3} (p) <5E17 cm^{-3} (p)	 1.0 <0.01	HF(49%): HNO_3(70%):Acetic 1:3:8	22°C; HNA etchant; see remarks for n-type substrates with same etchant; DI water rinse [62, 444, 446, 449]
3	Si–Ge (SiGe) <4E20 cm^{-3} (Ge) 1.0E21 cm^{-3} (Ge) 3.0E21 cm^{-3} (Ge) 8.0E21 cm^{-3} (Ge)	 1.0 0.8 0.5 0.2	Ethylenediamine: pyrocatechol: pyrazine:H_2O 1000 mL:160 g: 6 g:133 mL	79°C; EDP etchant, type S; no dopant; modest reduction in etch rate with high Ge concentration [448]
4	Si–Ge (SiGe) 1.5E22 cm^{-3} (Ge)	 0.0015	EDP	95°C; $Si_{0.7}Ge_{0.3}$; etches Si (no Ge) 180 Å/s [476]
5	Si–Ge (SiGe) <4E20 cm^{-3} (Ge) 1.5E21 cm^{-3} (Ge) 4.0E21 cm^{-3} (Ge)	 1.0 0.8 0.5	KOH:H_2O 515 g:1000 mL	60°C; KOH etchant (34 wt%); no dopant; slight reduction in etch rate with moderate Ge concentration; Ge codoped with boron for strain compensation (e.g., 1×10^{20} cm^{-3} and 1×10^{21} cm^{-3} Ge) provides reduced etch rates similar to non-Ge samples [448]
6	Si–Ge (SiGe) <4E20 cm^{-3} (Ge) 5.0E21 cm^{-3} (Ge) 7.0E21 cm^{-3} (Ge) 1.0E22 cm^{-3} (Ge) 1.5E22 cm^{-3} (Ge)	 1.0 0.1 0.05 0.01 0.005	KOH:H_2O 515 g:1000 mL	60°C; KOH etchant (34 wt%); no boron dopant; high reduction in etch rate with Ge concentration 17–34%; etches Si (no Ge) at 51 Å/s [476]
7	Si–Ge (SiGe) 1.5E22 cm^{-3} (Ge)	 0.0008	KOH:H_2O 130 g:1000 mL	85°C; KOH etchant (11.3 wt%); $Si_{0.7}Ge_{0.3}$; etches Si (no Ge) 170 Å/s [476]

Table 8.24 (continued)

	Material	Etch rate reduction	Etchant	Remarks and references
8	Si–Ge (SiGe) 1.5E22 cm^{-3} (Ge)	0.05	KOH:H_2O 110 g:1000 mL	Room temperature; KOH etchant (10 wt%); $Si_{0.7}Ge_{0.3}$; etches Si (no Ge) 5 Å/s; etch SiGe in HF:H_2O_2:Acetic 1:2:3 etchant at 17 Å/s at room temperature with 1000:1 selectivity to Si [84]
9	Si–Ge (SiGe) 1.5E22 cm^{-3} (Ge)	0.004	TMAH(2 wt% in H_2O)	85°C; TMAH etchant (2 wt%); $Si_{0.7}Ge_{0.3}$; etches Si (no Ge) 180 Å/s; reduced selectivity and slower Si etch rate with 25 wt% TMAH [476]

Table 8.25 Ion-implanted silicon etch stops and processes

	Material	Etch rate reduction	Etchant	Remarks and references
1	Silicon (Si), (100), implanted boron (B)		EDP, KOH, N_2H_4, NH_4OH, TMAH	Implanted boron etch stop; see Table 8.23 [475, 477]
2	Silicon (Si), (100), implanted oxygen (O)		EDP, KOH(33 wt%), KOH-IPA	Implanted oxygen etch stop (SiO_2); implanted O^+ with heated substrate (550°C plus self-heating); 1.1×10^{18} cm^{-2} dosage at 100 keV for 60-min etch stop in EDP; 1.2×10^{18} cm^{-2} dosage for 60-min etch stop in KOH-IPA; no postimplant anneal [478]
3	Silicon (Si), (100), implanted nitrogen (N)		EDP, KOH(33 wt%), KOH-IPA	Implanted nitrogen etch stop (Si_3N_4); implanted N^+ with heated substrate (550°C plus self-heating); 1.0×10^{18} cm^{-2} dosage at 200 keV for 60-min etch stop in EDP or KOH-IPA; 1.1×10^{18} cm^{-2} dosage for 60-min etch stop in KOH etchant (33 wt%); no postimplant anneal; high-temperature anneal needed for additional epi depositions; etch-rate reductions seen at 5.0×10^{16} cm^{-2} N at 120 keV with or without annealing [478, 479]
4	Silicon (Si), (100) 3.5E20 cm^{-3} (C) 5.0E20 cm^{-3} (C) 1.5E21 cm^{-3} (C) 4.0E21 cm^{-3} (C)	0.02 0.01 0.001 0.0002	Ethylenediamine: pyrocatechol: pyrazine:H_2O 1000 mL:160 g: 6 g:133 mL	85°C; EDP etchant, type S; implanted carbon etch stop (SiC); implanted C^{12} with nonheated substrate; 35 keV; 850°C postimplant anneal [480]
5	Silicon (Si), (100) 3.0E20 cm^{-3} (C) 2.5E21 cm^{-3} (C) 4.5E21 cm^{-3} (C) 8.0E21 cm^{-3} (C) 2.0E22 cm^{-3} (C)	0.5 0.1 0.01 0.001 0.0001	KOH:H_2O 800 g:1000 mL	85°C; KOH etchant (45 wt%); implanted carbon etch stop (SiC); implanted C^{12} with nonheated substrate; 35 keV; 850°C postimplant anneal [480]

during the elevated temperatures associated with epi growth and that a satisfactory seed layer for the epi deposition exists at the implanted surface.

8.6.5 Electrochemical Etching and Electrochemical Etch Stops

Although applicable to nearly any metal or semiconductor material, electrochemical etching techniques generally require external voltage supplies, monitors, reference electrodes, and one or more electrical connections to each wafer, which diminish their utility in favor of simple immersion in selective wet chemical etchants or use of dry-etching systems. However, in situations where a well-defined etch stop is needed between n-doped and p-doped material, the additional efforts may be worthwhile. An example is bulk-micromachined pressure sensors that use a low-doped n-type diaphragm with p-type piezoresistors.

Electrochemical etch stops can provide suitable stopping capability for wafers with an internal p–n junction, such as a lightly doped epitaxially deposited n-type epi layer on top of a p-type substrate. The doping requirements for the p^- and n^- sides are much reduced from heavy p^{++} etch stops and allows for piezoresistors and active devices. Accommodations must be made to provide good electrical contact to the internal junction, while protecting the connections from inadvertent exposure to the etchant. When etching at an elevated temperature, reverse leakage currents increase and can lessen the voltage drop across the diode. High current levels present during portions of the etch may cause variations in voltage across the wafer and prevent the etch from stopping near the junction, requiring metal backing plates, metallized pathways, or regions on the wafer with very low sheet resistance to circumvent.

Two-, three-, four-, and zero-electrode configurations with intrinsic galvanic couples are possible for silicon etching. Two-electrode configurations require a voltage be applied across the n-epi and a reference electrode placed in the etchant as seen in Fig. 8.13a, although this approach is intolerant of leaky junctions and may fail to etch or fail to stop the etch where desired. The three-electrode configuration uses a reference electrode such as a platinum sheet, mesh, or wire, in addition to connections to the n-epi and counterelectrode as seen in Fig. 8.13b. By setting a potentiostat so that the current through the reference electrode is zero, the interface potential between the reference electrode and the etchant is stable and less subject to variations in leakage currents or shorting in the sample, resulting in a more consistent etch stop. The four-electrode configuration requires an additional connection to the p-type substrate as seen in Fig. 8.13c and is more tolerant of substrate leakage, although it requires the most connections and external monitoring. As the etch nears completion, the current changes dramatically, bubble formation at the silicon surface or near the counter electrode stops, a smooth surface becomes visible, and the wafer can be withdrawn and rinsed. A zero-terminal configuration is illustrated in Fig. 8.13d. This configuration self-generates the required galvanic potentials by incorporating, for example, thin-film platinum on the front and/or back of a wafer with sufficient area to stop the etch as an internal p–n junction is reached. Internal

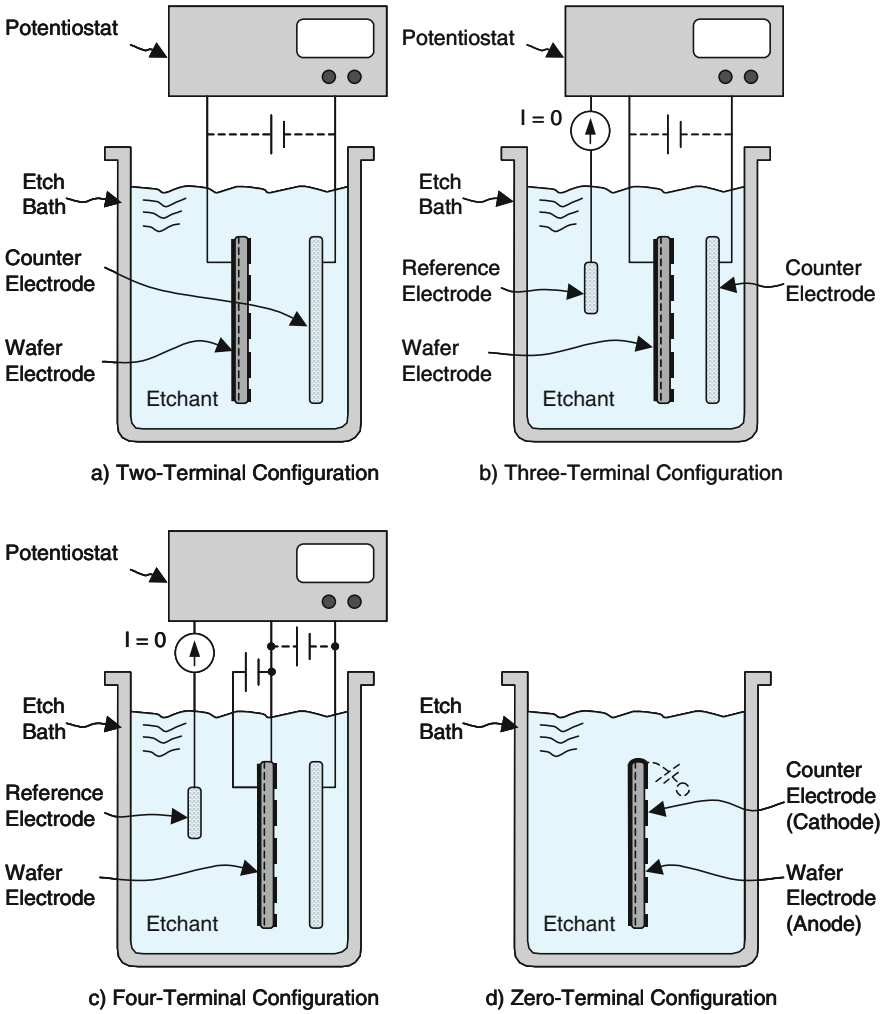

Fig. 8.13 Electrochemical etch stops require a predefined voltage across an internal p–n junction in a substrate. As a silicon wafer is etched and exposes a biased junction, the exposed n-type material is anodized and the etch rate slows appreciably. In a two-electrode configuration (**a**), one electrical connection is made to the wafer (anode or working electrode) and another to a counter-electrode (cathode) in the etchant, and connected to an external voltage supply and current monitor. A three-electrode configuration (**b**) adds a reference electrode near the working electrode, and the counter and reference electrodes are connected to a potentiostat to monitor the process. Voltage adjustments are made so that no current flows through the reference electrode. A four-electrode configuration (**c**) has a second connection to the wafer where it can set the potential on the substrate being etched in addition to the stop layer. A zero-terminal configuration (**d**) has a sizable platinum film on the wafer that serves as a galvanic cell to self-bias and passivate the n-type layer when it becomes exposed. Not shown are provisions for ohmic contact and protection for select portions of the wafer

ohmic connections and fixtures or passivation layers to protect portions of the wafer during etching are needed.

Judicious selection of applied voltages, current density, and etchant concentration can have a major impact on the electrochemically etched result, such as the production of an electropolished surface or porous silicon. As in anisotropic etching of silicon substrates with chemical etchants, the structures may become increasingly fragile as the silicon is removed. The etchants are generally anisotropic although the techniques work with certain isotropic etchants. The electrochemical etch stop generally applies to p-type substrates with an n-epi layer on top, however, a technique referred to as pulsed-potential anodization (PPA) allows the etching of n-substrates while stopping on a p-type layer [481]. Etch rates and etch stop ratios for various etchants and configurations are listed in Tables 8.26 and 8.27. The interested reader may consult some of the many excellent papers and books written on the subject [1, 2, 4, 78, 454].

Table 8.26 Electrochemical silicon etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si), (100) n^- substrate	4.6	KOH:H_2O 110 g:1000 mL	21°C; KOH etchant (10 wt%) (2 M); 2-terminal configuration; substrate etch rate before application of anodization potential: ~4.6 Å/s; substrate etch rate with anodization potential: ~0.009 Å/s (500:1); substrate set slightly higher than the passivation potential (–0.7 to –1.1 V with respect to (wrt) a standard calomel electrode(SCE)) where anodization current is minimum; etch ratio degrades to 100:1 at +5 V; etch rate degrades further to 30:1 with illumination [447, 482]
2	Silicon (Si), (100) p^- substrate	4.6	KOH:H_2O 110 g:1000 mL	21°C; KOH etchant (10 wt%) (2 M); 2-terminal configuration; substrate etch rate before application of anodization potential: ~4.6 Å/s; substrate etch rate with anodization potential: ~0.019 Å/s (250:1); substrate set slightly higher than the passivation potential (–0.7 to –0.9 V wrt SCE) where anodization current is minimum; etch ratio degrades to 9:1 at +5 V; illumination has little effect on etch rate ratio [447, 482]

8.6.6 Photoassisted Silicon Etching and Etch Stops

Photoassisted etching, also referred to as photoelectrochemical etching, allows the selective etching and nonetching of silicon, and depends upon doping, light intensity, and p–n regions within the silicon. The phenomenon is often observed

Table 8.27 Electrochemical etch stops and processes

	Material	Etch rate ratio	Etchant	Remarks and references
1	Silicon (Si), (100) p^- substrate (stops on n-diffusion)	3000:1	Ethylenediamine: pyrocatechol:H_2O 75 mL:12 g:24 mL	105–115°C; EDP etchant; 2-terminal configuration; Pt counterelectrode; +0.6 V applied to n-layer; etch rate of 210–290 Å/s prior to stopping on n-type layer; etch rate of passivated layer <0.1 Å/s after stopping [483]
2	Silicon (Si), (100) or (111) n^+ substrate (stops on n^- epi)		HF(49%):H_2O 1:9	Room temperature; DHF etchant (9:1); 2-terminal configuration; etches n^+ (111) at 550 Å/s; Pt counterelectrode; +6.0 V applied to $n^+ > 4 \times 10^{18}\,cm^{-3}$; $n^- < 2 \times 10^{16}\,cm^{-3}$; avoid illumination [484–486]
3	Silicon (Si), (100) p^- or p^+ substrate (stops on n^- implant)		HF(49%):H_2O 1:9	Room temperature; DHF etchant (9:1); 2-terminal configuration; etches p^- at 250 Å/s; +1.5 V applied ohmically to p^- substrate wrt Pt counterelectrode; $n^- <\sim 1 \times 10^{16}\,cm^{-3}$ [487]
4	Silicon (Si), (100) p^+ substrate (stops on n^- epi)		HF(49%): H_2SO_4(96%):H_2O 1:1:5	25–66°C; HF-sulfuric etchant; 2-terminal configuration; +0.5 V applied to n-epi wrt Pt counterelectrode; remove any brownish build-up with HF:HNO_3 (3:97) [488]
5	Silicon (Si), (100) p^- substrate (stops on n^- diffusion)		KOH:H_2O 250 g:1000 mL	75°C; KOH etchant (20 wt%); 2-terminal configuration; doping-selective etching (DSE); 1.9 V applied to n-type region wrt Pt counterelectrode in solution (between passivation potentials of n-type and p-type material); etches n-type material selectively; topside or bottom side etching; technique may apply to n^+ on n [489]
6	Silicon (Si), (100) p^- substrate (stops on n^- epi)	90:1	KOH:H_2O 665 g:1000 mL	60°C; KOH etchant (40 wt%); 3-terminal configuration; n-type diaphragms on p-type substrate; substrate etch rate before stop ~55 Å/s; diaphragm etch rate after stop ~0.6 Å/s; potentiostat connected to n-epi and set to –0.6 V or higher (more positive than the oxide formation potential for n-type Si) wrt SCE; p-substrate ideally floats to open circuit potential (OCP); SCE voltage set for 0 current through the SCE by adjusting the Pt counterelectrode voltage; current through counter electrode is ~0 mA while etching (for low-leakage diodes); current increases when etch stop occurs and diminishes after anodic passivation; sensitive to diode and parasitic leakages; avoid illumination [490, 491]

Table 8.27 (continued)

	Material	Etch rate ratio	Etchant	Remarks and references
7	Silicon (Si), (100) p^- substrate (stops on n^- diffusion or p^{++} or both)		$KOH:H_2O$ 1000 g:1000 mL	88°C; KOH etchant (50 wt%); 3-terminal configuration (no reference electrode); capacitive electrochemical etch stop (CECES); etches p-substrate 280 Å/s; +4.0 V for 3 ms then 0.0 V for 0.3 ms applied to n-region via 200 kΩ on-chip resistors wrt p^{++} substrate connections; Pt counterelectrode in solution also connected to resistors; timing parameters based on resistor parameters, etched area, and nonetched areas [492]
8	Silicon (Si), (100) n^- substrate (stops on p^- epi)		$KOH:H_2O$ 250 g:1000 mL	60°C; KOH etchant (20 wt%); 3-terminal configuration; pulsed-potential anodization (PPA); etches n-type regions selectively over p-type regions; apply +2 V for 1 s to p-type layer, then apply 0 V for ~30 s and repeat; modest reduction in etch rate from rate at open circuit potential; avoid illumination [481]
9	Silicon (Si), (100) p^- substrate (stops on inverted p^- substrate)		$KOH:H_2O$ 500 g:1000 mL	70°C; KOH etchant (30 wt%); 3-terminal configuration; metal-insulator-semiconductor (MIS) etch stop; homogenous p-type substrate with 1000 Å gate oxide; +1.2 V applied to substrate contacts wrt Pt counterelectrode in solution; +5 V gate voltage results in ~1 μm-thick features [493]
10	Silicon (Si), (100) p^- substrate (stops on n^- epi)	90:1	$KOH:H_2O$ 665 g:1000 mL	60°C; KOH etchant (40 wt%); 4-terminal configuration; n-type diaphragms on p-type substrate; substrate etch rate before stop ~55 Å/s; diaphragm etch rate after stop ~0.6 Å/s; potentiostat connected to p-substrate and set to –1.5 V (near open-circuit potential) wrt standard calomel electrode (SCE); n-epi set to +1.5 V wrt p-substrate; SCE voltage set for 0 current through the SCE by adjusting the Pt counterelectrode voltage; current through counter electrode is ~0 mA while etching (for low-leakage diodes); current increases when etch stop occurs and diminishes after anodic passivation; less sensitive to diode leakages than 3-terminal configuration [490, 494]
11	Silicon (Si), (100) p^- substrate (stops on n^- epi)	>380:1	$N_2H_4:H_2O$ 1:1	90°C; 50:50 hydrazine etchant; 2-terminal configuration; etches p-substrate at 530 Å/s; etches n-type layer after anodic passivation at <1.4 Å/s; Pt counterelectrode; n-type layer biased at +5.0 V wrt counterelectrode; 3000 Å oxide mask over Al pads; bubbling stops when etch is completed [495, 496]

Table 8.27 (continued)

	Material	Etch rate ratio	Etchant	Remarks and references
12	Silicon (Si), (100) p^- substrate (stops on n-epi)		TMAH(25 wt% in H_2O)	80°C; TMAH etchant (25 wt%); 0-terminal configuration; intrinsic galvanic cell (IGC) etch stop; Au (2000 Å) on Cr (600 Å) with sufficient area connected to n-epi generates internal biasing when immersed in solution [497–499]
13	Silicon (Si), (100) p^- substrate (stops on n-well diffusion)		TMAH(25 wt% in H_2O), with and without IPA	80°C; TMAH etchant (25 wt%) with 0 and 17% (by volume) IPA added; 3-terminal and 4-terminal configurations (–1.5 V on p-substrate and +1.0 V on n-bridges); Ag/AgCl reference electrode; Pt counterelectrode; reflux condenser; bubbling N_2; sealed wafer chuck; dip in DHF etchant prior to etching; etch in darkness; IPA has little effect [500]
14	Silicon (Si), (100) p^- substrate (stops on n^- Si)	varies	Aqueous alkali (CsOH, KOH, LiOH, NaOH, RbOH) and others	Results vary or are unknown [501]

while etching oxide with buffered hydrofluoric acid above heavily n-doped regions in silicon; oxide above p^+ regions will clear whereas oxide above the n^+ regions may not. Extinguishing incident light during the last portions of the etch can diminish or eliminate the effect [502]. Moderate levels of incident light on n-type material in HF solutions, for example, will cause anodization and etching without any substantial heating of the substrate. Broadband or narrowband light with energies above the bandgap may be applied to the etched side of the wafer, although the light can alternatively be applied to the opposite side of the wafer as generated carriers propagate through the wafer to the etch interface. In another configuration, internal p–n junctions are forward biased with the application of light as in a solar cell. Combined with judicious selection of the fraction of etched area and junction area, p-type portions in an n-type substrate are selectively etched or preferentially anodized and the process is stopped on the n-type material as the metallurgical junction is reached [503]. Autogenerated potentials from thin-film metallization on the wafer combined with external illumination allow connection-free etching of an n-type substrate while stopping on a diffused p-layer [504], as illustrated in Fig. 8.14. Although generally requiring no external electrical connections, electrical connections to the wafer and a potentiostat can provide the user with fuller control over the etch process. Use of light along with external electrical connections and voltage control allows the production of microporous (nanoporous), mesoporous, and macroporous silicon. Examples of photoassisted etching processes are found in Table 8.28. Photoassisted etch stops are found in Table 8.29. Further discussions and details may be found in the associated references and reviews [78].

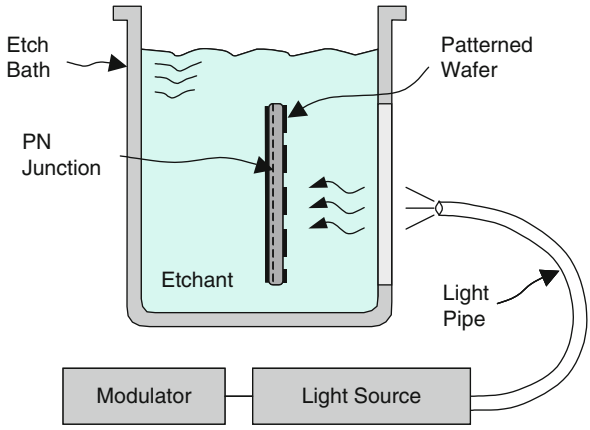

Fig. 8.14 Photoassisted etch stops use external light to generate a photovoltage across an internal p–n junction and slow down the etch rate as the junction is exposed by the etchant. If passivation around the wafer provides inadequate protection against the etchant, a fixture may be used

8.6.7 Thin-Film Etch Stops

Thin-film etch stops combine a deposited or otherwise formed etch-resistant layer with a selective etchant to allow partial removal of a substrate or an adjacent film and

Table 8.28 Photoassisted silicon etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si), (100) n^- substrate	150–200	HF(49%): H_2O 1:4	Room temperature; DHF etchant (4:1); 0-terminal configuration; photoassisted etching (nonthermal); n-type 3E-15 cm^{-3} substrate; 10 W/cm^2 optical power (UV laser) [505]
2	Silicon (Si), (100), 8–15 Ω cm	415	HF(49%): H_2O 2:3	Room temperature; DHF etchant (3:2); 2-terminal configuration; photo-induced preferential anodization; 500 mW/cm^2 HeNe laser source; Pt and Au counterelectrodes; 1500:1 selectivity enhancement over dark conditions (0.3 Å/s) [506]
3	Silicon (Si), (100), 2–6 Ω cm		HF(49%): H_2O 1:9	15°C; DHF etchant (9:1); 2-terminal configuration; photoassisted etching; macroporous silicon; +2 V applied to n^+ ion-implanted layer on wafer backside; Pt wire counterelectrode; added 0.1 mM of Triton X-100 surfactant; modulated light intensity produced modulated pore size with depth [507, 508]

stop automatically on the etch-stop layer. The thin film etches slowly or negligibly in the etchant, and can simultaneously serve as a passivation layer or a hard mask. The thin film can become free-standing, extremely fragile, and prone to buckling if not in tension as the substrate is etched, requiring careful handling during rinsing and subsequent handling steps.

Endpoints can be visibly detected if the etch stop material is transparent. Silicon dioxide and silicon nitride are transparent and have high selectivity to many of the anisotropic silicon etchants, although the oxide is generally under severe compression and may distort appreciably when etched free. Although some metals are sufficiently resistant to extended time in silicon etchants, the use of dielectric thin-film stops additionally provide electrical isolation for buried traces and active devices while protecting the devices during the etch. Double layers of thin-film etch stops can reduce the detrimental effects of defects such as pinholes. The etch-stop layer may be built in, such as a buried oxide layer in an SOI wafer. Thin-film etch stops generally allow multiple wafers to be chemically etched simultaneously in a batch format, as illustrated in Fig. 8.15. Table 8.30 presents some thin-film etch stops and their etch rates in some common anisotropic silicon etchants.

Table 8.29 Photoassisted etch stops and processes

	Material	Etch rate ratio	Etchant	Remarks and references
1	Silicon (Si), (100) p^- epi buried layer (stops on n^+ substrate and n^- surface features)		$HF(49\%):H_2O$ 1:4	Room temperature; DHF etchant (4:1); 0-terminal configuration; photo-induced preferential anodization (PIPA); forward-biased p–n junctions to generate photocurrent; n-type 1×10^{18} cm^{-3} substrate; p-type 1×10^{18} cm^{-3} buried layer; n-type 1×10^{15} cm^{-3} beams; 30 mW/cm^2 Xenon lamp; no metal electrodes; 10 Å/s lateral porous silicon formation rate; remove oxidized porous silicon layer with HF after 1000°C wet oxidation; 20 μm wide, 1 μm-thick beams formed [503]
2	Silicon (Si), (100) n^- substrate (stops on p^- diffusion)		$HF(49\%):H_2O$ 1:9	Room temperature; DHF etchant (9:1); 3-terminal configuration; photoassisted etching of n-regions (1×10^{15} cm^{-3}) around and below 3.3 μm-thick p-type diffused structures; +4.0 V wrt SCE applied to n-substrate via ohmic contact; p^- regions biased at –4.3 V wrt n-substrate; 2 W/cm^2 illumination; etch rate ~400 Å/s for lower bias (+1.5 V SCE); clear porous silicon layer with $HF:HNO_3$:Acetic 3:16:1 for 5 s or with 25 wt% KOH for 30 s at room temperature [509, 510]
3	Silicon (Si), (100) n^- substrate (stops on p^- epi or diffusion)		$KOH:H_2O$ 500 g:1000 mL	60–75°C; KOH etchant (30 wt%) (7 M); 0-terminal configuration; photovoltaic electrochemical etch stop (PHET); p-type diffusions (e.g., p-well); uses topside illumination and Pt film connected to n-regions for electrochemical cell; no electrical connections needed to the wafer; restrictions on etch-stop area [504]

8.6.8 Examples: Wet Chemical and Electrochemical Etch Stops

8.6.8.1 Example 1: Anisotropic Silicon Etching of an SOI Wafer

An 8000 Å silicon nitride layer and a 1.2 μm-thick thermal oxide on the backs and fronts of double-sided polished SOI wafers are patterned etched with large

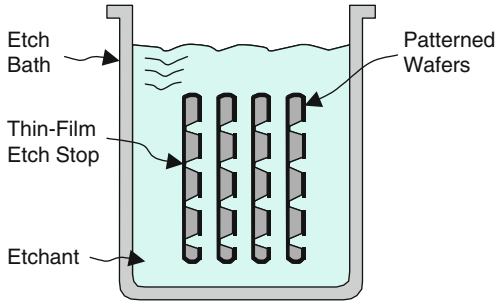

Fig. 8.15 Thin-film etch stops for anisotropic silicon etching use one or more etch-resistant layers on both sides of the wafer, with one side patterned. As the etch is completed, the etch-stop layer becomes free standing

squares on the bottom sides to expose 1–10 Ω cm n-type (100) silicon surfaces. A KOH-based etchant was selected for its high etching speed over a TMAH etchant. After a 10-s predip into DHF etchant (10:1), the wafers are inserted with a Teflon holder into a 30% KOH etchant at 90°C in a double-wall quartz etch bath to remove 500 μm of silicon at a rate of 135 μm/h, taking about $3\frac{3}{4}$ h. A reflux condenser is used on the etch flask to contain and condense evaporated water and etchant vapors. The etch stops automatically on the buried oxide, although the wafers are inspected visually at the estimated etch time to show nearly complete clearing and then reinserted for another 10 min of overetch. The wafers are rinsed in DI water for 10 min in a cascade-style rinse with a polypropylene tube to inject water carefully under the wafers, then blown dry with nitrogen. The remaining nitride is stripped off in hot phosphoric acid. The masking oxide and exposed portions of the buried oxide are subsequently removed in concentrated HF etchant (49%) for 2 min to expose tethered portions of a galvanically actuated micromirror. The wafers are carefully rinsed and dried, then diced between two sheets of dicing tape.

8.6.8.2 Example 2: Heavy Boron-Doped Etch Stop

A 2 μm-thick p-type epitaxial layer with a high boron concentration of 1.0×10^{20} cm^{-3} is grown epitaxially on a 1–10 Ω cm p-type (100) silicon wafer. A 1.5 μm-thick layer of low-temperature oxide is deposited on both sides of the wafer and patterned on the bottomside. The 525 μm-thick wafer is inserted into EDP type F etchant at 115°C for $6\frac{1}{2}$ h to remove exposed portions of the substrate and stop on the p^{++} epi layer. The oxide is stripped in a commercially available 6:1 buffered oxide etch for about 12 min to free up a heater and sense elements for a mass air flow sensor.

8.6.8.3 Example 3: Electrochemical Etch Stop

A CMOS wafer with a p-type substrate and active circuitry in 5 μm-deep n-wells has aluminum bond pads. Portions of the substrate around designated n-wells on each die have exposed silicon from a semicustom masking and etching step performed at the end of standard CMOS processing. The wafer is inserted into a special fixture that protects the sides and back of the wafer while allowing electrical connections

Table 8.30 Thin-film etch stops for anisotropic silicon etching

	Material	Etch rate selectivity	Etchant	Remarks and references
1	Aluminum (Al)	1:12	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
		3:2	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [460]
		Good	NH_4OH(doped)	75°C; 0.1 g/l Si added [460]
		1:1	TMAH(22 wt%)	90°C; etches Si(100) ~165 Å/s [465]
		3300:1	TMAH(doped)	90°C; 75 g/l Si added [465]
2	Chrome (Cr)	260:1	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
		Good	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [460]
3	Copper (Cu)	OK	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s; thickens [28]
4	Gold (Au)	Good	EDP(EPW)	110°C; etches Si(100) ~140 Å/s [442]
		Good	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s; Au/Cr [28]
		Good	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [460]
5	Molybdenum (Mo)	Good	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
6	Nickel (Ni)	Good	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
7	Niobium (Nb)	340:1	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
8	Palladium (Pd)	Good	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
9	Parylene (Parylene C)	2600:1	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
10	Photoresist (PR)	1:16	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
11	Platinum (Pt)	Good	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
12	Polyimide (PI)	OK	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s; thickens [28]
13	Silicides			Generally resistant to aqueous alkali etchants; see Table 8.20 [127]

Table 8.30 (continued)

	Material	Etch rate selectivity	Etchant	Remarks and references
14	Silicon, poly (Si-poly), boron doped at 4 $\times 10^{20}$ cm^{-3})	100:1	TMAH(22 wt%)	90°C; etches Si(100) ~165 Å/s [465]
15	Silicon–germanium (SiGe), (100)	650:1	EDP(EPW)	95°C; etches Si(100) ~180 Å/s [476]
		1200:1	KOH(11/3 wt%)	85°C; etches Si(100) ~165 Å/s [476]
		240:1	TMAH(2 wt%)	85°C; etches Si(100) ~180 Å/s [476]
		155:1	TMAH(25 wt%)	85°C; etches Si(100) ~70 Å/s [476]
16	Silicon dioxide (SiO_2), thermal	2500:1	EDP(EPW)	110°C; etches Si(100) ~140 Å/s [442]
		140:1	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
		9600:1	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [461]
		5000:1	TMAH(22 wt%)	90°C; etches Si(100) ~165 Å/s [465]
17	Silicon dioxide (SiO_2), LTO	OK	EDP(EPW)	110°C; etches Si(100) ~140 Å/s [442]
		115:1	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
		8300:1	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [461]
18	Silicon nitride (Si_3N_4)	Good	EDP(EPW)	110°C; etches Si(100) ~140 Å/s [442]
		Good	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
		21000:1	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [461]
		Good	TMAH(22 wt%)	90°C; etches Si(100) ~165 Å/s [465]
19	Silver (Ag)	OK	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s; thickens [28]
20	Tantalum (Ta)	Good	EDP(EPW)	110°C; etches Si(100) ~140 Å/s [442]
		390:1	KOH(30 wt%)	80°C; etches Si(100) ~180 Å/s [28]
		Good	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [461]
21	Titanium (Ti)	OK	KOH	80°C; etches Si(100) ~180 Å/s; softens [28]
		Good	NH_4OH(3.7 wt%)	75°C; etches Si(100) ~65 Å/s [461]

Table 8.30 (continued)

	Material	Etch rate selectivity	Etchant	Remarks and references
22	Titanium-tungsten (TiW)	7:2	KOH(30 wt%)	80°C; etches Si(100) ∼180 Å/s [28]
23	Tungsten (W)	Good	KOH(30 wt%)	80°C; etches Si(100) ∼180 Å/s [28]
24	Vanadium (V)	90:1	KOH(30 wt%)	80°C; etches Si(100) ∼180 Å/s [28]

to bond pads that are internally connected to the substrate and to the designated n-wells from the exposed front side. A 1-L solution of 5% TMAH etchant in water is freshly mixed with 38 g of silicic acid to reduce aluminum attack and 7 g of ammonium persulfate (AP) to decrease surface roughness, then heated to 80°C in a quartz etch bath with a quartz reflux condenser.

Using Teflon-coated wire and a four-terminal electrochemical etch configuration, the p-substrate is biased near the open-circuit potential at –1.5 V with respect to an Ag/AgCl reference electrode in the solution and the designated n-wells are reverse biased at +0.7 V with respect to the p-substrate. The fixture is immersed into the etching solution, and etched for 1¾ h (160 Å/s) to produce a self-limiting 100 μm-deep v-grooved cavity with (111)-oriented flanks while undercutting the 100 μm by 50 μm designated n-wells. The oxide etches a total of 120 Å (0.019 Å/s) and the aluminum etches a total of 80 Å (0.0125 Å/s). The wafer is carefully rinsed and dried, and then diced with dicing tape on both sides of the wafer. Prior to wirebonding, the dicing tape above each die is carefully peeled back to avoid breaking the thermally isolated structures [511, 512].

8.7 Sacrificial Layer Etching

Sacrificial layers, structural layers, and a highly selective wet etch combine to form freestanding microstructures for a wide variety of devices including cantilevered beams, resonators, pressure sensors, accelerometers, gyroscopes, flow sensors, IR detectors, inkjet heads, microphones, optical switches, microdisplays, microfluidic devices, microtips, electrical probes, bio-MEMS and RF-MEMS devices, micro fuel cells, and energy harvesting devices. Sacrificial layer etching is the selective removal of thin films or portions of the substrate under structural layers that allows the structural layers to become freestanding, attached to the substrate at only predefined locations. Cantilevered beams, for example, can be selectively undercut to make the beam freestanding at all but the base. Doubly supported beams are attached at each of two ends and freestanding elsewhere, and freestanding membranes, plates and shells are attached to the substrate at one or more sides. Figure 8.16 shows a cantilevered geometry where the freestanding structure is undercut with a timed etch and another where the sacrificial etching is self-stopping. The self-stopping process architecture allows structures with different undercut lengths to be fabricated on the same wafer at the same time, and provides the process engineer with a robust etching procedure.

Lateral etching with a liquid or gaseous etchant allows the sacrificial layer to be removed while leaving the structural layer intact. Extensive lateral etching is generally difficult to achieve with a dry plasma or RIE etch, whereas selective liquid etchants with their relatively small mean free path can enter very narrow and tortuous paths to efficiently remove sacrificial layers.

Structural layers are generally several micrometers thick and sacrificial layers can be several hundred angstroms to a hundred microns or more thick. The etchant must

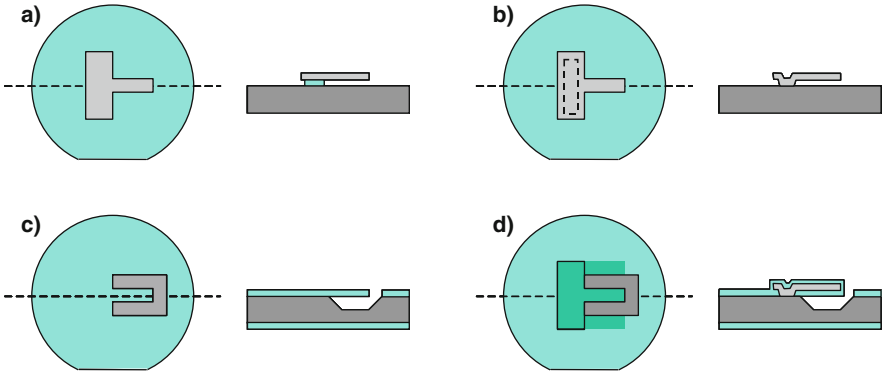

Fig. 8.16 Surface-micromachined structures can be made freestanding by removal of an underlying sacrificial layer or portion of the substrate with extensive lateral etching by a selective wet etchant. (**a**) A cantilevered beam, attached to the substrate through a support at the base, is freed up with a timed etch and a single masking step. (**b**) A cantilevered beam, attached to the substrate at the base through a patterned opening in the sacrificial layer, is freed up with a self-stopping etch using two masking steps. (**c**) A cantilevered beam, formed from the passivation layer, is freed up with a timed or a self-limiting anisotropic substrate etch using only one masking step. (**d**) A cantilevered beam, attached to the substrate at the base through a patterned opening in a passivation layer, is freed up with a selective substrate etch using a total of three masking steps

be very selective to effectively remove the sacrificial layer and leave the structural layers intact without much if any thinning. A high etch selectivity implies that the sacrificial layers are etched much faster than the structural layers and other layers that support the structural layers.

The etch rate and etch selectivity combine with the thickness of the structural layer to determine the maximum amount of time that the die or wafers can be in the etchant. An etchant with high selectivity allows the devices to be in the etchant for an extended time and provides significant overetching capability. In cases where the etch time is unduly limited, the user generally can make adjustments to the process or to the device design. The process may be adjusted by choosing a more selective etch process, using more selective materials, or incorporating an etch accelerator layer. Design alterations may limit the amount of time required in the etchant, for example, by limiting the undercut distance with narrower structural features or by strategically placing small openings in the structural features so that the etchant has local access to the sacrificial layer.

Certain devices require an isolation layer between the sacrificial layer and substrate, such as an LPCVD silicon nitride layer for electrical isolation. The etchant must similarly be selective over any isolation or passivation layers.

As surface-micromachined devices can be quite fragile after sacrificial etching, the etching and drying steps are generally placed late in the process sequence, and careful handling procedures may be needed to avoid unnecessary contact with or undue forces on the microstructures during subsequent dicing and packaging steps.

For particularly fragile structures, special rinse liquid removal techniques may need to be adopted. Devices subject to release stiction or in-use stiction may incorporate a coating such as a self-assembled monolayer (SAM) into the final rinse procedure.

8.7.1 Sacrificial Layer Removal Techniques

Wet chemical etching remains predominant in removal of sacrificial layers for MEMS devices. A room-temperature etchant using standard cleanroom chemicals and an etch process with abundant overetch capability followed by standard DI water rinse procedures may be satisfactory for relatively stiff structures. For example, a buffered HF etch followed by a set of dump rinses and a spin–dry sequence may be used to free long, narrow polysilicon shells with no special handling considerations.

For fragile structures, wet chemical etching may be augmented with special procedures to prevent breakage of the microstructure and reduce yield losses due to stiction from surface tension, van der Waals forces, and solid-residue bridging. Techniques such as freeze-sublimation drying or critical-point drying can be applied that prevent the microstructure from coming into surface-to-surface contact with the substrate and avoid opportunities for unwanted adherence from stiction.

Low surface-tension coatings may improve the process yield and device reliability. These may be applied as part of the final drying sequence, or be applied postrelease yet prior to packaging.

Dry vapor etching techniques can successfully free microstructures. By avoiding contact with any liquid, the capillary forces that tend to drive the microstructure into contact with the substrate during drying are effectively nullified. Vapor HF is one example of a dry release technique that can be done in specially designed fixtures [513]. Controlled gaseous xenon difluoride etching can selectively remove exposed portions of the silicon substrate and polysilicon layers to release metal and dielectric structures using a vapor phase etch without any liquids or plasmas [514–518]. With high selectivity to photoresist, silicon dioxide, silicon nitride, and aluminum, this isotropic etch can be highly effective for integrated MEMS devices to avoid issues related to stiction and provide compatibility with active on-chip devices. Under various conditions of pressure and temperature, other vapor etchants may be used to etch silicon including Cl_2, H_2O, H_2S, HBr, HCl, HI, HI-HF, and SF_6 [25]. Dry plasma etching with SF_6 and other etchants has been shown to be effective in selectively etching portions of a silicon substrate or a polysilicon sacrificial layer with moderate selectivity to oxide [519, 520].

Other sacrificial layer removal techniques include plasma or reactive ion etching of photoresist or other sacrificial materials to free up structural layers selectively. For example, an e-beam evaporated aluminum film on top of photoresist or polyimide can be patterned and etched, then the organic layer removed in an oxygen plasma [521, 522].

8.7.2 Sacrificial Oxide Removal for Polysilicon Microstructures

A predominant number of devices use deposited polysilicon thin films as the structural layer and silicon dioxide as the sacrificial layer, in part because the polysilicon films are IC compatible and structurally well-matched with the substrate, in part because the oxide layer is also IC compatible, and in part because hydrofluoric-based etchants have an extremely high selectivity to oxide over polysilicon. Lateral etches may exceed 500 μm, and the HF-based etchants can clear sacrificial oxides fewer than 100 Å thick with little impediment [523]. Polysilicon films for structural layers may be deposited as fine-grained, stress-controlled films. They may be codeposited with germanium as SiGe films, or doped in situ. Epitaxial processes for epi-poly, sputtered poly, and even amorphous silicon may also serve as structural layers. The underlying sacrificial oxide may be thermally grown offering the highest quality yet the slowest etching oxide. Low-temperature CVD oxides (LTO), doped oxides (BSG, PSG, and BPSG), sputtered oxides and spin-on glass (SOG) can be effectively used as sacrificial layers and etch much faster to provide shorter sacrificial etch times. A fast-etching oxide over a slow-etching thermal oxide serves as an etch accelerator layer to decrease the total etch time. A bilaminate layer such as oxide over silicon nitride allows the oxide to be removed with only minor etching of the nitride that may continue to serve as a buffer or isolation layer. Table 8.31 shows a progression of removal techniques for oxide sacrificial layers and polysilicon microstructures with various oxide types and etchants.

8.7.3 Alternative Sacrificial and Structural Layer Combinations

Deposited polysilicon, either LPCVD, PECVD, sputtered, or epi-poly, can serve alternatively as a sacrificial layer for oxide or nitride freestanding structures. Metals such as aluminum that are readily etched also may be used as sacrificial layers. Polymers including photoresist with overlying deposited layers of e-beam or sputtered metals have been used as sacrificial layers. Various alternative sacrificial layers and structural layers for MEMS devices have been proposed or explored, including structural layers of chromium, copper, gold, molybdenum, nickel–chrome, niobium, palladium, platinum, polyimide, silicon nitride, silver, tantalum, titanium–tungsten, tungsten, and vanadium, with sacrificial layers such as deposited unannealed PSG with an HF etchant [28].

Several authors have compiled collections of actual and prospective structural and sacrificial layers based largely on silicon substrates and silicon semiconductor manufacturing [28, 78, 408]. Nonsilicon systems such as III-V compounds also have seen development of a number of successful sacrificial layers, structural layers, and highly selective etchants and have been itemized elsewhere [532]. Table 8.32 lists a number of sacrificial and structural layer combinations with particular emphasis on etchants commonly available in development and manufacturing sites.

Table 8.31 Sacrificial layer removal for polysilicon microstructures

	Structural layer/sacrificial layer	Etch rate (Å/s)	Etchant	Remarks and references
1	Polysilicon (Si, poly)/oxide (SiO_2, CVD)		BHF	Room temperature; BHF etchant; 640°C polysilicon deposition; 1100°C anneal; 0.23–2.3 μm thick; 0.55–3.5 μm gap; 25–200 μm long cantilevers; 15–60 μm wide; 100–500 μm bridges; CVD oxide sacrificial layers; implanted PSG oxide etch accelerator layer; compressive films [524]
2	Polysilicon (Si, poly)/oxide (SiO_2, thermal)		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); 635°C polysilicon deposition; high-temperature anneal; 2.0 μm thick; 1.0 μm gap; 200 μm × 200 μm plates; thermal oxide sacrificial layer; reactive sealing (vacuum sealing) with oxide or poly; 0.01% compressive strain after annealing [525]
3	Polysilicon (Si, poly)/oxide (SiO_2, PSG)	5400	HF(49%) undiluted	Room temperature; HF etchant (49 wt%); 950°C anneal of PSG sacrificial layer; lateral etch rate for PSG(8 wt%); etch rate slows after ~280 μm of undercut; etch rate lessens for HF dilution and lower phosphorus content [526, 527]
4	Polysilicon (Si, poly)/oxide (SiO_2, thermal)	250	HF(73%) undiluted	Room temperature; HF etchant (49 wt%); etches slightly Al (0.35 Å/s) with 680:1 selectivity (40:1 selectivity with pad etch); add glycerol to BHF for 170:1 selectivity over Al; etches SiO_2 (300 Å/s) in HF(73%):IPA 2:1; avoid water rinsing [93]
5	Polysilicon (Si, poly)/oxide (SiO_2, SOG)		BHF	Room temperature; BHF etchant; 425°C cure of spin-on glass [528]
6	Polysilicon (Si, poly)/oxide (SiO_2, thermal)	45	HF(49%): H_2O 1:1, vapor	20°C; vapor HF etchant; sample at 31.5°C (critical) positioned in vapor above HF bath; avoid condensation; avoid substrate overheating [529, 530]
7	Polysilicon (Si, poly)/oxide (SiO_2, PSG)	48	HF(49%) undiluted, vapor	35°C; vapor HF etchant; bubbled N_2 through HF; slight vacuum; etches Al(0.5%Cu) (0.005 Å/s), SiO_2-thermal (2.5 Å/s), Ti (0.03 Å/s), TiN (0.01 Å/s) [531]

Table 8.32 Sacrificial layer removal for alternative structural and sacrificial layer combinations

	Structural layer/sacrificial layer	Etch rate (Å/s)	Etchant	Remarks and references
1	Aluminum (Al)/silicon (Si)	165–500	XeF_2(vapor) 4 Torr	Room temperature; XeF_2 vapor etchant; aluminum traces and oxide encapsulated polysilicon; doesn't significantly etch Al, PR, $Si3N_4$, SiO_2; loading and surface preparation effects [514]
2	Aluminum (Al)/oxide (SiO_2, SOG)	70	Ammonium fluoride, acetic acid	Room temperature; pad etchant; etches Al (0.5 Å/s); DI water rinse [90, 533]
3	Aluminum gallium arsenide (AlGaAs)/gallium arsenide (GaAs)	650	NH_4OH(29%): H_2O_2(30%) 1:30	25°C; $Al_xGa_{1-x}As$ structural layer with $x > 0.4$; 650:1 selectivity at $x = 0.6$ [196]
4	Aluminum nitride (AlN)/oxide (SiO_2, PSG)	165	NH_4F(40%):Acetic: H_2O 2:2:1	Room temperature; structural layer includes Al and Pt/Ta electrodes; DI water rinse [534]
5	Gallium arsenide (GaAs)/AlGaAs		HF(49%):H_2O 1:4	Room temperature; DHF etchant (4:1); GaAs substrate and structural layer; $Al_xGa_{1-x}As$ sacrificial layer with $x > 0.5$ [532]
6	Germanium (Ge, poly)/oxide (SiO_2, LTO)		BHF	Room temperature; BHF etchant; also etches in HF etchant; 400°C LPCVD Ge deposition; poly-Ge can be etched in hot NH_4OH(29%):H_2O_2(30%):H_2O 1:1:5 at 500 Å/s or piranha [535]
7	Gold (Au)/aluminum (Al)			50°C gold electroplating; aluminum or copper sacrificial layer [536]
8	Indium arsenide (InAs)/aluminum antimonide (AlSb)		HF(49%):H_2O 1:20	Room temperature; DHF etchant (20:1); InAs structural layer; aluminum antimonide sacrificial layer; doesn't significantly etch GaAs [130]
9	Indium gallium arsenide phosphide (InGaAsP)/indium gallium arsenide (InGaAs)		HF(49%): H_2O_2(30%)H_2O 1:1:8	Room temperature; structural layer is predominantly InP; sacrificial layer is $In_{0.53}Ga_{0.47}As$; DI water rinse [537]

Table 8.32 (continued)

	Structural layer/sacrificial layer	Etch rate (Å/s)	Etchant	Remarks and references
10	Nickel (Ni)/chromium (Cr)	350	HCl(38%):H_2O 1:1	Room temperature; electroplated Ni with Cu seed layer; doesn't significantly etch Cu or Ni [538]
11	Nickel (Ni)/oxide (SiO_2-PSG)	3300	HF(49%) undiluted	Room temperature; HF etchant (49 wt%); 1000°C PSG anneal; hexsil process; electroless nickel sandwiched within doped and undoped polysilicon; Triton X-100 surfactant added to etchant [539]
12	Nickel (Ni)/oxide (SiO_2)		BHF	Room temperature; BHF etchant; electroplated nickel through LIGA PMMA mold; strip Ni seed layer in dilute nitric acid prior; single mask [439]
13	Nickel (Ni)/photoresist (PR)		Acetone	Room temperature; electroplated nickel; sacrificial copper plating base; thin photoresist sacrificial layer; thick photoresist plating mold [540]
14	Nickel (Ni)/Ti		HCl(38%):H_2O 1:6	Room temperature etchant, followed by very dilute HF etch for removal of titanium sacrificial layer; electroplated nickel through PMMA mold; sacrificial LIGA (SLIGA); remove underlying polyimide (PI) with ammonium hydroxide [541–544]
15	Nickel (Ni)/zinc (Zn)	28	NH_4OH(29%): H_2O_2(30%):NaOH: H_2O 10 mL:10 mL:3 g: 100 mL	60–70°C etch temperature; sacrificial LIGA (SLIGA); sputtered Ti/Cu seed layer; follow with NH_4OH(29%):H_2O_2(30%):H_2O 100 mL:100 mL:500 mL [545]
16	Nickel–iron (NiFe)/copper (Cu)			50°C NiFe plating temperature; copper or photoresist sacrificial layer [536]
17	Nickel–iron (NiFe, iron-poor)/nickel–iron (NiFe, iron-rich)	1.4–220	Acetic:H_2O 1:9	40°C acetic acid etch; pulsed electrolyte agitation for in situ compositional control; preferentially etches iron-rich layers; low etch rates without biasing; high etch rates with anodic bias [546]
18	Oxide (SiO_2)/silicon (Si), (100)		EDP	120°C etch; thermal oxide cantilevers with Cr/Au metallization and buried p^{++} etch stop [547]

Table 8.32 (continued)

	Structural layer/sacrificial layer	Etch rate (Å/s)	Etchant	Remarks and references
19	Oxide (SiO_2)/silicon (Si), (100)	~12	TMAH(25 wt%): silicic acid:H_2O 80 mL:16 g:150 mL	Deposited and thermal oxides with embedded aluminum and polysilicon features from CMOS process; 70°C etch for 24 h; also etched in XeF_2 [514]
20	Oxide (SiO_2)/polysilicon (Si, poly)	1900	XeF_2(vapor) 3 Torr	Room temperature; XeF_2 vapor etchant; 1000:1 selectivity over PECVD and thermal SiO_2; doesn't significantly etch SiC [519]
21	Parylene C/photoresist (PR)	550	Acetone undiluted	Room temperature; parylene C micro-channels; novolak-diazoquinone positive PR; etches ~1 mm in 30 min; results are linear with the square root of time; slows moderately for postbaked resist [548]
22	Polyimide (PI)/aluminum (Al)	350	H_3PO_4(85%): HNO_3(70%):Acetic: H_2O	Room temperature; PAN etchant; 400°C cure for spin-coated polyimide; evaporated Al sacrificial layer [549, 550]
23	Polyimide (PI)/oxide (SiO_2, PSG)		BHF	Room temperature; BHF etchant; 140°C cure for spin-coated polyimide; PSG sacrificial layer; polyimide hinges for polysilicon structural layers; patterned apertures in poly for faster etching [551]
24	Polyimide (PI)/photoresist (PR)		Heat	450°C; thermal decomposition (dry release) of negative-acting polynorbornene (Avatrel 2000P); also SiO_2-PECVD structural layer [552]
25	Silicon (a-SI, amorphous)/aluminum (Al)		H_3PO_4(85%): HNO_3(70%):Acetic: H_2O 8:1:1:5	Room temperature; PAN etchant; 415°C amorphous silicon anneal; PAN etchant at 55°C; evaporated aluminum sacrificial layer [553]
26	Silicon (Si)/silicon (Si)		HF(49%): HNO_3(70%): Acetic 1:3:8	Room temperature; HNA etchant; 335–660°C bond to 7740 glass; dissolved wafer process; high (1:3:8) or low (EDP) doped substrate removal; leave low-doped (1:3:8) or highly doped (EDP) features on glass [554, 555]

Table 8.32 (continued)

	Structural layer/sacrificial layer	Etch rate (Å/s)	Etchant	Remarks and references
27	Silicon (Si)/silicon (Si), porous		$KOH:H_2O$ 10 g:1000 mL	Room temperature; KOH etchant (1 wt%); mask with Au, NiCr, poly-Si (restrictions), PR (limited), Si_3N_4, SiO_2 (limited), SiC; also polysilicon or nitride-encapsulated structures [556–559]
28	Silicon carbide (SiC)/polyimide (PI)	670	O_2 plasma	Dry etch; 400°C for PECVD SiC deposition; also SiO_2 and Al structural layers on polyimide sacrificial layer [408]
29	Silicon–germanium (SiGe, poly)/germanium (Ge, poly)	50–85	H_2O_2(30%) undiluted	90°C; etch rate varies with doping level; doesn't significantly etch Si or Si_xGe_{1-x} with x >0.4 [560]
30	Silicon nitride (Si_3N_4)/aluminum (Al)	~35	H_3PO_4(85%): HNO_3(70%):Acetic: H_2O 16:1:1:2	50°C; PAN etchant; PECVD silicon nitride; evaporated aluminum sacrificial layer; through KOH-etched backside cavities [561]
31	Silicon nitride (Si_3N_4)/silicon (Si, porous)		$KOH:H_2O$ 10 g:1000 mL	Room temperature; KOH etchant (1 wt%); auxiliary sacrificial layer to expose oxide sacrificial layer from wafer backside [562]
32	SU-8 (PR)/oxide (SiO2, SOG)		HF(49%):H_2O 1:1	Room temperature; DI water rinse [563]
33	SU-8 (PR)/SU-8 (PR)	330	PGMEA	Room temperature; 110°C postbake of SU-8; unexposed lower SU-8 layer dissolves away; Mg mask layer between SU-8 layers; pattern Mg with HCl; doesn't significantly etch Cr/Au; also SOG or SiO_2(PECVD) as sacrificial layers [564]
34	Titanium (Ti)/gold (Au)		Ammonium iodide, iodine, and alcohol	Room temperature; deposited titanium; deposited gold sacrificial layer [565]
35	Tungsten (W)/oxide (SiO_2, LTO)		HF(49%): NH_4F(40%) 1:6	Room temperature; 580°C selective CVD tungsten deposition; SiO_2(LTO) sacrificial layer [566, 567]

8.7.4 Etch Accelerator Layers for Enhanced Sacrificial Layer Removal

Etch accelerator layers allow an etchant to rapidly etch laterally along a relatively thin portion of a sacrificial layer, while etching the majority of the sacrificial layer more slowly yet with an effective etch distance less than the thickness of the sacrificial layer so that the etch time is determined predominantly by the lateral etch rate of the accelerator layer. Ion-implanted thermal oxides with argon-implanted dosages in excess of 1×10^{13} cm^{-2} or phosphorus-doped glass with argon-implanted dosages in excess of 1×10^{14} cm^{-2} have been shown to accelerate the lateral etch and cause an angular sidewall taper to form [568]. Similar effects have been observed for lateral etching of ion-implanted polysilicon and silicon nitride [569]. As the accelerator layer is removed, the etchant is exposed to the bulk of the sacrificial layer and can remove it relatively quickly, as illustrated in Fig. 8.17. Boron, phosphorus, or arsenic-doped glasses etch much faster in HF and buffered HF solutions for most levels of dopant, dopant type, and HF concentration [570]. Bilaminate layers of doped and undoped oxides have also been shown to favorably accelerate the lateral etch rate [571]. Other material configurations such as a polysilicon layer on top of a single crystal substrate allows an anisotropic etchant to laterally remove the polysilicon and anisotropically remove portions of the substrate under the polysilicon regions [572]. Table 8.33 lists some sacrificial etch accelerator layers and removal recipes.

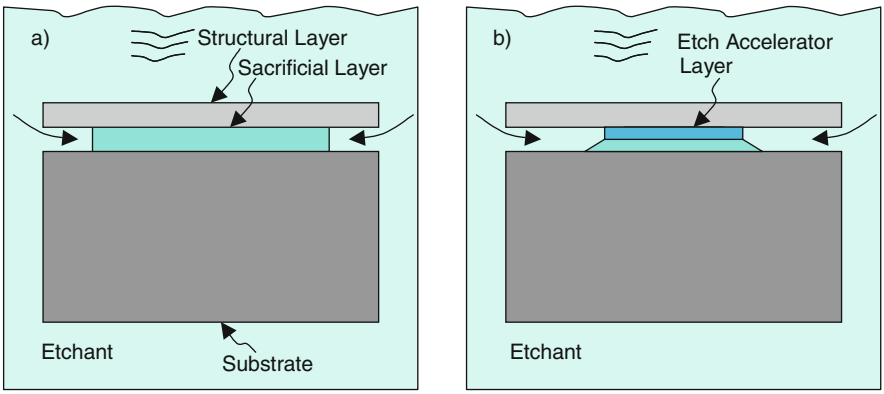

Fig. 8.17 Sacrificial etch accelerator layers allow a structure to be undercut rapidly. The sacrificial layer is structurally altered or augmented with a fast-etching layer so that the lateral etch rate of the sacrificial layer is effectively enhanced. (**a**) Lateral etching without an accelerator layer, and (**b**) lateral etching with an accelerator layer

Table 8.33 Sacrificial etch accelerator layers and removal processes

	Structural layer/sacrificial layer	Etch rate (Å/s)	Etchant	Remarks and references
1	Oxide (SiO_2, implanted)/oxide (SiO_2, thermal)	25/17	HF(49%): NH_4F(40%) 1:7	25°C; BHF etchant (7:1); 3×10^{13} cm^{-2} Ar implant at 50 keV; enhancement increases to 4.8 for $>1 \times 10^{14}$ cm^{-2} Ar at 50 keV or $< 1 \times 10^{15}$ cm^{-2} As at 80 keV [568, 569]
2	Oxide (SiO_2, PSG, implanted)/oxide (SiO_2, PSG)	105/65	HF(49%): NH_4F(40%) 1:7	25°C; BHF etchant (7:1); annealed PSG(7 wt%); 1×10^{14} cm^{-2} Ar implant at 50 keV [568]
3	Silicon nitride (Si_3N_4, implanted)/silicon nitride (Si_3N_4)	5.2:1	H_3PO_4(85%) undiluted	160°C; 1×10^{16} cm^{-2} As implant at 80 keV [569]
4	Silicon (Si, poly, implanted)/polysilicon (Si, poly)	2.6:1	HF(49%): HNO_3(70%):H_2O 3:100:4	Room temperature; HNW etchant; 1×10^{16} cm^{-2} Ar at 50 keV or 1×10^{16} cm^{-2} As at 80 keV [569]
5	Oxide (SiO_2, BSG)/oxide (SiO_2, CVD)	12/1.7	HF(49%): NH_4F(40%):H_2O 1:10:100	26°C; dilute BHF etchant; annealed BSG(30 mol% B_2O_3); selectivity increases with lower BHF concentration and decreases with higher BHF concentration [570]
6	Oxide (SiO_2-PSG)/oxide (SiO_2, CVD)	43/4	HF(49%): NH_4F(40%):H_2O 1:10:33	26°C; dilute BHF etchant; annealed PSG(8.2 mol% P_2O_5) [570]
7	Oxide (SiO_2-ASG)/oxide (SiO_2, CVD)	23/13	HF(49%): NH_4F(40%) 1:10	26°C; BHF etchant (10:1); annealed ASG(4.8 mol% As_2O_3) [570]
8	Oxide (SiO_2-CVD)/oxide (SiO_2, thermal)	90/17	HF(49%): NH_4F(40%) 1:6	25°C; BHF etchant (6:1); enhancement reduces from 5.3:1 to 3.7:1 with 625°C anneal and 2:1 with 800°C anneal [571]
9	Silicon nitride (Si_3N_4)/polysilicon (Si, poly) and Si(100)		KOH:H_2O 540 g:1000 mL	~850°C silicon nitride deposition; Si(100) sacrificial layer; polysilicon accelerator layer; KOH etchant (35 wt%)at 80°C [572]

8.7.5 Rinse Liquid Removal and Antistiction Coatings

Undercutting of structural layers by wet-chemical removal of thin-film sacrificial layers presents a special dilemma: how to remove the freestanding structures from the rinse liquid without causing them to break or stick. Rinsing the etchant and drying the freestanding microstructures can prove surprisingly difficult, in part because of the relative magnitude of surface tension and capillary forces that develop between the structural features and the substrate as the etchant or rinse liquid dries [573, 574]. Blow-drying and stiction effects during drying can be detrimental to the process yield. High-stiffness devices such as low- and medium-aspect ratio beams, plates, and shells provide enough rigidity to overcome capillary forces and surface-tension effects as the rinse liquid is spun off and the devices are blow-dried. Low-stiffness devices common in MEMS sensors and actuators may have sidewall or bottom surfaces that come in contact with other features or the substrate as the last of the rinse liquid evaporates from around the structures. This temporary contact may become permanent, causing yield loss.

Devices in operation may be subjected to high forces that cause contact between surfaces and subsequent sticking. In-use stiction concerns may best be resolved with appropriate design improvements such as increased structural stiffness or limited contact area, or with the application of suitable thin coatings around the microstructure. Release stiction also may be resolved through design by establishing and adhering to minimum structural stiffness design rules. Reductions in stiction may be obtained by limiting mechanical contact area during drying or while in use with structural features such as small detents, protrusions, or dimples in the structural layer or enhanced surface roughness to limit the exposed surface area in contact with the substrate, allowing the innate stiffness of the structural layer to restore the freestanding features after contact is made.

The general rinsing sequence can be augmented for devices with low stiffness elements: (1) a low surface-tension final rinse liquid such as alcohol may be useful in marginal situations; (2) the exposed surfaces may be chemically altered to reduce the surface tension effects by roughening or by altering their phobicity; (3) the final rinse liquid may be extracted in a nonliquid state via freezing and sublimation, or through critical-point drying; (4) the structures may be coated with an effective, low surface-tension coating prior to drying; or (5) vapor or dry release processes such as vapor HF or XeF_2 gas may be adopted for removal of the sacrificial layer that avoid the use of a liquid altogether.

Freezing and sublimation techniques involve freezing the final rinse liquid such as water, alcohol–water mixtures, or organic compounds such as cyclohexane or t-butyl alcohol, and then sublimating the frozen material with a vacuum pump or with enhanced air flow. Full wafers or single die are transferred quickly from the final rinse liquid to decant most of the liquid while preventing air drying, and then placed on a cooling plate or simply pumped down in a chamber to freeze the thin layer of liquid remaining on the wafer surfaces. Sublimation of the frozen liquid begins and fractions of an hour to several hours may be needed to complete the process.

Critical point drying can be an effective way to remove rinse liquid after sacrificial etching and avoid microstructure release stiction. At the critical point, liquid and gas phases coexist at the highest possible temperature. Above this critical temperature, no liquid phase exists. Carbon dioxide with a critical point of 7.38 MPa at 31.1°C is more suitable than water with a critical point of 22.1 MPa and 374°C [575]. Critical point drying with carbon dioxide may be used to remove final rinse liquid such as isopropyl alcohol or methanol [576, 577]. While under pressure at room temperature, the rinse liquid is methodically replaced with liquid CO_2 and then the chamber is elevated in pressure and temperature above the CO_2 critical point. The CO_2 is then vented while maintaining the temperature above the critical temperature to allow the devices to be dried without ever crossing a phase boundary.

Very thin layers of low surface-tension material may be deposited on exposed surfaces to reduce or prevent release stiction, such as self-assembled monolayers (SAM). These coatings can also reduce operational stiction, and may be applied as part of the rinsing sequence or in a later step after the devices have been dried.

Table 8.34 shows a succession of rinse-liquid removal processes that target polysilicon microstructures on silicon substrates with or without a buffer or isolation layer. The solvent-intensive processes may be more suitable for single-die release, although several of the processes have been scaled for wafer-level processes. The techniques are extendable to other structural and sacrificial material combinations.

8.7.6 Examples: Sacrificial Layer Removal and Structural Layer Release

8.7.6.1 Example 1: Fine-Grain Stress-Controlled Polysilicon with an Oxide Sacrificial Layer

A 2.0 μm-thick fine-grain stress-controlled polysilicon film is deposited on a 1.5 μm-thick thermally grown oxide and annealed. The polysilicon is patterned and etched, then undercut with concentrated HF etchant (49%) for 10 min to undercut about 10 μm on each side of the patterned polysilicon, resulting in freestanding cantilevered and doubly supported sections of polysilicon that are 20 μm wide. The HF is removed with a dilution rinse where DI water is flushed into the etch beaker to dilute the etchant without removing the wafer. The wafer is dried with a nitrogen gun, and high-stiffness beams and shells become freestanding.

8.7.6.2 Example 2: Poly-SiGe on a Patterned Oxide/Nitride Laminate

A 1.0 μm layer of borophosphosilicate glass (BPSG) is deposited on a 500 Å thick layer of silicon nitride on a silicon wafer. The bilaminate layer is patterned and etched to expose anchor points. A 2.0 μm-thick SiGe polysilicon film is deposited

Table 8.34 Rinse liquid removal processes

	Material	Removal rate (Å/s)	Rinse liquid	Remarks and references
1	Polysilicon microstructures on Si		H_2O	Freeze-sublimation drying; also sublimation drying; dilution rinse, set wafer horizontally with rinse water on top into roughing pump vacuum system; self-freezes when pumping; sublimates free with time; can be destructive due to water expansion when freezing; may need thermal isolation [578]
2	Polysilicon microstructures on Si		H_2O:Methanol	Freeze-sublimation drying; set wafer horizontally with rinse solution on top into roughing pump vacuum system; self-freezes when pumping; sublimates free with time; less destructive than water; may need thermal isolation [579]
3	Polysilicon microstructures on Si		t-Butyl alcohol	t-Butyl alcohol freeze-sublimation drying; displace rinse water with IPA, transfer rapidly to liquid t-butyl alcohol (>26°C), freeze in refrigerator, then sublimate in vacuum pumping system [580]
4	Polysilicon microstructures on Si		Cyclohexane	Freeze-sublimation drying; dilution DI water rinse, add IPA and transfer wafer to IPA bath, transfer to cyclohexane bath, freeze (<5°C) on Peltier cooler, then sublimate with N_2 gas flow [581]
5	Polysilicon microstructures on Si		Carbon dioxide (CO_2)	Supercritical CO_2 drying; dilution rinse, transfer to methanol bath, replace methanol with liquid CO_2 (~17°C at ~800 psi), increase chamber pressure above 1350 psi as temperature is brought above 40°C; retain temperature while venting CO_2 [576, 582]
6	Polysilicon microstructures on Si		Octadecyltrichloro-silane (OTS)	Self-assembled monolayer (SAM) coating and drying; 0.02 M solution in 5:1 hexadecane:CCl_4 mixture; HF etch, 15-min dilution rinse, NH_4OH:H_2O_2:H_2O 1:1:5 for 5 min at 70°C, 10-min DI water rinse, 5-min methanol bath, 15-min methanol, 5-min CCl_4 bath, 15-min CCl_4, 5-min OTS solution, 5-min CCl_4, 15-min CCl_4, 5-min methanol, 15-min methanol, then air dry with IR lamp; stable to 225°C [583, 584]

Table 8.34 (continued)

	Material	Removal rate (Å/s)	Rinse liquid	Remarks and references
7	Polysilicon microstructures on Si		Perfluorodecyltri-chlorosilane (FDTS)	Self-assembled monolayer (SAM) coating and drying; 0.001 M solution in iso-octane; HF etch, 10-min DI water rinse, 15-min H_2O_2(30 wt%) soak, 5-min H_2O rinse, 5-min IPA rinse, 2 × 5 - min iso-octane rinses, 10-min FDTS solution in N_2 drybox, 2 × 5 - min iso-octane rinses, 2 × 5 - min IPA rinses, 5-min DI water rinse, air dry; stable to 400°C [585]
8	Polysilicon microstructures on Si		Dichlorodimethyl-silane (DDMS)	Self-assembled monolayer (SAM) coating and drying; 0.001 M solution in iso-octane; HF etch, 5 × 2-min DI rinses, 10-min H_2O_2(30 wt%) soak, 1-1/2 min IPA wash and soak, 1-1/2 min iso-octane wash and soak, 10-min DDMS solution, 2-1/2 min iso-octane wash and soak, 1-min hot-plate dry, all in N_2-filled glove box at room temperature; stable to 400–450°C in air; vapor-phase variants available [586, 587]
9	Polysilicon microstructures on Si		Polydiphenylsiloxane (PDPS)	470–485°C; WASA (wafer anti-stiction agent) coating; silanol-terminated PDPS; evacuated N_2-backfilled box oven; also octaphenylcyclotetrasiloxane or mix with cyclic diphenylsiloxane; 25–45 min [588]

on the wafer and annealed. Buffered HF(6:1) is used to sacrificially etch the BPSG layer through an array of 4 μm-square holes in freestanding portions of the SiGe layer and leave the nitride layer relatively intact. The wafer is placed into successive beakers of methanol and then into a critical-point dryer (CPD) where the solvent is displaced with liquid CO_2 under pressure. The pressure and temperature are raised above the critical point and the chamber is vented while maintaining the temperature above the critical point temperature, and the structure becomes free standing.

8.7.6.3 Example 3: Silicon Nitride on a Polysilicon Sacrificial Layer

A 1.0 μm-thick layer of silicon-rich, stress-compensated silicon nitride is deposited on a rough-textured polysilicon film, patterned, and etched. The underlying polysilicon sacrificial layer is removed in a wet etchant comprising sulfuric, nitric, and acetic acids in a 2:3:2 ratio at room temperature. Standard dump-rinse and spin–dry procedures are used for the small aspect-ratio structures.

8.7.6.4 Example 4: Aluminum on Photoresist

A 2-μm thick layer of aluminum is e-beam evaporated onto a patterned layer of 1-μm thick photoresist. The aluminum is patterned and etched, and the photoresist is solvent etched in acetone for 10 min to free the 60 μm-wide aluminum structures. The structures are immersed in a rinse beaker with IPA for 5 min, then carefully dried with a nitrogen gun.

8.8 Porous Silicon Formation with Wet Chemistry

With the application of suitably applied voltages, current, and in some cases external light, silicon can be selectively etched into highly porous material using a hydrofluoric acid etchant. The transformed material retains its initial crystalline orientation, along with hydrided surfaces and a spongelike or sometimes fractal pore structure. The porous silicon can be further oxidized or etched, which can occur quite rapidly due to the large surface area of the porous material. The porous layer can support the deposition of additional films such as epitaxially grown silicon as the outer pores become plugged and provide a surface for further processing [589, 590].

Porous silicon can be formed by chemical staining etchants, although it is generally formed using dilute mixtures of hydrofluoric acid and either water or alcohol in an electrochemical etch that is driven with an external power supply. Unmasked portions of a silicon wafer are electrochemically etched with controllable pore sizes and depths depending on the dopant type, dopant level, current density, and etchant concentration, among other factors. Silicon surfaces exposed to the etchant are transformed into porous silicon as the bulk silicon is etched. Prestructured substrates with pyramidal etch pits or etched detents can cause pore initiation from the pit tip, followed by pore formation perpendicular to the wafer surface a distance of several hundred microns or more with continued application of current. Application of light

from the front or more commonly the back of a wafer can enhance and even modulate the pore diameter [507]. An etch bath that accommodates one or more wafers and a working or counterelectrode along with an external power supply or potentiostat allows the electrochemical etching of silicon, and under select conditions, porous silicon, as illustrated in Fig. 8.18. External light illumination (not shown) may be applied through one of the walls of the etch tank and into a fixture that holds the wafer. Alternatively, a side or bottom of the etch tank may be modified to secure the wafer in a leak-tight manner and allow light to be applied externally while the etchant acts on the inner surface.

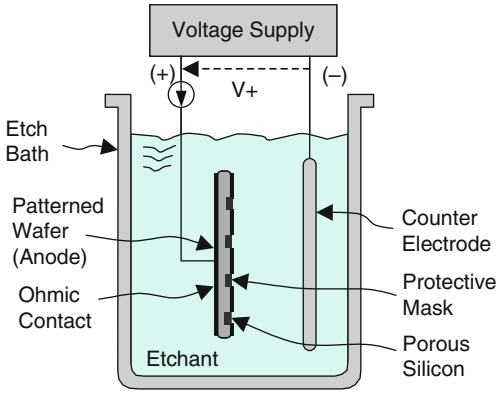

Fig. 8.18 Porous silicon formation is dependent primarily on dopant type, HF concentration, applied voltage, current density, and illumination levels. The silicon wafer can be masked to form porous silicon or completely remove the silicon at selective locations. Selective doping and biasing of the substrate can produce controlled 3-D structures

At large anodic (positive) bias, the p-type and n-type material are electrochemically etched and disappear. At lower anodic bias, p-type material can be selectively etched over the n-type. Combinations of n-and p-type diffusions, epi layers with various bias levels, and control of incident light can result in selective etching or selective porous silicon formation with subsequent removal to form three-dimensional microstructures. Masking with metal masks such as gold with an adhesion layer, unbiased polysilicon layers, silicon carbide, and silicon nitride allow localized etching or porous silicon formation. Silicon dioxide and even photoresist may be used for short times in a dilute HF solution. Many excellent reviews and summaries of porous silicon formation that emphasize micromachining aspects are available to the interested reader [557, 559, 591–595]. Materials such as GaAs and other III-V compounds also exhibit porous structures with wet electrochemical etching [596].

8.8.1 Nanoporous, Mesoporous, and Macroporous Silicon Formation

P-type silicon can be made porous with anodic biasing at nearly every doping level. N-type silicon requires relatively heavy doping in excess of about 1×10^{18} cm^{-3} with anodic biasing, and exhibits a diminished formation rate between 1×10^{16} and 1×10^{18} cm^{-3} [556]. Visible light may be applied to transform n-type material into

porous silicon for low doping levels, which generally has little effect on p-type or degenerate n-type material.

Macroporous silicon is obtained from low-doped n-type silicon with anodic bias and light in an HF solution, with pores having geometries larger than ~500 Å that generally grow perpendicular to the surface that can be initiated with prepatterned surface pits [595]. Micron-diameter pore sizes are controlled in part by the doping, the HF concentration and the applied current density [597]. Mesoporous silicon is formed from heavily doped degenerate n-type or p-type silicon, resulting in large inner surface areas and pore sizes between 20 and 500 Å with smooth surfaces for subsequent processing. Nanoporous silicon, also referred to as microporous silicon, is formed from low-doped p-type or low-doped n-type (with light assistance) silicon, resulting in geometries less than 20 Å with very high inner surface area and possible luminescence.

The conditions for porous silicon formation change for p-type and n-type silicon when illuminated [559]. Without light and without bias, there are essentially no reactions at either the p-type or n-type silicon surfaces when exposed to the etchant. Without light and with low applied anodic bias (positive on the silicon with respect to a counter- or working electrode), porous silicon forms in the p-type material and no reactions occur at the n-type surface. For cathodically biased (negative) silicon and no light, p-type silicon shows no reaction whereas the n-type surface evolves hydrogen. With light and without bias, the p-type material weakly evolves hydrogen and porous silicon is formed in the n-type material. With light and applied anodic bias, porous silicon forms in the p-type material and the n-type material. For cathodically biased silicon with light, hydrogen is evolved at both the p-type and n-type silicon surfaces. With high applied anodic bias, electrochemical etching (i.e., electropolishing) occurs for both p-type and n-type silicon [598, 599]. Organic electrolytes may also be effective in the formation of porous silicon [592]. Some porous silicon etch rates and etchant details are provided in Table 8.35.

8.8.2 Selective Porous Silicon Removal

As porous silicon can have pore sizes less than 20 Å and more than 500 Å (up to 10 μm for macroporous silicon) with porosities of 50% or higher, large amounts of surface area occur that enable etching or oxidizing at effective rates much higher than the bulk, allowing for the selective removal of the porous silicon even with nonselective etchants. A list of some approaches to the selective removal of porous silicon is found in Table 8.36

8.8.3 Examples: Porous Silicon Formation

8.8.3.1 Example 1: Chemical Porous Silicon Formation

A 1–3 Ω cm p-type boron doped wafer is inserted into a polypropylene beaker with a mixture of HF(49%):HNO_3(70%):H_2O 4:1:5 that is primed with several fragments of a silicon wafer prior to adding the DI water. The wafer is stain-etched between

Table 8.35 Porous silicon formation rates and processes

	Material	Formation rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si), n-type (100)		HF(49%):H_2O 1:9	15°C; DHF etchant (9:1); 5 wt% HF; n-type (2-6 Ω cm) silicon with n^+ implanted backside transparent contact; +2 V applied to silicon anode; light intensity modulation; pre-structured with oxide mask and shallow TMAH etch pits; macroporous silicon [507, 508]
2	Silicon (Si), p-type (100)	30	HF(49%):H_2O 2:3	Room temperature; DHF etchant (3:2); 20 wt% HF; p-layer with 1×10^{18} cm^{-3} boron between two n-layers with 1×10^{15} cm^{-3} dopant; lateral formation rate; no external bias; 100 mW/cm^2 light intensity from topside; porous silicon [503]
3	Silicon (Si), $n^-/p^+/n^-/p^+/p^-$ (substrate), (100)		HF(49%):H_2O 2:3	Room temperature; DHF etchant (3:2); 20 wt% HF; p^+ porous layers $\sim 1 \times 10^{18}$ cm^{-3} each, n^- barrier layers $\sim 5 \times 10^{15}$ cm^{-2}, p-substrate $\sim 2 \times 10^{15}$ cm^{-2} (8–16 Ω cm); multi-level porous silicon formation; two masking steps [600]
4	Silicon (Si)	65	HF(49%) undiluted	Room temperature; HF etchant (49 wt%); 5 mA/cm^2 (65 Å/s) then 100 mA/cm^2 for dual-rate anodization; subsequent epi deposition, local patterning and etching of epi, then rapid (>100x) wet oxidation of porous silicon layers at 950°C; silicon-on-oxidized porous silicon (SOPS) process for isolated silicon islands [601]
5	Silicon (Si), n-type (100)	625	HF(49%):Ethanol 1:2	Room temperature; 1.4–2.3 Ω cm; anodic bias; 25 mA/cm^2; fine pores; augmented with thin gold upper electrode; emits visible light [602]
6	Silicon (Si), p-type (100)	500	HF(49%):Ethanol 1:1	Room temperature; Hf etchant (25%) with ethanol; p-type (1 Ω cm) substrate with implanted backside contact; anodic biasing; 230 mA/cm^2 (formation rate reduces to 50 Å/s for 20 mA/cm^2); mask with oxide, n-doped poly-Si, NiCr/Au and PR; alcohol added to improve bubble release [558]
7	Silicon (Si), p^- type (100)	4000	HF(49%):Ethanol 1:1	Elevated temperature; boron-doped 1.0 Ω cm substrate; 1000 mA/cm^2; dark; microporous silicon [603]

Table 8.35 (continued)

	Material	Formation rate (Å/s)	Etchant	Remarks and references
8	Silicon (Si), n^+ type (100)	7500	HF(49%):Ethanol 1:1	Elevated temperature; n-doped 0.067 Ω cm substrate; 400 mA/cm^2; dark; mesoporous silicon [603]
9	Silicon (Si), n^- type (100)	15000	HF(49%):Ethanol 1:1	Elevated temperature; phosphorus-doped 5.0 Ω cm substrate; 1000 mA/cm^2; backside illumination; macroporous silicon; pre-structured surface [603]
10	Silicon (Si), p^+ type (100)		HF(49%):Ethanol 2:1	Room temperature; boron-doped 0.01–0.02 Ω cm substrate; 7 mA/cm^2; 12 μm-thick porous silicon with 15% porosity; subsequent low-temperature thin oxidation, brief HF dip, epi deposition, 1000 Å oxidation and bonded to oxidized Si handle wafer, then handle wafer is ground to expose porous silicon which is then stripped in HF:H_2O_2 1:5; ELTRAN process [590]
11	Silicon (Si), p-type, (100)		HF(49%): HNO_3(70%):H_2O 1:5:10	Room temperature (no intentional heating); HNW etchant; 0.05 Ω cm; stain etching; no bias; no impact by room light while etching; generates visible stains; visibly luminescent with applied UV light; prime solution with silicon fragments prior to adding water; 30-s to 10-min etches [604]
12	Silicon (Si), p-type, (111)		HF(49%): HNO_3(70%):H_2O 1:5:10	Room temperature; HNW etchant; 30–40 Ω cm; stain etching; no bias; luminescent with UV light [605]
13	Silicon (Si), p-type, (100)		HF(49%): HNO_3(70%):H_2O 4:1:5	Room temperature (no intentional heating); HNW etchant; 1–3 Ω cm; stain etching; no bias; generates visible stains; visibly luminescent with applied UV light; also (111) material and n-type material [604]
14	Silicon (Si), p^- type, (100)	450	HF(49%):H_2O 4:1	Room temperature; DHF etchant (1:4); 40 wt% HF; FIPOS process; 1.5 Ω cm; proton-implanted silicon n-type islands; 50 mA/cm^2; dual chamber for anodization; oxidize porous silicon (10–20x faster than thermal) and restore islands to p-type [606]

Table 8.36 Selective porous silicon removal rates and processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si), porous	400	HF(49%): H_2O_2(30%) 1:5	Room temperature; p^+ porous silicon with 15% porosity; doesn't significantly etch Si (<0.01 Å/s) [590]
2	Silicon (Si), porous		HF(49%): HNO_3(70%): Acetic 3:16:1	Room temperature; HNA etchant; 5-s dip may be adequate [509]
3	Silicon (Si), porous		KOH:H_2O 10 g:1000 mL	Room temperature; KOH etchant (1 wt%); 0.1 wt% KOH for nanoporous silicon to 10 wt% KOH for mesoporous silicon; also TMAH etchant or TMAH-based developer [557, 559, 595]
4	Silicon (Si), porous		KOH:H_2O 250 g:750 mL	25°C; KOH etchant (25 wt%); 30-s dip may be adequate [509]
5	Silicon (Si), porous		Oxidize then HF	Room temperature; HF, BHF, or DHF etchant; oxidize at 1000°C (wet) then etch [503]

30 s and 10 min to produce a porous silicon layer about 0.5 μm thick. After rinsing and drying, the resulting stains are visually luminescent with a reddish-orange color when exposed to UV light at 365 nm. Exposure to light during stain-etching does not affect the result [604].

8.8.3.2 Example 2: Nanoporous Silicon Formation

A 525 μm-thick p-type double-side polished silicon wafer with a resistivity of 1–10 Ω cm is implanted with boron to a dosage of $1 \times 10^{16}\,cm^{-2}$, annealed and then coated with a 0.5 μm-thick layer of aluminum layer on one side. The wafer is placed in a fixture that allows electrical contact to the aluminum layer via a metal spring while keeping the metalicized side dry. The fixture is inserted into a 1:1 mixture of HF(49%) and ethanol with the metal spring connected to an adjustable voltage supply. A platinum mesh serving as a counterelectrode is placed in the etchant and also connected to the power supply. The etch tank is covered to keep the wafer dark. The voltage is adjusted to supply 10 mA/cm^2. After 20 min, nanoporous silicon has formed to a depth of 10 μm. The wafer is rinsed in DI water, dried, and removed from the fixture [603].

8.8.3.3 Example 3: Mesoporous Silicon Formation

A lightly doped n-type wafer with a 10 μm-thick phosphorus-doped epi layer having a resistivity of 0.07 Ω cm and an ohmic backside contact is inserted into a fixture

and placed in a 1:1 mixture of HF(49%):ethanol at room temperature. A power supply provides 15 mA/cm^2 of electrical current between the wafer and a platinum electrode in the etchant for 5 min to form a mesoporous silicon layer that is 10 μm thick and stops on the lightly doped substrate [603].

8.8.3.4 Example 4: Macroporous Silicon Formation

An n-type (100) silicon wafer with a resistivity of 2–6 Ω cm and a single 150 μm-thick silicon diaphragm has a patterned frontside oxide and a cleared backside that is implanted to form an n$^+$ contact. While in a fixture, the frontside is etched in TMAH(25 wt%) etchant for 3½ min at 80°C to form pyramidal pits that are 2 μm wide on each side and periodically spaced in the *x*- and *y*-directions with a center-to-center spacing of 4 μm. The wafer is placed in a second fixture. The fixture and a platinum counterelectrode are inserted into an etch bath with HF(5 wt%) and some surfactant at 15°C, and the wafer is biased at +2 V. Light from an external halogen lamp illuminates the wafer backside, and the n-silicon is anodically etched from the frontside starting at the bottoms of the pyramidal pits. As the pores are formed, the light is modulated to vary the diameter of the pore holes with a 4 μm period until a depth of about 130 μm is reached. After opening the pores from the backside by removing the remaining silicon, the membranes are immersed in TMAH(25 wt%) for 60 min at 5°C to encourage (110) etching over (100) etching throughout the length of the pores, resulting in the periodic interconnecting of adjacent pores in a 3-D structure with bandgap properties as a photonic crystal [507].

8.9 Layer Delineation and Defect Determination with Wet Etchants

Wet chemical etching can be used to delineate thin films and substrate layers for validating designs and processes, and to detect and locate defects that cause yield losses or long-term reliability concerns. These etchants are often applied to devices that have been cross-sectioned to allow direct observation of structure details. Absolute doping levels may be intractable, however, dopant-selective etchants can reveal the type and relative doping levels in a substrate and delineate p–n junctions by decorating and making visible variations and transitions in the doped regions for verification of implant and epi profiles, thermal diffusion coefficients, and the thickness of various layers.

Although difficult to locate and observe on a molecular scale, crystalline defects such as dislocations and stacking faults can be detected with selective etchants. Short and sometimes extended etch times are required to generate sizeable etch pits in a substrate that indicates the presence of one or a series of defects, benefiting from the property of some etchants to attack defects preferentially. Etchants may be preferential to dislocations and defects that surround individual crystalline grains,

and grain boundaries in deposited films such as polysilicon and aluminum can be selectively etched to reveal the grain size.

Cross-sectioning of devices for process characterization, verification, qualification, or failure analysis may involve the delineation of layers to enhance their visibility in microscope or SEM micrographs. The micrographs can be enhanced by selective decoration or the generation of preferentially etched steps in a cross-sectioned stack of materials. Selective etchants for delineating different oxides, dielectrics, metals, and semiconducting regions in a device are described below. Other etchants are suitable for locating and determining the density of defects such as pinholes in deposited layers. This section ends with several examples of junction location and layer delineation. Many of the etchants and techniques presented in this section require special care and expertise to use well, as many are light-sensitive or can etch portions of the sample very rapidly. Several excellent references can be consulted for further details and discussions [607–610].

8.9.1 Dopant Level and Defect Determination with Wet Etchants

Selective etchants, such as hi–low etchants or p–n junction delineation etchants, can be used to determine junction depths for single p–n junctions or for complex configurations such as twin-well BiCMOS processes with n-type and p-type buried layers and multiple levels of interconnect. These etchants may stain or discolor one dopant type over another, or etch one type faster than the other to allow the user to locate metallurgical junctions in cross-sectioned samples. The hi–low etchants will etch highly doped material preferentially over lightly doped material. For increased accuracy in junction depth measurements, lapping and polishing a sample with an angled mounting fixture as low as 1° may be used. SEM micrographs often use 90° mounts for accurate dimensioning between layers. A series of dopant-sensitive etchants including hi–low etchants, p–n junction etchants and staining etchants for silicon are listed in Table 8.37.

Defects in crystalline or polycrystalline samples may be determined by the formation of etch pits or other visible features with orientation-sensitive etchants that etch more rapidly in the presence of dislocations and stacking faults in the substrate. Some of the etchants are more suitable for quantifying defect densities in boules or wafers of silicon, as they can etch the material quite rapidly. Table 8.38 shows a series of etchants for decorating defects in silicon with emphasis placed on etchants containing common cleanroom chemicals. Table 8.39 presents additional etchants containing metal compounds for decorating defects in silicon that may be more suitable for a failure analysis laboratory. Table 8.40 includes etchants that preferentially etch grain boundaries in certain materials of interest. Compilations of dislocation etchants for other materials such as III-V and II-VI compounds can be found in several references [76, 611, 612].

Table 8.37 Silicon dopant-sensitive etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si), n^+/n Silicon (Si), n^+/p Silicon (Si), p^+/n Silicon (Si), p^+/p	0.8–400	HF(49%): HNO_3(70%):Acetic 1:3:10	25°C; HNA etchant; also Dash etchant; hi–low etchant; bevel and polish sample; strong illumination; swab, squirt or drip etchant; 1–15 s; look for discoloration; etches lightly doped Si(100) 22 Å/s, Si(111) 0.8 Å/s; etches heavily doped n-type or p-type Si faster (~400 Å/s for $< 5 \times 10^{18}\,cm^{-3}$); 10–15 s for cross-sectioning; stain will appear and steps may be generated [45, 76, 441, 613–615]
2	Silicon (Si), n^+/n Silicon (Si), n^+/p Silicon (Si), p^+/n Silicon (Si), p^+/p		HF(49%): HNO_3(70%) 50 mL: 6 drops	Room temperature; hi–low etchant; bevel and polish sample; strong illumination; swab, squirt or drip etchant; 1–15 s; look for discoloration on p-type side [613, 616, 617]
3	Silicon (Si), n^+/p, alloyed with Al Silicon (Si), p^+/n, alloyed with Al		HF(49%): HNO_3(70%):Acetic 1:3:6	Room temperature; HNA etchant; p–n junction etchant; bevel and polish sample ~3°; no illumination; swab, squirt, or drip etchant; 10–60 s; generates step [613]
4	Silicon (Si), n/p Silicon (Si), p/n		HF(49%) undiluted	Room temperature; HF etchant (49 wt%); p–n junction etchant; strong illumination; n-type turns dark [618]
5	Silicon (Si), n/p Silicon (Si), p/n		HF(49%): HNO_3(70%) 200:1	Room temperature; p–n junction etchant; 5–10 s; illumination amplifies effect; p-type is stained [45]

Table 8.37 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
6	Silicon (Si), n/p Silicon (Si), p/n		HF(49%): HNO_3(70%) 3:97	Room temperature; p–n junction etchant; also 97:3 etchant; 3–5 s; n-type is stained [45]
7	Silicon (Si), n/p Silicon (Si), p/n		HF(49%): $CuSO_4 \cdot 5H_2O$:H_2O 10 mL:8 g:980 mL	Room temperature; p–n junction etchant; copper sulphate etchant; stains dopant levels down to 1×10^{14} cm^{-3}; bevel lap and polish prior; 5–60 s with illumination; rinse and dry; n-type is stained [45, 619]
8	Silicon (Si), n/p Silicon (Si), p/n		HF(49%):H_5IO_6:KI: H_2O 2 mL:5 g:5 mg: 50 mL	Room temperature; Sponheimer–Mills etchant; p–n junction etchant; add KI last; bevel lap and polish; add one part acetone to 30 parts staining solution before use; ~25 s in ultrasonic; simultaneous delineation of active devices including junctions, implants, oxides, nitrides, aluminum, tungsten, and polysilicon; p-type preferentially etched [45, 620]

Table 8.38 Silicon dislocation delineation etchants and etch processes: I

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si)	830	HF(49%):HNO_3(70%):Acetic 8:75:17	25°C; HNA etchant; planar etchant; all planes [441]
2	Silicon (Si)		HF(49%): HNO_3(70%):Acetic 2:3:2	Room temperature; HNA etchant; silicon polishing etchant; 2–3 min [45]
3	Silicon (Si), (100), (110), (111)	22	HF(49%): HNO_3(70%):Acetic 1:3:10	Room temperature; HNA etchant; also Dash etchant; reveals dislocations and stacking faults; 15–20 min for (100) and (110) surfaces; ~4 h for (111) surfaces; etch rate for n^- or p^- (100) material; faster for n^+ and p^+ (~400 Å/s) [441, 611, 614, 615]
4	Silicon (Si)		HF(49%): HNO_3(70%):Acetic 3:5:3	Room temperature; HNA etchant; also CP-4A etchant; highlights twinning defects in silicon [609]
5	Silicon (Si), poly		HF(49%): HNO_3(70%):Acetic 1:3:6	Room temperature; HNA etchant; delineates polysilicon grain boundaries; ~6 min [609]
6	Silicon (Si), poly	1000	HF(49%): HNO_3(70%):Acetic 36:1:20	Room temperature; HNA etchant; also Sopori etchant; defect etchant for polysilicon; dislocations and stacking faults; 5–30 s; cool to 10°C for slower etch rates; HNO_3 component may be doubled [621]

Table 8.39 Silicon dislocation delineation etchants and etch processes – II

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon (Si), (100)	300	HF(49%):CrO_3:H_2O 200 mL:10 g: 100 mL	Room temperature; Schimmel etchant (1 M CrO_3 in H_2O); nonstandard chemical; dislocations; 5–10 min; dilute with H_2O by 50% for heavily doped Si; circular etch pits in Si(100) and Si(111) [622, 623]
2	Silicon (Si), (100), (110), (111)	250	HF(49%):CrO_3:H_2O 100 mL:15 g: 100 mL	Room temperature; Yang etchant (1.5 M CrO_3 in H_2O); preferential etching of silicon surface and stacking defects; 2–15 min; well-defined etch pits [624]
3	Silicon (Si), (111)	210	HF(49%):CrO_3:H_2O 200 mL:50 g: 100 mL	Room temperature; Sirtl etchant (5 M CrO_3 in H_2O); favors (111) surfaces; ineffective for Si(100); preferential etching of silicon defects; ~3 min; 5–15 s for cross-sectioning; mix fresh; well-defined etch pits [45, 76, 624]
4	Silicon (Si), (100), (111)	165	HF(49%): CrO_3(5 M): $Cu(NO_3)_2 \cdot 3H_2O$: HNO_3(70%):Acetic: H_2O 60 mL:30 mL:2 g: 30 mL:60 mL:60 mL	Room temperature; Wright etchant; combine 15 g CrO_3 with 30 mL H_2O for 5 M solution; stacking faults, dislocations, swirls and striations; 1–5 min for crystalline defects; 5–10 s for cross-sectioning; dopant-sensitive [45, 625]
5	Silicon (Si), (100) or (111)		HF, others	25°C; Transene Wright etchant; reveals crystal dislocations, stacking faults, swirls, striations and slip lines; <100> and <111> orientations; p and n dopants; polyethylene or polypropylene tank [626]

Table 8.39 (continued)

	Material	Etch rate (Å/s)	Etchant	Remarks and references
6	Silicon (Si), (100), (111)	830	HF(49%): $Cu(NO_3)_2 \cdot 3H_2O$: HNO_3(70%):Acetic: H_2O 36 mL:1 g:25 mL: 18 mL:21 mL	20°C; Chandler etchant (MEMC etchant); dislocations, slip, twins, and stacking faults [627]
7	Silicon (Si), (100), (110), (111)	250	HF(49%):$K_2Cr_2O_7$: H_2O 200 mL:4.4 g: 100 mL	25–30°C; Secco etchant; $K_2Cr_2O_7$(0.15 M in H_2O); dislocations and lattice defects; ~20 min; ~5 min with ultrasonic; hold sample vertically; also polysilicon grain boundary etchant when used for 30 s at room temperature; dilute with 10 parts water for n-type staining etchant [45]; mix fresh; circular etch pits in Si(100), Si(111) [628]

Table 8.40 Grain-boundary delineation etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Aluminum (Al)		H_2SO_4(96%): HF(49%):H_2O 1:1:8	Room temperature; aluminum grain boundary etchant; 35–40 s [45]
2	Silicon (Si), poly	25	HF(49%): HNO_3(70%):Acetic 1:20:20	Room temperature; HNA etchant; polysilicon grain boundary etchant; ~30 s; illuminate and etch for 5–7 s for cross-sectioning; mix fresh [45]
3	Silicon (Si), poly		Wright etch:H_2O 1:5	Room temperature; polysilicon grain boundary etchant; 40 s [629]

8.9.2 Layer Delineation with Wet Etchants

Silicon, polysilicon, and layers of metals, oxides, and dielectrics and other material stacks can be beveled by grinding and polishing to form an elongated surface profile representative of the layer depths of a sample, then stained and inspected to determine thickness, crystallinity, dopant type, dopant concentration, and metallurgical junctions. Some etchants for delineating oxides of various types are found in Table 8.41. These may be combined sequentially with dopant-sensitive etchants as in Table 8.37 to highlight a variety of features of interest in a device. Table 8.42 shows several etchants for revealing pinholes and other defects in oxide and nitride passivation layers above deposited aluminum traces.

Table 8.41 Oxide layer delineation etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Silicon dioxide (SiO_2), (PSG) over SiO_2	220–570	HF(49%): HNO_3(70%):H_2O 3:2:60	23°C; HNW etchant; phosphosilicate glass (P_2O_5); etches SiO_2 (1.8 Å/s); selectivity of 100:1 to 300:1 PSG over SiO_2 [630]
2	Silicon dioxide (SiO_2), thermal	6	NH_4F(40%):Acetic: H_2O 1:1:1	Room temperature; AMS-5 etchant; oxide etching or cross-sectioning; etches doped, unannealed oxide up to 65 Å/s; slower attack on Al; omit H_2O for further reduction in Al attack [45]

Table 8.42 Pinhole detection etchants and etch processes

	Material	Etch rate (Å/s)	Etchant	Remarks and references
1	Aluminum (Al), passivated		H_2SO_4(96%) undiluted	120°C; pinhole detection; oxide or nitride passivation layers over aluminum; ~5 min [45]
2	Aluminum (Al), passivated		H_3PO_4(85%): HNO_3(70%):H_2O 80:8:38	50°C; pinhole detection; oxide or nitride passivation layers over aluminum; 2–5 min [45]
3	Aluminum (Al), passivated		H_3PO_4(85%): HNO_3(70%):Acetic: H_2O 80:5:5:10	Room temperature; PAN etchant; pinhole detection; oxide or nitride passivation layers over aluminum; 20–30 min [45]

8.9.3 Examples: Layer Delineation and Defect Determination

8.9.3.1 Example 1: Metallurgical Junction Determination

A test wafer is diced along a predetermined region containing a diffused n^+ runner in a p-type substrate. A sample including the region is potted onto a 3° mounting fixture, then lapped and polished to expose the layers. A few drops of p–n junction delineation etchant comprising concentrated HF, nitric, and acetic acids in a 1:3:10 combination is placed onto the sample in a bright light for 15 s. The sample is rinsed in DI water and blown dry. Microscope inspection reveals a 1.0 μm-deep conductive trace for a MEMS accelerometer with on-chip transistors [613, 631].

8.9.3.2 Example 2: Cross-Sectioning and Layer Delineation

An integrated CMOS and MEMS microphone die is attached with high-temperature wax to a vertical polishing fixture. After lapping and polishing, the die is structured for 5 s in an AMS-5 oxide etchant to delineate the thermal and deposited oxides, then structured for 3 s in a p–n junction etchant (97:3 HNO_3:HF) to delineate the n-doped regions. After rinsing and drying, an SEM shows deposited oxide and nitride passivation layers, two layers of aluminum separated by an intermediate oxide, tungsten vias with TiN local interconnects, a polysilicon gate layer, a thick field oxide, a gate oxide, n^+ diffusions and source/drains, p^+ diffusions and source/drains, an n-well, a p-well, and a p-type substrate associated with a twin-well CMOS process [45, 631].

References

1. S.A. Campbell, H.J. Lewerenz (Eds.): Semiconductor Micromachining, Vol. 1, Fundamental Electrochemistry and Physics (Wiley, Chichester, 1998)
2. S.A. Campbell, H.J. Lewerenz (Eds.): Semiconductor Micromachining, Vol. 2, Techniques and Industrial Applications (Wiley, Chichester, 1998)
3. A.R. Clawson: Guide to references on III–V semiconductor etching, Mater. Sci. Eng. 31, 1–438 (2001)
4. M. Elwenspoek, H.V. Jansen: Silicon Micromachining, Chapters 2, 7 (Cambridge University Press, Cambridge, 1998)
5. M. Gad-el-Hak (Ed.): MEMS: Design and Fabrication, Chapter 3 (CRC Press, Boca Raton, FL, 2006)
6. W.F. Gale, T.C. Totemeier (Eds.): Smithells Metals Reference Book, 8th edn (Elsevier, Amsterdam, 2004)
7. H. Geng (Ed.): Semiconductor Manufacturing Handbook, Chapter 11 (McGraw-Hill, New York, NY, 2005)
8. S.K. Ghandhi: VLSI Fabrication Principles – Silicon and Gallium Arsenide, 2nd edn (Wiley, New York, NY, 1994)
9. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn (Krieger, Huntington, NY, 1971)
10. C.A. Harper (Ed.): Handbook of Materials and Processes for Electronics, Chapter 14 (McGraw-Hill, New York, NY, 1970)
11. K.R. Williams (Ed.): Etching, In R. Hull (Ed.): Properties of Crystalline Silicon, Chapter 16 (INSPEC, London, 1999)
12. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices (American Institute of Physics, New York, NY, 1995, originally published 1967)
13. M. Kohler: Etching in Microsystem Technology (Wiley-VCH, Weinheim, 1999)
14. G.T.A. Kovacs: Micromachined Transducers Sourcebook, Chapter 2 (McGraw-Hill, Boston, MA, 1998)
15. M.J. Madou: Fundamentals of Microfabrication: The Science of Miniaturization, 2nd edn (CRC Press, Boca Raton, FL, 2002)
16. L.I. Maissel, R. Glang (Eds.): Handbook of Thin Film Technology, Chapter 7 (McGraw-Hill, New York, NY, 1970)
17. Y. Nishi, R. Doering: Handbook of Semiconductor Manufacturing Technology, Chapter 8 (Marcel Dekker, New York, NY, 2000)
18. T. Ohmi (Ed.): Scientific Wet Process Technology for Innovative LSI/FPD Manufacturing (CRC Press, Boca Raton, FL, 2006)
19. P. Rai-Choudhury (Ed.): Handbook of Microlithography, Micromachining and Microfabrication, Vol. 2: Micromachining and Microfabrication, Chapter 2 (SPIE Press, Bellingham, WA, 1997)
20. K.A. Reinhardt, W. Kern (Eds.): Handbook of Silicon Wafer Cleaning Technology, 2nd edn (William Andrew, Norwich, NY, 2008)
21. G.V. Samsonov, I. M. Vinitskii: Handbook of Refractory Compounds, Chapter 6 (Plenum, New York, NY, 1980)
22. S.M. Sze: Semiconductor Devices, Physics and Technology, Chapter 11 (Wiley, New York, NY, 1985)
23. S.M. Sze: Semiconductor Devices, Physics and Technology, 2nd edn, Chapter 12 (Wiley, New York, NY, 2002)
24. G.F. Vander Voort (Ed.): Metallography, Principles and Practice, Appendix G and others (McGraw-Hill, New York, NY, 1984)
25. J.L. Vossen, W. Kern (Eds.): Thin Film Processes, Chapter V-1 (Academic, New York, NY, 1978)
26. P. Walker, W. H. Tarn (Eds.): CRC Handbook of Metal Etchants (CRC Press, Boca Raton, FL, 1991)

27. K.R. Williams, R.S. Muller: Etch rates for micromachining processing, J. Micromech. Syst. 5(4), 256–269 (1996)
28. K.R. Williams, K. Gupta, M. Wasilik: Etch rates for micromachining processing – Part II, J. Micromech. Syst. 12(6), 761–778 (2003)
29. R. Williams: Modern GaAs Processing Methods, Chapter 5 (Artech House, Boston, MA, 1990)
30. S. Wolf, R.N. Tauber: Silicon Processing for the VLSI Era, Volume 1: Process Technology, Chapter 15 (Lattice Press, Sunset Beach, CA, 1986)
31. Facilities that may offer suitable foundry services for MEMS devices include: Colibrys (http://www.colibrys.com/, accessed December 24, 2010); Dalsa (http://www.dalsa.com/semi/technology/mems.aspx, accessed December 24, 2010); ELMOS SMI (http://www.si-micro.com/, accessed December 24, 2010); IMT (http://www.imtmems.com/, accessed December 24, 2010); MEMS and Nanotechnology Exchange (http://www.mems-exchange.org, accessed December 24, 2010); MemsTech (http://www.memstech.com/, accessed December 24, 2010); Micralyne (http://www.micralyne.com/, accessed December 24, 2010); Sandia National Laboratories (http://mems.sandia.gov/about/fabrication.html, accessed December 24, 2010); Silex (http://www.silexmicrosystems.com/, accessed December 24, 2010); MEMSCap (http://www.semiconductor-technology.com/projects/memscap/, accessed December 24, 2010); Sony Semiconductor Kyushu (http://www.sony.net/Products/SC-HP/memswld/index.html, accessed December 24, 2010); SVTC (http://www.svtc.com/, accessed December 24, 2010); Tanner (http://www.tanner.com/Labs/mems/, accessed December 24, 2010); Tronics (http://www.tronicsmems.com/, accessed December 24, 2010); and others.
32. E.J.J. Kruglick, A.L. Cohen, C.A. Bang: EFAB™ Technology and Applications, In M. Gad-el-Hak (Ed.), MEMS: Design and Fabrication, Chapter 6 (CRC Press, Boca Raton, FL, 2006)
33. K.A. Reinhardt, W. Kern (Eds.): Handbook of Silicon Wafer Cleaning Technology, 2nd edn., Chapter 2 (William Andrew, Norwich, NY, 2008)
34. Nanometrics, Inc.: http://www.nanometrics.com, accessed December 24, 2010
35. KLA-Tencor: http://www.kla-tencor.com, accessed December 24, 2010
36. Veeco Instruments: http://www.veeco.com, accessed December 24, 2010
37. Mitutoyo, Inc.: http://www.mitutoyo.com, accessed December 24, 2010
38. National Nanotechnology Infrastructure Network: http://www.nnin.org/nnin_overview.html, accessed December 24, 2010
39. See for example, MEMS and Nanotechnology Exchange, http://www.mems-exchange.org, accessed December 24, 2010
40. Transene Company, Inc., Danvers, MA 01923: Electronic Grade Chemicals, http://www.transene.com/elec_grade.html, accessed December 24, 2010
41. W.R. Runyan, K.E. Bean: Semiconductor Integrated Circuit Processing Technology, Chapter 6 (Addison-Wesley, Reading, MA, 1990)
42. H. Kikyuama, N. Miki, K. Saka, J. Takano, I. Kawanabe, M. Miyashita, T. Ohmi: Principles of wet chemical processing in ULSI microfabrication, IEEE Trans. Semicond. Manuf. 4(1), 26–35 (1991)
43. J. Buhler, F.-P. Steiner, H. Baltes: Silicon dioxide sacrificial layer etching in surface micromachining, J. Micromech. Microeng. 7, R1–R13 (1997)
44. See, for example, Cyantek Corp. (http://www.cyantek.com, accessed December 24, 2010); J.T. Baker (http://www.mallbaker.com, accessed December 24, 2010); Sigma-Aldrich, Inc. (http://www.sigmaaldrich.com, accessed December 24, 2010); and Transene Company, Inc. (http://www.transene.com, accessed December 24, 2010)
45. F. Beck: Integrated Circuit Failure Analysis, A Guide to Preparation Techniques (Wiley, Chichester, 1998)
46. M. Wong, M.M. Moslehi, R.A. Bowling: Wafer Temperature dependence of the vapor-phase HF oxide etch, J. Electrochem. Soc. 140(1), 205–208 (1993)

47. D.J. Monk, D.S. Soane, R.T. Howe: Determination of the etching kinetics for the hydrofluoric acid/silicon dioxide system, J. Electrochem. Soc. 140(8), 2339–2346 (1993)
48. W.P. Eaton, R.L. Jarecki, J.H. Smith: Prediction of Release-Etch Times for Surface-Micromachined Structures, 1997 Interational Conference on Solid-State Sensors and Actuators, Transducers '97, pp. 249–252 (Chicago, IL, June 16–19, 1997)
49. R.A. Haken, I.M. Baker, J.D.E. Beynon: An Investigation into the dependence of the chemically-etched edge profiles of silicon dioxide films on etchant concentration and temperature, Thin Solid Films 18(1), S3–S6 (1973)
50. K.S. Lebouitz, R.T. Howe, A.P. Pisano: Permeable Polysilicon Etch-Access Windows for Microshell Fabrication, 1995 International Conference on Solid-State Sensors and Actuators, Transducers '95, pp. 224–227 (Stockholm, Sweden, June 25–29, 1995)
51. Stanford Nanofabrication Facility: Wet Etch Rates for Various Non-Metal Films, http://snf.stanford.edu/Process/WetProcessing/WetER1.html, accessed December 24, 2010
52. J.T. Moore, D.L. Chapek: Trench Isolation for Semiconductor Devices, U.S. Patent No. 7.245,856, 2007
53. G.F. Vander Voort: Metallography, Principles and Practice (McGraw-Hill, New York, NY, 1984, reprinted 1999, Appendix G)
54. F.S. Becker, S. Rohl: Low pressure deposition of doped SiO_2 by pyrolysis of tetraethylorthosilicate (TEOS), J. Electrochem. Soc. 134(11) 2923–2931 (1987)
55. Transene Company, Inc., Danvers, MA 01923: Silicon Dioxide (SiO_2) Etchants, http://www.transene.com/sio2.html, accessed December 24, 2010
56. T.J. Cotler, J. Chapple-Sokol: High quality plasma-enhanced chemical vapor deposited silicon nitride films, J. Electrochem. Soc. 140(7), 2071–2075 (1993)
57. L.I. Maissel, R. Glang (Eds.): Handbook of Thin Film Technology (McGraw-Hill, New York, NY, 1970)
58. Transene Company, Inc., Danvers, MA 01923: http://www.transene.com/al2o3.html, accessed December 24, 2010
59. M. Reiche, G. Wagner: Wafer Thinning: Techniques for Ultra-Thin Wafers, Advanced Packaging, March 2003, http://ap.pennnet.com/Articles/Article_Display.cfm?Section=Articles&Subsection=Display&ARTICLE_ID=169369, accessed December 24, 2010
60. H. Robbins, B. Schwartz: Chemical etching of silicon I. The system HF, HNO_3, H_2O, and $HC_2C_3O_2$, J. Electrochem. Soc. 106(6), 505–508 (1959)
61. H. Robbins, B. Schwartz: Chemical etching of silicon II. The system HF, HNO_3, H_2O, and $HC_2C_3O_2$, J. Electrochem. Soc. 107(2), 108–111 (1960)
62. B. Schwartz, H. Robbins: Chemical etching of silicon IV. Etching technology, J. Electrochem. Soc. 123(12), 1903–1909 (1976)
63. T.-J. King, R.T. Howe, S. Sedky, G. Liu, B.C.-Y. Lin, M. Wasilik, C. Duenn: Recent Progress in Modularly Integrated MEMS Technologies, International Electron Devices Meeting, pp. 199–202 (San Francisco, CA, December 8–11, 2002)
64. P.R. Camp: A study of the etching rate of single-crystal germanium, J. Electrochem. Soc. 102(10), 586–593 (1955)
65. S. Kagawa, T. Mikawa, T. Kaneda: Chemical etching of germanium with H_3PO_4-H_2O_2-H_2O solution, Jpn. J. Appl. Phys. 21(11), 1616–1618 (1982)
66. J.L. Vossen, W. Kern, Eds.: Thin Film Processes, Chapter V-1, Table IV (Academic, New York, NY, 1978)
67. J. Bloem, J.C. van Vessem: Etching Ge with mixtures of HF-H_2O_2-H_2O, J. Electrochem. Soc. 109(1), 33–36 (1962)
68. B. Schwartz, H. Robbins: Chemical etching of germanium in solutions of HF, HNO_3, H_2O, and $HC_2H_3O_2$, J. Electrochem. Soc. 111(2), 196–201 (1960)
69. G.R. Booker, R. Stickler: Method of preparing Si and Ge specimens for examination by transmission electron microscopy, Brit. J. Appl. Phys. 13, 446–448 (1962)
70. B. Tuck: The chemical polishing of semiconductors, J. Mater. Sci. 10, 321–339 (1975)

71. S.K. Ghandhi, J.E. Ayers: Chemical etching of germanium, J. Electrochem. Soc. 135(8), 2053–2054 (1988)
72. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 11 (Krieger, Huntington, NY, 1971)
73. D.P. Brunco et al.: Germanium MOSFET devices: Advances in materials understanding, process development, and electrical performance, J. Electrochem. Soc. 155(7), H552–H561 (2008)
74. Transene Company, Inc., Danvers, MA 01923: Reagent Semiconductor Etchants, http://www.transene.com/si.html, accessed December 24, 2010; see also http://www.transene.com/etchants.html, accessed December 24, 2010
75. X.-Q. Wang, X. Yang, K. Walsh, Y.-C. Tai: Gas-Phase Silicon Etching with Bromine Trifluoride, 1997 International Conference on Solid-State Sensors and Actuators, Transducers '97, pp. 1505–1508 (Chicago, IL, June 16–19, 1997)
76. T. Mills: Precision VLSI Cross Sectioning and Staining, Proceedings of 21st Annual Reliability Physics Symposium, pp. 324–331 (Phoenix, AZ, April 5–7, 1983)
77. J. Vossen, W. Kern (Eds.): Thin Film Processes, Chapter V-1, Table III (Academic, New York, NY, 1978)
78. G. Jia, M.J. Madou: MEMS Fabrication, in The MEMS Handbook, MEMS Design and Fabrication, 2nd edn., vol. 2, Chapter 3 (M. Gad-el-Hak (Ed.), CRC/Taylor and Francis, Boca Raton, FL, 2006)
79. M.M. Hussain, N. Moumen, Z. Zhang, B.F. Womack: Metal wet etch issues and effects in dual metal gate stack integration, J. Electrochem. Soc. 153(5), G389–G393 (2006)
80. L.J. Stinson: Sulfur hexafluoride etching effects in silicon, J. Electrochem. Soc. 123(4), 551–555 (1976)
81. XACTIX, Inc., Pittsburgh, PA: Unique Capabilities of Xenon Difluoride for Releasing MEMS, http://www.xactix.com/XeF2_Unique.pdf, accessed December 24, 2010
82. R.J. Bicchieri: Standard Operating Procedure for XeF_2 Etcher, Aug. 2007, http://www-mtl.mit.edu/services/fabrication/sops/xef2.pdf, accessed December 24, 2010
83. Transene Company, Inc., Danvers, MA 01923: Reagent Semiconductor Etchants, http://www.transene.com/si.html, accessed December 24, 2010
84. K.D. Hobart, F.J. Kub, G.G. Jernigan, M.E. Twigg, P.E. Thompson: Fabrication of SOI substrates with ultra-thin si layers, Electron. Lett. 34(12), 1265–1267 (1998)
85. T.K. Carns, M.O. Tanner, K.L. Wang: Chemical etching of $Si_{1-x}Ge_x$ in $HF:H_2O_2:CH_3COOH$, J. Electrochem. Soc. 142(4), 1260–1266 (1995)
86. A.H. Krist, D.J. Godbey, Green: Selective removal of a $Si_{0.7}Ge_{0.3}$ layer from Si(100), Appl. Phys. Lett. 58(17), 1899–1901 (1991)
87. D.J. Godbey, A.H. Krist, K.D. Hobart, M.E. Twigg: Selective removal of $Si_{1-x}Ge_x$ from (100) Si using HNO_3 and HF, J. Electrochem. Soc. 139(10), 2943–2947 (1992)
88. F.S. Johnson, D.S. Miles, D.T. Grider, J.J. Wortman: Selective chemical etching of polycrystalline SiGe alloys with respect to Si and SiO_2, J. Electron. Mater. 21(8), 805–810 (1992)
89. D. Westberg, O. Paul, G.I. Andersson, H. Baltes: Surface micromachining by sacrificial aluminum etching, J. Micromech. Microeng. 6, 376–384 (1996)
90. B.A. Ganji, B.Y. Majilis: Deposition and Etching of Diaphragm and Sacrificial Layer in Novel MEMS Capacitive Microphone Structure, IEEE International Conference on Semiconductor Electronics, ICSE 2008, pp. 232–238 (Johor Bahru, Malaysia, November 25–27, 2008)
91. J.J. Kelly, C.H. de Minjer: An electrochemical study of undercutting during etching of duplex metal films, J. Electrochem. Soc. 122(7), 931–936 (1975)
92. C.A. Harper (Ed.): Handbook of Materials and Processes for Electronics, Chapter 14, Table 31, pp. 14–55 (McGraw-Hill, New York, NY, 1970)

93. P.T.J. Gennissen, P.J. French: Sacrificial Oxide Etching Compatible with Aluminum Metallization, 1997 International Conference on Solid-State Sensors and Actuators, Transducers '97, pp. 225–228 (Chicago, IL, June 16–19, 1997)
94. Transene Company, Inc., Danvers, MA 01923: Aluminum Etchants, http://www.transene.com/aluminum.html, accessed December 24, 2010; see also Etchant/Metal Compatibility Chart, http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
95. Stanford Nanofabrication Facility: Metal Wet Bench Operating Instructions, http://snf.stanford.edu/Equipment/wbmetal/Operation.html, accessed December 24, 2010
96. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 12 (American Institute of Physics, New York, NY, 1995, originally published 1967)
97. R.A. Levy (Ed.): Microelectronic Materials and Processes, Chapter 7 (Springer, New York, NY, 1989)
98. W.E. Beadle, J.C.C. Tsai, R.D. Plummer (Eds.): Quick Reference Manual for Silicon Integrated Circuit Technology, Chapter 5 (Wiley, New York, NY, 1985)
99. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 29 (Krieger, Huntington, NY, 1971)
100. J.L. Vossen, W. Kern (Eds.): Thin Film Processes, Chapter V-1, Table XIV (Academic, New York, NY, 1978)
101. A.E. Morgan, E.K. Broadbent, M. Delfino, B. Coulman, D.K. Sadana: Characterization of a self-aligned cobalt silicide process, J. Electrochem. Soc. 134(4), 925–935 (1987)
102. Transene Company, Inc., Danvers, MA 01923: Titanium Etchants, http://www.transene.com/ti.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
103. Transene Company, Inc., Danvers, MA 01923: Ti-Tungsten TiW-30, http://www.transene.com/tiw.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
104. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 9 (American Institute of Physics, New York, NY, 1995, originally published 1967)
105. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 30 (Krieger, Huntington, NY, 1971)
106. Transene Company, Inc., Danvers, MA 01923: Tungsten Etchant – TWF, http://www.transene.com/mo.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
107. Stanford Nanofabrication Facility: Tweezer Cleaning Procedures, http://snf.stanford.edu/Process/WetProcessing/TweezerCln.html, accessed December 24, 2010
108. UCSB Nanofabrication Facility: Organic Removal, http://www.nanotech.ucsb.edu/index.php?option=com_content&view=article&id=163, accessed December 24, 2010
109. K.A. Reinhardt, W. Kern (Eds.): Handbook of Silicon Wafer Cleaning Technology, 2nd edn., Chapter 4 (William Andrew, Norwich, NY, 2008)
110. MEMS and Nanotechnology Exchange: Photoresist Strip (O2 plasma), http://www.mems-exchange.org/catalog/P3704, accessed December 24, 2010
111. Washington Technology Center: Chemical Use Standard Operating Procedure Revision E, http://www.watechcenter.org/downloads/Chemical_Use.pdf, accessed December 24, 2010; see also Eric Miller, Solvent Strip Operating Procedure, Rev. 1.2, http://www.watechcenter.org/downloads/Solvent_Strip_Operation_Procedure_1_1.pdf, accessed December 24, 2010
112. UCSB Nanofabrication Facility: Standard Pre-Lithography Cleaning Process, http://www.nanotech.ucsb.edu/index.php?option=com_content&view=article&id=160, accessed December 24, 2010
113. Personal communication: David W. Burns (January, 2009)
114. Microelectronics Research Center, Georgia Institute of Technology: Wet Resist Stripping, http://grover.mirc.gatech.edu/processing/processmenu.php?m=p&l=4&s=4, accessed December 24, 2010

115. Microelectronics Research Center, Georgia Institute of Technology: Simple Clean, http://grover.mirc.gatech.edu/processing/processmenu.php?m=p&l=3&s=2, accessed December 24, 2010
116. UCSB Nanofabrication Facility, UC Santa Barbara: Particulate Removal, http://www.nanotech.ucsb.edu/index.php?option=com_content&view=article&id=162, accessed December 24, 2010
117. W. Kern, D.A. Puotinen: Cleaning solutions based on hydrogen peroxide for use in semiconductor technology, RCA Rev. 31(2), 187–206 (1970)
118. C.Y. Chang, S.M. Sze (Eds.): ULSI Technology, Chapter 2 (McGraw-Hill, New York, NY, 1996)
119. W. Kern (Ed.): Handbook of Semiconductor Wafer Cleaning Technology (Noyes, Park Ridge, NJ, 1993)
120. G. Ouimet, D.L. Rath, S.L. Cohen, E.E. Fisch, G.W. Gale: Defect reduction and cost savings through re-inventing RCA cleans, Advanced Semiconductor Manufacturing Conference and Workshop, 12–14, pp. 308–313 (Cambridge, MA, Nov. 12–14, 1996)
121. Virginia Semiconductor, Inc.: Wet-Chemical Etching and Cleaning of Silicon, http://www.virginiasemi.com/pdf/siliconetchingandcleaning.pdf, accessed December 24, 2010
122. Stanford Nanofabrication Facility: Wet Bench Diffusion, wbdiff, https://snf.stanford.edu/SNF/equipment/wet-benches/wet-bench-diffusion/Wet%20Bench%20Diffusion, accessed December 24, 2010
123. M. Bartur, M.-A. Nicolet: Thermal oxidation of transition metal silicides on Si: Summary, J. Electrochem. Soc. 131(2), 371–375 (1984)
124. H. Jiang, C.S. Petersson, M.-A. Nicolet: Thermal oxidation of transition metal silicides, Thin Solid Films 140, 115–129 (1986)
125. S.P. Murarka: Refractory silicides for integrated circuits, J. Vac. Sci. Technol. 17(4), 775–792 (1980)
126. T.P. Chow, A.J. Steckl: Refractory metal silicides: Thin-film properties and processing technology, IEEE Trans. Electron Dev. ED-30(11), 1480–1497 (1983)
127. S.P. Murarka: Silicides for VLSI Applications (Academic, New York, NY, 1983)
128. P. Rosser, G. Tomkins: Silicides for VLSI interconnects, Vacuum 35(10–11), 419–434 (1985)
129. H.C. Gatos, M.C. Lavine: Characteristics of the {111} surfaces of the III-V intermetallic compounds, J. Electrochem. Soc. 107(5), 427–433 (1960)
130. J. Fastenau, E. Ozbay, G. Tuttle, F. Laabs: Epitaxial lift-off of thin InAs layers, J. Electron. Mater. 24(6), 757–760 (1995)
131. A.F. Morpurgo, B.J. van Wees, T.M. Klapwijk, G. Borghs: Submicron processing of InAs based quantum wells: A new, highly selective wet etchant for AlSb, Appl. Phys. Lett. 70(11), 1435–1437 (1997)
132. A. Herczog, R.R. Haberecht, A.E. Middleton: Preparation and properties of aluminum antimonide, J. Electrochem. Soc. 105(9), 533–540 (1958)
133. C. Gatzke, S.J. Webb, K. Fobelets, R. . Stradling: In situ Raman spectroscopy of the selective etching of antimonides in GaSb/AlSb/InAs heterostructures, Semicond. Sci. Technol. 13, 399–403 (1998)
134. E. Yablonovitch, T. Gmitter, J.P. Harbison, R. Bhat: Extreme selectivity in the lift-off of epitaxial GaAs films, Appl. Phys. Lett. 51(26), 2222–2224 (1987)
135. J.-H. Kim, D.H. Lim, G.M. Yang: Selective etching of AlGaAs/GaAs structures using the solutions of citric acid/H_2O_2 and de-ionized H_2O/buffered oxide etch, J. Vac. Sci. Technol. B 16(2), 558–560 (1998)
136. L.H. Guan, M.S. Jusoh, A. Dolah, A. Yusof, M.R. Yahya, B.Y. Majlis: The Study of Etching Selectivity between InGaAs and AlGaAs in Acid Based Etching Solution, ICSE 2004 Proceedings, pp. 423–426 (Kuala Lumpur, December 7–9, 2004)
137. T. Wipiejewski, K.J. Ebeling: In situ controlled wet chemical etching of layered AlGaAs structures with interferometric accuracy, J. Electrochem. Soc. 140(7), 2028–2033 (1993)

138. A.G. Baca, C.I.H. Ashby (Eds.): Fabrication of GaAs Devices, Chapter 4 (Institution of Electrical Engineers, London, 2005)
139. T.R. Stewart, D.P. Bour: Chemical etching of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ using sulfuric and hydrochloric acids, J. Electrochem. Soc. 139(4), 1217–1219 (1992)
140. J.W. Lee, C.J. Santana, C.R. Abernathy, S.J. Pearton, F. Ren: Wet chemical etch solutions for $Al_xGa_{1-x}P$, J. Electrochem. Soc. 143(1), L1–L3 (1996)
141. J.W. Lee, C.J. Santana, C.R. Abernathy, S.J. Pearton: Investigation of Wet Chemical Etching of InGaAlP Alloys, Proceedings of the Symposium on Wide Bandgap Semiconductors and Devices, pp. 316–326 (Chicago, IL, October 8–13, 1995)
142. C. Yi, T.-H. Kim, A.S. Brown: InP-based AlInAs/$GaAs_{0.51}Sb_{0.49}$/GaInAs single heterojunction bipolar transistor for high-speed and RF wireless applications, J. Electron. Mater. 31(2), 95–98 (2002)
143. C.B. Vartuli, S.J. Pearton, J.W. Lee, C.R. Abernathy, J.D. Mackenzie, J.C. Zolper, R.J. Shul: Wet chemical etching of AlN and InAlN in KOH solutions, J. Electrochem. Soc. 143(11), 3681–3684 (1996)
144. J.R. Lothian, J.M. Kuo, W.S. Hobson: Wet and dry etching characteristics of $Al_{0.5}In_{0.5}P$, J. Vac. Sci. Technol. B 10(3), 1061–1065 (1992)
145. D. Zhuang, J.H. Edgar: Wet etching of GaN, AlN, and SiC – A review, Mater. Sci. Eng. Rep. 48(1), 1–46 (2005)
146. J.R. Mileham, S.J. Pearton, C.R. Abernathy, J.D. MacKenzie, R.J. Shul, S.P. Kilcoyne: Wet chemical etching of AlN, Appl. Phys. Lett. 67(8), 1119–1121 (1995)
147. N. Setter (Ed.): Electroceramic-Based MEMS: Fabrication-Technology and Applications, Chapter 13 (Springer, New York, NY, 2005)
148. K.M. Taylor, C. Lenie: Some properties of aluminum nitride, J. Electrochem. Soc. 107(4), 308–314 (1960)
149. T.L. Chu, R.W. Kelm, Jr.: The preparation and properties of aluminum nitride films, J. Electrochem. Soc. 122(7), 995–1000 (1975)
150. A. Reisman, M. Berkenblit, S. Zirinsky, S.A. Chan: The etching of crystallographically determined orifices in sapphire, J. Electrochem. Soc. 126(6), 1004–1008 (1979)
151. A. Reisman, M. Berkenblit, J. Cuomo, S.A. Chan: The chemical polishing of sapphire and MgAl spinel, J. Electrochem. Soc. 118(10), 1653–1657 (1971)
152. B. Zhou, W.F. Ramirez: Kinetics and modeling of wet etching of aluminum oxide by warm phosphoric acid, J. Electrochem. Soc. 143(2), 619–623 (1996)
153. P.J. Tsang, R.M. Anderson, S. Cvikevich: Amorphous CVD Al_2O_3 films by Ta-doping and their physicochemical properties, J. Electrochem. Soc. 123(1), 57–63 (1976)
154. L.I. Berger: Semiconductor Materials, Chapter 4 (CRC Press, Boca Raton, FL, 1997)
155. G.F. Vander Voort (Ed.): Metallography, Principles and Practice, Appendix I (McGraw-Hill, New York, NY, 1984)
156. H. Cordes, K. Kim: Self-diffusion in antimony, J. Appl. Phys. 37(4), 2181 (1966)
157. H.B. Huntington, P.G. Ghate, J.H. Rosolowski: Self-diffusion in antimony, J. Appl. Phys. 35(10), 3027–3032 (1964)
158. J.H. Wernick, J.N. Hobstetter, L.C. Lovell, D. Dorsi: Dislocation etch pits in antimony, J. Appl. Phys. 29(7), 1013–1018 (1958)
159. M.N. Shetty, J.B. Taylor: Dislocation etch pits in arsenic, J. Appl. Phys. 39(8), 3717–3722 (1968)
160. M.F. Ehman, S.B. Austerman: Dislocation etchant for beryllium oxide, J. Am. Ceram. Soc. 56(7), 382–384 (1973)
161. S.B. Austerman, J.B. Newkirk, D.K. Smith, H.W. Newkirk: Etching studies of beryllium oxide crystals, J. Mater. Sci. 2(4), 378–387 (1967)
162. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 5 (Krieger, Huntington, NY, 1971)
163. M.J. Rand, J.F. Roberts: Preparation and properties of thin film boron nitride, J. Electrochem. Soc. 115(4), 423–429 (1968)

164. R. Korn, G. Seyd, U. Paulsen: Cleaning Contaminated Surfaces of Nuclear Power Plants and Recovery of Removed Surface Particles, U.S. Patent. No. 3,895,465
165. L.M. Su, N. Grote, F. Schmitt: Diffused planar InP bipolar transistor with a cadmium oxide film emitter, Electron. Lett. 20(18), 716–717 (1984)
166. P.K. Nair, O.G. Daza, A.A.-C. Readigos, J. Campos, M.T.S. Nair: Formation of conductive CdO layer on CdS thin films during air heating, Semicond. Sci. Technol. 16(8), 651–656 (2001)
167. W. Wohlmuth, I. Adesida: Properties of R. F. magnetron sputtered cadmium-tin-oxide and indium-tin-oxide thin films, Thin Solid Films 479, 223–231 (2005)
168. E.P. Warekois, M.C. Lavine, A.N. Mariano, H.C. Gatos: Crystallographic polarity in the II-VI compounds, J. Appl. Phys. 33(2), 690–696 (1962)
169. M.V. Sullivan, W.R. Bracht: Chemical polishing of cadmium sulfide, J. Electrochem. Soc. 114(3), 295–297 (1967)
170. J. Sarlund, M. Ritala, M. Leskela, E. Siponmaa, R. Zilliacus: Characterization of etching procedure in preparation of CdTe solar cells, Sol. Energy Mater. Sol. Cells 44, 177–190 (1996)
171. M. Inoue, I. Teramoto, S. Takayanagi: Etch pits and polarity in CdTe crystals, J. Appl. Phys. 33(8), 2578–2582 (1962)
172. P. Gaugash, A.G. Milnes: Etching of cadmium telluride, J. Electrochem. Soc. 128(4), 924–926 (1981)
173. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 4 (American Institute of Physics, New York, NY, 1995, originally published 1967)
174. J. Enlund, J. Isberg, M. Karlsson, F. Nikolajeff, J. Olsson, D.J. Twitchen: Anisotropic dry etching of boron doped single crystal CVD diamond, Carbon 43, 1839–1842 (2005)
175. Transene Company, Inc., Danvers, MA 01923: http://www.transene.com/fto.htm, accessed January 3, 2009
176. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 10 (Krieger, Huntington, NY, 1971)
177. P.H. Holloway, G.E. McGuire: Handbook of Compound Semiconductors: Growth, Processing, Characterization, and Devices, Chapter 8 (Noyes, Park Ridge, NJ, 1995)
178. C.A. Harper (Ed.): Handbook of Materials and Processes for Electronics, Chapter 7, Table 27 (McGraw-Hill, New York, NY, 1970)
179. J.W. Faust Jr, A. Sagar: Effect of the polarity of the III-V intermetallic compounds on etching, J. Appl. Phys. 31(2), 331–333 (1960)
180. S.J. Silverman: Junction delineation in GaSb by differential chemical etch rate, J. Electrochem. Soc. 109(2), 166–168 (1962)
181. D.N. MacFadyen: On the preferential etching of GaAs by H_2SO_4-H_2O_2-H_2O, J. Electrochem. Soc. 130(9), 1934–1941 (1983)
182. D.W. Shaw: Localized GaAs etching with acidic hydrogen peroxide solutions, J. Electrochem. Soc. 128(4), 874–880 (1981)
183. S. Iida, K. Ito: Selective etching of gallium arsenide crystals in H_2SO_4-H_2O_2-H_2O system, J. Electrochem. Soc. 118(5), 768–771 (1971)
184. C.R. Tellier, G. Huve, T.G. Leblois: Micromachining of GaAs structures with an acidic hydrogen peroxide solution: Experimental and theoretical 3D etching shapes, Sens. Actuators A 127, 179–193 (2006)
185. Y. Mori, N. Watanabe: A new etching system, H_3PO_4-H_2O_2-H_2O for GaAs and its kinetics, J. Electrochem. Soc. 125(9), 1510–1514 (1978)
186. J.L. Merz, R.A. Logan: GaAs double heterostructure lasers fabricated by wet chemical etching, J. Appl. Phys. 47(8), 3503–3509 (1976)
187. J.R. Flemish, K.A. Jones: Selective wet etching of GaInP, GaAs, and InP in solutions of HCl, CH_3COOH, and H_2O_2, J. Electrochem. Soc. 140(3), 844–847 (1993)
188. E. Biedermann, K. Brack: Preparation of GaAs specimens for transmission electron microscopy, J. Electrochem. Soc. 113(10), 1088 (1966)

189. T. Takebe, T. Yamamoto, M. Fujii, K Kobayashi: Fundamental selective etching characteristics of HF + H_2O_2 + H_2O mixtures for GaAs, J. Electrochem. Soc. 140(4), 1169–1180 (1993)
190. J.L. Richards, A.J. Crocker: Etch pits in gallium arsenide, J. Appl. Phys. 31, 611–612 (1960)
191. S. Adache, K. Oe: Chemical etching characteristics of (001) GaAs, J. Electrochem. Soc. 130(12), 2427–2435 (1983)
192. J.M. O'Connor, E.F. Dvorsky, H.S. Hier, W.P. Reif: Rapid controlled thinning of gallium arsenide, J. Electrochem. Soc. 135(1), 190–193 (1988)
193. T.H. Yeh, A.E. Blakeslee: Junction delineation in gallium arsenide, J. Electrochem. Soc. 110(9), 1018–1019 (1963)
194. K. Kenefick: Selective etching characteristics of peroxide/ammonium hydroxide solutions for GaAs/$Al_{0.16}Ga_{0.84}As$, J. Electrochem. Soc. 129(10), 2380–2382 (1982)
195. J.C. Dyment, G.A. Rozgonyi: Evaluation of a new polish for gallium arsenide using a peroxide-alkaline solution, J. Electrochem. Soc. 118(8), 1346–1350 (1971)
196. Y. Uenishi, H. Tanaka, H. Ukita: Characterization of AlGaAs microstructure fabricated by AlGaAs/GaAs micromachining, IEEE Trans. Electron Dev. 41(10), 1778–1783 (1994)
197. J.J. Gannon, C.J. Nuese: A chemical etchant for the selective removal of GaAs through SiO_2 masks, J. Electrochem. Soc. 121(9), 1215–1219 (1974)
198. S.H. Jones, D.K. Walker: Highly anisotropic wet chemical etching of GaAs using NH_4OH:H_2O_2:H_2O, J. Electrochem. Soc. 137(5), 1653–1654 (1990)
199. Transene Company, Inc., Danvers, MA 01923: Gallium Arsenide Etchants, http://www.transene.com/gall.html, accessed December 24, 2010
200. L.M. Fraas: Three-Terminal Ternary III-V Multicolor Solar Cells and Process of Fabrication, U.S. Patent No. 4,451,691, 1984
201. A. Shintani, S. Minagawa: Etching of GaN using phosphoric acid, J. Electrochem. Soc. 123(5), 706–713 (1976)
202. W.H. Hackett Jr, T.E. McGahan, R.W. Dixon, G.W. Kammlott: A scanning electron microscope investigation of etching phenomena in GaP electroluminescent diodes, J. Electrochem. Soc. 119(7), 973–976 (1972)
203. T. Uragaki, H. Yamanaka, M. Inoue: Selective etching of GaP crystals with hot phosphoric acid, J. Electrochem. Soc. 123(4), 580–582 (1976)
204. R.H. Saul: The defect structure of GaP crystals grown from gallium solutions, vapor phase and liquid phase epitaxial deposition, J. Electrochem. Soc. 115(11), 1184–1190 (1968)
205. Transene Company, Inc., Danvers, MA 01923: Gallium Phosphide Etchant, http://www.transene.com/gap.html, accessed December 24, 2010
206. S. Rivillon, Yves J. Chabel, F. Amy, A. Kahn: Hydrogen passivation of germanium (100) surfaces using wet chemical preparation, Appl. Phys. Lett. 87(253101), 1–3 (2005)
207. M. Balog, M. Schieber: Chemical vapor deposition and characterization of HfO_2 films from organo-hafnium compounds, Thin Solid Films 41, 247–259 (1977)
208. N.J. Sauer, K.B. Chough: A selective etch for InAlAs over InGaAs and for different InGaAlAs quaternaries, J. Electrochem. Soc. 139(1), L10–L11 (1992)
209. M.C. Lavine, H.C. Gatos, M.C. Finn: Characteristics of the {111} surfaces of the III-V intermetallic compounds – Part III, J. Electrochem. Soc. 108(10), 974–980 (1961)
210. H.C. Gatos, M.C. Lavine: Etching and inhibition of the {111} surfaces of the III-V intermetallic compounds: InSb, J. Phys. Chem. Solids 14, 169–174 (1960)
211. J.F. Dewald: The kinetics and mechanism of formation of anode films on single-crystal InSb, J. Electrochem. Soc. 104(4), 244–251 (1957)
212. D.-S. Kim, S.R. Forrest, M.J. Lange, G.H. Olsen, M.J. Cohen: A three wavelength infrared focal plane array detector element, IEEE Photon. Technol. Lett. 6(2), 235–238 (1994)
213. A.H. Eltoukhy, J.E. Greene: Compositionally modulated sputtered InSb/GaSb superlattices: Crystal growth and interlayer diffusion, J. Appl. Phys. 50(1), 505–517 (1979)

214. F. Fiedler, A Schlachetzki, G. Klein: Material-selective etching of InP and an InGaAsP alloy, J. Mater. Sci. 17, 2911–2918 (1982)
215. S. Adachi, Y. Noguchi, H. Kawaguchi: Chemical etching of InGaAsP/InP DH wafer, J. Electrochem. Soc. 129(5), 1053–1062 (1982)
216. H. Ito, T. Ishibashi: Selective and nonselective chemical etching of InGa(As)P/GaAs heterostructures, J. Electrochem. Soc. 142(10), 3383–3386 (1995)
217. J.R. Lothian, J.M. Kuo, F. Ren, S.J. Pearton: Plasma and wet chemical etching of In0.5Ga0.5P, J. Electron. Mater. 21(4), 441–445 (1992)
218. J.W. Lee, S.J. Pearton, C.R. Abernathy, W.S. Hobson, F. Ren, C.S. Wu: Investigation of wet etching solutions for $In_{0.5}Ga_{0.5}P$, Solid-State Electron. 38(11), 1871–1874 (1995)
219. D. Gregusova, P. Elias, L. Malacky, R. Kudela, J. Skriniarova: Wet chemical MESA etching of InGaP and GaAs with solutions based on HCl, CH_3COOH, and H_2O_2, Phys. Stat. Sol. A 151, 113–118 (1995)
220. J.C.C. Fan, F.J. Bachner: Properties of Sn-doped In_2O_3 films prepared by RF sputtering, J. Electrochem. Soc. 122(12), 1719–1725 (1975)
221. J. Kane, H.P. Schweizer, W. Kern: Chemical vapor deposition of transparent electrically conducting layers of indium oxide dope with tin, Thin Solid Films 29, 155–163 (1975)
222. B. Tuck, A.J. Baker: Chemical etching of {111} and {100} surfaces of InP, J. Mater. Sci. 8(11), 1559–1566 (1973)
223. S. Adachi, H. Kawaguchi: Chemical etching characteristics of (001) InP, J. Electrochem. Soc. 128(6), 1342–1349 (1976)
224. C. Seassal, J.L. Leclercq, P. Viktorovitch: Fabrication of InP-based freestanding microstructures by selective surface micromachining, J. Micromech. Microeng. 6, 261–265 (1996)
225. S.B. Phatak, G. Kelner: Material-selective chemical etching in the system inGaAsP/InP, J. Electrochem. Soc. 126(2), 287–292 (1979)
226. S. Singh, R.S. Williams, L.G. Van Uitert, A. Schlierr, I. Camlibel, W.A. Bonner: Analysis of InP surface prepared by various cleaning methods, J. Electrochem. Soc. 129(2), 447–448 (1982)
227. C.W. Wilmsen (Ed.): Physics and Chemistry of III-V Compound Semiconductor Interfaces, p. 416 (Plenum, New York, NY, 1985)
228. J.E.A.M. van den Meerakker, P.C. Baarslag, M. Scholten: On the mechanism of ITO etching in halogen acids: The influence of oxidizing agents, J. Electrochem. Soc. 142(7), 2321–2325 (1995)
229. M. Scholten, J.E.A.M. van den Meerakker: On the mechanism of ITO etching: The specificity of halogen acids, J. Electrochem. Soc. 140(2), 471–475 (1993)
230. C.J. Huang, Y.K. Su, S.L. Wu: The Effect Of Solvent On The Etching of ITO electrode, Mater. Chem. Phys. 84, 146–150 (2004)
231. M. Venkatesan, S. McGee, U. Mitra: Indium tin oxide thin films for metallization in microelectronic devices, Thin Solid Films 170, 151–162 (1989)
232. G. Bradshaw, A.J. Hughes: Etching methods for indium oxide/tin oxide films, Thin Solid Films 33, L5–L7 (1976)
233. Transene Company, Inc., Danvers, MA 01923: Indium Tin Oxide Etchant TE-100, http://www.transene.com/tino.html, accessed December 24, 2010
234. J.B. MacChesney, P.B. O'Connor, M.V. Sullivan: Chemical vapor deposition of iron oxide films for use as semitransparent masks, J. Electrochem. Soc. 118(5), 776–781 (1971)
235. Transene Company, Inc., Danvers, MA 01923: http://www.transene.com/fe2o3.html, accessed December 24, 2010
236. D.G. Coates, W.D. Lawson, A.C. Prior: Single crystal photoconductive detectors in lead selenide, J. Electrochem. Soc. 108(11), 1038–1042 (1961)
237. R.F. Brebrick, W.W. Scanlon: Chemical etches and etch pit patterns on PbS crystals, Chem. Phys. 27(3), 607–608 (1957)
238. J. Baborowski: Microfabrication of piezoelectric MEMS, J. Electroceram. 12(1), 33–51 (2004)

239. S. Trolier, C. Geist, A. Safari, R.E. Newnham, Q.C. Xu: Etched Piezoelectric Structures, Sixth IEEE International Symposium on Applications of Ferroelectrics, pp. 707–710 (Bethlehem, PA, June 8–11, 1986)
240. K.K. Wong (Ed.): Properties of Lithium Niobate, Chapter 11.3 (INSPEC, London, 2002)
241. H.J. Lee, S.-Y. Shin: Lithium niobate ridge waveguides fabricated by wet etching, Electron. Lett. 31(4), 268–269 (1995)
242. K. Nassau, H.J. Levinstein, G.M. Loiacono: Ferroelectric lithium niobate. 1. Growth, domain structure, dislocations and etching, J. Phys. Chem. Solids 27, 983–988 (1966)
243. J.E. Gray, Z. Celik-Butler, D.P. Butler: MgO sacrificial layer for micromachining uncooled Y-Ba-Cu-O IR microbolometers on Si_3N_4 bridges, IEEE J. Microelectromech. Syst. 8(2), 192–199 (1999)
244. K. Sangwal, S.K. Arora: Etching of MgO crystals in acids: Kinetics and mechanism of dissolution, J. Mater. Sci. 13, 1977–1985 (1978)
245. B.N. Pramila Bai, N.H. MacMillan: Chemical polishes for {100}, {110} and {111} MgO surfaces, J. Mater. Sci. 14(2), 494–495 (1979)
246. D.J. Sharp: Thin Film Capacitors Employing Semiconductive Oxide Electrolytics, U.S. Patent No. 3,397,446, 1968
247. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 23 (Krieger, Huntington, NY, 1971)
248. C.-M. Zetterling (Ed.): Process Technology for Silicon Carbide Devices, Chapter 4 (INSPEC, London, 2002)
249. R. Cheung (Ed.): Silicon Carbide Microelectromechanical Systems for Harsh Environments, Chapter 4 (Imperial College Press, London, UK, 2006)
250. G.L. Harris, K. Fekade, K. Wongchotigul: Anodic etching of p-type cubic silicon carbide, J. Mater. Sci.: Mater. Electron. 3, 162–163 (1992)
251. J.S. Shor, A.D. Kurtz: Photoelectrochemical etching of 6H-SiC, J. Electrochem. Soc. 141(3), 778–781 (1994)
252. Transene Company, Inc., Danvers, MA 01923: Gallium Phosphide Etchant, http://www.transene.com/gap.html, accessed December 24, 2010; see also http://www.transene.com/etchants.html, accessed December 24, 2010
253. C. Li, P. Losee, J. Seiler, I. Bhat, T.P. Chow: Fabrication and characterization of 4H-SiC P-N junction diodes by selective-epitaxial growth using TaC as the mask, J. Electron. Mater. 34(4), 450–456 (2005)
254. Transene Company, Inc., Danvers, MA 01923: Tantalum Etchants SIE-8607 and 111, http://www.transene.com/tant_etch.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
255. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 26 (Krieger, Huntington, NY, 1971)
256. P. Skadron, V.A. Johnson: Anistropy and annealing behavior in extrinsic single-crystal tellurium, J. Appl. Phys. 37(4), 1912–1917 (1966)
257. B.J. Baliga, S.K. Ghandhi: Electrochemical patterning of tin oxide films, J. Electrochem. Soc. 124(7), 1059–1060 (1977)
258. M. Wittmer, H. Melchior: Applications of TiN thin films in silicon device technology, Thin Solid Films 93, 397–405 (1982)
259. A.R. Londergan, G. Nuesca, C. Goldberg, G. Peterson, A.E. Kaloyeros, B. Arkles, J.J. Sullivan: Interlayer mediated epitaxy of cobalt silicide on silicon (100) from low temperature chemical vapor deposition of cobalt, J. Electrochem. Soc. 148(1), C21–C27 (2001)
260. M.M. Hussain, M.A. Quevedo-Lopez, H.N. Alshareef, D. Larison, K. Mathur, B.E. Gnade: Deposition method-induced stress effect on ultrathin titanium nitride etch characteristics, Electrochem. Solid-State Lett. 9(12), G361–G363 (2006)
261. Y. Hu, S.P. Tay: Spectroscopic ellipsometry investigation of silicide formation by rapid thermal process, J. Vac. Sci. Technol. B 17(5), 2284–2289 (1999)

262. L. Kritikos, L. Zambelis, G. Papadimitropoulos, D. Davazoglou: Structure and electrical properties of selectively chemically vapor deposited vanadium oxide films from vanadium tri-i-propoxy oxide vapors, Surf. Coat. Technol. 201, 9334–9339 (2007)
263. I. Galesic, B.O. Kolbesen: Characterization of transition metal nitride formation in rapid thermal processing (RTP), Fresenius J. Anal. Chem. 365, 199–202 (1999)
264. M.J. Vellekoop, C.C.G. Visser, P.M. Sarro, A. Venema: Compatibility of zinc oxide with silicon IC processing, Sens. Actuators A21–A23, 1027–1030 (1990)
265. T. Xu, G. Wu, G. Zhang, Y. Hao: The compatibility of ZnO piezoelectric film with micromachining process, Sens. Actuators A Phys. 104(1), 61–67 (2003)
266. V. Bhatt, P. Pal, S. Chandra: Feasibility study of RF sputtered ZnO film for surface micromachining, Surf. Coat. Technol. 198(1–3), 304–308 (2005)
267. J.H. Lan, J. Kanick, A. Catalano, J. Keane: An Alternative Transparent Conducting Oxide to ITO for the a-Si:H TFT-LCD Applications, Second International Workshop on Active Matrix Liquid Crystal Displays, AMLCD '95, pp. 54–57 (September 25–26, Bethlehem, PA, USA, 1995)
268. Y.C. Lin, Y.C. Jian, J.H. Jiang: A study on the wet etching behavior of AZO (ZnO:Al) transparent conducting film, Appl. Surf. Sci. 254, 2671–2677 (2008)
269. A. Sagar, W. Lehmann, J.W. Faust Jr: Etchants for ZnSe, J. Appl. Phys. 39, 5336–5338 (1968)
270. K. Winchester, S.M.R. Spaargaren, J.M. Dell: The Use of ZnS as a Sacrificial Layer in the Construction of PECVD SiN_x Self-Supporting Structures, 1998 Conference on Optoelectronic and Microelectronic Materials and Devices, pp. 493–496 (1998)
271. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 3 (Krieger, Huntington, NY, 1971)
272. J.B. Mooney, J.O. McCaldin: Physical contact properties of beryllium metallization on silicon devices, J. Electrochem. Soc. 124(4), 625–627 (1977)
273. M.E. Straumanis, D.L. Mathis: The dissolution reaction and attack of beryllium by HF, HCl, and H_2SO_4, J. Electrochem. Soc. 109(5), 434–436 (1962)
274. D.L. Partin, J. Heremans, D.T. Morelli, C.M. Thrush, C.H. Olk, T.A. Perry: Growth and characterization of epitaxial bismuth films, Phys. Rev. B 38(6), 3818–3825 (1988)
275. L.C. Lovell, J.H. Wernick: Dislocation etch pits in bismuth, J. Appl. Phys. 30(2), 234–235 (1959)
276. A. Rogel: Durable chromium masks for photoresist applications, Rev. Sci. Instrum. 37, 1416 (1966)
277. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 7 (Krieger, Huntington, NY, 1971)
278. Transene Company, Inc., Danvers, MA 01923: http://www.transene.com/cr.html, accessed December 24, 2010
279. S. Kamiya, H. Takahashi, R. Polini, E. Traversa: Quantitative determination of the adhesive fracture toughness of CVD diamond to WC-Co cemented carbide, Diam. Relat. Mater. 9(2), 191–194 (2000)
280. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 8 (Krieger, Huntington, NY, 1971)
281. S.P. Murarka, D.B. Fraser, A.K. Sinha, H.J. Levinstein, E.J. Lloyd, R. Liu, D.S. Williams, S.J. Hillenius: Self-aligned cobalt disilicide for gate and interconnection and contacts to shallow junctions, IEEE Trans. Electron Dev. ED-34(10), 2108–2115(1987)
282. W. Lee, Y.J. Hu: U.S. Patent Publication 2002/0055262
283. F.-M. Yang, M.-C. Chen: Formation of self-aligned cobalt silicide in normal flow nitrogen furnace, Thin Solid Films 207, 75–81 (1992)
284. A.H.M. Kamal, M.J. Rack, M.N. Kozicki, D.K. Ferry, J. Lutzen, J.A. Hallmark: Ultrathin cobalt silicide layers formed by rapid thermal processing of metal on amorphous silicon, J. Vac. Sci. Technol. B 15(4), 899–902 (1997)

285. T.L. Alford, M. Mitan, J.W. Mayer: Nanometer-Scale Silicide Structures Formed by Focused Ion-Beam Implantation, Proceedings of the 14th International Conference on Ion Implantation Technology, pp. 677–681 (Taos, NM, USA, September 22–27, 2002)
286. A. Matsushita, T. Sadoh, T. Tsurushima: Narrow $CoSi_2$ Line Formation on SiO_2 by Focused Ion Beam, International Conference on Ion Implantation Technology, vol. 2, pp. 861–864 (Kyoto, Japan, June 22–26, 1998)
287. G.-C. Jo, K.-S. Chae: Etchant and Array Substrate having Copper Lines Etch by the Etchant, U.S. Patent No. 6,780,784, 2004
288. H.K. Johnston, T.L. Larson: Etching Compositions and Method for Etching Cu and Ni Based Metals at a Uniform Rate, U.S. Patent No. 3,702,273
289. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 6 (American Institute of Physics, New York, NY, 1995, originally published 1967)
290. Electronic Device Failure Analysis Society: Microelectronics Failure Analysis, 5th ed. (ASM International, 2004)
291. Transene Company, Inc., Danvers, MA 01923: http://www.transene.com/cu_etchant.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
292. D.R. Behrendt, S. Legvold, F.H. Spedding: Magnetic properties of dysprosium single crystals, Phys. Rev. 109(5), 1544–1547 (1958)
293. M. Jang, J. Oh, S. Maeng, W. Cho, S. Lee, K. Kang, K. Park: Characteristics of erbium-silicided n-type Schottky barrier tunnel transistors, Appl. Phys. Lett. 83(13), 2611–2613 (2003)
294. S. Hashimoto, S. Miura, T. Kubo: Dislocation etch pits in gold, J. Mater. Sci. 11(8), 1501–1508 (1976)
295. Transene Company, Inc., Danvers, MA 01923: Gold Etchants, http://www.transene.com/au_etchant.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
296. F.B. Litton: Preparation and some properties of hafnium metal, J. Electrochem. Soc. 98(12), 488–494 (1951)
297. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 12 (Krieger, Huntington, NY, 1971)
298. P.T. Dawson, S.A.J. Stazyk: Auger and x-ray characterization of surface nitride films on Ti, Zr, and Hf, J. Vac. Sci. Technol. 21(1), 36–41 (1982)
299. A.C. English: Detection of growth striations in germanium crystals, J. Appl. Phys. 31(8), 1498–1500 (1960)
300. G.F. Vander Voort: Metallography, Principles and Practice, Chapter 3 (McGraw-Hill, New York, NY, 1984, reprinted 1999)
301. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 13 (Krieger, Huntington, NY, 1971)
302. J.K. Rhee, P.K. Bhattacharya: A study of impurites and traps in liquid phase epitaxial InP in relation to melt prebaking, J. Electrochem. Soc. 130(3), 700–703 (1983)
303. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 5 (American Institute of Physics, New York, NY, 1995, originally published 1967)
304. R.N. Castellano, P.H. Schmidt: Chemical polish and etch for lithium, sodium and potassium, J. Electrochem. Soc. 118(4), 653–654 (1971)
305. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 15 (Krieger, Huntington, NY, 1971)
306. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 16 (Krieger, Huntington, NY, 1971)
307. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 10 (American Institute of Physics, New York, NY 1995, originally published 1967)
308. Transene Company, Inc., Danvers, MA 01923: http://www.transene.com/mo.html, accessed December 24, 2010

309. M. Tanielian, S. Blackstone, R. Lajos: A new technique of forming thin free standing single-crystal films, J. Electrochem. Soc. 132(2), 507–509 (1985)
310. Transene Company, Inc., Danvers, MA 01923: Nichrome Etchants TFC and TFN, http://www.transene.com/ni-cr.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
311. J.T. Sheu, S.P. Yeh, S.T. Tsai, C.H. Lien: Fabrication and Electrical Transport Properties of Nickel Monosilicide Nanowires, Proceedings of the 5th IEEE Conference on Nanotechnology, vol. 2, pp. 780–783 (Nagoya, Japan, July 11–15, 2005)
312. Y.-L. Jiang, G.-P. Ru, X.-P. Qu, B.-Z. Li, C. Detavernier, R. L. Van Meirhaeghe: Linear growth of Ni_2Si thin film on N+/P junction at low temperature, J. Mater. Res. 21(12), 3017–3021 (2006)
313. L.P. Fox: Method of Chemically Polishing Nickel, U.S. Patent No. 2,680,678, 1954
314. Y. Huang, B. Hekmatshoar, S. Wagner, J.C. Sturm: Top-gate amorphous silicon TFT with self-aligned silicide source/drain and high mobility, IEEE Electron Device Lett. 29(7), 737–739 (2008)
315. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 7 (American Institute of Physics, New York, NY 1995, originally published 1967)
316. J.D. Morse, A.F. Jankowski, R.T. Graff, J.P. Hayes: Novel proton exchange membrane thin-film fuel cell for microscale energy conversion, J. Vac. Sci. Technol. A 18(4), 2003–2005 (2000)
317. M.J. Graham, M. Cohen: On the mechanism of low-temperature oxidation (23°–450°C) of polycrystalline nickel, J. Electrochem. Soc. 119(7), 879–882 (1972)
318. Transene Company, Inc., Danvers, MA 01923: Nickel Etchants, http://www.transene.com/ni_etchant.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
319. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 9 (Krieger, Huntington, NY, 1971)
320. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 8 (American Institute of Physics, New York, NY 1995, originally published 1967)
321. M.S. Shivaraman, C.M. Svensson: Control of palladium adherence to silicon dioxide for photolithographic etching, J. Electrochem. Soc. 123(8), 1258 (1976)
322. R.N. Singh, D.W. Skelly, D.M. Brown: Palladium silicide ohmic contacts to shallow junctions in silicon, J. Electrochem. Soc. 133(11), 2390–2393 (1986)
323. Washington Technology Center: Chemical Use Standard Operating Procedure Revision E, http://www.watechcenter.org/downloads/Chemical_Use.pdf, accessed December 24, 2010
324. Transene Company, Inc., Danvers, MA 01923: http://www.transene.com/pd.html, accessed December 24, 2010
325. J.J. Kelly, G.J. Koel: Electrochemical aspects of the beveling of sputtered permalloy films, J. Electrochem. Soc. 125(6), 860–865 (1978)
326. B. Ilic, D. Czaplewski, P. Neuzil, T. Stanczyk, J. Blough, G.J. Maclay: Preparation and characterization of platinum black electrodes, J. Mater. Sci. 35, 3447–3457 (2000)
327. E. Alptekin, M.C. Ozturk, V. Misra: Tuning of the platinum silicide Schottky barrier height on n-type silicon by sulfur segregation, IEEE Electron Dev. Lett. 30(4), 331–333 (2009)
328. M.J. Rand, J.F. Roberts: Observations on the formation and etching of platinum silicide, Appl. Phys. Lett. 24(2), 49–51 (1974)
329. M.J. Rand: I-V characteristics of PtSi-Si contacts made from CVD platinum, J. Electrochem. Soc. 122(6), 811–815 (1975)
330. A.K. Pant, S.P. Murarka, C. Shepard, W. Lanford: Kinetics of platinum silicide formation during rapid thermal processing, J. Appl. Phys. 72(5), 1833–1836 (1992)
331. Transene Company, Inc., Danvers, MA 01923: Ruthernium Etchant RU-44, http://www.transene.com/ru_etchant.html, accessed December 24, 2010
332. C.C. Chen, A.A. Hendrickson: Dislocation etch pits in silver, J. Appl. Phys. 42(6), 2208–2215 (1971)

333. Transene Company, Inc., Danvers, MA 01923: Silver Etchant, http://www.transene.com/ag_etchant.html, accessed December 24, 2010; see also http://www.transene.com/etch_compatibility.html, accessed December 24, 2010
334. Y.H. Choo, O.F. Devereux: Mechanical failure of anodic films on aluminum and tantalum, J. Electrochem. Soc. 123(12), 1868–1876 (1976)
335. D.A. Vermilyea: Flaws in anodic Ta_2O_5 films, J. Electrochem. Soc. 110(4), 250–262 (1963)
336. W.H. Kohl: Handbook of Materials and Techniques for Vacuum Devices, Chapter 11 (American Institute of Physics, New York, NY 1995, originally published 1967)
337. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 25 (Krieger, Huntington, NY, 1971)
338. M.M. Hussain, N. Moumen, J. Barnett, J. Saulters, D. Baker, Z. Zhang: Metal wet etch process development for dual metal gate CMOS, Electrochem. Solid-State Lett. 8(12), G333–G336 (2005)
339. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 28 (Krieger, Huntington, NY, 1971)
340. B.H. Chin, R.E. Frahm, T.T. Sheng, W.A. Bonner: Carrier saturation in tin-doped InP films grown by liquid phase epitaxy, J. Electrochem. Soc. 131(6), 1373–1374 (1984)
341. J.H. Thomas III: Etch rates of an electroplated alloy (Sn-Ni) using a quartz crystal microbalance, J. Electrochem. Soc. 124(5), 677–680 (1977)
342. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 32 (Krieger, Huntington, NY, 1971)
343. K.J. Miller, M.J. Grieco, S.M. Sze: Growth of vanadium on silicon substrates, J. Electrochem. Soc. 113(9), 902–904 (1966)
344. V.F. Drobny: Nearly ideal unguarded vanadium-silicide Schottky-barrier diodes, IEEE Trans. Electron Devices ED-33(9), 1294–1298 (1986)
345. O.N. Carlson, J.A. Haefling, F.A. Schmidt, F.H. Spedding: Preparation and refining of yttrium metal by H-Mg alloy process, J. Electrochem. Soc. 107(6), 540–545 (1960)
346. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 33 (Krieger, Huntington, NY, 1971)
347. C.A. Hampel (Ed.): Rare Metals Handbook, 2nd edn., Chapter 34 (Krieger, Huntington, NY, 1971)
348. W. Tegart: The Electrolytic and Chemical Polishing of Metals, 2nd edn. (Pergamon, Oxford, 1959)
349. Transene Company, Inc., Danvers, MA 01923: Chromium Cerment Etchant TFE, http://www.transene.com/cr.html, accessed December 24, 2010
350. C. Detavernier, R.L. Van Meirhaeghe, W. Vandervorst, K. Maex: Influence of processing conditions on CoSi2 formation in the presence of a Ti capping layer, Microelectron. Eng. 71, 252–261 (2004)
351. M.R. Baklanov, I.A. Badmaeva, R.A. Donaton, L.L. Sveshnikova, W. Storm, K. Maex: Kinetics and mechanism of the etching of $CoSi_2$ in HF-based solutions, J. Electrochem. Soc. 143(10), 3245–3251 (1996)
352. A.T. Kuhn, D. Wakeman, E.Y. El Roubi, G.C.S. Collins: Anodic dissolution and oxygen evolution on binary and ternary iron-silicon alloys, Electrochem. Acta 28(4), 515–527 (1983)
353. T.J. Kang, H.-Y. Lee, Y.H. Kim: Reduction of sheet resistance and low-thermal-budget relaxation of stress gradients in polysilicon microcantilever beams using nickel-silicides, J. Microelectromech. Syst. 16(2), 279–288 (2007)
354. I.P. Nikitina, K.V. Vassilevski, N.G. Wright, A.B. Horsfall, A.G. O'Neill, C.M. Johnson: Formation and role of graphite and nickel silicide in nickel based ohmic contacts to n-type silicon carbide, J. Appl. Phys. 97, 083709 (2005)
355. M. Qin, M.C. Poon, C.Y. Yuen: A study of nickel silicide film as a mechanical material, Sens. Actuators 87, 90–95 (2000)

356. K.-H. Son, J.-K. Yoon, J.-H. Han, G.-H. Kim, J.-M. Doh, S.-R. Lee: Microstructure of $NbSi_2$/SiC nanocomposite coating formed on Nb substrate, J. Alloys Compounds 395, 185–191 (2005)
357. T.J. Kingzett, C.A. Ladas: Effect of oxidizing ambients on platinum silicide formation, J. Electrochem. Soc. 122(12), 1729–1732 (1975)
358. R.V. Skolozdra, T.F. Fedorov, N.M. Popova, E.I. Gladyshevskii: Tungsten-Rhenium-silicon system, Powder Metal. Metal Ceram. 8(9), 743–745 (1969)
359. U. Erlesand, M. Ostling, B.G. Svensson: Point defect generation during silicide formation, Appl. Surf. Sci. 53, 224–229 (1991)
360. B.D. Kraus, M.T. Andreas: U.S. Patent Publication No. US 2003/0205689 (2003)
361. A.E. Widmer, R. Fehlmann: The growth and physical properties of low pressure chemically vapour-deposited films of tantalum silicide on n+-type polycrystalline silicon, Thin Solid Films 138, 131–140 (1986)
362. G.J. Reynolds: Low pressure chemical vapor deposition of tantalum silicide, J. Electrochem. Soc. 135(6), 1483–1490 (1988)
363. S.P. Murarka, D.B. Fraser, A.K. Sinha, H.J. Levinstein: Refractory silicides of titanium and tantalum for low-resistivity gates and interconnects, IEEE Trans. Electron Devices ED-27(8), 1409–1417 (1980)
364. Transene Company, Inc., Danvers, MA 01923: Semiconductor and Thin Film Etchants for Microelectronic Circuits, http://www.transene.com/etchants.html, accessed December 24, 2010
365. H. Geng (Ed.): Semiconductor Manufacturing Handbook, Chapter 5 (McGraw-Hill, New York, NY, 2005)
366. M. Bhaskaran, S. Sriram, L.W. Sim: Nickel silicide thin films as masking and structural layers for silicon bulk micro-machining by potassium hydroxide wet etching, J. Micromech. Microeng. 18, 1–3 (2008)
367. J. M. Harris, S.S. Lau, M.-A. Nicoet, R.S. Nowicki: Studies of the Ti-W metallization system on Si, J. Electrochem. Soc. 123(1), 120–124 (1976)
368. J.-K. Yoon, K.-W. Lee, S.-J. Chung, I.-J. Shon, J.-M. Doh, G.-H. Kim: Growth kinetics and oxidation behavior of WSi_2 coating formed by chemical vapor deposition of Si on W substrate, J. Alloys Compounds 420(1–2), 199–206 (2006)
369. F. Mohammadi, K. . Saraswat: Properties of sputtered tungsten silicide for MOS integrated circuit applications, J. Electrochem. Soc. 127(2), 450–454 (1980)
370. M.F. Bain, B.M. Armstrong, H.S. Gamble: The deposition and characterisation of CVD tungsten silicide for applications in microelectronics, Vacuum 64, 227–232 (2002)
371. E.R. Vance, T.R. Finlayson: The lattice softening in V_3Si, J. Appl. Phys. 39(4), 1980–1982 (1968)
372. H.J. Levinstein, E.S. Greiner, H. Mason Jr: Observation of dislocations in V_3Si single crystals, J. Appl. Phys. 37(1), 164–166 (1966)
373. R.D. Frampton, E.A. Irene, F.M. d'Heurle: A study of the oxidation of selected metal silicides, J. Appl. Phys. 62(7), 2972–2980 (1987)
374. Plastics Design Library: Chemical Resistance, 1. Thermoplastics and 2. Thermoplastic Elastomers, Thermosets and Rubbers, 2nd edn. (Plastics Design Library, Morris, NY, 1994)
375. R.W. Johnson, T.L. Phillips, W.K. Weidner, S.F. Hahn, D.C. Burdeaux, P.H. Townsend: Benzocyclobutene interlayer dielectrics for thin film multichip modules, IEEE Trans. Compon. Hybrids Manuf. Technol. 13(2), 347–352 (1990)
376. Dow Chemical: Rework Procedures for Cyclotene 3000 Series and 4000 Series Resins, http://msdssearch.dow.com/PublishedLiteratureDOWCOM/dh_0055/0901b803800550f8.pdf?filepath=cyclotene/pdfs/noreg/618-00204.pdf&fromPage=GetDoc, accessed December 24, 2010
377. D. Burdeaux, P. Townsend, J. Carr: Benzocyclobutene (BCB) dielectrics for the fabrication of high density, thin film multichip modules, J. Electron. Mater. 19(12), 1357–1366 (1990)

378. D. Paul, A. Pallandre, S. Miserere, J. Weber, J.-L. Viovy: Lamination-based rapid prototyping of microfluidic devices using flexible thermoplastic substrates, Electrophoresis 28, 1115–1122 (2007)
379. R.C. Bening, T.J. McCarthy: Surface modification of poly(tetrafluoroethylene-co-hexafluoropropylene), Macromolecules 23(10), 2648–2655 (1990)
380. X. Wang, J. Engel, C. Liu: Liquid crystal polymer (LCP) for MEMS: Processes and applications, J. Micromech. Microeng. 13, 628–633 (2003)
381. T. Kamal, D.W. Hess: Photoresist removal using low molecular weight alcohols, J. Electrochem. Soc. 147(7), 2749–2753 (2000)
382. K.S. Lee, G.B. Blanchet, F. Gao, Y.-L. Loo: Direct patterning of conductive water-soluble polyanaline for thin-film organic electronics, Appl. Phys. Lett. 86, 074102 (2005)
383. D.A. Peters, C.A. Deckert: Removal of photoresist film residues from wafer surfaces, J. Electrochem. Soc. 126(5), 883–886 (1979)
384. H. Takahashi: Plasma-less photoresist stripping, ECS Trans. 11(2), 189–195 (2007)
385. J.E. Spencer, R.A. Borel, A. Hoff: High rate photoresist stripping in an oxygen afterglow, J. Electrochem. Soc. 133(9), 1922–1925 (1986)
386. S.Y.M. Chooi, P.-Y. Ee, V.K.T. Sih, M.-S. Zhou: Application of Ozonated Aqueous Solutions to Photoresist Strip and Ash Residue Removal Following Plasma Polysilicon Etching, Proceedings of the 6th International Symposium on Cleaning Technology in Semiconductor Device Manufacturing, vol. 99–36, pp. 212–218 (Honolulu, HI, October 17–22, 1999)
387. S. Verhaverbeke, J. Zhao: Novel wet photoresist strip for wafer level packaging, ECS Trans. 11(2), 235–238 (2007)
388. A. Andreatta, Y. Cao, J.C. Chiang, A.J. Heeger: Electrically-conductive fibers of polyaniline spun from solutions in concentrated sulfuric acid, Synth. Metals 26, 383–389 (1988)
389. R.K. Paul, C.K.S. Pillai: Melt/solution processable conducting polyaniline with novel sulfonic acid dopants and its thermoplastic blends, Synth. Metals 114, 27–35 (2000)
390. W.S. Beh, I.T. Kim, D. Qin, Y. Xia, G.M. Whitesides: Formation of patterned microstructures of conducting polymers by soft lithography, and applications in microelectronic device fabrication, Adv. Mater. 11(12), 1038–1041 (1999)
391. Y. Cao, P. Smith, A.J. Heeger: Counter-ion induced processibility of conducting polyaniline and of conducting polyblends of polyaniline in bulk polymers, Synth. Metals 48, 91–97 (1992)
392. J.W.L. Zhou, H.-Y. Chan, T.K.H. To, K.W.C. Lai, W.J. Li: Polymer MEMS actuators for underwater micromanipulation, IEEE/ASME Trans. Mechatron. 9(2), 334–342 (2004)
393. D.K. Armani, C. Liu: Microfabrication Technology for Polycaprolactone, a Biodegradable Polymer, 2000 IEEE Micro Electro Mechanical Systems, MEMS, pp. 294–299 (Miyazaki, Japan, January 23–27, 2000)
394. C. Chu, M. Bachman, Y.-M. Chiang, F. Gonzales, G.P. Li: Characterizations of metallized plastic MEMS, Mat. Res. Soc. Symp. Proc. 605, 97–102 (2000)
395. D.G. LeGrand, J.T. Bendler: Handbook of Polycarbonate Science and Technology, Chapter 15 (Marcel Decker, New York, NY, 2000)
396. J.N. Lee, C. Park, G.M. Whitesides: Solvent compatibility of poly(dimethlysiloxane)-based microfluidic devices, Anal. Chem. 75, 6544–6554 (2003)
397. J. Garra, T. Long, J. Currie, T. Schneider, R. White, M. Paranjape: Dry etching of polydimethylsiloxane for microfluidic systems, J. Vac. Sci. Technol. A 20(3), 975–982 (2002)
398. B.-H. Jo, L.M. Van Lerberghe, K.M. Motsegood, D.J. Beebe: Three-dimensional microchannel fabrication in polydimethylsiloxane (PDMS) elastomer, J. Microelectromech. Syst. 9(1), 76–81 (2000)
399. A. Plecis, Y. Chen: Fabrication of microfluidic devices based on glass-PDMS-glass technology, Microelectron. Eng. 84, 1265–1269 (2007)
400. B. Xu, F. Aria, G.M. Whitesides: Making honeycomb microcomposites by soft lithography, Adv. Mater. 11(6), 492–495 (1999)

401. T.P. Chou, G. Cao: Adhesion of sol-gel-derived organic-inorganic hybrid coatings on polyester, J. Sol-Gel Sci. Technol. 27, 31–41 (2003)
402. D. Briggs, D.M. Brewis, M.B. Konieczo: X-ray photoelectron spectroscopy studies of polymer surfaces, J. Mater. Sci. 11, 1270–1277 (1976)
403. J.R. Rasmussen, E.R. Stedronsky, G.M. Whitesides: Introduction, modification, and characterization of functional groups on the surface of low-density polyethylene film, J. Am. Chem. Soc. 99(14), 4736–4745 (1977)
404. J. Chen, S.K. Spear, J.G. Huddleston, R.D. Rogers: Polyethylene glycol and solutions of polyethylene glycol as green reaction media, Green Chem. 7, 64–82 (2005)
405. J.J. Frantzen: Etching Polyester Film, U.S. Patent. No. 3,186,883 (1965)
406. Microsystems Technology Laboratories, MIT: Standard Operating Procedures Kapton Tape, http://www.mtl.mit.edu/services/fabrication/sops/kapton_tape.html, accessed December 24, 2010
407. R.N. Leyden, W.E. Elias: Method for Selectively Forming Small Diameter Holes in Polyimide/Kevlar Substrates, U.S. Patent No. 4,889,858
408. A. Bagolini, L. Pakula, T.L.M. Scholtes, H.T.M. Pham, P.J. French, P.M. Sarro: Polyimide sacrificial layer and novel materials for post-processing surface micromachining, J. Micromech. Microeng. 12, 385–389 (2002)
409. Transene Company, Inc., Danvers, MA 01923: Kapton Polyimide Film Etchant, http://www.transene.com/kapton.html, accessed December 24, 2010
410. T. Hattori (Ed.): Ultraclean Surface Processing of Silicon Wafers, Chapter 44 (Springer, Berlin, 1998)
411. S.Y.M. Chooi, V.K.T. Sih, P.-Y. Ee, H.-S. Park: Post Nitride-STI Trench Etching (Incorporating DUV Resist and BARC) Polymer Cleaning, Proceedings of the 6th International Symposium on Cleaning Technology in Semiconductor Device Manufacturing, vol. 99–36, pp. 219–226 (Honolulu, HI, October 17–22, 1999)
412. S.B. Fuller, E.J. Wilhelm, J.M. Jacobson: Ink-jet printed nanoparticle microelectromechanical systems, J. Microelectromech. Syst. 11(1), 54–60 (2002)
413. M.T. Koesdjojo, C.R. Koch, V.T. Remcho: Technique for microfabrication of polymeric-based microchips from an SU-8 master with temperature-assisted vaporized organic solvent bonding, Anal. Chem. 81, 1652–1659 (2009)
414. T.R. Christenson: X-Ray – Based Fabrication, In M. Gad-El-Hak (Ed.): The MEMS Handbook: MEMS Design and Fabrication, vol. 2, Chapter 5 (CRC/Taylor and Francis, Boca Raton, FL, 2006)
415. J.-M. Cheng, D.-M. Wang, F.-C. Lin, J.-Y. Lai: Formation and gas flux of asymmetric PMMA membranes, J. Membr. Sci. 109, 93–107 (1996)
416. E. Meng, P.-Y. Li, Y.-C. Tai: Plasma removal of parylene C, J. Micromech. Microeng. 18, 1–13 (2008)
417. J.T.C. Yeh, K.R. Grebe: Patterning of poly-Para-Xylylenes by Reactive Ion Etching, J. Vac. Sci. Technol. A, 1(2, 1983, 604-608
418. V.J. Armond, J.R. Atkinson: Chromic acid as an etchant for bulk polypropylene and its use to study (i) nitric acid attack on polypropylene (ii) crackes in polypropylene induced by tensile stress, J. Mater. Sci. 4, 509–517 (1969)
419. K.-W. Lee, T.J. McCarthy: Surface-selective hydroxylation of polypropylene, Macromolecules 21(2), 309–313 (1988)
420. K. Sakaoku, A. Peterlin: Electron microscopy of drawn polypropylene, J. Polym. Sci. 9, 895–915 (1971)
421. C. Luo, A. Govindaraju, J. Garra, T. Schneider, R. White, J. Currie, M. Paranjape: Releasing SU-8 structures using polystyrene as a sacrificial material, Sens. Actuators A 114, 123–128 (2004)
422. R.-C. Ruaan, T. Chang, D.-M. Wang: Selection criteria for solvent and coagulation medium in view of macrovoid formation in the wet phase inversion process, J. Polym. Sci. B 37, 1495–1502 (1999)

423. L.P. Lee, S.A. Berger, D. Liepmann, L. Pruitt: High aspect ratio polymer microstructures and cantilevers for BioMEMS using low energy ion beam and photolithography, Sens. Actuators A 71, 144–149 (1998)
424. C.A. Costello, T.J. McCarthy: Surface-selective introduction of specific functionalities onto poly(tetrafluoroethylene), Macromolecules 20(11), 2819–2828 (1987)
425. C.A. Costello, T.J. McCarthy: Surface Modification of Poly(tetrafluoroethylene) with Benzoin Dianion, Macromolecules, 17(12), 2940–2942 (1984)
426. S.R. Kim: Surface modification of poly(tetrafluoroethylene) film by chemical etching, plasma, and ion beam treatments, J. Appl. Polym. Sci. 77, 1913–1920 (2000)
427. E.M. Petrie (Ed.): Handbook of Adhesives and Sealants, 2nd edn., Chapter 28.5.6 (McGraw-Hill, New York, NY, 2007)
428. J.M. Engel, J. Chen, D. Bullen, C. Liu: Polyurethane Rubber as a MEMS Material: Characterization and Demonstration of an All-Polymer Two-Axis Artificial Hair Cell Flow Sensor, 2005 IEEE Micro Electro Mechanical Systems, MEMS 279–282 (Miami, FL, January 30 – February 3, 2005)
429. U.S. Aithal, T.M. Aminabhavi, R.H. Balundgi, S.S. Shukla: Interactions of Organic Solvents with Polyurethane, Polymer Reviews, 30(1), 43–105 (1990)
430. C.E. Wilkes, J.W. Summers, C.A. Daniels (Eds.): PVC Handbook, Chapter 15 (Hanser, Munich, 2005)
431. K.H. Lee, H.Y. Kim, Y.M. La, D.R. Lee, N.H. Sung: Influence of a mixing solvent with tetrahydrofuran and N,N-dimethylformamide on electrospun poly(vinyl chloride) nonwoven mats, J. Polym. Sci. B 40, 2259–2268 (2002)
432. Arkema, Inc., Philadelphia, PA: Kynar PVDF Chemical Resistance Chart, http://www.arkema-inc.com/index.cfm?pag=719, accessed December 24, 2010
433. J.H. Heiss Jr, J.R. Wylie: Removal of RTV Silicon Rubber Encapsulants, U.S. Patent No. 4,089,704 (1978)
434. M. Agarwal, R.A. Gunasekaran, P. Coane, K. Varahramyan: Scum-free patterning of SU-8 resist for electroforming applications, J. Micromech. Microeng. 15, 130–135 (2005)
435. A. Pavolotsky, D. Meledin, C. Risacher, M. Pantaleev, V. Belitsky: Micromachining approach in fabricating of THz waveguide components, Microelectron. J. 36, 683–686 (2005)
436. P.M. Dentinger, W.M. Clift, S.H. Goods: Removal of SU-8 photoresist for thick film applications, Microelectron. Eng. 61–62, 993–1000 (2002)
437. A. Jourdain, P. De Moor, S. Pamidighantam, H.A.C. Tilmans: Investigation of the Hermeticity of BCB-Sealed Cavities for Housing (RF-)MEMS Devices, 2002 IEEE Micro Electro Mechanical Systems, MEMS, pp. 677–680 (Las Vegas, NV, January 20–24, 2002)
438. Dow Chemical: Processing Procedures for Cyclotene 4000 Series Photo BCB Resins, DS2100 Puddle Develop Process, http://www.dow.com/PublishedLiterature/dh_0055/0901b80380055101.pdf?filepath=cyclotene/pdfs/noreg/618-00259.pdf&fromPage=GetDoc, accessed December 24, 2010
439. R. Kondo, K. Suzuki, S. Sugiyama: Study on Fabrication of High Aspect Ratio Electrostatic Micro Actuators Using LIGA Process, 1998 International Symposium on Micromechatronics and Human Science, pp. 155–160 (Nagoya, Japan, November 25–28, 1998)
440. E. Bassous: Fabrication of novel three-dimensional microstructures by the anisotropic etching of (100) and (110) silicon, IEEE Trans. Electron Devices ED-25(10), 1178–1185 (1978)
441. K.E. Bean: Anisotropic etching of silicon, IEEE Trans. Electron Dev. ED-25(10), 1185–1193 (1978)
442. R.M. Finne, D.L. Klein: A water-amine-complexing agent system for etching silicon, J. Electrochem. Soc. 114(9), 965–970 (1967)
443. D.L. Kendall: Vertical etching of silicon at very high aspect ratios, Ann. Rev. Mater. Sci. 9, 373–403 (1979)

444. G.T.A. Kovacs, N.I. Maluf, K.E. Petersen: Bulk micromachining of silicon, Proc. IEEE 86(8), 1536–1551 (1998)
445. D.B. Lee: Anisotropic etching of silicon, J. Appl. Phys. 40(11), 4569–4574 (1969)
446. K.E. Petersen: Silicon as a mechanical material, Proc. IEEE 70(5), 420–457 (1982)
447. H. Seidel, L. Csepregi, A. Heuberger, H. Baumgartel: Anisotropic etching of crystalline silicon in alkaline solutions I. Orientation dependence and behavior of passivation layers, J. Electrochem. Soc. 137(11), 3612–3626 (1990)
448. H. Seidel, L. Csepregi, A. Heuberger, H. Baumgartel: Anisotropic etching of crystalline silicon in alkaline solutions II. Influence of dopants, J. Electrochem. Soc. 137(11), 3626–3632 (1990)
449. S.A. Campbell, H. J. Lewerenz (Eds.): Semiconductor Micromachining, vol. 2, Chapters 1–2 (Wiley, Chichester, 1998)
450. M. Elwenspoek, H.V. Jansen: Silicon micromachining, Chapters 2, 3, 6 and 7 (Cambridge University Press, Cambridge, 1998)
451. J.W. Gardner, V.K. Varadan, O. O. Awadelkarim: Microsensors, MEMS, and Smart Devices, Chapters 5, 6 (Wiley, Chichester, 2001)
452. K.R. Williams: Silicon Wet Orientation-Dependent (Anisotropic) Etch Rates, In R. Hull (Ed.): Properties of Crystalline Silicon, Chapter 16.2 (INSPEC, London, 1999)
453. M. Madou: Fundamentals of Microfabrication, Chapter 4 (CRC, Boca Raton, FL, 1998)
454. M. Madou: Fundamentals of Microfabrication: The Science of Miniaturization, 2nd edn, Chapter 4 (CRC, Boca Raton, FL, 2002)
455. W. Menz, J. Mohr, O. Paul: Microsystem Technology, Chapter 6 (Wiley, Weinheim, 2001)
456. A. Reisman, M. Berkenblit, S.A. Chan, F.B. Kaufman, D.C. Green: The controlled etching of silicon in catalyzed ethylenediamine-pyrocatechol-water solutions, J. Electrochem. Soc. 126(8), 1406–1415 (1979)
457. I. Zubel, M. Kramkowska: The effect of alcohol additives on etching characteristics in KOH solutions, Sens. Actuators A, 101, 255–261 (2002)
458. M. Mehregany, S. D. Senturia: Anisotropic etching of silicon in hydrazine, Sens. Actuators 13, 375–390 (1988)
459. M.J. Declercq, L. Gerzberg, J.D. Meindl: Optimization of the hydrazine-water solution for anisotropic etching of silicon in integrated circuit technology, J. Electrochem. Soc. 122(4), 545–552 (1975)
460. U. Schnakenberg, W. Benecke, B. Lochel: NH_4OH-based etchants for silicon micromachining, Sens. Actuators A21–A23, 1031–1035 (1990)
461. U. Schnakenberg, W. Benecke, B. Lochel, P. Lange: NH_4OH-based etchants for silicon micromachining: Influence of additives and stability of passivation layers, Sens. Actuators A25–A27, 1–7 (1991)
462. U. Schnakenberg, W. Benecke, P. Lange: TMAHW Etchants for Silicon Micromachining, 1991 International Conference on Solid-State Sensors and Actuators, Transducers '91, pp. 815–818 (San Francisco, CA, June 24–27, 1991)
463. J.T.L. Thong, W.K. Choi, C.W. Chong: TMAH etching of silicon and the interation of etching parameters, Sens. Actuators A 63, 243–249 (1997)
464. M. Shikida, K. Sato, K. Tokoro, D. Uchikawa: Differences in anisotropic etching properties of KOH and TMAH solutions, Sens. Actuators 80, 179–188 (2000)
465. O. Tabata, R. Asahi, H. Funabashi, K. Shimaoka, S. Sugiyama: Anisotropic etching of silicon in TMAH solutions, Sens. Actuators A 34, 51–57 (1992)
466. I. Zubel, M. Kramkowska: The effect of isopropyl alcohol on etching rate and roughness of (100) Si surface etched in KOH and TMAH solutions, Sens. Actuators A 93, 138–147 (2001)
467. E. Steinsland, T. Finstad, A. Hanneborg: Etch rates of (100), (111) and (110) single-crystal silicon in TMAH measured in situ by laser reflectance interferometry, Sens. Actuators 86, 73–80 (2000)

468. A. Merlos, M. Acero, M.H. Bao, J. Bausells, J. Esteve: TMAH/IPA anisotropic etching characteristics, Sens. Actuators A 37–38, 737–743 (1993)
469. P.M. Sarro, S. Brida, W.v.d. Vlist: Aluminum Passivation in Saturated TMAHW Solutions for IC-Compatible Microstructures and Device Isolation, SPIE Proceedings, vol. 2879, pp. 242–250 (Austin, TX, September 23, 1996)
470. M. Sekimura: Anisotropic Etching of Surfactant-Added TMAH Solution, 1999 IEEE Micro Electro Mechanical Systems, MEMS '99, pp. 650–655 (Orlando, FL, January 17–21, 1999)
471. P.M. Sarro, D. Brida, W.v.d. Vlist, S. Brida: Effect of surfactant on surface quality of silicon microstructures etched in saturated TMAHW solutions, Sens. Actuators 85, 340–345 (2000)
472. Transene Company, Inc., Danvers, MA 01923: Preferential Silicon Etchants, http://www.transene.com/si.html, accessed December 24, 2010
473. C.A. Desmond, C.E. Hunt, S.N. Farrens: The effects of process-induced defects on the chemical selectivity of highly doped boron etch stops in silicon, J. Electrochem. Soc. 141(1), 178–184 (1994)
474. N.F. Raley, Y. Sugiyama, T. Van Duzer: (100) silicon etch-rate dependence on boron concentration in ethylenediamine-pyrocatachol-water solutions, J. Electrochem. Soc. 131(1), 161–171 (1984)
475. E. Steinsland, M. Nese, A. Hanneborg, R.W. Bernstein, H. Sandmo, G. Kittilsland: Boron etch-stop in TMAH solutions, Sens. Actuators A 54, 728–732 (1996)
476. J.T. Borenstein, N.D. Gerrish, M.T. Currie, E.A. Fitzgerald: A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining, 1999 IEEE Micro Electro Mechanical Systems, MEMS '99, pp. 205–210 (Orlando, FL, January 17–21, 1999)
477. W.P. Maszara: Silicon-on-insulator by wafer bonding: A review, J. Electrochem. Soc. 138(1), 341–347 (1991)
478. I.G. Stoev, R.A. Yankov, C. Jeynes: Formation of etch-stop structures utilizing ion-beam synthesized buried oxide and nitride layers in silicon, Sens. Actuators 19, 183–197 (1989)
479. A. Soderbarg: Fabrication of BESOI-Materials Using Implanted Nitrogen as an Effective Etch Stop Barrier, 1989 IEEE SOS/SOI Technology Conference, pp. 64–65 (Stateline, NV, USA, October 3–5, 1989)
480. V. Lehmann, K. Mitani, D. Feijoo, U. Gosele: Implanted carbon: An effective etch-stop in silicon, J. Electrochem. Soc. 138(5), L3–L4 (1991)
481. S.S. Wang, V.M. McNeil, M.A. Schmidt: An etch-stop utilizing selective etching of N-Type silicon by pulsed potential anodization, J. Microelectromech. Syst. 1(4), 187–192 (1992)
482. J.W. Faust Jr, E.D. Palik: Study of the orientation dependent etching and initial anodization of si in aqueous KOH, J. Electrochem. Soc. 130(6), 1413–1420 (1983)
483. T.N. Jackson, M.A. Tischler, K.D. Wise: An electrochemical p-n junction etch-stop for the formation of silicon microstructures, IEEE Electron Device Lett. EDL-2(2), 44–45 (1981)
484. R.L. Meek: Electrochemically thinned N/N+ epitaxial silicon – Method and applications, J. Electrochem. Soc. 118(7), 1240–1246 (1971)
485. H.J.A. van Dijk, J. de Jonge: Preparation of thin silicon crystals by electrochemical thinning of epitaxially grown structures, J. Electrochem. Soc. 117(4), 554–554 (1970)
486. M.J.J. Theunissen, J.A. Appels, W.H.C.G. Verkuylen: Application of preferential electrochemical etching of silicon to semiconductor device technology, J. Electrochem. Soc. 117(7), 959–965 (1970)
487. C.J.M. Eijkel, J. Branebjerg, M. Elwenspoek, F.C.M. van de Pol: A new technology for micromachining of silicon: Dopant selective HF anodic etching for the realization of low-doped monocrystalline silicon structures, IEEE Electron Device Lett. 11(12), 588–589 (1990)
488. C.P. Wen, K.P. Weller: Preferential electrochemical etching of P+ silicon in an aqueous HF-H_2SO_4 electrolyte, J. Electrochem. Soc. 119(4), 547–548 (1972)
489. Y. Linden, L. Tenerz, J. Tiren, B. Hok: Fabrication of three-dimensional silicon structures by means of doping-selective etching (DSE), Sens. Actuators 16, 67–82 (1989)

490. B. Kloeck, S.D. Collins, N.F. De Rooij, R.L. Smith: Study of electrochemical etch-stop for high-precision thickness control of silicon membranes, IEEE Trans. Electron Dev. 36(4), 663–669 (1989)
491. R.L. Smith, B. Kloeck, N. De Rooij, S.D. Collins: The potential dependence of silicon anisotropic etching in KOH at 60C, J. Electroanal. Chem. 238, 103–113 (1987)
492. K.J. Ma, K. Najafi: A New Capacitive Electro-Chemical Etch-Stop Technique, 1994 IEEE Micro Electro Mechanical Systems, MEMS '94, pp. 158–163 (Oiso, Japan, January 25–28, 1994)
493. L. Smith, A. Soderbarg: Electrochemical etch stop obtained by accumulation of free carriers without p-n junction, J. Electrochem. Soc. 140(1), 271–275 (1993)
494. M.K. Andrews, G.C. Turner: bipolar effects in the fabrication of silicon membranes by the anodic etch stop, Sens. Actuators A 29, 49–57 (1991)
495. M. Hirata, K. Suzuki, H. Tanigawa: Silicon diaphragm pressure sensors fabricated by anodic oxidation etch-stop, Sens. Actuators 13, 63–70 (1988)
496. M. Hirata, S. Suwazono, H. Tanigawa: Diaphragm thickness control in silicon pressure sensors using an anodic oxidation etch-stop, J. Electrochem. Soc. 134(8), 2037–2041 (1987)
497. C.M.A. Ashruf, P.J. French, P.M.M.C. Bressers, P.M. Sarro, J.J. Kelly: A new contactless electrochemical etch-stop based on a gold/silicon/TMAH galvanic cell, Sens. Actuators A 66, 284–291 (1998)
498. P.J. French, M. Nagao, M. Esashi: Electrochemical etch-stop in TMAH without externally applied bias, Sens. Actuators A 56, 279–280 (1996)
499. C.M.A. Ashruf, P.J. French, P.M. Sarro, R. Kazinczi, X.H. Xia, J.J. Kelly: Galvanic etching for sensor fabrication, J. Micromech. Microeng. 10, 505–515 (2000)
500. M.C. Acero, J. Esteve, C. Burrer, A. Gotz: Electrochemical etch-stop characteristics of TMAH:IPA solutions, Sens. Actuators A 46–47, 22–26 (1995)
501. S.A. Campbell, H.J. Lewerenz (Eds.): Semiconductor Micromachining, vol. 2, Chapter 2 (Wiley, Chichester, 1998)
502. H. Nielsen, D. Hackleman: Some illumination on the mechanism of SiO_2 etching in HF solutions, J. Electrochem. Soc. 130(3), 708–712 (1983)
503. T. Yoshida, T. Kudo, K. Ikeda: Photo-Induced Preferential Anodization for Fabrication of Monocrystalline Micromechanical Structures, Proceedings of MEMS '92, pp. 56–61 (Travemunde, Germany, February 4–7, 1992)
504. E. Peeters, D. Lapadatu, R. Puers, W. Sansen: PHET, an electrodeless photovoltaic electrochemical etchstop technique, J. Microelectromech. Syst. 3(3), 113–123 (1994)
505. R.W. Ade, E.E. Harstead, A.H. Amirfazli, T. Cacouris, E.R. Fossum, P.R. Prucnal, R.M. Osgood Jr: Silicon photodetector structure for direct coupling of optical fibers to integrated circuits, IEEE Trans. Electron Devices, ED-34(6), 1283–1289 (1987)
506. L. Tenerz, B. Hok: Micromachining of three-dimensional silicon structures using photoelectrochemical etching, Electron. Lett. 21(25–26), 1207–1209 (1985)
507. M. Garin, T. Trifonov, A. Rodriguez, L.F. Marsal, R. Alcubilla: Optical PRoperties of 3D macroporous silicon structures, Mater. Sci. Eng. B 149, 275–280 (2008)
508. J. Schilling, F. Muller, S. Matthias, R.B. Wehrspohn, U. Gosele: Three-dimensional photonic crystals based on macroporous silicon with modulated pore diameter, Appl. Phys. Lett. 78(9), 1180–1182 (2001)
509. R. Mlcak, H.L. Tuller, P. Greiff, J. Sohn: Photo-Assisted Electrochemical Machining of Micromechanical Structures, Proceedings of MEMS '93, pp. 225–229 (Fort Lauderdale, FL, February 7–10, 1993)
510. R. Mlcak, H.L. Tuller, P. Greiff, J. Sohn, L. Niles: Photoassisted electrochemical micromachining of silicon in hf electrolytes, Sens. Actuators A 40, 49–55 (1994)
511. E.H. Klaassen, R.J. Reay, C. Storment, G.T. A. Kovacs: Micromachined thermally isolated circuits, Sens. Actuators A 58, 43–50 (1997)
512. K. Biswas, S. Kal: Etch characteristics of KOH, TMAH and dual doped TMAH for bulk micromachining of silicon, Microelectron. J. 37, 519–525 (2006)

513. A.E.T. Kuiper, E.G.C. Lathouwers: room-temperature HF vapor-phase cleaning for low-pressure chemical vapor deposition of epitaxial Si and SiGe layers, J. Electrochem. Soc. 139(9), 2594–2599 (1992)
514. E. Hoffman, B. Warneke, E. Kruglick, J. Weigold, K.S.J. Pister: 3D Structures with Piezoresistive Sensors in Standard CMOS, 1995 IEEE Micro Electro Mechanical Systems, MEMS '95, pp. 288–293 (Amsterdam, January 29 – February 2, 1995)
515. P.B. Chu, J.T. Chen, R. Yeh, G. Lin, J.C.P. Huang, B.A. Warneke, S.J. Pister: Controlled pulse-etching with xenon difluoride, 1997 International Conference on Solid-State Sensors and Actuators, Transducers '97, pp. 665–668 (Chicago, IL, June 16–19, 1997)
516. K. Hamaguchi, T. Tsuchiya, K. Shimaoka, H. Funabashi: 3-nm gap fabrication using gas phase sacrificial etching for quantum devices, 2004 IEEE Micro Electro Mechanical Systems, MEMS 2004, pp. 418–421 (Maastricht, The Netherlands, Jan 25–29, 2004)
517. J.D. Brazzle, M.R. Dokmeci, C.H. Mastrangelo: Modeling and characterization of sacrificial polysilicon etching using vapor-phase xenon difluoride, 2004 IEEE Micro Electro Mechanical Systems, MEMS 2004, pp. 737–740 (Maastricht, The Netherlands, Jan 25–29, 2004)
518. G. Xuan, T.N. Adam, J. Suehle, E. Fitzgerald, P.Lv,N. Sustersic, M.J. Coppinger, J. Kolodzey: Xenon difluoride dry etching of Si, SiGe alloy and Ge, 2006 International SiGe Technology and Device Meeting, pp. 142–143 (Princeton, NJ, October 30, 2006)
519. T. Zhu, P. Argyrakis, E. Mastropaolo, K.K. Lee, R. Cheung: Dry etch release processes for micromachining applications, J. Vac. Sci. Technol. B 25(6), 2553–2557 (2007)
520. F. Ayazi, K. Najafi: High-Aspect-Ratio Dry-Release Poly-Silicon MEMS Technology for Inertial-Grade Microgyroscopes, IEEE Position Location and Navigation Symposium, pp. 304–308 (San Diego, CA, March 13–16, 2000)
521. P.F. Van Kessel, L. Hornbeck, R.E. Meier, M.R. Douglass: A MEMS-based projection display, Proc. IEEE 86(8), 1687–1704 (1998)
522. C.W. Storment, D.A. Borkholder, V. Westerlind, J.W. Suh, N.I. Maluf, G.T.A. Kovacs: Flexible, dry-released process for aluminum electrostatic actuators, J. Microelectromech. Syst. 3(3), 90–96 (1994)
523. D.W. Burns: unpublished result
524. R.T. Howe, R.S. Muller: Polycrystalline silicon micromechanical beams, J. Electrochem. Soc. 130(6), 1420–1423 (1983)
525. H. Guckel, D.W. Burns: Planar Processed Polysilicon Sealed Cavities for Pressure Transducer Arrays, 1984 International Electron Devices Meeting, vol. 30, pp. 223–225 (San Francisco, CA, December, 1984)
526. D.J. Monk, D.S. Soane, R.T. Howe: Hydrofluoric acid etching of silicon dioxide sacrificial layers I. Experimental observations, J. Electrochem. Soc. 141(1), 264–269 (1994)
527. D.J. Monk, D.S. Soane, R.T. Howe: Hydrofluoric acid etching of silicon dioxide sacrificial layers II. Modeling, J. Electrochem. Soc. 141(1), 270–274 (1994)
528. S.-J. Lee, S.-Y. Roh, C.-J. Kim: A New sacrificial layer improving the structural characteristics of micro electromechanical systems, J. Korean Phys. Soc. 32(5), 731–734 (1998)
529. J. Anguita, F. Briones: HF/H2O vapor etching of SiO_2 sacrificial layer for large-area surface-micromachined membranes, Sens. Actuators A 64, 247–251 (1998)
530. H. Cao, R.J. Weber: Vapor HF Sacrificial Etching for Phosphorus Doped Polycrystalline Silicon Membrane Structures, IEEE International Conference on Electro/Information Technology, EIT, pp. 289–293 (Ames, IA, USA, May 18–20, 2008)
531. A. Witvrouw, B. Du Bois, P. De Moor, A. Verbist, C. Van Hoof, H. Bender, C. Baert: A comparison between wet HF etching and vapor HF etching for sacrificial oxide removal, Proc. SPIE, 4174, 130–141 (2000)
532. K. Hjort: Sacrificial etching of III-V compounds for micromechanical devices, J. Micromech. Microeng. 6, 370–375 (1996)

533. M.Y. Sim, S. Gleixner: Studying the Etch Rates and Selectivity of SiO_2 and Al in BHF Solutions, 16th Biennial University/Government/Industry Microelectronics Symposium, pp. 225–228 (San Jose, CA, June 25–28, 2006)
534. R. Lanz, P. Carazzetti, P. Muralt: Surface Micromachined BAW Resonators Based on AlN, IEEE Ultrasonics Symposium, pp. 981–983 (Munich, Germany, October 8–11, 2002)
535. A.E. Franke, D. Bilic, D.T. Chang, P.T. Jones, T.-J. King, R.T. Howe, G.C. Johnson: Post-CMOS Integration of Germanium Microstructures, 12th International Conference on Micro-Electro-Mechanical Systems MEMS '99, pp. 630–637 (Orlando, FL, January 17–21, 1999)
536. A. Maciossek, B. Lochel, H.-J. Quenzer, B. Wagner, S. Schulze, J. Noetzel: Galvanoplating and sacrificial layers for surface micromachining, Microelectron. Eng. 27, 503–508 (1995)
537. D.P. Kelly, M.W. Pruessner, K. Amarnath, M. Datta, S. Kanakaraju, L.C. Calhoun, R. Ghodssi: Monolithic suspended optical waveguides for InP MEMS, IEEE Photon. Technol. Lett. 16(5), 1298–1300 (2004)
538. A.B. Frazier, M.G. Allen: High Aspect Ratio Electroplated Microstructures Using a Photosensitive Polyimide Process, 1992 IEEE Micro Electro Mechanical Systems, MEMS '92, pp. 87–92 (Travemunde, Germany, February 4–7, 1992)
539. C.G. Keller, R.T. Howe: Nickel-Filled Hexsil Thermally Actuated Tweezers, 1995 International Conference on Solid-State Sensors and Actuators, Transducers '95, pp. 376–379 (Stockholm, Sweden, June 25–29, 1995)
540. Z. Cui, R.A. Lawes: A new sacrificial layer process for the fabrication of micromechanical systems, J. Micromech. Microeng. 7, 128–130 (1997)
541. H. Guckel, K.J. Skrobis, T.R. Christenson, J. Klein, S. Han, B. Choi, E.G. Lovell: Fabrication of Assembled Micromechanical Components via Deep X-Ray Lithography, 1991 IEEE Micro Electro Mechanical Systems, MEMS '91, pp. 74–79 (Nara, Japan, January 30 – February 2, 1991)
542. H. Guckel: High-aspect-ratio micromachining via deep x-ray lithography, Proc. IEEE 86(8), 1586–1593 (1998)
543. H. Guckel, T.R. Christenson, K.J. Skrobis, D.D. Denton, B. Choi, E.G. Lovell, J.W. Lee, S.S. Bajikar, T.W. Chapman: Deep X-Ray and UV Lithographies for Micromechanics, 4th IEEE Solid-State Sensor and Actuator Workshop, pp. 118–122 (Hilton Head Island, SC, June 4–7, 1990)
544. H. Guckel, K.J. Skrobis, T.R. Christenson, J. Klein: Micromechanics for actuators via deep x-ray lithography, Proc. SPIE 2194, 2–10 (1994)
545. X. Huang, G. Liu, X. Ying, J. Wang, Y. Guo, C. Kang, Y. Tian: Applications of thick sacrificial-layer of zinc in liga process, Microsyst. Technol. 14, 1257–1261 (2008)
546. S.D. Leith, D.T. Schwartz: In-situ fabrication of sacrificial layers in electrodeposited NiFe microstructures, J. Micromech. Microeng. 9, 97–104 (1999)
547. K.E. Petersen: Micromechanical light modulator array fabricated on silicon, Appl. Phys. Lett. 31(8), 521–523 (1977)
548. K. Walsh, J. Norville, Y.-C. Tai: Photoresist as a Sacrificial Layer by Dissolution in Acetone, 2001 IEEE Micro Electro Mechanical Systems, MEMS, pp. 114–117 (Interlaken, Sweden, January 21–25, 2001)
549. M.A. Schmidt, R.T. Howe, S.D. Senturia, J.H. Haritonidis: Design and calibration of a microfabricated floating-element shear-stress sensor, IEEE Trans. Electron Dev. 35(6), 750–757 (1988)
550. O. Paul, D. Westberg, M. Hornung, V. Ziebart, H. Baltes: Sacrificial Aluminum Etching for CMOS Microstructures, 1997 IEEE Micro Electro Mechanical Systems, MEMS '97, pp. 523–528 (Nagoya, Japan, January 26–30, 1997)
551. K. Suzuki, I. Shimoyama, H. Miura: Insect-model based microrobot with elastic hinges, J. Micromech. Syst. 3(1), 4–9 (1994)

552. C.E. White, T. Anderson, C.L. Henderson, H.D. Rowland, W.P. King: Microsystems manufacturing via embossing of photodefinable thermally sacrificial materials, Proc. SPIE 5374, 361–370 (2004)
553. S. Chang, W. Eaton, J. Fulmer, C. Gonzalez, B. Underwood, J. Wong, R.L. Smith: Micromechanical Structures in Amorphous Silicon, 1991 International Conference on Solid-State Sensors and Actuators, Transducers '91, pp. 751–754 (San Francisco, CA, June 24–27, 1991)
554. L.J. Spangler, K.D. Wise: A New Silicon-on-Glass Process for Integrated Sensors, IEEE Solid-State Sensor and Actuator Workshop, pp. 140–143 (Hilton Head Island, SC, June 6–9, 1988)
555. S.T. Cho: A batch dissolved wafer process for low cost sensor applications, Proc. SPIE 2639(10), 10–17 (1995)
556. T.E. Bell, P.T.J. Gennissen, D. DeMunter, M. Kuhl: Porous silicon as a sacrificial material, J. Micromech. Microeng. 6, 361–369 (1996)
557. P. Steiner, A. Richter, W. Lang: Using porous silicon as a sacrificial layer, J. Micromech. Microeng. 3, 32–36 (1993)
558. W. Lang, P. Steiner, A. Richter, K. Marusczyk, G. Weimann, H. Sandmaier: Application of porous silicon as a sacrificial layer, Sens. Actuators A 43, 239–242 (1994)
559. T. Bischoff, G. Muller, W. Welser, F. Koch: Frontside micromachining using porous-silicon sacrificial-layer technologies, Sens. Actuators A 60, 228–234 (1997)
560. B.L. Bircumshaw, M.L. Wasilik, E.B. Kim, Y.R. Su, H. Takeuchi, C.W. Low, G. Liu, A.P. Pisano, T.-J. King, R.T. Howe: Hydrogen Peroxide Etching and Stability of P-Type Poly-SiGe Films, 2004 IEEE Micro Electro Mechanical Systems, MEMS, pp. 514–519 (Maastricht, The Netherlands, January 25–29, 2004)
561. P.R. Scheeper, W. Olthuis, P. Bergveld: Fabrication of a Subminiature Silicon Condenser Microphone Using the Sacrificial Layer Technique, 1991 International Conference on Solid-State Sensors and Actuators, Transducers '91, pp. 408–411 (San Francisco, CA, June 24–27, 1991)
562. W. Kronast, B. Muller, W. Siedel, A. Stoffel: Single-chip condenser microphone using porous silicon as sacrificial layer for the air gap, Sens. Actuators A 87, 188–193 (2001)
563. A.H. Ma, S.-Ho Tsang, M. Parameswaran, A.M. Leung: Spin-On Glass as a Sacrificial Layer for Patterned Metallization of Compliant SU-8 Microstructures, Canadian Conference on Electrical and Computer Engineering, CCECE 2007, pp. 288–291 (Vancouver, BC, April 22–26, 2007)
564. V. Conedera, L. Salvagnac, N. Fabre, F. Zamkotsian, H. Camon: Surface micromachining technology with two SU-8 structural layers and sol-gel, SU-8 or SiO_2/sol-gel sacrificial layers, J. Micromech. Microeng. 17, N52–N57 (2007)
565. K. Yamada, T. Kuriyama: A New Modal Mode Controlling Method for a Surface Format Surrounding Mass Accelerometer, 1991 International Conference on Solid-State Sensors and Actuators, Transducers '91, pp. 655–658 (San Francisco, CA, June 24–27, 1991)
566. N.C. MacDonald, L.Y. Chen, J.J. Yao, Z.L. Zhang, J.A. McMillan, D.C. Thomas: Selective chemical vapor deposition of tungsten for microelectromechanical structures, Sens. Actuators 20, 123–133 (1989)
567. L.-Y. Chen, N.C. MacDonald: A Selective CVD Tungsten Process for Micromotors, 1991 International Conference on Solid-State Sensors and Actuators, Transducers '91, pp. 739–742 (San Francisco, CA, June 24–27, 1991)
568. J.C. North, T.E. McGahan, D.W. Rice, A.C. Adams: Tapered windows in phosphorus-doped SiO_2 by ion implantation, IEEE Trans. Electron Devices ED-25(7), 809–812 (1978)
569. J. Gotzlich, H. Ryssel: Tapered windows in SiO_2, Si_3N_4, and polysilicon layers by ion implantation, J. Electrochem. Soc. 128(3), 617–619 (1981)
570. A.S. Tenney, M. Ghezzo: Etch rates of doped oxides in solutions of buffered HF, J. Electrochem. Soc. 120(8), 1091–1095 (1973)

571. L.K. White: Bilayer taper etching of field oxides and passivation layers, J. Electrochem. Soc. 127(12), 2687–2693 (1980)
572. S. Sugiyama, T. Suzuki, K. Kawahata, K. Shimaoka, M. Takigawa, I. Igarashi: Micro-Diaphragm Pressure Sensor, International Electron Devices Meeting, pp. 184–187 (Los Angeles, CA, December 7–10, 1986)
573. C.H. Mastrangelo, C.H. Hsu: Mechanical stability and adhesion of microstructures under capillary forces-part i: basic theory, J. Microelectromech. Syst. 2(1), 33–43 (1993)
574. C.H. Mastrangelo, C.H. Hsu: Mechanical stability and adhesion of microstructures under capillary forces-part ii: experiments, J. Microelectromech. Syst. 2(1), 44–55 (1993)
575. R.C. Weast (Ed.): CRC Handbook of Chemistry and Physics, 60th edn. (CRC Press, Boca Raton, FL), 1979/1980
576. G.T. Mulhern, D.S. Soane, R.T. Howe: Supercritical Carbon Dioxide Drying of Microstructures, 1993 International Conference on Solid-State Sensors and Actuators, Transducers '93, pp. 296–299 (Yokohama, Japan, June 7–10, 1993)
577. C.W. Dyck, J.H. Smith, S.L. Miller, E.M. Russick, C.L.J. Adkins: Supercritical Carbon Dioxide Solvent Extraction from Surface-Micromachined Micromechanical Structures, SPIE Micromachining and Microfabrication (Austin, TX, October 14–15, 1996)
578. D.W. Burns: unpublished result (1988)
579. H. Guckel, J.J. Sniegowski, T.R. Christenson: Fabrication of micromechanical devices from polysilicon films with smooth surfaces, Sens.Actuators 20, 117–122 (1989)
580. N. Takeshima, K.J. Gabriel, M. Ozaki, J. Takahashi, H. Horiguchi, H. Fujita: Electrostatic Parallelgram Actuators, 1991 International Conference on Solid-State Sensors and Actuators, Transducers '91, pp. 63–66 (San Francisco, CA, June 24–27, 1991)
581. R. Legtenberg, H.A.C. Tilmans: Electrostatically driven vacuum-encapsulated polysilicon resonators: Part I. Design and fabrication, Sens. Actuators A 45, 57–66 (1994)
582. J.Y. Kim, C.-J. Kim: Comparative Study of Various Release Methods for Polysilicon Surface Micromachining, 1997 IEEE Micro Electro Mechanical Systems, MEMS '97, pp. 442–447 (Nagoya, Japan, January 26–30, 1997)
583. L. Alley, G.J. Cuan, R.T. Howe, K. Komvopoulos: The Effect of Release-Etch Processing on Surface Microstructure Stiction, Technical Digest of the 5th Solid-State Sensor and Actuator Workshop, pp. 202–207 (Hilton Head Island, SC, USA, June 22–25, 1992)
584. W.R. Ashurst, C. Yau, C. Carraro, C. Lee, G.J. Kluth, R.T. Howe, R. Maboudian: Alkene based monolayer films as anti-stiction coatings for polysilicon MEMS, Sens. Actuators A 91, 239–248 (2001)
585. U. Srinivasan, M.R. Houston, R.T. Howe, R. Maboudian: Alkyltrichlorosilane-based self-assembled monolayer films for stiction reduction in silicon micromachines, J. Microelectromech. Syst. 7(2), 252–260 (1998)
586. B.H. Kim, T.D. Chung, C.H. Oh, K. Chun: A new organic modifier for anti-stiction, J. Microelectromech. Syst. 10(1), 33–40 (2001)
587. W.R. Ashurst, C. Carraro, R. Maboudian, W. Frey: Wafer level anti-stiction coatings for MEMS, Sens. Actuators A 104, 213–221 (2003)
588. J.R. Martin: Process for Wafer Level Treatment to Reduce Stiction and Passivate Micromachined Surfaces and Compounds Used Therefor, U.S. Patent No. 7,364,942 (2008)
589. M. Ito, K. Yamagata, H. Miyabayashi, T. Yonehara: Scalability Potential in ELTRAN® SOI-Epi Wafer, IEEE International SOI Conference, pp. 10–11 (Wakefield, MA, USA, October 2–5, 2000)
590. T. Yonehara, K. Sakaguchi, N. Sato: Epitaxial layer transfer by bond and etch back of porous Si, Appl. Phys. Lett. 64(16), 2108–2110 (1994)
591. G. Barillaro, A. Nannini, M. Piotto: Electrochemical etching in HF solutions for silicon micromachining, Sens. Actuators A 102, 195–201 (2002)
592. H. Foll, M. Christophersen, J. Carstensen, G. Hasse: Formation and application of porous silicon, Mater. Sci. Eng. R, 39, 93–141 (2002)

593. V. Lehmann: Porous silicon – A new material for MEMS, 1996 IEEE Micro Electro Mechanical Systems, MEMS ′96, pp. 1–6, (San Diego, CA, Feb. 11–15, 1996)
594. V. Lehmann: The physics of macropore formation in low doped n-type silicon, J. Electrochem. Soc. 140(10), 2836–2843 (1993)
595. P. Steiner, W. Lang: Micromachining applications of porous silicon, Thin Solid Films 225, 52–58 (1995)
596. P.A. Kohl, F.W. Ostermayer Jr: Photoelectrochemical methods for III-V compound semiconductor device processing, Ann. Rev. Mater. Sci. 19, 379–399 (1989)
597. C. Levy-Clement, A. Lagoubi, M. Tomkiewicz: Morphology of porous n-type silicon obtained by photoelectrochemical etching I. Correleations with material and etching parameters, J. Electrochem. Soc. 141(4), 958–967 (1994)
598. R.L. Smith, S.D. Collins: Porous silicon formation mechanisms, J. Appl. Phys. 71(8), R1–R22 (1992)
599. D.R. Turner: Electropolishing silicon in hydrofluoric acid solutions, J. Electrochem. Soc. 105(7), 402–408 (1958)
600. S.S. Tsao, T.R. Guilinger, M.J. Kelly, P.J. Clews: Multilevel porous silicon formation, J. Electrochem. Soc. 136(2), 586–587 (1989)
601. H. Takai, T. Itoh: Isolation of silicon film grown on porous silicon layer, J. Electron. Mater. 12(6), 973–982 (1983)
602. A. Richter, P. Steiner, F. Kozlowski, W. Lang: Current-induced light emission from a porous silicon device, IEEE Electron Device Lett. 12(12), 691–692 (1991)
603. V. Lehmann: The physics of macroporous silicon formation, Thin Solid Films 255, 1–4 (1995)
604. R.W. Fathauer, T. George, A. Ksendzov, R.P. Vasquez: Visible luminescence from silicon wafers subjected to stain etches, Appl. Phys. Lett. 60(8), 995–997 (1992)
605. S. Liu, C. Palsule, S. Yi, S. Gangopadhyay: Characterization of stain-etched porous silicon, Phys. Rev. B 49(15), 10318–10325 (1994)
606. K. Imai, H. Unno: FIPOS (Full Isolation by Porous Oxidized Silicon) technology and its application to LSI's, IEEE Trans. Electron Devices ED-31(3), 297–302 (1984)
607. F. Beck: Integrated Circuit Failure Analysis, A Guide to Preparation Techniques, Chapters 3, 6 (Wiley, Chichester, 1998)
608. C.A. Harper (Ed.): Handbook of Materials and Processes for Electronics, Chapter 7 (McGraw-Hill, New York, NY, 1970)
609. W.R. Runyan, T.J. Shaffner: Semiconductor Measurements and Instrumentation, 2nd edn, Chapters 2, 9 (McGraw-Hill, New York, NY, 1998)
610. K.R. Williams: Silicon Preferential (Defect Delineation) Etch Rates, In R. Hull (Ed.), Properties of Crystalline Silicon, Chapter 16.3 (INSPEC, London, 1999)
611. W.R. Runyan, T.J. Shaffner: Semiconductor Measurements and Instrumentation, 2nd edn., Chapter 2 (McGraw-Hill, New York, NY 1998)
612. S.A. Campbell, H.J. Lewerenz (Eds.): Semiconductor Micromachining, vol. 2, Chapter 10 (Wiley, Chichester, 1998)
613. W.R. Runyan, T.J. Shaffner: Semiconductor Measurements and Instrumentation, 2nd edn., Chapter 9 (McGraw-Hill, New York, NY, 1998)
614. T.L. Chu, J.R. Gavaler: Stacking faults in vapor grown silicon, J. Electrochem. Soc. 110(5), 388–393 (1963)
615. W.C. Dash: Copper precipitation on dislocations in silicon, J. Appl. Phys. 27(10), 1193–1195 (1956)
616. H. Robbins: Junction delineation in silicon, J. Electrochem. Soc. 109(1), 63–64 (1962)
617. C.S. Fuller, J.A. Ditzenberger: Diffusion of donor and acceptor elements in silicon, J. Appl. Phys. 27(5), (1956)544–553
618. P.J. Whoriskey: Two chemical stains for marking p-n junctions in silicon, J. Appl. Phys. 29(5), 867–868 (1958)

619. C.P. Wu, E.C. Douglas, C.W. Mueller, R. Williams: Techniques for lapping and staining ion-implanted layers, J. Electrochem. Soc. 126(11), 1982–1988 (1979)
620. T. Mills, E.W. Sponheimer: Precision VLSI Cross Sectioning and Staining, Proceedings of 20th Annual Reliability Physics Symposium, pp. 214–220 (San Diego, CA, March 30–31, 1982)
621. B.L. Sopori: A new defect etch for polycrystalline silicon, J. Electrochem. Soc. 131(3), 667–672 (1984)
622. D.G. Schimmel: Defect etch for <100> silicon evaluation, J. Electrochem. Soc. 126(3), 479–483 (1979)
623. V.D. Archer: Methods for defect evaluation of thin <100> oriented silicon epitaxial layers using a wet chemical etch, J. Electrochem. Soc. 129(9), 2074–2076 (1982)
624. K.H. Yang: An etch for delineation of defects in silicon, J. Electrochem. Soc. 131(5), 1140–1145 (1984)
625. M. Wright Jenkins: A new preferential etch for defects in silicon crystals, J. Electrochem. Soc. 124(5), (1977)757–762
626. Transene Company, Inc., Danvers, MA 01923: Wright Etchant, http://www.transene.com/wright.html, accessed December 24, 2010
627. T.C. Chandler: MEMC Etch – A chromium trioxide-free replacement for delineating dislocations and slip in silicon, J. Electrochem. Soc. 137(3), 944–948 (1990)
628. F. Secco d' Aragona: Dislocation etch for (100) planes in silicon, J. Electrochem. Soc. 119(7), 948–951 (1972)
629. R.T. Howe, R.S. Muller: Polycrystalline and amorphous silicon micromechanical beams – Annealing and mechanical properties, Sens. Actuators 4, 447–454 (1983)
630. W.A. Pliskin, R.P. Gnall: Evidence for oxidation growth at the oxide-silicon interface from controlled etch studies, J. Electrochem. Soc. 111(7), 872–873 (1964)
631. H. Baltes, O. Brand, G.K. Fedder, C. Hierold, J. Korvink, O. Tabata (Eds.): Advanced Micro and Nanosystems, vol. 2, CMOS-MEMS (Wiley-VCH, Weinheim, 2005)

Chapter 9
MEMS Lithography and Micromachining Techniques

Daniel R. Hines, Nathan P. Siwak, Lance A. Mosher, and Reza Ghodssi

Abstract Photolithography is a patterning process that uses light to transfer a pattern from a mask to a photosensitive polymer layer. The resulting pattern can either be etched into the underlying surface or used to define the patterning of a layer deposited onto the masked surface. This is essentially a two-dimensional process that can be repeated numerous times to fabricate various structures and devices. A classic use of these techniques is the fabrication of transistors on a silicon substrate as practiced in the semiconductor industry. Development over a number of years has yielded optimization of processing conditions, equipment, and materials to achieve ever smaller sized features and an increased density of integration. In the effort to fabricate even smaller (submicron to nanometer) features, other fabrication methods have also been developed such as electron beam lithography, focused ion beam lithography, and nanoimprint lithography. This chapter presents an introduction and practical approach to lithography and micromachining techniques in the context of MEMS device fabrication. The topics that are discussed here include: UV lithography, grayscale lithography, e-beam lithography, X-ray lithography, direct-write lithographies and imprint lithographies. A detailed description including highlighted examples of each of these lithographic techniques is presented in this chapter. At the end of the chapter a compilation of hands-on case studies is presented to assist readers in implementing these techniques in their own laboratories and developing custom fabrication capabilities that fulfill their own unique requirements.

9.1 Overview

Photolithography as it is practiced today in the semiconductor and MEMS industries employs a light source, an optical projection system (stepper), a mask, and a photoresist film coating the surface of a substrate into which a desired pattern is to

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be transferred. Typically the patterning of the photoresist layer is not the desired end result but rather the means by which the entire surface of the desired substrate can be patterned in a parallel fashion. The advancements in resolution of the photolithographic process have been a primary driving force behind the increased device density on IC chips that has been empirically predicted by Moore's law [1]. The combination of smaller wavelength light sources, improvements in optical projection systems and highly engineered chemistry of photoresists [2–8] have led to rapid advances in chip design to the point where the modern era has seen entire music collections replaced by a single iPod^{TM} handheld device and the prevalence of cell phones in modern culture. Today we can carry around laptop computers that operate at 2 GHz, have hundreds of GBs of storage capacity, are approximately 1 in. thick, and weigh only a few pounds!

In 1957 Jay Lathrop and James Nall of the U.S. Army's Diamond Ordnance Fuse Laboratory in Maryland patented a photolithographic technique used to deposit thin-film metal strips approximately 200 μm wide to connect discrete transistors on a ceramic substrate. In 1958, Jay Last and Robert Noyce at Fairchild Semiconductor built one of the first optical projection systems and used it to make many identical transistors on a single Si wafer. In 1954, Bell Labs developed and combined the primary fabrication procedures associated with oxidation, photomasking, etching, and diffusion processes that underlie IC production to this day. The first monolithic integrated circuits developed in the late 1950s contained only a small (∼10) number of electrical components. An example of a circa 1961 integrated circuit containing four transistors and five resistors is shown in the left panel of Fig. 9.1. In contrast,

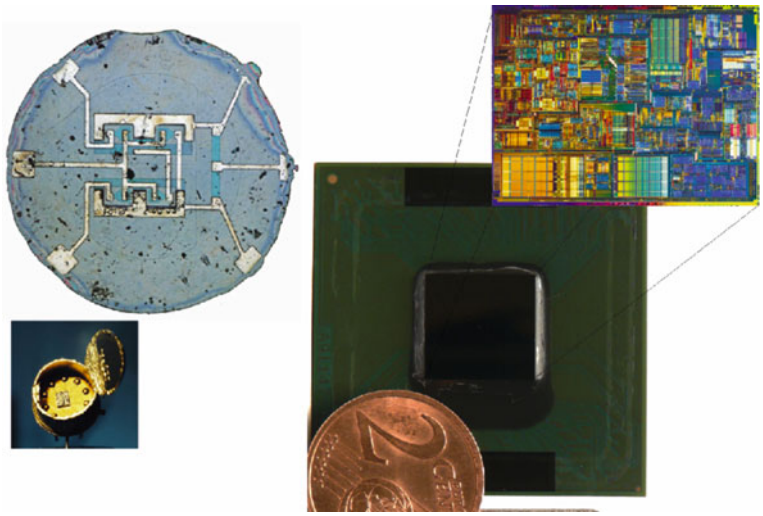

Fig. 9.1 *Left*, *top*; images of a circa 1961 integrated circuit from Fairchild Semiconductor containing four transistors and five resistors. *Left*, *bottom*; image of a typical packaged IC chip with the top cut open. *Right*; images of an Intel Pentium4 processor containing approximately 55 million transistors

development of lithography techniques has led to microprocessors with approximately 55 million transistors, as in the Intel Pentium4 processor (2001) shown in the right panel of Fig. 9.1.

The same basic fabrication processes developed by the semiconductor industry for the fabrication of IC chips are also used in the MEMS industry, and although fabrication of devices within the MEMS community draws directly from these lithographic techniques, MEMS requirements demand the development of processing capabilities that go beyond those employed for IC chip fabrication [9, 10]. For example, in MEMS devices, it may be desirable to pattern polymeric (or elastomeric) materials to create flow channels rather than passivation layers, introducing different materials into the fabrication process, as well as additional material functionality. Also employed are silicon-on-insulator wafers which can be used to create freely moving structures (such as gears) or mechanical members that are only partially attached to the underlying substrate (such as cantilevers and microbeams) rather than monolithic Si transistors. Using similar materials to produce different components often requires modified, if not dramatically different, processing steps. Beyond conventional lithographic fabrication, there are emerging fields of soft lithography [11–21] and related printing techniques that show great promise for MEMS fabrication. Many of these techniques have been developed as procedures for patterning and processing unconventional materials such as organic thin-films, polymeric substrates and dielectric layers, 3-D structures produced by combining molding and sintering processes, inkjet printing of active or structural materials, and so on. These unconventional fabrication methods have the potential to drastically change the way electronics and MEMS devices are fabricated and open new possibilities for device applications that never existed before.

Photolithography, although not the only one, is by far the most developed patterning method available for the fabrication of MEMS devices. The process, with the main components illustrated in Fig. 9.2, is described in detail in Section 9.2.

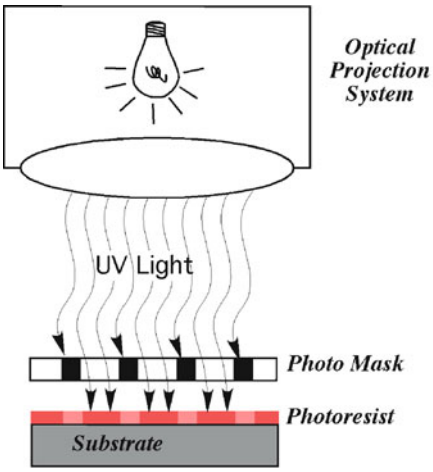

Fig. 9.2 Common components in a photolithography system

Briefly, UV light is used to create a pattern of open areas in a polymer film called photoresist. Material is then either added to or removed from these open areas. The desired patterns are first designed as opaque and transparent regions on a glass plate called a photomask. The photomask is mounted into an optical projection system where an image of the mask is focused onto a semiconductor wafer coated with photoresist. After exposure, the photoresist layer is developed to reveal the photomask pattern transferred into the photoresist. Both the optical projection system and photoresist chemistry are highly engineered to achieve high resolution and high repeatability within the photolithographic process.

For standard photolithography, the photomasks and photoresist chemistry are both designed to produce 2-D patterns within the photoresist film. However, the photomask can be modified to transmit different intensities of UV light. This is accomplished by using closely spaced pixels rather than fully opaque and/or transparent areas, or by using variably transmissive mask media. The limitations on pixel dimensions imposed by mask manufacturing and the resolution of optical projection systems, as well as the variable optical absorbance of mask media give rise to specific transmission intensities referred to as gray levels. These gray levels can be used to structure the thickness profile of a photoresist layer. Given appropriate etch parameters, this process of grayscale lithography (Section 9.3) can be used to create 3-D structures on a substrate surface.

UV light is not the only energy source that can be used to change the solubility of regions within a polymer film. For example, the solubility of PMMA can be dramatically changed by exposure to electrons and X-rays [7]. Both electrons and X-rays have shorter wavelengths than UV light and so can achieve higher resolution patterns. The main difference between UV lithography and both e-beam and X-ray lithographies is simply in the light source and method used for exposure.

For e-beam lithography (Section 9.5.1) the "light source" is essentially an SEM that has been modified to switch the electron beam on and off as it is scanned. Using a scanned electron beam, the resolution of e-beam lithography is greater than that of UV lithography. However, a disadvantage is that the exposure now involves a high vacuum system and is a serial rather than a parallel process, as in wide-area exposure or projection. The electron beam has to be moved point-by-point across the area to be exposed rather than all points exposed simultaneously, such a direct-write approach will drastically increase the time to expose a pattern. For applications that require massive parallelism and mass production, this can be problematic.

In the case of X-ray lithography (Section 9.4), the light source is typically a synchrotron, and wafers are exposed similarly to a contact projection system analogous with UV lithography. The advantage of X-ray lithography is the extremely high aspect ratio and near vertical sidewalls that can be patterned into the photoresist. Disadvantages include the need for exposures to be performed at a synchrotron, cost and difficulty of X-ray mask production, and the low sensitivity of resists to X-rays thus demanding long exposure times.

UV light, electrons, and X-rays can all be used to modify chemical bonds within a polymer film but do not have enough energy to remove material directly from a substrate surface. For these energy sources, a photoresist layer can be patterned

by changing the chemistry of the film (i.e., solubility) but the substrate cannot be patterned directly. By contrast, ion beams are energetic enough to remove atoms directly from a substrate surface. Focused ion beam lithography (FIB; Section 9.5.2) can be used to directly pattern a substrate surface without the need for a photoresist layer. Here, substrate atoms are physically removed by a process called sputtering. Both electron and ion beams can be used to modify the chemistry of a gas introduced above the substrate such that the resulting gas molecules are either deposited onto the substrate or chemically bonded with substrate atoms to form volatile compounds that are easily removed from the substrate. In this way, both electron and ion beam lithography can be performed directly on a substrate surface.

Of specific interest for MEMS applications is the ability to utilize direct-write methods to fabricate 3-D mechanical structures onto a substrate. At the nanoscale, material can be added to a substrate by coating an AFM tip with a specific molecule and then dragging the tip across the substrate. Thus with dip-pen lithography (Section 9.5.4) molecules get pulled off the tip to form a line on the substrate, much like a nanoscale fountain pen. On a larger scale, laser beams can be used to transfer materials from one substrate to a second substrate. This is performed by depositing a desired material over a sacrificial layer on the first substrate. A laser beam is then used to vaporize the sacrificial layer thus removing the desired materials from the first substrate and transferring it over to the second substrate. Laser beams can also be used to polymerize precursor polymer solutions.

Stereolithography (Section 9.5.6) can be performed by submerging a substrate into a precursor polymer solution and moving the laser beam and stage in a predetermined pattern to produce a 3-D polymerized structure attached to the substrate.

Printing techniques can also be used to fabricate MEMS components. Inkjet printers (Section 9.6.1) were first designed to deposit high-contrast, passive inks onto a substrate (paper) in a step-by-step fashion. Pressure pulses are used to force ink through small holes in the printing head. New inks are being designed that allow the printing of 3-D structures made from polymers, metal nanoparticles, organic molecules, and the like [22–24].

Other forms of printing such as soft lithography and nanoimprint lithography are being used to pattern films on substrate surfaces. Soft lithography (Section 9.6.2) uses a PDMS stamp coated with a specific molecule. The stamp is brought into contact with the substrate resulting in some or all of the film coating the PDMS stamp to be inked onto the substrate. Nanoimprint lithography (NIL; Section 9.6.3) creates a pattern in a resist layer by direct contact with a templated surface. The resulting pattern in the resist layer is similar to that produced by UV lithography, however, NIL can achieve pattern resolution in the tens of nm.

The last printing method to be discussed in this chapter is transfer printing (Section 9.6.4). This method can be used to directly assemble dissimilar materials onto a common substrate. The process relies on differential adhesion to transfer a patterned film from one substrate to a second substrate. As long as the adhesion is properly engineered, a wide variety of dissimilar materials can be sequentially assembled onto the same substrate to produce both electronic and mechanical

devices in ways that are difficult if not impossible to achieve using conventional lithographic processes.

This chapter begins by presenting a detailed discussion of conventional photolithography methods with an emphasis on MEMS processing. Related lithographic methods based on X-rays, electron beams, and ion beams are then presented. The chapter also covers fabrication processes developed more specifically for MEMS applications such as grayscale lithography and microstereolithography that are meant for fabricating 3-D structures. The chapter concludes with new, emerging fabrication techniques based on soft lithography and printing techniques that have only recently been considered and developed for MEMS processing applications.

9.2 UV Lithography

The concepts underlying photolithography are quite simple. The process uses a patterned mask comprised of transparent and opaque regions. Using an optical projection system, this pattern is illuminated onto a photosensitive film called a photoresist. When light strikes the photoresist, it causes a chemical change to take place within the photoresist film which in turn changes the ability of the photoresist to be dissolved by various solvents. This allows specific areas of the photoresist layer to be removed, which uncovers (exposes) the underlying substrate surface for further processing. The real advantage of the photolithographic process is that it can be performed over large areas at a very high resolution. The photolithographic process contains four main components (photomask, optical projection system, photoresist, and substrate) and can be described by a five-step process.

I. Deposit photoresist
II. Expose photoresist
III. Develop photoresist
IV. Transfer pattern
V. Remove photoresist

These steps are illustrated in Figs. 9.2 and 9.3 with each component and processing step labeled. Each of the four components and five processing steps is discussed in appropriate detail below. Specific examples relevant to MEMS processing are highlighted.

9.2.1 Photo Masks

Masks for photolithography are plates that contain transparent and opaque regions laid out to form a desired pattern [25]. These patterns contain microscopic features that form parts of electronic circuits or parts of MEMS devices. An example of a photomask is shown in Fig. 9.4. Typically the plate is either glass or quartz that has been designed for transparency in the UV and contains an opaque patterned

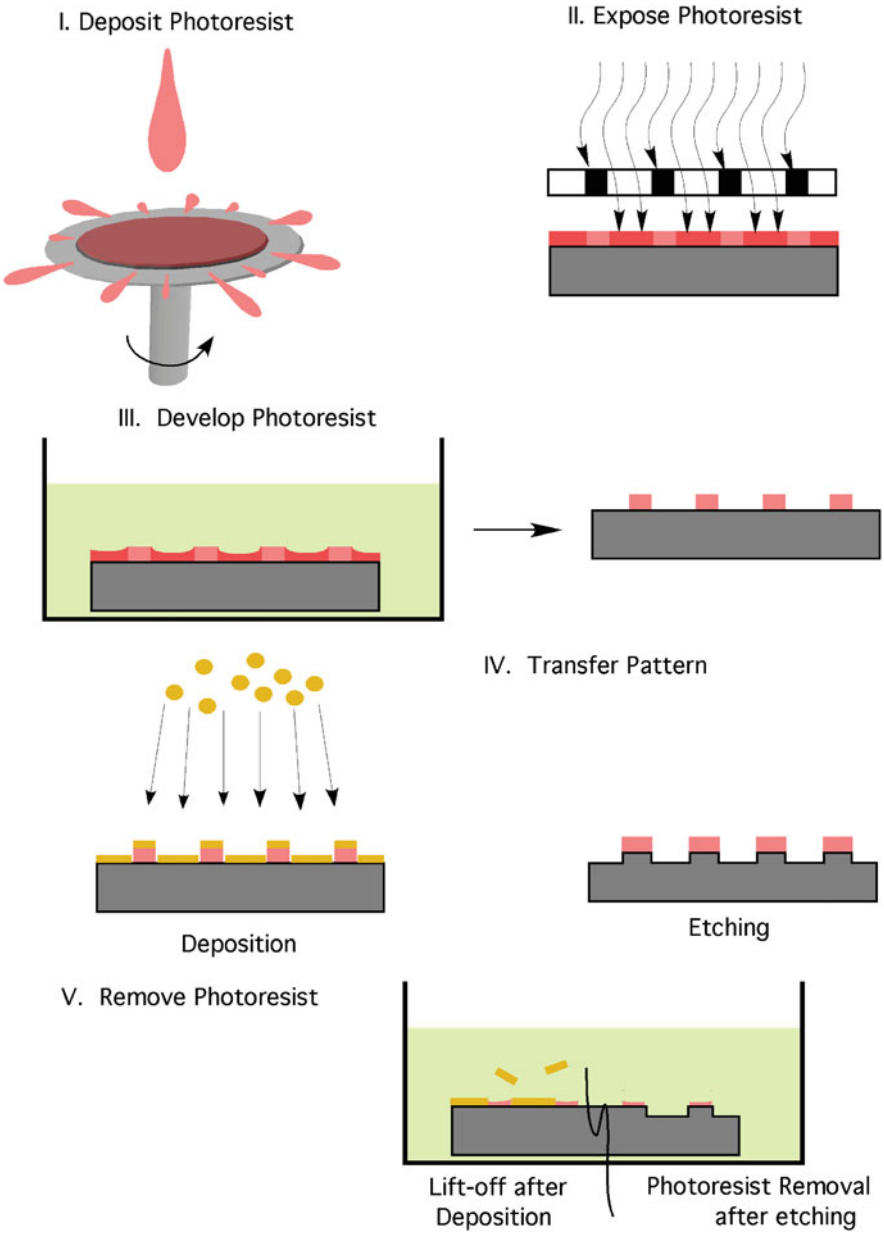

Fig. 9.3 Photolithography processing steps

metal film such as a typical 800 Å thick chromium layer on the top surface (much like a front surface mirror). Iron oxide is another common patterning material for photomasks. It has the advantage of being transparent in the visible while opaque in the UV, making it easier to align to previously patterned features in multilayer

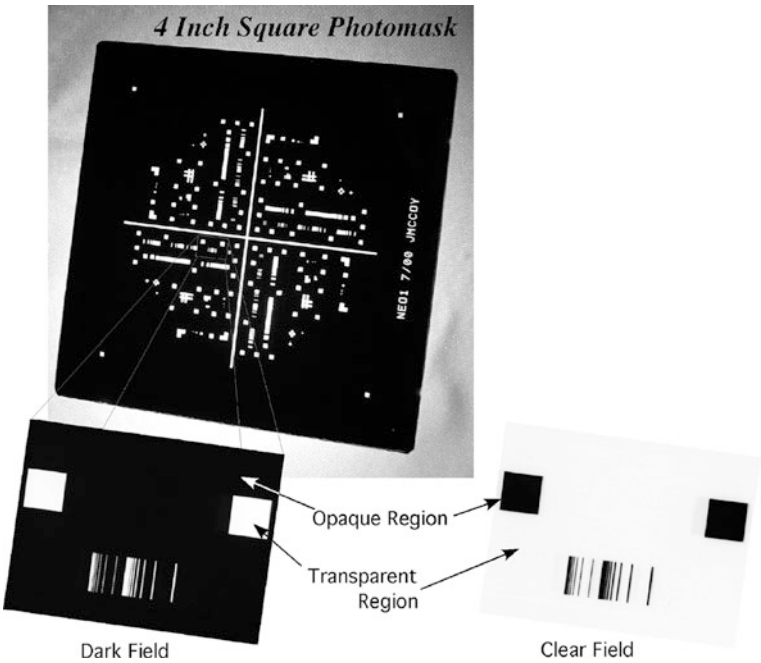

Fig. 9.4 Optical images of 4 in.^{2} square photomask. Magnified area represented in both clear field and dark field

lithography schemes where this is necessary. Photomasks can be designed for either clear field or dark field patterning as shown in the lower panels of Fig. 9.4. A dark field mask has the desired pattern contained in the transparent part of the mask whereas the clear field mask has the pattern contained in the opaque part of the mask.

For contact, soft-contact, and proximity lithography the mask is designed to produce a 1:1 image in the photoresist layer [26]. These masks come in contact or close contact (10–20 μm above the photoresist surface) with the photoresist layer and thus are susceptible to contamination and wear. A contact mask may need to be cleaned on a regular basis which exposes the surface to additional damage. Contact masks are mostly used for research and development and prototyping. For low-resolution processing, an inexpensive transparency mask can be made using a drawing program on the computer and a printer loaded with transparency film. Photomasks with resolution in the 30–40 μm range can be made using a professional graphics (>3000 dpi) quality printer. Standard laser printers (<1200 dpi) can achieve a reasonable resolution but cannot typically achieve the necessary level of opacity to print usable masks.

Projection lithography masks (often called reticles) are typically designed to produce 1:4, 1:5, or 1:10 reduced images in the photoresist layer. They are used with

an optical projection system where the image of the mask is projected onto the surface of the photoresist layer through a complex series of optics. Because projection masks do not come into contact with the photoresist layer, they are much less susceptible to wear or damage and therefore are more suitable for use in high-volume production facilities.

There are four variations of projection photomasks. The simplest type uses a combination of transparent and opaque regions to define a pattern that can be imaged onto a photoresist layer. The resolution of such a standard projection mask is diffraction-limited [27]. To overcome diffraction limitations by very closely spaced features, optical interference effects can be engineered into the mask. This can be accomplished by either changing the thickness of a transparent region of the mask (alternating phase-shift) [28] or by increasing the transmittance of the originally opaque region of the mask (attenuated phase-shift) [29]. Such phase-shift modifications in the transmitted light through a photomask cause either constructive or destructive interference patterns. With proper mask engineering of features on the photomask, the resulting light intensity pattern imaged into the photoresist layer can be of higher resolution than was achievable with a standard photomask as is illustrated in Fig. 9.5.

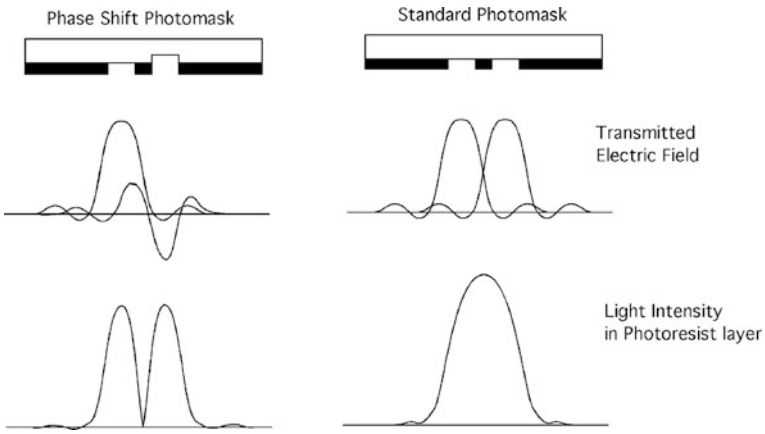

Fig. 9.5 Transmitted light intensity through (*left panel*) a phase shift photomask as compared to that for (*right panel*) a standard photomask (Modified from [30])

A standard projection photomask can be further modified by pixelating an originally opaque region of the mask. If the pixel size and spacing are below the resolution limit of the optical projection system then the pixelated region attenuates the intensity of the transmitted light without imaging individual pixels into the photoresist. These styles of masks are used for grayscale lithography. Due to mask fabrication limits and resolution limits of a given optical projection system, a finite number of discrete pixel sizes and spacings can be realized. Each discrete pixel size and spacing translates into a specific intensity of transmitted light from 100% (transparent region, no pixels) to 0% (opaque region). Each intensity level is referred to as

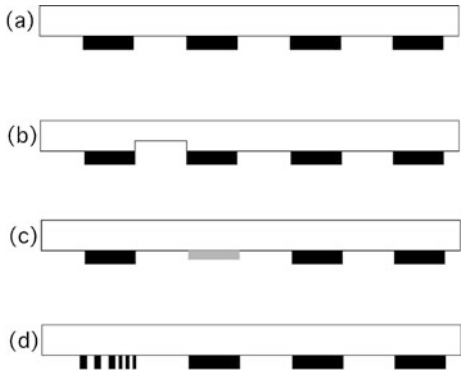

Fig. 9.6 Cross-section illustration of (**a**) standard projection photomask, (**b**) alternating phase-shift photomask, (**c**) attenuated phase-shift photomask, and (**d**) grayscale photomask

a gray-level. An illustration of the different types of projection photomasks is shown in Fig. 9.6.

Photomasks are typically made from soda-lime glass, borosilicate glass, or fused quartz. Thermal expansion and optical transmission are the primary considerations for choosing the mask material. Table 9.1 lists the thermal expansion coefficients for these materials. The transmission properties are shown in Fig. 9.7. The dimensions of soda-lime glass can change by 1.2 μm across a 5 in. mask for every 1°C change in temperature. However, for mask fabrication tools and steppers that are housed in a temperature-controlled environment, this is not typically a great concern and thus soda-lime glass can be used. For mask fabrication tools that use e-beam lithography, the mask is in a high vacuum environment, which can affect heat transfer. Therefore, borosilicate glass is more commonly used with these e-beam mask-writing tools. In UV lithography applications using wavelengths shorter than 350 nm, and for applications achieving very high resolution, quartz masks are needed due to thermal effects and transmissivity.

Table 9.1 Thermal coefficient for materials used as photomasks

Material	Thermal coefficient, ppm/°C
Soda lime	9.3
Borosilicate	3.7
Quartz	0.5

Reproduced with permission from [31], Microlithography: From Computer Aided Design (CAD) to Pattern Substrate, Cornell NanoScale Science and Technology Facility

Typically, electronic circuits and completed MEMS devices are fabricated in stages, requiring several sequential photolithography steps. Each step or layer requires a separate photomask containing part of the overall circuit or device pattern that must be carefully aligned to the previously patterned features on the substrate. An example of a four-layer photolithography process and the associated photomasks (both clear and dark field mask sets) are shown in Fig. 9.8.

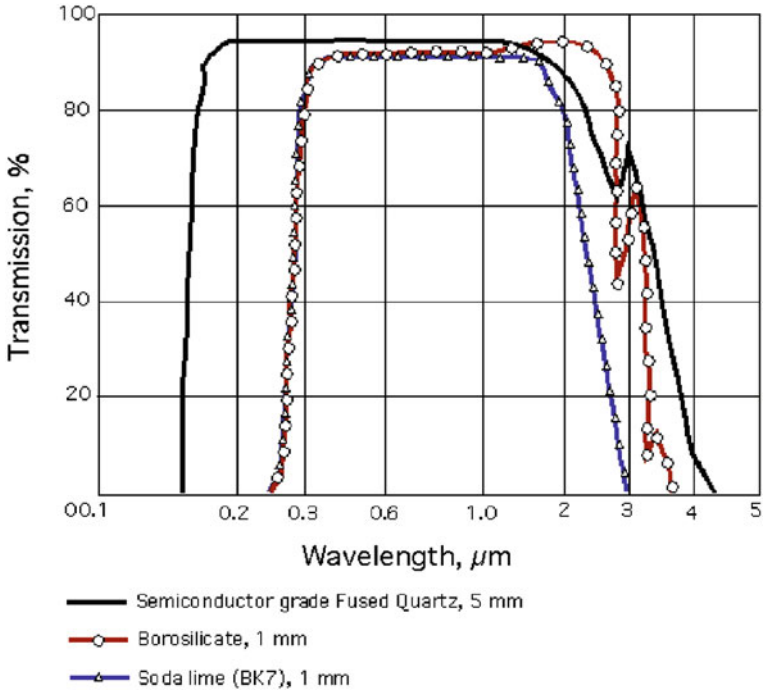

Fig. 9.7 Transmission of UV light through different mask materials (Modified from [30])

9.2.2 Optical Projection Systems

Optical projection systems are the tools used to create an image of the pattern contained in the photomask onto the surface of the photoresist layer. They typically utilize UV light from a mercury arc lamp the spectral emission of which is shown in Fig. 9.9. Several prominent emission lines are visible in the UV region of the spectrum at 435.8, 404.7, and 365.4 nm which are referred to as g-, h-, and i-lines, respectively. Both optical projection systems and photoresist formulations have been optimized for maximum performance at these wavelengths.

9.2.2.1 Contact Aligner

A contact aligner (used with contact and proximity masks) consists of a UV light source for exposure, a microscope with X, Y, Z and rotation (R) stages for wafer alignment and a mask holder. The mask and a photoresist covered wafer are brought into close proximity with the Z stage and aligned as needed with the X, Y, and R stages. Once aligned, the wafer and mask are brought into full contact (or close proximity) and exposed. Contact aligners are typically benchtop units, of which the MJB3 (shown in Fig. 9.10) and the MA-6 are commonly used examples. A contact aligner transmits a 1:1 image of the photomask onto the photoresist layer. This

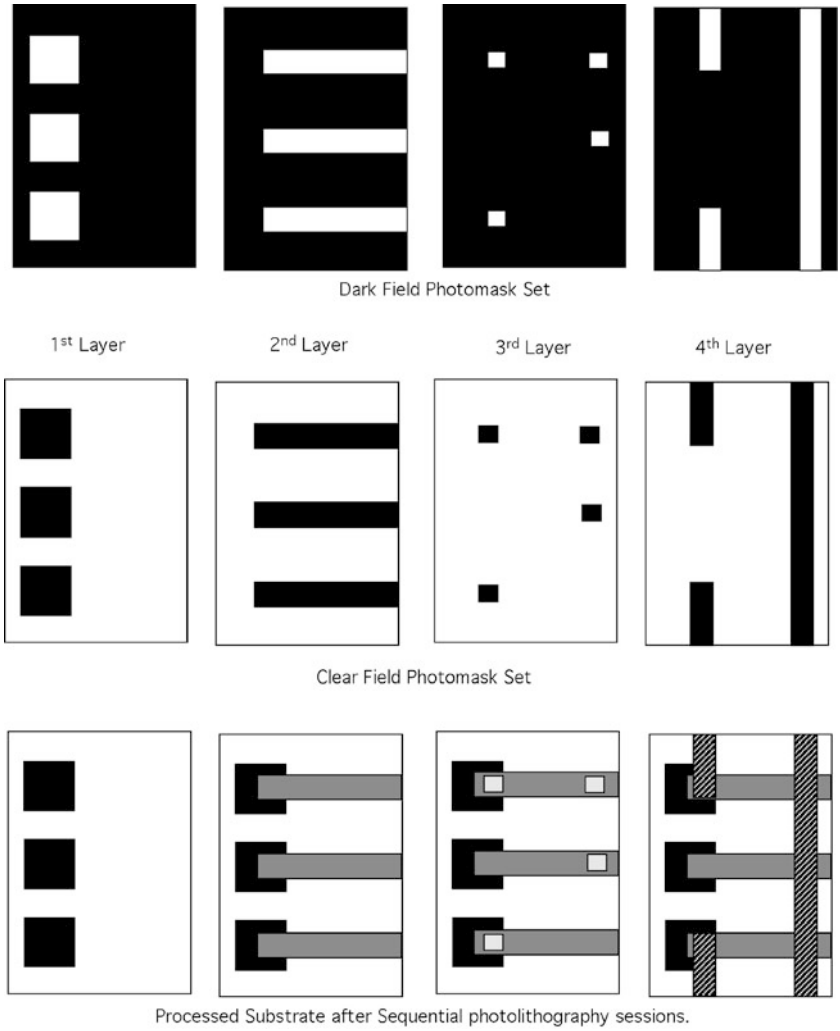

Fig. 9.8 Multilevel mask set for sequential photolithographic fabrication. Mask set examples are shown for both (**a**) bright field (clear field) and (**b**) dark field masks. The final patterned substrate is illustrated in (**c**) [25] (Modified from http://www.photronics.com/about/basics.jsp Reprinted with permission of PHOTORONICS, INC. from Photomask Basics)

allows large area patterns to be exposed into the photoresist in one step. Because the photomask and photoresist layer are in direct contact, there are no focusing problems onto the surface of the wafer. Substrates of various thicknesses can be easily handled and the alignment/exposure is not sensitive to wedge error (substrate not perfectly flat in relation to the projected image) as the substrate holder can tilt slightly to provide intimate contact with the mask.

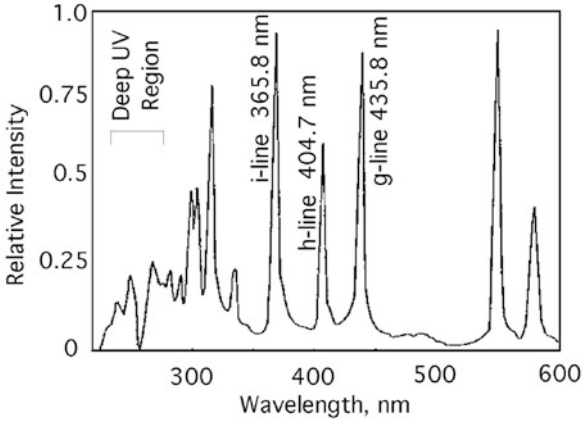

Fig. 9.9 Hg emission versus wavelength (Reprinted with permission from [32])

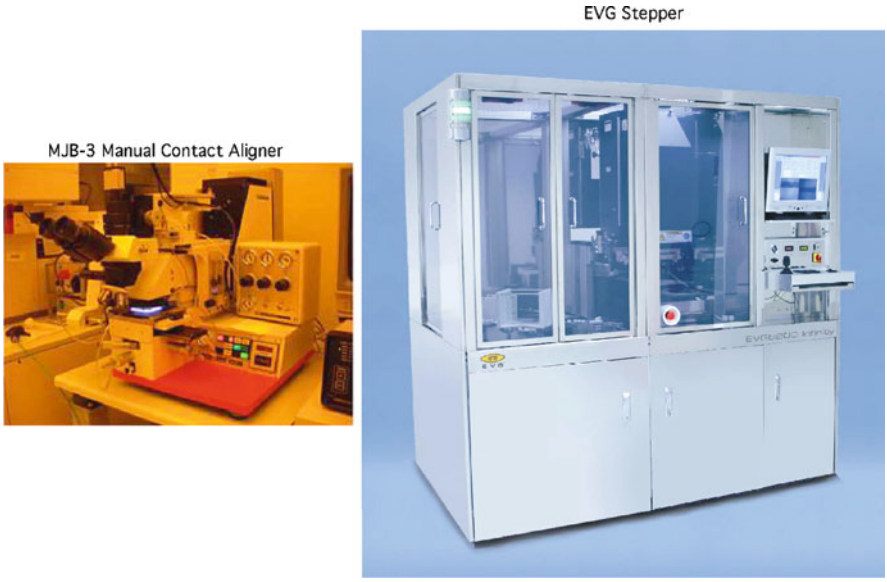

Fig. 9.10 Optical lithography systems: Manual contact aligner (*left*) and stepper (*right*) (Aligner reprinted courtesy of SUSS MicroTec Lithography GmbH, stepper reprinted courtesy of EV Group, Inc.)

Mixing photolithography with other patterning methods is also possible. For example, nanoimprint lithography features can be etched into the surface of a photomask allowing simultaneous patterning via both NIL and photolithography. Also, printing methods can be combined with photolithography by applying a printable layer or ink to the surface of a photomask. Such combined patterning methods

require contact to the substrate and therefore are only possible using contact aligner photomasks.

Contact aligners also possess several disadvantages. Contact between the photomask and the photoresist layer can cause damage to the photomask and is also a source of dirt and contamination. Particles trapped between the photomask and the photoresist layer, or a nonuniform photoresist layer can prevent proper contact and thus adversely affect the quality of the patterned features in the photoresist. Resolution is typically less for contact aligners as compared to steppers. Also contact aligners are less automated than steppers resulting in slower and less accurate operation.

Figure 9.11 contains a diagram showing the main components of a contact aligner. Some contact aligners have the ability to perform backside alignment. This allows the bottom surface of a substrate to contain a pattern that is in alignment with a pattern on the top surface of the same substrate. The aligner uses a second set of optics to align the previously patterned bottom surface of the substrate to a stored image of the photomask. Once aligned, a photoresist layer on the top surface of the substrate can be patterned.

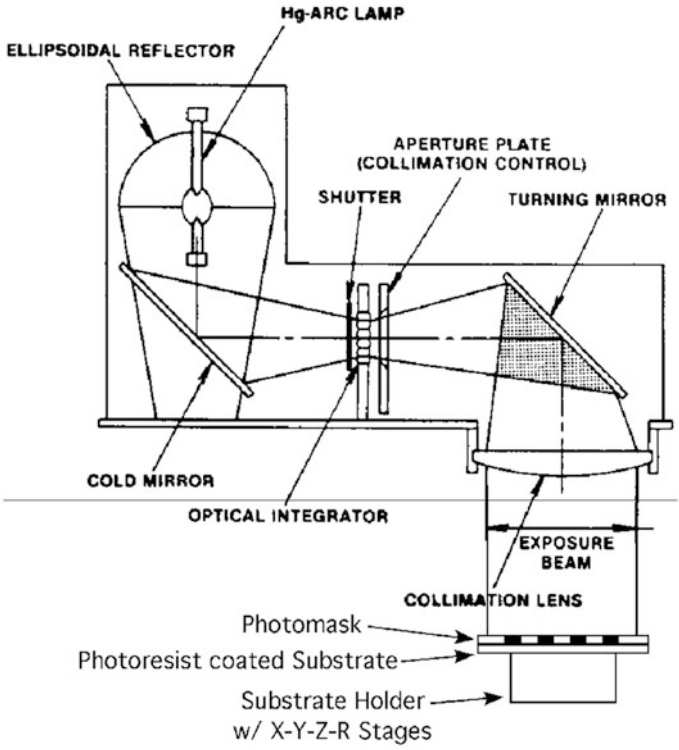

Fig. 9.11 Diagram showing the main components of a contact aligner (Reprinted with permission from [3])

9.2.2.2 Stepper

A stepper (used with projection photomasks or reticles) differs from a contact aligner in several ways. Primarily, a stepper contains an optical projection system that can produce an image of the photomask onto the surface of the photoresist layer. The image at the photoresist surface is typically a 1:4, 1:5, or 1:10 reduction in the size of the mask pattern and covers only a small area on the substrate. The lens system in a stepper is complex and contains numerous large-size optical elements, only a few of which are shown schematically in Fig. 9.12.

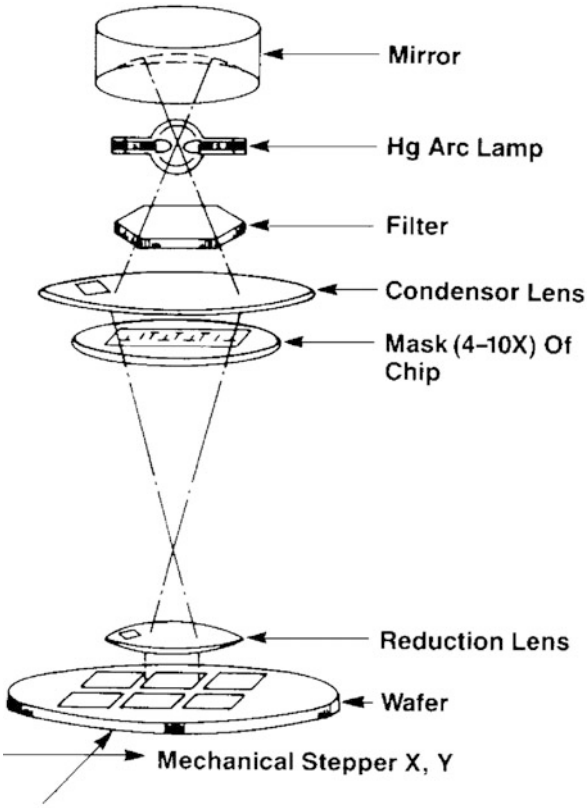

Fig. 9.12 Simplified schematic drawing of optical components in a stepper (Reprinted with permission from [33])

This lens system is designed to correct optical aberrations over a 30 mm circular field of exposure, therefore, alignment is critical and processes are sensitive to temperature, humidity, and vibrations. For this reason, the lens assembly is housed in a massive, vibration isolation enclosure equipped with both precise temperature and humidity control. The alignment of the photomask to the photoresist-coated substrate is much more computer controlled for the stepper as compared to the contact aligner. Also the position of the substrate holder is manipulated by high-precision, computer-controlled micrometers. As can be seen in Fig. 9.10, a stepper is

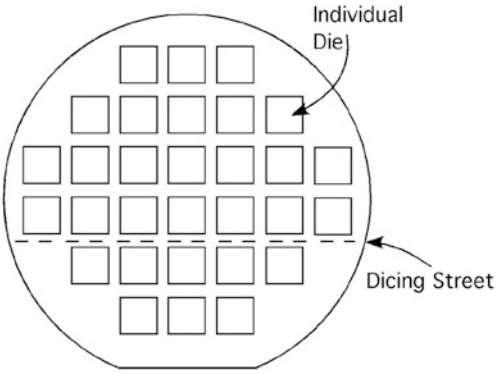

Fig. 9.13 Die layout on exposed substrate

usually a large format machine. The entire substrate is processed by moving (stepping) the substrate to an unexposed area and repeating the exposure. Each exposure of the mask is referred to as a die on the substrate. The stepping/exposing process is repeated until the entire area of the substrate has been processed in a layout similar to that illustrated in Fig. 9.13.

9.2.3 Photoresist

Photoresist typically consists of a mixture of organic polymers in a solvent combined with photosensitive additives. Photoresist is designed to change solubility due to exposure to UV light. The exposed area becomes either more soluble (positive resist) or less soluble (negative resist) upon exposure. The difference between these two main types of photoresist chemistries (positive and negative photoresist) is illustrated in Fig. 9.14.

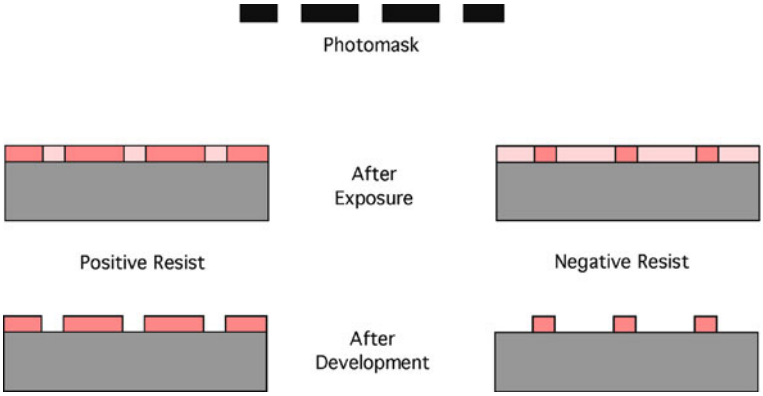

Fig. 9.14 Patterning of positive and negative photoresist highlighting regions of insolubility that remain after exposure and developing [32]

Photoresist chemistry is designed to have an extremely high contrast; changes in solubility are nonlinear and exhibit a threshold response resulting in sharply defined features with steep sidewalls even where small exposure intensity fluctuations exist within the photoresist layer. An example would be exposing photoresist to a sine wave intensity pattern. The desired result would be a sawtooth pattern in the photoresist layer rather than a sine wave pattern. In some cases, reflection of light from the substrate surface can produce interference effects within the photoresist layer. This is more an issue in situations utilizing steppers that employ higher intensity light sources as compared to contact aligners.

A standing wave profile as a function of photoresist thickness is shown in Fig. 9.15 which results in a sidewall profile as illustrated in Fig. 9.16. Such sidewall roughness can be drastically reduced by performing a postexposure bake [34]. Also, antireflective coatings (ARC) are sometimes applied to the substrate surface prior to the application of the photoresist layer [35].

Due to absorption affects, the top surface of the photoresist receives a larger exposure dose than the bottom surface. This results in a slightly larger exposed area at the top surface as compared to the bottom surface. This means that more

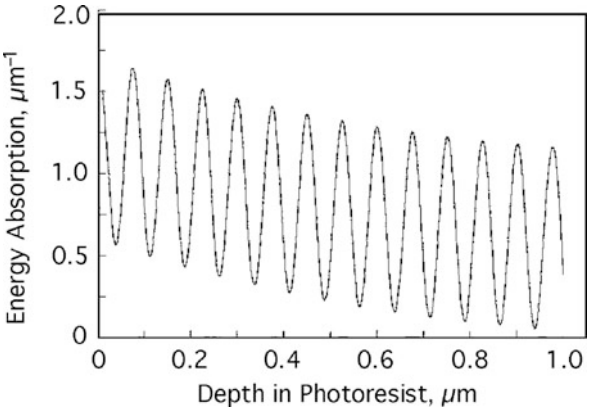

Fig. 9.15 Energy absorption of UV light as a function of depth in a 1 μm thick layer of photoresist (Reprinted with permission from [32])

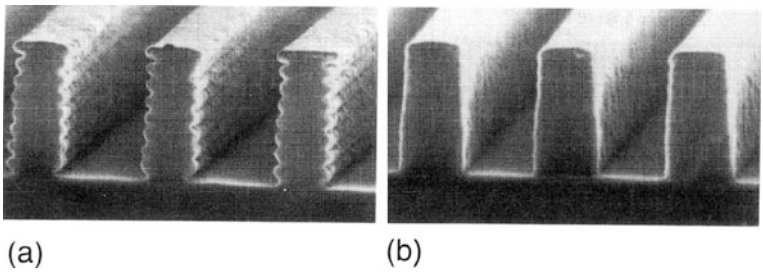

Fig. 9.16 Example of reflective standing wave effect of photoresist sidewall profile (**a**) without and (**b**) with antireflective coating (Reprinted with permission from B.W. Smith, M. Hanratty: Multilayer resist Technology, Chapter 10, In J.R. Sheats, B.W. Smith (Eds.): Microlithography Science and Technology (Marcel Dekker, New York, NY, 1998))

material will be dissolved away at the top than at the bottom of the exposed area. For a positive photoresist, such an exposure profile versus depth results in an "overcut" sidewall profile (a sidewall angle less than 90°). This is acceptable for etching applications but not for "liftoff" applications. For a negative photoresist, such an exposure profile versus depth results in an "undercut" sidewall profile (a sidewall angle greater than 90°). This is desirable for liftoff applications but can result in loss of pattern fidelity for etching applications. Ideal, overcut, and undercut sidewall profiles are illustrated in Fig. 9.17.

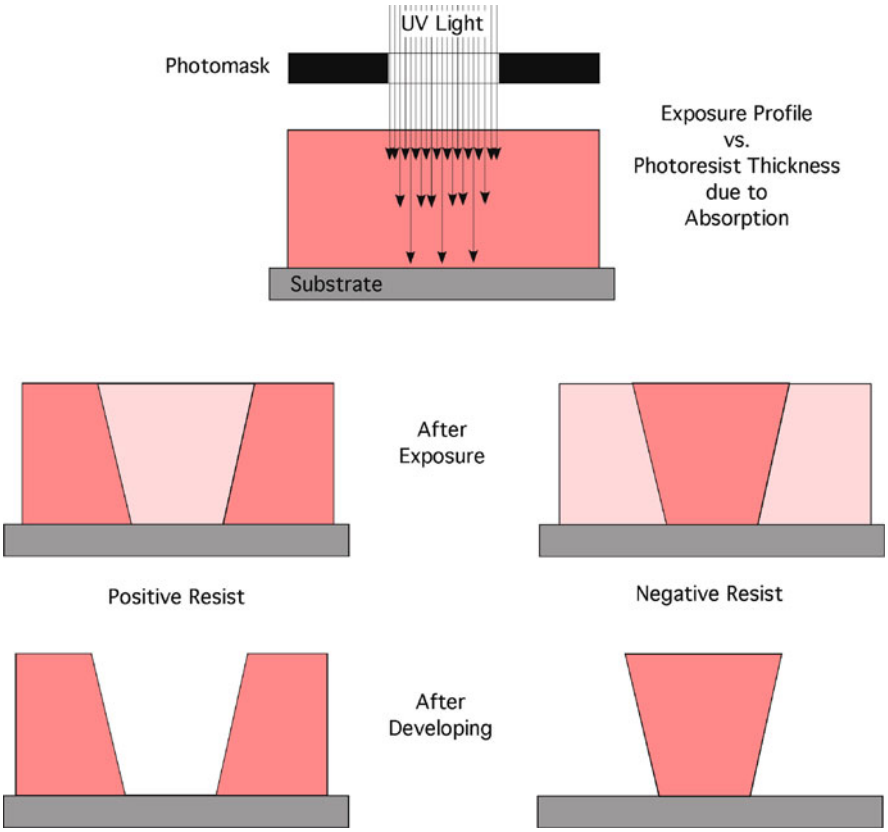

Fig. 9.17 Edge profile of photoresist layer resulting from absorption of light during exposure

9.2.3.1 Positive Photoresist

Upon exposure to light, the solubility of a positive photoresist increases due to polymer chain scission. Common formulations of positive photoresists have included diazoquinone ester (DQ) as a sensitizer in a novalac resin (phenol formaldehyde resin) (N). These molecules are shown in Fig. 9.18. Such formulations are referred to as DQN resists. A typical DQN resist formulation is listed in Table 9.2.

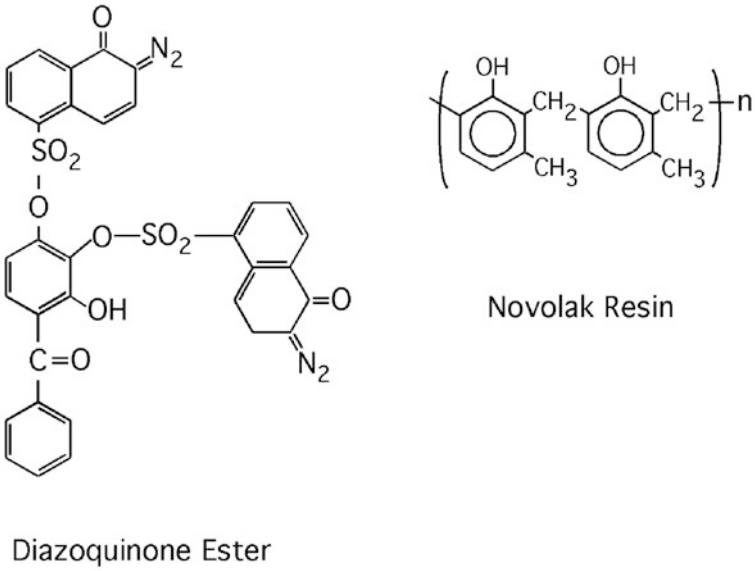

Fig. 9.18 Chemical formulas of (**a**) diazoquinone ester and (**b**) novolak resin components of standard positive photoresists (Reprinted with permission from [7])

Table 9.2 Photoresist components for positive DQN resist

Resist component	Weight, g
DQ	2
Novolak	8
Cellosolve acetate	20
Butyl acetate	2
Xylene	2
Water (trace)	0.05

Reprinted with permission from [7]

DQN-based resists are insensitive to oxygen and work very well at near ultraviolet (UV) wavelengths provided by the 365 (i-line), 405 (h-line), and 435 (g-line) nm lines of an Hg lamp typically found in research and development cleanroom facilities. For deep UV (DUV) (248 nm) and extreme UV (EUV) (193 nm) applications, positive photoresist formulations that do not contain aromatic molecules, such as PMMA-based materials, need to be utilized. A 15% loading of the photoresponsive DQ is enough to photochemically transform the two-component resist into a polar (base) soluble product upon exposure to UV light [7].

Positive resists are generally more expensive than negative resists; however, they exhibit higher pattern resolution causing them to be more widely used for photolithographic processing applications. Positive resists do not tend to swell when submerged in developer and can be developed in aqueous-based solvents that decrease the amount of generated hazardous waste material. Photochemical

reactions in a positive resist are not sensitive to oxygen and the phenolic resin component provides plasma etch resistance to the resist. DQN-based positive resists can be thermally stabilized to 200°C and are suitable for use for image reversal. However, they tend to have a narrower processing window and exhibit lower wet chemical etch resistance and lower adhesion to substrate surfaces. For this reason an adhesion promoter such as hexamethyldisilazane (HMDS) is applied to the substrate surface prior to coating the substrate with a photoresist layer [7, 36].

Commonly used positive resists include Shipley 1813 and Fujifilm OiR-906-10. Processing case studies are included below for both of these resists. Other common formulations of positive photoresist are shown in Table 9.3.

Table 9.3 Commonly used positive photoresists

Polymer	References from Moreau
Polyhydroxystyrenes	[23, 185]
Polyvinylphenol	[24]
Styrene-methacrylic acid	[25, 186]
PMMA-methacrylic acid	[26]
Styrene-acrylic acid	[27]
Esterified polyvinyl alcohol	[28]
Polyimide	[29]
Silylated novolak	[30, 211]

Reprinted with permission from [7]

9.2.3.2 Negative Photoresist

Upon exposure to light, the solubility of negative photoresists decreases due either to cross-linking of the polymer chains or a photochemical reaction. Many polymers will cross-link when exposed to light. Various types and classifications of negative photoresists are listed in Table 9.4.

An early negative photoresist formulation referred to as KTFR combined a bis-aryldiazide photosensitive cross-linking agent with a polyisoprene cyclized polymer as shown in Fig. 9.19 [7, 37, 38].

Such resists suffer from sensitivity to oxygen and solvent swelling. To overcome such deficiencies, onium salts [39, 40] were identified as photosensitive

Table 9.4 Classifications and types of negative photoresists

Thermoset	Elastomers	Thermoplastics
Diallylphthalates	Acrylates	Acetates
Epoxies	Polysulfides	Acrylates
Phenolics	Neoprenes	Cellulosics
Urethanes		Polycarbonates
Silicones		Polystryenes
Polyimides		

Reprinted with permission from [7]

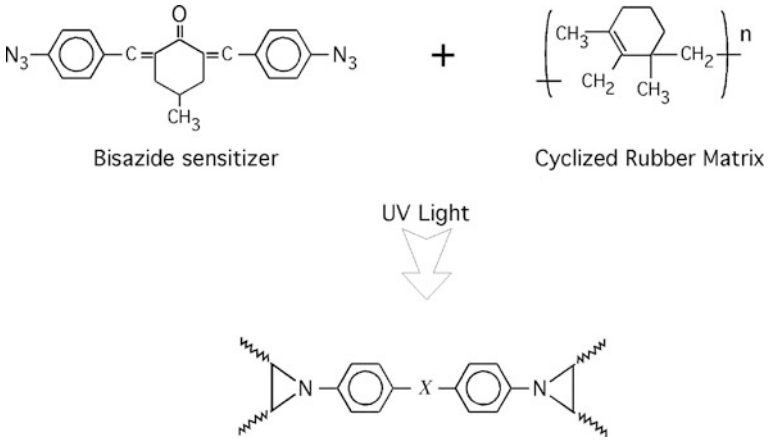

Fig. 9.19 Negative photoresist components before and after exposure to UV light (Reprinted with permission from [38])

additives that, when exposed to light, catalyze (chemically amplify) cross-linking or decreased solubility.

Negative resists are not widely used for photolithographic processing applications because they exhibit a lower pattern resolution in comparison to positive resists. They also tend to swell when submerged in developer. Negative resists are cheaper and have higher chemical resistance than positive resists. They are also more adhesive to substrate surfaces and harder to remove after processing. In addition, negative resists exhibit larger processing windows and can be formulated from a wide variety of polymers.

Common types of negative resist include chemically amplified epoxy or vinyl derivatives. A case study of the common Futurrex NR7-1500PY is presented below [30, 38].

For MEMS processing, SU-8 has recently become a commonly used negative resist material. SU-8 was first developed by IBM in 1989 and is now sold by MicroChem Corporation. SU-8 is highly transparent above 360 nm. This means that UV light can penetrate through a thick layer (up to about 2 mm). The lack of absorption results in nearly vertical sidewalls, thus allowing the fabrication of SU-8 structures with very high aspect ratios (>20). Because of this unique feature SU-8 is not usually used as a sacrificial pattern transfer layer but rather as a patterned polymer layer that is permanently incorporated into device fabrication. SU-8 is presented in more detail in Chapter 5.

9.2.3.3 Image Reversal for Positive Resist (Converting Positive Resist into a Negative Resist)

Because of the typical overcut sidewall edge profile in a positive photoresist, it is not suitable for liftoff processes. Also, a negative resist is not as attractive as a positive

resist in many applications because of lower resolution and the generation of larger amounts of hazardous waste. Therefore, image reversal processes have been developed that enable a positive resist to be used to produce a negative tone image. The image reversal process for a positive resist is accomplished by postbaking the resist layer in an ammonia vapor oven [31, 41–43]. The interaction of the ammonia with the UV exposed regions of the photoresist (i.e., soluble regions) renders the photoresist insoluble and also insensitive to further UV exposure. A subsequent flood exposure converts the previously unexposed regions of the photoresist to a soluble form. Thus, upon developing, the initially unexposed regions of the photoresist are dissolved away leaving a negative image of the initial photomask pattern.

9.2.4 Substrate

Historically, MEMS and IC fabrication have been performed using Si, Ge, or GaAs substrates. Flat panel displays are typically fabricated on glass substrates. More recently, microfluidic devices, lab-on-a-chip, and flexible electronics have incorporated polymeric substrates. Often transparent substrates can be more challenging to perform lithography on, as the reflection or lack thereof can broaden exposure regions, or reduce the dose directed to the photoresist. In all cases, photolithography demands that the substrate be flat and well cleaned. Inorganic substrates can be cleaned in several ways: for example: RCA clean, plasma (or UVO) clean, or solvent clean.

9.2.5 Processing Steps for UV Lithography

9.2.5.1 Deposit Photoresist

Spin Coating

Photoresist is typically applied to substrates via spray or spin coating. Although spin coating is a rather simple process, the tolerances for film thickness, uniformity, and repeatability raise a number of important issues that must be understood and controlled. As illustrated in Fig. 9.20, there are typically four stages of film evolution during the spin-coating process. The puddle formation stage results from the dispensing of the photoresist onto the substrate surface prior to spinning. The photoresist at this point is a thick puddle that covers some or all of the substrate. The film formation stage develops during acceleration of the spin coater as spinning commences.

The photoresist at this point covers the entire substrate, is starting to thin out at the center of rotation and is getting thicker toward the edges of the substrate. The thick-film stage develops after acceleration when the spin coater has reached the desired spin speed. The photoresist at this point is a relatively uniform but thick film (tens to hundreds of microns thick) that may contain thickness variations near

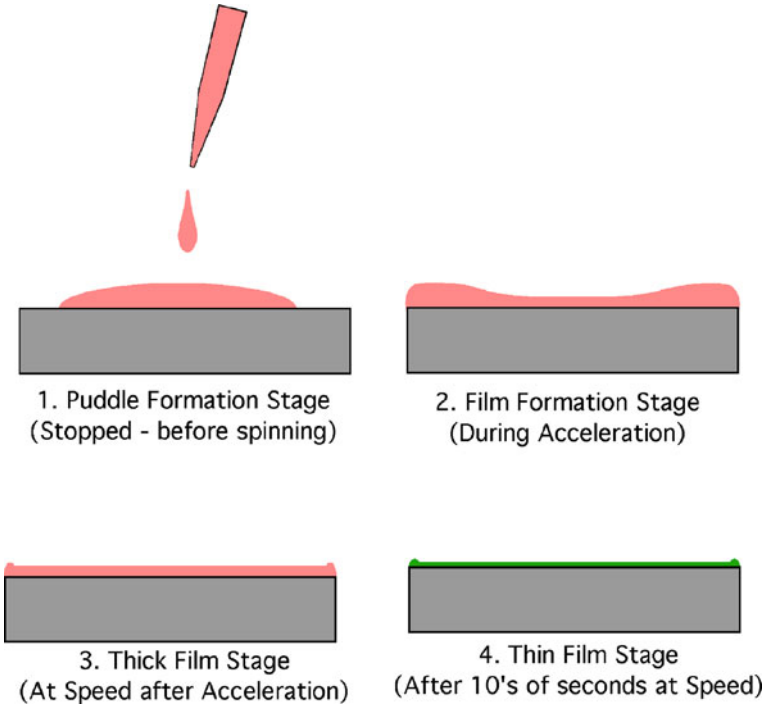

Fig. 9.20 Stages of film evolution during the spin coating process (Modified from [44] and used with permission)

the edge of the substrate. The thin-film stage develops after tens of seconds at the desired spin speed. The photoresist at this point is approaching its target thickness over the entire area of the substrate and may still have thickness variations only at the very edge of the substrate. As the film progresses from the thick-film stage to the thin-film stage, optical interference fringes resulting from reflection off both the top surface of the resist layer and the interface between the resist and substrate can be seen to change color as it gets thinner. Viewed at an appropriate angle, these thickness fringes can be seen to appear at the center of the wafer and rapidly travel radially out to the edge of the wafer while the wafer is spinning.

Several artifacts can appear in the photoresist as a result of spincoating: (1) striations that are nonuniformities in thickness typically on the order of 30 nm caused by nonuniform drying of the resist after spin coating; (2) edge effects that result from excess resist buildup at the wafer edge that can be 20–30 times thicker than the resist layer; and (3) streaks caused by particulate contamination on the surface of the substrate or in the resist itself.

As IC feature sizes decrease, resist thickness must also decrease. For MEMS processing however, such state-of-the-art feature sizes are typically not encountered. Rather, MEMS processing may require thicker resist layers that cover surfaces containing intricate topology, thus defining a different set of resist constraints that affect

viscosity, solvent evaporation rates, and so on. Such constraints must be factored into the production of flat, uniform, stress-free films.

After spin coating, the remaining solvents must be removed from the resist film. This is typically performed with a prebake (or soft-bake) on a hotplate or in an oven. On a hotplate the temperature increase of the photoresist starts at the bottom of the film and progresses upward. This prevents solvent vapors from getting trapped in the film during the prebake. In contrast, in an oven the temperature rise is more uniform throughout the film which can decrease the rate at which solvents are driven out of the film. In an oven, the top surface of the photoresist can form a skin that may trap solvent vapors and subsequently form bubbles or other imperfections in the resist layer. For this reason, prebaking in an oven is typically a slower process than prebaking on a hotplate.

Spray Coating

For substrates that have very nonuniform surfaces or deep trenches and tall features, as is common with MEMS processes, spin coating will not be able to produce a uniform photoresist coating. In cases such as these, the more commonly used method is spray coating [45, 46]. In a spray coating system, photoresists are mixed in different ratios with solvents to facilitate the spraying onto the surfaces of the wafer [47]. In the spray-coating process, there is direct perpendicular impingement of the coating solution that promotes coverage into deep trenches and along tall features. This is usually achieved by a reciprocating spray nozzle that coats the wafer surface to the desired photoresist thickness. For thicker films, the solutions used in spray coating are often diluted as compared to that used to achieve a similar spin-coated film thickness. These systems are critical to the fabrication of many high-aspect-ratio MEMS structures. Unfortunately, very few commercialized spray coating photoresists exist and most need to be mixed and characterized on a case-by-case basis [47].

9.2.5.2 Expose Photoresist

For a positive photoresist layer, the solubility of certain well-defined areas can be increased by the exposure to UV light. In contrast, for a negative photoresist layer, the solubility of certain well-defined areas can be decreased by the exposure to UV light.

This is performed by mounting a photoresist coated wafer and a photomask containing the desired mask pattern into an optical projection system (i.e., a contact aligner or stepper). The mask pattern and wafer are aligned in X, Y, Z, and Rotation as needed. Once properly aligned, UV light is transmitted through the mask to expose the desired area of the photoresist layer as described above. Depending on the resist properties, a postexposure bake may be necessary to achieve the desired solubility change in the exposed region of the resist layer.

9.2.5.3 Develop Photoresist

After exposing selected areas of the photoresist layer to UV light, the soluble regions can be removed by submerging the photoresist coated wafer in a solution of the appropriate solvent. A 30–90 s soak is typically sufficient to wash away the soluble regions of the exposed photoresist layer. To halt the developing process, the wafer is removed from the developer solution and then typically submerged into a deionized (DI) water bath for approximately 30 s and dried in a stream of clean/dry N_2 gas. At this point the photoresist layer should contain a pattern of open areas identical to the mask pattern. A careful inspection of the open areas and sidewalls with a high-powered optical microscope is recommended.

If there is any photoresist visible in the open areas then either the photoresist was not exposed to enough UV light or it was developed for too short a time. If the photoresist was underexposed then the lithography process will need to be repeated with a fresh layer of photoresist and a longer exposure time. If the photoresist was underdeveloped, the photoresist layer can be returned to the developing bath for a short time. It is noted that there exist a large number of developer solutions that can be used to an equal effect. In most cases, however, manufacturers of photoresist create various developers that are specifically optimized to be used with each photoresist and should be consulted when developing a more detailed or sensitive process flow.

9.2.5.4 Transfer Pattern

The patterned photoresist layer covering the surface of a substrate contains areas that are "open" (i.e., where the photoresist has been removed). At this point material can either be added to or removed from the substrate surface within these open areas.

Removing material is called etching. Wet etching techniques are presented in Chapter 8. Dry (plasma) etching techniques are presented in Chapter 7. Etching processes rely on the photoresist having a much slower etch rate than the substrate surface. The fidelity of the pattern transfer as a result of the etching process depends both on how directional the etch process is and on the profile of the photoresist sidewall at the edge of the open areas. If the photoresist sidewall is perfectly vertical and the etch rate in the horizontal direction is zero (i.e., perfectly anisotropic) then the pattern developed into the photoresist layer will be perfectly transferred into the substrate surface due to the etching process. Any deviations in the perfection of the photoresist sidewall will correspondingly result in removing more substrate material than desired. Etch rates that are not perfectly anisotropic will either produce less than vertical sidewall profiles in the substrate (sidewall angle less than 90°), undercut beyond the edge of the photoresist opening (sidewall angle greater than 90°) or over etching (features in the substrate surface that are larger than the openings defining the photoresist pattern).

Adding material is referred to as deposition. Deposition of semiconductor and dielectric materials is presented in Chapter 3 and deposition of metals in

Chapter 4. Typically material is added over the entire substrate thus covering the photoresist surface and the substrate surface that is accessible in the open areas of the patterned photoresist layer. The process of photoresist depositing and developing can leave a thin invisible residue on the substrate surface in the open areas of the photoresist pattern. This residue can cause a decrease in the adhesion of the deposited layer to the substrate surface and should be removed prior to deposition. This residue layer is typically removed by performing a low-power oxygen plasma etch (sometimes referred to as a descum) just prior to materials deposition.

9.2.5.5 Remove Photoresist

Once deposition is completed, the unwanted material has to be removed from the surface of the photoresist and also the photoresist removed. For a method that includes an additive process, this is accomplished all in one step called "liftoff". Liftoff is performed by submerging the substrate (covered with the photoresist and deposited layers) into a solvent bath. The solvent dissolves the photoresist layer thus causing the deposited layer on the photoresist surface to float away. Lift-off processes can be slow because the photoresist has very little surface area exposed to the solvent. The processing time can be decreased by increasing the temperature of the solvent bath. Also applying the solvent in the form of an aerosol spray can help the liftoff process. For this to work properly the deposited layer must be discontinuous at the edges of the opening in the patterned photoresist. Therefore the photoresist sidewall profile should be undercut. For this reason, negative photoresists or positive photoresists with image reversal work best for liftoff applications inasmuch as they inherently have undercut profiles. This is illustrated in Fig. 9.21.

For processes that involve etching rather than deposition, only the photoresist layer needs to be removed after substrate etching. Photoresist is typically removed in one of two ways: either using the appropriate solvent or using plasma etching

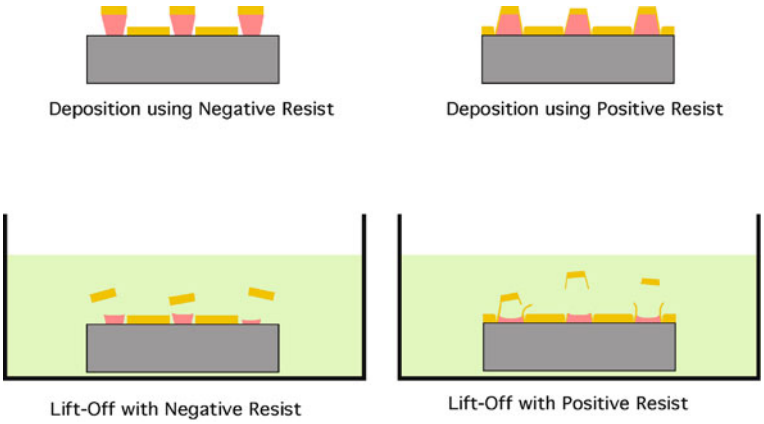

Fig. 9.21 Illustration of liftoff with positive and negative resists

(sometimes referred to as ashing). Acetone is the most common solvent for photoresist in the cleanroom and is usually sufficient to clean the surface. In some cases, the photoresist can be more difficult to remove, such as after successive baking steps or etching steps, and for these cases the photoresist manufacturers provide specific photoresist solvents, usually called "strippers," or "resist removers." These solvents tend to be much more aggressive than acetone, and may damage other materials on the surface of the wafer. Care must be taken when using these solutions to remove photoresist.

Plasma etching to remove photoresist is more straightforward. "Ashing" consists of an O_2 plasma that chemically reacts with and consumes organic matter on the wafer, and thus the photoresist. In some cases an argon plasma can be used to remove photoresist, but in this case the argon plasma merely physically sputters the photoresist material away and can damage other materials on the wafer. In many situations ashing is preferred over some of the more aggressive solvent options, but it is noted that the plasma techniques do not always remove photoresist, such as is the case with some negative resist formulations that are less reactive.

9.3 Grayscale Lithography

UV lithography processing methods presented in the previous section strictly pertain to high-resolution, 2-D patterning on flat substrates. Great effort has gone into producing near-vertical sidewalls for etching applications and slightly undercut sidewalls for liftoff applications. This is fine for the semiconductor industry, however, there are MEMS-based applications where precise control over the sidewall profile of the photoresist and subsequent etch processing is highly desirable. For example, applications in the area of optics [48–50], microfluidics [51], and photonic crystals [52] require the ability to apply 3-D fabrication methods to MEMS substrates.

Two-dimensional lithography photomasks are designed to either block or transmit light. The resolutions of these masks are diffraction limited. The primary goal is to completely expose and subsequently remove all the photoresist from specific area(s) on the coated substrate. In 3-D lithography applications, the goal is to pattern the photoresist such that the patterned photoresist layer is comprised of areas containing variable thickness profiles. To accomplish this, both the photomask and the photoresist properties can be manipulated. For the photomask [53–62], the opaque areas that define the pattern can be modified to be partially transparent. An illustration of this is shown in Fig. 9.22.

There are a number of methods that can be used to achieve this. One method uses commercially available high energy beam sensitive (HEBS) glass that uses the beam-induced reduction of silver ions in a silver–alkali–halide material to produce the darkening of the glass via coloring specks of silver atoms. This directly modulates the opacity of the photomask with no graininess. HEBS glass mask resolution is limited only by the beam writers, and examples of sub-0.25 μm features have

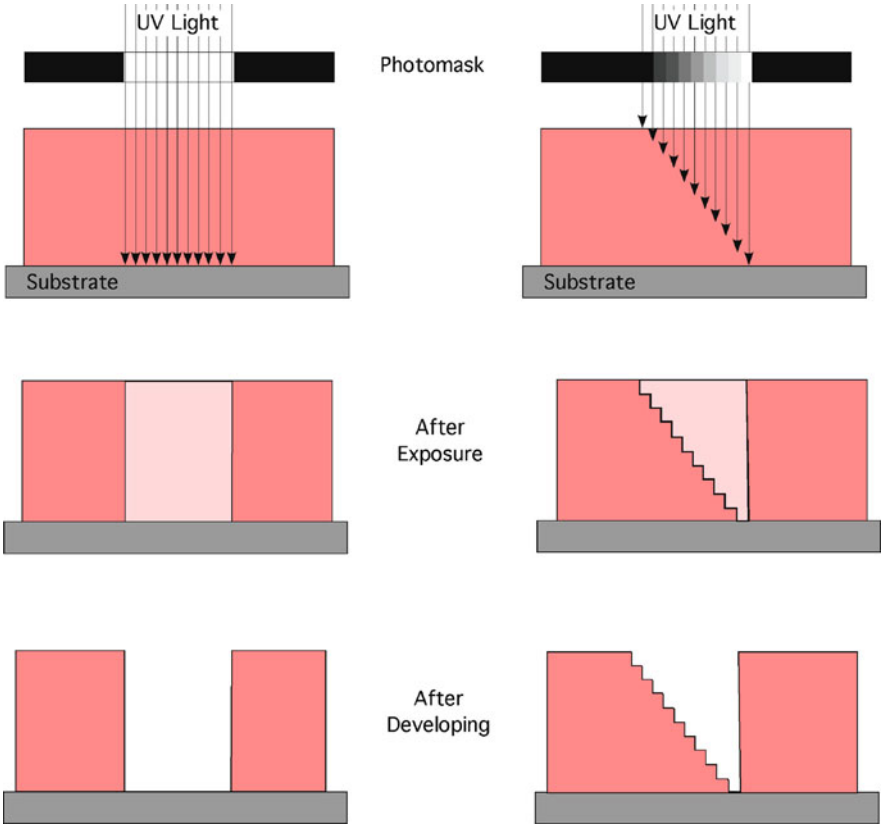

Fig. 9.22 Comparison between photoresist exposure profile using standard and grayscale photomasks (Modified from [63], reprinted with permission)

been written for these photomasks. These masks can also be used in both projection and contact lithography systems, which makes them more versatile when considering equipment availability and differing cleanroom capabilities. The cost of HEBS masks can also be up to one order of magnitude more than standard chrome on quartz plates, which has significantly limited the wide adoption of this technique in the MEMS community. However, when an extremely smooth 3-D profile is required, or contact lithography is the only option available, HEBS glass is an excellent choice for grayscale lithography. HEBS glass is often used for lenses and high-density lens arrays due to the smoothness achieved in the final photoresist profile. Figure 9.23 shows an example of patterned silicon structures using HEBS glass lithography.

As already mentioned, HEBS glass masks are fabricated using an electron beam to initiate the chemical reduction of the silver-containing doped glass. The opacity of the mask is determined by the electron beam parameters with the dose practically controlled by changing the dwell time and the energy of the beams. The

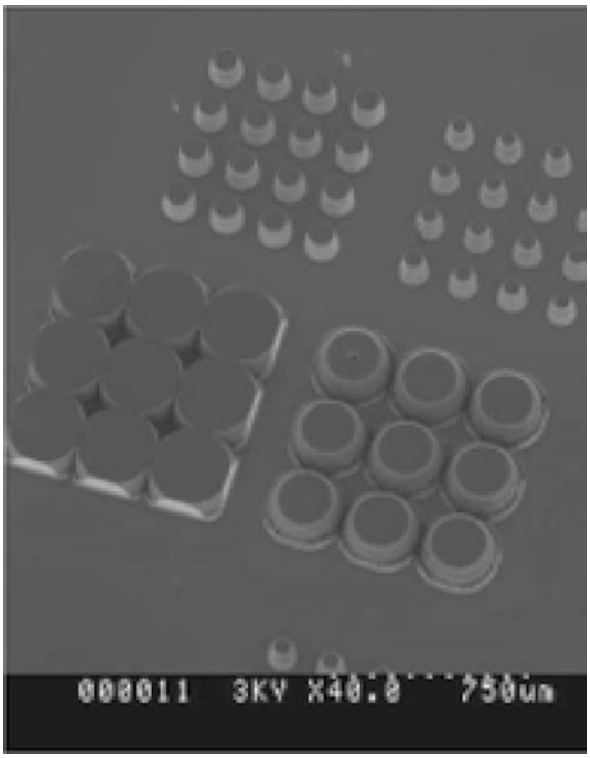

Fig. 9.23 Silicon profile generated using a HEBS glass mask and DRIE etching (Reprinted with permission, Lawrence Livermore National Laboratory, https://www-eng.llnl.gov/mic_nano/mic_nano_MEMS.html)

ability to fine-tune the dose allows for a very large number of gray levels, over 500 for most cases. Unlike a chrome mask, however, the dark areas of the mask never become 100% opaque. Fabrication of a mask is performed exclusively through Canyon Materials, Inc. (CMI) who provide detailed instructions of how to structure the mask design file for them to perform the electron beam exposure of the mask. Inasmuch as many processing variations exist for the photoresists and optical lithography sources, CMI provides standardized calibration masks to establish proper photoresist exposure times, thicknesses, and development procedures. There are a number of publications available showcasing the capabilities of these masks [64–66].

There is another commonly used method that has been more widely adopted, utilizing a variable transmission mask just like the HEBS glass, but with standard mask fabrication techniques. This is accomplished by pixelating the chrome patterns on the masks so as to control the amount of light transmitted. This technique necessitates the use of a stepper lithography system, which can be a problem if such a system is not readily available. As discussed below, the limitations on pixelation result in a finite number of transmission steps (called gray levels) between 0 and 100% transmission. For the photoresist, both sensitivity to UV light exposure and

selectivity to the subsequent substrate etching will be important for utilizing all the gray levels. For example, if the photoresist is too sensitive to UV light, light from the first grayscale level will fully expose the photoresist at the substrate surface before light from the last grayscale level has a chance to expose the top surface of the photoresist. If the photoresist is removed too fast during the substrate etch then the photoresist will be consumed before the desired etch depth can be reached. Likewise, if the photoresist is not consumed at all then none of the grayscale levels can be transferred into the substrate etch.

9.3.1 Photomask Pixelation

To establish partial transmission of UV light during the exposure step in the photolithographic process, the opaque part of the photomask can be pixelated as shown in Fig. 9.24. The pixels need to be designed so that they modulate the transmission of UV light without being directly imaged onto the surface of the photoresist. For this reason the pixel dimensions need to be below the diffraction limit of an optical projection system. When making a particular mask design, the spacing (pitch) and the pixel dimensions are varied to create different levels of transmission, generating the gray levels in the photoresist pattern. In this way, the minimum dimensions available in the design of a pixelated gray mask are limited by the projection lithography system's resolving power, and the resolution of the mask writing system. In addition, less pattern control is available when making complex 3-D structures inasmuch as pixel size and pixel spacing are all different based upon the particular transmission or gray level being expressed. Minimum dimensions for singular gray levels are then fixed by this pixel size and pitch limitation. Pixelated grayscale masks are in general best suited for larger patterns, or for situations where mask cost is a restrictive parameter. A more detailed discussion of the mask design and pixelation is included in the case study section of this chapter (Case Study 10).

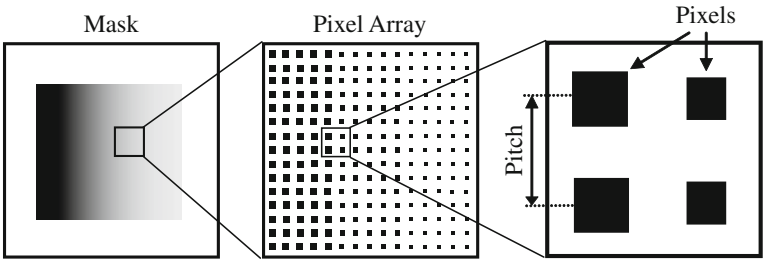

Fig. 9.24 Pixelation of a gray-scale photomask (Reprinted with permission from [67])

9.3.2 Photoresist Properties for Grayscale Lithography

9.3.2.1 Contrast and Thickness

A photoresist contrast curve is shown in Fig. 9.25, with thickness plotted as a function of the logarithm of the UV light exposure. Two exposure points are noted: E_{th} is the minimum exposure required for the photoresist to react to light and E_c is the minimum exposure required to completely remove (or clear) the photoresist from the substrate surface [68]. The linear slope between these two exposure points is defined as the "contrast." A larger photoresist contrast translates to a smaller difference between the two exposure endpoints and to a smaller processing window. For grayscale lithography, larger processing windows are desirable so that good differentiation between exposure levels can be realized. Therefore, low-contrast photoresists are typically used for grayscale lithography.

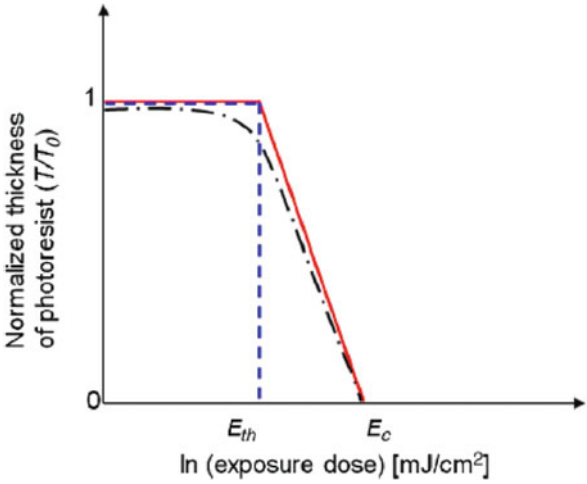

Fig. 9.25 UV light exposure profile as a function of photoresist thickness (Reprinted with permission from [68], copyright 2008, American Institute of Physics)

In addition to contrast, the thickness of the photoresist layer is also important. The thickness should be chosen so that E_{th} is the exposure produced by the largest grayscale level and that it occurs at the top of the photoresist surface precisely when E_c is the exposure produced by the smallest grayscale level.

9.3.2.2 Exposure and Developing Times

The exposure time is determined as the time needed to deliver an exposure equal to E_c. Theoretically, determining the exposure time is straightforward but in practice it can be problematic. Temperature, humidity, variations in photoresist thickness, intensity fluctuations of the stepper, and so on can all affect both the exposure and the developing time. Therefore, it is typical to empirically determine these times by performing test exposures using a calibrated mask. Overexposing or underexposing will leave a thickness bias on the whole photoresist structure that will interfere with

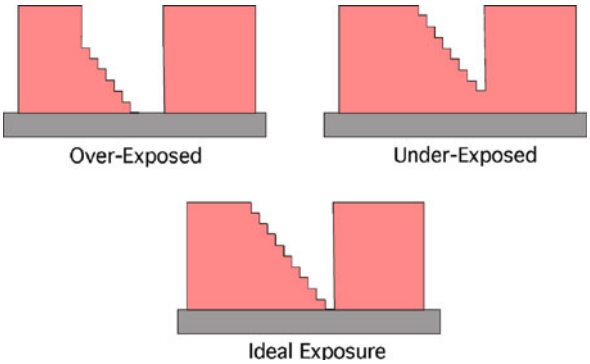

Fig. 9.26 UV exposure levels for gray-scale lithography (Modified from [67], reprinted with permission)

the proper transfer into the substrate beneath, creating a disparity in the final device thickness, as illustrated in Fig. 9.26.

9.3.2.3 Etch Selectivity

Photoresist etch selectivity is defined as the ratio of the substrate etch rate to the photoresist etch rate for a given set of etching conditions. A high etch selectivity is usually desirable for standard photolithography applications where the original fidelity of the photoresist pattern is designed to survive the substrate etch, thus producing a perfect replica of the photoresist pattern etched into the surface of the substrate. For grayscale lithography, the photoresist layer is designed to be consumed during the substrate etch. Often times varying levels of O_2 gas are introduced during the etch to speed up the photoresist consumption rate. Using this method, it is easier to fine-tune the resulting selectivity rate. The resulting pattern etched into the substrate reflects the thickness profile of the original photoresist pattern. Each gray level developed into the photoresist corresponds to a specific etch depth into the substrate surface which is determined by the etch selectivity and the starting thickness of the patterned photoresist layer. The difference in final structure transfer is illustrated in Fig. 9.27. Photoresist thicknesses of 6–10 μm, when combined with etch selectivity between 40 and 100, translate into substrate etch depths ranging from tens to hundreds of micrometers. An example of a fully transferred pattern using HEBS glass has already been shown above (Fig. 9.24), and a typical transferred pattern using a pixelated mask is shown in Fig. 9.28. More detailed discussion of the silicon etching process is given in Chapter 7.

9.4 X-Ray Lithography

X-ray lithography was originally developed as an attempt to achieve smaller device geometries by using the very short wavelength of X-rays (~0.7–1 nm optimally), the ability to have highly collimated X-ray sources, and the relatively small scattering

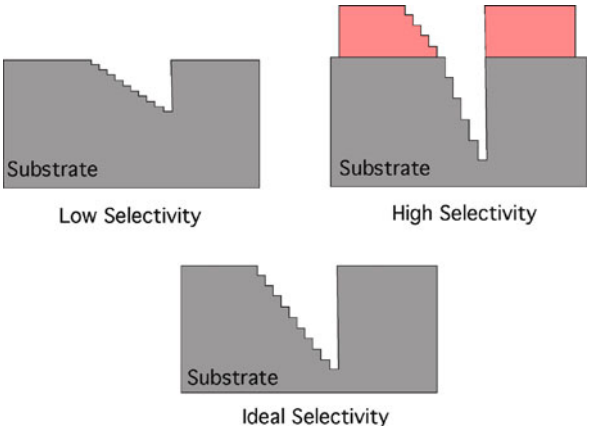

Fig. 9.27 Etch selectivity profiles for gray-scale lithography (Modified from [67], reprinted with permission)

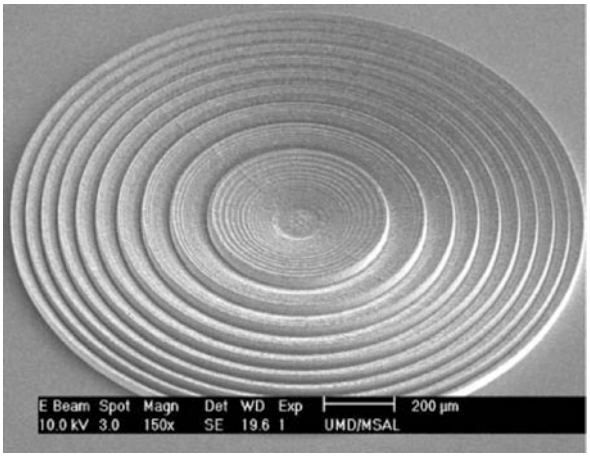

Fig. 9.28 Silicon Fresnel lens patterned using a pixelated grayscale mask and etched using DRIE (Reprinted with permission from [69])

of X-rays through common materials. Theoretically, 20 nm resolution features can be defined, but in practice it is more common to see features in the 50 nm range [70]. This is due to a number of challenges encountered in the lithography process, such as synchrotron X-ray wavelength spectral broadening, mask–substrate distance, and mask distortions [71].

X-ray lithography follows a very similar process to that of UV lithography: a pattern is transferred into an optically sensitive resist material (in this case X-ray sensitive resist) by illumination through a mask onto the resist. Although there was an initial interest in X-ray lithography for VLSI design, most X-ray lithography is used today for the fabrication of high-aspect-ratio molds in a process commonly referred to as LIGA (***Li****thographie,* ***G****alvanoformung,* ***A****bformung*) [72]. LIGA was initially used in the fabrication of nozzles for uranium enrichment (Fig. 9.29), with

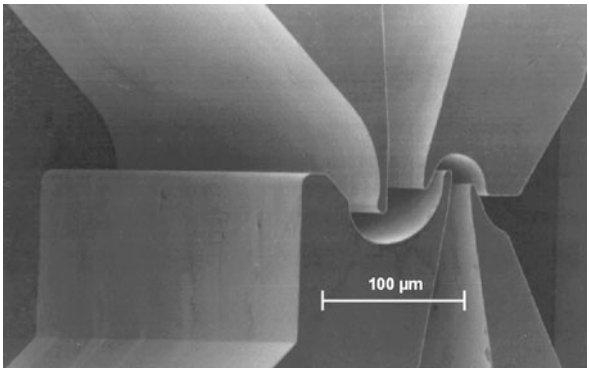

Fig. 9.29 LIGA-fabricated uranium enrichment nozzle (Reprinted with permission from [73])

many other applications being developed after the initial demonstration of this technology [73]. LIGA takes advantage of the very high aspect ratios (100:1) achievable through X-ray lithography and uses the resulting polymer resist structures as molds for electroplating (metals), or other molding processes. There have also been examples of SLIGA performed which incorporates sacrificial layers into the standard LIGA process thus allowing for the creation of freestanding and moveable structures directly on the substrate [74]. X-ray lithography is used in MEMS processes and devices primarily in this context [75, 76].

The primary challenge for X-ray lithography is in the required light sources for highly collimated X-ray beams. These types of sources are generally much more complex than the typical UV discharge lamps used in UV lithography. In addition, due to their very high energy, X-rays cannot be focused and guided using traditional lenses and mirrors as in UV lithography. The synchrotron is one of the most important enabling tools of high-aspect-ratio X-ray lithography, capable of emitting high-power, highly collimated radiation. This high collimation permits relatively large distances between the mask and the substrate without the penumbral blurring that occurs from other X-ray sources, and also enables the high aspect ratios in exposed photoresist, which is beneficial to the development of LIGA.

In the electron storage ring or synchrotron, electrons follow a circular path. The radial acceleration of the electrons causes electromagnetic radiation to be emitted forward. The radiation is thus strongly collimated in the forward direction of the moving electrons and is essentially parallel. These radiation sources also provide higher flux densities, which enable shorter exposure times. Photon energies for a LIGA exposure are approximately distributed between 2.5 and 15 keV.

9.4.1 X-Ray Masks

X-ray masks are one of the bottlenecks in the commercial development of LIGA and X-ray lithography [77], because there are a number of materials used for this process, depending on the particular research group's fabrication facilities and

capabilities. The general concept employed in X-ray mask generation is to have a highly transparent material for the field of the mask (low-Z materials), and an X-ray-absorbent material to define the features on the mask (high-Z materials). This is commonly done with a substrate material of graphite or vitreous carbon, or sometimes silicon nitride, silicon carbide, or diamond membranes [78, 79]. The latter are not as readily preferred as the membranes required for the masks in these cases are very fragile. Beryllium substrates are very attractive mask materials due to their very high X-ray transparency and the ability to make them much thicker and more stable as compared to membrane approaches. The patterned absorbing features are typically X-ray absorbing metals such as tin, copper, gold, or lead [76].

One of the challenges to making these large area masks is the ability to maintain low distortion in the finalized masking image. Due to the 1:1 mask transfer, the accuracy of the mask features is paramount in importance. These distortions are caused by a number of factors, with a major one being film stresses in the membrane materials. More masks are being made out of SiC due to this distortion issue. Research has also been undertaken in an attempt to predict these distortions and counteract them with the design of the mask itself, similar to what occurs in ultra-high-resolution masks for UV lithography. Even the mounting of the mask contributes to distortions in the mask pattern due to stresses; most masks are mounted in metal rings to prevent some of these adverse effects.

The definition of the mask features can be done a number of ways and greatly depends on the required resolution of the mask patterns. Direct-write methods such as electron beam lithography are used to achieve the most accurate features for the mask, but this carries the disadvantage of being very time consuming for the large-area masks in X-ray lithography. Other methods (such as described in this chapter) are also employed to pattern the X-ray masks with their own varying lithographic tolerances.

Fabrication of these masks is often quite involved, in an attempt to reduce film stresses and achieve high-resolution features. Typically, the mask fabrication begins with a silicon wafer that is coated with the membrane material (silicon nitride, silicon carbide). Two methods are commonly used to pattern the mask absorber metal (tungsten, titanium, gold, etc.). The metal can be blanket deposited on the backside of this coated wafer, and then patterned using subtractive processes (dry or wet etching). Other methods employ thicker photoresists and rely on additive processes such as plating to deposit a thicker absorber coating which is required for lower Z materials such as gold to achieve good exposure contrast. This can be done a number of ways, one of which involves performing an X-ray lithography step on a thinner coating of X-ray photoresist to form a plating mold for the final mask, but can be performed with normal thick photoresist plating mold technologies as well. The thickness of this absorbing pattern can vary from a few microns to up to 50 μm, and depends on the thickness of the photoresist to be exposed, both of which are directly related to the required X-ray energy [76].

The completed mask is normally placed in a glass or metal ring at this point in the process to provide the wafer with stability and strength. After this step, the membrane is released by backside etching of the silicon wafer. A photograph of a finalized X-ray mask is shown in Fig. 9.30.

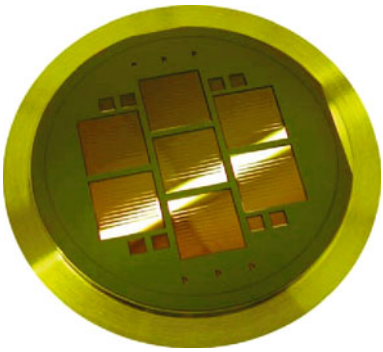

Fig. 9.30 An example of an X-ray mask made from SiC (Reprinted with permission from [80])

9.4.2 X-Ray Photoresists

X-ray photoresists function very similarly to the resists used in e-beam lithography (see Section 9.5.1), and thus most e-beam resists can be used for X-ray lithography; poly(methyl methacrylate) (PMMA) is most commonly used for X-ray lithography, however, SU-8 is also a possible choice [81]. PMMA is exposed through the generation of Auger and photo electrons by the X-rays entering the photoresist. These interactions chemically alter the resist polymer chains through scission, reducing their order from approximately 1,000,000 to 1000. This is what allows the polymer to be dissolved by developers that attack the lower-order polymer chains [82].

Photoresists used in X-ray lithography for MEMS applications are generally applied in thick layers to take advantage of the high aspect ratios achievable, particularly for LIGA. The typical choice PMMA is applied to the substrate for some of the thinner applications by way of spinning, or more probably by a glue-down process in which a precast sheet of PMMA is attached to the substrate material [82]. This second option allows for much thicker molding layers and also prevents the buildup of stress which can be caused by casting the photoresist directly on the substrates. The PMMA is then milled down to the precise height before X-ray exposure. In some cases, after exposure a second PMMA layer is glued to the surface for a second exposure, facilitating the creation of even higher aspect ratios [83].

In the case of ultra-high- and very-high-resolution X-ray lithography, the thickness of the photoresist is somewhat limited, with thicknesses of typically 5–50 μm. These thicknesses have been found to be the threshold for adverse optical effects such as diffraction and scattering which occur because of mask dimensions and X-ray energy, respectively [84].

9.4.3 Exposure

Due to the fragility of X-ray masks fabricated on thin membranes, contact lithography is not possible without damaging the masks. In addition, the high energy of the

X-rays prevents the use of a typical projection lithography system where patterns can be focused onto the surface of the substrate and reduced in scale. As necessitated by these conditions, all X-ray masks must be 1:1. Instead of using these more common lithographic techniques (projection and contact), proximity masking is used. Divergence and near-field diffraction commonly encountered in traditional proximity UV lithography are not as large a problem for X-ray lithography due to the highly collimated radiation and the very small wavelength of the X-rays. Mask-wafer spacing of anywhere from 5 to 50 μm is typical and varies depending on the available equipment or the required resolution, as increasing this gap does have a negative effect on the final patterns [70, 82–84].

Exposure times and energies vary greatly based upon the thickness of the photoresist used and the required critical dimension size. X-ray energies for exposure of high-resolution patterns are typically around 1 keV, whereas a more typical MEMS application will require X-ray energies of 5–15 keV. A typical dose for PMMA is 4–20 kJ/cm^3. Anything higher than this could possibly cause the resist to burn [85]. Exposure times vary, again, based upon the thickness of the resist, but generally are no more than a few hours. Care must be taken not to perform very long exposures to prevent mask and substrate heating due to the X-ray exposure, which can cause misalignment and mask distortions [86]. The time of the exposure plays a large part in the choice of the masking material used.

Karl Suss has created a commercially oriented X-ray stepper tool that allows a pattern to be exposed using X-ray lithography [71, 87, 88]. This particular device operates with a proximity gap of 20–50 μm, and has a scanning speed of 0.5–20 mm/s. In the literature, custom modifications to this tool have yielded very small proximity gaps to approximately 10 μm [70]. The tool still requires a separate synchrotron radiation source, however. The stepper functions similarly to that of a standard stepper and can align masks to each other via CCD cameras to facilitate multilevel X-ray exposures with high pattern alignment accuracy.

9.4.4 Development

For high-aspect-ratio structures the resist–developer system usually has a ratio of dissolution rates in the exposed and unexposed areas of 1000:1. Developers vary: GG developer (composed of diethothxy and morpholine) is sometimes used [82]; another standard developer used is a mixture of tetrahydro-1,4-oxazine (20%), 2-aminoethanol-1 (5%), 2-(2-butoxyethoxy)ethanol (60%), and water (15%) [89]. The former provides nearly 100% selectivity and does not induce any additional stresses or cracks in the exposed resist. Developers vary on a case-by-case basis and are usually empirically standardized and characterized.

After development, the substrate is rinsed with deionized water and dried either in a vacuum or by spinning. At this stage, the PMMA structures can be released as the final product or can be used as molds for subsequent metal deposition. An illustration of the complete process is shown in Fig. 9.31. Discussion of the plating

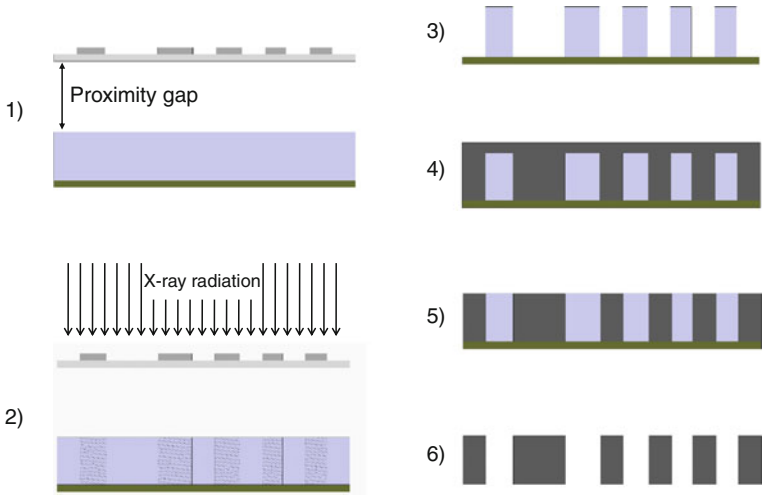

Fig. 9.31 X-ray lithography process. Steps 4–6 are unique to the LIGA micromachining method. (1) Mask is fabricated with transparent membrane and metal absorbing pattern and brought within a proximity to a conductive substrate coated with PMMA or other thick X-ray photoresist. (2) X-ray radiation exposes PMMA resist. (3) Development of PMMA. (4) Metal is plated into the PMMA mold (nickel, gold, copper). (5) Wafer is lapped to remove the metal cap; for mold fabrication, this step may be omitted. (6) Substrate and PMMA are removed and the metal mold/part is ready for additional processing or assembly

and injection techniques that can be used for the final LIGA fabricated structures are explored in more detail in Chapters 4 and 5.

9.5 Direct-Write Lithography

The lithographic processes discussed above include the use of a mask for patterning a layer of resist. It is also possible to pattern the resist layer directly by forming the source into a narrow beam and scanning it across the surface of the resist. By blocking the beam or scanning it in a desired fashion, the resist layer can be exposed pixel-by-pixel. After exposure, the resist layer can then be further processed just as it would have been had it been exposed through a mask in the photolithographic method. Electron beams, ion beams, and laser beams can all be used in such direct-write techniques.

9.5.1 E-Beam Lithography

Electron-beam (e-beam) lithography uses electrons to expose a resist layer. Like photons in photolithography, the solubility of a resist layer can be changed due to interactions with electrons. By scanning the electron beam across the surface of the

resist layer in a fashion almost identical to scanning electron microscopy (SEM), the resist layer can be patterned. In an SEM, magnetic or electrostatic deflectors are used to scan or raster the beam across the surface of the resist layer. Added to this is the means to blank the beam by inserting electrostatic plates into the column that can deflect the beam so that desired areas (or pixels) are left unexposed. Dedicated systems that have been designed solely for e-beam lithography can provide state-of-the-art capabilities. However, in many research and development labs, e-beam lithography is performed using an SEM fitted with a beam blanker controlled by a separate computer running commercially available SEM lithography software. A diagram of the scanning and beam blanking of an SEM-based e-beam lithography system is shown in Fig. 9.32.

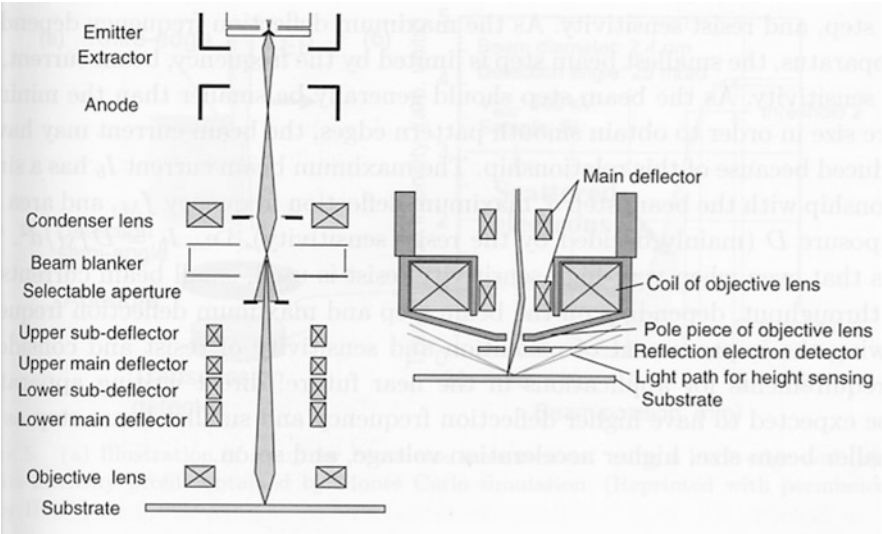

Fig. 9.32 Illustration of an e-beam lithography system (Reprinted by permission from [90])

For a Gaussian beam focused using magnetic lenses, a resolution of 10 nm or less is possible with e-beam lithography. The exposure speed is too slow, however, for large-scale production and is therefore typically used for mask fabrication, prototyping, or research and development applications. For example, photomasks and nanoimprint lithography templates are routinely fabricated using e-beam lithography due to the high resolution available.

Depending on the magnification setting of the microscope during writing, the electron beam can only be scanned over a finite area (e.g., a 100 × 100 μm area). To pattern larger areas, exposed areas can be "stitched" together by moving the substrate to a new area and continuing the exposure. This is similar to the action of a stepper but with e-beam, the subsequent exposures do not have to be identical and can be connected.

E-beam lithography is capable of producing high-resolution patterns, thus it is also well suited for NEMS applications. Many NEMS devices incorporate mechanical resonators, cantilevers, and doubly clamped beams. Applications involving mass sensing with cantilevers have a mass in the □ictogram and mass detection capability in the attogram [91] and zeptogram [92] range. Ekinci and Brugger [93] give an account of fabrication of NEMS cantilevers from Si, GaAs, AlGaAs, AlN, SiN, SiC, and nanocrystalline diamond all fabricated using e-beam lithography. The resolution achievable with e-beam lithography is limited by machine stability, beam diameter, and proximity effects. Yamazaki [90] gives an account of several factors associated with machine stability that can affect pattern resolution.

As the electron beam interacts with the resist layer and the underlying substrate, electrons can be scattered or absorbed. The scattered electrons can contribute to unwanted exposure in nearby areas of the photoresist layer. This type of exposure error is referred to as the "proximity effect." A Monte Carlo simulation of electron scattering for PMMA resist on a silicon substrate is shown in Fig. 9.33 [94]. Three main types of electron scattering are important in e-beam lithography: forward scattering, backscattering, and secondary electron emission. Forward scattered electrons can be minimized by using thin resist layers and high acceleration voltages. Backscattered electrons are largely responsible for proximity effects. Secondary electrons are a cascade of low voltage electrons that are created from the interaction of primary beam electrons with the resist or substrate materials. Secondary electrons produced within the resist layer account for the bulk of the resist exposure dose and can cause beam broadening on the order of 10 nm. Because secondary electrons have low energy, they travel only a short distance within the resist and thus do not contribute much to proximity effects.

The proximity effect is highlighted in Fig. 9.34a for an uncorrected exposure. Note that larger and more closely spaced features are more fully developed (less

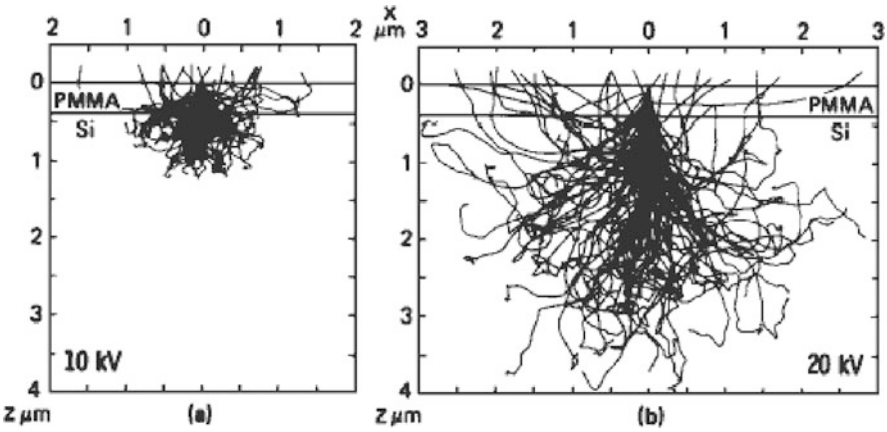

Fig. 9.33 Simulation trajectories for electrons in PMMA film on Si substrate (Reprinted with permission from [94], copyright 1975, American Vacuum Society)

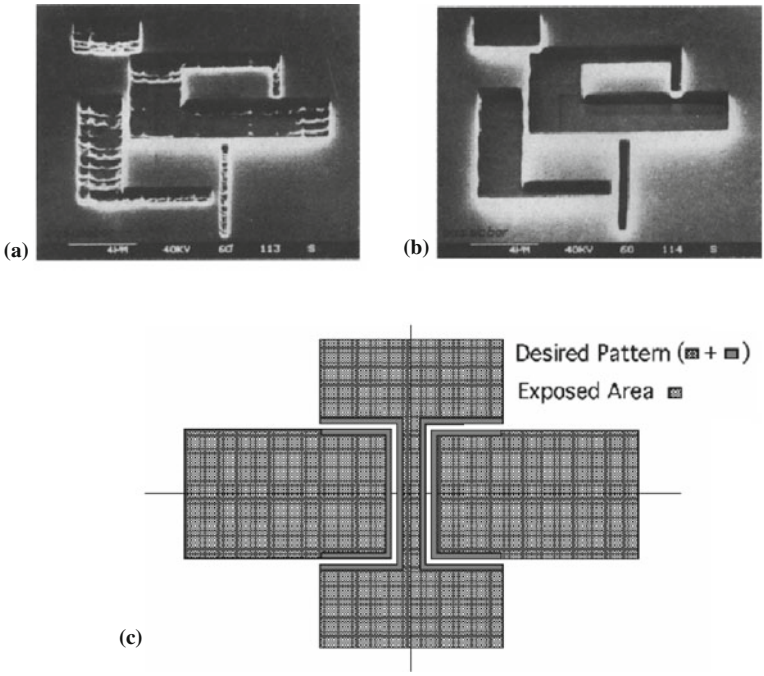

Fig. 9.34 Examples of proximity effect corrections (**a**) uncorrected exposure (noted by residual resist in patterned areas), (**b**) corrected exposure using dose modulation and (c) schematic illustrating the pattern biasing technique ((**a**) and (**b**) reprinted with permission from [97], copyright 1981, American Vacuum Society)

residual resist). To some extent, proximity effects can be minimized by assigning different dose rates to different sized features. Also film thickness and beam energy can be adjusted to minimize beam scattering under certain controlled settings. The most common way to correct proximity effects is to modulate the dose rate. There are several dose modulation techniques [95, 96] based on calculations that solve the shape-to-shape interactions. If the dose for a large-area feature is normalized to unity, then smaller and isolated features are assigned a somewhat larger dose. The result of the dose modulation proximity effect corrections is shown in Fig. 9.34b. An alternative approach to proximity effect corrections is to bias the patterning [95, 96]. As illustrated in Fig. 9.34c, pattern biasing compensates for the overdosing of closely spaced features by slightly reducing the size of the patterns. This is more easily implemented within an e-beam writing system but does not have the dynamic range of dose modulation.

Polymethylmethacrylate (PMMA) is a standard positive e-beam resist. Other resist materials include poly(2,2,2-trifluoroethyl--chloroacrylate) (EBR-9) which is an acrylate-based resist that is commonly used in mask writing applications and is ten times faster but also has ten times lower resolution than PMMA, and poly(butene-1-sulfone) (PBS) which is a high-speed positive e-beam resist

commonly used for photo mask patterning. See [98] for a more detailed discussion about different e-beam resists. A case study of PMMA e-beam resist is given below. For liftoff applications, a bilayer resist is typically applied to the substrate. For example, the 200-nm layer of methylmethacrylate (MMA) is spin coated onto the substrate and baked. A subsequent 200-nm layer of PMMA is then spin coated onto the substrate and baked. The MMA is more sensitive to the e-beam exposure than PMMA so it dissolves away at a faster rate during development producing an undercut below the edges of the PMMA features.

Several companies provide design and control software for performing e-beam lithography with an SEM. One of the most popular systems is the Nanometer Pattern Generation System (NPGS). Within the NPGS software application, parameters for controlling the SEM are stored in a run file and the desired patterns are drawn using DesignCAD software. Within a DesignCAD file, color coding is used to designate different dose exposures for different features. When a specific DesignCAD file is selected within a run file, separate beam control lists (referred to as layers) appear for each color. Within a given layer, magnification, distance between pixels, beam current, and doses can be specified. Some of these details are discussed in more detail in the case study below.

9.5.2 Ion Beam Lithography and Focused Ion Beam (FIB)

Beams of ions can be used to create patterns directly on the surface of a substrate (i.e., no photoresist). A focused beam of ions can be used to selectively remove or deposit material at a desired location. Whereas photons and electrons are effective for patterning soft materials, ions are sufficiently heavy to allow patterning/removal of hard materials such as metals, ceramics, and inorganic semiconductors. Therefore, a sacrificial resist layer is not needed as the ion beam can directly pattern (remove material from) the substrate. The removal process is referred to as sputtering, which is the removal of material by ion bombardment. This is a purely mechanical process. Popular ion sources include As, Be, Ga, and Si (for the related process of ion implantation in the semiconductor industry, Ar, B, and P are commonly used). Various ion-target interactions produce competing processes such as swelling, deposition, milling implantation, backscattering, and nuclear reactions. Ion species, incident angle, ion energy, and ion interaction with the target material are all important interactions. For appropriate ion energies, ion–target atom collisions can transfer sufficient energy to the atom to overcome binding energy (3.8 eV for Au and 4.7 eV for Si) resulting in the removal of the atom from the substrate surface (i.e., sputtering). Most typically, Ga^+ ions are used for focused ion beam lithography applications. A common type of source is a liquid metal reservoir that feeds metal ions to a sharpened (tungsten) needle. Such a source has a typical brightness of 10^6 A/cm^2 sr. A summary of ion sources and related properties can be found in Utke, Hoffmann, and Melngailis [99].

A FIB system consists of an ion source, ion optics, beam deflectors, and a substrate stage [100]. A review of these components and each of their functions and

designs is given by Tseng et al. [101]. The machine is similar to an SEM in both function and size. Typically the system is housed in a high-vacuum chamber (10^{-7} torr) to minimize scattering of ions from the beam. The vacuum chamber column is typically 30–50 cm tall and 15–20 cm in diameter [99]. The range of beam energies is 1–50 KeV. Typical spot size for these is about 50 nm. As in e-beam lithography, the ion beam is scanned across the substrate surface in the desired pattern and blanked off at points where no materials removal is desired. The amount of material removed for a given beam energy and diameter is determined by the time the beam is held at a specific point (dwell time) and the size of the beam step to an adjacent position (pixel spacing (PS)). The roughness of the milled structure can be minimized by using a smaller PS. For Gaussian beams with a standard deviation of the Gaussian distribution σ, smooth features have been produced with $\mathrm{PS}/\sigma = 1.5$ [102].

For a single pass (scan) of the ion beam, a V-shaped channel (line) is produced. The depth profile of such a line is shown in Fig. 9.35 from Tseng [102].

The profile is notably wider than the beam diameter indicating that the energy of scattered ions is large enough to cause sputtering. Also redeposition is evident at the side of the line-depth profile. For precision pattern formation both sputtering and

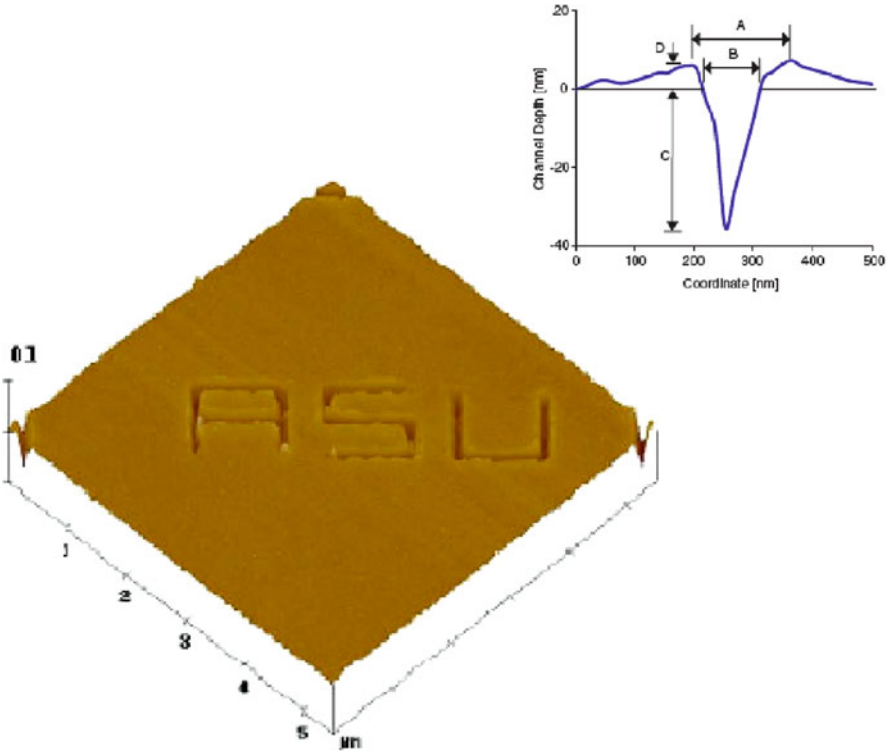

Fig. 9.35 AFM image of FIB single-line scan and associated height profile scan (Reprinted with permission from [102], copyright 2004, American Vacuum Society)

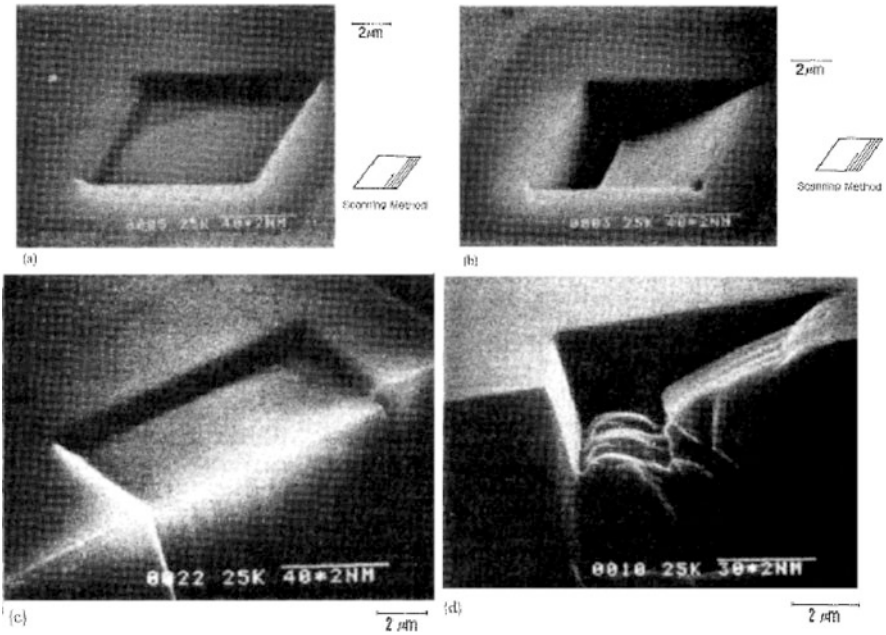

Fig. 9.36 FIB profile after single and multiple scans with the same total dose (Reprinted with permission from [103])

redeposition must be controlled. For many features in nano- and microfabrication, it is desirable to have vertical sidewall profiles and flat-bottomed features with high aspect ratios. To obtain most types of desired patterns with FIB, multiple passes must be performed. As shown in Fig. 9.36, multiple scans can lead to better feature profiles. Figure 9.36a, b were fabricated using the same total exposure time: for (a) a single pass was performed at 5 μm/s whereas for (b) 200 passes were performed at 1 mm/s. The total dose rate was the same for both cases (1.9×10^{18} ions/cm^2) but the single-pass feature shows an inclined bottom due to redeposition (keep in mind that for some applications such a feature profile may have advantages).

Because of the dynamics of redeposition, different scanning histories can produce dramatically different features. For example, Fig. 9.37 shows the difference between scanning from edge-to-center as opposed to scanning from center-to-edge. Review papers covering FIB and associated uses of these tools can be found in [100, 104–117].

9.5.3 Gas-Assisted Electron and Ion Beam Lithography

With the introduction of a precursor gas, both electron and ion beams can be used to perform either material removal or deposition. The removal process here is beam induced etching rather than sputtering as was presented above. For electron beam

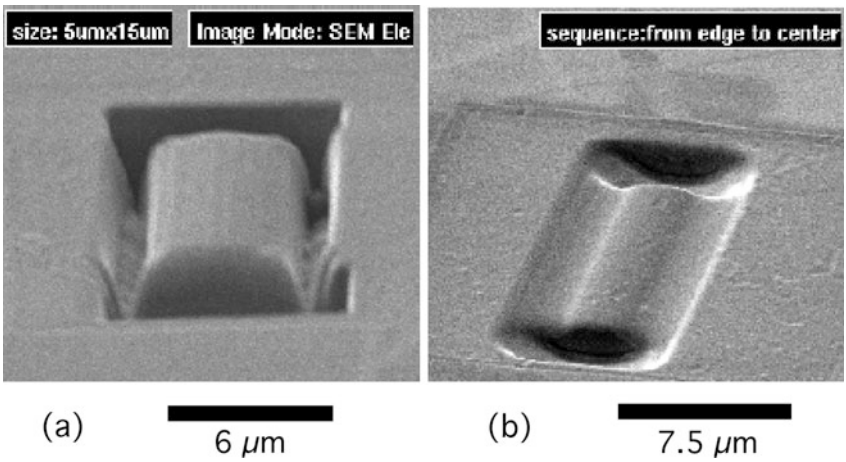

Fig. 9.37 FIB feature resulting in scanning from (**a**) center-to-edge and from (**b**) edge-to-center (Reprinted with permission from [118])

induced etching, the etching process is initiated by an excitation/dissociation of molecules in the precursor gas. The resulting gas molecules can then chemically react with atoms on the surface of the substrate forming volatile molecules containing substrate atoms that are easily removed in vacuum [119]. Precursor gases can also be added to an ion beam to combine the affect of etching and sputtering.

In addition to gas-assisted milling, electron and ion beams can also be used to perform gas-assisted deposition of materials [119, 120]. An example of a similar process is often observed in SEMs with the formation of thin-films resulting from contamination after the electron beam has scanned over a specific area on the surface of a sample. Silicone vacuum pump oil was deliberately used to form a polymer film on a substrate in an SEM as one of the first demonstrations of this technique [121, 122]. More recently the process of electron-beam-induced deposition has been exploited to deposit other desired materials [123–125]. van Dorp and Hagen [126] list more than a dozen materials and precursor gases that have been used for gas-assisted e-beam deposition. A compelling example of e-beam-induced deposition is illustrated using a tungsten precursor gas to fabricate a nanoscale map of the world on a Si_3N_4 substrate. The map is 230 nm across and contains height variations that represent mountain ranges around the world [127].

9.5.4 Dip-Pen Lithography (DPN)

Dip-pen lithography is an extension of scanning probe microscopy and atomic force microscopy (AFM). Instead of imaging a surface with a probe tip, the probe tip is used to deliver an "ink" to the substrate surface. An AFM tip is coated with an ink, and then when brought into proximity to a surface, a meniscus is formed between the

tip and surface. As the tip is moved with respect to the surface, ink is pulled off the tip (due to surface tension) and remains on the surface. In this way, sub-50 nm lines of material can be deposited either sequentially or in parallel (using multiple tips). Possible inks include small organic molecules, polymers, DNA, proteins, peptides, colloidal nanoparticles, metal ions, and sols. Both hard and soft substrate materials can be patterned, including insulating, semiconducting, and metallic substrates. The process of writing dots and lines is dependent on parameters such as temperature, humidity, writing speed, and contact force between tip and substrate, in addition to the physical and chemical properties of both the ink and substrate materials.

Biological samples are also possible with these schemes, rhodamine 6G (R6G) being a good example [128]. An ultrasharp Si_3N_4 tip was dipped into a 2×10^{-5} M solution of R6G for 30 s and then dried in N_2 gas. The pattern was then written on a mica substrate in a 23°C and 36% humidity air environment. The feature was written at both 0.01 and 0.04 μm/s. In this case, the 0.01 μm/s drawn feature generated a smooth and continuous line, whereas the 0.04 μm/s case produced a discontinuous line.

For the writing of chemical materials, DPN can be used to deposit nanometer-size features comprised of self-assembled monolayers (SAM). For example, high-resolution patterns of octadecanethiol (OTS) molecules on an Au film [129] and hexamethyldisilazane (HMDS) molecules on either a Si or a GaAs substrate [130] can be fabricated. Such SAMs can be used to fabricate high-resolution hydrophobic/hydrophilic patterns or chemical etch barriers for further processing. Zhang et al. [131] demonstrated DPN by writing 16-mercaptohexadecanoic acid (MHA) features onto a Au-coated Si substrate. The MHA pattern was used as a wet chemistry etch mask for the Au film and then the patterned Au layer was subsequently used as a reactive ion etch (RIE) mask for the Si.

9.5.5 Direct-Write Laser

Since their advent, the interaction of laser beams with materials has been of prime interest. Any laser process that modifies, adds, or removes material from a substrate can be thought of as a form of direct-write laser lithography. This is a maskless technique that scans the laser beam from point to point. This can allow for a one-step process that does not need a resist layer, backing, or wet chemistry. It is also not restricted to 2-D processing on flat surfaces. The laser beam and/or substrate can be moved in x, y, or z in a manner that can produce a 3-D feature of arbitrary shape. This can also be performed on arbitrary-shaped substrate surfaces not only flat wafers. Inasmuch as the laser beam can be programmed to raster in any desirable way, the need to design and fabricate new or multiple mask sets in eliminated. Several main components are needed: (1) laser source, (2) optics to shape and deliver the laser bean to a desired location, (3) substrate mount, and (4) relative translation between laser and substrate. Three main classes of laser direct-write lithography can be enumerated: subtractive, additive, and modification.

The subtractive mode typically involves photochemical, photothermal, or photophysical processes [132] of which ablation, surface cleaning, milling, and drilling are examples. The modification mode typically involves thermal methods causing a chemical or structural change. For example, thermally induced phase change from crystalline to amorphous, sintering, and changes in solubility (similar to UV exposure in photolithography but on a point-by-point processing). The addition mode typically involves the transfer of material from one substrate to a second substrate. For example, a bilayer film on a transparent substrate where the bottom layer is vaporized by the laser beam thus tearing off the top layer which is then propelled across the gap to be deposited onto the second substrate. The additive process is illustrated in Fig. 9.38 and has been used to fabricate a thin-film transistor (TFT) by Blanchet et al. [133].

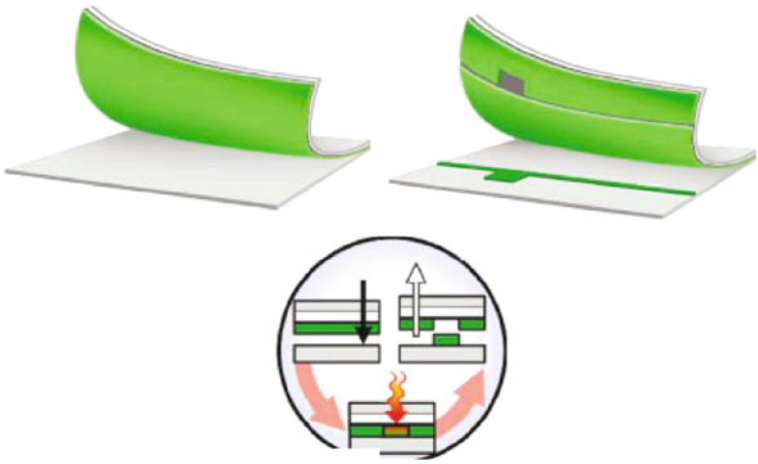

Fig. 9.38 Illustration of the direct-writing laser additive process to transfer one material onto a second substrate (Reprinted with permission from [133], copyright 2003, American Institution of Physics)

Laser-induced chemical-vapor deposition (LCVD) is an example of the modification method [134] that can be used to form 3-D structures on a substrate. The substrate is surrounded by material in the gas phase and the laser beam is focused to the desired location to induce a chemical reaction to change the gas into a solid form. The laser beam is moved around to create the desired structure [135]. Two types of reactions are generally used, either decomposition reactions or combination reactions. These reactions can be either photolytic or pyrolytic. Duty et al. [135] list materials that have been deposited using pyrolytic methods. The list includes metals such as Al, Cu, and Au; semiconductors such as Si and Ge; and ceramics such as Si_xN_y, SiC, and TiN. The list also includes starting reagents along with various processing parameters. Figure 9.39 illustrates the LCVD process where a laser beam is depicted to induce a chemical reaction to convert a gas or liquid phase into a solid as

Fig. 9.39 Schematic illustration of LCVD process (Reprinted with permission from [136])

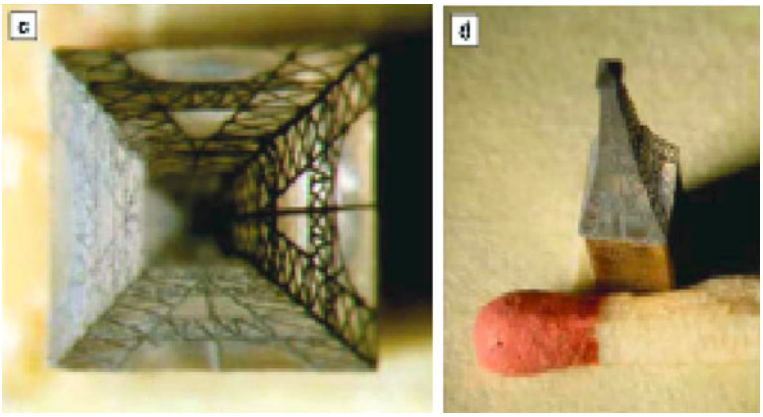

Fig. 9.40 Three mm tall replica of the Eiffel Tower fabricated using LCVD (Reprinted with permission from [136])

the laser is moved. Figure 9.40 shows a 3 mm tall replica of the Eiffel Tower fabricated using LCVD to deposit Al features onto a preformed polycarbonate structure.

9.5.6 Stereolithography and Microstereolithography

Stereolithography (SL), sometimes referred to as rapid prototyping, was first introduced in 1981 [137–139]. In its simplest form it employs a laser source, a vat of photocurable polymer, a sample holder, and a means of moving the beam relative to the liquid polymer. A CAD-generated design is used to control the relative motion between the laser and the vat causing photopolymerization where the laser interacts with the liquid polymer. This mapping/polymerization produces a solid structure defined by the CAD control and held in place by the sample holder. The process is shown schematically in Fig. 9.41.

The process can also be performed with solutions loaded with photocurable metallic or ceramic suspensions. In this way, metal or ceramic parts can be fabricated. If the photocurable solution is replaced by a powder, 3-D structures can be fabricated by laser-induced sintering.

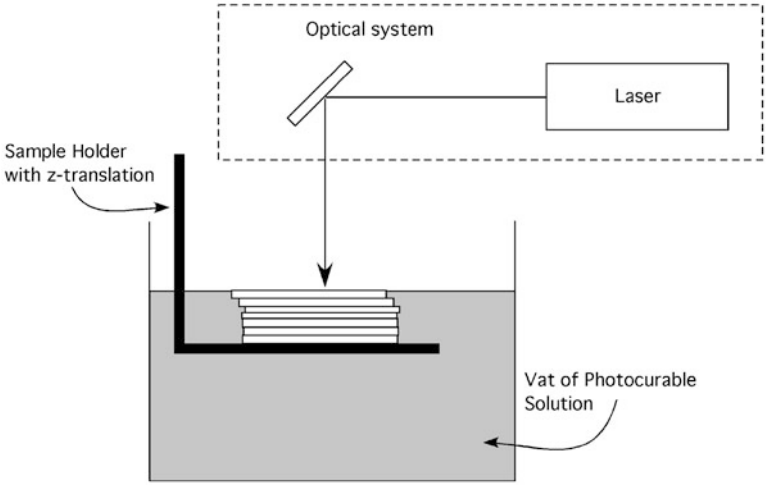

Fig. 9.41 Schematic illustration of stereolithography system (Reproduced with permission from [140], copyright 2002, Wiley-VCH)

Microstereolithography (MSL) is an extension of stereolithography to the micron scale. Instead of employing a laser spot size of around 200 μm, the laser spot is focused down to 1–2 μm. Also the parts are small enough to be self-supporting and so the support structure generally needed for SL-formed parts may not be needed for MSL. Photopolymerization happens on the surface of the vat as the beam is scanned in 2-D ($x-y$). Once the desired layer is formed, it is lowered to allow fresh liquid to cover the previously formed structure and a new layer is polymerized on top of the existing feature. In this way a 3-D structure is generated layer by layer. For SL the polymerized layer thickness is on the order of hundreds of μm's thick whereas for MSL it is on the order of microns thick.

Two main types of MSL exist, scanning and projection, of which the scanning mode is most widely used. The size and shape of structures fabricated using a single beam of UV light is limited by the physical size of the focused beam and the fact that the polymerization occurs at the surface of the vat as the beam (or vat) is scanned in 2-D. The scanning aspect of SL and MSL can introduce a speed limitation for the fabrication of structures. Because polymerization takes place at the surface of the vat, the UV light can be projected through a mask (as in projection photolithography). In this case polymerization across the entire desired area of the surface happens simultaneously thus removing the need for any scanning in the $x-y$ direction. Subsequent layers can be polymerized by lowering the substrate to allow more uncured liquid to cover the surface and then repeat the exposure. The shape of structures is limited by the number of different masks available and the ability to align subsequent masks to previous polymerized layers. This limitation can be overcome by using dynamic liquid crystal masks, or using a micromirror array to project patterns. Figure 9.42 shows an example of features that can be fabricated using MSL.

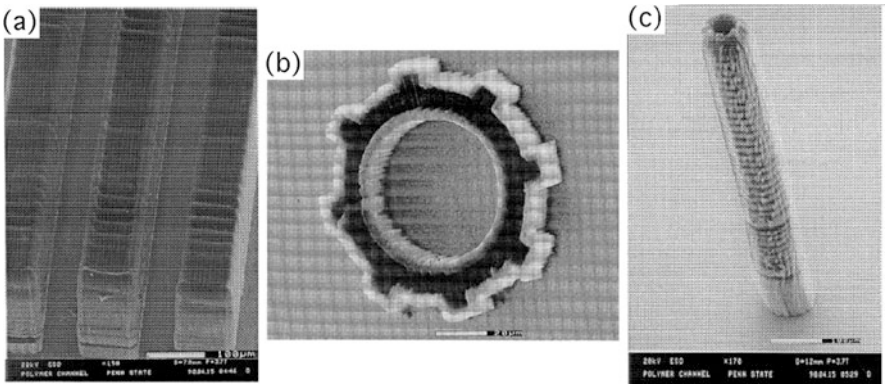

Fig. 9.42 Illustration of various structures fabricated using MSL: (**a**) microchannels, (**b**) gear, and (**c**) microtube (Reprinted with permission from Elsevier, [141])

A limitation of single-photon processing is that polymerization occurs at the surface of the vat. This can be overcome by using a two-photon process. The process employs two intersecting infrared (IR) beams. At the point of intersection, the liquid polymer can polymerize only by simultaneous absorption of two photons. This produces a spot size below the diffraction limit of a single beam and allows the polymerization to take place anywhere within the vat, not just at the surface. This also allows for small structures that are truly 3-D. The two-photon absorption process can take place either as a resonant excitation or a simultaneous absorption. In the resonant-excitation mode the first photon is absorbed to create a real excited state with a lifetime on the order of $10^{-4} - 10^{-9}$ s. Polymerization can occur only if a second photon is absorbed by the monomer while in the excited state. In the simultaneous absorption process, no intermediate excited state exists. Therefore both photons must be absorbed within 10^{-15} s of each other [142].

The two-photon absorption process is a nonlinear effect with polymerization dependent on the square of the photon density. This phenomenon is responsible for a resolution better than the diffraction limit of the single-beam profile. Figure 9.43 shows examples of features fabricated using two-photon MSL. Note that whereas the features in Fig. 9.42 are in the hundreds of microns, these structures are on the micron scale with submicron details!

9.6 Print/Imprint Lithography

Printing is an ancient art dating back to the eighth and ninth centuries A.D. An example of such a printed work is the Diamond Sutra which was fabricated using a technique referred to as block printing. Printing using movable type based on clay [147] was invented in 1041 and based on metal [148] in 1232. Ushering in a more modern style of printing, Gutenberg is credited with having invented the

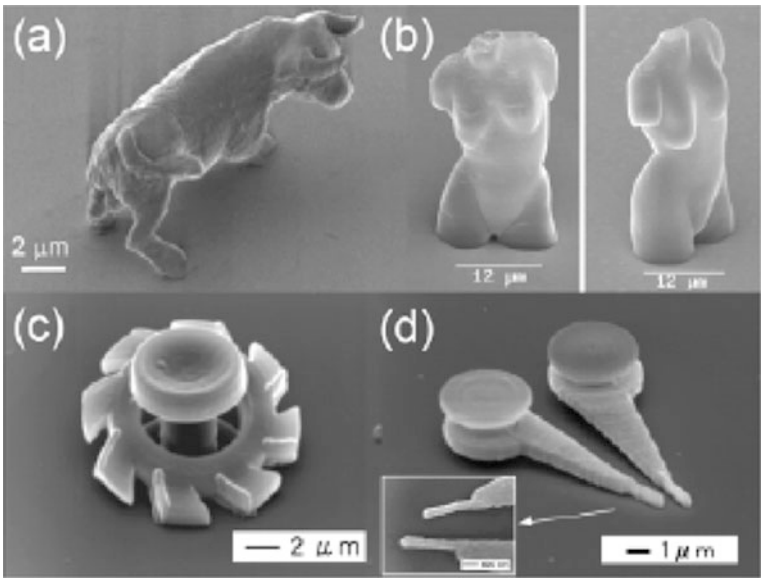

Fig. 9.43 3-D microstructures produced by multiphoton microfabrication: (**a**) microbull model [143]; (**b**) Venus model [144]; (**c**) microturbine [145]; (**d**) nanotweezers [146] (Reproduced with permission; copyright Wiley-VCH)

modern printing press in the 1450s. Lithography, which is a form of printing based on a planographic process that relies on patterning inks onto a flat surface using hydrophilic and hydrophobic interactions, was invented in 1798.

The semiconductor industry has developed a form of pattern transfer for the fabrication of solid-state electronics based on Si called photolithography. As described in Section 9.2 above, photoresist is applied to and patterned on Si wafer substrates in the manufacturing of computer chips and on glass substrates in the manufacturing of flat-panel displays. Either way, the fabrication methods are limited to batch processing of finite size substrates. Serious efforts are underway to develop larger-scale manufacturing processes that can fabricate electronic devices in a continuous fashion in a manner more similar to the fabrication of magazines or newspapers. In order to accomplish this, the added requirement of flexible substrates will be needed.

As a testimony to the importance of such efforts, Xia and Whitesides [20] list no fewer than 18 different nonphotolithographic patterning methods being developed to fabricate devices at the micrometer and nanometer length scales. The table is reproduced here as Table 9.5. The earliest reference dates back to 1974, with a majority of the references coming from the 1990s. Even though printing is an old technique with a rich history in fabricating and/or reproducing images and writing, it is being revisited as a method for fabricating active electronic devices, circuits, and MEMS components.

Table 9.5 Nonphotolithographic methods for micro- and nanofabrication[a]

Method	Resolution[b]	References
Injection molding	10 nm	[149–154]
Embossing (imprint)	25 nm	[155–163]
Cast molding	50 nm	[164–166]
Laser ablation	70 nm	[167–172]
Micromachining with a sharp stylus	100 nm	[173]
Laser-induced deposition	1 μm	[174–176]
Electrochemical micromachining	1 μm	[177]
Silver halide photography	5 μm	[178–180]
Pad printing	20 μm	[181]
Screen printing	20 μm	[182]
Inkjet printing	50 μm	[24, 183–186]
Electrophotography (xerography)	50 μm	[187, 188]
Stereolithography	100 μm	[189–192]
Soft lithography		[18, 21, 193, 194]
Microcontact printing (μCP)	35 nm	[195, 196]
Replica molding (REM)	30 nm	[197]
Microtransfer molding (μTM)	1 μm	[198]
Micromolding in capillaries (MIMIC)	1 μm	[199]
Solvent-assisted micromolding (SAMIM)	60 nm	[200]

[a]These numbers do not represent ultimate limits
[b]The lateral dimension of the smallest feature that has been generated
Reproduced with permission from [20], copyright 1998,Wiley-VCH

Various types of printing techniques are reviewed here as they pertain to the patterning and/or assembly of components needed to fabricate active electronic devices and MEMS components.

The printing industry has been primarily interested in reproducing pictures and/or text on a page. Both are passive features composed of two components: an ink and a substrate (the page). The ink is designed for passive color and high visual contrast against the substrate. The substrate can be made from various materials such as paper, plastic, metals, glass, and so on. For the printing of active devices the substrate materials may not change much but the inks will have to be very different.

Visual contrast and passive color will no longer be important properties. Admittedly, transparency over certain optical ranges may be important for some applications; however, active inks will primarily be chosen for their conductivity, semiconducting properties, insulating properties, and mechanical properties among others. Such inks will need to be prepared and processed in ways that optimize these properties. This will most likely require techniques very different from those used to prepare and process passive inks, therefore traditional printing techniques are not discussed. Rather, the discussion is dedicated to introducing and reviewing printing methods being developed that will meet the needs for printing active materials.

9.6.1 Inkjet Printing

Inkjet printing [22] is a digital form of printing that can be performed either in a continuous or a drop-on-demand mode. For the continuous mode, a stream of droplets passes through a set of signal drive electrodes. An electrical pulse to the electrodes causes a droplet to be deflected to the substrate. Undeflected droplets are collected and recirculated back to the ink reservoir. For the drop-on-demand modes, a piezoelectric pulse is used to create a droplet by pushing ink through a nozzle. Nozzles are typically 20–30 μm in diameter and create ink droplets of about 10–20 pL. The droplet-on-demand mode results in better printing quality when compared to continuous mode inkjet printing with feature resolution on the order of 20–50 μm for standard inkjet printing.

Viscosity and surface tension are important parameters of the ink. Ink must fill the nozzle in approximately 100 μs and not drip out between demands. This typically requires a viscosity range of 2–100 cp and a minimum surface tension of about 35 mN/m. To prevent the ink from drying and clogging the nozzle, a liquid such as ethylene glycol can be added at a level of 10–20%. If an ink contains particulates, the particulates must remain uniformly suspended in the ink and not contribute to clogging in the nozzle. This usually requires a particulate size less than 1 μm.

High-molecular-weight polymers tend to be too viscous to print easily using inkjet printing. However, inkjet printing of waxy and low-molecular-weight polymers is possible. Printed droplets can exhibit pinholes and can have a tendency to bead up when printed onto nonabsorbent substrates (such as plastics). Also, edge roughness and printing resolution can be affected by droplet-spreading characteristics and can be difficult to control. Some materials' printing problems can be overcome by incorporating additives into the ink that can be postprocessed, such as the addition of UV curable polymers. Also precursor materials can be used directly as inks that are postprocessed, such as precursor metal solutions.

A wide range of materials has been successfully inkjet printed. Calvert [22] lists nanoparticle suspensions, sol-gels, conducting polymers, ceramic powders, solder, DNA, and proteins as materials that have been inkjet printed, all of which must either be suspended or dissolved. Some organic semiconductor materials tend to be insoluble (pentacene, e.g.) and, therefore, soluble forms of these materials have been investigated for use in specific inkjet applications [201]. Other organic semiconductor materials tend to be very sensitive to drying conditions such as poly(3-hexylthiophene) (P3HT) [202]. In either case, inkjet printing of these materials has, to date, typically resulted in low-quality films.

There have been attempts to improve the resolution associated with inkjet printing. One method used an undisclosed print head technology as part of a superfine inkjet printing system [203]. This system was reported to have achieved a line width of 3 μm. Also, Sirringhaus et al. have developed a droplet-on-droplet technique in which the second droplet does not wet the first droplet [204]. When printed, the second droplet slides off the first droplet, producing a sub-100 nm gap between the printed features, which are then used as source/drain electrodes for an OTFT device.

9.6.2 Soft Lithography

Photolithography has been used for decades in the fabrication of inorganic electronics; however, it has several disadvantages that limit its usage for nontraditional materials: it allows for very little variation in the chemistry of either the resist layer or the substrate and it can only be performed on flat surfaces in a batch-processing mode.

In an attempt to go beyond the limitations of photolithography, soft lithographic methods have been developed, as listed in Table 9.5. Soft lithography encompasses techniques such as microcontact printing [195, 196] (μCP), replica molding [197] (REM), microtransfer molding [198] (μTM), micromolding in capillaries [199] (MIMIC), and solvent-assisted micromolding [200] (SAMIM). These techniques all have in common a patterned elastomeric mold or stamp (typically made from polydimethylsiloxane (PDMS)). Because the stamp (mold) is flexible, these techniques are compatible with nonflat surfaces.

Soft lithography techniques have also been used to print patterned layers from PDMS stamps onto substrates. For example, Au evaporated onto the patterned surface of a PDMS stamp and then treated with a thiol- terminated self-assembled monolayer (SAM) has been printed onto a GaAs substrate [205]. Also PDMS features have been printed onto Si substrates by treating the patterned surface of a PDMS stamp with a fluorinated SAM and then adding an extra layer of PDMS [206]. When contacted to the Si substrate, the top layer of PDMS can be transferred to the Si surface. Childs and Nuzzo [206] provide detailed procedures for preparing PDMS films and bonding such films to Si substrates to produce both closed and open patterns on the substrate. Below, a case study is provided for the preparation of PDMS films.

Unlike photolithography, which transfers a pattern using optical techniques, soft lithography is a direct printing method. Also, the stamp (mold) can be replicated from a reusable master template. Therefore, soft lithography has the potential to be a less complex and less expensive method of patterning compared to photolithography. In addition, soft lithographic techniques can be used to directly pattern a wider range of surfaces comprised of polymers, sol-gels, biological materials, organic thin-films, and colloidal materials, in addition to inorganic surfaces.

9.6.3 Nanoimprint Lithography (NIL)

In addition to the limitations discussed above, pattern sizes produced by photolithography are limited by the resolution of the optical system used to transmit light through the mask. Over decades of research, this resolution limit has been steadily reduced at the expense of increased complexity and cost of the fabrication equipment. Nanoimprint lithography (NIL) [156] has been developed as a patterning technique that can simultaneously improve pattern resolution and reduce both equipment complexity and cost. It is based on a rigid template containing a

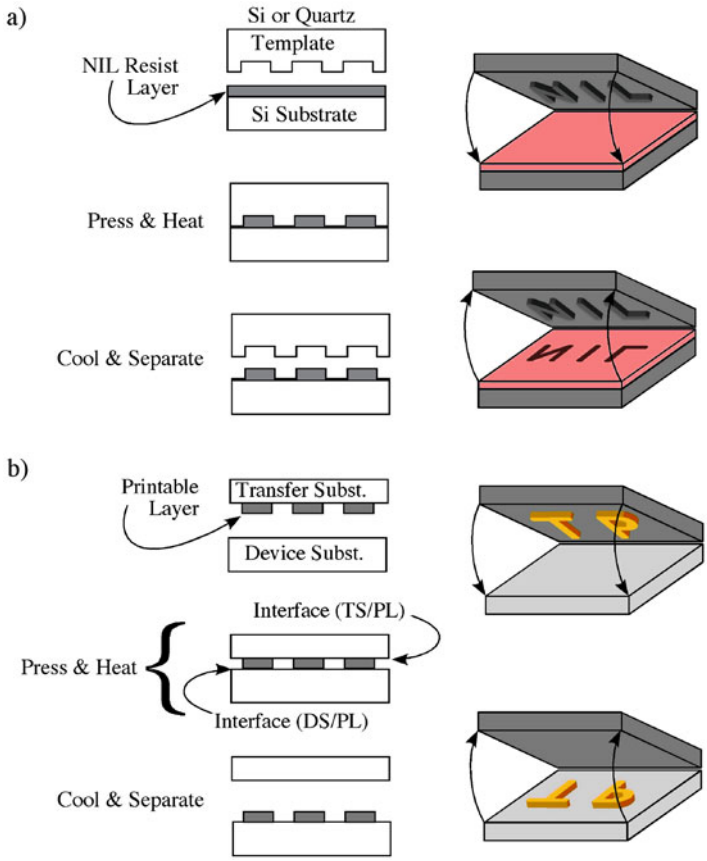

Fig. 9.44 (**a**) Nanoimprint lithography (NIL) and (**b**) the transfer printing method (Reprinted with permission from [219], copyright 2007)

patterned surface. The template is pressed into a resist layer that has been coated onto a substrate. Two types of NIL have been developed and are referred to as hot and cold embossing. Hot embossing uses a thermoplastic resist layer and cold embossing uses a UV-curable liquid layer. The general process is illustrated in Fig. 9.44a.

In hot embossing, the patterned template surface is placed in contact with the thermoplastic resist layer. The resist layer is heated up above its glass transition temperature and the template is pressed into the resist layer. After a specified time the resist layer is cooled down below its glass transition temperature and the pressure is released. The template is then removed to reveal a replica of the template surface contained in the surface of the resist layer.

In cold embossing, sometimes referred to as step-and-flash imprint lithography [207] (SFIL), the patterned template surface is placed in contact with a UV-curable liquid layer. The resist layer is then cured by exposure to UV light. The template

is then removed to reveal a replica of the template surface contained in the surface of the resist layer. In this case, the template (or possibly the substrate) must be transparent to UV light. This is similar to replica molding [197] which typically uses a flexible template, however, SFIL has been developed using a rigid transparent template.

Several variations of hot embossing have been reported [208, 209] as a means of reducing the operating pressure and/or temperature. One technique eliminates the resist layer entirely [210]. NIL is also being expanded to include imprinting into a variety of active materials as opposed to sacrificial resists [211]. The resolution of NIL has been demonstrated to be at the 10 nm level [212]. Most of the developmental work associated with NIL is directed toward inorganic substrates and is targeted as a disruptive technology competing against photolithography and e-beam lithography. Schift [213] provides a review article that discusses a wide variety of processing issues and materials parameters associated with conventional NIL. NIL techniques have begun to enter the realm of MEMS fabrication largely associated with microfluidics applications incorporating small-diameter flow channels. Nanochannel fabrication for applications involving DNA stretching and sequencing, protein separation, and drug delivery are discussed by Kim et al. within Chapter 13 in the book *Unconventional Nanopatterning Techniques and Applications* [15].

Many variations of NIL are being developed in order to address specific applications that are not so easily accomplished by conventional techniques. For example, rather than competing with photolithography, NIL can be combined with photolithography to simultaneously pattern large and small features. Work on combining nanoimprint and photolithography (CNP) [214, 215] uses a hybrid mold that is at once both a photomask and an NIL template. In addition, large volume roll-to-roll NIL (R2RNIL) has also been envisioned for high-speed manufacturing. A body of work designed to integrate NIL fabrication methodologies into MEMS-based systems is beginning to emerge in the literature. S. Park and H. Schift have contributed an entire chapter discussing NIL technology for biological application in a book devoted to bio-MEMS [216]. A variety of topics is presented such as nanofluidic devices, engineered nanopores, and nanopatterns defined by variations in surface chemistry or protein coverage. Applications such as battery and fuel cell technologies can greatly benefit from increased surface area coatings. Zhang et al. have incorporated NIL processing methods into the design and fabrication of MEMS-based fuel cells as a means for increasing reaction surface areas among fuel, catalyst, and electrolytes [217]. X. Fan et al. has utilized NIL as a low-cost method for the fabrication of PMMA microlens arrays on a Si substrate [218].

9.6.4 Transfer Printing

As is illustrated in Fig. 9.44b, the same processing method used for NIL can be used to transfer a patterned layer (printable layer) from one substrate (the transfer substrate) to a second substrate (the device substrate). The only requirement is that

the printable layer adheres more strongly to the device substrate than to the transfer substrate. This process is referred to as transfer printing. In general, the transfer printing process does not rely on temperature, but only on contact of the printable layer to the surface of the device substrate where an appropriate differential adhesion exists between the two interfaces containing the surfaces of the printable layer. This is the same governing principle seen in decals for detailing model cars and airplanes or for a child's temporary tattoos.

It is with such a process that we wish to develop the ability to fabricate flexible electronics and MEMS devices. Plastic substrates present an obvious choice of materials for this application, not only because they are flexible, but also because of their low density, optical clarity, low cost, compatibility with roll-to-roll processing, and so on. The process is simple in concept but has the potential to allow a wide variety of dissimilar materials to be combined onto a single substrate in ways difficult if not impossible to achieve with conventional methods. Figure 9.45 shows examples of metallic, organic, and carbon-based materials that have been printed onto a plastic substrate.

Figure 9.45a illustrates a 50 μm wide serpentine Au electrode printed onto a Kapton substrate. The Au feature was fabricated on a Si wafer transfer substrate using standard photolithography. Prior to printing, the transfer substrate was spin coated with a layer of polyimide. The Au/polyimide bilayer was then printed onto the Kapton substrate. The profilometer scan shows that the printed Au feature protrudes above the Kapton surface. In general, Au features from 200 nm wide lines up to full 3 in. diameter films have also been successfully printed onto PET substrates.

Figure 9.45b illustrates a 50 nm thick pentacene film printed onto a PET substrate. In this example, a Pn film was thermally evaporated onto a SiO_2/Si wafer transfer substrate. Prior to printing, an Au electrode was evaporated onto the transfer substrate such that it also partially covered the Pn film. The three resulting regions (Au, Au/Pn, and Pn) were all successfully transfer printed onto the PET substrate. Pn has also been printed onto Au, PC, latex, nitrile, PVC, and PMMA surfaces, to name a few examples. In addition, Pn films can be patterned by printing against a patterned photoresist film.

Figure 9.45c shows an example of a CNT network printed onto a PET substrate that contains previously printed Au electrodes. The CNT network was grown by CVD onto a SiO_2/Si wafer transfer substrate. Similarly, graphene has also been printed onto Au and polymer surfaces.

The last example shown in Fig. 9.46 illustrates the ability to print inorganic features directly onto a prepatterned plastic or elastomer substrate. Here a Si grid is shown printed onto a patterned PC substrate. Others have used PDMS as an intermediate substrate for the printing of Si features using a kinetic printing process where the adhesion is controlled by the speed at which the intermediate substrate is removed. For all these illustrations, adhesion to the first substrate must be less than adhesion to the final substrate. Efforts to establish printing parameters for a wide variety of materials have relied on the engineering of surface energies. Self-assembled monolayers (SAMS) can provide an easy effective tool for establishing the desired surface energy of a given substrate [222]. For example, the adhesion of

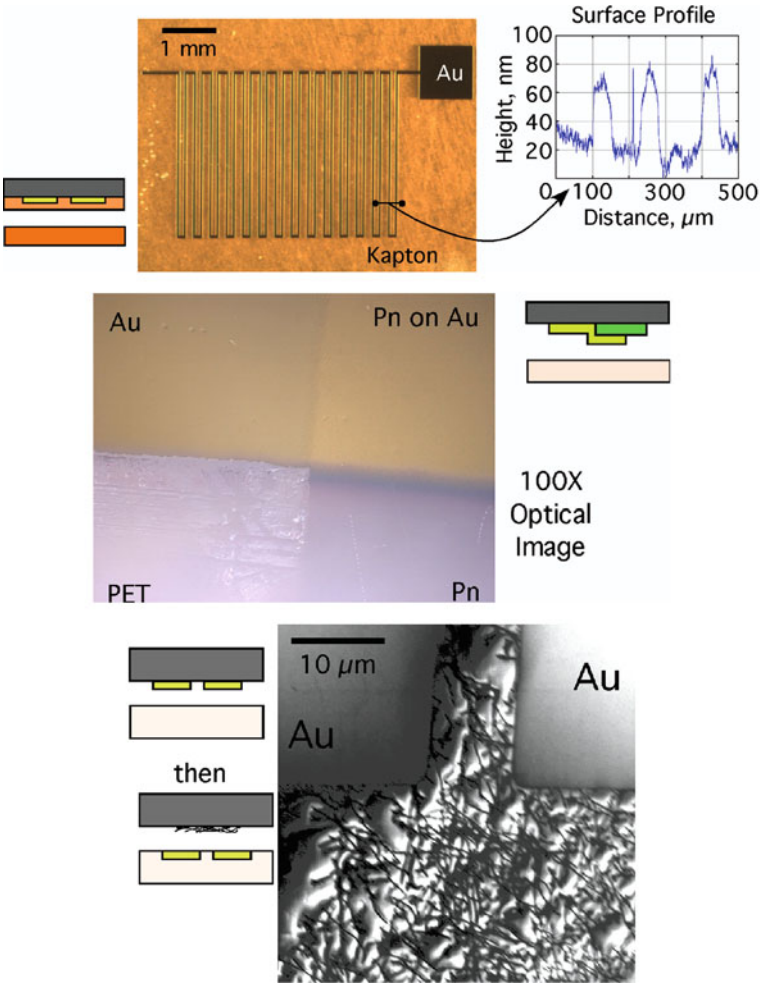

Fig. 9.45 Transfer printed films: (**a**) Optical image of a Au serpentine line transfer printed onto a Kapton substrate; (**b**) optical image of a Pn film (and Au film) printed onto a PET substrate; and (**c**) SEM image of a CNT network printed onto a PET substrate. The substrate contains previously printed Au electrodes (**a**) and (**c**). Reprinted by permission from [220]. (**b**) Reprinted by permission from [221]

Au to Si is low enough to allow Au to be easily printed onto a plastic substrate (such as PET or PC). However, the adhesion of Al to Si is too high for the Al print from a bare Si substrate.

If, however, the Si surface is coated with a TDFS SAM prior to Al deposition, then the adhesion of the Al to the Si substrate surface can be reduced to the point where it can be successfully printed. The same is true for PMMA films. Also P3HT has been shown to print better from OTS-coated Si as compared to bare Si substrates. In addition to lowering the adhesion between the printable layer and the

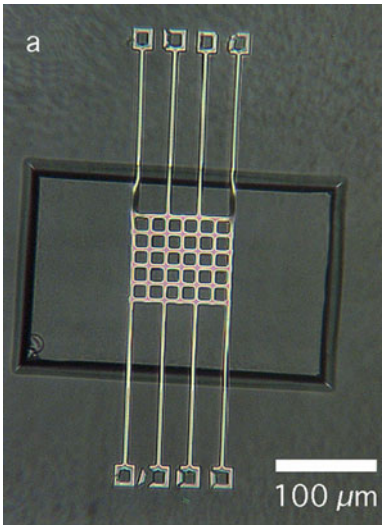

Fig. 9.46 Micrograph showing a Si grid resonator printed over a preprinted cavity on PC film

transfer substrate, the adhesion between the printable layer and the device substrate can be increased. This can be accomplished in various ways using SAMS [223], plasma treatments [224], increased surface roughness, and so on. The transfer printing method described above has been implemented to assemble dissimilar materials sequentially onto a single substrate for the fabrication of both electronic devices such as thin-film transistors and mechanical devices such as thin-film resonators; examples of both are shown in Fig. 9.47.

9.7 Case Studies

In a commercial semiconductor device fab or MEMS foundry, the lithography is performed using large-diameter wafers (8–12 in. diameter). The wafers are mounted in cassettes that can be loaded into each machine or solvent bath for automated processing. In a research and development lab it is more typical to handle smaller-diameter wafers (3–6 in.) or even pieces of a wafer such as $1 \times 1\,\text{cm}^2$. The following case studies are geared toward the processing methods in a research and development lab.

9.7.1 Case Study 1: Substrate Cleaning-RCA Clean(s)

Werner Kern developed the basic procedure in 1965 while working for Radio Corporation of America (RCA). The full cleaning procedure consists of three steps:

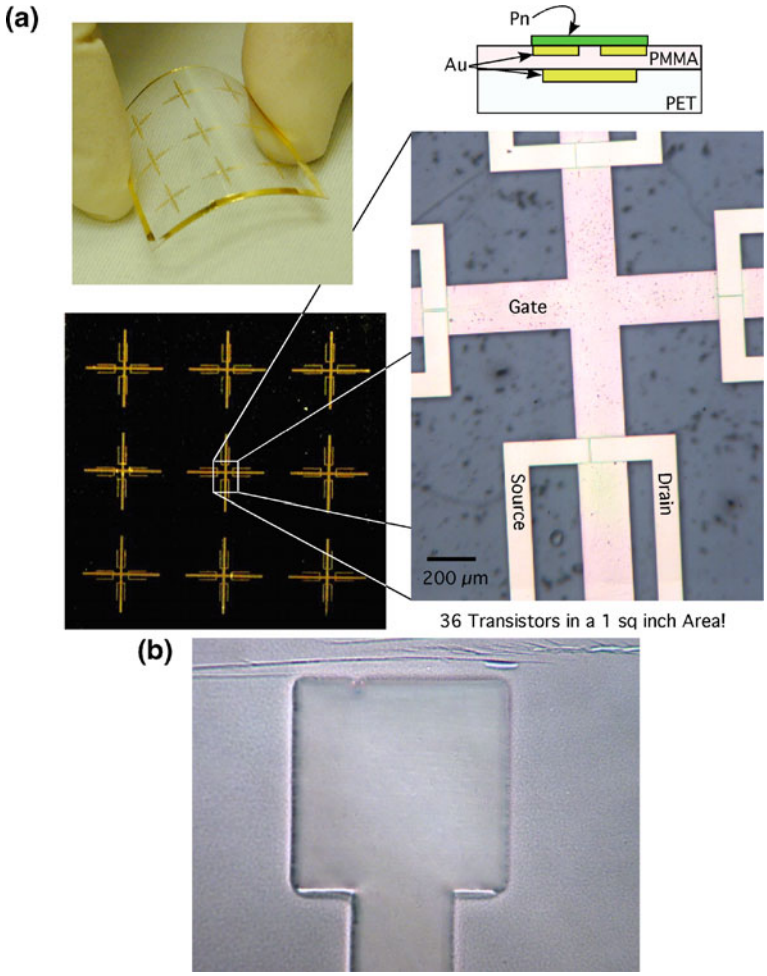

Fig. 9.47 (**a**) Electronic and (**b**) mechanical devices assembled onto plastic substrate using transfer printing methods (Reprinted by permission from [220] and [225]

1. Removal of the organic contaminants (organic clean)
2. Removal of thin oxide layer (oxide strip)
3. Removal of ionic contamination (ionic clean)

9.7.1.1 Recipe Steps

Organics Removal (RCA1)

1. Submerge substrate in a 1:1:5 solution of NH4OH + H_2O_2 + H_2O at 75–80°C for 15 min.

2. Rinse in DI water.
3. Blow dry with N_2 gas.
4. Put in 120°C oven for 20 min.

Oxide Removal (RCA2)

1. Submerge substrate in a 1:50 solution of $HF + H_2O$ (buffered oxide etch -BOE) at 25°C for 1 min.
2. Rinse in DI water.
3. Blow dry with N_2 gas.
4. Put in 120°C oven for 20 min.

Ionic Contamination Removal (RCA3)

1. Submerge substrate in a 1:1:6 solution of $HCl + H_2O_2 + H_2O$ at 75–80°C for 15 min.
2. Rinse in DI water.
3. Blow dry with N_2 gas.
4. Put in 120°C oven for 20 min.

9.7.1.2 Notes

In many cases, removal of organic contamination is sufficient; however, further cleaning can be performed for removal of oxide layer and ionic contamination.

9.7.2 Case Study 2: Substrate Cleaning, O_2 Plasma Clean

The O_2 plasma cleaning method is primarily used to remove organic contaminants. One of the main advantages of plasma cleaning is that it does not employ wet chemistry. This case study is based on using a PlasmaTherm 970 Reactive Ion Etcher (RIE).

9.7.2.1 Recipe Steps

1. Load wafer into the plasma chamber.
2. Run O_2 plasma for 5 min at 200 W, 100 mtorr, 20 SCCM.
3. Vent chamber and remove wafer.

9.7.2.2 Note

Depending on processing conditions, plasma treatments have the potential to affect the roughness of the substrate surface. Usually the roughness increases.

9.7.3 Case Study 3: Substrate Cleaning, Solvent Clean

The solvent clean is a general-purpose method that can be performed in most any laboratory environment.

9.7.3.1 Recipe Steps

1. Submerge a substrate for 5 min in separate beakers of each of the following solvents.
   Trichloroethylene (TCE)
   Acetone
   Methanol
   2-propanol (IPA)
2. Rinse with fresh IPA.
3. Blow dry with dry N_2 gas.
4. Place in 120°C oven for 20 min.

9.7.3.2 Note

As the wafer is transferred from one bath to the next, be sure that the wafer surface stays wet and that no part is allowed to dry before entering the next bath – never let the wafer surface dry – always keep the wafer surface wet. For example, acetone tends to leave a very thin residue on the substrate surface that is extremely difficult to remove. As an optional step, ultrasonic agitation can be added to each solvent bath during cleaning.

9.7.4 Case Study 4: Positive Photoresist Processing: General Processing for Shipley 1800 Series Photoresist

This case study is adapted from processing notes from the Cornell Nanofabrication Center. Shipley 1800 series photoresist is a general-purpose, broadband (365–436 nm) positive resist. It is best suited for use on a 5x stepper and HTG Contact Aligner. It is not recommended for the 10:1 Stepper. The 1800 series resists include S1805, S1813, S1818, S1818J (dyed), S1827 (0.5, 1.3, 1.8, and 2.7 μm). This case study assumes that the substrate is a Si wafer.

9.7.4.1 Recipe Steps

1. (Optional) After wafer cleaning, perform a dehydration bake by putting the substrate in a drying oven at 150°C for 30 min.
2. Mount the substrate onto a spin coater and verify that the spin coater is set up with the appropriate parameters.

3. Apply an HMDS treatment to the substrate surface. Using a disposable pipette, syringe, or eye-dropper, apply HMDS solution to the entire substrate surface. Allow to sit for 10 s and then spin for 30 s at 3000–5000 rpm on a spin coater.
4. Dispense photoresist onto the middle of the substrate and spin at the desired speed for 20–30 s (thicker films take a longer time to reach uniformity). Substrate surfaces containing topography may benefit from slower rate rates.
5. Soft bake by removing the substrate from the spin coated and placing of a hot plate. Bake for 1–2 min at 90–115°C. Thicker films benefit from longer baking times.
6. Mount the photoresist coated substrate and the appropriate photo mask into the contact aligner (see contact aligner case study) and expose for the desired time. Exposure time will vary depending on resist thickness, baking time, substrate reflectivity, and so on.
7. Develop for 1 min in AZ 300MIF or CD 26. Can also use MF-321 (no dilution), or Microposit Developer Concentrate (MDC) diluted 1:2 (MDC minimizes Al etch rate but is not metal-ion free). Use agitation while developing.
8. (Optional) Hardbake at 115°C for 1 min on the hot plate, or 20–30 min in the oven. The hardbake serves to promote adhesion during wet etching or increase selectivity during dry etching.

This case study is generic with some processing conditions not specifically stated. Below is a specific case study designed for S1813. Positive photoresists can be sensitive to humidity. After UV exposure it may be advantageous to leave the photoresist coated substrate sit out in the cleanroom for 30 min. This allows the photoresist layer to absorb humidity which tends to minimize the production of bubbles in the resist layer during postbake.

9.7.5 Case Study 5: Positive Photoresist Processing: Specific Processing for Shipley S1813

This case study is adapted from the Ph.D. thesis titled "Design of MEMS-based Tunable Antennas, Organic Transistors, and MEMS-based Organic Control Circuits" by Madhurima Maddela, Auburn University. The processing steps are designed specifically for Shipley S1813 positive photoresist.

9.7.5.1 Recipe Steps

1. Clean the substrate.
2. Mount the substrate onto a spin coater and verify that the spin coater is set up with the appropriate parameters.
3. Dispense enough S1813 photoresist to cover the center half of the substrate and then spin coat for 30 s at 2500 rpm using a ramp rate of 500 rpm.

4. Softbake the photoresist coated substrate by placing it on a hot plate at 110°C for 60 s.
5. Mount the photoresist coated substrate and the desired photo mask into an optical projection system (i.e., a contact aligner or a stepper) and expose. The exposure time varies from system to system and will most likely need to be determined by trial and error. Ask a fellow cleanroom worker or technical support staff member for a good starting point.
6. Perform a postexposure bake by placing the substrate onto a 110°C hot plate for 60 s.
7. Develop the photoresist layer by submersing in CD-30 photoresist developer for 45 s. Gently agitate while in the solution. Remove the substrate and rinse for 30 s in DI water. Remove the substrate from the DI water and dry with a N_2 gun.

9.7.6 Case Study 6: Positive Photoresist Processing: Specific Processing for OiR 906-10

This case study is adapted from the Ph.D. thesis titled "Monolithic Suspended Optical Waveguides for InP MOEMS" by Kelly, Master's Thesis, University of Maryland, College Park, MD, June 2005. The processing steps are designed specifically for OiR 906-10 positive photoresist. In order to achieve optimum sidewall roughness and angle and the best possible feature resolution, projection lithography was used to pattern suspended waveguides. A 5x reduction Alphastep 1000 stepper lithography system was used to achieve critical dimensions down to 0.5 μm. A 5 in. chrome on quartz mask with a 5 cm × 5 cm mask area and a 0.1 μm spot size was used. This 25 cm^2 mask area was stepped down to a 100 mm^2 area on the chip.

9.7.6.1 Recipe Steps

1. Clean the substrate.
2. Mount the substrate onto a spin coater and verify that the spin coater is set up with the appropriate parameters.
3. Apply an HMDS treatment to the substrate surface. Using a disposable pipette, syringe, or eye-dropper, apply HMDS solution to the entire substrate surface. Allow to sit for 10 s and then spin dry for 60 s at 3000 rpm on a spin coater.
4. Dispense enough Arch OiR906-10 photoresist to cover the center half of the substrate and then spin coat for 60 s at 3000 rpm. The target photoresist film thickness is 1 μm.
5. Softbake the photoresist coated substrate by placing it on a hot plate at 90°C for 60 s.
6. Mount the photoresist coated substrate and the desired photo mask into the stepper and exposure for the desired time. The stepper parameters and exposure time may best be determined by first exposing and developing a test wafer (see process notes below).

7. Perform a postexposure bake by placing the substrate onto a 110°C hot plate for 60 s.
8. Develop the photoresist layer by submersing in ODP 4262 photoresist developer for 60 s. Gently agitate while in the solution. Remove the substrate and rinse for 30 s in DI water. Remove the substrate from the DI water and dry with a N_2 gun.

9.7.6.2 Notes

Several alignment procedures associated with the Alphastep stepper may need to be carefully addressed: autoleveling of wafer pieces cannot be implemented on this stepper and the lamp intensity can fluctuate over periods of only a couple of hours. In order to level the wafer pieces, we employed a technique of shimming the chuck using various pieces of aluminum foil and Post-It notes. A program was run to measure the wafer height across the chip using the stepper's laser measurement system, then the chuck was shimmed to try to level the surface. The focal depth of the stepper optics was 2 μm, so this process was repeated until the die-to-die variation in height was less than 1 μm. In our case, a single 10 × 10-mm die per chip was used so the entire chip area had to be leveled to ±1 μm to achieve optimum resolution.

In order to provide the correct exposure time and focus depth, a focus exposure matrix was used prior to exposing each chip. A mask with a test pattern of bars and spaces varying from 2.0 μm down to 0.5 μm in width was used for this matrix. An exposure dose between 100 and 120 mJ/cm^2 with a focus depth between −1 and 1 provided the best feature resolutions and resist profiles. The optimum exposure time and stepper parameters were determined from an optical inspection of the developed test wafer(s) using a high-quality optical microscope.

9.7.7 Case Study 7: Negative Photoresist Processing: Specific Processing for NR7-1500PY

This case study describes specific processing conditions for the Futurrex NR7-1500PY negative photoresist. An MJB3 manual contact aligner is used for UV exposure.

9.7.7.1 Recipe Steps

1. Perform solvent clean on a Si wafer.
2. Mount wafer on spin coater and set up spin coater with a ramp rate of 1000 rpm and spin speed of 4000 rpm and a time of 60 s.
3. Dispense photoresist onto the surface of the wafer. Dispense enough resist to cover at least half the surface area of the wafer. Turn on the spin coater.
4. Remove the photoresist coated substrate from the spin coated and place on a preheated hotplate at 90°C for 1 min.

5. Mount the substrate and desired photomask onto the MJB3 contact aligned. With the microscopy, image a feature on the mask. Then, using the z-translation bar and fine adjustment knob, raise the wafer up such that the top surface of the photoresist is just below the bottom surface of the mask when the z-translation bar is in the "contact" position (be sure that the slide bar is in the contact position and not in the "soft contact" position). This is the position just before the shadow image of the mask feature disappears. Using the z-translation fine-adjustment knob, raise the wafer into contact with the mask. This is the point where the shadow image of the mask feature disappears. Now move the slide bar into the soft contact position. At this point the mask and photoresist surfaces will be in focus but not in contact. Adjust the X, Y, and Rotation of the wafer to be in alignment with the mask. Once proper alignment has been established, move the slide bar into contact mode. Set the exposure time to 16 s and push the expose button.
6. Remove the wafer from the contact aligner and place onto a preheated hotplate at 90°C for 1 min.
7. Submerge the wafer into a bath of RD6 photoresist developer for 15 s. Gently agitate either the solvent or the wafer during developing. Remove the wafer and submerge into a bath of DI water for 30 s and apply agitation. Remove the wafer from the DI water bath and rinse in DI water (i.e., spray down with a squirt bottle filled with DI water). Then dry with N_2 gas (i.e., use a N_2 gas stay gun equipped with a point-of-use filter connected to a clean dry source of N_2 gas).
8. Perform etch or deposition processing as required.
9. Prepare a bath of RR2 photoresist solvent that is large enough so that the wafer can be vertically submerged (not laying flat but rather standing on edge). Also prepare separate acetone and IPA baths in which the wafer can lay flat. Place the RR2 bath on a hotplate and heat the solution to 85°C. Be very careful not to let the solution temperature rise above 100°C as RR2 is flammable! Place the wafer vertically into the warm RR2 bath and gently agitate. Once liftoff is complete, transfer the wafer to the acetone bath. Agitate gently and then transfer the wafer to the IPA bath (as the wafer is transferred from one bath to the next, be sure that the wafer surface stays wet and that no part is allowed to dry before entering the next bath – never let the wafer surface dry – always keep the wafer surface wet). Remove the wafer from the IPA bath and rinse it down with IPA from a squirt bottle. Then dry with N_2 gas.

9.7.7.2 Note 1

For liftoff involving Au films less than 100 nm thick, the metal film tends to lift off in small pieces and look like a fine mesh as it lifts off. Au pieces that are tens of microns in size tend to backstick to the patterned Au features and cannot be subsequently removed. This backsticking can largely be prevented by processing ¼-wafer pieces in a 500 ml bath of RR2 that is stirred at 300 rpm with a 1 in. long stir bar. The wafer piece is held with flat nose metal tweezers at a position such that

the top surface of the wafer is pointed slightly down from the vertical and so that the backside is slightly turned into the solvent flow. This sample position allows the Au film and pieces to be swept away from the wafer surface during liftoff.

9.7.7.3 Note 2

Thicker Au films can take several to ten or so minutes to completely lift off. We have found that the liftoff time can be dramatically reduced by performing an O_2 plasma exposure after deposition but before liftoff. For example, 5 min in a PlasmaTherm 790 at 200 W, 19 SCCM O_2, and 100 mtorr reduces the liftoff time from about 10 min to about 1 min for a 100 nm thick Au film. RR2 is an aggressive solvent and can attack the Si surface; therefore, there can be an advantage to shorter liftoff times. Albeit with limited investigation, the plasma exposure does not appear to adversely affect the Au or Si surfaces, such a process may not be compatible with other materials or with previous processing steps that may have been performed on the wafer.

9.7.8 Case Study 8: E-Beam Lithography

E-beam lithography can be performed with any number of different SEM systems, therefore only a generic account of SEM functions is presented as part of this case study.

1. Start with a 1 cm^2 Si substrate that has been cleaned (see cleaning procedures for UV lithography).
2. Spin coat a layer of MMA at 4000 rpm for 60 s and bake for 5 min at 200°C.
3. Spin coat a layer of PMMA 950 K A7 at 4000 rpm for 60 s and bake for 5 min at 180°C.
4. With a diamond scribe, scratch a line into the PMMA. Go deep enough to produce a small number of Si shards near the end of the scratch. An example is shown in Fig. 9.48.
5. Mount the substrate on the SEM sample holder. It is usually a good idea to place the sample in a specific orientation so that it is easier to locate and align the

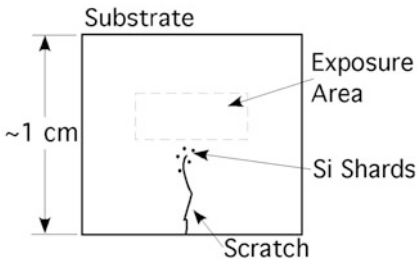

Fig. 9.48 Illustration of substrate for e-beam lithography

sample with respect to the microscope. For focus and alignment, it is desirable for the sample holder also to contain a calibration standard sample such as gold nanoparticles and a Faraday cup. The Faraday cup is a hole in the sample holder into which the electron beam can be directed for measuring the beam current.

6. Vent the antechamber, load the sample holder into the SEM, and pump a vacuum on the antechamber. Once the desired vacuum level has been established, move the sample holder into place in the microscope column.
7. Move the sample holder to position away from the sample and near the Faraday cup. Some SEMs allow different sample holders to be specified and specific spots on a given sample holder to be defined. In such a case, move to the predefined position of the Faraday cup.
8. Starting with the magnification at maximum, establish the electron beam in the SEM column, for example, open the gate valve and turn on the detector. Slowly decrease the magnification (and adjust the focus if needed) to image the Faraday cup. Center the electron beam in the Faraday cup and adjust the beam current to the desired value.
9. Move the sample holder to the calibration standard sample and focus the SEM. How well focused the SEM is at this point will have a large impact on the resolution and quality of the lithography; so, take your time and do a good job here.
10. Locate the edge of the sample containing the scratch and move along the scratch unit until you reach the end. Doing this at too low a magnification can cause unwanted exposure to the resist layer. Doing this at too high a magnification can take "forever."
11. Once at the end of the scratch, refocus on a Si shard. Do this first by adjusting the height of the sample (z adjustment) and then fine-tune by adjusting the focus itself. It is best to not have to adjust the stigmators during this final focus.
12. Switch over to NPGS control of the SEM and turn on the beam blanker. Set the SEM to the desired magnification. This is typically 1000x. Move the sample to the desired location or exposure.
13. Select the desired run file and verify that it contains the desired settings. Run the run file (click on the "process run file" button). After the exposure is finished, move to another exposure location and repeat the exposure using the desired run file.
14. Once all the desired patterns have been exposed, set the SEM to the maximum magnification, turn off the electron beam, turn off the beam blanker, and switch back to SEM mode.
15. Move the sample holder to the "home" position and remove it from the SEM column. Vent the antechamber and remove the sample holder. Remember to close the antechamber and leave it under vacuum.
16. Develop the sample in a 1:3 solution of MIBK:IPA for 90 s. Rinse in DI water for 30 s. The developing time may be sample-dependent so several test samples might be needed. Samples should now be ready for further processing.

9.7.8.1 Notes on Using the NPGS Software

The NPGS and DesignCAD software can be loaded onto an office PC so that files can be prepared offline from the SEM. Make sure that within the DesignCAD application that the features are drawn using "PolyFill" under the NPGS menu bar selection. Select a feature and use the info box to assign it to a specific layer. Choose a different color for each layer. Within a run file, all the beam control parameters can be independently assigned for each separate layer. The desired beam control parameters in a given run file are dependent on the specific SEM and feature that will be written. Several test exposures will most likely be needed. A good place to start can be determined by looking at other run files on the NPGS computer connected to the SEM or by talking with other e-beam users.

9.7.9 Case Study 9: Fabrication of PDMS Templates

PDMS is a two-part elastomer and is typically formulated as 10 parts base to 1 part curing agent. The resulting material is transparent in the UV and visible regions, flexible, and has a low Young's modulus. The surface is tacky and has a low surface energy. The Young's modulus can be somewhat controlled by the ratio of base to curing agent and curing temperature, however, other formulations have been developed for higher Young's modulus [15]. The typical formulation is referred to as soft-PDMS (s-PDMS) with a Young's modulus less than 2 MPa. Formulations designed for higher Young's modulus (9 MPa) are referred to as hard-PDMS (h-PMDS). For reference, Si has a Young's modulus of 130 GPa. Molds made for materials such as PDMS are referred to as soft mold and are used in soft lithography applications. Molds made from materials such as Si are referred to as hard molds and are used in imprint lithography applications. Molds made from materials with a Young's modulus between that of PDMS and Si are referred to as rigiflex molds [15]. A review of mold materials can be found in [15].

1. By weight, mix 10 parts PDMS base with 1 part PDMS curing agent. Use a container that is clean of particulates and other possible contaminants. Make sure that the container is large enough to contain all the PDMS as it is degassed in a vacuum chamber and that the container is small enough to fit into the vacuum chamber.
2. After thorough mixing, place the PDMS into a vacuum chamber and pump a vacuum into it until no gas bubbles are visible in the PDMS. Depending on the vacuum level and amount of PDMS, this could take around 20 min. To avoid contamination of the PDMS it is recommended to use an oil-free pump such as a scroll pump or diaphragm pump.
3. Once degassed, the PDMS can be applied either by pouring on or by spin coating onto a substrate. PDMS has a viscosity of 362 cP (about the same consistency as honey). The viscosity can be decreased by mixing with a solvent. For example

a dilution of 69% by weight with toluene will lower the viscosity to 50 cP [15]. The speed at which the PDMS flows will depend on the viscosity of the material.

4. After pouring, let the PDMS sit at room temperature long enough to completely flow over the entire area and reach equilibrium. This could take some time depending on how much PDMS is used and the size of the area to be covered. Tilting the substrate around to different angles will allow gravity to assist in getting the PDMS to cover all areas of the substrate. It is best to hold the substrate from the backside with vacuum tweezers so that the PDMS does not flow off the edge of the substrate due to wetting the tip of the mechanical tweezers.
5. For spin coating, the thickness of the film can be controlled by adding toluene to lower the viscosity of the PDMS prior to spin coating. After spinning, let the PDMS film stand at room temperature (no baking on a hotplate) until all the solvent has had a chance to evaporate and the remaining PDMS has reached a uniform thickness over the entire substrate area.
6. The PDMS can be cured by letting it sit at room temperature for 24 h. Faster curing is possible such as at 70°C for 2 h.
7. Once cured the PDMS can be left in place or peeled off as a free-standing film.
8. For microfluidics, the PDMS would be cast onto a mold containing the negative topology of the desired flow channels. Once removed from the mold, the PDMS can be placed onto the desired substrate to create the flow channels. Where it touches the substrate, the PDMS film will wet a substrate surface to form a conformal contact. With no prior surface treatment, adhesion between the PDMS and substrate is generally nonpermanent and the PDMS film can be easily removed and repositioned.
9. The adhesion between PDMS and a Si substrate (or a second PDMS film) can be made permanent in the following ways.

    a. Place a clean Si substrate (free of particulates or contamination on the surface) into a UVO cleaner with the substrate surface about 2 mm below the light source and expose for 15 min.
    b. Remove the Si substrate and similarly place the PDMS film in the UVO cleaner and expose for 150 s.
    c. Remove the PDMS film and contact it to the Si substrate. While in contact, place the assembly into a 70°C oven and heat for at least 20 min. Once removed from the oven, the PDMS will be permanently bonded to the Si Substrate. Note that the position of the materials in the UVO cleaner, duration of exposure, and amount of "aging" after exposure(s) are all critical parameters affecting the interfacial adhesion strength between the PDMS film and Si substrate (Childs also contains useful information about PDMS processing).

9.7.10 Case Study 10: Photomask Fabrication [226, 227]

Photomasks are typically designed using a CAD (computer-aided design or computer-aided drafting) software application. GDS (graphic data system) is the

standard file format accepted by mask manufacturers and mask fabrication tools. Alternatively the DXF (drawing exchange format) file format commonly associated with the popular AutoCAD drawing application is widely accepted but can contain problematic conversion errors. Within the CAD software application, the desired photomask pattern is best laid out using square or rectangle shapes having 90° corners. This "Manhattan geometry" avoids circles and slanted lines that can add complexity and cost to mask fabrication. Features are best laid out on a grid with 0.125 μm or 0.1 μm grid size. Smaller grid sizes such as 0.05 μm or 0.025 μm are possible but can dramatically increase fabrication complexity and cost.

Features should be drawn so that they snap to grid lines rather than fall in between grid lines. Examples of good and bad features are shown in Fig. 9.49. Figure 9.49a illustrates a good feature. Figure 9.49b–d illustrate rounded corners, features not aligned to the grid, and features aligned to the grid but incorporating non-90° angles, respectively. Features should also be aligned so that they are easily cleaved or separated after final fabrication as illustrated at the bottom of Fig. 9.49.

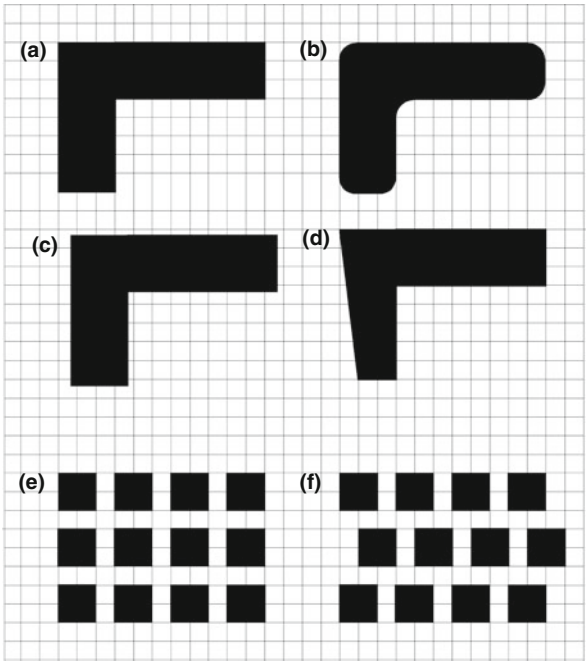

Fig. 9.49 Optimized (**a**) and (**e**) and unoptimized (**b**)–(**d**) and (**f**) grid layouts for photomask patterns (Modified from [26]; used with permission)

As in a mechanical drawing submitted to a machine shop, critical dimensions and tolerances of a mask design need to be considered. Typically, minimum feature sizes of 5–2.5 μm with tolerances of ±0.5 to ±0.25 μm are cost effective. Device fabrication commonly uses several levels of photolithography which require multiple masks. Each mask has to be aligned to the previously fabricated pattern; therefore, layer-to-layer registration must be accounted for during mask design. Overlay registrations of 0.5 mm to 0.25 μm over 4 in. are typically achievable.

Additional issues to keep in mind during mask design [26] include the following.

1. Alignment to crystal axis of substrate (wafer flat is ~2° off axis)
2. Avoid patterns within 2–5 mm of wafer edge.
3. Don't mix large and small features in the same mask level.
4. If performing a wet etch, account for lateral undercut of substrate in the mask design.
5. If performing DRIE etch, account for etch rate as a function of distance from substrate center. Etch rate is slower in the center and faster at the edges of the substrate.
6. Include alignment marks: one big enough to see with the naked eye and one the size of the smallest mask feature. Strategically place marks so that they are accessible to the stepper of contact aligner to be used.

9.7.10.1 Photomask Defects

Fabrication errors and damage due to handling can cause defects in pattern features on a photomask. Figure 9.50 shows several types of both opaque and clear defects. After it has been fabricated, careful inspection is usually required to verify the integrity of a photomask. A visual inspection under an optical microscope can pick out defects on the order of 3 μm and should always be performed prior to using a photomask. A visual inspection can identify defect, dirt, and dust. If dirt and dust are found the photomask should be carefully cleaned.

A more careful inspection for defects can be performed using a KLA die-to-die inspection system. This is an automated tool that optically compares two similar areas on a photomask. The machine pixelates optical images and compares

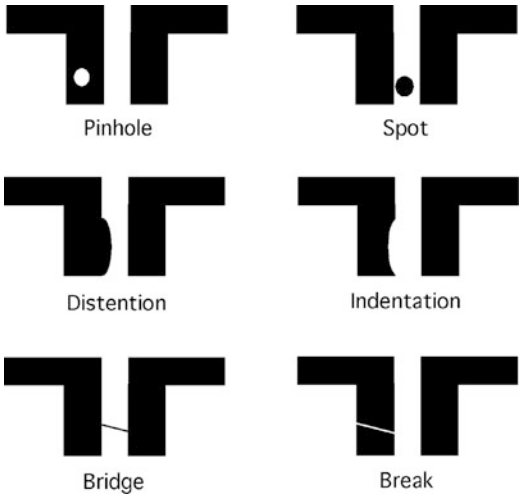

Fig. 9.50 Illustration of feature defect on a photomask (Modified from [226])

transmitted light intensities. Discrepancies are registered as possible defects and flagged for further human inspection and classification. A similar die-to-database, KLA Reticle Inspection System (KLARIS) inspection can be performed where the photomask is compared to a computer-generated database. Defects that can affect the performance of fabricated devices must be repaired or a new mask must be fabricated. Defects are typically repaired with a focused ion beam system that can either remove opaque defects of add material to clear defects [228]. These repair steps are similar to FIB and gas-assisted ion beam process methods discussed in Sections 9.5.2 and 9.5.3, respectively.

9.7.10.2 Grayscale Lithography Pixelated Photomasks

As discussed above, partial transmission of UV light during the exposure step pixelates mask patterns below the diffraction limit of the optical projection system. The pixelation is determined by two basic parameters: the pitch and the pixel size. As an example, for a standard 5x reduction stepper the resolution at the substrate level is generally about 0.6 μm which corresponds to a pixel size of 3 μm on the mask. The largest pixel size in a grayscale mask for this system must be smaller than this 3 μm resolvable dimension. A convenient choice for the maximum pixel size is thus 2.0 μm with a maximum spacing between pixels of 2.6 μm. The minimum pixel size is set by the resolution of the mask fabrication tool which is typically limited to a spot size of 0.6 μm and a minimum beam step of 0.1 μm. The available grayscale levels would therefore correspond to 15 pixel sizes from 0.6 up to 2.0 μm with a pixel size step of 0.1 μm. This is just a basic example of how the particular pixelation would be performed, which will vary depending on the exact projection lithography system being used.

Practical guides that include discussions about manufacturing photomasks can be found at the following.

Cornell University:
http://www.cnf.cornell.edu/cnf5_courses.html
Stanford University:
http://snf.stanford.edu/Process/Masks/Masks.html
University of Alberta:
http://www.nanofab.ualberta.ca/site/?page_id=47
Brigham Young University:
http://www.ee.byu.edu/cleanroom/masks.phtml
University of California, Berkeley:
http://microlab.berkeley.edu/ (click on 'mask making')
Much more can be found by exploring links at
Harvard University:
http://people.seas.harvard.edu/~jones/lab_arch/nano_facilities/nano_facilities.html

9.7.10.3 Mask Manufacturers

Compugraphics
Advanced Reproductions
Image Technology
Infinite Graphics
Applied Image
Photronics
Delta Mask
Microtronics
ADTEK Photomask

9.7.11 Case Study 11: Multiphoton Absorption Polymerization (MAP)

Multiphoton absorption polymerization (MAP) exploits the inherent optical nonlinear property of multiphoton absorption to localize the fabrication in the region of high photon intensity, for example, a laser focal point. Such localization allows complex, arbitrary, three-dimensional fabrication, with feature sizes as small as 40 nm [229]. MAP can be performed with both negative and positive photoresists. The exposure laser source can be from near IR to visible light [230, 231]. In this case study, acrylic negative photoresist is discussed and an 800 nm fs laser is used as the exposure light source.

1. Start with a 25 mm^2 glass cover slip substrate that has been cleaned with an oxygen plasma cleaner for 2 min.
2. Coat the glass surface to promote final device adhesion by dipping it in the solution that has 93 vol% ethanol, 5 vol% DI water, and 2 vol% (3-acryloxypropyl)trimethoxysilane for 12 h under stirring at room temperature.
3. Rinse the cover slip with ethanol for 1 h and dry it in a 95°C oven for 1 h.
4. Prepare a resist by mixing 48.5 wt% of (6) trimethylolpropane triacrylate (Sartomer, SR-499), 48.5 wt% tris(2-hydroxy ethyl)isocyanurate triacrylate (Sartomer, SR-368) and 3 wt% 2,4,6- trimethylbenzoylethoxyphenylphosphine oxide (BASF, Lucirin TPO-L) on rotator for 12 h.
5. Put a drop of well-mixed resist on the acrylate-modified glass substrate, use Scotch tape to fix the substrate on a regular glass slide. The tape also works as a spacer; it is on the order of 100 μm thick but can be made several millimeters thick depending on the sample. Cover the resin with a cover slip having a thickness smaller than the focal distance of the microscope objective (usually use #1 cover slip). An example is shown in Fig. 9.51.
6. Align the laser beam into the microscope objective. Fix the sandwiched resin sample on the stage that is mounted on the microscope.
7. Finding the surface of the substrate is critical in MAP. Using the fine-tuning knob, move the objective up and down until the fabricated line can barely be

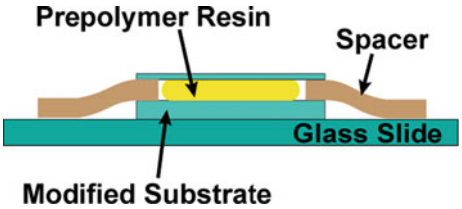

Fig. 9.51 Illustration of a sample in MAP [232] (Reprinted with permission from [232])

seen on a monitor connected to a CCD camera. Focusing an ultrafast laser into a prepolymer sample generates a cross-linked polymeric dot. The desired pattern can be achieved by a moving stage in 3-D with respect to the laser focal point. A homemade labview program transfers (x, y, z) coordination from a prepared text file to stage [233].

8. After determining the location of the surface, run the program to fabricate desired 3-D microstructures. The laser intensity needs to be adjusted to meet the requirement of the structure.
9. Upon finishing fabrication, carefully take off the substrate with the structure. Develop the resist by rinsing twice in dimethylformamide for 3 min each, followed by two rinses in ethanol for 3 min each.
10. Dry the sample by either allowing the solvent to evaporate on its own or by blowing with dry air. Supercritical CO_2 drying can be performed for ultrafragile structures.

9.7.12 Case Study 12: Lithography Using Focused Ion Beams

Focused Ion Beam (FIB) has not been widely used for lithography because it is so powerful a tool for direct micromachining and because it does not give huge advantages over e-beam lithography, which is already well established with its own huge body of knowledge, software, and tools. We are considering here high-resolution FIBs (0.005–0.1 micrometer beams) at energies in the range 10–50 keV with heavy ions such as Ga.

A FIB system can be used for lithography by, for example, adapting software designed to control an SEM for lithography. This software should be able to control beam position and exposure time (ion dosage) via the beam blanker. The major differences between electron beam lithography and ion beam lithography lie in the very different sensitivities of resists to ions compared with electrons, and the much smaller proximity effects because of the secondary ion spectrum of the ion beam at such low energy. In fact, proximity effects can be ignored.

The process flow for FIB lithography is very similar to that for e-beam lithography. The main differences relate to avoiding statistical effects due to the high sensitivity of the resists, which could tempt one to write too quickly, and the development of resists. FIB lithography techniques have been developed mostly by

Melngailis at M.I.T. [234, 235], who used PMMA and novolac-based (negative) resists (the latter with a unique silylation process), and by Matsui [236] at NEC Corporation who used PMMA and novolac. The process flows are all generally similar, including the method below.

We describe here a bilevel spin-on-glass (SOG) process developed by Milgram at Tektronix and Puretz [237] at the Oregon Graduate Institute to provide high-resolution negative resist. This resist would be used to provide a precise opening above a substrate through which implantation or metal deposition could be performed, for example. In the Milgram–Puretz approach a very thin layer of SOG is spun over a thick resist. The SOG is implanted with Ga ions which all stop in the SOG. This radically changes the SOG sensitivity in an O_2 reactive ion etch to make it equal to that of the underlying thick resist. When both layers are subjected to the O_2 etch the result is an opening where the ions were implanted, with very vertical sidewalls due to the anisotropic nature of the etch.

1. One begins typically with a Si substrate cleaned as it would be for any lithography process. The substrate is then attached to a SEM stub. It is recommended that a magnification calibration sample be attached adjacent to the substrate, so that the FIB magnification can be precisely known.
2. Two micrometer thick layer of Hunt 206 photoresist (HPR206) is prepared by spinning on the liquid in the usual manner. This is followed by a 30 min bake at 220°C, in air.
3. A siloxane SOG is applied typically using a pipette, and then spun to produce a thin (~125 nm) layer. The glass is then cured at 200°C in air.
4. The sample can have a fiducial mark placed on it using an optical microscope, to assist in finding exposed areas. It is then placed in the FIB vacuum chamber and the system pumped out to normal operating pressure.
5. The beam can be aligned and focused by using the fiducial mark, starting at low magnification, and proceeding to the magnification that will ultimately be used for the resist exposure. Ideally, a Faraday cup would be used to measure the beam current precisely. Alternatively, if the stage can be biased at ~ +10 V (to suppress secondary electron emission), beam current can be read directly from the stage. Magnification calibration should be performed at the magnification setting to be used, prior to resist exposure. In this way ion dosages can be well known.
6. Implants of 10^{14}–10^{16} Ga ions/cm^2 at a beam energy of 15 keV is sufficient to expose the desired pattern in the SOG. The FIB needs to be under the control of the lithography software for this step.
7. After exposure, turn off the ion beam and vent the specimen chamber so the sample can be removed.
8. The SOG is then etched in an O_2 reactive ion etch (RIE); a selectivity on the order of 1:100 has been found for unimplanted versus implanted SOG.
9. The RIE etching of HPR206 shows a selectivity of 100:1 over the unexposed SOG. The result is an etched layer of material with a highly vertical sidewall (no trapezoidal shapes) through which implantation into the silicon can be done (see Fig. 9.52).

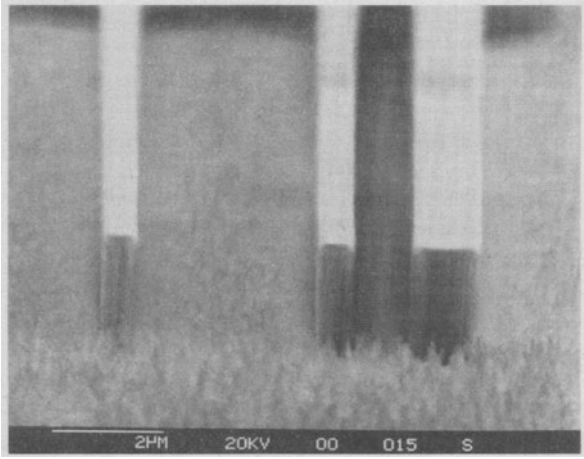

Fig. 9.52 Example of plasma processed SOG-HPR206 bilayer lines created with FIB lithography (Reprinted with permission from [237])

References

1. G.E. Moore: Cramming more components onto integrated circuits, Electronics 38, 11–117 (1965)
2. W. Brunsvold, W. Conley, W. Montgomery, et al: Acid-sensitive phenol-formaldehyde polymeric resists, Polymers for microelectronics – Resists and dielectrics, ACS Symposium Series 537, 333–347 (1994)
3. Deforest: Photoresist: Materials and Processes (McGraw-Hill, New York, NY, 1975)
4. G.A. Delzenne: In Encyclopedia of Polymer Science and Technology, Plastics, Resins, Rubbers, Fibers (Interscience, New York, NY, 1976)
5. P.P. Hanson: Unconventional photographic systems – A bibliography of Reviews, Photogr. Sci. Eng. 14, 438 (1970)
6. J. Kosar: Light Sensitive Systems (Wiley, New York, NY, 1965)
7. W.M. Moreau: Semiconductor Lithography Principles, Practices, and Materials (Plenum, New York, NY, 1987)
8. D.H. Ziger, C.A. Mack: Generalized-approach toward modeling resist performance, AIChE J. 37, 1863–1874 (1991)
9. G.K. Ananthasuresh, L.L. Howell: Mechanical design of complicated microsystems – A perspective & prospects, J. Mech. Des. 127, 736 (2005)
10. S. Kota, G.K. Ananthasuresh, S.B. Crary, et al.: Design & fabrication of microelectromechanical systems, J. Mech. Des. 116, 1081 (1994)
11. Z. Cui: Micro- Nanofabrication Technologies & Applications (Springer, New York, NY, 2005)
12. Z. Cui: Nanofabrication: Principles, Capabilities & Limits, (Springer, New York, NY, 2008)
13. F. Hua, Y. Sun, A. Gaur, M.A. Meitl, L. Bilhaut, L. Rotkina, J. Wang, P. Geil, M. Shim, J.A. Rogers, A. Shim: Polymer imprint lithography with molecular-scale resolution, Nano Lett. 4, 2467–2471 (2004)
14. S.R. Quake, A. Scherer: From micro to nanofabrication with soft materials, Science 290, 1536 (2000)
15. J.A. Rogers, H.H. Lee: Unconventional Nanopatterning Techniques & Applications (Wiley, New York, NY, 2009)
16. V.N. Truskett, M.P.C. Watts: Trends in imprint lithography for biological applications, Trends Biotechnol. 24, 312 (2006)

17. G.M. Whitesides, E. Ostuni, S. Takayama, X.Y. Jiang, D.E. Ingber: Soft lithography in biology & biochemistry, Annu. Rev. Biomed. Eng. 3, 335 (2001)
18. G.M. Whitesides, Y. Xia: Soft lithography, Annu. Rev. Mater. Sci. 28, 153–184 (1998)
19. J.L. Wilbur, A. Kumar, E. Kim, G.M. Whitesides: Microfabrication by microcontact printing of self assembled monolayers, Adv. Mater. 6, 600–604 (1994)
20. Y. Xia, G.M. Whitesides: Soft lithography review, Angew. Chem. Int. Ed. 37, 550–575 (1998)
21. X.-M. Zhao, Y. Xia, G.M. Whitesides: Soft lithographic methods for nano-fabrication, J. Mater. Chem. 7, 1069–1074 (1997)
22. P. Calvert: Inkjet printing for materials and devices, Chem. Mater. 13, 3299–3305 (2001)
23. E. Sachs, M. Cima, P. Williams, D. Brancazio, J. Cornie: 3-Dimensional printing – Rapid tooling & prototypes directly from a CAD mode, J. Eng. Ind. – Trans. ASME 114, 481 (1992)
24. C. Wu: Ink jets not just for the printed page, Sci. News 151, 205 (1997)
25. Photomask Basics. Available: http://www.photonics.com/about/basics.jsp. Photonics Media, Laurin Publishing (1996–2010)
26. Contact Mask Design Principles. Available: www.amfitzgerald.com, A.M. Fitzgerald & Associates, LLC. (2008–2010)
27. M.J. Madou: Fundamentals of Microfabrication: The Science of Miniaturization, 2nd edn. (CRC Press, Boca Raton, FL, 2002)
28. C.-M. Shiah, Y.-Y. Hsu, Y.-C. Tung, H.-Y. Liao, K.-T. Tsai, J.-B. Wang: Alternating phase shift mask, US Patent No. 6,977,127, 12/20/05 (2005)
29. Z. Krivokapic, C.A. Spence: Attenuated phase shift mask, US Patent No. 5,928,813, 07/27/1999 (1999)
30. SU-8: Thick Photo-Resist for MEMS. Available: http://memscyclopedia.org/su8.html
31. Microlithography. Available: http://www.cnf.cornell.edu/cnf5_courses.html. Cornell Nano Scale Science and Technology Facility (2009)
32. M.S. Hibbs: System Overview of Optical Steers and Scanners, Chapter 1, In J.R. Sheats, B.W. Smith (Eds.): Microlithography Science and Technology (Marcel Dekker, New York, NY, 1998)
33. E.J. Walker: Reduction of photoresist standing-wave effects by post-exposure bake, IEEE Trans. Electron. Dev. 22, 464–466 (1975)
34. J.M. Shaw; M. Hatzakis: Performance characteristics of diazo-type photoresists under e-beam and optical exposure, IEEE Trans. Electron. Dev. 25, 425–430 (1978)
35. M.S. Hibbs: System Overview of Optical Steers and Scanners (Marcel Dekker, New York, NY, 1998)
36. B.W. Smith: Resist Processing (Marcel Dekker, New York, NY, 1998)
37. J.J. Sagura, J.V.A. Allan: Azide sensitized resin photographic resist, US Patent No. 2,940,853, June 14 (1960)
38. J.M. Shaw, J.D. Gelorme, N.C. LaBianca, W.E. Conley, S.J. Holmes: Negative photoresists for optical lithography, IBM J. Res. Dev. 41, 81–94 (1997)
39. J.V. Crivello, J.H.W. Lam: Photoinitiated cationic polymerization by dialkyl phenyl sulfonium salts, J. Polym. Sci. Polym. Chem. Ed. 17, 2877 (1979)
40. J.V. Crivello: Possibilities for photoimaging using onium salts, Proceedings of the SPIE Regional Technical Conference on Photopolymers, Society of Polymer Engineers, 267 (1982)
41. E. Alling, C. Stauffer: Image reversal of positive photoresist, SPIE Proceedings, 539 Advances in Resist Technology & Processing (1985)
42. M.L. Long, J. Newman: Image reversal techniques with standard positive photoresist, Proceedings of the Society of Photo-optical Instruments Engineers 469, 189–193, (1984)
43. W.G. Oldham, E. Hieke: IEEE Electron Device Lett. 1, 217–219, (1980)
44. R.B. Darling: Photolithography Tutorial, University of Washington, Center for Applied Microtechnology

45. I.S. Daraktchiev: Process for coating a photoresist composition onto a substrate, US Patent No. 4,996,080, 2/26/1991 (1991)
46. N.P. Pham, T.L. Scholtes, R. Klerk, B. Wieder, P.M. Sarro, J.N. Burghartz: Direct Spray Coating of Photoresist for MEMS Applications, Presented at Micromachining and Microfabrication Process Technology VII, San Francisco, CA, USA (2001)
47. L. Yu, Y. Yeow Lee, F.E.H. Tay, C. Iliescu: Spray coating of photoresist for 3D microstructures with different geometries, J. Phys. Conf. Ser. 34, 937–942 (2006)
48. E. DiFabrizio, F. Romanato, M. Gentili, S. Cabrini, B. Kaulich, J. Susini, R. Barret: High-efficiency multilevel zone plates for keV X-rays, Nature, 401, 895–898 (1999)
49. P. Ehbets, H.P. Herzig, D. Prongue, M.T. Gale: High-efficiency continuous surface-relief gratings for two-dimensional array generation, Opt. Lett., 17, 908–910 (1992)
50. B. Morgan, C. Waits, J. Krizmanic, R. Ghodssi: Development of a deep silicon phase fesnel lens using gray-scale technology and deep reactive ion etching, J. Microelectromech. Sys. (JMEMS) 13, 113–120 (2004)
51. P. Yao, G.J. Schneider, D. Prather: Three-dimensional lithography fabrication for microchannels, J. Microelectromech. Sys. (JMEMS) 14, 799–805 (2005)
52. P. Yao, G.J. Schneider, D. Prather, E. Wetzel, D. O'Brein: Fabrication of three-dimensional photonic crystals with multilayer photolithography, Opt. Express 13, 2370–2376 (2005)
53. V. Kudryashov, X.-C. Yuan, W.-C. Cheong, K. Radhakrishnan: Grey scale structures formation in SU-8 with e-beam and UV, Microelectron. Eng. 67–68, 306–311 (2003)
54. Y.-T. Lu, C.-S. Chu, H.-Y. Lin: Characterization of the gray-scale photography with high-resolution gray steps for the precise fabrication of diffractive optics, Opt. Eng. 43, 2666–2670 (2004)
55. B. Morgan, R. Ghodssi: Vertically-shaped tunable MEMS resonators, J. Microelectromech. Sys. (JMEMS) 17, 85–92 (2008)
56. B. Morgan, X. Hua, T. Iguchi, T. Tomioka, G. Oehlein, R. Ghodssi: Substrate interconnect technologies for 3-D MEMS packaging, Microelectron. Eng. 81, 106–116 (2005)
57. B. Morgan, J. McGee, R. Ghodssi: Automated 2-axis optical fiber alignment using gray-scale technology, J. Microelectromech. Sys. (JMEMS) 16, 102–110 (2007)
58. B. Morgan, C.M. Waits, R. Ghodssi: Compensated Aspect Ratio Dependent Etching (CARDE) using gray-scale technology, Microelectron. Eng. 77, 85–94 (2005)
59. B.C. Morgan: Electrostatic MEMS Actuators Using Gray-Scale Technology, Ph.D. thesis, University of Maryland, College Park, MD (2006)
60. Y. Olinger, P. Sixt, J.M. Stauffer, J.M. Mayor, P. Regnault, G. Voirin: One-step 3D shaping using a gray-tone mask for optical and microelectronic applications, Microelectron. Eng. 23, 449–454 (1994)
61. C.M. Waits, A. Modafe, R. Ghodssi: Investigation of gray-scale technology for large area 3-D silicon MEMS stuctures, J. Micromech. Microeng. 13, 170–177 (2003)
62. M. Woytasik, J.-P. Grandchamp, E. Dufour-Gergam, J.-P. Gilles, S. Megherbi, E. Martincic, H. Maathias, P. Crozat: Two- and three-dimensional microcoil fabrication process for three-axis magnetic sensors on flexible substrates, Sens. Actuators A Phys. 132, 2–7 (2006)
63. L. Mosher: Double-Exposure Gray-Scale Photolithography, Master's Thesis, University of Maryland, College Park, MD (2008)
64. C.-C. Chen, C.-H. Hou, J.-K. Sheu, J.-Y. Chang, M.-H. Li, G.-C. Chi, C. Wu: Gratings in GaN membranes, Jpn. J. Appl. Phys. 43, 5854–5856 (2004)
65. C.-C.L. Chen, Chien-Chieh, J.Y. Cheng, Y.L. Huang, C.-Y. Chang, M.-H. Li, Y.-S. Huang, L.-Y. Chien, J.-Y. Chang, G.-C. Chi, W.-T. Cheng, J.-H. Yeh, C. Wu: Microlens and micromirror for optical MEMS fabricated by e-beam photolithography and ICP etching, International Conference of Optics in Computing (OC2002), Taipei, Taiwan, 322 (2002)
66. V.P. Korolkov, A.I. Malyshev, A.G. Poleshchuck, V.V. Cherksshin, H.J. Tiziani, C. Pruss, T. Schoder, J. Westhauser, C. Wu: Fabrication of gray-scale masks and diffractive optical elements with LDW glass, Proceedings of SPIE – Lithographic and Micromachining Techniques for Optical Component Fabrication, 4440, 73–84 (2001)

67. L. Mosher, C.M. Waits, B. Morgan, R. Ghodssi: Double-exposure grayscale photolithography, J. Microelectromech. Syst. 18, 308–315 (2009)
68. E. Lee, J. Won Hahn: J. Appl. Phys. 103, 083550 (2008)
69. J. Krizmanic, B. Morgan, R. Streitmatter, N. Gehrels, K. Gendreau, Z. Arzoumanian, R. Ghodssi, G. Skinner: Development of ground-testable phase frenel lenses in silicon, Exp. Astron. 20, 299–306 (2005)
70. Y. Chen, R.K. Kupka, F. Rousseaux, F. Carcenac, D. Decanini, M.F. Ravet, H. Launois: 50-nm x-ray lithography using synchrotron radiation, J. Vac. Sci. Technol. B 12, 3959–3964 (1994)
71. Z. Cui: Micro-Nanofabrication: Technologies and Applications (Higher Education Press, Beijing, 2005)
72. E.W. Becker, W. Ehrfeld, P. Hagmann, A. Maner, D. Münchmeyer: Microelectron. Eng. 4, 35–56 (1986)
73. W. Ehrfeld, P. Bley, F. Götz, P. Hagmann, D. Münchmeyer, J. Mohr, O.H. Moser, D. Münchmeyer, W. Schelb, D. Schmidt, E.W. Becker: Fabrication of microstructures using the LIGA process, Presented at Micro Robots and Teleoperators Workshop, IEEE (1987)
74. H. Guckel: High-aspect-ratio micromachining via deep X-ray lithography, Proc. IEEE, 86, 1586 (1998)
75. H. Guckel, T.R. Christenson, K.J. Skrobis, T.S. Jung, J. Klein, K.V. Hartojo, I. Widjaja: A first functional current excited planar rotational magnetic micromotor, Presented at Micro Electro Mechanical Systems, 1993, MEMS ′93, Proceedings an Investigation of Micro Structures, Sensors, Actuators, Machines and Systems (IEEE 1993)
76. V. Saile, U. Wallrabe, O. Tabata, G.K. Fedder: LIGA and Its Applications, Volume 7 of Advanced Micro and Nanosystems (Wiley-VCH, Weinheim, Germany, 2008)
77. K. Guckel, K.J. Skrobis, T.R. Christenson, J. Klein, S. Han, B. Choi, E.G. Lovell: Fabrication of assembled micromechanical components via deep X-ray lithography, Presented at Micro Electro Mechanical Systems, 1991, MEMS ′91, Proceedings an Investigation of Micro Structures, Sensors, Actuators, Machines and Robots (IEEE, 1991)
78. A.R. Shimkunas, P.E. Mauger, L.P. Bourget, R.S. Post, L. Smith, R.F. Davis, G.M. Wells, F. Cerrina, R.B. McIntosh: Advanced electron cyclotron resonance chemical vapor deposition SiC coatings and x-ray mask membranes, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 9, 3258 (1991)
79. G.M. Wells, S. Palmer, F. Cerrina, A. Purdes, B. Gnade: Radiation stability of SiC and diamond membranes as potential x-ray lithography mask carriers, J. Vac. Sci. Technol. B 8/6, 1575–1578 (1990)
80. J. Goettert: From Design to LiGA Polymer Chips: A Customer Experience, Presentation (Louisiana State University, 2005)
81. M. Gad-el-Hak: MEMS: Design and Fabrication, 2 edn. (CRC Press, Boca Raton, FL, 2006)
82. Y. Liu, P. Sheng: Modeling of X-ray fabrication of macromechanical structures, J. Manufact. Proces 4, 109 (2002)
83. H. Guckel, K.J. Skrobis, J. Klein, T.R. Christenson: Micromechanics via x-ray assisted processing, J. Vac. Sci. Technol. 12/4, 2559–2564 (1994)
84. R.K. Kupka, F. Bouamrane, C. Cremers, S. Megtert: Microfabrication: LIGA-X and applications, Appl. Surf. Sci. 164, 97 (2000)
85. H. Guckel: Deep x-ray lithography for micromechanics and precision engineering, Rev. Sci. Instrum. 67, 3357 (1996)
86. Y. Vladimirsky, J. Maldonado, R. Fair, R. Acosta, O. Vladimirsky, R. Viswanathan, H. Voelker, F. Cerrina, G.M. Wells, M. Hansen, R. Nachman: Thermal effects in x-ray masks during synchrotron storage ring irradiation, J. Vac. Sci. Technol. B 7/6, 1657–1661 (1989)
87. A. Flamholz, R. Ristein: X-ray steer exposure system performance and status, J. Vac. Sci. Technol. B 8/6, 2002–2007 (1990)

88. M. Reilly, Q. Leonard, G. Wells, C. Capasso, P. Anderson, J. Taylor, W. Waldo, K. Yamazaki, G. Chen, K. Simon, F. Cerrina: Performance of the modified Suss XRS 200/2 M X-ray steer at CXrL, Jpn. J. Appl. Phys. 33, 6899 (1994)
89. H. Guckel, T.R. Christenson, K.J. Skrobis, D.D. Denton, B. Choi, E.G. Lovell, J.W. Lee, S.S. Bajikar, T.W. Chapman: Deep X-ray and UV lithographies for micromechanics, Presented at Solid-State Sensor and Actuator Workshop, 1990. 4th Technical Digest, (IEEE 1990)
90. K. Yamazaki: Electron Beam Direct Write (World Scientific, Singapore, 2008)
91. K.L. Ekinci, X.M.H. Huang, M.L. Roukes: Ultraelectromechanical Mass Detection, Appl. Phys. Lett. 84, 4469 (2004)
92. Y.T. Yang, C. Callegari, X.L. Feng, K.L. Ekinci, M.L. Roukes: Zeptogram-scale nanomechanical mass sensing, Nano Lett. 6, 583 (2006)
93. K.L. Ekinci, J. Brugger: Nanofabrication of Nanoelectromechanical Systems (NEMS) (World Scientific, Singapore, 2008)
94. D.F. Kyser, N.S. Viswanathan: Monte Carlo simulation of spatially distributed beams in electron-beam lithography, J. Vac. Sci. Technol. 12, 1305–1308 (1975)
95. B.D. Cook, S.-Y. Lee: Fast proximity effect correction: An extension of PYRAMID for thicker resists, J. Vac. Sci. Technol. B 11, 2762 (1993)
96. J. Jacob, S. Lee, J. McMillan, N. MacDonald: Fast proximity effect correction: An extension of PYRAMIN for circuit patterns of arbitrary size, J. Vac. Sci. Technol. B 10, 3077–3082 (1992)
97. E. Kratschmer: Verification of a proximity effect correction program in electron beam lithography, J. Vac. Sci. Technol. 19, 1264–1268 (1981)
98. M.A. McCord, M.J. Rooks: Electron Beam Lithography, PM39: (SPIE Publications, Bellingham, WA, 1997)
99. I. Utke, P. Hoffmann, J. Melngailis: Gas-assisted focused electron beam and ion beam processing and fabrication, J. Vac. Sci. Technol. B 26, 1197–1276 (2008)
100. J.H. Orloff, M. Utlaut, L.W. Swanson: High Resolution Focused Ion Beams (Kluwer, New York, NY, 2003)
101. A.A. Tseng, S. Jou, A. Notargiacomo, T.P. Chen, Recent developments in tip-based nanofabrication and its roadmap, J. Nanosci. Nanotechnol. 8, 2167–2186, 2008
102. A.A. Tseng: Recent developments in micromilling using focused ion beam technology, J. Micromech. Microeng. 14, R15–R34, 2004
103. H. Yamaguchi, A. Shimase, S. Haraichi, T. Miyauchi: Characteristics of silicon removal by fine focused gallium ion beam, J. Vac. Sci. Technol. B 3, 71 (1985)
104. S. Dhara: Formation, dynamics, and characterization of nanostructures by ion beam irradiation, Crit. Rev. Solid State Mater. Sci. 32, 1–50 (2007)
105. L. Frey, C. Lehrer, H. Ryssel: Nanoscale effects in focused ion beam processing, Appl. Phys. A: Mater. Sci. Process. 76, 1017–1023 (2003)
106. L.A. Giannuzzi, F.A. Stevie: Introduction to Focused Ion Beams: Instrumentation, Theory, Techniques and Practice (Springer, New York, NY, 2005)
107. J. Gierak, E. Bourhis, M.N.M. Combes, et al.: Exploration of the ultimate patterning potential achievable with focused ion beams, Microelectron. Eng. 78–79, 266–278 (2005)
108. R.M. Langford, P.M. Nellen, J. Gierak, et al.: Focused ion beam micro- and nanoengineering, MRS Bull. 32, 417–423 (2007)
109. S. Matsui, R. Kometani: Three-dimensional nanostructure fabrication by focused-ion-beam chemical vapor deposition and its applications, IEICE Trans. Electron. E90C, 25–35 (2007)
110. J. Mayer, L.A. Giannuzzi, T. Kamino, et al.: TEM sample preparation and FIB-induced damage, MRS Bull. 32, 400–407 (2007)
111. J. Melngailis: Focused ion-beam technology and applications, J. Vac. Sci. Technol. B 5, 469–495 (1987)
112. W.J. MoberlyChan, D.P. Adams, M.J. Aziz, et al.: Fundamentals of focused ion beam nanostructural processing: Below, at, and above the surface, MRS Bull. 32, 424–432 (2007)

113. P.M. Nellen, V. Callegari, U. Sennhauser: Preparative methods for nanoanalysis of materials with focused ion beam instruments, Chimia 60, A735–A741(2006)
114. S. Reyntjens, R. Puers: A review of focused ion beam applications in microsystem technology, J. Micromech. Microeng. 11, 287–300 (2001)
115. A.A. Tseng: Recent developments in nanofabrication using focused ion beams, Small 1, 924–939 (2005)
116. M.D. Uchic, L. Holzer, B.J. Inkson, et al.: Three-dimensional microstructural characterization using focused ion beam tomography, MRS Bull. 32, 408–416 (2007)
117. M.A. Volkert, A.M. Minor: Focused ion beam microscopy and micromachining, MRS Bull. 32, 389–395 (2007)
118 Y.Q. Fu, N.K.A. Bryan, Experimental study of microcylindrical lenses fabricated using focused-ion-beam technology, J. Vac. Sci. Technol. B 19, 4 1259–1263 (2001)
119. S.J. Randolph, J.D. Fowlkes, P.D. Rack: Focused, nanoscale electron-beam-induced deposition and etching, Crit. Rev. Solid State Mater. Sci. 31, 55–89 (2006)
120. N. Silvis-Cividjian, C.W. Hagen: Electron-Beam-Induced Nanometer-Scale Deposition Advances in Imaging and Electron Physics, Vol. 143 (Elsevier Academic, San Diego, CA, 2006)
121. A.N. Broers, W.W. Molzen, J.J. Cuomo, et al.: Electron-beam fabrication of 80-A metal structures, Appl. Phys. Lett. 29, 596–598 (1976)
122. R.W. Christy: Formation of thin polymer films by electron bombardment, J. Appl. Phys. 31, 1680–1683 (1960)
123. H.W.P. Koops, R. Weiel, D.P. Kern, et al.: High-resolution electron-beam induced deposition, J. Vac. Sci. Technol. B 6, 477–481 (1988)
124. S. Matsui, K. Mori: New selective deposition technology by electron-beam induced surface-reaction, Jpn. J. Appl. Phys. Part 2-Lett. 23, L706–L708 (1984)
125. S. Matsui, K. Mori, K. Saigo, et al.: Lithographic approach for 100-nm fabrication by focused ion-beam, J. Vac. Sci. Technol. B 4, 845–849 (1986)
126. W.F. van Dorp, C.W. Hagen: A critical literature review of focused electron beam induced deposition, J. Appl. Phys. 104, 081301 (2008)
127. P.A. Crozier, C.W. Hagen: High-Resolution Electron-Beam-Induced Deposition, In A.A. Tseng (Ed.): Nanofabrication Fundamentals and Applications, pp. 399–430 (World Scientific, River Edge, NJ, 2008)
128. M. Su, V.P. Dravid: Colored ink dip-pen nanolithography, Appl. Phys. Lett. 80, 4434–4436 (2002)
129. A.A. Tseng, A. Notargiacomo: Nanoscale fabrication by nonconventional approaches, J. Nanosci. Nanotechnol. 5, 683–702 (2005)
130. A. Ivanisevic, C.A. Mirkin: "Dip-Pen" nanolithography on semiconductor surfaces, J. Am. Chem. Soc. 123, 7887–7889 (2001)
131. H. Zhang, N.A. Amro, S. Disawal, R. Elghanian, R. Shile, J. Fragala: High-throughput dip-pen-nanolithography-based fabrication of Si nanostructures, Small 3, 81–85 (2007)
132. D. Bäuerle: Laser Processing and Chemistry, 3rd edn. (Springer, Berlin, 2000)
133. G.B. Blanchet, Y.L. Loo, J.A. Rogers, F. Gao, C.R. Fincher: Large area, high resolution, dry printing of conducting polymers for organic electronics, Appl. Phys. Lett. 82, 463–365 (2003)
134. S.D. Allen: Laser chemical vapor-deposition – A technique for selective area deposition, J. Appl. Phys. 52, 6501–5605 (1981)
135. C. Duty, D. Jean, W.J. Lackey: Laser chemical vapour deposition: Materials, modeling and process control, Int. Mater. Rev. 46, 271–287 (2001)
136. M. Stuke, K. Mueller, T. Mueller, K. Williams, R. Oliver, D.A.A. Ohberg, G. Fuhr, R.S. Williams: Direct-writing of three-dimensional structures using laser-based processes, MRS Bull. 32, 32–39 (2007)
137. J.C. Andre, A.L. Methaute, O.D. Wittee: Dispositif pour realiser un modeie de piece industrielle, French Patent No. 8,411,241, July 16 (1884)

138. C. Hull: Apparatus for production of three-dimensional objects by stereolithography, US Patent No. 4,575,330, August 8 (1984)
139. H. Kodama: Automatic method for fabricating a three-dimensional plastic model with photohardening polymer, Rev. Sci. Instrum. 52, 1770–1773 (1981)
140. V.K. Varadan, X. Jiang, V.V. Varadan: Microstereolithography and Other Fabrication Techniques for 3D MEMS (Wiley, Chichester, 2001)
141. X. Zhang, X.N. Jiang, C. Sun: Micro-stereolithography of polymeric and ceramic microstructures, Sens. Actuators 77, 149–156 (1999)
142. W.P. Bichard: Principles and Applications of Photochemistry (Oxford University Press, Oxford, 1998)
143. S. Kawata, H.-B. Sun, T. Tianaka, K. Takada: Finer features for functional microdevices – Micromachines can be created with higher resolution using two-photon absorption, Nature 412, 697–698 (2001)
144. J. Serbin, A. Egbert, A. Ostendorf, B.N. Chichkov, R. Houbertz, G. Domann, J. Schulz, C. Cronauer, L. Frohlich, M. Popall: Femtosecond laser-induced two-photon polymerization of inorganic-organic hybrid materials for applications in photonics, Opt. Lett. 28, 301–303 (2003)
145. S. Maruo, K. Ikuta, H. Korogi: Force-controllable, optically driven micromachines fabricated by single-step two-photon microstereolithography, J. Micromech. Syst. 12, 7 (2003)
146. S. Maruo, K. Ikuta, H. Korogi: Submicron manipulation tools driven by light in a liquid, Appl. Phys. Lett. 82, 133–135 (2003)
147. J. Needham: Science and Civilization in China, Vol. 5, Pt 1 Paper and Printing (Cambridge [Eng.] University Press, Cambridge, 1985)
148. K. Doo-jong: History of Korean printing, Korea J. 3, 22 (1963)
149. P. Hoyer: Semiconductor nanotube formation by a two-step template process, Adv. Mater. 8, 857–859 (1996)
150. P. Hoyer, N. Baba, H. Masuda: Small quantum-sized CdS particles assembled to form a regularly nanostructured porous film, Appl. Phys. Lett. 66, 2700–2702 (1995)
151. T.E. Huber, L. Luo: Far-infrared propagation in metal wire microstructures, Appl. Phys. Lett. 70, 2502–2504 (1997)
152. P.E.J. Legierse, J.H.T. Pasman: Polymers in Information Storage Technology (Plenum, New York, NY 1989)
153. H. Masuda, K. Fukuda: Ordered metal nanohole arrays made by a two-step replication of honeycomb structures of anodic alumina, Science 268, 1466–1468 (1995)
154. W. Michaeli, R. Bielzer: Metal injection molding: Shaping sintered metal parts, Adv. Mater. 3, 260–262 (1991)
155. S.Y. Chou, P.R. Krauss, P.J. Renstrom: Imprint of sub-25 nm vias and trenches in polymers, Appl. Phys. Lett. 67, 3114–3116 (1995)
156. S.Y. Chou, P.R. Krauss, P.J. Renstrom: Imprint lithography with 25-nanometer resolution, Science 272, 85–87 (1996)
157. M. Emmelius, G. Pawlowski, H.W. Vollmann: Materialien für die optische Datenspeicherung, Angew. Chem. Int. Ed. Engl. 101, 1475–1501 (1989)
158. M.T. Gale: Micro-Optics: Elements, Systems and Applications (Taylor & Francis, London, 1997)
159. H.W. Lehmann, R. Widmer, M. Ebnoether, A. Wokaun, M. Meier, S.K. Miller: Fabrication of sub-micron crossed square-wave gratings by dry etching and thermoplastic replication techniques, J. Vac. Sci. Technol. B 1, 1207–1210 (1983)
160. C.M. Rodia, Precision electroforming for optical disk manufacturing, Proc. SPIE Int. Soc. Opt. Eng. 529, 69–75 (1985)
161. K.-H. Schlereth, H. Bötther: Embossed grating lead chalcogenide distributed-feedback lasers, J. Vac. Sci. Technol. B 10, 114–117 (1992)
162. F.P. Shvartsman: Diffractive and Miniaturized Optics (SPIE Optical Engineering Press, Bellingham, WA, 1993)

163. J.S. Winslow: Mastering and replication of reflective videodiscs, IEEE Trans. Consum. Electron. 22, 318–326 (1976)
164. H.C. Haverkorn van Rijsewijk, P.E.J. Legierse, G.E. Thomas: Manufacture of laservision discs by a photopolymerization process, Philips Tech. Rev. 40, 287–297 (1982)
165. J.G. Kloosterboer, G.J.M. Liits, H.C. Meinders: Photopolymerizable lacquers for LaserVision video discs, Philips Tech. Rev. 40, 198–309 (1982)
166. B.D. Terris, H.J. Mamin, M.E. Best, J.A.L. Rugar: Nanoscale replication for scanning probe data storage, Appl. Phys. Lett. 69, 4262–4264 (1996)
167. D.Y. Kim, S.K. Tripathy, L. Li, J. Kumar, Laser-induced holographic surface relief gratings on nonlinear optical polymer films, Appl. Phys. Lett. 66, 1166–1168 (1995)
168. N. Kramer, M. Niesten, C. Schönenberger: Resistless high resolution optical lithography on silicon, Appl. Phys. Lett. 67, 2989–2991 (1995)
169. M. Müllenborn, H. Dirac, J.W. Peterson: Silicon nanostructures produced by laser direct etching, Appl. Phys. Lett. 66, 3001–3003 (1995)
170. U. Reblan, H. Endert, G. Zaal: Laser ablation on the micrometer scale, Laser Focus World 30, 91–96 (1994)
171. M.A. Roberts, J.S. Rossier, P. Bercier, H. Giault: UV laser machined polymer substrates for the development of microdiagnostic systems, Anal. Chem. 69, 2035–2042 (1997)
172. S.A. Weiss: Think small – Lasers compete in micromachining, Photon. Spectra 29, 108–114 (1995)
173. N.L. Abbott, A. Kumar, G.M. Whitesides: Using micromachining, molecular self-assembly, and wet etching to fabricate 0.1–1- μm scale structures of gold and silicon, Chem. Mater. 6, 596–602 (1994)
174. T.J. Hirsch, R.F. Miracky, C. Lin: Selective-area electroless copper plating on polyimide employing laser patterning of a catalytic film, Appl. Phys. Lett. 57, 1357–1359 (1990)
175. V. Malba, A.F. Bernhardt: Laser surface modification for selective electroplating of metal: A 2.5 m/s laser direct write process, Appl. Phys. Lett. 60, 909–611 (1992)
176. A. Miehr, R.A. Fisher, O. Lehmann, M. Stuke: Laser direct writing of beta-Co/Ga and Mn/Ga alloy microstructures from organometallic single-source precursors, Adv. Mater. Opt. Electron. 6, 27–32 (1996)
177. M. Datta: Fabrication of an array of precision nozzles by through-mask electrochemical micromachining, J. Elecrochem. Soc. 142, 3801–3805 (1995)
178. A. Rose, P.K. Weimer: Physical limits to the performance of imaging-systems, Phys. Today 42, 24–32 (1989)
179. M.R.V. Sahyun: Secrecies of photographic development revealed! ChemTech 22, 418–424 (1992)
180. H. Tabei, S. Nara, K. Matsuyama: Method for forming a printed circuit by photolysis of silver salt of organic acid, J. Elecrochem. Soc. 121, 67–69 (1974)
181. S. Leävuori, J. Väänänen, M. Lothi, J. Remes, A. Uusimäki: A novel thick-film technique, gravure offset printing, for the realization of fine-line sensor structures, Sens. Actuators A, 42, 593–596 (1994)
182. H. Moilanen, J. Laalainen, S. Leävuori: Development of piezoelectric micromovement actuator fabrication using a thick-film double-paste printing method, Sens. Actuators A, 43, 357–365 (1994)
183. E. Anczurowski, J. Oliver, R.H. Marchessault: New papers for new printers, ChemTech 16, 304–310 (1986)
184. A.P. Blanchard, R.J. Kaiser, L.E. Hood: High-density oligonucleotide arrays, Biosens. Bioelectron. 11, 687–690 (1996)
185. M. Döring: Inkjet Printing, Philips Tech. Rev. 40, 192–198 (1982)
186. A.V. Lemmo, J.T. Fisher, H.M. Geysen, D.J. Rose: Characterization of an inkjet chemical microdispenser for combinatorial library synthesis, Anal. Chem. 69, 543–551 (1997)
187. Q.M. Pai, B.E. Springett: Physics of electrophotography, Rev. Mod. Phys. 65, 163–211 (1993)

188. M. Stolka: Hard copy materials, ChemTech 19, 487–495 (1989)
189. T.M. Bloomstein, D.J. Ehrlich: Stereo laser micromachining of silicon, Appl. Phys. Lett. 61, 708–781 (1992)
190. O. Lehmann, M. Stuke: Laser-driven movement of three-dimensional microstructures generated by laser rapid prototyping, Science 270, 1644–1646 (1995)
191. D.C. Neckers: Stereolithography – An introduction, ChemTech 20, 615–619 (1990)
192. F.T. Wallenberger: Rapid prototyping directly from the vapor phase, Science 267, 1274–1275 (1995)
193. D. Qin, Y. Xia, J.A. Rogers, R.J. Jackman, X.-M. Zhao, G.M. Whitesides: Microfabrication, microstructures and microsystems, Top. Curr. Chem. 194, 1–20 (1998)
194. Y. Xia: Soft lithography: Micro- and nanofabrication based on microcontact printing and replica molding, Harvard University (1996)
195. H.A. Biebuyck, N.B. Larsen: Lithography beyond light: Microcontact printing with monolayer resists, IBM J. Res. Dev. 41, 159 (1997)
196. A. Kumar, G.M. Whitesides: Features of gold having micrometer to centimeter dimensions can be formed through a combination of stamping with an elastomeric stamp and an alkanethiol "ink" followed by chemical etching, Appl. Phys. Lett. 63, 2002–2004 (1993)
197. Y. Xia, E. Kim, X.-M. Zhao, J.A. Rogers, M. Prentiss, G.M. Whitesides: Complex optical surfaces formed by replica molding against elastomeric masters, Science 273, 347–349 (1996)
198. X.-M. Zhao, Y. Xia, G.M. Whitesides: Fabrication of three-dimensional micro-structures: Microtransfer molding, Adv. Mater. 8, 837–840 (1996)
199. E. Kim, Y. Xia, G.M. Whitesides: Polymer microstructures formed by moulding in capillaries, Nature 376, 581–584 (1995)
200. E. King, Y. Xia, X.-M. Zhao, G.M. Whitesides: Solvent-assisted microcontact molding: A convenient method for fabricating three-dimensional structures on surfaces of polymers, Adv. Mater. 9, 651–654 (1997)
201. A. Afzali, C.D. Dimitrakopoulos, T.L. Breen: High-performance, solution-processed organic thin film transistors from a novel pentacene precursor, J. Am. Chem. Soc. 124, 8812 (2002)
202. J.-F. Chang, B. Sun, D.W. Breiby, M.M. Nielsen, T.I. Sölling, M.G. McCulloch, H. Sirringhaus: Enhanced mobility of poly(3-hexylthiophene) transistors by spin-coating from high-boiling-point solvents, Chem. Mater. 16, 4772–4776 (2004)
203. K. Murata: Super-fine ink-jet printing for nanotechnology, Presented at Proceedings of the International Conference on MEMS, NANO and Smart Systems, Los Alamitos, CA (2003)
204. C.W. Sele, T. von Werne, R.H. Friend, H. Sirringhaus: Lithography-free, self-aligned inkjet printing with sub-hundred-nanometer resolution, Adv. Mater. 17, 997 (2005)
205. Y.-L. Loo, J.W.P. Hsu, R.L.Willett, K.W. Baldwin, K.W.West, J.A. Rogers: High-resolution transfer printing on GaAs surfaces using alkane dithiolmonolayers, J. Vac. Sci. Technol. B 20, 2853 (2002)
206. W.R. Childs, R.G. Nuzzo: Decal transfer microlithography: a new soft-lithographic patterning method, J. Am. Chem. Soc. 124, 13583 (2002)
207. M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B.J. Choi, M. Wedlake, T. Michaelson, S.V. Sreenivasan, J. Ekerdt, C.G. Willson: Step and flash imprint lithography: A new approach to high-resolution patterning, Presented at SPIE's 24th International Symposium on Microlithography: Emerging Lithographic Technologies III, Santa Clara, CA (1999)
208. P.S. Hong, J. Kim, H.H. Lee: Contrast modified room-temperature imprint lithography, Appl. Phys. Lett. 88, 173105 (2006)
209. H. Lee, G.-Y. Jung: Wafer to wafer nano-imprinting lithography with monomer based thermally curable resin, Microelectron. Eng. 77, 168–174 (2005)
210. S.Y. Chou, C. Keimel, J. Gu: Ultrafast and direct imprint of nanostructures in silicon, Nature 417, 835 (2002)

211. H.W. Ro, R.L. Jones, H. Peng, D.R. Hines, H.-J. Lee, Eric K. Lin, A. Karim, D.Y. Yoon, D.W. Gidley, C.L. Soles: The direct patterning of nanoporous interlayer dielectric insulator films by nanoimprint lithography, Adv. Mater. 19, 2919–2924 (2007)
212. S.Y. Chou, P.R. Krauss, W. Zhang, L. Guo, L. Zhuang: Sub-10 nm imprint lithography and applications, J. Vac. Sci. Technol. B 15, 2897 (1997)
213. H. Schift: Nanoimprint lithography: An old story in modern times? A review, J. Vac. Sci. Technol. B 26, 458–480 (2008)
214. X. Cheng, L.J. Guo: A combined-nanoimprint-and-photolithography patterning technique, Microelectron. Eng. 71, 277–282 (2004)
215. L.J. Guo: Recent progress in nanoimprint technology and its applications, J. Phys. D-Appl. Phys. 37, R123–R141 (2004)
216. W. Wang, S.A. Soper: Bio-MEMS: Technologies and Applications (CRC Press, Boca Raton, FL, 2007)
217. Y. Zhang, J. Lu, H. Zhou, T. Itoh, R. Maeda: Application of nanoimprint technology in MEMS-based micro direct-methanol fuel cell (μ-DMFC), J. Microelectromech. Syst. 17, 1020 (2008)
218. X. Fan, H. Zhang, S. Liu, A. Hu, K. Jia: NIL – A low-cost and high-throughput MEMS fabrication method compatible with IC manufacturing technology, Microelectron. J. 37, 121 (2006)
219. D.R. Hines: Organic Electronics with Polymer Dielectrics on Plastic Substrates Fabricated Via Transfer Printing (University of Maryland, College Park, MD, 2007)
220. D.R. Hines, A.E. Southard, A. Tunnell, V. Sangwan, T. Moore, J.-H. Chen, M.S. Fuhrer, E.D. Williams: Transfer printing as a method for fabricating hybrid devices on flexible substrates, Proceedings of the SPIE, San Diego, CA (2007)
221. D.R. Hines, S. Mezhenny, M. Breban, E.D. Williams, V.W. Ballarotto, G. Esen, A. Southard, M.S. Fuhrer: Nanotransfer printing of organic and carbon nanotube thin-film transistors on plastic substrates, Appl. Phys. Lett. 86, 163101–163103 (2005)
222. D. Janssen, R.D. Palma, S. Verlaak, P. Heremans, W. Dehaen: Static solvent contact angle measurements, surface free energy and wettability determination of various self-assembled monolayers on silicon dioxide, Thin Solid Films 515, 1433–1438 (2006)
223. M. Coll, L.H. Miller, L.J. Richter, D.R. Hines, O.D. Jurchescu, N. Gergel-Hackett, C.A. Richter, C.A. Hacker: Formation of silicon-based molecular electronic structures using flipchip lamination, J. Am. Chem. Soc. 131, 12451–12457 (2009)
224. K.J. Lee, M.J. Motala, M.A. Meitl, W.R. Childs, R. Menard, A.K. Shim, J.A. Rogers, R.G. Nuzzo: Large-area, selective transfer of microstructured silicon: A printing-based approach to high-performance thin-film transistors suorted on flexible substrates, Adv. Mater. 17, 2332–2336 (2005)
225 D.R. Hines, A. Southard, M.S. Fuhrer: Poly(3-hexylthiophene) thin-film transistors with variable polymer dielectrics for transfer printed flexible electronics, J. Appl. Phys. 104, 024510 (2008)
226. Photomask Basicsfor Stanford Users: Available http://snf.stanford.edu/Process/Masks/PhotomaskBasics-General.pdf
227. S. Rizvi: Handbook of Photomask Manufacturing Technology (CRC Press, Boca Raton, FL, 2005)
228. O. Takaoka: Advanced photomask defect repairing technology using FIB and SPM, Int. J. Autom. Technol. 2 (2008)
229. L. Li, R.R. Gattass, E. Gershgoren, H. Hwang, J.T. Fourkas: Achieving lambda/20 resolution by one-color initiation and deactivation of polymerization, Science 324, 910–913 (2009)
230. C.N. LaFratta, J.T. Fourkas, T. Baldacchini, R.A. Farrer: Multiphoton fabrication, Angew. Chem. Int. Ed. 46, 6238–6258 (2007)
231. L. Li, J.T. Fourkas: Multiphoton polymerization, Mater. Today 10, 30–37 (2007)
232. L. Li: Multiphoton absorption: Fabrication, functionalization and applications, PhD dissertation, University of Maryland, College Park, MD (2009)

233. C.N. LaFratta: Multiphoton Absorption Polymerization: Issues and Solutions (University of Maryland College Park, College Park, MD, 2006)
234. W. Chu, A. Yen, K. Ismail, I. Shepard, H.J. Lezec, C.R. Musil, J. Melngailis, Y.-C. Ku, J.M. Carter, H.I. Smith: Syb-100-nm x-ray mask technology using focused-ion beam lithography, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 7, 1583 (1989)
235. M.A. Hartney, D.C. Shaver, M.I. Shephard, J.S. Huh, J. Melngailis: Silyation of focused ion beam exposed resists, Appl. Phys. Lett. 59, 485 (1991)
236. S. Matsui, Y. Kojima, Y. Ochiai: High-resolution focused ion beam lithography, Appl. Phys. Lett. 53, 868 (1988)
237. A. Milgram, J. Puretz: A bilevel resist for ion beam lithography, J. Vac. Sci. Technol. B 3, 879 (1985)

Chapter 10
Doping Processes for MEMS

Alan D. Raisanen

Abstract Doping processes are utilized to modify electrical properties of semiconductors by making mobile charge carriers available in the material. Doping processes are used in MEMS devices for creating electrically conductive layers for power distribution, heaters, transducers, and other structures. Doped layers are also widely used for controlling specialty etch processes by modification of surface electrochemistry. Typical MEMS doping applications, standard processes for doping MEMS materials, and diagnostic techniques are reviewed.

10.1 Overview

The doping of semiconductors is one of the oldest and most fundamental processes used in making semiconductor devices. Doping processes alter the concentration and distribution of free carriers in a semiconductor matrix, making possible electronic devices based on p−n junctions or metal–oxide–semiconductor structures. Doping processes are also critical for the successful formation of electrical contacts in devices fabricated from semiconductors, not only for transistors and other electronic systems but also for MEMS devices based on silicon or other materials. The scientific literature related to doping processes for electronic devices is quite extensive, describing details of dopant distribution and electrical activation important in forming ever-shallower dopant profiles for devices at smaller length scales. In contrast, the role of doping processes in current MEMS fabrication is relatively straightforward and primarily affects creation of electrically conductive layers and layers modified to alter material etch properties.

Doped MEMS structures are most heavily utilized as resistive structures for heaters in thermally driven actuator devices, as heaters in microchemical reactors, or as piezoresistors in sensor devices. More indirectly, doping processes can be utilized

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in sophisticated fabrication techniques utilizing differential etch rates between volumes of silicon doped by different dopant species or concentrations. Most of discussion here is limited to silicon applications as much of MEMS work to date is focused on silicon, but all the concepts are generally applicable to other semiconductor materials.

10.2 Applications

10.2.1 Electrical Properties

Doping is primarily a means of altering the electronic properties of semiconductors by introducing impurities that contribute free carriers (electrons and holes). Intrinsic (undoped) semiconductor crystals will contain a modest concentration of carriers due to simple thermal excitation and defects. This intrinsic carrier density depends on the semiconductor energy gap and on the temperature [1]. Intrinsic carrier concentration increases exponentially with temperature as illustrated for Ge and Si single crystals in Fig. 10.1. Unfortunately, at reasonable temperatures these relatively low intrinsic carrier concentrations are insufficient for most technologically interesting purposes such as p–n junctions and etch modification, and the large variation in carrier concentration observed as a function of temperature limits the ability to design devices that operate reliably over a significant temperature range. Impurity atom dopants can be added to the crystal to overcome these deficiencies. Still, thermal excitation of intrinsic carriers can become important for semiconductor devices that reach a high temperature, such as heater elements [2]. At a certain point, intrinsic carrier excitation becomes large enough that it can initiate

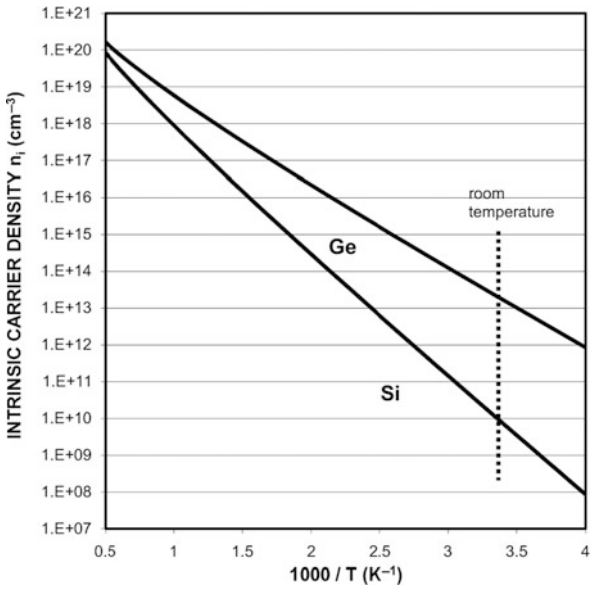

Fig. 10.1 Intrinsic carrier concentration in undoped Si and Ge crystals as a function of temperature (Calculated from models in [1])

a thermal runaway event, with large currents producing high temperatures, which excite higher intrinsic carrier densities enabling even higher currents, and eventual catastrophic results for the device.

Silicon single crystals have a diamond lattice structure illustrated in Fig. 10.2, with an underlying face-centered cubic structure and tetrahedrally bonded Si atoms. Many other technically important semiconductors have a similar diamond or zincblende structure, such as Ge, GaAs, or β-SiC [3]. In order for impurity atoms to function as electrically active dopants in the silicon structure, they must be capable of contributing a mobile electron or hole without acting as an electronic trap or recombination center [4]. For Si crystals, viable doping impurities are primarily found in either group III or group V of the periodic table (Fig. 10.3).

Group III atoms such as boron, aluminum, and gallium, when incorporated into the silicon semiconductor lattice, form an empty localized electronic state in the semiconductor bandgap located just above the valence band edge. Electrons in the valence band are easily promoted into this state at moderate temperatures, resulting in a nonlocalized, mobile hole state in the valence band. This hole then acts as a free carrier in the semiconductor crystal, allowing it to support a current flow. These group III dopants are known as electron *acceptors*, and a silicon crystal with an excess of acceptor levels is defined as p-type.

Group V atoms such as phosphorus, antimony, and arsenic also form localized electronic states in the silicon bandgap, but these impurities form filled states just below the conduction band edge. At moderate temperatures, electrons occupying these states are easily promoted into the conduction band of the semiconductor, where they act as free electronic carriers. These dopants are known as electron *donors*, and a crystal with an excess of donor levels is defined as n-type. It is possible for a semiconductor crystal to be doped with both donor- and acceptor-type dopants simultaneously. The donors and acceptors then effectively cancel each other out (compensation), and the crystal type is essentially determined by which dopant type predominates.

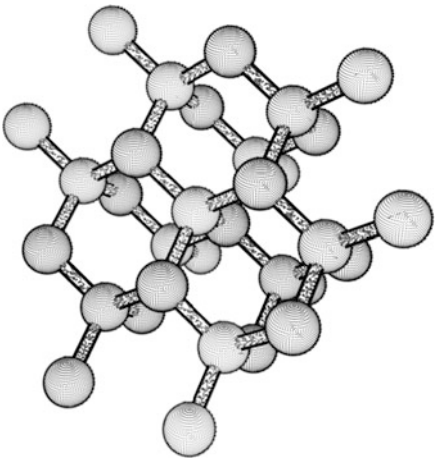

Fig. 10.2 Atomic arrangement of a silicon crystal illustrating the diamond lattice structure

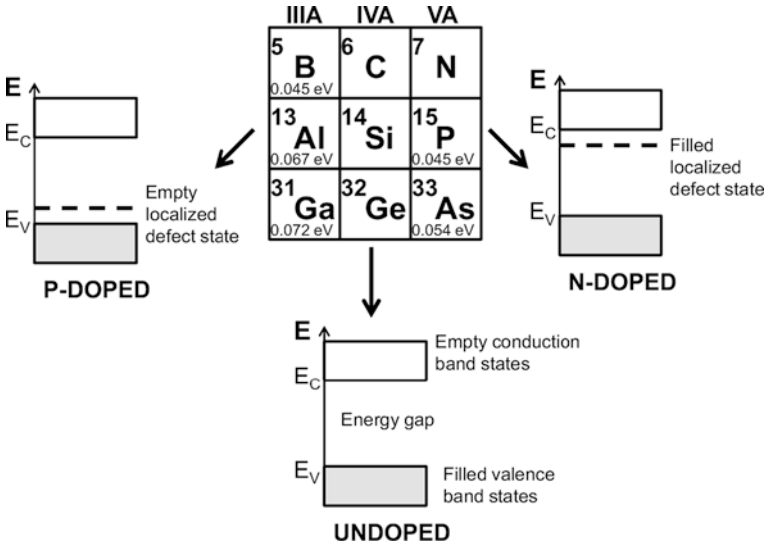

Fig. 10.3 Portion of the periodic table showing group IV semiconductors and some dopants important for silicon technologies. Schematic band structures of the silicon crystal are shown for p-doped (group III impurity), undoped, and n-doped (group V impurity). Energy shown in electron volts corresponds to the separation between the acceptor state and valence band edge (p-dopants), or between the donor state and the conduction band edge (n-dopants) (Ionization energy data from [5])

Impurity atoms added to the crystal can occupy a variety of locations including individual interstitial sites between silicon atoms, agglomerated as clusters of impurity atoms, or at lattice sites replacing a silicon atom. Missing atoms, displaced atoms, dislocations, and other crystal imperfections are also present in any real semiconductor, and many of these defects can have a significant effect on the semiconductor electronic structure [6]. See Fig. 10.4. Although many of these point

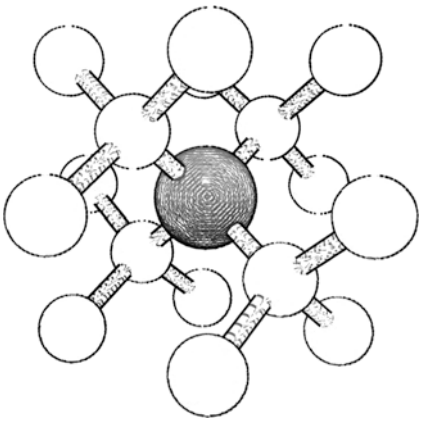

Fig. 10.4 Dopant atom incorporation in a silicon lattice as a substitutional impurity

and extended defect structures can act as dopants in a semiconductor, they are generally very difficult to control from an engineering standpoint. Reproducible devices are generally made by controlled introduction of substitutional defects. In order to be electrically active and contribute to the conductivity of the silicon crystal, the dopant atom must be incorporated into the silicon lattice as a substitutional impurity. Impurity atoms residing in other sites can act as scattering or recombination centers, degrading carrier mobility without adding to free carrier concentration. Silicon atoms displaced from lattice sites can also add states in the bandgap, acting as dopants or scattering centers. These self-interstitial dopants can become important in ion implant processes or other processes that cause silicon crystal damage.

The most commonly used dopants in silicon include B as an acceptor and P, As, and Sb as donors. These dopants are chosen for ease of processing, high solid solubility, and controllable diffusion characteristics. Dopants may be introduced into the crystal during growth or deposition, or introduced externally by diffusion or ion implantation [7]. It is a straightforward exercise to adjust the dopant concentration in the crystal to obtain a desired material resistivity through a very broad range, for applications like silicon-based resistors or heater elements. Figure 10.5 illustrates the relationship of silicon crystal resistivity to carrier concentration for phosphorus (n-type, donor) and boron (p-type, acceptor) impurity atoms at 300 K.

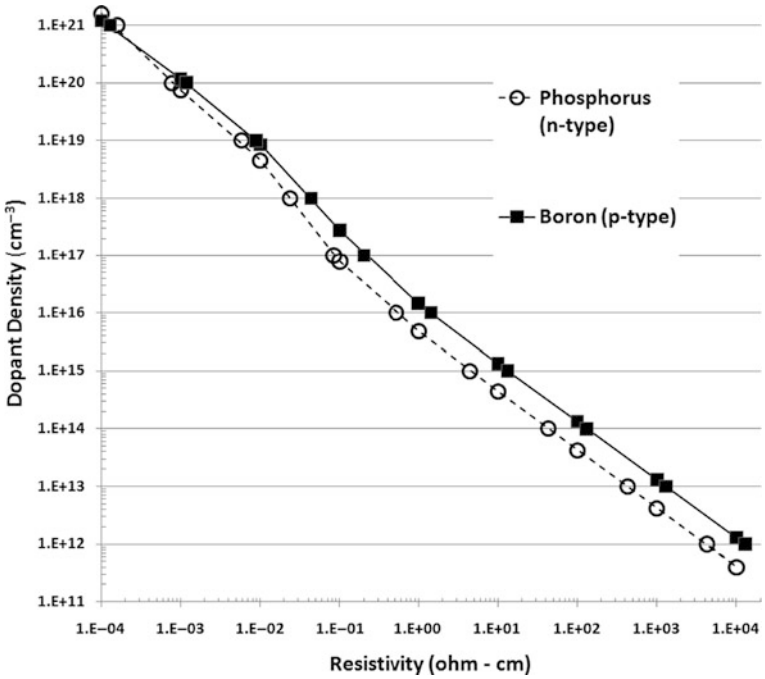

Fig. 10.5 Resistivity of boron and phosphorus doped silicon as a function of dopant concentration at 300 K (Data tabulated in [8])

The total amount of dopant which may be loaded into a silicon crystal is limited by the solid solubility of the impurity atom in the silicon lattice. If a higher dopant concentration is attempted, additional dopant atoms will fail to incorporate in the silicon lattice, instead segregating into inclusions or clusters of dopant atoms that do not contribute to the crystal's carrier concentration, and may in fact degrade the conductivity of the crystal by trapping or scattering mobile carriers. Figure 10.6 illustrates the measured solid solubilities of different species in silicon as a function of temperature [9–11]. Standard silicon dopants such as B, As, and P have quite high solid solubility, making it possible to very heavily load silicon with active dopants to obtain high electrical conductivities.

In MEMS technologies, one of the key applications of doping technology is fabrication of conductors and resistors in silicon, as schematically illustrated in Fig. 10.7. These structures are easy to integrate into a variety of silicon processing schemes in both bulk and surface micromachining processes. Silicon conductors and resistors require high-temperature processing to implement but will also tolerate very high temperatures without damage, making them ideal for process sequences involving anneals for stress relief, thermal oxidation, or other high-temperature processes.

In addition to being utilized as gate electrodes in MOS devices and as general interconnect "wiring" on a chip [7], heavily doped silicon layers are commonly used as electrically conductive structural elements. These materials find use in electrostatically driven devices such as comb drives [12], which benefit from the highest conductivity, and thus highest active doping density, obtainable. Single-crystal

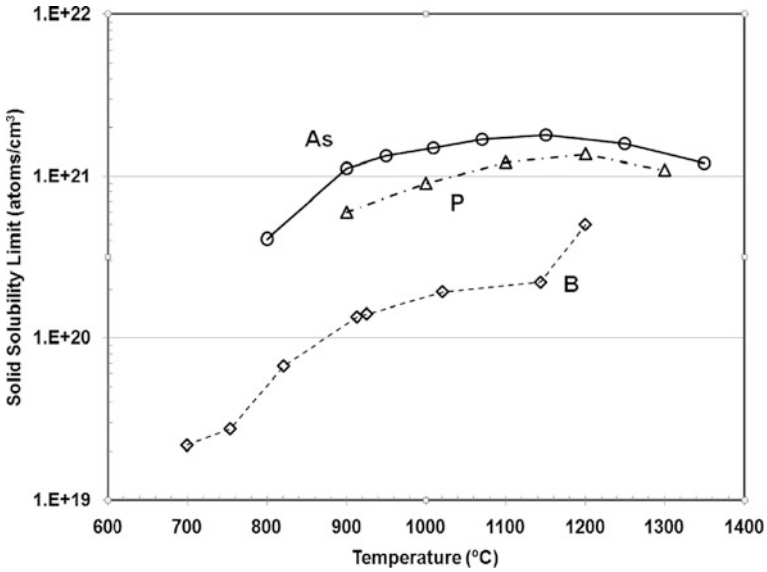

Fig. 10.6 Solid solubility of important dopants in Si as a function of temperature (Boron from Vick [9] and Trumbore [10], phosphorus from Trumbore [10], and arsenic from Trumbore [10] and Sandhu [11]. Used with permission)

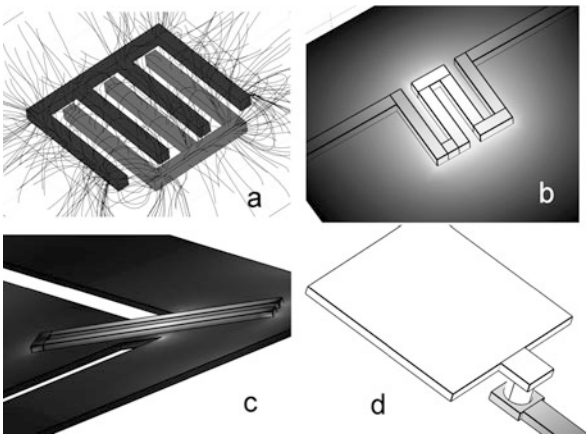

Fig. 10.7 Archetypical applications of doped Si structures in MEMS: (**a**) electrostatic structure (comb drive, showing electric field lines), (**b**) transducer resistive element (electrical heater, showing thermal power dissipation), (**c**) sensing resistive element (strain gauge on supported diaphragm, showing Von Mizes stress), and (**d**) electrical contact to metal pad for input/output

silicon or silicon-on-insulator materials used to fabricate such structures can be readily obtained with resistivities down to 10^{-3} Ω cm or better. Deposited materials such as polysilicon thin-films will be substantially worse due to lower mobilities and higher scattering, but even polysilicon is easily doped to resistivities of 0.1 Ω cm, corresponding to sheet resistances of 25 Ω/square for a 500 nm thick layer.

Resistive elements may be fabricated with a very broad range of resistive values. The greatest advantage of silicon as a resistor material is that the resistivity may be tuned to match the needs of the application through about seven orders of magnitude as illustrated in Fig. 10.5. In contrast, most thin-film resistor materials such as TiW or TaN can only be adjusted through a comparatively narrow range by altering process conditions such as reactive gas background, pressure, or deposition temperature [13].

Resistors in MEMS are often used as heater elements to provide motion via differential thermal expansion, or as simple heaters to drive chemical reactions. Silicon resistors also make excellent strain gauge elements for mechanical sensing applications. The resistance of a resistor is significantly altered by a mechanical stress applied to the device, according to the piezoresistive coefficient of the resistive material. In silicon, the piezoresistive coefficient decreases as the doping level increases. For maximum sensitivity to mechanical stress, a low doping concentration, and hence high resistivity, is advantageous.

Figure 10.8 illustrates piezoresistive coefficients for single-crystal silicon at 25°C in the (100) plane, a common SEMI standard wafer type used in the microelectronics industry. The data are consolidated from data and calculations by Kanda [14]. Longitudinal coefficients correspond to the case where the mechanical stress is applied parallel to the current flow in the silicon, and transverse coefficients correspond to the case where the applied mechanical stress is perpendicular to the

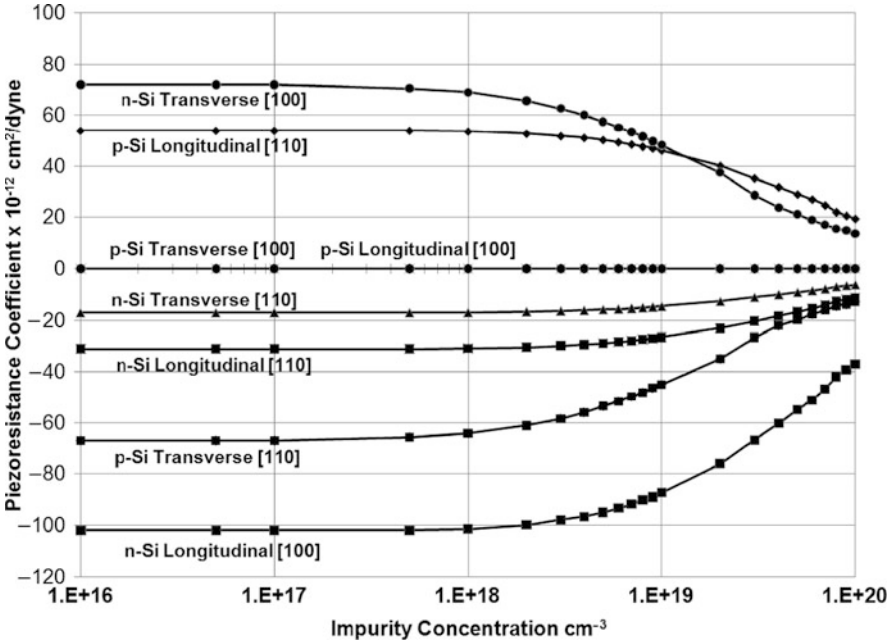

Fig. 10.8 Single-crystal silicon piezoresistive coefficients as a function of active impurity concentration for p-type and n-type material. Transverse coefficients indicate that the tensile stress and electric current are at right angles to each other, and longitudinal values indicate that the stress and electric currents are parallel (Consolidated from calculations by Kanda [14], used with permission)

current flow. Coefficients are shown for resistors oriented in the [100] direction, oriented 45° to the flat on a (100) wafer, or resistors oriented in the [110] direction, perpendicular or parallel to the (100) wafer flat. These are common resistor configurations for strain sensors on cantilevers or membranes fabricated on a silicon surface.

The change in resistance of a resistor is then related to the piezoelectric coefficient by

$$\frac{\Delta\rho}{\rho} = \Pi\sigma \tag{10.1}$$

where σ is the applied mechanical stress and Π is the piezoelectric coefficient in the appropriate direction. Figure 10.8 clearly implies that resistors oriented in the [100] direction are best fabricated from n-doped material, whereas resistors in the [110] direction will have highest sensitivity if fabricated from p-doped material. Polysilicon is also widely used for piezoresistive sensors despite having typically lower piezoresistive response compared to single crystal silicon [15], although the piezoresistive coefficients show considerable variation related to polysilicon microstructure and fabrication details.

Silicon is commonly used as a "local interconnect" material in microelectronic and MEMS devices [7]. Although it has relatively high resistivity relative to metallic conductors such as aluminum, silicon will tolerate high-temperature processing and is quite suitable for short electrical leads. Fabricating these local interconnects or resistors is usually a straightforward process of doping the silicon to a conveniently high value, annealing it to redistribute and activate the dopants, then patterning and etching the silicon to produce a well-defined lead or resistor structure.

In order to fully utilize silicon as a conductive material, it is generally necessary to form metal contacts on the surface to allow the connection of wires or other probes in a packaged device. Gold and aluminum wire bonds to metal pads are very common interconnect methods, and high-volume applications use solder bumps formed on the metal pad to enable "flip-chip" and related packaging techniques. For research purposes, making direct contacts to heavily doped silicon with a metal probe tip is possible, but such simple contacts tend to be mechanically and electrically unreliable for anything other than short-term usage.

Metal–semiconductor contact formation is a topic that has received heavy investigation over the decades [16], and continues to receive attention to this day. Application of a metal film to a semiconductor surface causes a redistribution of charge carriers in the near-surface region of the semiconductor as illustrated by the energy-level diagrams in Fig. 10.9. The metal, shown in Fig. 10.9a on the left, is

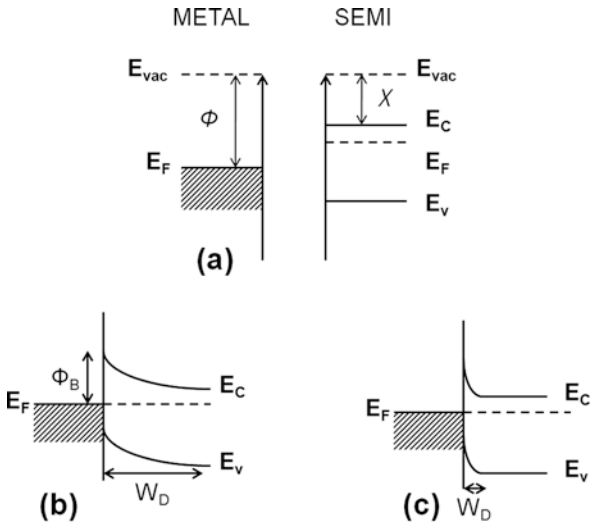

Fig. 10.9 Energy band diagrams for metal/n-semiconductor contacts. The metal and semiconductor surfaces are separated in (**a**), showing the respective Fermi levels, valence and conduction bands, and vacuum levels. The two surfaces are placed in contact in (**b**), illustrating the redistribution of charge which brings the metal and semiconductor Fermi levels into alignment, producing band bending of the conduction and valence bands in the semiconductor. A Schottky barrier of height Φ_B is generated at the interface. In (**c**), the doping level of the semiconductor is much higher than in (**b**), producing a very narrow depletion width W_D, through which carriers can easily tunnel

described by a partially filled set of electronic states. One can define an energy reference called the Fermi level, denoted E_F, which designates the energy at which the probability of the states at that energy being occupied is 0.5. At absolute zero, this implies the states above E_F are empty and the states below E_F are filled, but at finite temperatures there is a tailing off of occupied states towards higher energy leading to a distribution of occupied and unoccupied states centered at the Fermi level.

The vacuum level E_{vac} is the energy above which an electron is no longer bound to the solid; that is, it becomes a free electron in space. The difference between the vacuum level E_{vac} and the Fermi level E_F is known as the work function Φ of the metal. In the semiconductor, we have a conduction band edge at E_C, above which electrons are free to move as carriers under the influence of an electric field, and a valence band edge E_V, below which holes can move as carriers. The semiconductor also has a well-defined Fermi level E_F, where the probability of an electronic state being occupied is 0.5. In the example illustrated, the semiconductor is n-type, because E_F is close to E_C implying the presence of carriers in the conduction band. The energy difference between the conduction band and the vacuum level in the semiconductor is called the electron affinity χ, which is analogous to the metal's work function.

When the metal and semiconductor are brought together, charge will move from one side to the other until the Fermi levels align on both sides. This charge redistribution makes one side slightly positive and the other side slightly negative, inducing a built-in electric field at the junction. This electric field alters the electronic structure of the semiconductor as shown in Fig. 10.9b, a phenomenon known as band bending. The discontinuity between the semiconductor conduction band (in the n-type semiconductor example shown here) and the metal Fermi level produces a barrier against electronic transport across the boundary. This discontinuity, called the Schottky barrier Φ_B has a height equal to the difference between the metal Fermi level and the semiconductor electron affinity. The band bending area is called the depletion region, where electrons in the example illustrated have transferred into the metal. Similar diagrams can be generated for p-type semiconductors [5], where holes diffuse into the metal and the discontinuity is between the metal Fermi level and the valence band of the semiconductor. The width of this depletion region is determined by the doping level of the semiconductor, with higher doping levels producing narrower depletion regions.

The presence of a Schottky barrier at a metal–semiconductor interface has profound implications for electron transport through these junctions. In essence, a significant barrier height produces a rectifying junction with electrical properties similar to a diode, allowing easy current flow in only one direction. Some electronic devices make explicit use of this phenomenon, but it is typically undesirable for making good electrical contacts with predictable bidirectional current flow properties. See Fig. 10.9.

In principle, matching a metal work function with a semiconductor electron affinity would eliminate this barrier entirely, but in practice this does not work in most cases due to the presence of defect states at the interface, metal–semiconductor intermetallic phase formation, or other complicating factors [16]. The technique

employed by most workers is to dope the semiconductor, or at least the surface region of the semiconductor, to a high level, resulting in a very narrow depletion width (<100 nm). Even if the actual Schottky barrier height is quite large, electrons and holes can simply tunnel through the narrow barrier, enabling low-resistance current transport in either direction [5]. Doping densities of 1×10^{18} cm^{-3} or better are common for contact formation applications. Simple aluminum contacts on doped silicon are most common in the MEMS world, but specific contact metallurgies and doping strategies are usually required to create good ohmic contacts for different semiconductors [17].

10.2.2 Etch Stop Techniques

Although dopant processes in semiconductors are most commonly used for producing electrically active devices, dopants also have an important role in bulk micromachining fabrication sequences. Modification of the dopant concentration in silicon and other semiconductors has the useful effect of altering the etch rate of the semiconductor matrix in specific etchants. This effect can be employed as a reasonably accurate etch stop for fabrication of thin unsupported membranes or other structures, and forms the basis for a variety of electrochemical etch techniques.

Silicon can be etched with a number of wet chemical etches, including mixtures of hydrofluoric (HF), nitric (HNO_3), and acetic (CH_3COOH) acids [18], heated mixtures of ethylene diamine ($C_2H_4(NH_2)_2$), pyrocatechol ($C_6H_4(OH)_2$), and water [19], tetramethyl ammonium hydroxide ($(CH_3)_4NOH$) [20], and solutions of hot potassium hydroxide (KOH) and water [21]. All of these commonly used silicon etches are significantly sensitive to the doping level of the silicon material being etched.

Hydrofluoric acid, nitric acid, and acetic acid (HNA) constitute a common wet isotropic etch solution for silicon and polysilicon, with typical etch rates of a few microns per minute. It is possible to use standard photoresist films to mask this etchant for short times, although the resist is attacked by the strong oxidizer HNO_3 and the interface between silicon and the photoresist is often attacked during etches of more than a few microns causing film peeling and pattern failure. Silicon dioxide, silicon nitride, and sometimes gold are used as etch masks for deeper etches. The HNA etch chemistry can be difficult to use reproducibly because the etch rate, selectivity, and even etch profile (Fig. 10.10) depend on the chemical mixture

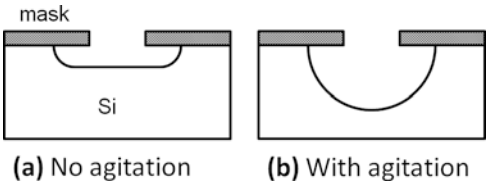

Fig. 10.10 Isotropic HNA etch profiles generated (**a**) without solution agitation, (**b**) with solution agitation

composition and age, agitation, and doping of the silicon material itself. Defects in the silicon can also affect the etch significantly, and many workers use the HNA etch and variants to "decorate" and delineate various crystal defects.

Models of the mechanism by which HNA etches silicon involve injection of holes to increase the oxidation state of the silicon atoms, enabling attachment of hydroxyl groups (OH^-) [22]. The oxidized silicon then reacts with the HF in the solution to produce soluble hexafluorosilicic (H_2SiF_6) species, which dissolve in the solution. The key factor that makes these etches interesting from a doping perspective is the necessity for hole injection to initiate the etch, rendering this etch susceptible to changes in doping concentration of the material being etched. With the correct etchant concentration, silicon doped in excess of 10^{17} cm^{-3} of either n- or p-type will be etched rapidly, whereas silicon with a lighter doping level will be etched more slowly [23]. This differential etch rate can be utilized in MEMS fabrication for producing channels, releasing membranes, and other three-dimensional structures. Many workers attempting these etch processes have encountered significant difficulties in reproducing exact results found in the literature, as etch results tend to be sensitive to low levels of chemical contaminants, roughness of the silicon surface, presence of defects, and other minor variables [24]. Specific process recommendations are given in the process selection guide following this section. See Fig. 10.11.

In contrast to the isotropic HNA wet chemical etch, ethylenediamine/pyrocatechol (EDP), TMAH, and KOH etches are highly anisotropic; that is, they have very different etch rates in different crystallographic directions within the silicon crystal. This effect can be used to produce geometrically faceted structures, self-limited channel etches, nozzles, and controlled undercuts or release etches with a minimum of masking steps [12].

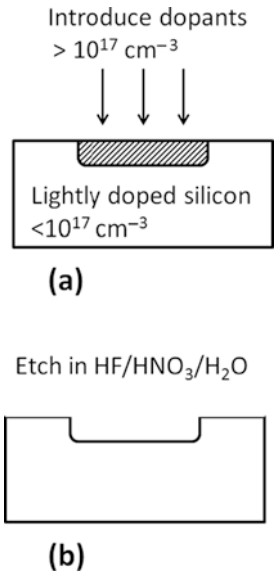

Fig. 10.11 Dopant-dependent etch stop procedure for isotropic HNA etch. Lightly doped silicon is not etched, whereas heavily doped material is dissolved

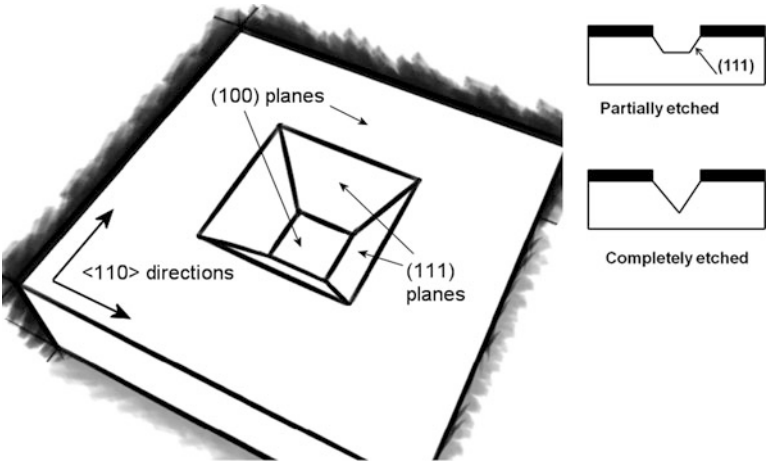

Fig. 10.12 Geometry of silicon orientation-dependent etch processes

Figure 10.12 illustrates one of the most common geometric arrangements used by MEMS researchers, with a (100) surface plane wafer covered by a mask with a square hole in it oriented along <110> directions. The masking material is usually silicon nitride, although silicon dioxide can be used for relatively short etches as it is slowly attacked, by KOH in particular. When exposed to the anisotropic etch chemistries, the (100) planes etch rapidly, and the (111) planes etch relatively slowly. A geometric structure is revealed composed of (111) planes, which forms a pyramidal etch pit terminating in a point if it is allowed to etch to completion.

One of the useful features of this type of etch is its self-limiting behavior; timing is not critical as etching essentially stops once (111) planes are all that remain. Long v-shaped grooves can be fabricated by opening long slots in the mask, and the depth of the grooves will be determined by the width of the slot. Holes for vias or nozzles can be etched right through the entire silicon wafer by making certain that the mask opening is large enough to prevent the (111) planes from coming to a point before the wafer is etched completely through.

The atomic density of each crystal plane is regarded as the origin of the etch rate anisotropy [25]. The (111) plane in silicon has the highest atomic packing density and lowest number of dangling bonds per unit area, and is therefore the slowest etching plane. Other plane etch rates vary according to their relative atomic packing densities and bond densities. The mechanism of etching in these alkaline solutions is believed to involve injection of electrons during Si reaction with hydroxyl ions in the solution, which enables dissociation of water molecules and production of hydrogen and silicates $Si(OH)_6^{2-}$ [21]. The silicates are then complexed by the etch solution forming soluble silicon-containing species. Dangling bond densities, as well as formation of a screening boundary layer of water molecules at the surface, both of which vary according to the crystal plane exposed, are also believed to play a role in setting the anisotropic etch rates observed between crystal planes.

A common structure fabricated with the anisotropic etch process is a thin diaphragm made of silicon, used in pressure sensors and various transducers. If the etch rate and wafer thickness are known, it is possible to time the etch and remove a wafer from the anisotropic etchant before etching penetrates all the way through the silicon, leaving a thin membrane. Control of the membrane thickness by this method is difficult, as the etch rate varies somewhat depending on solution age, and the thickness of silicon wafers varies slightly between individual wafers. Fortunately, the etch rate of silicon in these anisotropic etchants varies with doping level.

High levels of boron doping have been found to inhibit the etching of KOH [26, 27], EDP [28], and TMAH [29] anisotropic etchants, as illustrated in Fig. 10.13. Doping densities of $1 \times 10^{19} - 1 \times 10^{20}$ cm^3 or higher are required, which approach the solid solubility limits for boron. Other dopants, such as phosphorus, or even nondopants such as germanium are reported to exhibit this effect to a lesser degree [28], but are more difficult to implement as etch stops due to the very high doping densities required. Seidel [28] explains this etch stop behavior in terms of the strong band bending produced at the silicon interface by the highly doped layer. Normally, electrons injected into the silicon from the etch solution will be confined near the interface due to the presence of a Schottky barrier, where they will be available to reduce water molecules necessary to drive the reaction.

A heavily doped boron layer produces a very narrow depletion width at the interface, as illustrated in Fig. 10.9c. Electrons at the surface can easily tunnel through

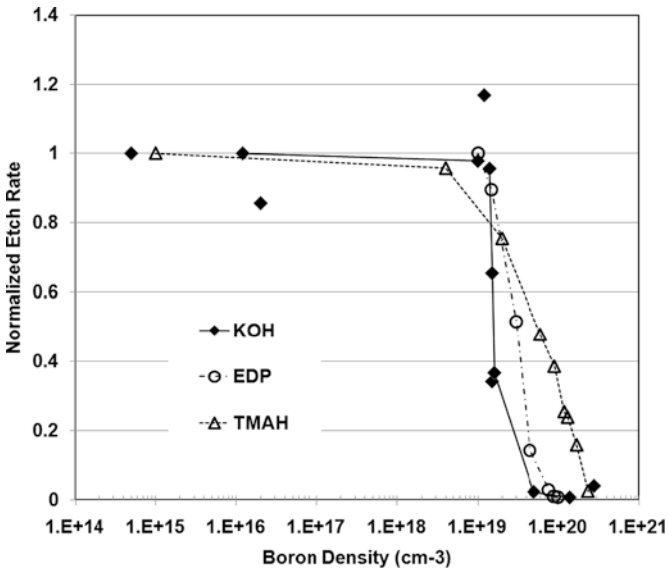

Fig. 10.13 Relative etching rates of boron-doped silicon (100) planes in KOH, EDP, and TMAH anisotropic etch chemistries as a function of doping level. (KOH data from [26, 27], EDP from [28], and TMAH from [29], used with permission)

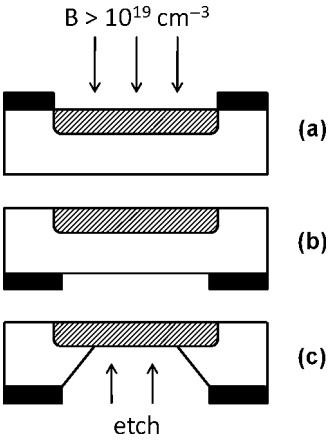

Fig. 10.14 Boron etch stop used to fabricate a thin diaphragm in (100) silicon using anisotropic etchant

this narrow depletion region and diffuse into the crystal bulk, starving the surface silicon oxidation reaction and stopping the etch.

To fabricate a structure such as a thin silicon diaphragm, a process like the one schematically illustrated in Fig. 10.14 is used. The front surface of a wafer is heavily doped by boron, with the depth of the doped layer selected by the desired thickness of the final diaphragm structure. The wafer is then etched from the backside through an opening designed to fit the desired lateral size of the final diaphragm structure. The etch proceeds until the heavily boron doped region is encountered, at which point the etch rate decreases by one to three orders of magnitude. The etch rate decrease makes it relatively easy to remove the wafer from the etchant before the diaphragm is penetrated, and allows good control of final diaphragm thickness. The very high doping density, however, makes integration of this process with conventional CMOS electronics difficult.

Transistors are difficult to fabricate with high substrate doping levels, and high boron concentration produces mechanical stress and defects in the silicon that compromise electronic performance [30]. In addition, boron can outdiffuse during high-temperature processing steps, producing undesired doping in other parts of the chip. Deposition of a lightly doped silicon epilayer on the boron doped layer can be used to overcome this issue in some cases.

The dependence of silicon etch rate on doping, and more fundamentally on the transfer of electrons and holes between the surface and the etch solution, suggests that etch rates could be controlled electrochemically by altering a potential applied between the silicon surface and the etch solution. A number of electrochemical etch stop arrangements have been developed [30–32] that allow very precise control of etching without requiring the extreme doping densities of the conventional boron etch stop.

An electrochemical cell schematically illustrated in Fig. 10.15 is configured to allow application of an electrical potential between the wafer to be etched and an immersed counterelectrode. When a potential is applied between the p−n junction and the counterelectrode, charge is able to flow across the silicon/solution barrier

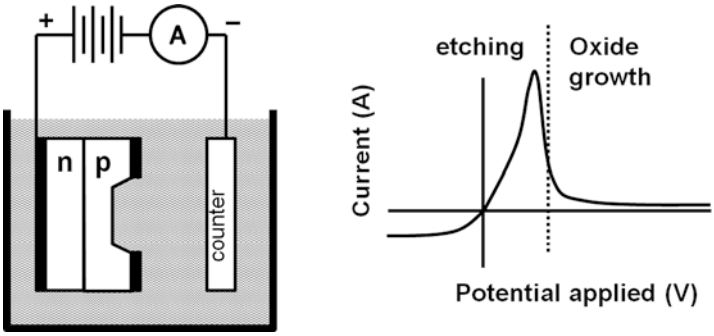

Fig. 10.15 Schematic of electrochemical etch stop process. A p–n junction immersed in an alkaline solution is biased by an external voltage. At voltages lower than the peak current position, silicon etches in the solution, but at higher voltages an oxide is formed, passivating the silicon against further etching

and drive electrochemical reactions at the surface. Figure 10.15 shows a schematic current–voltage response of silicon immersed in the etch solution, with etching occurring below a certain critical voltage, and oxidation of the surface occurring above that voltage. The critical voltage is found where the current flow through the cell reaches a maximum. Above that voltage, rapid oxidation of the silicon surface forms an insulating layer on the silicon, preventing any further etching from occurring.

In the case of a p−n junction as shown, a bias can be applied such that the n-type silicon is above the critical passivation voltage, but the voltage drop across the reverse-biased p−n junction will result in the p-type material having a potential low enough for etching to still occur. Thus, by operating very close to the critical voltage, the p-type silicon can be etched by the solution, whereas any n-type silicon that becomes exposed will form a passivating oxide, preventing further etch [30].

The electrochemical etch stop is typically utilized in the case of a p-type wafer with an n-type epilayer or lightly doped layer on the surface, which is intended to become a released thin membrane or other mechanical structure. Electronic components with other doping levels can be embedded in the lightly doped n-layer at the wafer surface, as long as there is continuous buried n-type layer surrounding them. The doping level of the n-type layer is moderate, typically 10^{15} cm^{-3} or higher, whereas the p-type layer is more heavily doped. By applying a potential to the wafer, it is possible to alter the Schottky barrier height of the n and p regions of the wafer, controlling charge injection and thus the rate of oxidation of the silicon surface, which is required for the etch process. By proper selection of etch conditions and applied bias, it is possible to suppress the etch rate of the n-type material while still maintaining etch conditions on the p-type material. The p-type silicon will undergo the usual oxidation/etch process observed for silicon in anisotropic etchants, until the p−n boundary is reached, at which point the etch will stop. This phenomenon allows excellent control over the etch stop condition, at the cost of significant complications in fixturing the wafer for etching [12].

The primary difficulty is in forming a good ohmic contact to the n-type layer on the surface of the wafer, and in protecting the wafer top surface and edges from etchant attack while the p-type region at the back of the wafer is being etched away. Various wafer fixturing systems made of Teflon and other polymers are available commercially (e.g., see Advanced Micromachining Tools GmbH, Frankenthal, Germany) to overcome this difficulty, and materials such as black wax (e.g., Apiezon Wax W, M&I Materials, Manchester, UK) can be utilized effectively to protect wafer surfaces as well.

In addition to the anisotropic etch processes described here, electrochemical techniques have been utilized to implement many isotropic "porous silicon" etch processes using hydrofluoric acid as the oxidation/etch medium [33, 34]. Silicon is etched by striking a balance between formation and removal of an oxide layer at the surface. This process is delicately controlled by the doping level and electrical bias in substantially the same manner as the anisotropic etches. Some workers have used illumination of the wafer to add yet another control mechanism to the etch stop process [35, 36]. By illuminating the p−n junction under bias, charge may be injected photoelectrically to drive the oxidation/etch reaction. Low doping levels are possible using this technique, although the problems in fixturing the wafer remain the same.

10.2.3 Materials and Process Selection Guidelines: Etch Stop Techniques

Boron etch stop	
Applicability	Useful for thinning silicon wafers and producing thin unsupported diaphragms. Can also be used to produce cantilevers, beams, and other structures in silicon. Thickness of a diaphragm or final structure geometry can be controlled to high accuracy by placement of boron dopant.
Implementation	Generate a region of very high boron doping corresponding to the area to be protected. The required doping levels are $5 \times 10^{19} - 1 \times 10^{20}$ boron atoms/cm^{-3}. Higher dopant densities are most effective in producing an etch stop. Diffusion times can be substantial, doping a 10 μm thick layer to 1×10^{20} cm^{-3} boron with solid or gas phase diffusion requires approximately 10 h at 1100°C in an inert atmosphere.
	Boron layer is implemented as the top surface of a wafer, and etching proceeds from the back. The boron-doped layer can be subsequently covered with an epitaxial silicon layer to provide a lightly doped region for electronic fabrication.
	Wet etches are performed in a heated reflux condenser type bath. Agitation may be added with a mechanical stirrer or N_2 bubbler, often required to prevent solution stratification and suppress surface roughness originating from H_2 bubbles on the surface.
Thermal budget	Activation of boron-doped region will generally require anneal or diffusion temperatures >900°C. Etch stop layer can be fabricated prior to other structures requiring lower temperatures, and etch/release can be the last processing step to avoid issues in processing thinned wafers and released structures.

Viable etchants	***KOH***: 10–60 wt% at 40–100°C are common depending on desired etch rate and surface roughness. In general higher KOH concentrations produce smoother etched surfaces with lower etch rates (e.g., etch rate 140 μm/h for 25 wt% KOH versus 80 μm/min for 60 wt% KOH [21]. Some workers add up to 20% by volume of isopropyl alcohol to improve surface roughness and anisotropy [37]. Author's lab uses 22 wt% KOH at 95°C for routine work on Si(100) with 190 μm/h etch rates and nearly mirror-smooth etch facets. It is a good idea to "condition" the KOH bath by dissolving some silicon chips or etching partway through a wafer to stabilize the etch rate, as fresh etch solution can have anomalously high etch rates for a short time. *Caution*: Hot KOH is very corrosive and can cause severe skin burns. ***EDP***: Many variations are possible. Some literature recipes include: EDP type S: 1 liter ethylenediamine, 133 ml water, 160 g pyrocatechol, 6 g pyrazine. 50–119°C, etches 45 μm/h at 115°C [38]. EDP type F: 1 liter ethylenediamine, 320 ml water, 320 g pyrocatechol, 6 g pyrazine, 50–119°C, etches 45 μm/h at 115°C [38]. EDP type B: 1 liter ethylenediamine, 320 ml water, 160 g pyrocatechol, 118°C, etches 50 μm/h [39]. EDP type T: 1 liter ethylenediamine, 470 ml water, 176 g pyrocatechol, etches 32 μm/h at 110°C [19]. These etches tend to be sensitive to oxygen contamination and a substantial decrease in the etch rate is observed as the solution "ages" in air. Use of an inert gas purge is recommended. *Caution*: This solution is quite corrosive and also toxic, so it should never be used without excellent containment and ventilation. ***TMAH***: TMAH is extensively used in the microelectronics industry as a photoresist developer. Solutions of 2–50 wt% TMAH in water are reported [20, 40] with typical operating temperatures of 70–90°C. Etch rate is reduced at higher concentrations, but surface roughness obtained during etch is decreased. Etch rates of 60 μm/h are obtained for 20 wt% TMAH in water at 90°C [40]. *Caution*: Solution is corrosive, but this is probably the safest to handle of the common anisotropic alkali etches.
Selectivity	***KOH***: selectivities of 10–100 between boron-doped and undoped regions can be obtained. Lower KOH concentrations result in higher selectivity [21] at the cost of increased etch surface roughness [37]. ***EDP***: As with KOH, selectivities of 10–100 between boron-doped and undoped regions can be obtained. Slightly higher selectivity as a function of doping is obtained at lower etch temperatures, down to 66°C or less [28]. ***TMAH***: Selectivities of 10 or better can be obtained, but higher boron concentrations are required than for KOH and EDP [29].
Material compatibility	***KOH***: Etches are most compatible with Si_3N_4 masks deposited by CVD processes. PECVD Si_3N_4 can be used if necessary but typically has inferior etch resistance. SiO_2 sometimes used as a mask for short etches but it is eroded at 10–50 Å/min depending on etch conditions. Teflon and occasionally stainless steel are normally used for wafer fixturing. Potassium contamination is incompatible with microelectronics, requiring a 1:1:1 $H_2O/HCl/H_2O_2$ decontamination etch before further processing. *Caution*: Solution is exothermic when mixed and should be used hot.

EDP: Etches are most compatible with Si_3N_4 masks deposited by CVD processes. SiO_2 sometimes used as a mask for moderate etches but it is eroded at 1–10 Å/min. Some metals including Ta, Au, Cr, Ag, and Cu can be used as masks [12]. Decontamination etch (as with KOH) is recommended before further processing to avoid tool contamination.

TMAH: SiO_2 and Si_3N_4 are both excellent masks for TMAH etch, with selectivity >1000. Most metals are compatible. Some authors have demonstrated compatibility with aluminum as well by doping the solution with silicon or polysilicic acid [41].

Isotropic doping-dependent etch stop

Applicability	Useful for etching channels and pits, or releasing membranes, cantilevers, and other structures fabricated over heavily doped silicon.
Implementation	Create a region of heavily doped $>10^{17}$ cm^{-3} silicon surrounded by lighter-doped material. The proper etchant solution will attack the heavily doped material without etching the more lightly doped material. Agitation of the solution is required for most reproducible results, but the solution may be used at room temperature.
Thermal budget	Activation of doped regions will generally require anneal or diffusion temperatures >900°C. Temperature-sensitive components can be fabricated on the wafer once the dopants have been activated, but are likely to be attacked by the HNA solution if not protected by a robust passivation layer.
Selectivity	Selectivity of 10–100 between heavily doped and lightly doped Si are reported [41, 42].
Viable etchants	Solutions of 250 ml HF, 500 ml HNO_3, and 800 ml acetic acid at room temperature obtain etch rates of 4–20 μm/min [22] at room temperature, and show selectivity to dopant density. Unfortunately these solutions are notoriously difficult to use reproducibly. Small variations in surface roughness or defect density, solution contamination, degree of agitation, and illumination can generate radically different etching behavior [23]. *Caution*: Solution is a strong oxidizer and the HF is corrosive and toxic.
Material compatibility	Silicon nitride films are best for masking, but silicon dioxide is usable for short etches (etch rate 30–70 nm/min). Polymers work for very short etches (e.g., 0.5 μm) but should generally be avoided as the solution is a strong oxidizer.

Electrochemical etch stop

Applicability	Useful for thinning silicon wafers and producing thin unsupported diaphragms. Can also be used to produce cantilevers, beams, and other structures in silicon. Thickness of a diaphragm or final structure geometry can be controlled to high accuracy by placement of a p−n junction and proper electrochemical biasing conditions.
Implementation	Any of the alkaline etches described for the boron etch stop technique may be used. A p-type region in contact with the etch solution, and an n-type region buried below it, is required for the etch stop technique to function. An electrical contact must be fabricated on the n-type region to apply the electrochemical bias. Other areas of the wafer, specifically the topside not being etched, must be protected from the alkaline solution. Black wax (Apiezon W) is often utilized, and sample fixturing can be designed or purchased from commercial vendors. Fixturing approaches can be problematic, as o-rings used to seal the fixture from etchant apply significant force to the wafer, often leading to breakage as the wafer is thinned by the etch.

Thermal budget	Activation of doped regions will generally require anneal or diffusion temperatures >900°C. Temperature-sensitive components can be fabricated on the wafer once the dopants have been activated, but will need to be protected from the etch solution by passivation layers or fixturing.
Selectivity	Selectivity between n and p silicon-doped regions is reported at 200:1 in KOH [43] and as high as 3000:1 in EDP [31].
Viable etchants	KOH, EDP, and TMAH all exhibit this effect.
Material compatibility	Same general materials requirements as the underlying KOH, EDP, and TMAH etch solution. Good electrical contacts must be made to the n-doped layer, and these contacts must be protected from the etchant.

10.3 In Situ Doping

One of the most effective methods of doping a semiconductor material is during the growth of that material. Incorporation of dopant atoms during the high-temperature growth phase results in an undamaged crystal structure with activated dopants, avoiding the need for subsequent annealing processes and large thermal budgets. Unfortunately, only bulk material or blanket films can be easily formed in this manner, so complex device structures will generally require some additional processing technique.

10.3.1 Chemical Vapor Deposition

Polysilicon is a polycrystalline form of silicon commonly used as a thin-film mechanical material in MEMS and as an electronic gate for MOS electronic devices. Polysilicon is straightforward to deposit on a wafer surface with chemical vapor deposition techniques, and is easily etched with a variety of wet chemical and dry plasma processes. It is compatible with high temperatures, thermally matched to the underlying silicon wafer, and can be doped to achieve a wide range of conductivity values.

As stated above, polysilicon is typically deposited using a chemical vapor deposition process in a low-pressure three-zone tube furnace, although the process is also compatible with single-wafer deposition equipment such as used in cluster tools. A common arrangement is illustrated in Fig. 10.16. Wafers stored vertically in a carrier are centered in a three-zone quartz hot wall furnace that is evacuated with a vacuum pump. A throttle valve controlled by a pressure sensor is normally placed at the output port to allow continuous closed loop control of the process pressure. Reactants are introduced at the front of the tube. Silane (SiH_4) is the most common reactant gas, but dichlorosilane (SiH_2Cl_2) and silicon tetrachloride ($SiCl_4$) are occasionally used as well. At the wafer surface, silane is broken down to produce elemental silicon and hydrogen gas.

Minor process details, such as reactor vacuum integrity, carbon and oxygen contamination, and wafer fixturing details can produce significant variations in

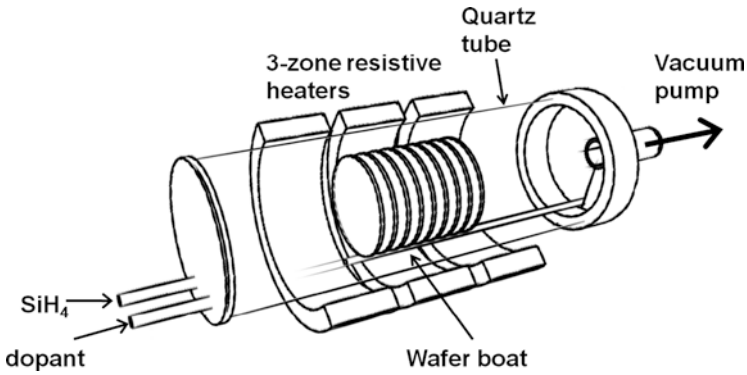

Fig. 10.16 Schematic of low-pressure chemical vapor deposition system

deposition rate and morphology [7], making quantitative comparison of literature results difficult. A typical undoped polysilicon process recipe used in the author's laboratory uses a deposition temperature of 650°C, with 100 sccm SiH_4 flow at 300 mTorr total pressure, which produces deposition rates of 110 Å/min. Thickness uniformities for a 5000 Å film of <5% within wafer and 10% along the length of the boat are typical. Three to four sacrificial "dummy" wafers are placed at the front and back of the boat to improve the thickness uniformity of the device wafers.

A small temperature gradient of 10–15°C is generally added to each zone, with the coolest zone closest to the gas inlet, and the hottest zone closest to the exhaust port. The increase in reaction rate at higher temperatures along the wafer load helps compensate for the reduction in SiH_4 partial pressure at the wafer surface as reactant is consumed. Increasing silane gas flow or pressure will increase the deposition rate to some degree, but altering these parameters will also modify the uniformity within the boat and within each wafer, so it is usually necessary to optimize temperature, pressure, and gas flow simultaneously to produce a viable process in each individual reactor.

Polysilicon film morphology and deposition rate depend strongly on deposition temperature, with deposition temperatures below 575°C producing fine-grained or amorphous films and low deposition rates. Deposition temperatures above 625°C produce large column-shaped crystallites [44]. Intermediate temperatures produce small microcrystallites or amorphous films, depending on reactor configuration, impurities, and other details. Figure 10.17 illustrates the typical morphologies observed in most reactors, with the transition between amorphous low-temperature depositions and columnar crystallite depositions occurring gradually somewhere between 525 and 625°C.

As long as sufficient silane is delivered to the process, deposition rates follow an Arrhenius relationship with an activation energy of about 1.7 eV [7]. The process is then driven by the reaction rate at the wafer surface rather than by mass transport effects, and good thickness uniformity can be maintained over all wafers.

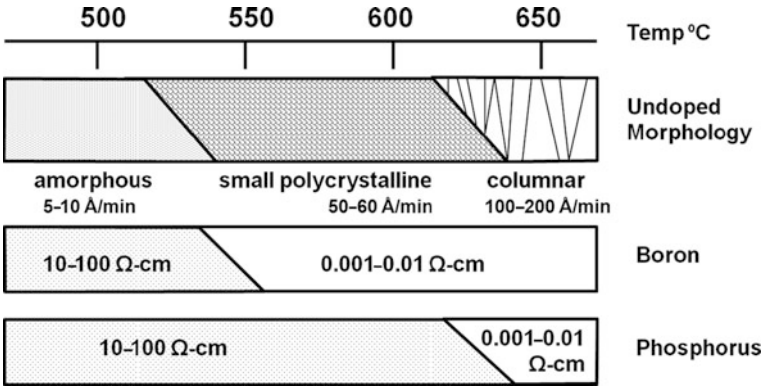

Fig. 10.17 Polysilicon undoped morphology and in situ doping resistivity trends as a function of deposition temperature. Minimum resistivities generally observed for high doping densities are listed for in situ boron and phosphorus-doped films

Lower silane flows result in the deposition process being governed by mass transport rates, and deposition rate, uniformity, and morphology then tend to be much more sensitive to reactor geometry details.

By adding a suitable source gas to the input reactant stream during chemical vapor deposition, it is practical to dope the polysilicon grains during growth. Phosphorus oxychloride ($POCl_3$) is a liquid material that can be added to the reactor using an inert gas bubbler or vapor draw system, and is used as a phosphorus dopant in CVD systems. Diborane (B_2H_6), arsine (AsH_3), and phosphine (PH_3) are gaseous materials that can be added to the reactor to provide boron, arsenic, and phosphorus dopants, respectively. Typical dopant flows are no more than a few percent of the silane flow, and using a dilute (e.g., 2% PH_3 in N_2) source gas is not uncommon for safety reasons [45].

It should be noted that every one of these materials (SiH_4, $POCl_3$, B_2H_6, AsH_3, and PH_3) is significantly hazardous, with SiH_4 being pyrophoric, $POCl_3$ being corrosive, and the rest being very toxic. Safety equipment including gas detectors and waste scrubbers are critical for these processes. Most workers use in situ doped polysilicon processes when a heavily doped polysilicon film is desired, such as that used for comb drives, local interconnect, gates, and other electrostatic devices. Resistance control of in situ doped material for lighter-doping levels tends to be poor between wafers and from run to run, often making simpler diffusion or ion implant processes more attractive for these applications.

At low doping levels, dopants tend to segregate to the grain boundaries between crystallites, producing little effect on the conductivity of the polycrystalline film. Resistivity of polysilicon at low dopant levels is then very sensitive to the exact morphology of the film. Dopants added to amorphous films collect at the large numbers of grain boundaries between the numerous small crystallites, where they are relatively ineffective compared to the same dopant density added to more crystalline films grown at higher temperature, where more of the dopant is incorporated in the

crystallites themselves. This leads to a relatively abrupt decrease in the resistivity observed for a polysilicon film saturated by dopants as the morphology of the film goes from amorphous to columnar crystalline at increased deposition temperatures.

Addition of phosphorus (PH_3) dopant during the polysilicon deposition process has the effect of suppressing large crystallite growth until higher temperatures are achieved relative to an undoped deposition, as illustrated schematically in Fig. 10.17. The minimum resistivity achievable tends to be in the range 10–100 Ω cm below about 625°C, which corresponds to the range where amorphous deposition occurs. At temperatures higher than about 625°C, the columnar growth mode predominates, and the minimum resistivity obtainable drops to about 0.001–0.01 Ω cm. Total deposition rates of polysilicon grown with phosphine and arsine dopant gases are strongly suppressed [7, 46], with up to an order of magnitude decrease in deposition rate observed with dopant flows of more than a few percent of the silane flow.

Addition of boron (B_2H_6) dopant during the polysilicon deposition process increases the deposition rate of polysilicon by as much as two to three times [46], with little effect on the overall morphology. Low-resistivity polysilicon with large microcrystallites can be obtained at temperatures as low as 525–550°C.

10.3.2 Crystal Growth and Epitaxy

Conventional crystal growth techniques are used to produce boules and wafers of a given desired dopant concentration. A wide range of dopant concentrations is possible but only bulk material can be produced. Much of the silicon produced in the world today is grown by the Czochralski technique illustrated in Fig. 10.18 [47, 48]. A quartz crucible containing very high-purity polysilicon and dopant materials such as antimony or phosphorus is heated by a set of electric heaters until it is above the melting point of silicon at 1414°C. A small single-crystal seed of silicon is lowered into the melt on a support rod, and then slowly withdrawn. The crystal orientation of the boule can be selected by proper orientation of the seed crystal.

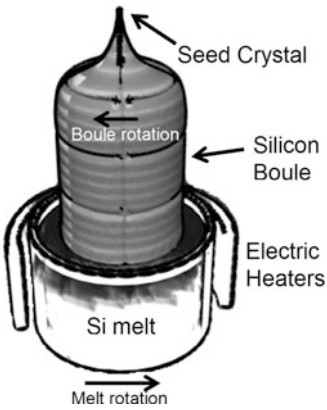

Fig. 10.18 Czochralski silicon crystal growth method

New silicon grows on the seed from the melt, using the seed crystal structure as a template, and cools as the boule is withdrawn. The crucible and the growing boule of single-crystal silicon are continuously rotated in opposite directions as the crystal is drawn. The entire apparatus is housed in an inert gas environment during the process, which takes many hours depending on the size of the crystal boule being grown.

This growth technique produces silicon of a doping level set by the amount of dopant material included in the original melt. Oxygen, from crucible quartz dissolved into the melt by the molten silicon, and carbon, from sublimation of the carbon heater elements used to heat the melt, are incorporated in the boule during growth [48], with typical levels $>10^{17}$ cm^{-3} for oxygen and $>10^{15}$ cm^{-3} for carbon. These impurities are often beneficial in trapping and immobilizing trace metallic impurities, but can also cause problems for some devices. For example, oxygen precipitates in silicon used for anisotropic KOH etching can induce small pitting defects that degrade the mirror finish of etch facets.

An alternative popular silicon crystal growth method is the float-zone technique schematically illustrated in Fig. 10.19. This method avoids use of a crucible or other container that can introduce contaminants into the boule. A large polysilicon rod is lowered gradually through a zone heated inductively by radio frequency energy. A seed crystal at the lower end provides the template for single-crystal growth of the larger boule. Silicon is melted by the RF power, and surface tension of the liquid allows it to flow down through the hot zone and recrystallize on the seed crystal. Impurities in the initial polysilicon rod tend to stay segregated in the liquid zone rather than incorporate in the growing single-crystal zone, so boules of extremely high purity can be grown this way. Dopants may be introduced by incorporating them in the original polysilicon rod, exposing the hot zone to a flow of suitable dopant gas such as phosphine or diborane, or even by feeding a rod of dopant material into the molten zone and letting it melt [49]. Silicon with resistivities exceeding

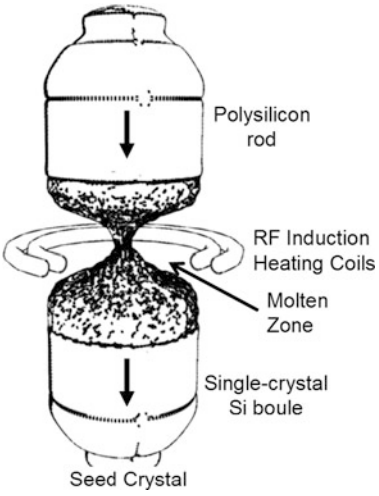

Fig. 10.19 Silicon single-crystal growth by the float-zone technique

10^4 Ω-cm can be grown by this method for special applications such as radio frequency integrated circuits, which require very low substrate conductivities.

Single-crystal epitaxial films of silicon or other semiconductors are often grown on wafers that have been prepared by bulk silicon growth techniques such as the Czochralski or float-zone techniques. Unlike the polycrystalline or amorphous materials grown with simple polysilicon deposition methods, these epitaxial growth techniques replicate the crystal structure of the underlying wafer, producing a thin layer of single-crystal material with optimized properties. Epitaxial techniques are widely used to grow semiconductor layers with specific dopant levels, stacks of layers with different composition or dopant levels (multilayers), and atomically abrupt junctions not obtainable with ex situ doping techniques. Alloys such as SiGe and compound semiconductors can be grown on substrates with the proper lattice structure using heteroepitaxial growth methods.

A variety of epitaxial growth techniques exists such as liquid phase epitaxy, vapor phase epitaxy (VPE), molecular beam epitaxy (MBE), atomic layer epitaxy (ALE), and metal–organic vapor phase epitaxy (MOCVD or OMVPE). Most techniques operate by heating a substrate to a large fraction of its melting temperature and exposing it to a flow of reactants. High substrate temperatures allow for a high mobility of adatoms on the surface, allowing deposited materials to conform to the underlying crystal structure.

Vapor phase and metal–organic vapor phase epitaxial reactors are probably the most common systems used for producing commercial quantities of material, as these systems can achieve a fairly high throughput. See Fig. 10.20. Substrates may be heated by simple electrical heating elements, optical, or radio frequency energy, and the chamber walls are generally cooled ("cold wall" reactor), which minimizes deposition on the walls. Horizontal and vertical configurations exist, with some reactors accepting one wafer at a time, and others handling multiple wafers. Subatmospheric pressure processes are typical, but full atmospheric pressure processes are not unknown.

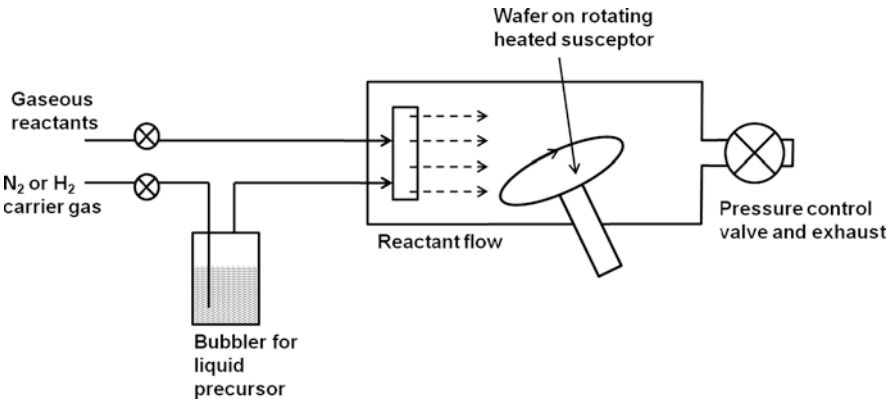

Fig. 10.20 Metal–organic vapor phase epitaxy (MOCVD) system schematic

A common configuration in the microelectronics industry is the silicon epitaxial reactor, which flows hydrogen and silane, dichlorosilane, or silicon tetrachloride over multiple wafers at temperatures above 900°C. Deposition kinetics is a complex interaction between deposition of Si and etching from the Cl species in the gas stream. Dopants may be introduced by adding phosphine or other dopant gases. This produces a high-quality single-crystal film at deposition rates that can approach 1 μm/min. This type of reactor would be used to place a low doping density silicon epilayer over a heavily doped boron etch stop layer, for example, to allow subsequent fabrication of transistors or other active devices on top of a released diaphragm.

III-V epilayers for optoelectronic devices are commonly grown using liquid precursor materials delivered by bubbling hydrogen through a heated fluid bath. Vapor is entrained in the gas flow and delivered to the reactor. Examples of common liquid precursors for GaAs epitaxy include trimethylgallium ($Ga(CH_3)_3$) and tertiary butyl arsine $AsH_2(t\text{-}C_4H_9)$, but a vast array of chemicals exists for aluminum, gallium, arsenic, phosphorus, and boron sources for MOCVD growth. II-VI materials such as $Hg_{1-x}Cd_xTe$, used in infrared detector devices, can also be profitably grown using MOCVD epitaxy techniques.

Molecular beam epitaxy (MBE) is a high vacuum deposition technique that grows an epilayer on a substrate by exposing it to an atomic or molecular beam of reactant. See Fig. 10.21. For example, elemental Si is used for deposition of Si epilayers, and Al, Ga, and As are used to deposit $Al_{1-x}Ga_xAs$ alloy semiconductor epilayers. Beams of dopant atoms can also be added to the flux of material impinging on the substrate, allowing very precise control of dopant level and alloy composition. Beams of solid-source material are generated by temperature-controlled collimated evaporation cells ("effusion" or "Knudsen" cells) equipped

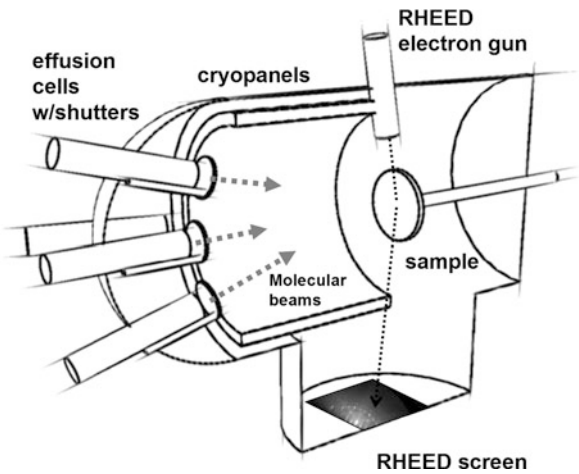

Fig. 10.21 Molecular beam epitaxy (MBE) system

with shutters to start and stop the molecular beam, and liquid and gaseous species are introduced by special cracking cells or gas injectors.

Deposition rates are generally low, on the order of 1 μm/h or less. The vacuum system is maintained at a low pressure (10^{-7}–10^{-11} torr) ensuring that chemical reactions only occur at the substrate when the beams impinge on it, and to prevent contaminants from being included in the growing film. Large vacuum pumps and liquid nitrogen cooled cryoshrouds help maintain low pressure and adsorb stray gas molecules before they can be incorporated in the epilayer. Most MBE systems can only deposit an epilayer on a single substrate at a time. This, coupled with the low deposition rate, makes the MBE growth technique less popular for production of commercial quantities of epitaxial material, but they are capable of producing very precise structures with material composition and doping density modulated at the monolayer level, which is often not practical with MOCVD or other high-throughput techniques.

For example, "delta doping" (Fig. 10.22) is a technique used to produce an extremely abrupt layer of dopants with very high dopant levels [50] that can actually exceed the solid solubility limits in bulk material. The dopants are confined to a narrow region of material, often as thin as a single atomic layer in the crystal. This thin dopant layer alters the electronic structure of the semiconductor, forming a narrow, deep quantum well in the conduction band that can trap electrons in the form of a highly mobile two-dimensional "electron gas." If the well is sufficiently deep and narrow, a set of electronic subbands is also formed which have unique optical and electronic properties. High-performance transistors can be fabricated by this approach which takes advantage of the high mobile charge density in the conduction channel and resonant tunneling effects. Optical devices such as lasers and detectors are also made possible by transitions between the well subbands.

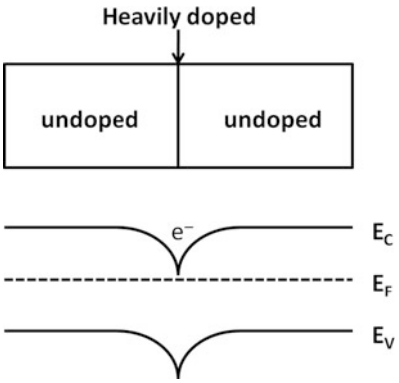

Fig. 10.22 Delta doping concept. A layer of very heavy dopant density is grown between two layers of much lighter dopant density. Conduction and valence bands form a potential well that can confine electrons in a two-dimensional layer

10.4 Diffusion

Diffusion processes to fully dope a thin-film or produce a desired dopant profile are common in the semiconductor and MEMS fields. These processes rely on

straightforward thermal diffusion of dopant species from areas of high concentration to areas of low concentration at high temperature, usually >900°C in silicon materials.

Diffusion of dopants in Si and other materials can be described by Fick's law of diffusion [50], where the concentration of dopant at time t and depth x below a surface is usually expressed in simplified form as

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2}, \tag{10.2}$$

where D (in cm^2/s) is the diffusivity of the dopant species in Si at a specified temperature. More advanced models incorporate the fact that this diffusivity is actually a function of dopant concentration and is affected by other factors such as oxidizing or nitridizing ambient environments in the diffusion tube, but for reasonably low concentrations and inert environments it can be regarded as a constant.

In the simplest possible model, diffusivity varies with temperature according to an Arrhenius relationship,

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right), \tag{10.3}$$

where D_0 is the frequency factor and E_a the activation energy for diffusion. More complex models for D_0 incorporate corrections for concentration, crystal damage, oxidation, and other factors [52, 53]. Values for D_0 and E_a for a few typical silicon dopants in single-crystal silicon are given in Table 10.1. Diffusivity will depend on the concentration of interstitials, vacancies, grain boundaries, and other defects in the crystal [54, 55], so it is clear that polycrystalline material will have a significantly higher diffusivity than single-crystal materials.

Table 10.1 illustrates that the diffusion constant for As in polysilicon is more than 10^3 higher than in single-crystal silicon even at relatively low temperatures. Diffusion through polysilicon films is strongly influenced by the morphology of the film, but because the diffusivities are high and the film thicknesses are low, in practice even a short anneal will evenly distribute any dopant evenly throughout the thickness of the film. Lateral diffusion of a micron or more can be expected with polysilicon even during short high-temperature anneals.

Table 10.1 Frequency factor D_0 and activation energy E_a for calculating diffusion constants as a function of temperature (Kelvin) for common dopants in Si. Values for single crystal (c-Si) and polysilicon (poly) are listed

Dopant	D_0 (cm^2/s)	E_a (eV)	Ref
B (c-Si)	2.64	3.6	900–1200°C [Mathiot]
As (c-Si)	35.3	4.11	950–1150°C [Ishikawa]
P (c-Si)	3.62	3.61	950–1150°C [Ishikawa]
As (poly)	8.6×10^4	3.9	800°C [Swaminathan]

Two solutions for Equation (10.2) are broadly useful, corresponding to the case of (1) constant dopant concentration, and (2) fixed total dopant quantity. Case 1 is commonly encountered in gas and solid-state diffusion processes where the dopant is continuously introduced during the process or is available from a large reservoir, so the dopant is never depleted by the quantity that diffuses into the silicon surface. The solution that satisfies (Equation (10.2)) under these conditions is

$$C(x,t) = C_S \mathrm{erfc}\left(\frac{x}{2\sqrt{Dt}}\right), \tag{10.4}$$

where x is the depth below the silicon surface in cm, C_S is the fixed dopant concentration in the ambient (atoms/cm^{-3}), D is the diffusivity from Equation (10.3), and t is the amount of time that the sample is held at the diffusion temperature in seconds. The erfc is the complementary error function, which is tabulated in many reference works [56] and is even a native function supported in spreadsheet applications such as Microsoft Excel©.

The second case is appropriate for instances where the total amount of dopant at the start of the diffusion process is fixed at some value and not replenished as it is consumed by diffusion into the silicon. This is common for materials such as spin-on dopants or deposited glass thin-film dopants, which have a finite amount of dopant in a small reservoir. The solution to Equation (10.2) under this set of conditions is then given as

$$C(x,t) = \frac{Q_T}{\sqrt{\pi Dt}} \exp\left(-\frac{x^2}{4Dt}\right), \tag{10.5}$$

where Q_T is the total quantity of dopant at the beginning of the anneal at the surface in atoms/cm^2.

10.4.1 Gas Phase Diffusion

Gas phase diffusion processes were widely used at the beginning of semiconductor technology, but tend to be less popular now simply due to the toxic gases required. Dopant atoms are introduced by flowing a suitable gas such as phosphine, diborane, $POCl_3$, or BCL_3 into a furnace that maintains the substrates at a temperature sufficient to produce indiffusion. See Fig. 10.23. The constant gas flow sets a constant dopant concentration in the tube ambient, providing appropriate conditions for the application of Equation (10.4). A burn box or scrubber of some type is required for dealing with the toxic effluent from the tube, and the furnace must be sealed or otherwise isolated from the laboratory environment to prevent even ppm levels of dopant gas from escaping. Nitrogen or argon is usually admitted to the furnace to provide an inert environment.

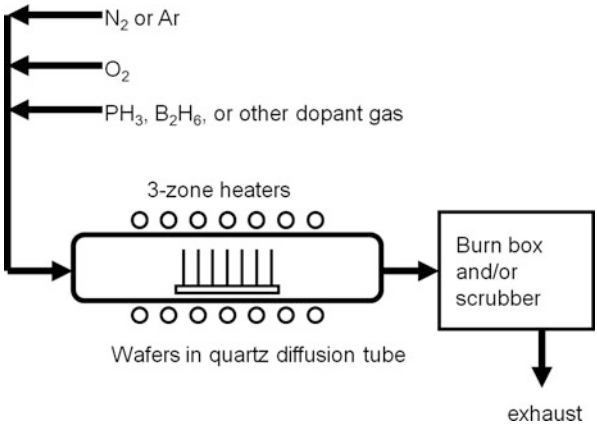

Fig. 10.23 Gas phase diffusion schematic. Process equipment is essentially a modified diffusion furnace with provision for introducing dopant gases and dealing with toxic effluents

10.4.2 Solid State Diffusion

Sources of dopant atoms can be also conveniently introduced by applying a thin film of material to the substrate to be doped. These thin films are often glass materials containing boron or phosphorus. Films of phosphorus- or boron-doped glass can be applied with LPCVD deposition equipment using a low-pressure silane and oxygen chemistry (at about 400°C and 300 mtorr) with a small amount of added PH_3 or B_2H_6. The dopant gas is often diluted in N_2, or even SiH_4, to avoid having to work with a 100% toxic gas cylinder under high pressure. Liquid dopants such as Trimethylphosphite ($P(OCH_3)_3$ and Trimethylborate ($B(OCH_3)_3$), available from Air Products corporation of Allentown, PA, have become popular low-toxicity substitutes for PH_3 or B_2H_6, respectively, and may be added to the SiO_2 deposition process by entraining dopant vapor with N_2 or He in a bubbler. Typical doping levels for boron- and phosphorus-doped glasses are 4–7 wt%, as higher levels of doping are hygroscopic and can be difficult to work with.

Spin-on liquid materials are a very convenient doping method requiring little process equipment and no toxic material storage [57]. These materials are available for Sb, As, P, and B doping from Honeywell Electronic Materials in Tempe, AZ, Emulsitone Corporation in Whippany, NJ, or Filmtronics Corporation in Butler, PA. A typical process used in the author's laboratory is illustrated in Fig. 10.24, where the liquid dopant is first spin-cast on a silicon wafer. Film thickness is generally not critical. Excess solvent is driven off by a 15 min bake on a hotplate at 200°C. The coated wafers are loaded into a diffusion tube in a N_2 ambient and a diffusion process is performed, with time and temperature selected to produce the desired doping profile. Finally, the dopant glass is removed with a 10:1 solution of hydrofluoric acid.

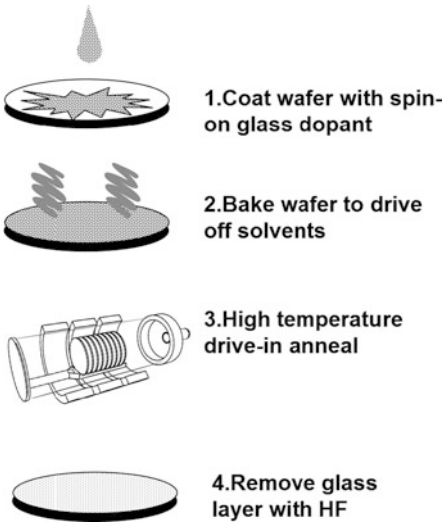

Fig. 10.24 Use of liquid spin-on dopant materials

Solid-source dopant materials are another convenient source of dopant that does not require toxic materials. Boron and phosphorus solid diffusion dopant sources are available from Saint-Gobain Ceramics in Amherst, NY. Donor wafers made of glass or silicon carbide saturated with boron or phosphorus-rich materials are added to a furnace wafer carrier with the silicon wafers to be doped as shown in Fig. 10.25. Silicon wafers are sandwiched between dopant source wafers and are used in a slightly oxidizing ambient at atmospheric pressure. At the high temperatures utilized for diffusion, dopants diffuse out of the solid sources and immerse the substrates in an ambient rich in dopant atoms, allowing indiffusion of dopant into the target substrate. A thin coating of borosilicate or phosphosilicate glass is left on the silicon surface after annealing which must be removed with hydrofluoric acid. Dopant wafers are usable for dozens of runs and are inert, nonflammable, and nontoxic.

An old but extremely effective method of producing metallurgical junctions for contacts and other heavily doped applications is the so-called alloy contact illustrated in Fig. 10.26, where an aluminum metal thin-film or small bead of material is placed in contact with the semiconductor to be doped and contacted. Annealing the contact above the Al–Si eutectic temperature at 577°C allows some metal to diffuse into the semiconductor, doping it p-type as indicated in Fig. 10.3. This forms a heavily doped p-type region immediately below the metal, producing a diode in n-type material (a), or an ohmic contact in p-type material (b). This technique also works with indium metal, although it can be trickier due to the low melting point of indium. Aluminum–antimony alloys can be used to form ohmic contacts to n-type material. This technique was used early in the development of microelectronics to produce diffused junctions for diodes and semiconductors, but was eventually replaced with more controllable processes such as gas and solid-state diffusion [7].

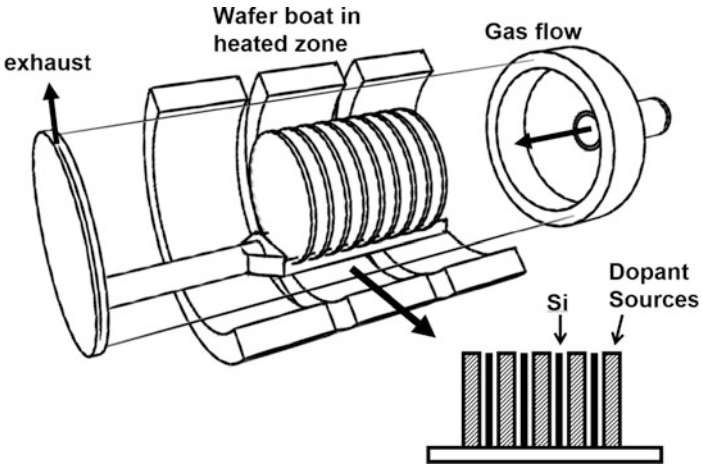

Fig. 10.25 Use of solid-source dopant wafers in diffusion tube

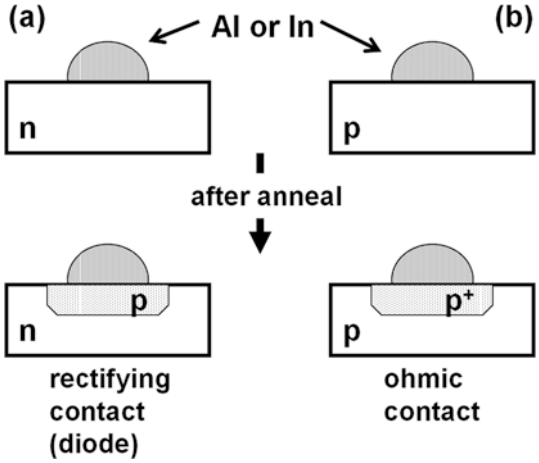

Fig. 10.26 Formation of metallurgical junctions for self-doped contacts. Al or In metal balls sintered on the surface of n-type silicon produce diodes, and on p-type silicon produce ohmic contacts

10.4.3 Masking Materials

Doping blanket films or the entire surface of silicon wafers is straightforward, but many devices require dopants to be placed in a specific area. This process requires a mask material that can withstand the high temperatures encountered during the diffusion process, which can run as high as 1250°C for a deep diffusion in a SiC furnace tube. The mask must also have a low diffusion coefficient for the dopant that is being introduced. In practice SiO_2 and Si_3N_4 films meet these requirements

[58], and are generally convenient to deposit in any laboratory performing silicon processing. Silicon nitride can be deposited with dichlorosilane and ammonia in a LPCVD furnace [51]. To make certain it adheres to the silicon wafer throughout the diffusion temperature cycle, it is advisable to put a thin (250–400 Å) thermally grown SiO_2 layer underneath. Openings in the nitride can be formed by standard lithographic techniques and plasma etching in CF_4 or SF_6. SiO_2 masks can be grown by thermal oxidation and subsequently patterned with HF or plasma etching, or they can be grown in specific areas by the LOCOS (local oxidation of silicon) process (which uses a nitride mask) [7, 59]. Nitride films of about 1500 Å thickness are typical, and oxide films from 2500 Å– 1.25 μm are common. See Fig. 10.27.

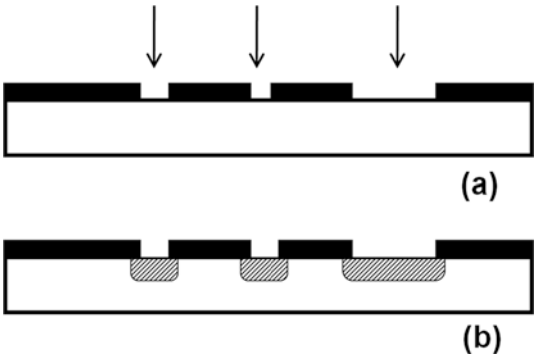

Fig. 10.27 Masking during diffusion. The mask material must have a very low diffusivity for the dopant species while being able to resist temperatures of 1100°C or more. SiO_2 and Si_3N_4 are common mask materials. Openings in the mask in (**a**) allow dopant atoms to diffuse into the silicon. Lateral diffusion under the mask results in diffused areas slightly larger than the openings in the mask as shown in (**b**)

10.4.4 Modeling

A variety of software packages is available to accurately model diffusion of dopant atoms in the solid state, many based upon the SUPREM series of simulation models developed at Stanford University. Code for one- and two-dimensional simulation is available from Stanford University directly [60] or incorporated into a variety of commercial software packages such as ATHENA by Silvaco Corporation. Modeling ultrashallow junctions for advanced CMOS devices requires the latest code to account for dopant clustering, transient diffusion enhancement, and other effects not incorporated in the simple Fick's law (Equations (10.3)–(10.5)). However, for MEMS applications, detailed modeling of dopant tails, transient diffusion and other second-order effects are often more than necessary, and simple one-dimensional analytical expressions are usually adequate to model the process required for doping a boron etch stop to produce a given silicon diaphragm thickness.

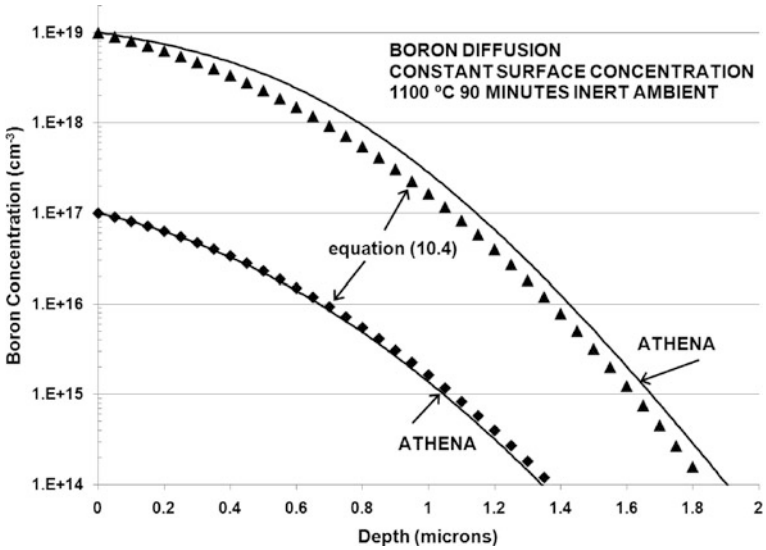

Fig. 10.28 Simulation of boron diffusion from a constant surface concentration of 1×10^{17} cm^{-3} and 1×10^{19} cm^{-3} at 1100°C for 90 min. *Solid lines* are simulations using ATHENA, and discrete markers are computed via Equation (10.4)

Figure 10.28 illustrates a comparison between an ATHENA simulation (solid lines) and calculations from Equation (10.4) for a 90 min, 1100°C boron diffusion with constant surface dopant concentrations of 10^{17} and 10^{19} cm^{-3}. Agreement is quite good and only departs at the highest doping densities, where concentration effects and electric fields induced by the high dopant concentration lead to higher effective diffusivities. Even these factors can be substantially accounted for by using diffusivities adjusted for concentration effects or ambient environments other than inert gases (e.g., oxidizing environments during diffusion). See data tabulated in Properties of Silicon (INSPEC, London, 1988). Brigham Young University at the time of this writing has an excellent set of simple online diffusion and implant profile calculation tools at their Electrical and Computer Engineering, which at the time of this writing is hosted at http://cleanroom.byu.edu.

10.5 Ion Implantation

Ion implantation is a process for doping semiconductor substrates using ballistic implantation of high-energy ions. It is more convenient than conventional high-temperature diffusion processes as it allows simple control of dopant density by altering implant current and time, and good control of the dopant profile by altering ion energy and thus implantation depth. A broader range of masking materials is possible as well, inasmuch as the mask does not have to withstand a high-temperature process, increasing convenience in patterning and mask removal.

Significant crystal damage occurs during the implantation process, which generally must be repaired by annealing processes to restore useful crystal structure and activate the dopant atoms.

A high-energy ion affecting a solid will undergo a number of electronic and physical collisions until it comes to rest. In general, heavy ions, such as arsenic, do not penetrate as far as light ions, such as boron. The interaction between incoming ions and the silicon lattice is composed of two components, nuclear and electronic. The nuclear interaction is essentially a physical collision between the incoming ion and a lattice atom, and scales with the atomic weight of the ion. The nuclear interaction also depends on energy, with a lower collision cross-section at high energies. The electronic interaction is an interaction between the incoming charged ion and the electronic structure of the solid. Motion of the ion through the solid produces a realignment of electrons in the solid, gradually draining kinetic energy from the ion as it passes. As the ion enters the solid, it loses energy from electronic interactions, increasing the effective nuclear cross-section of the ion. A nuclear collision will eventually occur, with the probability of that collision being maximized at some depth below the surface at which the nuclear collision cross-section is maximized by the electronic energy loss. Plots of the ion density deposited in a solid as a function of penetration depth will have a characteristic peak depending on ion energy and mass, with an approximately Gaussian profile around the peak position, as illustrated in Fig. 10.29 for 100 keV implants in silicon calculated using ATHENA and a simple Gaussian model.

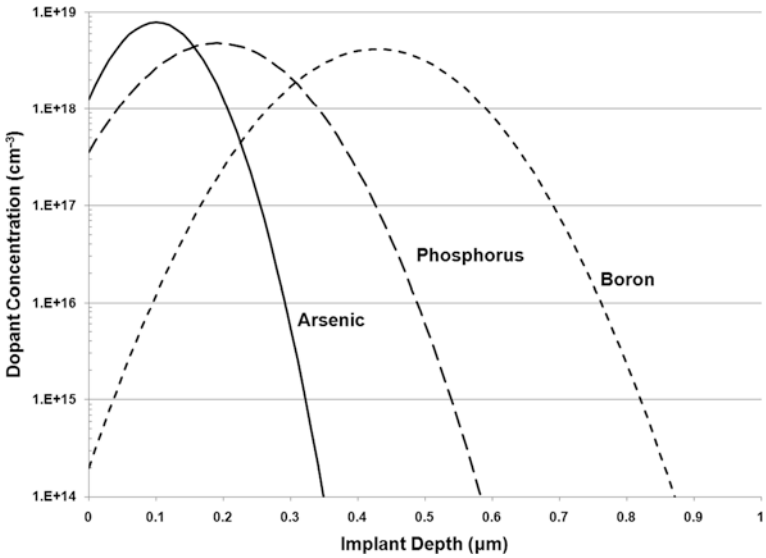

Fig. 10.29 Simulated dopant profile for ion-implanted boron, phosphorus, and arsenic at 100 keV and 1×10^{14} ions/cm^{-3}. Lighter ions penetrate more deeply into the silicon. Calculated using ATHENA

The depth of the Gaussian implant concentration peak and the width of the peak (standard deviation), called the longitudinal straggle, is determined by the relative electronic and nuclear scattering cross-sections for the ion and substrate atoms. These cross-sections are tabulated for many ions, and can be calculated to a high degree of accuracy using software tools such as SRIM (stopping range of ions in solids) [61]. SRIM calculations for ion range and longitudinal straggle are shown in Fig. 10.30 for boron, phosphorus, and arsenic implants in silicon up to 300 keV. These calculations may be used to estimate the position of the highest dopant concentration as well as the width of the implanted dopant distribution. The maximum dopant contribution of the implanted distribution is related to the total implanted dose by [59].

$$Q = \sqrt{2\pi}\,\Delta R_{\mathrm{P}} C_{\mathrm{P}}, \tag{10.6}$$

where Q is total dose implanted (atoms/cm^2), ΔR_{P} is the longitudinal straggle from SRIM or Fig. 10.30, and C_{P} is the peak concentration in atoms/cm^3.

These simple calculations allow estimates to be made for the proper energy and dose to provide a given implant profile, but more sophisticated calculations are best conducted using a simulation tool such as SUPREM IV [60] or ATHENA (Silvaco Corp, Santa Clara, CA). In particular, activation of dopants will broaden the implanted profile through diffusion, and ions implanted in a crystalline solid undergo processes such as channeling, which are not accounted for by SRIM and simple Gaussian profile calculations.

Unlike diffusion methods, which result in the highest dopant concentration at the surface in contact with the dopant source, ion implant processes can easily place the ion dose well below the substrate surface, enabling structures such as deep buried channels. Ions can also be implanted through overlying structures at sufficiently high energies. Ion implant offers unique process opportunities by decoupling dopant concentration (ion current) and dopant profile (ion energy), which is not possible with basic diffusion processes.

10.5.1 Equipment

Ion implantation is performed by a small particle accelerator that ionizes atoms from a solid or gaseous dopant source. To produce a beam of dopants, a suitable source material must first be vaporized and ionized. A simple ion source can be constructed by using a hot filament to ionize a gaseous feedstock containing dopant atoms. Historically, BF_3 gas is used to produce boron dopants, PH_3 is used for phosphorus implants, and AsH_3 is used for arsenic implants. Because many of these gas dopant materials are highly toxic, there is a trend toward safer delivery systems than high-pressure gas bottles, such as the subatmospheric Safe Delivery Source^{TM} systems pioneered by Advanced Technology Materials Corp. Solid materials can be utilized as source materials by direct thermal sublimation or vaporization in a more complex electric arc or inductively coupled plasma source.

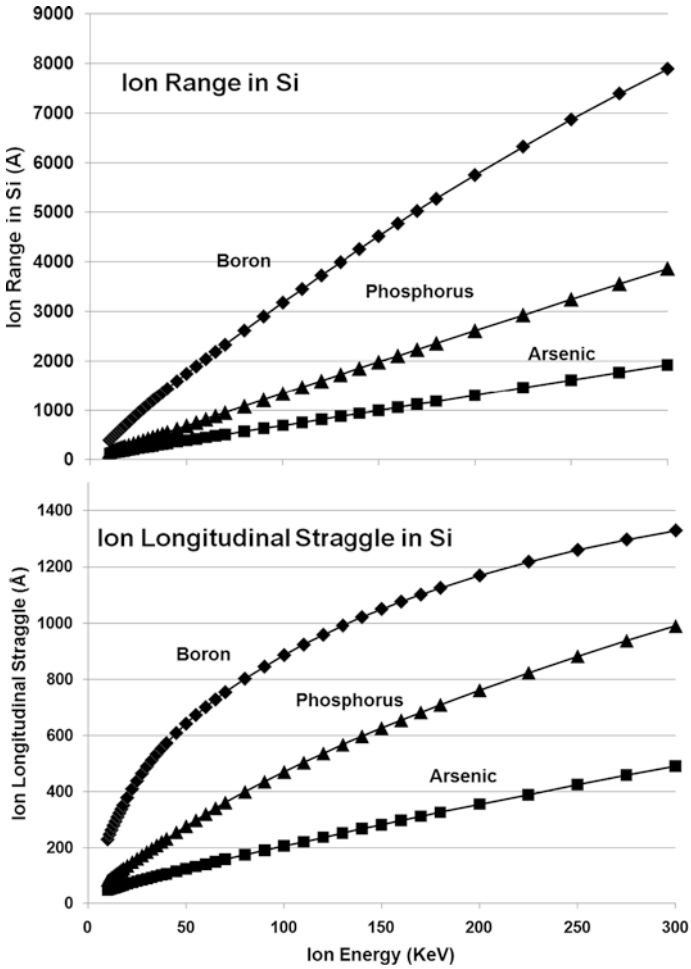

Fig. 10.30 Calculated ion range and longitudinal straggle, in angstroms, for boron, phosphorus, and arsenic ions in silicon. Calculated using SRIM [61]

Once a stream of ions is produced from a source, a mass selector extracts the desired dopant from the ionizer and accelerates the ions to the desired energy. Mass selectors may be conventional magnetic sectors as illustrated in Fig. 10.31 or quadrupole mass filters. Focusing optics produce a collimated beam that can be directed onto the substrates, and rastering electrostatic or magnetic optics scan the beam across the wafer surface. In high-current machines, the substrates themselves are mechanically scanned across the beam. At high beam currents an electron flood source is utilized to neutralize the surface charge produced by the ion bombardment, and a wafer cooling system may be used to prevent excessive temperature increase of the wafers and subsequent damage to masking materials.

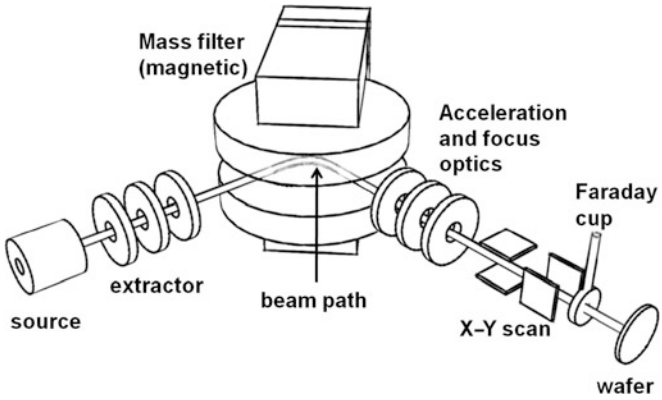

Fig. 10.31 Schematic of a medium-current ion implant system

Specialized implanters are available for specific tasks. Medium-current implanters operate well from about 5–200 keV ion energy, with currents up to a few milliamps. Individual substrates are typically held stationary, and the beam is electronically rastered over the surface by an $X-Y$ scanning system. Medium current machines are good for producing moderate implant doses (up to about ($>1 \times 10^{14} - 5 \times 10^{16}$ ions/cm^2) with high throughputs, suitable for such applications as channel stop and threshold adjust implants. Obviously, higher doses are obtainable by simply using longer exposures and accepting lower process throughput. High-current implanters are optimized for producing very large doses ($>1 \times 10^{14} - 5 \times 10^{16}$ ions/cm^2) for source/drain implants, polysilicon doping, and SOI wafer production. Typically high-current implanters mount a batch of wafers on a cooled rotating stage assembly. The ion beam is rastered in a linear or fan pattern rather than in two dimensions, and the stage is rotated and translated through the linear beam pattern to uniformly irradiate each wafer.

A third variation of the basic ion implanter technology is the low-energy implanter, optimized for producing ion beams at low energies, <10 keV. Conventional implanters have difficulty in obtaining high-current beams at the low energies useful for producing very shallow dopant profiles, so low-energy implanters have been developed with short beam paths and optics optimized for low-energy, high-current ion beams.

10.5.2 Masking Materials

A wide variety of masking materials are usable with ion-implant processes. Silicon dioxide, silicon nitride, polysilicon, and metals are sometimes used for implant masks, especially in "self-aligned" processes that place implanted species in silicon laterally adjacent to the edge of an overlying structure. Conventional photoresist is probably the most commonly used material as it is easy to apply, pattern, and

remove after the implant is complete, in contrast to the hard masking materials required for high-temperature diffusion processes. Resist damage or burning can be an issue with high-current implants, and aggressive removal methods with oxygen plasmas or sulfuric acid/peroxide stripping solutions are often required to strip the damaged polymer. Candidate materials for masks, or even complete stacks of dissimilar materials, can be easily simulated for ion stopping effectiveness using the SRIM [61] simulation software.

10.5.3 Modeling

Simple calculations of implanted profiles may be performed using software tools such as SRIM [61] or by estimating implant depths from tabulated cross-section values [61, 62]. For relatively coarse applications, such as generation of a heavily doped boron stop layer or production of a heavily doped polysilicon layer, these estimates will often suffice. However, thermal cycles must be included after implant as dopants will diffuse through the crystal during activation with conventional thermal methods. This can be approximated by Gaussian broadening the implanted profile via Equation (10.5), or by simply using a modeling tool such as SUPREM.

For more precise work including perturbations such as ion channeling, amorphous layers, or implant through oxides or other surface films, a 1-D or 2-D process simulator is indispensable. For example, Fig. 10.32 illustrates a high-dose boron implant of 1×10^{16} B11+ at 100 keV, before and after an anneal in an inert environment of 90 min at 1100°C. As-implanted, the boron profile has a significant shoulder at higher depths due to ions "channeling" through preferred directions in the crystal structure [63]. One such channel is shown in Fig. 10.33 through a silicon–diamond structure. At the correct angle, long "tunnels" extend through the crystal structure allowing ions to penetrate anomalously deep with little chance of scattering. The presence of this shoulder is not predicted by range calculations in Fig. 10.30, which would lead to predictions of the implanted profile being shallower and of higher concentration than it actually is. The channeling effect can be suppressed by implanting through a thin screening oxide and adding a small tilt to the substrate to prevent ions from entering at the channeling angle. Simulation codes based on SUPREM can simulate the channeling effect by using dual-Pearson implant profiles [64].

10.5.4 Crystal Damage

Ion scattering from a solid through electronic interactions produce relatively little damage to the crystal structure, but actual collisions between ion cores during nuclear interactions can cause severe crystal damage. These collisions are essentially elastic in nature, and sufficiently high-energy events can cause a cascade of

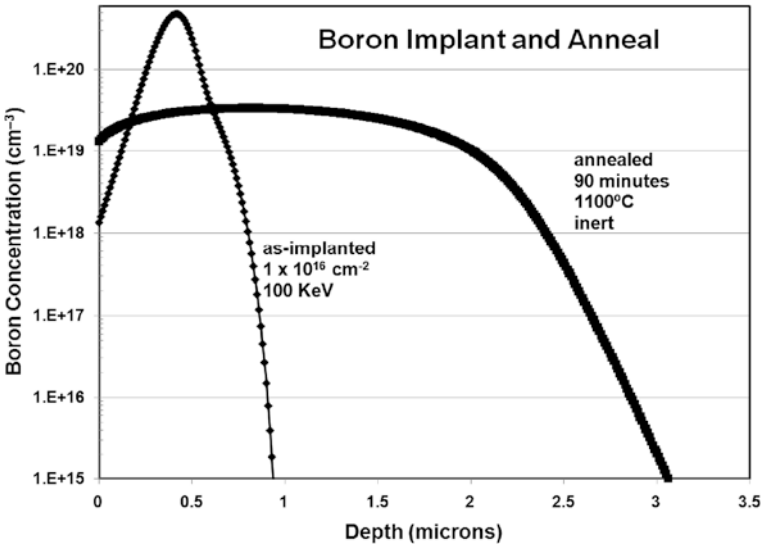

Fig. 10.32 ATHENA simulation of boron implantation and subsequent anneal. Note non-Gaussian implanted distribution and long-range diffusion

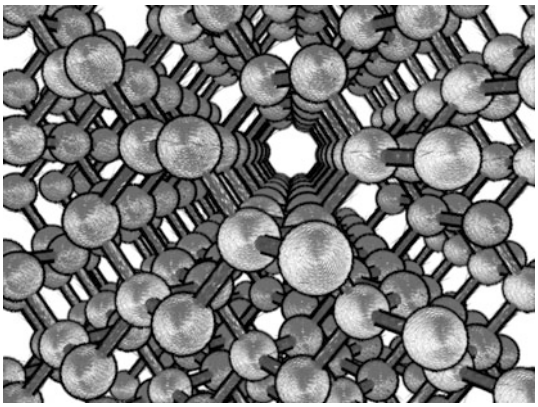

Fig. 10.33 Channel-through silicon crystal structure. Ion propagation down these channel directions results in deeper implant profiles than expected from simple models

secondary knock-on collisions, each displacing atoms from their equilibrium lattice positions where they can induce a variety of acceptor, donor, and trap electronic levels. Ions implanted into a lattice will generally come to rest in a variety of interstitial positions incompatible with acting as electrically active dopants. Atoms on the surface of the crystal, either from contamination or from structures formed on the surface, can be struck by incoming ions and end up implanted deep in the substrate by elastic collision. At high ion doses entire layers of the lattice can be rendered amorphous. The damage to the lattice due to ion collisions must be repaired by some type of thermal process in order to activate the dopant concentration.

Layers that have been rendered completely amorphous are generally easier to recrystallize and activate than layers which have been damaged but not rendered amorphous. Typical implant doses required to produce an amorphous layer are $1 \times 10^{15}\,\mathrm{cm}^{-3}$ and up. When annealed, a fully amorphous layer will begin assembling a new crystal structure using undamaged crystalline silicon below the amorphous layer (or even above it if the implant was well below the surface) as a template, in a process known as solid-state epitaxy. Excellent recrystallization can often be obtained at temperatures below 600°C if the damaged layer is rendered fully amorphous. This effect can be accomplished intentionally without doping [65] by implanting nondopant species such as argon or silicon into a silicon substrate. Sometimes an amorphous layer will be intentionally formed at a silicon surface to inhibit channeling. Channels are sealed when the crystal order near the surface is destroyed, allowing implants to be performed for shallow junctions without channeling tails.

10.5.5 Buried Insulator Layers

An interesting application of implant technology is in the production of silicon-on-insulator wafers used in a variety of electronics and MEMS applications. Two competing technologies exist, both of which depend on implantation of a heavy ion dose well below the surface of a silicon wafer.

In the SIMOX (separation by implantation of oxygen) process illustrated in Fig. 10.34, a very high dose ($> 1.8 \times 10^{18}\,\mathrm{cm}^{-2}$) of oxygen ions is implanted at high energy (200 keV or better) in a single-crystal silicon wafer. The implanted wafer is annealed to more than 1300°C to eliminate crystal damage from the ion implantation and to drive formation of a buried oxide insulating layer. This results in a thin crystalline silicon layer isolated from the bulk silicon wafer, which can be used for released MEMS structures or transistors [66].

A related process is the SmartCut^{TM} process (Fig. 10.35), which begins with a single-crystal silicon wafer coated with thermal oxide. Hydrogen or helium is implanted through the oxide to a specific depth below the silicon surface. Typical hydrogen ion doses of $> 3.5 \times 10^{16} - 1 \times 10^{17}$ are required. Once implanted, a second silicon wafer is bonded to the oxide layer, and the wafer undergoes a series of anneals that results in voids and blistering in the implanted zone. The implanted layer breaks free from the underlying donor silicon wafer, resulting in a silicon wafer with a second layer of single-crystal silicon separated by the original thermal oxide layer [67]. Both of these processes are only made possible by the ability of ion implantation doping to deposit ions at a controlled depth below the substrate surface.

10.5.6 Case Study: Heavily Doped Polysilicon

A project to fabricate thin-film polysilicon resistive heater elements as part of a microscopic MEMS infrared target array required heavily doped polysilicon with

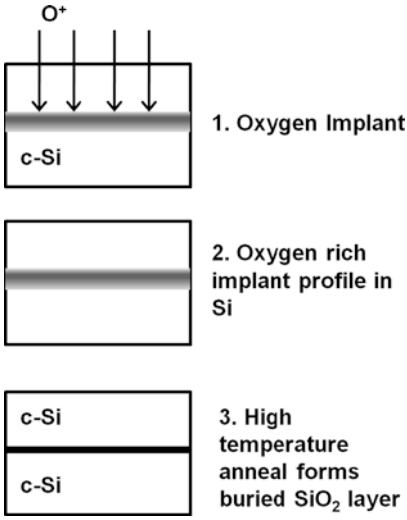

Fig. 10.34 SIMOX process for production of SOI wafers

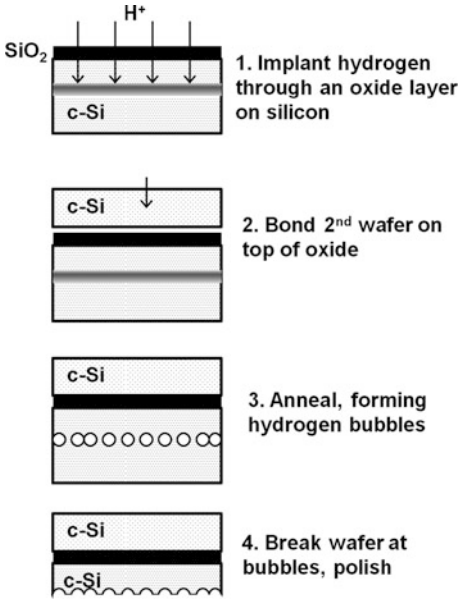

Fig. 10.35 SmartCut process for production of SOI wafers

good resistance uniformity across a six-inch wafer. Spin-on dopant sources and ion implantation were chosen as candidate processes to dope the polysilicon.

Six-inch (100) wafers were prepared with a 2 μm thick plasma-enhanced TEOS oxide deposition to act as electrical and thermal insulation. Polysilicon was deposited using a low-pressure chemical vapor deposition tube. The tube process

temperature is ramped with an increase in temperature from the load/gas injection end to the source/pump end, from 635°C at the entrance, to 650°C at the center where the wafers are located, and 665°C at the output. A 100 sccm flow of SiH_4 is injected at the load end, and the pressure is controlled to 300 mtorr by a throttle valve during the process. These conditions produce a polysilicon deposition rate of 110 Å/min.

All wafers were coated with a nominally 4000 Å polysilicon deposition. The coated polysilicon wafers were measured with a Nanospec™ spectroscopic reflectometer after coating. Four doping treatments were then performed.

Wafer 1	Spin on Borofilm-100 liquid dopant from Emulsitone Corp (Whippany, NJ) at 3000 rpm for 30 s, and bake at 200°C for 15 min in a convection oven to remove solvents. Anneal in diffusion tube in N_2 ambient for 55 min at 950°C, then anneal in O_2 ambient for an additional 5 min at 950°C. Strip oxide film in 10:1 HF solution.
Wafer 2	Spin on N-250 Emitter Diffusion Source liquid dopant from Emulsitone Corp (Whippany, NJ) at 3000 rpm for 30 s, and bake at 200°C for 15 min in a convection oven to remove solvents. Anneal in diffusion tube in N_2 ambient for 25 min at 950°C, then anneal in O_2 ambient for an additional 5 min at 950°C. Strip oxide film in 10:1 HF solution.
Wafer 3	Implant dose 1×10^{16} Boron-11 at 35 keV energy. Anneal in diffusion tube in N_2 ambient for 25 min at 950°C, then anneal in O_2 ambient for an additional 5 min at 950°C. Strip oxide film in 10:1 HF solution.
Wafer 4	Implant dose 1×10^{16} Phosphorus-31 at 100 keV energy. Anneal in diffusion tube in N_2 ambient for 25 min at 950°C, then anneal in O_2 ambient for an additional 5 min at 950°C. Strip oxide film in 10:1 HF solution.

Polysilicon thicknesses were measured again after the oxide strip so that actual bulk resistivities could be computed with the thicknesses corrected for any material lost to oxidation. An automated four-point probe system was used to measure the polysilicon sheet resistance for each wafer. The results are shown below.

Wafer	Initial thickness (Å)	Final thickness (Å)	Sheet resistance (Ω/sq)	Resistance uniformity (%)	Resistivity Ω cm
1	3979	3663	164.5	3.9	6.0×10^{-3}
2	4007	3572	158.3	10.2	5.7×10^{-3}
3	4049	3907	152.2	1.4	5.9×10^{-3}
4	4059	3880	81.1	1.6	3.1×10^{-3}

All four treatments obtained quite high doping levels suitable for our purposes. Resistivity uniformity for the spin-on dopant processes was somewhat inferior to the ion implantation results. The more costly ion implantation process was selected for this project, as resistance uniformity was critical. For applications requiring heavily doped polysilicon with less stringent resistivity requirements, the spin-on dopants produce quite comparable results at significantly lower process cost and complexity.

10.6 Plasma Doping Processes

Ion implantation processes are very effective at producing tailored dopant profiles with a high degree of control over dose and depth profile, while maintaining compatibility with a very broad selection of masking techniques. Unfortunately, one major disadvantage of conventional ion implant technology is the line-of-sight limitation imposed by the generation and transport of the dopant ion beam. Implantation of deep trench sidewalls, for instance, cannot be performed, and shadowing effects produced by large topographies, as often encountered in MEMS devices, can result in serious doping level nonuniformities. A second shortcoming of conventional implant technologies is in the difficulty of producing large beam currents at low kinetic energies, useful for producing very shallow junction depths for modern deep-submicron integrated circuitry.

A relatively new doping process has been developed specifically to address these shortcomings, called plasma doping or plasma immersion ion implantation [68, 69] (See Fig. 10.36). This process places substrates to be treated in a vacuum chamber and immerses the substrate in a plasma discharge rich in dopant ions. The plasma can be generated with a variety of methods, with electron cyclotron resonance and inductively coupled sources being popular. A bias is applied to the substrate by imposing a DC voltage (in the case of electrically conductive substrates) or by applying a radio frequency or pulsed voltage.

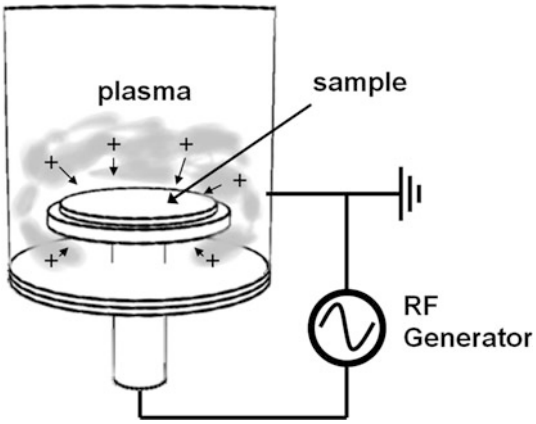

Fig. 10.36 Plasma immersion ion implantation schematic

Much as is seen in reactive ion etch processes, a negative bias is developed on the substrate surface as a consequence of the large difference in electron versus ion mass and mobility [70]. Positively charged ions in the plasma then bombard the negatively biased substrate, resulting in implantation of the ionized species. In contrast to conventional beamline ion implantation processes that typically deliver ions at 10 keV or more, the ions in the plasma impact the substrate surface at a relatively low energy, 100–5000 eV, which can be adjusted by varying the RF bias on the wafer. The plasma chemistry is chosen to be rich in the desired dopant species,

such as BF_3 to obtain boron ions and PH_3 to obtain phosphorus. The induced RF bias accelerates plasma ions relatively perpendicular to the substrate surface, thus there is no problem in doping wafers with large topographies problematic for conventional beam implant techniques. Even high-aspect-ratio deep trenches can be successfully doped [71] as illustrated schematically in Fig. 10.37.

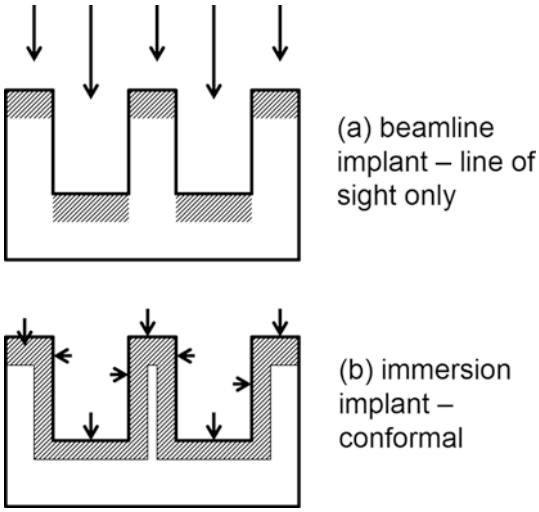

Fig. 10.37 Plasma immersion ion implantation of three-dimensional structure sidewalls

Trenches etched in silicon with up to 25:1 aspect ratio implanted with boron ions from a BF_3 plasma show about a 2:1 enhancement of sheet resistivity between the bottom of the trench and the sidewall, indicating some anisotropy in narrow structures but remarkably good ability to dope vertical structures [69]. The small size of the trenches prevents ions from being extracted from the plasma sheath perpendicular to the trench sidewall, but ions moving in the vertical direction undergo reflections and collisions that result in large ion doses being delivered to the sidewall surfaces at shallow angles where they can be adsorbed. These surface ions are transported to the bulk silicon by knock-on collision processes and electron excited diffusion. At higher ion energies, this angle of incidence for ion delivery becomes more and more vertical, resulting in a loss of implant current to the sidewalls relative to the bottom of the trench [69].

The combination of low implant energy and rapid thermal processing techniques for activation can produce extremely shallow junctions for advanced CMOS devices [72, 73]. Junction depths of 100 nm or less are obtainable for wafer DC biases of 5 kV or less after rapid thermal annealing to 1050°C for 10 s [73]. Little or no etching of silicon or damage to sensitive gate oxide structures is observed.

Plasma doping processes are capable of delivering ion currents an order of magnitude higher than most conventional ion implant machines, offering significant throughput advantages for high-dose applications. Fabrication of silicon-on-insulator wafers using SIMOX and SmartCut processes, with oxygen and hydrogen implanted species, respectively, have been demonstrated [73].

One significant difference between beamline implants and plasma immersion implants is potentially in the purity of the implanted species. Inasmuch as immersion implant systems lack any means of filtering out different ion masses or energies, a distribution of ion energies is injected into the substrate surface, leading to some broadening of the implanted dopant profile relative to monoenergetic beamline processes. All positively charged species in the plasma are implanted into the substrate to some extent, leading to somewhat higher levels of contamination relative to beam line processing. However, species such as fluorine in a BF_3 plasma generally have little effect from a doping standpoint, so plasma implant processes are regarded as being potentially as clean as beamline implant processes as long as materials used in fixturing and chamber walls are compatible.

One of the major uses of plasma immersion implant is in surface treatments. Conventional beamline implants cannot effectively treat the surfaces of complex structures due to the strict line-of-sight requirement. Tribological properties of many metals can be improved by implanting very large doses of carbon, nitrogen, or other dopant species into the surface [74]. These surfaces exhibit enhanced wear resistance, making them valuable in applications such as bearing surfaces in machine tools, molding tooling, and biomedical implants. Large ion currents delivered to surfaces can go beyond simple doping and actually alter the chemical nature of a surface by driving reactions such as oxidation or nitridation, allowing synthesis of these films on sensitive surfaces that would not withstand more conventional thermal synthesis techniques [74, 75]. For example, significantly enhanced resistance to biofouling has been reported on metal oxide surfaces synthesized by immersion implant [75], an important parameter for implantable medical devices.

10.7 Dopant Activation Methods

Dopants introduced during crystal growth or high-temperature diffusion methods are fully incorporated into the crystal matrix and immediately contribute to the electron and hole concentration of the crystal. Dopants introduced from outside by ballistic processes such as ion implantation are unlikely to occupy the correct lattice or interstitial sites in order to contribute to the free carrier inventory of the crystal. Instead, they occupy defect or interstitial sites that simply act as scattering centers and decrease the mobility of carriers in the crystal. The process of reordering the semiconductor crystal to properly incorporate dopants so they contribute electrons and holes to the matrix is known as *activation*.

10.7.1 Conventional Annealing Methods

The most straightforward activation process is simple thermal annealing. The substrate is heated to a sufficiently high temperature to mobilize crystal and dopant atoms, and it is maintained at that temperature for a time sufficient to regrow the

crystal structure with the dopants incorporated. The equipment required for conventional annealing is relatively modest, typically consisting of a three-zone diffusion furnace with quartz liner like the one illustrated in Fig. 10.25. The atmosphere of an annealing furnace is often an inert ambient such as N_2 or Ar, but often an oxidizing ambient of O_2 or steam is introduced to suppress autodoping effects (dopants migrating from wafer to wafer or from process fixturing to wafers) or to modify the final doping profile by oxidation redistribution of dopants at the surface.

The primary disadvantage of this process is the requirement for extended periods at elevated temperatures, which allows dopants to diffuse for a long distance. This limits the ability to produce junctions of an arbitrarily shallow profile. The high thermal budget also limits materials' compatibility for MEMS devices to those that can withstand extended periods at the high temperature.

The temperature and time required for dopant activation and crystal damage repair depend critically on the amount of damage done by an implant process, which varies with the implant dose and implant species. In general, implant damage at low total dose, below $1 \times 10^{12}\,\mathrm{cm}^{-2}$, can be easily removed by an anneal of about 600°C due to the small number of atoms displaced from their normal lattice positions. If a crystal structure has become fully amorphous, for implant doses of about $1 \times 10^{15}\,\mathrm{cm}^{-2}$ or higher, annealing the damage can also be performed at the relatively low process temperature of 600°C. In this case, the amorphous layer regrows using the underlying crystal structure as a template via the solid-phase epitaxy process. Complexes of buried defects remain at the boundary between the amorphous and crystalline zone after annealing which can affect electrical devices using this region, but in general very high levels of dopant activation can be obtained [7].

For ion implantation doses between about $1 \times 10^{13} - 1 \times 10^{15}$, damage to the crystal will be increasingly severe, but the crystal retains a recognizable structure that will compete with solid-phase epitaxy for regrowth. Silicon atoms displaced from their normal lattice sites can condense into extended defect structures that are difficult to break up and reintegrate into a pristine crystal structure. Annealing temperatures of up to 1050°C can be required to rebuild the crystal structure and provide a high degree of dopant activation in these heavily damaged crystals. Unfortunately, these high-temperature conventional anneals drive large amounts of diffusion of the dopant species, making formation of shallow doped layers problematic, as illustrated in Fig. 10.32. If a shallow junction is desired and only conventional thermal annealing processes are available, it is often a good strategy to implant a high dose ($5 \times 10^{15}\,\mathrm{cm}^{12}$ or higher) of Ar or Si to render the surface or buried region fully amorphous before implanting with the desired dopant species. The amorphous layer can then be annealed at relatively low temperature via solid-phase epitaxy. Fortunately, for many MEMS processes it is desirable to have substantial movement of dopants during diffusion, such as the formation of a boron etch stop for a 20 μm thick diaphragm, so inexpensive thermal processes are heavily utilized.

10.7.2 Rapid Thermal Processes

Rapid thermal processes (Fig. 10.38) have been developed as a solution to the problem of maintaining shallow junction depths while achieving full activation of high-dose implants [76, 77]. These processes subject a substrate to a high-temperature anneal for a very short time, measured in minutes or seconds, and in some of the newest process equipment, milliseconds [78]. The short high-temperature process allows movement of atoms and dopants over a distance corresponding to a few lattice constants, enabling removal of crystal damage without allowing significant diffusion of dopants. Heating is usually applied by high-power optical lamps that have been carefully arranged to produce very uniform heating of the substrate. High temperature rate ramping of substrates as brittle as silicon leads to breakage due to differential thermal expansion if significant thermal gradients are allowed to form.

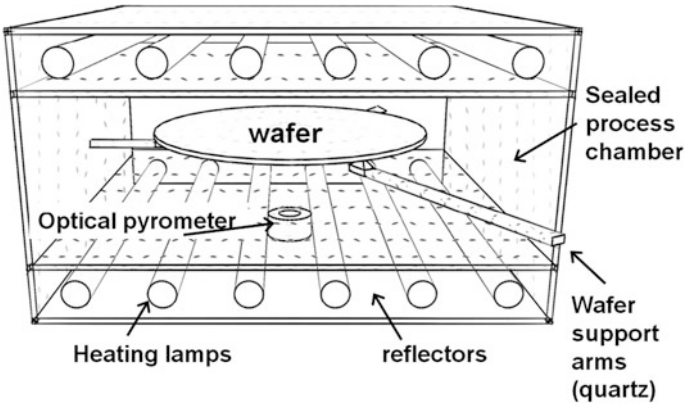

Fig. 10.38 Schematic of a rapid thermal processing system processing chamber

As with conventional thermal anneal, the RTP process chamber is often fitted with a gas injection system allowing oxidation or nitridation of the surface during anneal [77]. Temperature of the substrate is generally monitored with an optical pyrometer that controls the lamp intensity in a closed loop system. Severe difficulties can be encountered if the infrared emission characteristics of the substrate are allowed to vary [76]. This often becomes an issue if there are thin-films of various types present on the back of the silicon wafer. Often a test wafer fitted with a thermocouple can be used to calibrate the optical pyrometer system for a specific wafer configuration.

10.7.3 Low-Temperature Activation

Some process flows require a smaller thermal budget than even rapid thermal processes are capable of. For example, a process might call for implantation and activation of a dopant on the back of a wafer that already has a complete device on the front that will not tolerate temperatures of more than 400°C (a common CMOS temperature sensitivity), or dopants must be activated in an amorphous thin-film deposited on a low-temperature glass or polymer substrate. A few relatively exotic processes have been developed to allow activation of dopants at very low temperatures that are compatible with glass substrates, most metals, and some polymers.

Excimer and infrared laser annealing processes can be used to activate dopants after ion implantation on sensitive substrates [79], such as in low-temperature deposited amorphous silicon on glass used in display applications. These processes generally work by illuminating a small spot on the substrate with a high-intensity laser pulse sufficient to liquefy the material [80]. The pulse is of a short duration, so the melted region quickly resolidifies without significantly heating the bulk of the substrate, regenerating the crystal structure and providing for some degree of dopant activation. The pulsed laser beam is scanned across the area to be annealed by a rastering system. These systems have the advantage of being simple to scale up to large substrates, making them attractive in a variety of large area display and solar panel applications [81].

10.7.4 Process Selection Guide: Dopant Activation

Conventional thermal anneal	
Thermal budget	• Conventional diffusion furnace technology with quartz liners is good up to 1100°C. Silicon carbide tubes are usable to 1200°C. Higher temperatures require specialized equipment.
Time	• Depends on desired diffusion distances and/or degree of crystal damage, but usually >1 h due to need to ramp furnace temperature. • Furnace temperature ramp up and down can only be done slowly (<10°C/min), increasing process time
Material compatibility	• Silicon • SiO_2 • Si_3N_4 • Some refractory metals/silicides • Materials must have low vapor pressure at process temperature • Materials must not chemically react or form eutectic alloys with adjacent materials • Materials must not have large differences in thermal expansion coefficients
Disadvantages	• High temperature • Lengthy process

Solid-phase epitaxy	
Thermal budget	• Generally 500–700°C
Time	• Depends on thickness of amorphized layer • Regrowth rates of 10–100 Å/min are typical at temperatures near 600°C [7] • Temperature ramp rate of furnaces also increases process time • Typically 1 h or more
Material compatibility	• Silicon • SiO_2 • Si_3N_4 • Some refractory metals/silicides
Disadvantages	• Requires amorphous layer, so applicable only to ion implant processes • Requires high ion doses or heavy ions to produce amorphous layer
Rapid thermal anneal	
Thermal budget	• Typically >700°C for silicide anneals • 900–1200°C for dopant anneals
Time	• Very fast, tens of seconds to minutes • Flash lamp assist can be very fast, tens of milliseconds [78]
Material compatibility	• Silicon • SiO_2 • Si_3N_4 (delamination due to stress in nitrides can be a serious issue) • Some refractory metals/silicides
Disadvantages	• Single wafer process; low throughput • Temperature measurement difficult, generally requires accurate optical model of substrate emission for pyrometer [76] • Dislocation formation possible in crystals due to thermal nonuniformities
Laser anneal	
Thermal budget	• Effectively room temperature for the bulk of the substrate, although a narrow region at the surface will reach high temperature for a short time
Time	• Each point of the surface reaches high temperature for a very short time (<1 s), but scanning the entire wafer can take several minutes
Material compatibility	• Only the surface scanned by the laser is heated, so a variety of thermally sensitive materials (metals, polymers, etc.) can exist elsewhere on the wafer • Scanned region must be resistant to ablation or vaporization (standard Si, SiO_2, Si_3N_4 refractories) • Ideal for substrate materials with large thermal expansion coefficient mismatches
Disadvantages	• Single wafer process; low throughput • Scanning process lowers throughput even further

10.7.5 Case Study: Rapid Thermal Anneal Versus Conventional Thermal Anneal

A university research project silicon substrate diode design (Fig. 10.39) required a shallow but heavily doped boron implant, 1×10^{20} boron/cm^3 with less than 0.5 μm junction depth. We suspected that conventional diffusion tube annealing would cause excessive diffusion and an unacceptably large junction depth. ATHENA simulation of a 1 h 1100°C thermal anneal process predicted a junction depth exceeding

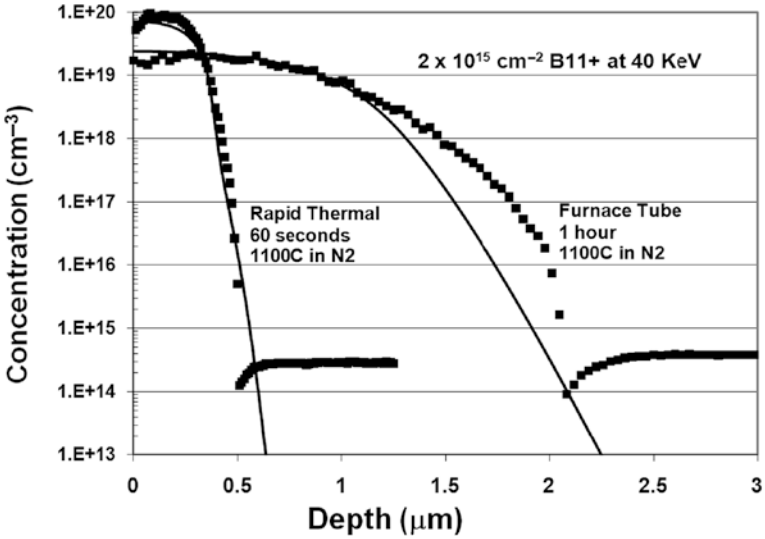

Fig. 10.39 RTP versus thermal anneal for a boron implant. Data markers are spreading resistance results; *solid lines* are simulations from ATHENA using Dual Pearson implant model. Data courtesy of Professor Karl Hirschman at Rochester Institute of Technology

2 μm. A rapid thermal anneal lasting 60 s was chosen in hopes of achieving the desired shallow junction.

Two experiments were performed for comparison purposes, the 1 h conventional anneal at 1100°C, and the 1 min rapid thermal anneal at 1100°C. A screening oxide layer of 300 Å of thermal SiO_2 was grown on the lightly P-doped n-type silicon (100) wafers prior to implant to suppress boron channeling effects in the silicon. Implants were performed on a Varian 350D medium-current implanter using $B11^+$ ions at 40 keV energy. The wafers were annealed and the screening oxide was stripped in hydrofluoric acid. Both wafers were sent to Solecon Laboratories in Reno, NV for spreading resistance characterization.

Final spreading resistance profiles are in reasonable agreement with ATHENA simulations. The rapid thermal anneal junction depth stayed at 0.5 μm, whereas the conventionally annealed junction depth was found to be just over 2 μm.

10.8 Diagnostics

Analysis of doped layers is generally focused on extracting process parameters such as dopant density, junction depth, and degree of electrical activation. Some parameters can be conveniently extracted nondestructively from wafers in midprocess, but most require destructive analysis of a completed device. Electrical measurements are convenient, inexpensive, and generally nondestructive, making them well suited for statistical process control and routine characterization of junctions and

doping levels. Spreading resistance and surface analytical techniques provide substantially more information than electrical measurements, but are much slower and considerably more expensive.

10.8.1 Electrical Measurements

Electrical resistivity measurements are by far the most common and straightforward analytical techniques available for characterizing doped layers and films. This class of diagnostic test can generally be accomplished with very modest test equipment found in many semiconductor laboratories, and fully automated four-point probe wafer mapping systems are commercially available.

Four-point probe instrumentation (Fig. 10.40) is a convenient method of nondestructively verifying target resistivity of a doped layer. It can be conveniently used on completed device structures or on partially completed layers in midprocess. Four probe points, usually made of a tungsten carbide or other hard conductive material for durability, are arranged in a line with equal spacing d between probes. A small current I is forced across the two outer probe tips, and a potential V is measured across the inner two probe tips. The sheet resistance is then given by

$$R_S = \frac{V}{I} \times \text{C.F.}, \tag{10.7}$$

where C.F. is a correction factor determined by the geometry of the measurement. In practice, current values are typically chosen to produce voltage drops on the order of 10 mV.

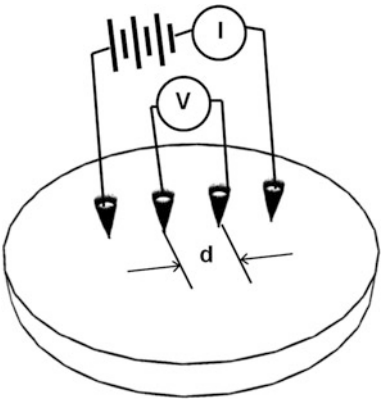

Fig. 10.40 Four-point probe apparatus for measurement of sheet resistances

For samples that are large relative to the interprobe spacing d, the correction factor converges to the value for an infinite plane, which is 4.53. This is the most common geometrical arrangement when working with silicon wafers, but correction factors are tabulated for other circular geometries in Swartzendruber [82] and can be calculated for arbitrary sizes and shapes of sample via Smits [83]. Sheet resistance

is expressed in ohms per square (Ω/square), a hybrid unit that essentially assumes a constant layer thickness when comparing measurements. If the thickness θ of the doped layer is known by some other measurement method, the bulk resistivity in Ω cm can be easily determined by

$$\rho = R_S \times \theta. \tag{10.8}$$

Four-point probe resistance measurements are a convolution of junction/thin film depth and resistivity, so are most useful in cases where the film thickness is accurately known (such as a deposited layer) or where the technique is being used as an inline warning of processing anomalies. If the expected sheet resistance (from previous measurements or by process modeling predictions) is not obtained, more complex analyses can then be performed to discover the origin of the discrepancy.

Spreading resistance measurement techniques are significantly more revealing than simple four-point probe measurements, as both layer depth and resistivity are extracted simultaneously. Doping type (n or p) can also be extracted in most cases.

Spreading resistance measurement is a destructive technique, as it requires cleaving the substrate and grinding a shallow bevel into the edge. See Fig. 10.41. The angle of the bevel is chosen so that the depth of the junction to be probed will be spread over several lateral measurements. A set of very sharp, closely spaced metal or carbide points is stepped along this beveled surface, and the effective measurement depth is then obtained geometrically as the lateral distance moved multiplied by the tangent of the bevel angle. Sufficient pressure is applied to the small tips to actually alter the phase of the silicon material in close proximity to the tip.

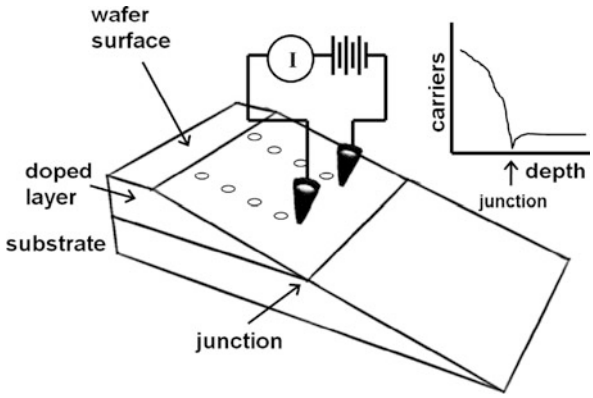

Fig. 10.41 Spreading resistance technique apparatus. The probe points are stepped along a bevel ground in the silicon. Inflections in the carrier concentration correspond to n–p junctions

This high-pressure beta-tin structure silicon allotrope is metallic in character [84], allowing good ohmic contact formation even with relatively light silicon doping levels. The current at a given bias voltage, usually a few millivolts, is measured at each point, allowing construction of a plot of spreading resistance versus position. The relationship between the measured spreading resistance and the resistivity of material near each point by is given by

$$R_{SR} = \frac{\rho}{2a}, \tag{10.9}$$

where a is the radius of the probe tips. The local resistivity number is corrected for sampling volume effects and the carrier concentration is extracted from empirical mobility calibration tables. In practice it is difficult to accurately relate the local resistivity to dopant concentration without the use of calibrated resistivity standards. It is possible to extract the type of the semiconductor with the same measurement geometry, except that no voltage bias is applied and one of the tips is heated with respect to the other.

A small voltage is generated between the probes by the Seebeck effect [85]. The polarity of this voltage is determined by the semiconductor type, with the hot probe becoming positive for n-type material and negative for p-type material. Once a carrier concentration profile is obtained, it can be related to the actual dopant profile by iterative solution of Poisson's equation [86]. Alternatively, some process modeling software such as ATHENA (Silvaco Corp, Santa Clara, CA) has a spreading resistance simulation option built in, allowing the anticipated spreading resistance profile to be constructed for comparison with measurements.

An in-house spreading resistance profiling capability is often beyond the reach of many laboratories, but fortunately commercial vendors such as Solecon Labs in Reno, NV are available to provide this service for a nominal cost. Some workers include process monitor wafers in each implant and diffusion process to facilitate spreading resistance analysis of junctions, but it is also straightforward to include test "strips" for each doping process on device wafers that are large enough to cut and bevel, typically at least $50 \times 500\,\mu\text{m}$ or larger.

Test structures fabricated on semiconductor device wafers are another convenient method of verifying dopant parameters or analyzing process anomalies. Properly designed, Van der Pauw and Kelvin resistor structures illustrated in Fig. 10.42 can be used to measure sheet resistances, lateral diffusion, and other parameters on completed or in-process wafers [7, 59]. These structures utilize four-point measurement geometries and are well suited for modestly equipped laboratories, as meaningful measurements can be made with simple power supplies, voltmeters, and ammeters. Resistivity of a layer measured by a symmetrical Van der Pauw structure [87], as illustrated in Fig. 10.42a, is expressed as

$$R_S = \frac{\pi}{\ln 2} R. \tag{10.10}$$

where

$$R = \frac{1}{4}\left(\frac{V_{12}}{I_{34}} + \frac{V_{23}}{I_{41}} + \frac{V_{34}}{I_{12}} + \frac{V_{41}}{I_{23}}\right) \tag{10.11}$$

in units of ohms/square.

In practice, one simply applies a current flow across two neighboring terminals, and measures a voltage drop across the other two terminals. All terminals are rotated one position and the measurement is repeated, until all four combinations

have been measured. These resistance measurements are averaged and the geometric correction factor is applied to extract the sheet resistance R_s. Nonsymmetrical structures are possible to measure, but are not straightforward to measure analytically. Symmetrical structures as illustrated are relatively simple mathematically to analyze. A related structure, the Kelvin resistor, is illustrated in Fig. 10.42b. This structure consists of two legs of material on two different layers, such as on a polysilicon layer and a metal layer, with a contact at the intersection. A current is applied across two dissimilar terminals as shown, and the voltage drop is measured across the other two dissimilar terminals. The contact resistance between the two materials is then simply V/I.

10.8.2 Junction Staining Techniques

Determination of junction depths can be performed by chemically decorating the n- and p-type semiconductor regions by means of a stain and directly observing the decorated regions with a microscope. A remarkably large variety of stains has been reported by various workers for specific applications [30, 88, 89], but the most common stain chemistries for silicon contain dilute hydrofluoric acid and/or nitric acid. A number of commercially prepared stain solutions are also available for different materials that avoid the use of hydrofluoric acid for safety reasons, such as the Safe-T-Stain line of materials from Epak Electronics in Somerset, UK.

Effectiveness of the stain typically depends on the level of doping of the semiconductor, and is often enhanced by applying bright illumination during the staining process (providing hole injection which drives many of these silicon oxidation reactions). The mechanism of the stain is closely related to the production of porous silicon and the electrochemical etch stop techniques described in previous sections, with partial oxides of silicon produced at the surface of the doped regions, providing visual contrast by interference of light in the thin oxide.

The edge of the sample to be examined is beveled at a shallow angle as in the spreading resistance technique, to magnify the depth of the junction laterally as the cosine of the bevel angle. As beveled edges are somewhat difficult to produce quickly and reproducibly, commercial apparatus for providing a v-shaped groove for

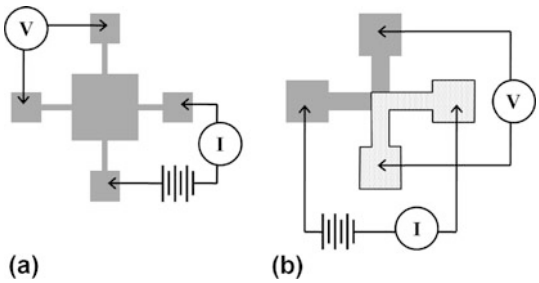

Fig. 10.42 (**a**) Van der Pauw structure for measuring sheet resistance of a layer, and (**b**) Kelvin structure for measuring contact resistance between two layers

junction staining studies is commonplace, as are systems for producing a shallow hemispherical crater in the surface of a sample with a spherical ball-bearing lap.

10.8.3 SIMS

Secondary ion mass spectroscopy (SIMS) is a powerful technique for measuring the composition of surfaces and near-surface regions [90]. See Fig. 10.43. This method focuses a beam of ions on a surface, typically argon but often xenon, oxygen, or cesium, to sputter material from the surface.

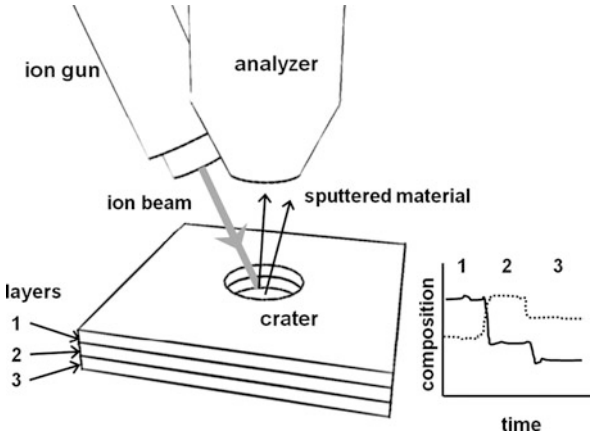

Fig. 10.43 Schematic of a secondary ion mass spectroscopy measurement. As the ion beam etches through each layer, the composition of the layer can be determined and a complete depth profile of the surface is obtained

The sputtered surface atoms are collected by a mass spectrometer and analyzed to produce an elemental fingerprint of the surface. At sufficiently high ion currents, a crater is eroded in the surface allowing the chemical composition of the substrate to be measured as a function of depth below the surface. The concentration of dopants as a function of depth is easily plotted, with sensitivities to atomic concentrations as low as 10^{12} atoms/cm^3 in some instances. Precise calibration of the depth scale can be problematic, as sputter yield depends significantly on the matrix of the material being sputtered [90]. Various thin-film standards are generally used to provide a calibration of sputter etch rate. High sputter etch rates also produce some degree of intermixing at the surface being analyzed, limiting depth resolution somewhat.

10.8.4 Case Study: Characterizing Junctions and Diagnosing Implant Anomalies

Determining the fraction of dopant that has been electrically activated is a common task when a very low thermal budget process is designed. If the drive-in temperature is too low, or the drive-in time is too short, only partial activation will occur, and device properties will be adversely affected by having a low carrier concentration.

In this example, structures on a silicon on glass (SOG) wafer would be seriously damaged by any thermal processing in excess of 600°C, and would exhibit degradation with time even at this relatively low temperature. The process flow requires a shallow phosphorus implant to provide heavily doped regions for source/drain regions of transistors and for contacts. The desired phosphorus implant dose of 1×10^{14} atoms/cm^2 was expected to be difficult to fully activate as it would cause severe crystalline damage without fully amorphizing the silicon surface region, making solid epitaxy processes at the low 600°C anneal temperature relatively ineffective at restoring crystalline order. A minimum total annealing time was desired to minimize damage to our wafers, and to minimize diffusion distance to keep the junction shallow.

Two measurements of completed junctions were performed to verify that the annealing time was sufficient. First, spreading resistance measurements were performed to extract the carrier concentration depth profile. A SIMS analysis was also performed on pieces of the same wafer to measure the total dopant depth profile. These two measurements are plotted in Fig. 10.44.

The SIMS profile illustrates the distribution of phosphorus atoms in the SOI layer regardless of whether they have been incorporated in the silicon crystal structure, or are simply occupying interstitial or damage sites. The spreading resistance profile shows only the concentration of electrical carriers, not the atoms themselves. The

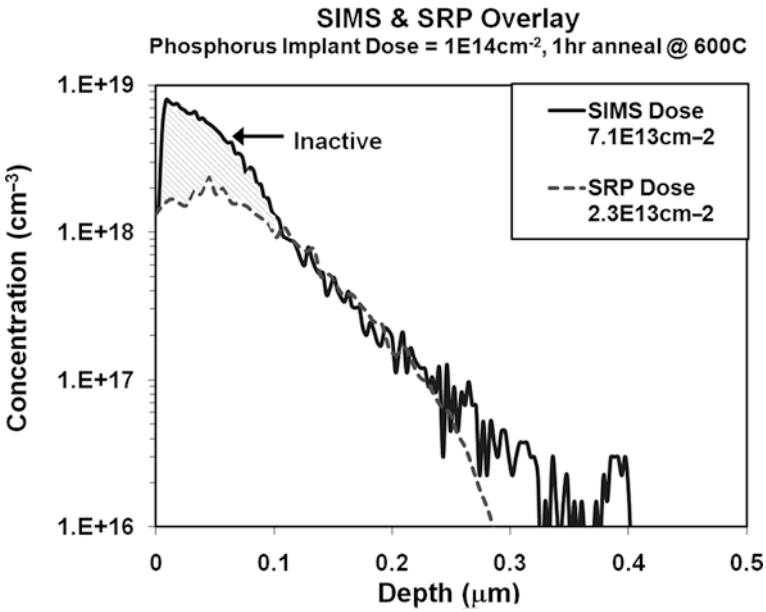

Fig. 10.44 Comparison of SIMS and SRP measurements of a phosphorus implant annealed at low temperature. A substantial amount of inactive dopant is present at the surface. Data courtesy of Professor Karl Hirschman at Rochester Institute of Technology

two analytical methods are highly complementary, probing the dopant concentration with different physical methods to provide a profile of inactive dopants as well as the usual carrier concentration profile. We see that the surface region contains a large fraction of phosphorus that does not add to the carrier concentration inventory. In fact, the fraction of dopant activated near the surface is only on the order of 25% of the total. Deeper in the SOI layer, the dopant is nearly completely active, so the total activation fraction throughout the implanted region is closer to 33%. This degree of activation proved to be sufficient for the source/drain regions of the transistors. Complete activation of this implant will require a longer or higher temperature anneal.

References

1. C.D. Thurmond: The standard thermodynamic function of the formation of electrons and holes in Ge, Si, GaAs and GaP, J. Electrochem. Soc. 122, 1133–1141 (1975)
2. B.W. Chui, M. Asheghi, Y.S. Ju, K.E. Goodson, T.W. Kenny, H.J. Mamin: Thermal conduction from microcantilever heaters in partial vacuum, Nanoscale Microscale Thermophys. Eng. 3, 217 (1999)
3. W.A. Harrison: Electronic Structure and the Properties of Solids (W.H. Freeman and Company, San Francisco, CA, 1980)
4. N.W. Ashcroft, N.D. Mermin: Solid State Physics (Saunders College, Philadelphia, PA, 1976)
5. S.M. Sze: Physics of Semiconductor Devices (Wiley, New York, NY, 1981)
6. D.A. Drabold, S.K. Estreicher: Theory of Defects in Semiconductors (Springer, New York, NY, 2007)
7. S.M. Sze: VLSI Technology (McGraw-Hill, New York, NY, 1988)
8. M. Pawlik: Resistivity of n- and p-Type Si, Doping Dependence, Properties of Silicon, p. 83 (INSPEC, London, 1988)
9. G.L. Vick, K.M. Whittle: Solid solubility and diffusion coefficients of boron in silicon, J. Electrochem. Soc. 116, 1142–1144 (1969)
10. F.A. Trumbore: Solid solubilities of impurity elements in germanium and silicon, Bell Syst. Techn. J. 39, 205–233 (1960)
11. J.S. Sandhu, J.L. Reuter: Arsenic source vapor pressure kinetics and capsule diffusion, IBM J. Res. Dev. 15, 464–471 (1971)
12. M. Gad-el-Hak: The MEMS Handbook (CRC Press, Boca Raton, FL, 2002)
13. T. Riekkinen, J. Molarius, T. Laurila, A. Nurmela, I. Suni, J.K Kivilahti: Reactive sputter deposition and properties of Ta_xN thin films, Microelectron. Eng. 64, 289–297 (2002)
14. Y. Kanda: A graphical representation of the piezoresistance coefficients in silicon, IEEE Trans. Electron Dev. 29, 64–70 (1982)
15. P.J. French, A.G.R. Evans: Piezoresistance in polysilicon and its applications to strain gauges, Solid State Electron. 32, 1–10 (1989)
16. L.J. Brillson: The structure and properties of metal-semiconductor interfaces, Surf. Sci. Rep. 2, 123–326 (1982)
17. L.J. Brillson: Contacts to Semiconductors: Fundamentals and Technology (Noyes Publications, Park Ridge, NJ, 1993)
18. H. Robbins, B. Schwartz: Chemical etching of silicon, J. Electrochem. Soc. 106, 505–508 (1959)
19. R.M. Finne, D.L. Klein: A water-amine complexing agent for etching silicon, J. Electrochem. Soc. 114, 965–970 (1967)
20. J.T.L. Thong, W.K. Choi, C.W. Chong: TMAH etching of silicon and the interaction of etching parameters, Sens. Actuators A63, 243–249 (1997)

21. H. Seidel, L. Csepregi, A. Heuberger, H. Baumgartel: Anisotropic etching of crystalline silicon in alkaline solutions I, J. Electrochem. Soc. 137, 3612–3626 (1990)
22. K. Petersen: Silicon as a mechanical material, Proc. IEEE 70, 420–457 (1982)
23. V.A. Ukraintsev, R. McGlothlin, M.A. Gribelyuk, H. Edwards: Strong effect of dopant concentration on etching rate, J. Vac. Sci. Technol. B 16, 476–480 (1998)
24. H. Robbins, B. Schwartz: Chemical etching of silicon, J. Electrochem. Soc. 107, 108–111 (1960)
25. G.T.A. Kovaks, N.I. Maluf, K.E. Petersen: Bulk micromachining of silicon, Proc. IEEE 1536–1551 (1998)
26. E.D. Palik, J.W. Faust, H.F. Gray, R.F. Greene: Study of the etch-stop mechanism in silicon, J. Electrochem. Soc. 129, 2051–2059 (1982)
27. E.D. Palik, O.J. Glembocki, R.E. Stahlbush: Fabrication and characterization of Si membranes, J. Electrochem. Soc. 135, 3126–3134 (1988)
28. H. Seidel, L. Csepregi, A. Heuberger, H. Baumgartel: Anisotropic etching of crystalline silicon in alkaline solutions II, J. Electrochem. Soc. 137, 3626–3632 (1990)
29. E. Steinsland, M. Nese, A. Hanneborg, R. Bernstein, H. Sandmo, G. Kittilsland: Boron etch-stop in TMAH solutions, Sens. Actuators A54, 728–732 (1996)
30. S.D. Collins: Etch stop techniques for micromachining, J. Electrochem. Soc. 144, 2242–2262 (1997)
31. T.N. Jackson, M.A. Tischler, K.D. Wise: An electrochemical p-n junction etch-stop for the formation of silicon microstructures, IEEE Electron Dev. Lett. EDL-2, 44–45 (1981)
32. P.M. Sarro, A.W. Van Herwaarden: Silicon cantilever beams fabricated by electrochemically controlled etching for sensor applications, J. Electrochem. Soc. 144, 1724–1729 (1986)
33. T.E. Bell, P.T.J. Gennissen, D. DeMunter, M. Kuhl: Porous silicon as a sacrificial material, J. Micromech. Microeng. 6, 361–369 (1996)
34. C.J.M. Eijkel, J. Branebjerg, M. Elwenspoek, C.M. Van De Pol: A new technology for micromachining of silicon: Dopant selective HF anodic etching for the realization of low-doped monocrystalline silicon structures, IEEE Electron Dev. Lett. 11, 588–589 (1990)
35. C.M.A. Ashruf, P.J. French, P.M. Sarro, P.M.M.C. Bressers, J.J. Kelly: Electrochemical etch stop engineering for bulk micromachining, Mechatronics 8, 595–612 (1998)
36. D. Lapadatu, M. De Cooman, R. Puers: A double-sided capacitive miniaturized accelerometer based on photovoltaic etch-stop technique, Sens. Actuators A 53, 261–266 (1996)
37. I. Zubel, M. Kramkowska: The effect of isopropyl alcohol on etching rate and roughness of (100) Si surface etched in KOH and TMAH solutions, Sens. Actuators A93, 138–147 (2001)
38. A. Reisman, M. Berkenblit, S.A. Chan, F. B. Kaufman, D.C. Green: The controlled etching of silicon in catalyzed ethylenediamine-pyrocatechol-water solutions, J. Electrochem. Soc. 126, 1406–1415 (1979)
39. E. Bassous, E.F. Baran: The fabrication of high precision nozzles by the anisotropic etching of (100) silicon, J. Electrochem. Soc. 125, 1321–1327 (1978)
40. O. Tabata, R. Asahi, H. Funabashi, S. Sugiyama: Anisotropic Etching of Silicon in $(CH_3)_4NOH$ Solutions, Solid State Sensors and Actuators, 1991, Digest of Technical Papers, 1991 International Conference on Transducers, San Francisco, CA, USA, June 24–28 (IEEE, 1991)
41. G. Kovacs, N. Maluf, K. Petersen: Bulk micromachining of silicon, Proc. IEEE 86, 1536–1551 (1998)
42. B. Schwartz, H. Robbins: Chemical etching of silicon, J. Electrochem. Soc. 123, 1903–1909 (1976)
43. H.A. Waggener: Electrochemically controlled thinning of silicon, Bell Syst. Tech. J. 49, 473–475 (1970)
44. E. Ibok, S. Garg: A characterization of the effect of deposition temperature on polysilicon properties, J. Electrochem. Soc. 140, 2927–2937 (1993)
45. A. Baudrant, M. Sacilotti: The LPCVD polysilicon phosphorus doped in-situ as an industrial process, J. Electrochem. Soc. 129, 1109–1116 (1982)

46. D. Briand, M. Sarret, K. Kis-Sion, T. Mohammed-Brahim, P. Duverneuil: In-Situ doping of silicon deposited by LPCVD: pressure influence on dopant incorporation mechanisms, Semicond. Sci. Technol. 14, 173–180 (1999)
47. T. Sinno, E. Dornberger, W. Von Ammon, R.A. Brown, F. Dupret: Defect engineering of Czochralski single-crystal silicon, Mater. Sci. Eng. 28, 149–198 (2000)
48. W. Zulehner: Czochralski growth of silicon, J. Crystal Growth 65, 189–213 (1983)
49. T.F. Ciszek: Solid-source boron doping of float-zoned silicon, J. Crystal Growth 264, 116–122 (2004)
50. E.F. Schubert: Delta doping of III-V compound semiconductors: fundamentals and device applications, J. Vac. Sci. Technol. A 8, 2980–2996 (1990)
51. T.L. Chu, C.H. Lee, G.A. Gruber: The preparation and properties of amorphous silicon nitride films, J. Electrochem. Soc. 114, 717–722 (1967)
52. D. Mathiot, J.C. Pfister: Dopant diffusion in silicon: A consistent view involving nonequilibrium defects, J. Appl. Phys. 55, 3518–3530 (1984)
53. Y. Ishikawa, Y. Sakina, H. Tanaka, S. Matsumoto, T. Niimi: The enhanced diffusion of arsenic and phosphorus in silicon by thermal oxidation, J. Electrochem. Soc. 129, 644–648 (1982)
54. B. Swaminathan, K.C. Saraswat, R.W. Dutton, T.I. Kamins: Diffusion of arsenic in polycrystalline silicon, Appl. Phys. Lett. 40, 795–798 (1982)
55. P.M. Fahey, P.B. Griffin, J.D. Plummer: Point defects and dopant diffusion in silicon, Rev. Mod. Phys. 61, 289–384 (1989)
56. M. Abramowitz, I. Stegun: Handbook of Mathematical Functions (Dover, New York, NY, 1972)
57. B.H. Justice, R. Aycock: Spin-On Dopant Method, U.S. Patent 4514440 (1985)
58. T. Aoyama, H. Tashiro, K. Suzuki: Diffusion of boron, phosphorus, arsenic, and antimony in thermally grown silicon dioxide, J. Electrochem. Soc. 146, 1879–1883 (1999)
59. J.D. Plummer: Silicon VLSI Technology (Prentice-Hall, Englewood Cliffs, NJ, 2000)
60. Code available at www-tcad.stanford.edu at the time of this writing
61. J.F. Ziegler, J.P. Biersack, U. Littmark: The Stopping Range of Ions in Solids (Pergamon Press, New York, NY, 1985), SRIM software available for download at the time of this writing at www.srim.org
62. L.C. Northcliffe, R.F. Schilling: Range and stopping power tables for heavy ions, Nucl. Data A7, 233–463 (1970)
63. G. Hobler: Theoretical estimate of the low-energy limit to ion channeling, Nucl. Instrum. Meth. Phys. Res. B 115, 323–327 (1996)
64. C. Park, K.M. Klein, A.F. Tasch: Efficient modeling parameter extraction for dual Pearson approach to simulation of implanted impurity profiles in silicon, Solid-State Electron. 33, 645–650 (1990)
65. H.S. Chao, P.B. Griffin, J.D. Plummer: Influence of dislocation loops created by amorphizing implants on point defect and boron diffusion in silicon, Appl. Phys. Lett. 68, 3570–3572 (1996)
66. B. Diem, P. Rey, S. Renard, S.V. Bosson, H. Bono, F. Michel, M.T. Delaye, G. Delapierre: SOI 'Simox': From bulk to surface micromachining, a new age for silicon sensors and actuators, Sens. Actuators A 46–47, 8–16 (1995)
67. M. Bruel, B. Aspar, A-J. Auberton-Herve: Smart-Cut: A new silicon on insulator material technology based on hydrogen implantation and wafer bonding, Jpn. J. Appl. Phys. 36, 1636–1641 (1997)
68. A. Anders: Handbook of Plasma Immersion Ion Implantation and Deposition (Wiley, New York, NY, 2000)
69. P.K. Chu, S. Qin, C. Chan, N.W. Cheung, L.A. Larson: Plasma immersion ion implantation – A fledgling technique for semiconductor processing, Mater. Sci. Eng. R17, 207–280 (1996)
70. M.A. Lieberman: Model of plasma immersion ion implantation, J. Appl. Phys. 66, 2926–2929 (1989)
71. C. Yu, N. Cheung: Trench doping conformality by plasma immersion ion implantation (PIII), IEEE Electron Dev. Lett. 15, 196–198 (1994)

72. M.J. Goeckner, S.B. Felch, Z. Fang, D. Lenoble, J. Galvier, A. Grouillet, G.C.-F. Yeap, D. Bang, M.-R. Lin: Plasma doping for shallow junctions, J. Vac. Sci. Technol. B 17, 2290–2293 (1999)
73. N.W. Cheung: Plasma immersion ion implantation for semiconductor processing, Mater. Chem. Phys. 46, 132–139 (1996)
74. J. Pelletier, A. Anders: Plasma-based ion implantation and deposition: A review of physics, technology, and applications, IEEE Trans. Plasma Sci. 33, 1944–1959 (2005)
75. P.K. Chu: Recent developments and applications of plasma immersion ion implantation, J. Vac. Sci. Technol. B 22, 289–296 (2004)
76. R.B. Fair: Rapid Thermal Processing (Academic, Boston, MA, 1993)
77. V.E. Borishenko, P.J. Hesketh: Rapid Thermal Processing of Semiconductors (Plenum Press, New York, NY, 1997)
78. T. Gebel, M. Voelskow, W. Skorupa, G. Mannino, V. Privitera, F. Priolo, E. Napolitani, A. Carnera: Flash lamp annealing with millisecond pulses for ultra-shallow boron profiles in silicon, Nucl. Instrum. Meth. Phys. Res. B 186, 287–291 (2002)
79. C.W. White, J. Narayan, R.T. Young: Laser annealing of ion-implanted semiconductors, Science 4, 461–468 (1979)
80. R.F. Wood, G.E. Giles: Macroscopic theory of pulsed-laser annealing, Phys. Rev. B 23, 2923–2942 (1981)
81. S. Uchikoga, N. Ibaraki: Low-temperature poly-Si TFT-LCD by excimer laser anneal, Thin Solid Films 383, 19–24 (2001)
82. L. Swartzendruber: Correction Factor Tables for Four-Point Probe Resistivity Measurements on Thin, Circular Semiconductor Samples, National Bureau of Standards Technical Note 199 (1964)
83. F.M. Smits: Measurement of sheet resistivities with the four point probe, Bell Syst. Tech. J. 5, 711–718 (1958)
84. J.Z. Hu, I.L. Spain: Phases of silicon at high pressure, Solid State Commun. 51, 263–266 (1984)
85. T.H. Geballe, G.W. Hull: Seebeck effect in silicon, Phys. Rev. 98, 940–947 (1955)
86. S. Selberherr: Analysis and Simulation of Semiconductor Devices (Springer, New York, NY, 1984)
87. L.J. van der Pauw: A method of measuring specific resistivity and hall effect of discs of arbitrary shape, Philips Res. Rep. 13, 1–9 (1958)
88. R. Subrahmanyan, H.Z. Massoud, R.B. Fair: Accurate Junction-Depth Measurements Using Chemical Staining, Semiconductor Fabrication: Technology and Metrology, pp. 126–149 (American Society for Testing and Materials, Ann Arbor, MI, 1989)
89. J.L. Vossen, W. Kern: Thin Film Processes (Academic, San Diego, CA, 1978)
90. A.W. Czanderna, T.E. Madey, C.J. Powell: Beam Effects, Surface Topography, and Depth Profiling in Surface Analysis (Plenum Press, New York, NY, 1998)

Chapter 11
Wafer Bonding

Shawn J. Cunningham and Mario Kupnik

Abstract Wafer bonding is an integral part of the fabrication of MEMS, optoelectronics, and heterogeneous wafer stacks, including silicon-on-insulator. Wafer bonding can be divided into two technological groups: direct bonding and intermediate layer bonding. Direct bonding relies on the cohesive bond that is formed when the surfaces of two wafers are brought together under specific temperature and pressure conditions. Direct bonding relies on critical parameters such as surface energy, surface roughness, and surface morphology. Intermediate layer bonding relies on the cohesive bond that is formed when the surfaces of two wafers are mated with an intermediate layer. The intermediate layer can be an adhesive, polymer, solder, glass frit, or metal. Surface roughness and topography are less critical for bonding with an intermediate layer. Wafer bonding has found application in MEMS to fabricate MEMS devices, to encapsulate the MEMS device in an hermetic environment, and to transfer bond a complete MEMS device to a wafer with integrated circuits. Wafer bonding has found its earliest applications for pressure sensors and accelerometers, but the applications remain boundless.

11.1 Introduction

Without having access to the toolbox "wafer bonding," the realization of microelectromechanical systems (MEMS), with its broad range of applications, would be unimaginable. Wafer bonding is broadly classified as a bulk micromachining method in contrast to a surface micromachining fabrication method, which so far can be seen as the main method for the silicon integrated circuit (IC) industry. The

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reason to classify wafer bonding as bulk micromachining (i.e., in the same category as etching deep feature into substrates) is that during wafer bonding two entities, such as two wafers or individual dies and a substrate are brought into contact. In surface micromachining mostly thin-films are deposited, grown, patterned, and selectively etched. This categorization is not flawless, of course, because sometimes wafer bonding is used to transfer a thin-film only, such as the device layer of a silicon-on-insulator (SOI) wafer on top of another wafer or the recently emerging techniques in ultrathin wafer handling.

Wafer bonding can undoubtedly be counted as an enabling technology for the field of MEMS, in the same way one would count high-aspect-ratio micromachining of silicon using deep reactive ion etching (DRIE) [1] or selectively etching substrates with liquid etchants, just to give two examples. Wafer bonding provides us with the ability to fabricate sophisticated structures; it allows sealing and encapsulating devices or parts of a wafer; it enables us to transfer layers of various materials from one wafer to another wafer; or it simply provides support for a device fabrication itself during a sequence of fabrication steps.

The latter example is probably the one the reader already might be familiar with, in particular when she or he has some hands-on experience in microfabrication. Very often it is helpful to spin photoresist on a carrier wafer and then press a device wafer, or pieces of such a wafer, against it. By heating this stack, one has performed wafer bonding with an intermediate layer, photoresist in this example. Even though most of the time[1] this bond will be separated at some later point (e.g., by resist remover or acetone), it is a first simple example of its usefulness. The carrier wafer can be used for mechanical support as a protection layer, or it can act as a holder for pieces for further fabrication steps.

In general terms, wafer bonding aims to put two wafers (whole substrates or pieces) together. This can be achieved either in a very nonintuitive way without any intermediate material (direct bonding) or with an intermediate material (bonding with intermediate material), as we explain later. In either case, the wafers can be of the same material or of different materials. The range of possibilities of how to achieve this goal, as we describe in this chapter, is extensive. The bond can be required to be of a permanent nature (irreversible) for the realization of a particular 3-D MEMS structure, or of an impermanent nature (reversible) in the case where a fabrication process requires or benefits from such a step, as in the example mentioned before. There can be only one bonding step, or more than one for a multiwafer stack (lamination).

The requirements for the bond are as versatile as the possibilities of how to perform the bond. In some applications one needs hermetic sealing capability, such as in device encapsulation or devices that require vacuum cavities (e.g., pressure sensors, capacitive micromachined ultrasonic transducers (CMUTs) [2], micro resonators [3], or devices that need to be sealed in a certain ambient. In other applications an electrical contact at the bonding interface might be required or the resilience against liquid etchants might be essential for subsequent fabrication steps. The cleanliness

[1] A good example for an exception where the resist (SU-8) is used as a permanent intermediate layer for a MEMS device fabrication is described in [4].

state of the wafer during a certain stage might limit the usage of certain materials required for the bond, as well as the targeted bond strength that should be achieved for reliable device operation and robustness in terms of humidity, thermal expansion effects, or other influences.

There might be a certain thermal budget available that the wafers or materials used can handle. A good example is the thermal limit a CMOS substrate can handle (~400–450°C), which is an actual topic of importance for several applications where sets of arrays of MEMS devices benefit from the integrated circuitry beneath, with all its advantages (low parasitic capacitance, low-power consumption, etc.). Such thermal limitation can be for performing the bond itself or to strengthen the bond (irreversibility) in a subsequent annealing step. A good example for the advent of such an application is the monolithic integration of capacitive micromachined ultrasonic transducer (CMUT) arrays for volumetric imaging probes and therapeutic applications.

Another aspect of the thermal budget is the thermal expansion effects. The thermal expansion effects are not significant when bonding similar materials together as in silicon–silicon direct bonding. The thermal budget and materials are very important when bonding dissimilar materials or similar materials with an intermediate layer. A good example is the anodic bonding of silicon to Pyrex. Silicon and Pyrex do not have the same coefficient of thermal expansion (CTE) but in fact they do have the same CTE at two temperatures (316 and 528°C). With knowledge of the bonding temperature and the material CTE, the user can select the optimal temperature to minimize stress in the bond interface or to minimize die warpage. The thermal mismatch is subsequently important if the bonded assembly is mounted to a first-level package.

At this stage the reader might already recognize the breadth of the topic of wafer bonding. Before describing the structure of this chapter, we would like to recommend literature for further reading on the topic of wafer bonding. A good start are the books *Bonding in Microsystem Technology* by Dziuban [5] (which contains a lot of material for anodic wafer bonding), *Semiconductor Wafer Bonding: Science and Technology* by Tong and Gösele [6], and *Wafer Bonding: Applications and Technology* by Alexe and Gösele [7]. Furthermore, the excellent review articles from Plößl and Kräuter [8] (focused on direct wafer bonding), Niklaus et al. [9], and Schmidt [10] are highly recommended. In addition, we recommend the excellent MIT thesis "Wafer Bonding: Mechanics-Based Models and Experiments" from Turner [11].

In this chapter, our focus is on providing an overview on wafer bonding for MEMS, and we discuss all the main techniques for wafer bonding suitable for MEMS in general.

As mentioned earlier, wafer bonding can be done directly or by using an intermediate material between the wafers. In fact, all wafer bonding techniques can be classified based on this observation, as outlined in Fig. 11.1. A similar structure is used for this chapter:

The first part of the chapter is focused on direct wafer bonding, which is considered as the more difficult bonding technique. As shown in Fig. 11.1, we list three bonding techniques in the category of direct wafer bonding:

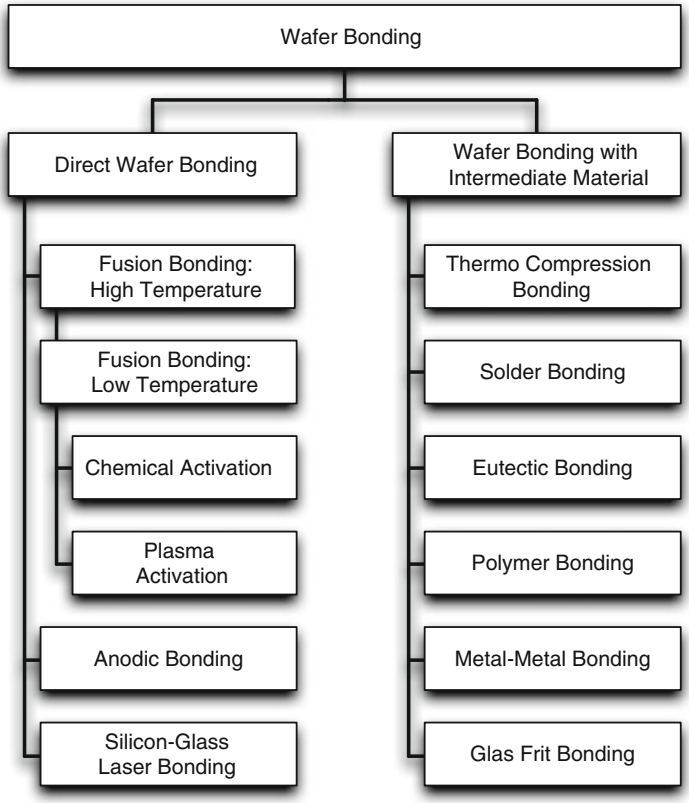

Fig. 11.1 Overview of various wafer-bonding techniques, classified by direct wafer bonding and wafer bonding with intermediate materials

First, we have temperature-assisted direct wafer bonding at high or low temperatures, often called fusion bonding. Because in both cases the activation is essential, the two most frequently used techniques (i.e., chemical and plasma activation) are listed as well. After providing some background information, we briefly explain the physics involved and define the key parameters required to quantify and verify the requirements for successful temperature-assisted direct wafer bonding. Then some general recommendations are given, which the reader might find useful when planning a MEMS process that is based on direct wafer bonding. We then describe in detail how a direct wafer bonding step is embedded in a MEMS device fabrication process. In addition, we discuss how a wafer bonding tool works in principle, and define when the usage of such a tool is inevitable.

Second, we list an electrochemically assisted direct wafer bonding technique at lower temperatures (<500°C), called anodic bonding. We count anodic bonding in the direct bonding category, albeit there are cases (e.g., see Section 11.2.5), where

an intermediate material such as Pyrex is sputtered on a wafer before the anodic bonding step. However, for most cases two substrates, such as silicon and glass, are anodic bonded without such an intermediate sputtered material. We explain the basic principles and discuss an anodic-bonding-based MEMS fabrication process for an accelerometer (wafer-level encapsulation).

The third technique that we list in the direct bonding category is silicon–glass laser bonding, which is a laser-assisted direct wafer bonding technique.

The second part of the chapter is focused on wafer bonding with intermediate materials. As shown in Fig. 11.1, there is large choice of techniques available. In this chapter we only briefly describe thermocompression bonding and eutectic bonding. Then polymer bonding is discussed in more detail including some example MEMS processes.

After comparing some of the main wafer bonding techniques in Section 11.4, we briefly discuss the bonding of heterogeneous compounds.

This is followed by a section about wafer bonding process integration focused on localized wafer bonding and through wafer via technology, including several process examples. The localized wafer bonding technique is one of the approaches used to limit the temperature exposure of the full wafer or device(s). The through via technology may not seem to belong in this chapter, which is true for many applications. When we use direct bonding to form SOI or other heterogeneous structures, the through wafer vias are not important. When we apply wafer bonding to encapsulation of a MEMS device, we have two alternatives: traverse the bond interface with the electrical interconnect, or fabricate through wafer vias to achieve an uninterrupted bond interface. Both scenarios have been successful.

In Section 11.7 we describe the main techniques to characterize the quality of wafer bonding techniques in general, and then we provide information about the existing wafer bonding infrastructure. At the end of the chapter, we list wafer bonding service providers and introduce the wafer bonding tool vendors with examples of their products suitable for MEMS applications.

11.2 Direct Wafer Bonding

As outlined in Fig. 11.1, there are several techniques for direct wafer bonding. In microelectronics and the MEMS industry, direct wafer bonding is considered the most difficult wafer bonding technique. In addition to strict requirements in terms of cleanliness (particle-free environment), the uncertainty might be related to the lack of availability of specific metrology tools during fabrication process development, such as for surface roughness and wafer curvature. Another aspect related to this might be proper surface activation before the direct bond. As we show at the end of the chapter, in the last couple of years a healthy infrastructure of equipment vendors and bonding service providers has developed, which will help to feature the full potential of wafer bonding for MEMS in future.

11.2.1 Background and Physics

Direct wafer bonding describes the process of bonding two wafers together without any intermediate material. Because wafers are composed of brittle material, direct wafer bonding is fascinating: it contradicts our everyday experience. We are not used to scenarios that two bodies just stick together without some assistance, such as by glue or other malleable layers in between. In direct wafer bonding, however, this is exactly the case, as demonstrated in Fig. 11.2.

For malleable materials it is easier to imagine that two surfaces can be brought into close enough proximity so that forces between molecules or atoms start to play a role, resulting in adhesion large enough that bonding occurs. Plastic deformation provides enough mutual conformity on both sides that short-range forces can more easily start to act.

In the case of brittle materials, such as silicon wafers, there is much less conformity between the two surfaces and bonding can occur only under very specific conditions. It is exactly these conditions one needs to keep in mind when developing a fabrication process for a MEMS device based on direct wafer bonding, as we later show.

As outlined in the excellent review article from Plößl and Kräuter [8], which contains a lot of material about the historic perspective on direct wafer bonding as well, Galileo Galilei (1564–1642) had already hypothesized that two plane polished surfaces of marble, metal, or glass, would adhere to each other whereas two rough surfaces would not. Galilei postulated that it is the vacuum between the surfaces that is the driving mechanism behind this adhesion. In the mean time, it is now well known that this is not the case.

For direct wafer bonding, the short-range surface forces based on weak interatomic bonds, such as van der Waals forces and hydrogen bonds are the dominant ones. Van der Waals forces are attributed to fluctuations in the electron distribution around atoms resulting in polarization (dipoles) of neighboring atoms, which leads to small but finite attraction forces [12]. They are much weaker, but act over slightly larger distances, than strong chemical bonds (covalent bonds), in which pairs of electrons are shared between atoms. The effect of van der Waals forces is best visualized by a force-separation curve (Fig. 11.3). In terms of the given numbers, this curve is only valid for van der Waals forces; that is, the effect of hydrogen bonds is neglected. Such a curve can be understood as a result of the combination of two force components. First, the forces of attraction fall off rapidly with separation as expected. Second, there must be a repulsive force component that starts to dominate at a certain distance ($<\sim 0.2$ nm), because otherwise the attractive forces alone would let the material collapse into virtually zero volume.

The shaded area in Fig. 11.3 corresponds to the work of adhesion (W) available for the bonding (energy per unit area), the total work done by the surface attraction. Before bonding two identical surfaces, both surfaces provide half of W, that is, the free surface energies γ_1 and γ_2. When the bonding wave propagates, the area in contact increases (Fig. 11.2), resulting in increasing the interface energy γ_{12}. Thus, the surface energy available for the remaining nonbonded area decreases.

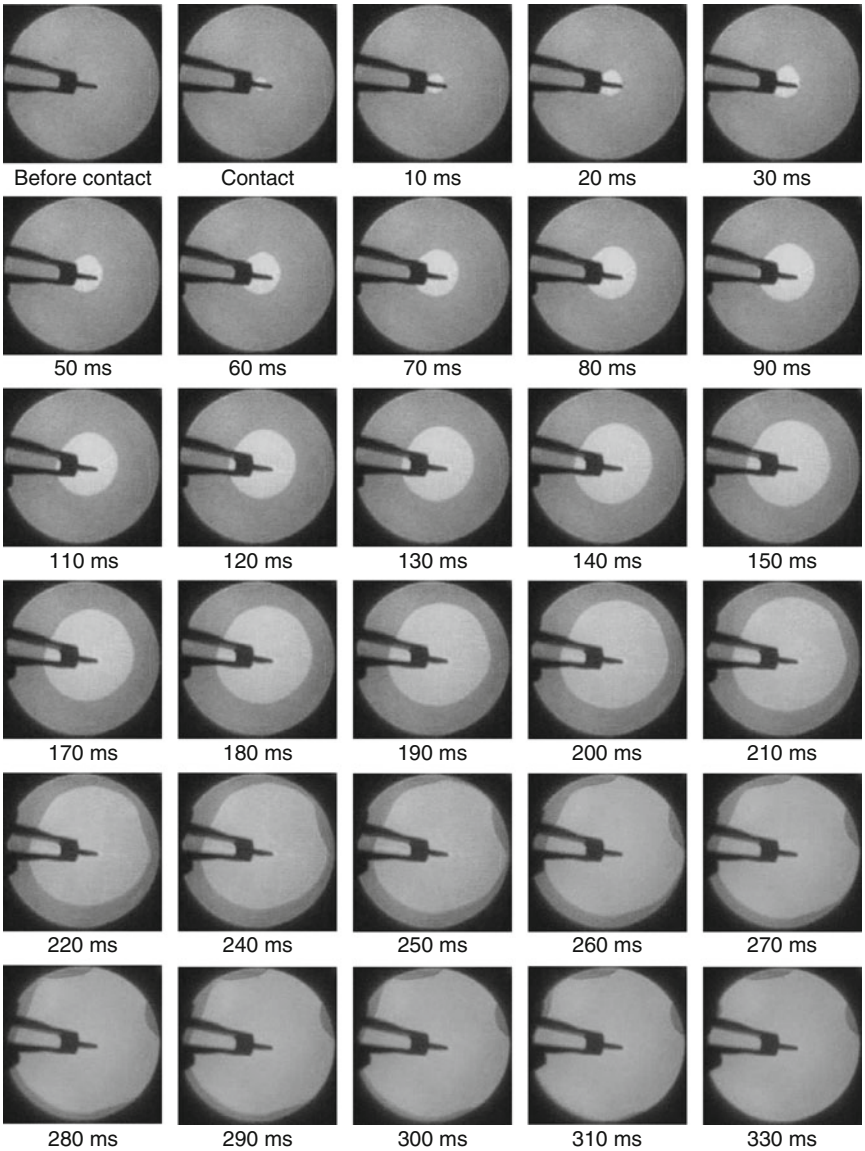

Fig. 11.2 Sequence of frames from a video that shows two 4 in. silicon wafers bonding together without any intermediate material. The wafers were illuminated by an IR light source from the bottom and an IR-sensitive camera was used. The wafers were placed on top of each other, separated by 150 μm thick spacers at the perimeter and then the direct bond was initiated by gently pushing in the center with the backside of plastic tweezers. At locations where the two surfaces are already in intimate contact, more IR light can pass through, which results in a brighter illumination for this area. Within 330 ms the "bonding wave" propagated over a distance of 9 cm (visible diameter of wafers in this setup)

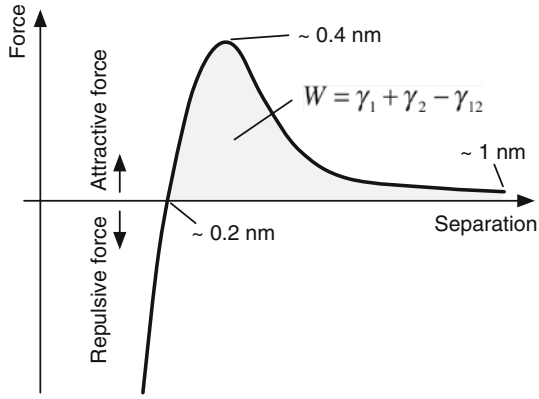

Fig. 11.3 Typical force-separation curve valid for van der Waals forces between two surfaces. In terms of the given numbers, this curve is only valid for van der Waals forces; that is, the effect of hydrogen bonds is neglected. See, for example, [11–13]

11.2.2 Parameters for Successful Direct Wafer Bonding

The concept of work of adhesion provides a basic understanding of the parameters one needs to focus on during the development of a MEMS process that requires direct wafer bonding. The goal of this section is to provide a guideline for the development of a MEMS fabrication process that contains a direct wafer bonding step.

Before further discussing all relevant parameters for such a guideline, we define important topographical parameters of wafers in general. As Turner [11] describes in his thesis, three different flatness deviations may be loosely defined for that purpose (Fig. 11.4), which are based on their spatial wavelengths.

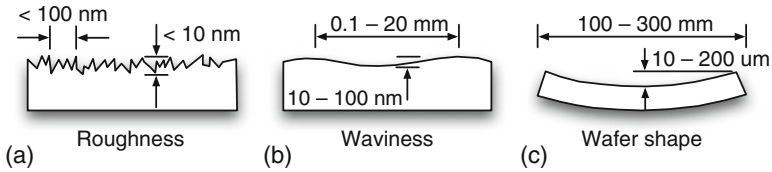

Fig. 11.4 Typical types of flatness variations on typical wafer, after [11]

11.2.2.1 Surface Roughness

The flatness variation with the smallest spatial wavelength is described by roughness parameters (Fig. 11.4, leftmost) such as the root-mean-square (RMS) value of the roughness depth. This important parameter is calculated by taking the root mean square of the series of measurements of deviations from the centerline. The best tool for carrying out such measurements is an atomic force microscope (AFM) [14]. Having access to an AFM for the development of a MEMS fabrication process that includes a direct wafer bonding step is invaluable. The AFM enables checking the wafer surface for the presence of particles and it delivers the surface roughness

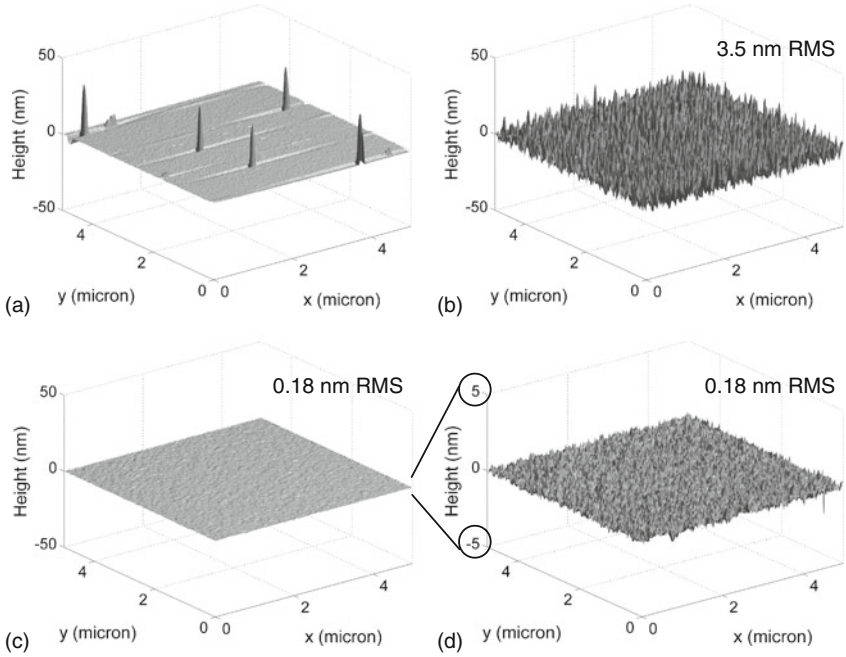

Fig. 11.5 Atomic force microscope measurements of three different samples: (**a**) wafer contaminated with particles; (**b**) silicon wafer with rough surface (has been exposed to plasma), which would fail to bond via direct wafer bonding; (**c**) fresh prime quality wafer with smooth surface; (**d**) rescaled (z-axis) view of the same data from (**c**). These wafers direct bonded successfully. For all three samples an area of 5×5 μm was scanned

information directly as a first indication of whether this wafer can be direct bonded. Figure 11.5 shows exemplary results of such AFM measurements for three different silicon samples.

On the first sample (Fig. 11.5a), five particles have been detected by the AFM. The grooves, before and after each particle, are related to the dynamics of the AFM cantilever and can be ignored for this context. Because for all of these measurements only a small area of 5×5 μm was scanned, this wafer can be assumed heavily contaminated by particles, and, thus, requires proper cleaning (see Section 11.2.4.1) prior to direct wafer bonding.

The second measurement result (Fig. 11.5b) is from a silicon wafer that was exposed to a plasma-etching tool (resist removal tool). The surface roughness is significantly larger than from the fresh prime quality silicon wafer (Fig. 11.5c, d). These two samples were used for direct wafer bonding tests. The intentionally roughened wafer did not bond and the smooth wafer bonded well.

The roughness of the surface is an important parameter, but it is not the only one, as we show later. Therefore, only a quantitative upper limit of the RMS surface roughness number for the direct "bondability" of a wafer can be given as a

guideline. This limit is around 0.25 and 0.5 nm for hydrophobic[2] and hydrophilic silicon wafers, respectively. These numbers are based on our own experiments and reported in the literature; see, for example, [8].

11.2.2.2 Waviness or Nanotopography

The waviness or nanotopography is found on a scale about three orders of magnitude larger than roughness (Fig. 11.4, center). In addition to AFM measurements over a larger scan area, a good indicator of the wafer quality is the total thickness variation (TTV), because it quantifies the wafer topography on that range of spatial wavelength as well. It is defined as the maximal height difference between the highest and lowest elevation of the top surface of the wafer. Off-the-shelf prime grade wafers exhibit TTV values of around 2 μm.

11.2.2.3 Wafer Shape

The wafer shape has the largest spatial wavelength and reflects the radius of curvature and warp of the wafer. Direct wafer bonding in particular requires that both wafers merge into the exact same curvature state, which requires energy to overcome the strain energy present in the wafers before the bond. Note that depending on the fabrication steps before the bonding step, the wafers can be flat, concave, or convex. Certainly, the worst-case scenario is the situation where a concave and a convex wafer are supposed to be direct bonded. The bond wave will only advance, as it does in Fig. 11.2, when the surface energies for the nonbonded area are large enough to overcome the strain per unit area [11]. As example, Fig. 11.4 (rightmost) shows a concave wafer shape. Such a shape can be due to a compressive layer, such as a thick thermally grown silicon dioxide layer on the backside, for example.

11.2.3 Recommendations for Successful Direct Wafer Bonding

As mentioned at the beginning of this section, our goal is to provide a guideline with recommendations for those parameters one needs to focus on while planning a MEMS fabrication process that utilizes a direct wafer bonding step:

- Ensure a particle-free bonding surface, that is, a clean environment. This is absolutely necessary for a good bonding yield.
- Protect the bonding surface during all fabrication steps prior to direct wafer bonding. Any exposure of the bonding area to plasma or liquid etchants must be avoided or minimized to the absolute minimum. For example, Miki and

[2] A hydrophobic (in Greek *hydro* means water and *phobos* means fear) surface is characterized by a high contact angle of water on that surface; that is, a hydrophobic surface has a low wettability. Hydrophilic (in Greek *philia* means friendship) surfaces have low contact angle of water, that is, high wettability.

Spearing [15] investigated the effect of buffered oxide etch (BOE) and/or potassium hydroxide solutions (KOH) on the surface roughness of silicon wafers. Their experiments showed a clear decline of the effective work of adhesion (bond energy) with the BOE and/or KOH treatment time due to increased surface roughness. The immediate conclusion is that too long an overetch during a silicon dioxide strip step, using BOE, can prevent successful direct wafer bonding. Without proper AFM measurements such an increase in surface roughness would stay undiscovered.

The protection of the bonding surface can be achieved with different techniques, such as by using photoresist, thermally grown oxide, silicon nitride, or other protective layers. This ensures low surface roughness values, assuming the layer can be removed after certain fabrication steps without harming the wafer surface. This is also valid for removing photoresist. Instead of using a plasma-based resist-removing tool (ashes the resist by heat), as commonly found in MEMS and CMOS foundries, one should rather use a regular piranha solution (H_2O_2:H_2SO_4) for removing the photoresist to avoid any extensive plasma exposure of the wafer surface. Maintaining a low surface roughness is purely motivated by the goal to maximize the available work of adhesion. The larger the free surface energies, the more energy is available to overcome the strain in the wafers. Based on this observation more recommendations can be given.

- Keep the wafers as flat as possible before the direct wafer bonding step in terms of their radius of curvature. In case you have a MEMS process that includes several fabrication steps before bonding, such as DRIE of cavities and/or the deposition of tensile or compressive films, try to monitor the radius of curvature of the wafer. The exact knowledge of these changes in curvature allows planning steps for stress state compensation of the wafer. For example, a MEMS fabrication process requires an etch step (DRIE), but also the thermal growing of thick silicon dioxide, for electrical insulation. By monitoring the curvature of the wafer, we can selectively reduce the thickness of the compressive oxide on the backside with the goal of reducing the radius of curvature before the direct bonding step. This minimizes the required energy to overcome the strain energy present in the wafers before the bond, and, this increases the likelihood of a successful direct bond with good yield.
- In addition, avoid using thick wafers when not required in your MEMS process. Where you have the choice between thicker and thinner substrates, choose the thinner one. For example, in the fabrication process of a MEMS device a direct wafer bonding step is required for transferring the active layer of an SOI wafer. After that transfer the handle and buried oxide layer (BOX) need to be removed. In this case it is better to order the SOI wafer with a thinner handle wafer and with a thinner BOX layer when possible. This makes it easier to perform the direct wafer bonding step, because there is less energy required to overcome the strain in the wafers. The reduced energy to deform thin wafers is because the stiffness of the wafer scales to the cubic power of thickness (αt^3), which means if the wafer thickness is reduced by a factor of 2 the stiffness is reduced by a factor of 8. This is a very advantageous scaling for bonding.

- The overall integration of your MEMS process should consider a proper surface activation method. This again has the goal of maximizing the available free surface energies. There are several choices available, such as chemical-assisted and plasma-assisted activation (see Section 11.2.4.1).
- While planning the layout of your MEMS fabrication process, keep the propagation of the bonding wave in mind. Basically all wafer bonding tools initiate the first contact between the two wafers in the center and then apply a defined force on the wafer stack to support the bonding step. Before the tool applies the force, the bonding wave propagates fairly symmetrical to the outside, as visible in Fig. 11.2. In case your MEMS fabrication process contains an etch step before the direct wafer bonding step for things such as fluid channels or cavities, the etch pattern plays a significant role. A larger bonding area will provide more free surface energy for the bond. Hence, for the same curvature and roughness situation, it will always be easier to bond a nonpatterned wafer or a wafer with a pattern that provides more bonding area. In addition, a good layout choice that supports stable bond wave propagation might be helpful as well. Such a pattern could be a spoke pattern, that is, a bonding area between the MEMS devices that provides continuing outwardly radial stripes, as investigated by [11] in great detail.

11.2.4 Procedure of Direct Wafer Bonding

This section gives a detailed overview of how wafers are direct bonded. The structure of the section is based on Fig. 11.6, which outlines how a direct wafer bonding step is embedded in a MEMS fabrication process.

11.2.4.1 Surface Preparation for Direct Wafer Bonding

Planarization Step

Sometimes the bonding criteria, as described in the previous section, are fulfilled and one does not need to polish the wafer surface by chemical mechanical polishing (CMP) to achieve the surface smoothness required for direct wafer bonding. However, for many MEMS devices, CMP is required to obtain a sufficiently smooth and flat surface. In addition, CMP can also be seen as a cleaning step because it can be used to remove the uppermost layer of material (few nanometers) and, thus, eliminating all surface contaminants present on the surface. For wafers with etched patterns or other surface topography, CMP can be challenging due to dishing and erosion effects [8, 16]. In addition to silicon and thermally grown silicon dioxide, CMP enables preparation of many other commonly used materials in MEMS processes for direct wafer bonding, such as polycrystalline silicon, low-temperature oxide (LTO), tetraethoxysilane (TEOS) (low stress) silicon nitride, silicon carbide, quartz, fused silica, aluminum oxide, certain types of polymers, and even nanocrystalline diamond films. Based on our own experience, we can recommend for such cases to consult with a highly specialized CMP company, such as Entrepix, Inc., Tempe, AZ, CTO Dr. Robert Rhoades.

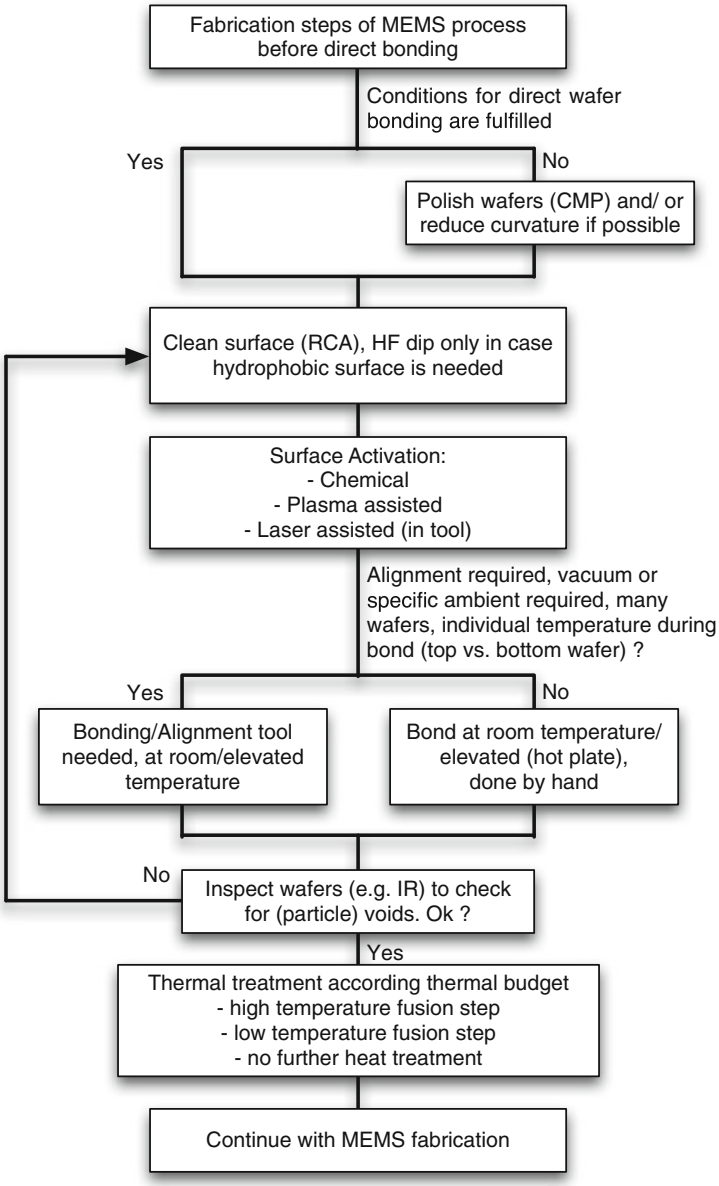

Fig. 11.6 Quantitative overview of how a direct wafer bonding step can be seen embedded in a MEMS fabrication process. Depending on the type of MEMS device there are several options available

Cleaning of Wafer Surface

After the wafers are in the state of having a smooth surface, careful cleaning is required. The surface of the wafers for a direct wafer bonding step requires extra careful cleaning. The goal is to have no particle contamination, no organic contamination (hydrocarbons from air, commonly found in high concentrations in cleanroom environments), and no ionic contamination (from metal tweezers, glassware, etc.).

The effect of these three types of contamination in terms of bonding is different [8].

Particles on the surface, such as shown in Fig. 11.5, have the most severe influence on direct wafer bonding. They act as spacers and produce a separation. As a rule of thumb, a 1 μm large particle on a 4 in. silicon wafer produces a void of about 1 cm in diameter [8]. As shown in Fig. 11.6, particle-induced voids can be detected by simple IR inspection after the room temperature bond has been performed. Because at that stage the bond is reversible, the wafers can be separated and cleaned again. In the case where the particle void is ignored or too small for IR detection (the large wavelength of the IR source limits the resolution), the size of the void will only reduce slightly during the subsequent annealing step and, thus, reduce the yield.

In terms of organic contamination the main problem is that the quality of adhesion becomes degraded. After the room temperature bonding step, usually nonbonded areas do not occur or at least are not large enough to be detected by IR, but then during the thermal treatment step, thermally induced voids can occur (nucleation of interface bubbles).

The concerns of metallic contamination are not so much on the quality of the direct bond itself, but on the electronic properties of the semiconductor material, which often might not be a problem at all for MEMS devices.

In general, the cleaning step for direct wafer bonding is not different than standard cleaning procedures [17, 18] in the microelectronics industry. A standard hydrogen peroxide-based RCA1[3] wet cleaning procedure (mixture of ammonium hydroxide, hydrogen peroxide, and DI water, in ratio 1:1:5) can be used, followed by an RCA2 clean (mixture of hydrochloric acid, hydrogen peroxide, and DI water). Another alternative, which the authors of this chapter use at the Stanford Nanofabrication Facility, is to use a hydrogen peroxide and sulfuric acid (piranha clean) mixture instead of the RCA1, followed by a standard RCA2 step. No increase in surface roughness has been found (surface roughness measurements by AFM) after this cleaning procedure, even after extensive cleaning times.

As indicated in Fig. 11.6, a dip in hydrofluoric acid (HF) can be included in the cleaning sequence. In the case of a silicon wafer this would create a hydrophobic surface because the native oxide is removed. Using this HF dip usually is advantageous, because the native oxide layer often acts as a trap for metallic or organic contaminations. It does not prevent the option of performing a hydrophilic bond,

[3]Named after the company Radio Corporation of America (RCA), in which Werner Kern, the developer of this cleaning procedure, was working at that time [17].

because it depends on the type of surface activation step, whether a hydrophobic or hydrophilic direct bond is made.

Activation of Wafer Surface

For direct wafer bonding the surface activation step after the wafer cleaning is probably the most important step. The goal is twofold: to maximize the available free surface energy and to terminate the wafer surface, that is, the dangling bonds, which would be very reactive in the case where the wafers need to be exposed to cleanroom air before the direct bonding step can be performed.

As mentioned in the previous section, there is often the important choice of whether the direct bonding should be performed with a hydrophobic or hydrophilic surface. Several aspects should be considered for the decision of whether a hydrophobic or hydrophilic surface is used. These aspects are discussed as follows for the example of silicon wafers:

- Two silicon wafers can be direct bonded with hydrophobic surfaces by stripping the native oxide right before the bonding step by means of, for example, performing an HF dip. In this case the bonding surface provides good electrical connection as well. However, as soon as the bare silicon surface comes in contact with any oxygen-providing ambient (also from the cleaning solutions used for the RCA clean, as discussed before), a fresh native oxide layer will grow, and, thus, the surfaces will be hydrophilic. The same is the case for wafers with intentionally grown oxide films, but only when there is enough time and water available for sufficient hydration of the oxide film. Such oxide film will be relatively dehydrated, in particular right after oxidation in a dry ambient, and, thus, be hydrophobic.
- Another aspect concerns the available thermal budget for the heat treatment step, that is, the maximum temperature the wafers can handle. In this context, the choice between hydrophobic versus hydrophilic bonding surfaces is essential because it affects the bond mechanism for both the room temperature bonding, as well as the reactions during the heat treatment step with the danger of increased void formation (interface bubbles). This is discussed in Section 11.2.4.4 in more detail.
- For hydrophobic silicon surfaces the dangling bonds are terminated by hydrogen and fluorine depending on the ambient conditions, except in bonding tools where the native oxide is removed under vacuum condition (see Section 11.8.2 about wafer bonding tool vendors for details). The dangling bonds of the hydrophilic silicon surface are terminated by oxygen–hydrogen (OH) groups (silanol groups). The free surface energy of this OH-terminated surface is significantly higher ~5 times due to hydrogen bonds [8], which, in general, is the reason why it is more difficult to initiate a direct bond with hydrophobic than with hydrophilic silicon wafers.

Thus, in general, a surface activation that leads to hydrophilic surfaces is preferred and commonly used for direct wafer bonding.

The activation for a hydrophilic surface can be performed by chemical activation, that is, by simply immersing the wafers into an ammonium hydroxide solution, similar as RCA1, at around 75°C for 15 min, as described, for example, in [19]. Another approach for effective hydrophilization is using oxygen plasma [20]. For example, [19] uses a 100 W, 6 sccm oxygen gas plasma in a reactive ion etcher with a base pressure of 15 mtorr for a duration of 10 s and reports significantly improved bonding strengths, even after low-temperature annealing (∼300°C). For both activation methods (i.e., chemical and plasma) the goal is to have a high density of OH groups on the bonding surfaces.

When one direct bonds two wafers that have thicker films than just native oxide, special care must be taken. Even after a long heat treatment at high temperatures (>1000°C) after the bond, the silicon dioxide to silicon dioxide bonding interface can be a significant weak point in the stack for the remaining fabrication steps in the MEMS device and, thus, should be avoided if possible. Köhler et al. [21] investigated this for liquid HF, which produces significant damage at the oxide–oxide bond interface. These authors report that the bond interface of silicon dioxide to silicon dioxide is heavily attacked by liquid HF due to capillary forces at the interface, which can form a void between the two silicon wafers and weaken the structure (high stress point). This is not the case for silicon-to-silicon and silicon-to-silicon dioxide bonding interfaces. Furthermore, for the grown interface between silicon and silicon dioxide no such damage can be observed.

Even more dramatic is the effect when vapor HF is used, which is commonly used in MEMS fabrication processes as well. We conducted the following experiment to demonstrate how the silicon dioxide to silicon dioxide bonding interface is attacked by HF vapor. We oxidized two silicon wafers (2.5 μm, wet ambient at 1100°C) and then performed a direct bond (chemically activated as described before, and thermal treatment at 1100°C for 4 h). After etching (DRIE) trenches into the silicon wafers from one side, we exposed the silicon dioxide to HF vapor. The wafer was kept at 45°C during this HF vapor etching step to avoid condensation. The first 2.5 μm oxide were etched with an etch rate of ∼100 nm per minute, as expected. As soon as the oxide-to-oxide bonding interface was reached by the HF vapor, the interface was severely attacked (Fig. 11.7a). At the bonding interface, the horizontal etch rate increased by a factor of ∼250 (!) (Fig. 11.7b). It seems that imperfections along the oxide–oxide bonding interface in combination with capillary forces are responsible for this high anisotropic etch rate. However, for intentional release steps of large structures this can be advantageous. In the case where the oxide–oxide interface is exposed to plasma etching, no such behavior can be observed. In addition, the same experiment, repeated for a silicon-to-silicon oxide bonding interface, reveals that no horizontal etch rate increase occurs.

11.2.4.2 Bonding Step – By Hand or by Using a Wafer Bonding Tool

The next decision one has to make (Fig. 11.6) depends on the type of MEMS device that is fabricated. As previously shown in Fig. 11.2, two wafers can be direct bonded

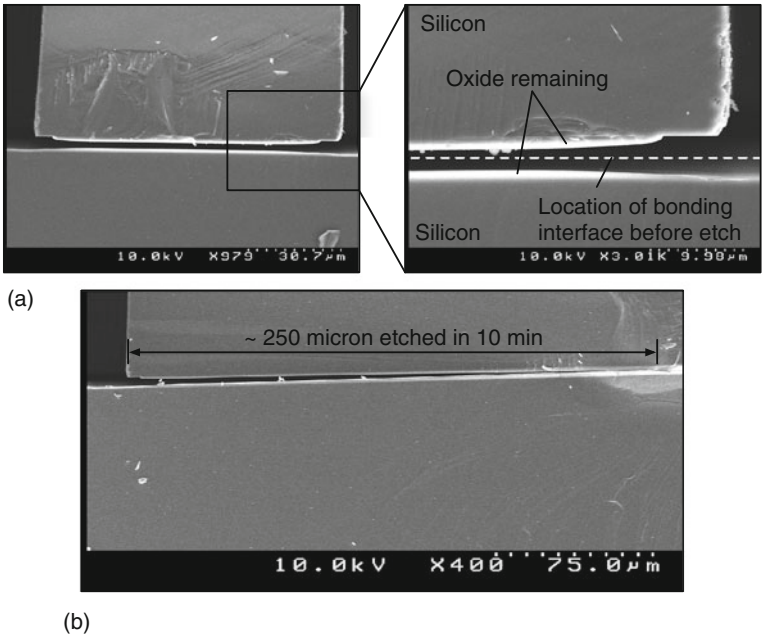

Fig. 11.7 SEMs showing that a direct bonded silicon dioxide-to-silicon dioxide bonding interface is very vulnerable when exposed to HF vapor

by just putting them on top of each other and gently applying some force at the center location. Then this wafer stack can be loaded in a furnace, on top of a hot plate, or beneath an IR lamp to strengthen the bond. Therefore, in principle no complicated bonding tool is required for the bonding step itself. A good example for such a case is the device described by Sarioglu and Solgaard [22]. This novel AFM cantilever was fabricated based on a direct wafer bonding step: first the room temperature bond was performed by hand with the help of a tilted support block made of Teflon (polytetrafluoroethylene, hand-bonding tool; see Fig. 11.8) and then the wafer stack was heated up in a regular oxidation furnace to 1050°C for 2 h to strengthen the bond.

This hand-bonding tool allows submillimeter wafer level alignment for the bonding and it is used as follows. The first wafer is placed on top of the block, and one of the flats can be aligned to one of the edges on the left side (depends on the wafer type and location of flats). The groove on the left side provides a well-defined edge so that the wafer alignment is improved and it collects particles. Then the second wafer is positioned on top of the first wafer. It will float on an air cushion, which aligns the two wafers automatically by gravity due to the tilt. Then the pin (right) is used to apply some force at the center location of the wafer stack, which initiates the propagation of the bonding wave.

The best results are obtained when the bonding is performed below a flow bench (fewer particles) or even better at an oxidation furnace, because then the airflow direction is towards the operator. The tool is heavily used for direct wafer bonding

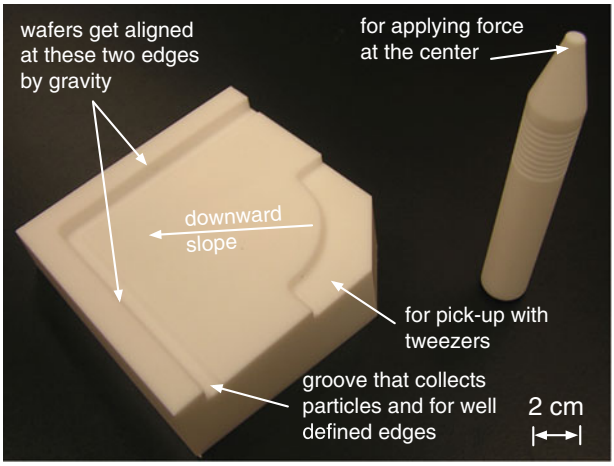

Fig. 11.8 Very useful tool for direct hand bonding available at the Stanford Nanofabrication Facility. This version is for 4 in. wafers and made of polytetrafluoroethylene (Teflon). It was designed by Dr. Aaron Partridge, SiTime Corporation, Sunnyvale, CA, and machined by Karlheinz Merkle, Machine Shop Supervisor at Department of Physics, Stanford University

at the Stanford Nanofabrication Facility. Because it is made from Teflon it can be cleaned regularly in a diffusion clean wet bench.

However, often a commercially available bonding tool will be required or preferred. A description of commercially available tools with more information can be found in Section 11.8.2. There are several reasons why a bonding tool is inevitable or advantageous for many MEMS processes. For example:

- Requirement for good alignment between top and bottom wafer. Several micrometers down to 200 nm are possible[4] on 300 mm wafers between the top and bottom wafer.
- Another reason is the necessity of evacuating cavities during the wafer bonding step. In that case the direct bonding step needs to be performed in vacuum or in a different atmosphere. A good example for the vacuum requirement is the fabrication of wafer-bonded capacitive micromachined ultrasonic transducers (CMUTs), first demonstrated by [2].
- State-of-the-art bonding tools provide further advantages such as reproducible bonding conditions (temperature, pressure, force, etc.); the ability to activate, dry, and preclean the surfaces in the bonder itself; and high-end models support automatic operation for better throughput. At the end of this chapter we discuss the

[4]Most customers today specify a 1–3 μm alignment requirement for their bonding applications. Only the latest high-end tools support low alignment tolerances down to 200 nm (personal email exchange with Jim Hermanowski, from SUSS MicroTec Inc.). The market for such systems is focused on 3-D IC fabrication, such as high-density memories (SRAM, DRAM, Flash), RF technologies, and the like.

operation principle of such bonding tools, which support many different methods for wafer bonding, in more detail.

- As a general rule, one can say that the likelihood for successful direct wafer bonding is higher when bonding tools are used. Furthermore, a better bond quality can be expected as well. Many times, however, direct bonding by hand can be advantageous for certain MEMS applications, because of the low cost (no tool purchase) and the short time required to bond wafers by hand compared to bonding tools.

11.2.4.3 Basic Operation Principle of a Wafer Bonding Tool

The basic operation principle of a bonding tool is explained (simplified) as follows (see Figs. 11.9 and 11.10):

The first wafer, with cleaned and activated bonding surface facing upwards, is put on the chuck of the bonding tool (Fig. 11.9a). An exemplary photograph of a

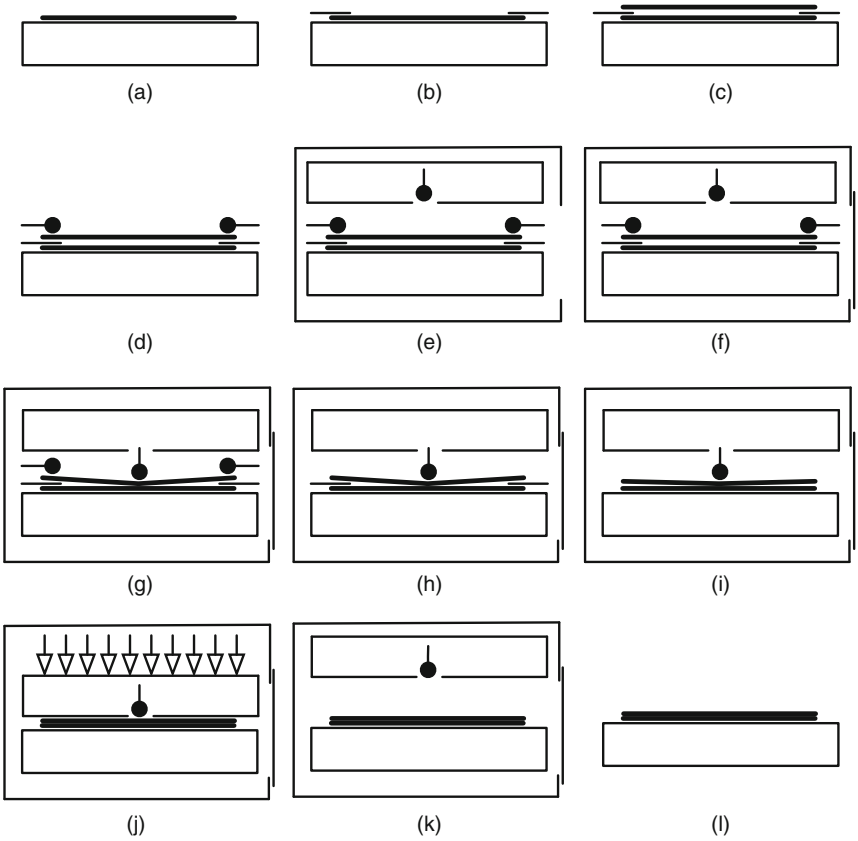

Fig. 11.9 Exemplary sequence of steps (simplified) of how a bonding tool bonds two wafers

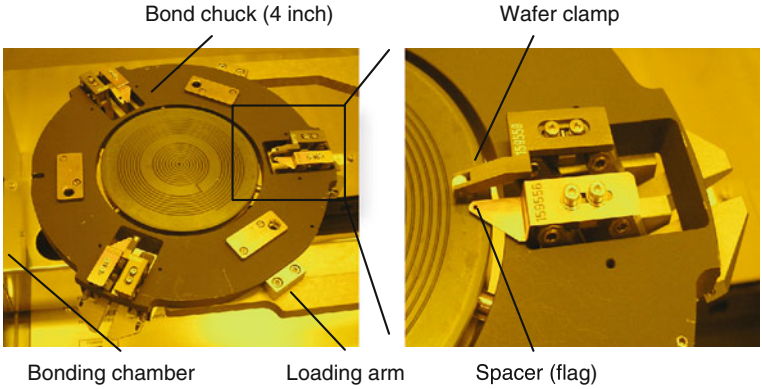

Fig. 11.10 Exemplary photograph of a chuck (hand alignment only) of a wafer bonder (Model SB6 from SUSS MicroTec AG, Germany). Pictures were taken at the Stanford Nanofabrication Facility, Stanford, CA. There are many different chucks (for alignment, for various wafer sizes, and for pieces) available

chuck with spacers and wafer clamps is shown in Fig. 11.10. Then thin spacers, also called flags (~150 μm thick) are positioned on top of this wafer at the outermost perimeter, that is, a few mm into the wafer area only (Fig. 11.9b). After that, the second wafer, with the bonding surface facing downwards, is carefully placed on top of these spacers (Fig. 11.9c), before wafer clamps are attached to hold this stack in place (Fig. 11.9d). It can be recommended to use an N_2 gun, equipped with a particle filter, before placing the top wafer to ensure that no particles are present between the wafers. Note that the steps so far can be performed in a regular alignment tool as well for aligned wafer bonding, but then a compatible wafer chuck is required. The next step is to open the purged chamber of the wafer bonding tool and load in the chuck (Fig. 11.9e).

After the chamber is closed, the pump down and heating cycle is initiated (Fig. 11.9f). Most bonders allow heating the top and bottom fixture, which will be in contact with the chuck and the wafer stack, inside the bonder independently (~up to 500°C). After the target vacuum level (e.g., 10^{-5} mbar) is reached a pin or membrane is used to apply some force in the center of the wafer stack (Fig. 11.9g), as one would do during bonding by hand as well. At that stage the bond wave cannot propagate far because the spacers are still positioned between the wafers. The wafers are constrained in terms of any movement, and, thus, the wafer clamps can be removed (Fig. 11.9h). Then the spacers are pulled out (Fig. 11.9i) and the bond wave can propagate over the entire surface, as was the case in (Fig. 11.2). The center pin or membrane is still in contact with the wafers, but in addition, now the tool has space to move the top fixture down (Fig. 11.9j) and can apply a considerable amount of force (e.g., 1000 N for direct bonding), depending on the type of bonding that is performed.

In the case of anodic bonding (Section 11.2.5), an electrical voltage can be applied via the center pin as well. For thermal compression or metal–metal bonding,

usually much larger forces (up to 100 kN) are used. The bonded wafer stack will remain for a certain amount of time (minutes to hours) under these pressure and temperature conditions. It is also possible to ramp up the temperature with a certain rate for performing a thermal treatment step already inside the bonder. After that, the force is released by moving the top fixture up (or the chuck is moved down) and the temperature can be reduced by nitrogen or by slowly purging the chamber (Fig. 11.9k). After unloading the chuck from the chamber, the bonded wafer stack can be picked up (Fig. 11.9l) and is ready for inspection under IR.

11.2.4.4 Inspection Before Heat Treatment

The next step (Fig. 11.6) is performing a first inspection by IR whether the bond was successful or not. An illustration of such a system can be found in, for example, the review article by Schmidt [10] or in the paper from Liu et al. [19].

The objective is to see whether the bond wave propagated over the entire wafer surface without the presence of any voids due to particles or contaminants. Such an example of two successfully direct bonded silicon wafers at room temperature is shown in Fig. 11.11a. Voids with the typical Newton's rings pattern or unbonded areas are not visible, which means that the wafer can be loaded in a furnace for further heat treatment to strengthen the bond. Another goal of an IR inspection after the room temperature bond can be the verification of alignment tolerances. In state-of-the-art wafer bonding tools (see Section 11.8.2), the IR inspection system can be integrated into the tool for inline quality control.

In particular for direct wafer bonding, all of this is of great value because after the room temperature bond, the bond is still reversible; that is, the wafers can be

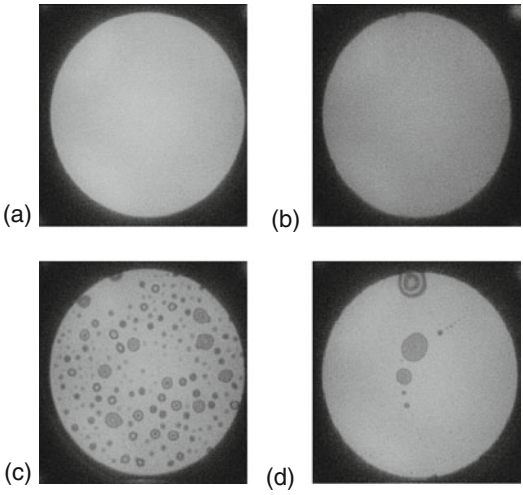

Fig. 11.11 IR images of direct-bonded silicon wafers, annealed at different temperatures. (**a**) Room temperature bond without annealing; (**b**) bonded silicon waver pair after thermal treatment at 950°C for 7 h; (**c**) 235°C anneal for 5 h; (**d**) 400°C for 14 h. These experiments were done in the Stanford Nanofabrication Facility, Stanford University, Stanford, CA

separated,[5] cleaned, surface activated, and aligned again for a second trial. However, there are some exceptions to mention. This is not the case when systems are used that perform a heating treatment already in the bonding tool, which makes the bond irreversible. In addition, with the advent of the latest bonding tools featuring special surface activation techniques (ion irradiation or in situ radical surface activation), the full bond strength (covalent bonds) can be achieved even without such heat treatment.

11.2.4.5 Thermal Treatment to Increase the Bond Strength

After the IR inspection there are several choices of how to proceed (Fig. 11.6). First, depending on the initial activation method used, full bond strength might already have been achieved, that is, covalent bonds without any or only low heat treatment (<500°C). The case of no heat treatment is still more exception than rule, but it is heavily researched at the moment and the first commercial tools with special surface activation modules are available. Such activations can be based on chemicals (Ziptronix technology [23, 24]) or other techniques (ion irradiation developed by Mitsubishi Heavy Industries LTD, in situ radical activation developed by Applied Microengineering Ltd [25–27]).

However, most likely a heat treatment will be required after the room temperature bond to increase the bond strength suitable for MEMS device fabrication. There are basically two temperature ranges of interest. The annealing can be done at temperatures larger or lower than ~500°C, which reflects a very loose classification into high and low temperature direct bonding. Another important classification is related to the application of technology, that is, the limits of 400–450°C (maximum temperature a CMOS wafer can handle) and 800°C (maximum temperature for wafers with diffusion layers); see, for example, [28].

The heat treatment step (annealing step) is the reason why instead of direct wafer bonding the term fusion bonding is often used. Because the bond strength (energy of adhesion) is tremendously increased during the heat treatment (~one order of magnitude), the wafers "fuse" together. The mechanism when heat is applied is to transform the weak interatomic bonds, present after performing the room temperature bond, into strong covalent bonds. A regular oxidation furnace can be used for high temperatures up to 1200°C.

Even though the goal of the heat treatment step is the same for hydrophilic- and hydrophobic-activated wafer surfaces, there are several differences to consider. As shown by Tong and Gösele [6], with a heating treatment of >500–600°C, the same surface energies can be achieved for the bond, but the hydrophilic-activated wafers already reach higher surface energies at lower annealing temperatures (200°C). Note that the given numbers in this section are for bonding in air. In general, vacuum allows achieving higher surface energies at even lower heat treatment temperatures.

[5]The thin tip of a plastic tweezers or a simple razor blade can be used to gently separate the two wafers at the outermost edge first.

In the rest of this section we discuss the two most studied cases, that is, heat treatment of hydrophilic and hydrophobic silicon wafers.

Heat Treatment of Hydrophilic Silicon Wafers

The bond at room temperature for the hydrophilic wafers is formed by hydrogen bonds between chemisorbed water molecules on both wafer surfaces. At elevated temperatures (>110°C [10]) the desorption of water molecules sets in and the water molecules are driven away from the bonding interface. This happens either along the bonding interface to the outside or through the native oxide to the bulk silicon, where the water molecules react with the silicon to form silicon dioxide and hydrogen. Thus, the heat treatment ensures that as soon as the water molecules have left the bonding interface, the opposing silanol groups can come close enough and start forming covalent Si–O–Si bonds (siloxane bonds) [8]. The formation of covalent bonds translates to increased fracture surface energies ($\sim$1.2 J m^{-2}), which are lower than the cohesive strength of silicon ($\sim$2.5 J m^{-2}, see, e.g., [29]. Only when heat treatment temperatures of around 700–800°C, or even higher, are used can the cohesive strength of silicon be reached. Plößl and Kräuter [8] attribute this partially to the formation of microgaps, which can only be closed when the native oxide gets viscous enough for better compliance.

For the case that one of the two wafers has a thicker oxide film and the other one only native oxide the situation is similar. However, this case is classified by [8] as being ideal, that is, better compared to direct bonding two wafers with native oxide only. This is because the native oxide from the first wafer allows the diffusion of water molecules out of the interface and the thick oxide film from the other wafer can absorb the hydrogen molecules, which reduces the formation of interface bubbles (thermal induced voids) when moderate heating treatment temperatures are used.

For illustration of this effect we conducted the experiment shown in Fig. 11.11. Hydrophilic-activated silicon wafers (4 pairs) have been direct bonded and then inspected under IR. For all four pairs a void-free room temperature bond was achieved, as shown for the first sample, which was not annealed at all (Fig. 11.11a). The bonds were performed with the hand bonding tool shown in Fig. 11.8. The second sample (Fig. 11.11b), was annealed for 9 h at 950°C. This temperature was high enough so that after the heat treatment no voids were visible under IR. The third sample, however (Fig. 11.11a), was annealed at a very moderate temperature of only 235°C for 5 h. A large number of thermal induced voids are visible after that. For the fourth sample (Fig. 11.11d) which was annealed at 400°C for 14 h, the number of visible thermal induced voids is significantly reduced, albeit some larger voids remained (Newton's rings are clearly visible).

We also performed the same experiment for the case where one of each wafer pair has a thicker oxide film, 1 μm to be specific. For the exact same three heat treatment conditions as described before no thermal induced voids occurred.

Furthermore, such observations also provide understanding of why bonding two oxidized silicon wafers is more difficult, in particular when the heat treatment is

performed at moderate temperature levels (~500°C). The thick oxide layers on both sides make it difficult for the water molecules to diffuse through to the silicon to react; that is, the water molecules remain and gather together to form microcavities. In addition to the previously mentioned weak points in terms of liquid HF or HF vapor of such an oxide to oxide bond, this is another reason why direct oxide–oxide bonding should be avoided.

Heat Treatment of Hydrophobic Silicon Wafers

The main difference from the previous case is that the dangling bonds of the silicon are terminated mostly by hydrogen atoms before the bond. As mentioned earlier, these bonds are weaker than the OH groups of a hydrophilic silicon wafer. In addition, a higher heat treatment is required to increase the fracture surface strength. As [8] outlines, a significant increase occurs at ~400°C and the cohesive strength of silicon can be reached at 700°C, which is lower than for the hydrophilic silicon wafers (~900°C). The mechanism is similar; that is, the goal again is to transform the weak hydrogen bonds into strong covalent silicon bonds by driving out of the hydrogen atoms in the interface.

11.2.4.6 Remaining Fabrication Process for MEMS Device

After the heat treatment, the remaining steps required for the MEMS device fabrication can be done. Note that for these steps the choice of direct wafer bonding offers two main advantages. First, there are no limitations in terms of temperature limits because the direct wafer bond is high-temperature stable. Second, direct wafer bonding does not add any additional materials to the wafers, such as required for bonding with intermediate layers. As a result, the cleanliness level of the wafer does not get degraded and diffusion clean equipment can be used after the bonding step as well.

11.2.5 Anodic Bonding

The anodic bond process has been described beginning with [30]. An electrochemical process [31, 32], it is driven by elevating the temperature of the glass–silicon wafer pair and applying an electric potential across the wafer pair as shown in Fig. 11.12. The silicon and glass wafers are aligned and placed together on a hot plate with the silicon against the hot plate. The potential is applied after the temperature of the wafers is raised by the hot plate and allowed to reach equilibrium. The electric potential is applied, often times in small increments relative to the total voltage across a small region adjacent to the silicon anode, which has been depleted of sodium ions. The electric fields are highest in this thin depletion zone. These high electric fields are the drivers of the oxygen anions, which are transported to the anode interfacial surface and form an oxide with the anode atoms.

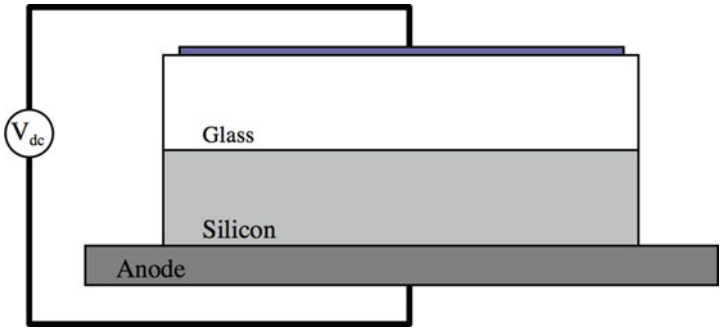

Fig. 11.12 Basis anodic bonding process

The most common implementation of the anodic bonding process uses a silicon substrate and a Pyrex substrate. The two materials have fulfilled the roles of both lid and substrate, but a common scenario is an insulating Pyrex interconnect substrate to which is bonded a silicon MEMS device and subsequently a silicon lid. The two common process parameters are substrate temperature (180–500°C) and applied voltage (200–1000 V). The bonding process has been demonstrated with vacuum or inert atmospheres, such as dry nitrogen, argon, neon. The atmosphere that is being encapsulated is driven by the product requirements such as high mechanical Q for resonators or damped frequency response for mechanical filters or high-g products.

As shown in Fig. 11.12, the silicon and glass wafers are aligned and maintained in intimate contact with the silicon wafer on the hot chuck of a wafer bonder. Usually, the backside of the glass wafer is metallized for electrical contact, in which the silicon substrate is the anode and the glass metallization is the cathode as shown. The resultant applied electric field drive Na (or Li) ions from the glass silicon interface. The disassociated oxygen ions react with the silicon to form an irreversible silicon–oxide bond. The primary variables in this process are time, temperature, and voltage. Because of the strong electrostatic pressure [33] that is developed this process is more tolerant of surface topography or defects. During this process, the oxygen may not be completely consumed by the silicon in the MEMS cavity. The resulting partial pressure of oxygen will be detrimental to the vacuum level or mechanical Q of the MEMS device. In this case, an oxygen getter will be needed to maintain the low vacuum levels. The partial pressure of oxygen will change the viscosity of the encapsulated gas and will need to be included in the estimate gas damping or again eliminated through specific oxygen getters.

One aspect of this process that requires consideration is the concept that wafers of two different materials are being bonded together at an elevated temperature. Because the coefficients of thermal expansion for the two wafers are different, wafer bow and interfacial stress will develop that can lead to premature failure. The CTE for silicon and glass will vary with temperature so an optimal operating point may be found that will minimize the stress but it may not optimize the bond strength.

Depending on the process parameters, it was mentioned that the elevated temperatures that might be associated with the anodic bonding process could be detrimental to integrated CMOS circuits or the MEMS materials themselves. The effect of the anodic bonding process on integrated CMOS electronics has been studied using the MOS capacitors. The parameters studied include N_m, the measured concentration of mobile ions; N_{eff}', the measured effective oxide charge; and D_{it}, the measured density of interface traps. The effect on these parameters was examined for MOS capacitors inside and outside the bond cavity.

N_m, N_{eff}, and D_{it} all increased with anodic bonding and their increase was greater for devices outside the cavity. The increase was least when the gap was large between the gate electrode and the glass wafer (<10–200 μm). A silicon nitride passivation layer over the gate electrodes reduced N_m. The increased N_m caused and increased N_{eff} and D_{it}, for the capacitors outside the bond cavity. The increased N_{eff} and D_{it} inside the cavity was caused by negative bias-temperature instability (NBTI), which is caused by a combination of high temperature and high electric field across the oxide. A likely reaction is for hydrogenous species A (H_2O) reacting with Si–H defects to form a positive oxide charge (AH^+) and an interface trap (Si·) ($\equiv \mathrm{Si} - \mathrm{H} + \mathrm{A} + \mathrm{p}^+ \leftrightarrow \equiv \mathrm{Si} \cdot + \mathrm{AH}^+$).

The anodic bonding process described above has been used to bond wafers for the formation of silicon microstructures such as pressure sensors, accelerometers, and gyros. In addition, anodic bonding has been used to fabricate a wafer-level encapsulation of a microstructure. A production process is described for the fabrication of a MEMS accelerometer for automotive airbag deployment. The fabrication process used anodic bonding to bond a silicon micromachined sensing element to a Pyrex substrate with fixed capacitor plates. In addition, the process anodic bonded a second patterned wafer to the same Pyrex substrate. The second silicon wafer encapsulated the sensing element and provided a hermetic environment of a dry inert gas (i.e., nitrogen, neon, argon).

The Ford Microelectronics (FMI) waferlevel encapsulation process [34–36] is a classic example of lateral electrical feedthroughs. Although it is not an RF device, some of the same techniques do apply to the RF device. The goals of this process were to provide a wafer-level, hermetic encapsulation of a silicon accelerometer (and other products that might be developed using the same process). This eliminated the coat–saw–strip process for sawing an unencapsulated device. It provided the technology needed to put the MEMS device into a low-cost plastic package and that was robust to the plastic packaging process. It provided an inert environment (dry nitrogen, neon) that could be maintained for 15 years. With reference to RF applications of this encapsulation process, the electrical feedthroughs are fabricated on as an insulating substrate (Pyrex) that will include a thin insulator (sputtered Pyrex) between the interconnect and a silicon lid. The design of this feedthrough performance could address the silicon resistivity, the transmission line width, and the thickness of the sputtered Pyrex.

On the 7740 Pyrex substrate, the DC interconnects were patterned by liftoff and deposited by evaporation of a metal stack comprised of Cr/Au/Pt/Au/Cr (1500 Å) (Fig. 11.13a). This thickness is acceptable for DC interconnection of the

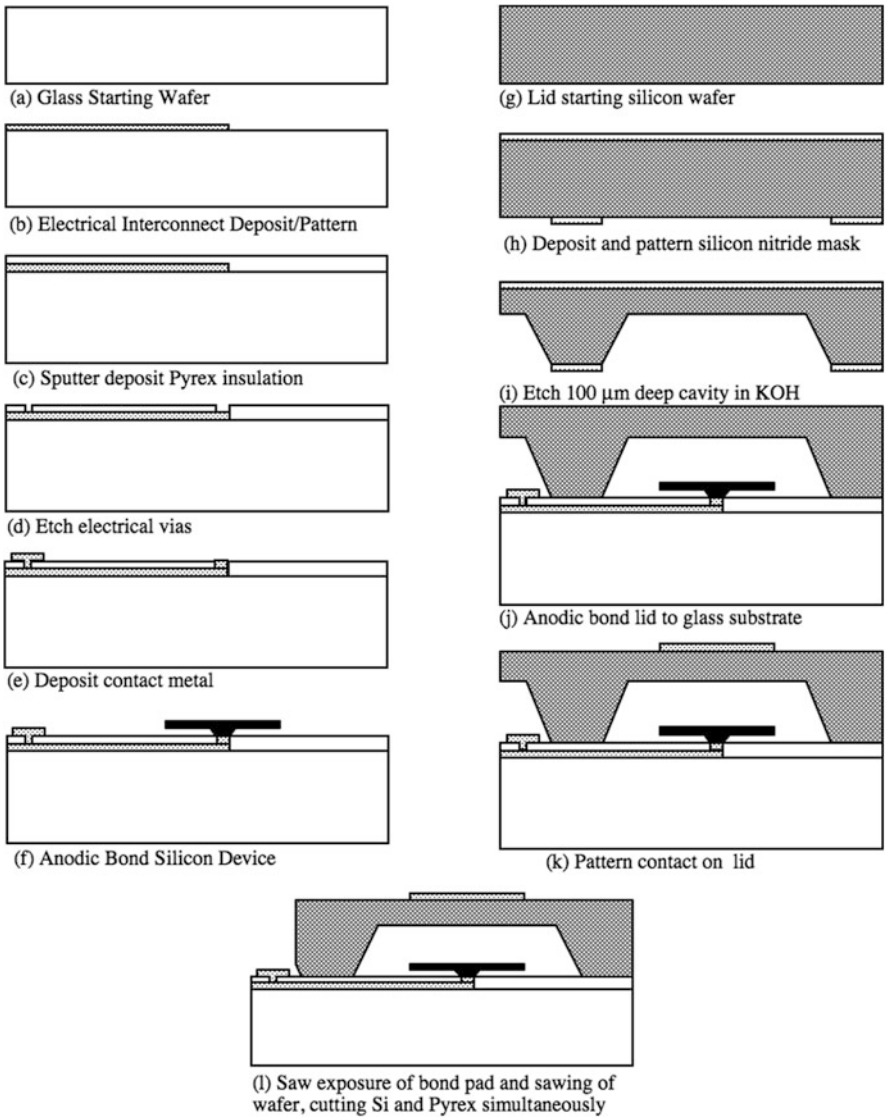

Fig. 11.13 Accelerometer wafer-level encapsulation process

electrostatic MEMS device, but the access resistance would be limiting on the RF performance. In the next steps, Pyrex is sputtered (1.5 μm) over the interconnects to provide a planarized bonding interface (Fig. 11.13b). It was found for these metal and Pyrex film thicknesses that the surface was adequately planarized to form a hermetic anodic bond. For thicker metal films necessary for RF performance (0.5–1 μm or thicker), the sputtered Pyrex layer would need to be thicker and a CMP process

would need to be introduced. These are known processes that could be introduced. Following the sputtered Pyrex deposition, electrical vias are wet etched (Fig. 11.13c) and filled with an evaporated Cr/Au/Pt contact metallization (Fig. 11.13d). A silicon microstructure is fabricated in parallel (not shown) and separately bonded to this interconnect substrate (Fig. 11.13e).

The FMI process was a three-wafer process that included the Pyrex interconnect/electrode substrate and a silicon device wafer that included an n-device layer, a p+ etch stop layer, and an n–handle wafer. Each of the three wafers included shared unit process steps, but they could be processed independently and in parallel. During early production, it was found that the manual anodic bonder was a bottleneck in the fabrication production flow. This occurred because two anodic bonding steps were performed for each completed device. The first anodic bond was formed between the device wafer and the Pyrex substrate. The second anodic bond was formed between the Pyrex substrate, including the bonded device, and a silicon lid. The bottleneck was eliminated by adding an automated bonding system that included an alignment station, robot, and bonding station. This is just a reminder as you consider moving your wafer-level encapsulation process into production. The third wafer was a silicon wafer ((100) n-silicon) used as the lid (Fig. 11.13g). The first step was to deposit Si_xN_y on both sides of the wafer and pattern one side, such that the Si_xN_y acted as a masking layer for a KOH etch (Fig. 11.13h). The KOH etch formed a 100 μm deep cavity to provide a volume for the MEMS device and to provide standoff height for the sawing process to expose the bond pads (Fig. 11.13i).

At this point the silicon wafer could be stored until needed for a mating wafer, when the silicon nitride is stripped so the silicon wafer can be bonded to the Pyrex wafer. On consideration with this particular stack is the thermal mismatch between the silicon wafer and the Pyrex wafer. This bonding process was performed at 300 V and 315°C, where there is only a small difference in the CTEs of the two materials. The silicon lid is shown bonded to the Pyrex wafer including the MEMS devices in Fig. 11.13i. In Fig. 11.13j, a contact is deposited and patterned on top of the lid for electrical connection. In subsequent assembly processes, it was possible to wire bond to the contact on top of the lid further demonstrating the robustness of the bond. During the wafer sawing process, the first saw cuts partially saw through the silicon wafer to expose the bond pads. With the bond pads exposed, a wafer-level electrical test was performed to identify known the good die and verify functionality. After the functional test, the sawing process was completed to singulate the die, which did not affect the integrity of the bond (Fig. 11.13k).

The packaged accelerometer product is shown in Fig. 11.14 at three levels of assembly. The wafer-level encapsulated silicon accelerometer is epoxy mounted to a Kovar lead frame. On the same lead frame paddle and adjacent to the accelerometer die is the Delta–Sigma modulator ASIC that is used to convert the capacitance signal for the accelerometer to a digital signal using the airbag deployment module. The accelerometer die is wire bonded to the ASIC for sensing purposes and the ASIC is wire bonded to the package pins. Figure 11.14a shows a lead frame strip with several accelerometer and ASIC die mounted to the lead frame and ready for the next processing steps. A close-up image of the accelerometer die is shown in Fig. 11.14b,

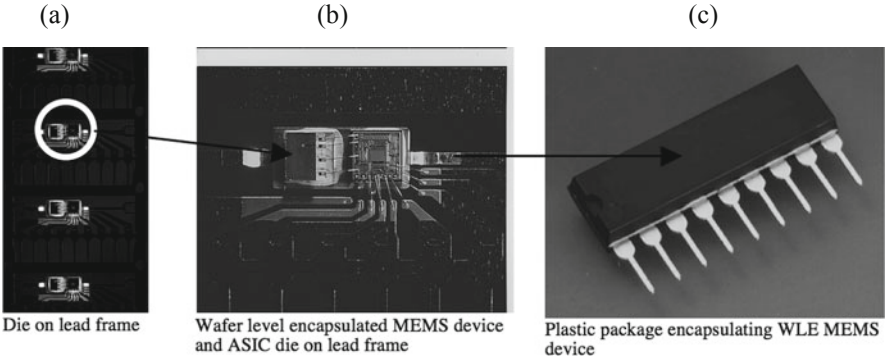

Fig. 11.14 MEMS device shown with hermetic wafer-level encapsulation and low-cost, molded plastic package

where the silicon lid can be seen bonded to the Pyrex substrate. In Fig. 11.14c, the lead frame, accelerometer die, and ASIC die have been plastic over molded to form a hermetic package. The package is hermetic because the silicon lid anodic bonded to the Pyrex substrate is hermetic. Without the ability to form a hermetic bond by anodic bonding of a silicon wafer to a Pyrex substrate, this hermetic accelerometer in a low cost plastic over molded package would not be possible.

11.2.6 Silicon–Glass Laser Bonding

Wild et al. [37] produced strong reproducible bonds between polished silicon and Pyrex wafers by laser bonding. The silicon and glass wafers are compressed together between two plates as shown in Fig. 11.15. One of the plates is transparent to the incident laser light, which needs to impinge upon the glass–silicon interface. They used a fiber-coupled, Nd:YAG laser ($\lambda = 1064$ nm) with a power of 15–30 W with a laser scan velocity of 100–400 mm/min. They demonstrated bond spots and lines up to 300 μm wide. The compressive load ranged from 10 to 30 MPa. They found the hot zone was small and self-limiting by temperature-dependent thermal

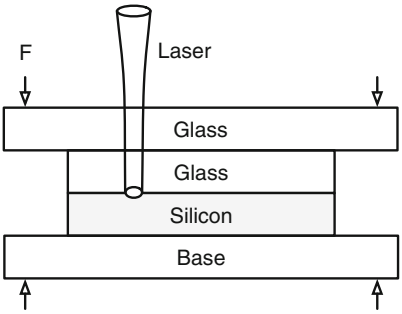

Fig. 11.15 Basic silicon–glass laser bonding process

absorption and conductivity. The absorption increases and conductivity decreases with increasing temperature. It is typical for the temperature outside the hot zone to be 150–250°C for <2 s.

11.3 Wafer Bonding with Intermediate Material

11.3.1 Thermocompression Bonding

Tsau et al. [38] have characterized the fabrication of wafer-level thermocompression bonds, which can be described and the solid-state welding of two surfaces with applied heat and pressure. The bonding material of choice is Au because it is oxidation resistant, has a low yield point, is corrosion resistant, has a high electrical conductivity, is an hermetic seal, and SiO_2 can be used as a diffusion barrier between silicon and Au. The typical bonding temperature is 300°C, which is much lower than fusion bonding at 800°C and on the order of anodic bonding at roughly 300°C. The applied pressure between the two wafers is 7 MPa. It was found that 1500 Å of SiO_2 provides an adequate diffusion barrier between Si and Au. The critical strain energy release rate was determined to be 22–67 J/m^2, which is largely independent of the Au bond layer thickness for a thickness range of 0.23–1.4 μm. A simple view of the process is shown in Fig. 11.16.

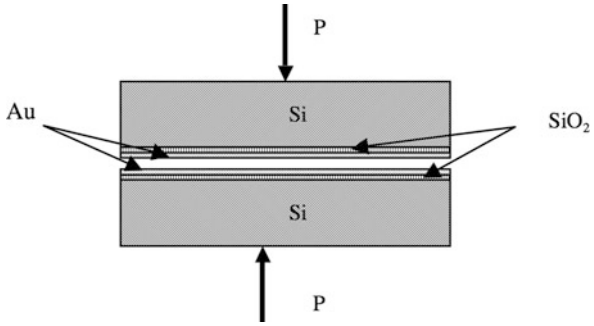

Fig. 11.16 Wafer-level thermocompression bonding

11.3.2 Eutectic Bonding

The most common eutectic bond formed is between Au and Si as described by Wolffenbuttel and Wise [39], but Au–In eutectic bonds are being developed for lower temperature bonding. The Au–Si eutectic point is 363°C, which is maintained for about 40 min. The Au usually includes an adhesion layer such as Cr or Ti and a diffusion barrier such as Pt. In Fig. 11.17, two examples of Au–Si eutectic bond constructions are shown. In the first flow an SOI wafer with a silicon handle wafer, SiO_2 isolation layer, and a silicon device layer is bonded to a silicon wafer with a

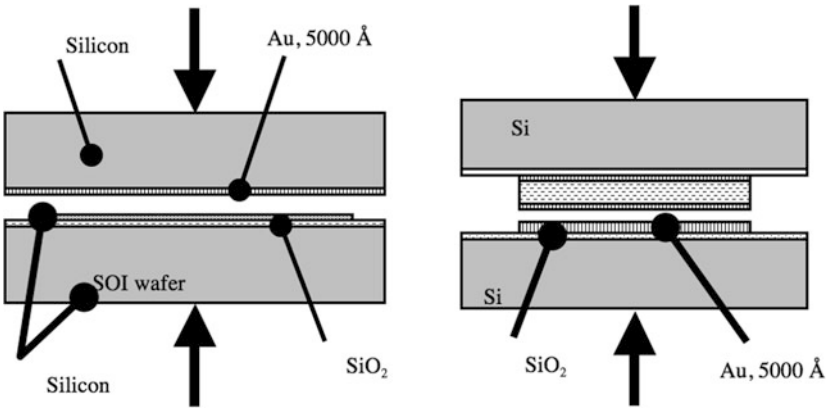

Fig. 11.17 Au–Si and Au–In eutectic bonding

5000 Å Au layer. In a second implementation, the first wafer is a silicon wafer with a SiO_2 diffusion barrier (prevent diffusion between Au and Si), and a 5000 Å Au layer (including a 150 Å Cr adhesion layer). The second silicon wafer includes a SiO_2 isolation layer, a 150 Å Cr adhesion layer, 1100 Å Au ($AuIn_2$) layer, followed by a 6 μm indium bonding layer, and concluding with a 1500 Å ($AuIn_2$) layer to prevent indium oxidation. The Au–In bonding process is performed at 250°C for 15 min with a 2 kgf force. The Au–In bonding temperature of 250°C is significantly lower than the Au–Si eutectic of 363°C.

11.3.3 Polymer Bonding

Niklaus et al. [9, 40–42] have written an excellent review of adhesive wafer bonding and demonstrated the general application of adhesive bonding. Their purpose was to describe the importance of adhesive wafer bonding that uses an intermediate polymer layer to bond two substrates. The adhesive is applied to a surface of one or both wafers. The typical method of application is by spin coating for thickness uniformity. The wafers are joined together by the application of pressure. Finally, heat or UV light is applied to convert the adhesive from a liquid or viscoelastic state to a solid state. Adhesive bonding is often chosen for the following advantages: low bonding temperature (RT to 450°C); compatibility with CMOS wafers; compatibility with a high degree of surface roughness or topography; compatibility with various wafer materials, including silicon, GaAs, glass (Pyrex, Hoya), Sapphire, and InP to InGaAsP [43], compatible with various surface conditions relative to cleanliness. Because adhesive bonding can accommodate various degrees of surface roughness, topography, and even contamination, it does not require special treatments such as planarization, chemical-mechanical polishing, or cleaning. On the other hand, the polymers are not stable over a wide temperature range, cannot

survive in various harsh environments that include solvents, and do not provide hermetic bonds against gases or moisture. In many cases the polymer or adhesive bond materials are used for temporary bonds [44].

A list of polymers used in adhesive bonding is given in Table 11.1 showing four general material classes including thermoplastics such as Parylene [45–47], thermosets, elastomers, and hybrids. A thermoplastic has the characteristics of solidifying upon cooling and can be remelted. Thermoset materials experience significant cross-linking that forms a three-dimensional bond network and cannot be remelted or reshaped. The elastomeric materials can sustain a large deformation with low stress (5–10x the unstretched dimension).

Table 11.1 Polymers used in wafer bonding

Polymer material	Characteristics
Epoxies	Thermosetting Thermal and two component curing Strong and chemically stable
UV epoxies (Su8)	Thermosetting UV curable (if one substrate is UV transparent) Strong and chemically stable Bondable with patterned films
Positive photoresists	Thermoplastic Hot melt Void formation at the interface Weak bonds
Negative photoresists	Thermosetting Thermal and UV curable Weak bond Low thermal and chemical stability Bondable with patterned films
BCB (benzocyclobutene)	Thermosetting Thermal curable High assembly yield Strong bond Thermally and chemically stable Bondable with patterned films
Flare	Thermosetting Thermal curable High assembly yield Bondable with patterned films
PMMA (polymethylmethacrylate)	Thermoplastic Hot melt
PDMS (polymethylsiloxane)	Elastomeric materials Thermal curing
Fluoropolymers	Thermoplastic and thermosetting Thermal curable or hot melt Chemically stable Bondable with patterned films

Table 11.1 (continued)

Polymer material	Characteristics
Polyimides	Thermosetting and thermoplastics Thermal curing and hot melt Voids form during imidization process Wafer/chip scale process Bondable with patterned films
MSSQ (methylsilesquioxane)	Thermosetting Thermal curing Strong Chemically and thermally stable Void formation during curing
PEEK (polyetherketone)	Thermoplastic materials Hot melt
ATSP (thermosetting copolyesters)	Thermosetting Thermal curing
PVDC (thermoplastic copolymers)	Thermoplastic Hot melt
Parylene	Thermoplastic Hot melt
LCP (liquid crystal polymer)	Thermoplastic material Hot melt Very good moisture barrier
Waxes	Thermoplastic Hot melt Low thermal stability Temporary bonding

From Niklaus et al. [9]

The typical process steps for adhesive wafer bonding include: (1) cleaning and drying the wafers; (2) treating the wafer surface with an adhesion promoter; (3) application of the polymer adhesion layer to one or both of the wafers; (4) a soft bake for partial curing of the adhesive; (5) wafers are placed in a bond chamber where they are aligned and contact established; (6) an external load or pressure is applied to the wafer stack; (7) the adhesive is remelted or cured during the pressure loading; and (8) the wafers are cooled, the pressure removed, and the wafers removed from the bonding chamber.

The cleaning and drying process is intended to remove particles, surface contaminants, and moisture from the wafer surfaces. Adhesion promoters may be needed with some polymers and some materials. They are intended to change the surface state of the wafer and enhance adhesion between the wafer and the polymer. The polymer is applied to the wafer surfaces by spraying, electrodeposition, stamping, screen printing, brushing, and dispensing of liquid precursors. The most common method in MEMS and electronic fabrication is spin coating. The viscosity of the liquid precursor and the spin speed of the wafer determine the resulting thickness and will result in highly uniform thickness and smooth surfaces. Polymer adhesive thicknesses have been achieved between 0.1 and 100 μm. In addition, the polymer

can be patterned so that the polymer bonds to a limited area of the mating wafer. A softbake is performed to remove solvents and other volatiles from the polymer material. Thermosetting materials are not or partially polymerized during the prebake. Thermoplastic materials can be completely polymerized because they can be remelted during the bonding process.

The wafers are commonly joined in a vacuum chamber to prevent voids and trapped gases from being formed at the bond interface. It is necessary to be able to pump away the trapped gases before the bond is initiated. During the pressure loading steps, thermosetting polymers should be at the bonding pressure before the curing temperature is reached because the polymerization is not reversible. With thermoplastic materials, the bond pressure can be reached after the bonding temperature is achieved. The remelting and curing of the adhesive occurs at the bonding temperature. At the end of the bonding process, the sequence of chamber purge, release of bonding pressure, and cooldown depend on the type of polymer. With thermoplastics, the wafers should be cooled before the bonding pressure is released so that the polymer is hardened and solidified before the pressure is released. In Table 11.2, a process is outlined for the thermosetting polymer BCB (benzo-cyclo-butene) [48].

Table 11.2 Typical BCB bonding process

Process step	Processing parameters
Cleaning	
Adhesion promoter	
Polymer application	Spin coating on one or both wafers
Softbake	$T = 100 - 170°\text{C},\ t =$ few minutes
Atmosphere	10^{-3} mbar
Bonding pressure	$P_B = 0.2 - 0.5$ MPa
Curing temperature	$T_B = 200 - 300°\text{C}$
Bonding time	$t = t(T_B) - t = 1$ h at 250°C

In the continued pursuit of lower temperature encapsulation processes, bonding processes have been developed using epoxy or BCB bonding. This type of bonding is consistent with many IC packaging alternatives. Some of the advantages of epoxy bonding include low cost, an established process for packaging, and low temperatures (60–200°C). It is insulating so that it can be bonded directly to RF circuits or transmission line. Because it is insulating it can work with through wafer or surface transmission lines, which pass through the bond area. Two concerns associated with organic bonds are hermeticity/leak rates and outgasing contamination. Leak rates of 10^{-7} cc/sec have been achieved with epoxy and gross leak by BCB. The outgasing can change the encapsulated environment, leave films that cause in-use stiction and reduce lifetime, or more specifically reduce the reliability of switch contacts.

A simple example of BCB bonding is shown where the substrate and lid wafer can be either silicon or glass, with the BCB applied to one of the wafers as shown

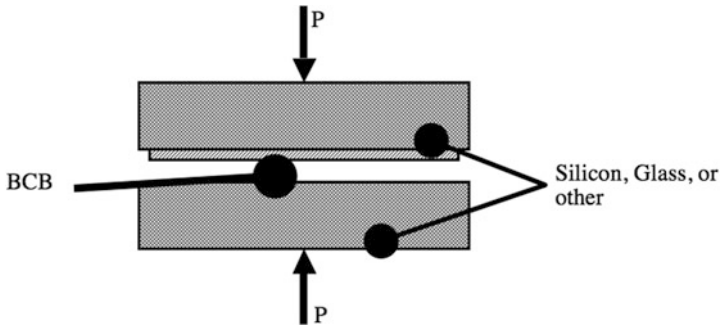

Fig. 11.18 BCB bonding schematic

in Fig. 11.18. The BCB is a photosensitive, patternable material. It has a low loss tangent: 8×10^{-4} to 2×10^{-3} for 1 MHz to 10 GHz. It has a high resistivity and low dielectric constant of 2.65. During the processing, pressure and temperature are needed. A typical bonding pressure is 250 gf. The BCB flows at a temperature of 170°C and cures at 250°C.

Jourdain et al. [49] demonstrated wafer-level packaging of RF MEMS devices using BCB bonding with both thick and thin (<100 mm) lid wafer processes. Using the BCB material allowed the implementation of coplanar RF transmission lines under the BCB seal ring rather than developing through wafer interconnect/transmission line processes. The BCB process is a low temperature process where the BCB reflows at 150°C and cures at 250°C. To achieve the RF performance, low-loss, high-resistivity lid materials are used and the cavity height should exceed 1/3 CPW width with the high resistivity silicon. The BCB process was demonstrated with a thick lid wafer that was formed from silicon or glass. A cavity is etched 10–80 mm into the lid wafer that is approximately 650 mm thick as shown in Fig. 11.19a. The BCB is spin coated and patterned on the wafer to a thickness of 3–10 mm. The lid wafer can be diced into individual die and bonded to a device die or the lid wafer can be bonded to the device wafer (Fig. 11.19b). In this case, a die level bond is described using standard flip-chip bond equipment. The lid is flipped to mate the BCB seal ring to the device wafer as shown in Fig. 11.19c. The BCB bond was formed with an applied force of 250 gf, at a reflow temperature of 170°C, and a cure temperature of 250°C.

The thin lid wafer process was developed as a low-profile encapsulation process. The lid wafer is less than 100 μm thick and is handled by bonding the thin lid wafer to a handle wafer using wax (Fig. 11.19d). With the lid wafer bonded to the handle wafer, the BCB is spin coated and patterned to form the seal ring at a thickness of 3–10 μm. As in the previous case, the thin lids are sawn into individual lids that are flip-chipped onto the MEMS die to form the seal (Fig. 11.19e). The wafer is heated to 150°C to melt the wax to remove the handle wafer and cure the BCB material as shown in Fig. 11.19f. The lidded MEMS device wafer is sawn into individual die after lidding.

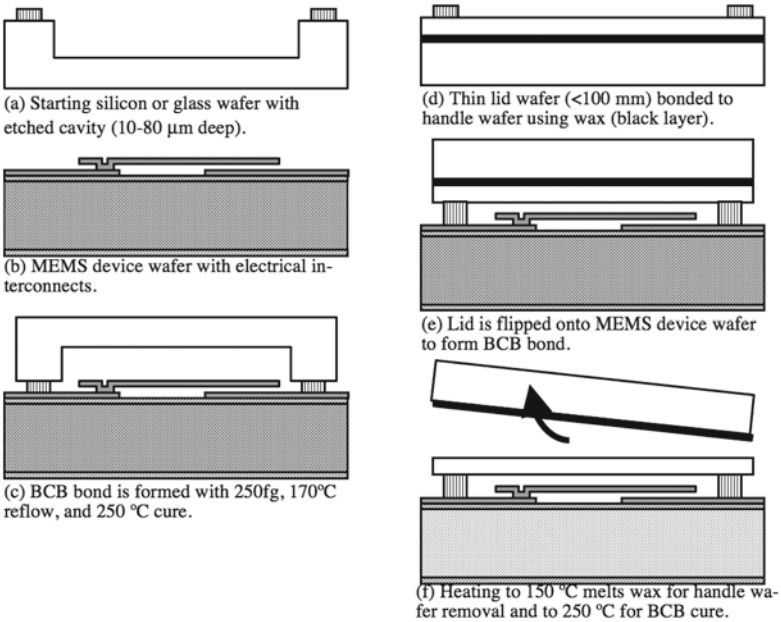

Fig. 11.19 BCB bonding for thick and thin wafers

A second example of low-temperature organic bonding for micropackaging is the microcap packaging process described by Pan [50]. In this process a silicon carrier wafer (100) is used as a lid form, which typically has a thickness of 525 μm with a 1.5 μm thick thermal oxide (Fig. 11.20a). The microcap form is etched into the silicon using a 30% wt solution of KOH at 70°C using the thermal oxide as an etch mask as shown in Fig. 11.20b. The thermal oxide etch mask is removed before a 1500 Å Ni seed layer and passivation layer are sputter deposited as shown in Fig. 11.20c. A thick photoresist is deposited and patterned for electroplating the thick Ni (15 mm) cap structure shown in Fig. 11.20d. In Fig. 11.20e, a photopatternable bonding material is deposited, solvents evaporated and developed, and the electroplating template is stripped. The cap wafer is now ready to be flip-chipped onto the device wafer as shown in Fig. 11.20f. The bond was formed using a combination of force, temperature, and materials. Once the bond is formed the carrier wafer is removed to leave the Ni cap bonded to the device wafer (Fig. 11.20g). The Ni seed layer passivation is needed to be able to separate the carrier wafer from the Ni cap.

The bonding strength was measured and found to be maximized between 80 and 120°C. SU8 had the highest bond strength rated at 213 kg/cm^2 and 90°C. Other bonding layers included AZ-4620 (86 kg/cm^2 at 90°C), SP-341 (100 kg/cm^2 at 90°C), and JSR (88 kg/cm^2 at 90°C). The bond strength increased with increasing bond force and the authors recommended a minimum bond force of 50 N. The glass

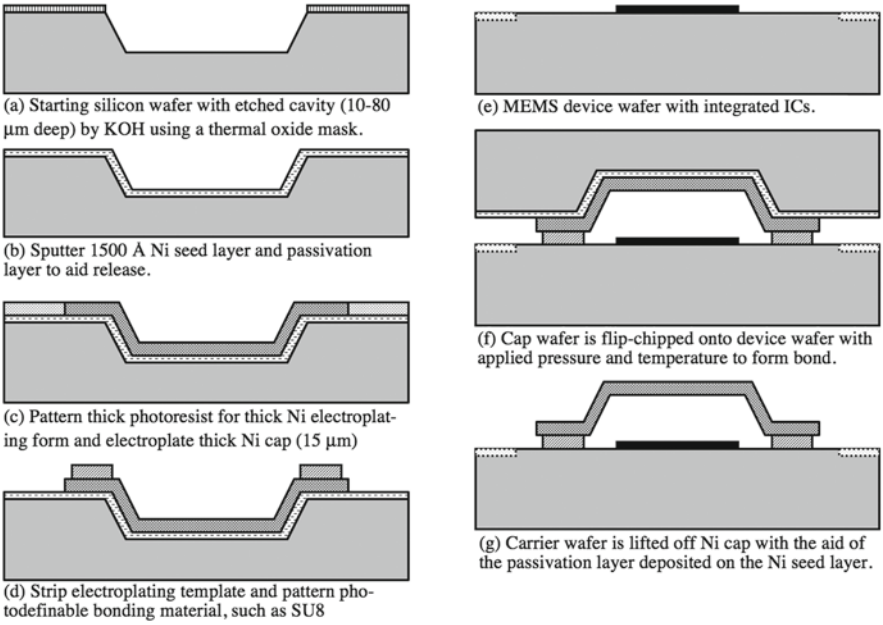

Fig. 11.20 Microcap packaging process using Ni cap and photodefinable bonding material

transition temperature of the bond material limits the bonding temperature from 115 to 180°C.

A final example of an encapsulation process using epoxy and other organic materials has been developed. The process begins with a completed MEMS device and substrate that can be 8–10 in. glass, silicon, or GaAs wafers. The MEMS device die is flipped (device down as shown in Fig. 11.21a) and bonded to Kapton film using a B-stage epoxy. The Kapton has a cavity to house the MEMS device and includes the transmission lines for the RF signals. At this point the MEMS die is encapsulated in polyimide. The polyimide is etched to create vias for interconnection of the RF I/O and DC control lines. The vias are metallized with Ti/Cu/Ti as shown in

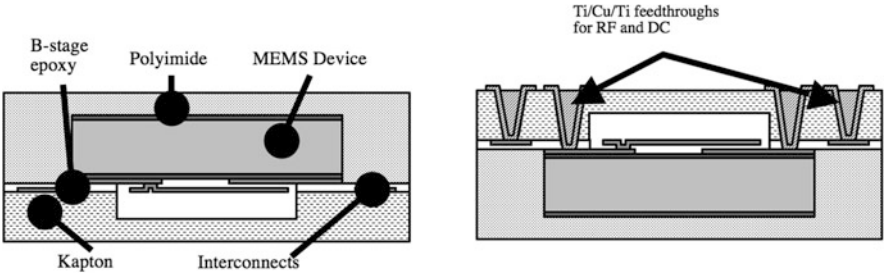

Fig. 11.21 Encapsulation process using Kapton, polyimide, and vertical feedthroughs

Fig. 11.21b. This process produced low-loss feedthroughs at <0.1 dB at 10 GHz. Finally, the polyimide encapsulated, Kapton substrate passed an 85% RH, 85°C, 10,000 h test with air bridges.

11.4 Direct Comparison of Wafer Bonding Techniques

The type of bonding that is used will be determined by many factors: materials, surface roughness and topography, temperature or pressure limitations, and product requirements. In Table 11.3, a summary of wafer bonding techniques is presented.

11.5 Bonding of Heterogeneous Compounds

The bonding of heterogeneous materials includes wafer bonding of lattice mismatched materials, which is important because these heterogeneous devices cannot be formed by other methods. Wafer bonding enables the integration of GaAs/InP, InP/Si [51], GaAs/Si, and GaAs/GaN. Eom et al. [52] have described the formation of YBa_2Cu_3. The integration of these heterogeneous structures has allowed the production of light-emitting diodes, vertical cavity lasers, avalanche photodiodes, vertical couplers, and heterojunction bipolar transistors (HBTs). It is possible to wafer-bond GaAs to another GaAs wafer or other material [53–55], which increases the technological opportunities. This provides the flexibility to design enhanced optoelectronic systems. The bonding of wafers to sapphire has been described by Kopperschmidt et al. [56] and the construction of strained layers is described by Taraschi et al. [57–59].

The bonding of GaAs wafers has been described by Akatsu et al. [60], who have pursued more moderate direct bonding conditions to improve the bonding process for GaAs. In a typical direct bonding process, high anneal temperatures are used to increase the bond strength between two wafers. But this approach with GaAs can compromise the integrity of the interface such that gallium or arsenic oxides may be enclosed by bubbles that form as part of the decomposition of absorbates. The high temperatures have been between 400 and 975°C for a few hours to 20 h in an inert or reducing atmosphere. Another issue with the high anneal temperatures is the thermal mismatch between dissimilar materials such as GaAs and silicon. The high mechanical load will cause structural damage and make it difficult to scale the process to whole wafers. Typical mechanical loads of up to 40 kg/cm^2 have been used.

A major challenge for GaAs bonding is cleaning the surfaces because of the complexity of removing the oxides of Ga and As at the same time. The native oxides of Ga and As exist on the wafer surface when exposed to air and coexist with carbon contaminants and absorbed water. The water can be removed by low-temperature heating and the oxides can be desorbed above 580°C. The carbon contaminants are not removed by thermal cleaning but can be removed by atomic hydrogen in an ECR (electron cyclotron resonance) plasma.

Table 11.3 Wafer bonding methods, conditions and applications

Wafer bonding method	Bonding conditions	Advantages disadvantages	Applications
Direct bonding	RT-1200°C No-small pressure	+ High bond strength + Hermetic + High temperature compatibility – High surface flatness requirements – High temperature incompatible with integrated CMOS process	SOI wafer fabrication Heterogeneous structures
Anodic bonding	150–500°C 200–1500 V Electrostatic pressure No mechanical pressure	+ High bondstrength + Hermetic + Resistant to high temperature – Bond temperature and high voltage are not compatible with CMOS wafers	Sensor packaging and fabrication
Solder bonding	150 – 450°C Low bond pressure	+ High bond strength + Hermetic + Compatible with CMOS wafers – Solder flux	Flip-chip bumping Hermetic sealing
Eutectic bonding	200–400°C Low to moderate bonding pressure	+ High bond strength + Hermetic + CMOS compatible – Native oxide sensitivity	Hermetic sealing
Thermocompression bonding and metal–metal bonding	350–600°C 100–850 MPa (high bond pressure)	+ Hermetic + CMOS compatible – High bonding pressure – High surface flatness	Hermetic sealing Wire bonding Flip-chip bumping 3-D ICs
Ultrasonic bonding	RT – 250°C High bond pressure	+ CMOS compatibility – Only small bond area demonstrated	Wire bonding
Low temperature melting glass bonding	400–1100°C Low–moderate bonding pressure	+ High bond strength + Hermetic – CMOS compatibility	Hermetic sealing
Adhesive bonding	RT–400°C	+ High bond strength + Low bond temperature + Substrate material diversity + CMOS compatible – Not hermetic – Temperature stability	3-D ICs Temporary bonding MEMS packaging

The cleaning of GaAs wafers begins with the desorption of arsenic oxides by heating to produce a Ga-rich surface. The arsenic oxide can be removed by the heating but also by the hydrogen cleaning. The hydrogen cleaning follows the process $As_2Ox + 2xH\cdot \rightarrow xH_2O \uparrow + As_2(1/2\ As_4) \uparrow$, where $x = 1, 3,$ or 5 representing the various arsenic oxides. The Ga oxide is decomposed in the following process $Ga_2 + 4H\cdot \rightarrow Ga_2O(\uparrow) + 2H_2O \uparrow$. The remaining Ga_2O is volatile at temperatures above 200°C but temperatures above 350–400°C are preferred so the Ga_2O is reliably desorbed. In Table 11.4, a preferred direct bonding process is provided. The preferred process of Table 11.4 includes the thermal cleaning with atomic hydrogen and a low bonding temperature of 150°C. When the wafers were thermally cleaned (400°C for 30 min) in a H_2 or UHV (ultrahigh vacuum) process, the wafers had low bond strength or formed no bond with a bonding temperature of 350°C.

Table 11.4 GaAs direct bonding process

Process step	Process parameters
Wafer cleaning	Thermal and hydrogen clean >350°C
Cleaning time	30 min
Bonding temperature	150°C
Bonding force	0 N/m^2
Bond energy	0.7–1.0 J/m^2

11.6 Wafer Bonding Process Integration

11.6.1 Localized Wafer Bonding

A key requirement of the bonding process to achieve a strong and hermetic bond is the temperature. In a conventional bonding process the entire wafers (substrate, lid, and interface) are raised to a uniform temperature. The temperature depends on the process: 1000°C for silicon-to-silicon fusion bonding, 300°C for silicon-to-glass anodic bonding, 363°C for Au–Si eutectic bonding, or 450°C for glass frit bonding. These temperatures are too high for many MEMS material systems or when the MEMS process includes integrated electronics. The integration of MEMS and CMOS using wafer bonding has been described by Farrens et al. [61], Lin et al. [62], Parameswaran et al. [63], Sedkey et al. [64], Van der Groen et al. [65], Frazier [66], and Ghodssi et al. [67]. This means the global temperature of the bonding process needs to be lowered or that the high temperature needed for bonding should remain localized to the bonding interface so that temperature-sensitive structures are not heated to a high temperature. In this section, we discuss the processes that have been developed with localized heating and bonding to encapsulate MEMS devices. Cheng et al. [68–70] describe both direct and indirect localized heating and bonding. In direct bonding, the heater material also acts as the bonding and sealing material [71–74]. In indirect bonding, the heating element is preserved during the heating

and bonding process because a separate material is used as the bonding and sealing material [75].

Cheng et al. [68, 70] have demonstrated localized silicon fusion bonding between an insulated silicon substrate and a glass wafer (7740 Pyrex). The insulated silicon substrate will contain the MEMS devices and could contain integrated electronics. Electrical and thermal isolation are provided on the silicon substrate by a nominal 0.8 μm silicon dioxide layer. For fusion bonding, polysilicon is used as the microheater and seal material. It is nominally 1.0 μm thick, 5 μm wide, and forms a closed ring that defines the bond region. Two electrical taps are made from the microheater to provide connection to the current source. The microheater is provided an input current of 31 mA to develop a local temperature of about 1300°C, which is above the Pyrex softening point of 820°C and close to the polysilicon melting point. This process takes about 5 min and is performed with a 1 MPa pressure applied to the parts. In a conventional fusion bonding process, where the entire substrate is heated, the bonding temperature is typically over 1000°C for approximately 2 h. In a second experiment Cheng et al. [68] found that raising the local temperature to 1000°C for 30 min, when the current was 29 mA resulted in a bond of lower strength and quality.

In addition, Cheng et al. [68, 70] demonstrated a localized Au–Si eutectic bonding process between the insulated silicon device substrate and a silicon lid. In this case, the microheater material was Au, and 5 μm wide and 0.5 μm thick. It is provided a current of 0.27 A for 5 min, which raised the local temperature to an estimated 800°C. During the bonding process, the Au diffused into the silicon to form the bond and seal. The diffusion and solubility of Au in Si increase with increasing temperature. The local heating process provides a higher temperature (800°C) than a more conventional Au–Si eutectic process performed at about 410°C for 20 min. The local heating process was shown to provide a more uniform, higher strength, and higher quality bond than the conventional process.

11.6.2 Through Wafer via Technology

Why are we discussing through wafer via technology in this chapter on wafer bonding? The answer depends on the reason for using the wafer bonding process. If the wafer bonding process is being utilized to fabricate a heterogeneous wafer stack, such as SOI or InGaAs/Si, or to transfer one thin-film to another wafer or heterogeneous wafer stack then the through wafer via technology does not need to be considered, which is not to say that the through wafer via technology does not apply to these heterogeneous wafers. The through wafer via technology should be considered whenever electrical connections are required for a multitude of active electrical devices. We discuss the important considerations when integrating wafer bonding and through wafer vias (TWV), which have been referred to as TSV (through silicon via, which is rather limiting) and TWI (through wafer interconnects).

Why are we developing through wafer interconnect technologies? One reason is to increase the density of devices on the MEMS substrate. One of the reasons for

developing through wafer interconnects is to achieve high-density interconnections with a smaller footprint. This is because the dies rapidly become bond pad limited or wire bond limited, if all of the bond pads are placed at the perimeter of the die. With the through wafer interconnects, the electrical connection can be made directly to the bottom of the MEMS device for the purpose of actuation or to the RF ports of the RF MEMS component. The die can now be directly bonded to a substrate using a solder reflow or thermo-compression process.

Another case for through wafer interconnects was described in the Ford Microelectronics process, which describes perimeter bond pads that are exposed by wafer dicing following the wafer-level encapsulation process. The wafer saw exposure of the bond pads is eliminated by using the through wafer interconnect technology. A second reason is reliability. The through wafer interconnect process is associated typically with a wafer-level encapsulated MEMS device. Because of the through wafer interconnect process, the MEMS device is protected during any and all backend processes, such as wafer saw, wafer grinding, plastic encapsulation, flip-chip mounting and underfill, solder reflow, shipping, and handling. This means fewer opportunities to introduce contaminants (e.g., photoresist protect films and other particles).

As discussed previously, the electrical interconnects or transmission lines can be fabricated across the wafer and pass through a space defined as the bond/seal region between the substrate and the lid or can be fabricated through the wafer as described in this section. The through wafer interconnects take on two basic configurations. The first configuration fabricates the TWI through the substrate upon which the MEMS devices are built. This process in theory can be implemented by fabricating the TWI before or after the MEMS fabrication. The second configuration fabricates the TWI through the lid wafer. In this latter case, the TWI can be fabricated before or after the lid is bonded to the device wafer. Whether the TWIs are fabricated through the lid or the substrate, there are many different ways to implement the various processes.

Surface interconnects/transmission lines pose many challenges beyond the simplicity of their deposition and patterning. The first challenge is topography created by the interconnect that may have a thickness of 0.5 μm for a standard CMOS AlCu layer. The topography poses greater challenges for the direct bonding methodologies because these require low topography and low surface roughness. The topography will need to be addressed by the deposition of a dielectric film to encapsulate the electrical interconnect. In a subsequent step, a chemical-mechanical polishing is performed to eliminate the topography of the interconnect. The next step is the preparation of the polished surfaces and finally direct bonding of the wafers. Because the interconnect will be encapsulated in a dielectric material for electrical isolation from the bonded wafers, this will determine the selection of dielectric materials and the selection of the direct bonding technique. The surface topography is more easily addressed by wafer bonding with intermediate layers, which will eliminate the need for planarization by CMP. If the intermediate layer is a dielectric, such as a glass frit, polymer (BCB), or adhesive, the intermediate layer will provide the dielectric isolation between the interconnect and the bonded wafer.

If the intermediate layer bonding is based on a metal eutectic or a solder, the topography will need to be addressed in a similar manner. Solder bonding will accommodate the surface topography easily, but the solder will form an electrical contact to the interconnect unless it is encapsulated in an insulating layer. In some cases it may be desirable to form an electrical contact to the seal ring such as grounding the seal ring for some RF applications. If electrical isolation is required, the interconnects can be encapsulated in an insulating film that is planarized as we described for the direct bonding process. This process sequence will be required for intermediate bonding by eutectic formation, because the eutectics (e.g., Si–Au) do not accommodate the surface topography. If the interconnect is encapsulated in the dielectric it is still possible to form an electrical connection of the conductive seal ring by forming a short via through the thin dielectric to the interconnect.

The second challenge for surface interconnects is the electrical isolation or contact, which has been described in the previous paragraph as part of the solution to bond over the surface topography.

The third challenge is the formation of an hermetic seal because it is possible the interconnect will provide a leakage path, moisture, or gas. It is important that the dielectric isolation layer, solder, or glass frit form a conformal coverage of the interconnect topography, which means an absence of voids parallel to the interconnect sidewall between the sidewall and the intermediate layer.

The fourth challenge is the exposure of the electrical contact pads for wirebonding or solder bumping. This process has been described earlier as part of the Ford Microelectronics process. This involves providing a cavity on the bonded wafer that aligns to the electrical pad on the base wafer. Once the bond is formed the pads can be exposed by the use of a wet chemical etch, a plasma etch, or DRIE, or by saw exposure. These have all been used successfully, but the DRIE and sawing enable a well-controlled high-aspect-ratio exposure. The wet etch is usually isotropic which leads to very large pad openings and therefore die.

We have described electrical interconnects that are patterned on the surface of the wafer and through the bonded area and that are fabricated through the wafer. We next describe the similar challenges that relate to TWIs that are fabricated through the device wafer or through an encapsulation wafer. The first challenge of surface interconnects is the surface topography, which is not a typical challenge for the TWIs. The second challenge is the electrical isolation of the TWIs. The isolation of the TWI from the bonded wafer or seal ring is easily accomplished by blanket dielectric films that may not require CMP. If it is necessary to connect a TWI to a conductive seal ring, this can be fabricated with a short damascene via described above. The isolation of the TWI from the via sidewalls is often accomplished by deposited dielectric that provides the best isolation for a greater thickness. Because the dielectric constant (4 for silicon oxide) is relatively large, the coupling can be high depending on the thickness. Air isolated TWIs have been developed, that replace the silicon oxide with air that has a dielectric constant of approximately 1. The air isolated TWIs will reduce parasitic capacitance coupling by a factor of 4.

A through wafer interconnect process was developed at Stanford so that they could create a high density array of cantilevers as demonstrated by Chow et al. [76].

Without the through wafer interconnects, the cantilever density is limited because of the need for area to place bond pads and route electrical interconnects. Additional goals included flip-chip integration of MEMS device die and integrated circuit die, low parasitic capacitance using reverse-biased PN junctions, and low resistance achieved with high-conductivity polysilicon.

This process was demonstrated on 400 μm thick n-type, <100> silicon wafers. A 2 μm thick thermal oxide is used as a mask on both sides of the wafer for etching the through wafer vias (Fig. 11.22a). The deep silicon etch is performed by etching halfway through the wafer from both sides. In this manner, it is possible to achieve a via with a 20:1 aspect ratio (Fig. 11.22b). With the oxide mask remaining in place, the silicon is boron doped to fabricate a pn-junction (Fig. 11.22c). Next, the vias are filled with polysilicon (Fig. 11.22d) that is etched back to clear the oxide via mask and the vias (Fig. 11.22e). The oxide is repatterned to form boron doped junctions on the front and back surfaces of the wafer. After the oxide mask is etched, a mask pattern is used to form isolated ohmic contacts by implanting phosphorus (Fig. 11.22f). The fabrication process is completed by liftoff patterning of Au contacts on the doped junctions (Fig. 11.22g).

In this process, they were able to achieve a 0.05 pF parasitic capacitance with a reverse-biased (10 V) pn-junction. This compares to 0.28 pF for a metal-insulator-semiconductor (MIS) isolation system. The series resistance was 900 Ω and the leakage current was measured to be 7 nA.

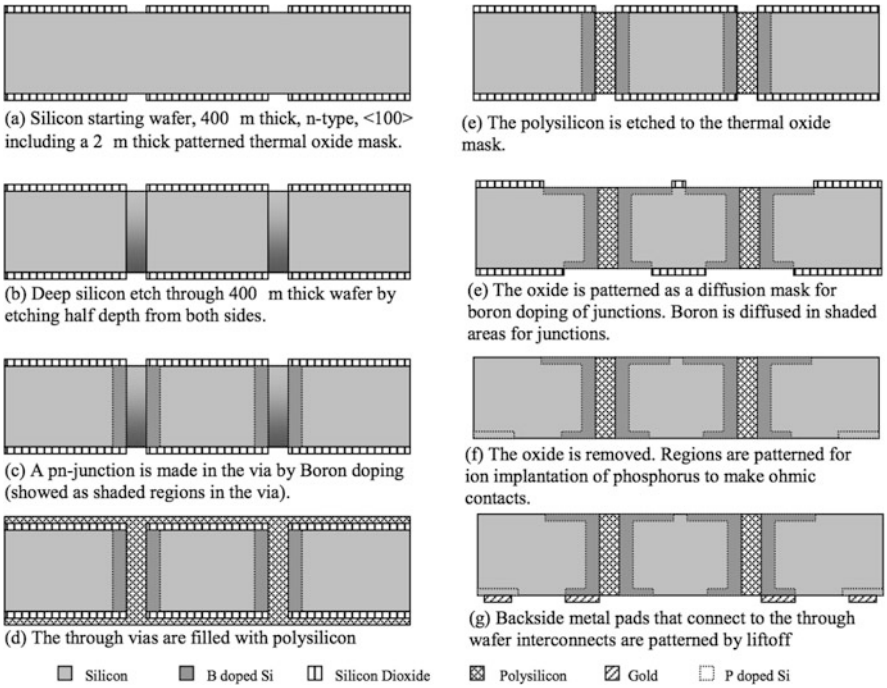

Fig. 11.22 Through wafer interconnect fabrication process using isolated polysilicon vias

A second through via process used a high-density low pressure (HDLP) SF_6/C_4F_8 plasma to create via holes through a p-type, 4 in., 525 μm thick, 10 Ω cm, double-side polished silicon wafer. The via holes were square with dimensions of 30 μm/side, which resulted in an aspect ratio of 17.5:1. A 1 μm thick thermal oxide was grown at 1100°C for an isolation layer. A 1.5 μm thick low pressure chemical vapor deposited (LPCVD) polysilicon was deposited as an adhesion layer for a subsequent copper layer that had poor adhesion to the thermal oxide. Next a 250 nm CVD copper layer was deposited as a seed layer for the 6 μm thick electroplated copper. The through wafer interconnect resistance was further reduced by the 6 μm thick electroplated copper with a sheet resistance of 2.8 mΩ/cm. This process resulted in vias with ultralow resistance of 50 mΩ/via.

Following the thick Cu deposition, a 7 μm thick photoresist (Shipley PEPR 2400) was electroplated for the subsequent patterning of the Cu and polysilicon. The Cu and polysilicon were wet etched and dry etched in SF_6 plasma, respectively. Finally the electroplated photoresist was removed to expose the isolated vias.

The process used to develop through wafer interconnects for MEMS applications is based on etching high-aspect-ratio holes through the silicon wafer, depositing an insulation layer, and depositing a conductive layer. The insulation layer will provide electrical isolation of the conductive vias from the silicon wafer.

It was demonstrated in a process with 50, 75, 100, and 200 μm diameter vias through a 525 μm thick 4 in. p-type, <100> silicon wafer. The vias were patterned with a thick photoresist (AZ 4620 at 20 μm thick, and AZ 400 K developer) (Fig. 11.23) and etched with a deep inductively coupled plasma etcher (Fig. 11.23b). Then PECVD silicon dioxide was selected for the isolation layer (Fig. 11.23c). It was deposited by sputtering because of the improved step coverage. The silicon

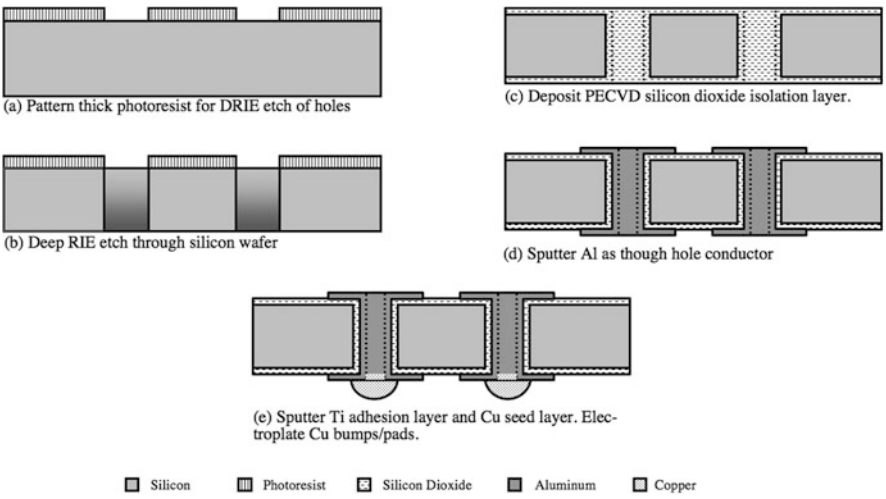

Fig. 11.23 Through wafer via process

dioxide was deposited to approximately 7000 Å, which is difficult to measure on the sidewalls because of the surface roughness.

The conductive layer was demonstrated by two approaches. In the first approach, a thin aluminum was sputtered from both sides of the wafer to achieve 1 μm on the surface and approximately 2000 Å on the sidewall (Fig. 11.23d). In the second approach, copper was electroplated as the conductor. This required 1500 Å of titanium to be deposited first as an adhesion layer between the copper and the silicon dioxide. The copper and titanium patterning was completed by etching in $H_2O(80\%) + H_2SO_4(10\%) + H_2O_2(10\%)$ and in $H_2O(90\%) + HF(10\%)$ to remove the copper and titanium, respectively (Fig. 11.23e).

The primary goal of the next process (Fig. 11.24) was to improve the resistance and parasitic capacitance of through wafer interconnects. The improvements are in direct comparison to the dielectric isolated metal or polysilicon and to the pn-junction, reverse-biased through wafer interconnects. The improvements will come from air gap isolated interconnects.

The process begins in a typical fashion for etching deep high-aspect-ratio vias through a silicon wafer. First, a 1.2 μm thermal oxide is grown and patterned to be used as deep silicon etch mask (Fig. 11.24a). Also, the thermal oxide provides isolation between the metallized via and the silicon substrate. In addition, a thick

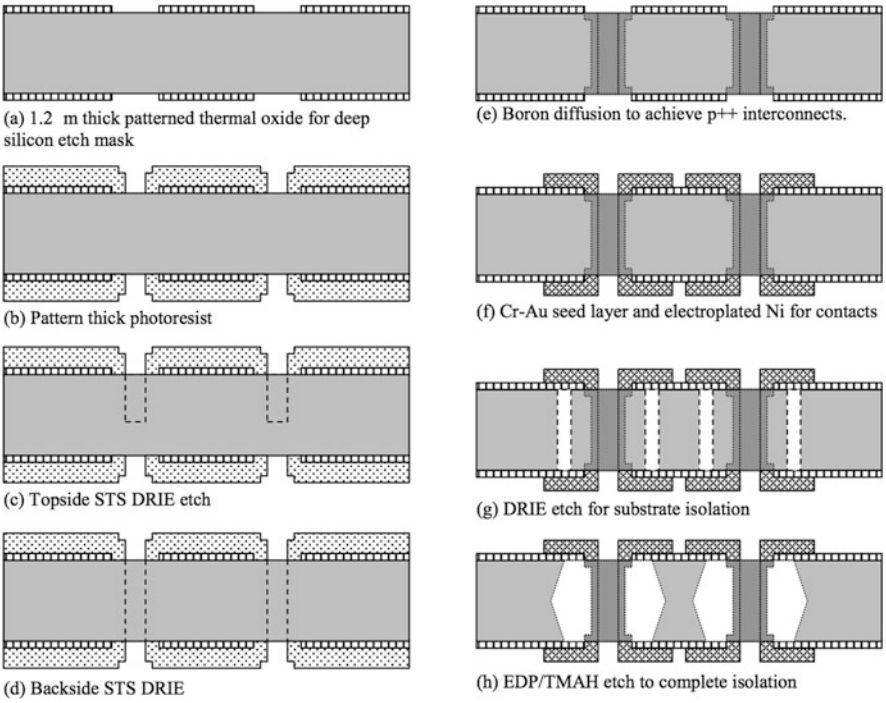

Fig. 11.24 Air isolation TWI process

photoresist (16 μm AZ9260) is deposited and patterned as the deep silicon etch mask (Fig. 11.24b). Similar to other processes, the deep RIE is performed from the topside and backside to define a high-aspect-ratio through wafer via (Fig. 11.24c,d). The topside and backside etches were both targeted for 150 min to etch 250 μm deep. Following the via etch, the thick photoresist is stripped.

The via interconnects are fabricated by doping the via silicon with boron during a 6 h diffusion process that produces a 12–15 μm p++ region (Fig. 11.24e). The next steps are associated with fabricating metal electrical contacts to the p++ interconnect (Fig. 11.24f). First, a Cr–Au seed layer is deposited for electroplating an 8–10 μm thick Ni contact layer. An alternate DRIE is performed to create isolation between the p++-doped interconnect and the substrate (Fig. 11.24g). The isolation is enhanced by an anisotropic wet silicon etch (EDP, TMAH, or KOH) to complete the air gap isolation (Fig. 11.24h).

The University of Michigan design/process achieved a 27 Ω series resistance (this compared to calculated 4. Ω series resistance that was attributed to necking of the doped interconnect) and a 10 fF parasitic capacitance. The parasitic capacitance is dominated by the Ni contact frames that couple to the silicon substrate through the 1.2 μm thick oxide.

11.7 Characterization Techniques for Wafer Bonding

The characterization of the wafer bond is either destructive or nondestructive. Nondestructive techniques include imaging techniques to examine the bond interface or to evaluate voids in the bond interface that are distributed across the wafer. Destructive techniques include cross-section analysis and bond strength evaluation. The nondestructive techniques can be used as an in-process or end-of-line evaluation. The destructive techniques are used at end-of-line. The assessment of bond quality includes defect rate, bond strength, stresses [77], bond energies [78], hermeticity (if used for packaging), materials, and harsh environments [79].

The nondestructive imaging techniques include optical microscopy, infrared microscopy, acoustic microscopy [80], white light interferometry, secondary ion mass spectroscopy (SIMS), transmission electron spectroscopy (TEM), multiple internal reflection spectroscopy [81], and X-ray topography. Optical microscopy will require one of the wafers to be optically transparent so that defects, voids [82, 83], and contaminations can be identified through one wafer to the interface. Optical microscopy is an efficient and inexpensive means of inspection. The infrared imaging mounts the bonded wafers (transparent to IR such as silicon) above an IR source and in the path of an IR-sensitive camera. Interfacial bond defects will show up as changes in contrast in the IR image and appear to have a “Newton’s rings” pattern. The resolution of this technique is limited to about $^1/_4$ of the wavelength of the IR source. For the typical source this resolution is several mm. This technique will not identify voids that are identified by other techniques. IR imaging resolution is further limited by high doping levels, IR absorbing films, and by rough surfaces.

The advantage of IR imaging is its speed, simplicity, and low cost to implement and perform. The increased resolution is obtained at the expense of cost and speed.

Ultrasound or acoustic microscopy uses the propagation properties of a sound wave in the bonded materials. The measurements are made in water or other liquids and are relatively expensive to make. The propagation and scattering of the acoustic wave depends on the elastic properties of the materials, which distinguishes the bonded wafers and any voids that are present. The measurement resolution of the acoustic microscopy depends on the measurement frequency but it is in the range of 10 μm.

X-ray topography is an expensive and time-consuming method when compared to other techniques that are used to image cross-sections to examine distortion or defects in lattice planes. It is applied to single crystalline materials and has a typical resolution of 2–20 μm.

Two destructive techniques include interface etching [84] and cross-sectional analysis. With interface etching, one wafer is sacrificed by etching until the interface or selective etch stop is reached. Once the interface is reached, voids and defects can be visually inspected. This is a common approach with SOI wafers. Cross-sectional analysis is usually performed in conjunction with a scanning electron microscope (SEM) or transmission electron microscope (TEM) to image the bond interface. For access to the bond interface the wafers are cleaved to expose the bonded interface by using a focused ion beam (FIB). The image of the bonded interface can be further enhanced by a defect etch to enhance the void.

Bond strength characterization is measured by a number of techniques that include the pressure burst test, tensile test, shear test, bending test, and the razor blade test (knife edge test). The tensile and shear tests are performed on prepared samples of a specific area. The tensile test uses mounts to the two wafer surfaces to load the sample perpendicular to the bond interface. The maximum load at failure or the maximum stress, which is the maximum load divided by the sample area, is used as the failure criterion. The shear test is similarly constructed but the load is applied to the two wafers so that it acts parallel to the bond interface. The shear failure is characterized by the maximum shear load or by the maximum shear stress, which is the maximum shear force divided by the bond area tested.

The tensile/shear test has certain challenges relative to implementation and characterization. The first challenge is the isolation of loading conditions. Without due care and even with due care, it is possible to have torsion and bending loads that are superimposed on the tensile (shear) load. The superposition of these and other loading stated causes the sample to fail differently and at a lower load compared to the simple tensile load. The second challenge is stress intensifiers that increase the stress locally during the tensile test. It is the local maximum stress rather than the area averaged stress that leads to failure and propagation of an interface crack. A third challenge is the characteristics of the failure that include the propagation of the failure. If the crack propagates into one of the wafers or travels some distance along the bond interface then turns into one of the wafers, it is not directly measuring the strength of the bond.

The knife edge test uses a blade of specified thickness that is inserted directly into the bond interface where a crack has been initiated. As the blade is inserted the length of the opening between the two wafers (crack length) is measured using an imaging technique to estimate the surface energy from the blade thickness, crack length, and elastic modulus of the wafers. The surface energy scales as the fourth power of the crack length; that is, uncertainties in crack length are magnified fourfold. The crack length has been observed to be time- and humidity-dependent so conditions must be carefully monitored. One challenge of the knife edge test is using it to characterize a strong bond where it is difficult to insert the knife edge without a crack propagating into one of the wafers (chipping).

The four-point bending test is performed on a sample that has a precrack started in one of the wafers. The precrack can be started by etching or sawing. When the sample is loading under four-point bending conditions, the precrack is expected to propagate into the weak interface of the bond. The load versus displacement is used to calculate the elastic energy and the surface energy of the bond.

Quantitative approaches have been developed through shear and tensile testing of bonded dies (Nese and Hanneborg [85], Obermeier [86], DeReus and Lindahl [87], Kubair and Spearing [88], and Tatic-Lucic et al. [89]) or burst pressure testing of bonded cavities (Stratton et al. [90]). Niklaus et al. [9] reviewed these techniques for the evaluation of adhesive bonds. These tests usually result in the load or pressure at failure, which is not broadly applicable as a failure criterion because it depends on the specimen size, geometry, and type of loading. Although the loading conditions are simple, the stress state at the interface corner where fracture initiates, is quite complex. This complexity of the interfacial loading has been argued by Madou [91] to be a negative attribute of the tests because they fail to "yield information about the detailed nature of the bond." Another approach, the blasé test, is used to determine the interface surface energy. It was argued by Madou [91] to be advantageous because it creates a well-defined interfacial loading.

In the blade test (Maszara et al. [92]), a thin blade is inserted into the interface between two bonded wafers to propagate a crack. The blade test was approximated by replacing the blade with patterned lines of varying pitch as demonstrated by Tatic-Lucic et al. [89]. The elastic energy in the system is varied and correlated with the surface energy required to produce a bond within the spaced lines. Based on the extracted bond surface energy, the differences between different process variations have been compared.

Elastic interface fracture mechanics applied to the fracture of silicon–glass anodic bonds was attempted by Hurd et al. [93], and Go and Cho [94]. The application of interface fracture mechanics is based on a crack propagating along the interface. One challenge of interface fracture mechanics is the resulting crack does not propagate along the interface, but turns away from the interface into the glass. Another anodic bond fracture specimen was demonstrated by inserting a thin metal blade between the silicon and glass prior to bonding [94]. In each case, an attempt was made to apply interface fracture mechanics, but this was problematic and not valid because often the crack does not propagate along the interface. Chen et al.

[95] have examined the effect of morphology on bond strength for copper wafer bonding.

Another approach is to correlate fracture initiation at the silicon–glass interface corner with a critical value of the stress intensity calculated from a linear elastic stress analysis. In the spirit of the interface fracture mechanics this approach is intended to be universal (independent of bond size) and can be used to design a variety of different reliable bonds. It is guided by application to adhesively bonded butt joints (Reedy and Guess [96–98]), homogeneous acrylic (Dunn et al. [99]), and etched silicon microstructures (Suwito et al. [100]). This approach is valid for other homogeneous or heterogeneous wafer bonded structures that are produced using any of the processes described previously as proposed by Dunn et al. [101], Labossiere and Dunn [102], and Labossierre et al. [103].

11.8 Existing Wafer Bonding Infrastructure

In his 1998 review, Schmidt [10] saw the primary driver for wafer-to-wafer bonding to be the enablement of wafer-level packaging followed by the fabrication of microstructures and the fabrication of heterogeneous starting wafer material. In the meantime one might add the emerging need of 3-D IC integration, such as for high-density memories. Schmidt [10] outlined several areas where continued progress was needed in order to realize the full potential of wafer-to-wafer bonding. One of these areas was to have a healthy infrastructure of equipment vendors and bonding services that supply wafer bonding equipment solutions.

In the meantime, there is such a infrastructure available. For beginning R&D purposes one can choose wafer bonding services to test the feasibility of a MEMS fabrication process that requires wafer bonding. We provide a list for such services in Section 11.8.1. Several tool vendors are available that provide state-of-the-art wafer bonding tools. Most equipment offered provides an automatic/robotic interface for handling wafers and automatic wafer-to-wafer alignment, the automatic contacting of the wafers, and the recipe for a process in terms of pressure, voltage, temperature, time (ramp up, hold, ramp down, anneal), and ambient environment (vacuum, dry nitrogen or other inert gas). In Section 11.8.2 we provide an overview of available wafer bonding tool vendors and discuss some aspects of their systems.

11.8.1 Wafer Bonding Services

Table 11.5 Wafer bonding service providers

Company information	Principle services
Applied Microengineering, Ltd. 173 Curie Ave Didcot Oxfordshire OX11 0QG United Kingdom www.aml.co.uk	Wafer Size: 50–200 mm Processes: FB, AN, AB, DS, MM, TC Materials: Silicon, CW, Glass
Dalsa Semiconductor 18 Airport Blvd. Bromont, Quebec, Canada J2L 1S7 www.dalsasemi.com	Wafer Size: 100–150 mm Processes: FB, AB, DS, MM, TC Materials: Silicon, Glass, CW, CMOS
Innovative Micro Technology 75 Robin Hill Road Santa Barbara, CA 93117 www.imtmems.com	Wafer Size: up to 150 mm Processes: FB, AN, AB, TC, Eutectic, Glass Frit Materials: Silicon, Glass TWV: Yes
Integrated Sensing Systems (ISSYS) 391 Airport Industrial Drive Ypsilanti, MI 48198 www.mems-issys.com	Wafer Size: 100–150 mm Processes: FB, AN, DS, Glass Frit Materials: Silicon, Glass
Silex Microsystems Bruttovägen 1, SE-175 26 Järfälla, Sweden www.silexmicrosystems.com	Wafer Size: 150 mm, 200 mm Processes: FB, AN, AB, DS, TC Materials: Silicon, Glass TWV: Yes
Ziptronix Inc. 800 Perimeter Park Dr., Ste B Morrisville, NC 27560 www.ziptronix.com	Wafer Size: to 300 mm Processes: FB, Materials: Silicon, CW

11.8.2 Bonding Tool Vendors

In addition to existing wafer bonding services (Table 11.5), there is a healthy infrastructure of wafer bonding vendors available from which to choose. We have identified four companies that sell state-of-the-art bonding tools. Thus, there is a multifaceted product portfolio available. Depending on the needs for academia or industry, one can choose from manually operated tabletop systems up to fully automated systems that perform cleaning, surface activation, wafer alignment, and bonding including postbonding inspection (IR), in a closed environment inside the bonding tool itself. Almost every tool supports all bonding methods that we have

discussed in the previous sections for various substrate sizes, but there are different aspects in specialties of each of these tools. To give a first overview, we briefly introduce these companies (in alphabetical order) with some examples and aspects of their tools. Each company provided photos for the shown figures, company descriptions, and tool specifications for that purpose.

11.8.2.1 Applied Microengineering Ltd (AML), UK

The company AML offers wafer bonding machines (Fig. 11.25a) capable of in situ alignment under vacuum and elevated temperature, surface activation, and bonding. The target markets are the MEMS, IC, and III-V industries. The tools offer high throughput, because pumpdown, heating, and alignment are performed in parallel, speeding up the bonding time per wafer.

The supported wafer sizes range from 2 to 8 in. The alignment tolerance is specified to be 1 μm and the unique XYZ-Theta alignment mechanism (Fig. 11.25b,d) allows a large distance between the bonding surfaces before the bond (surface activation and outgasing) without contacting the surfaces with flags or spacers.

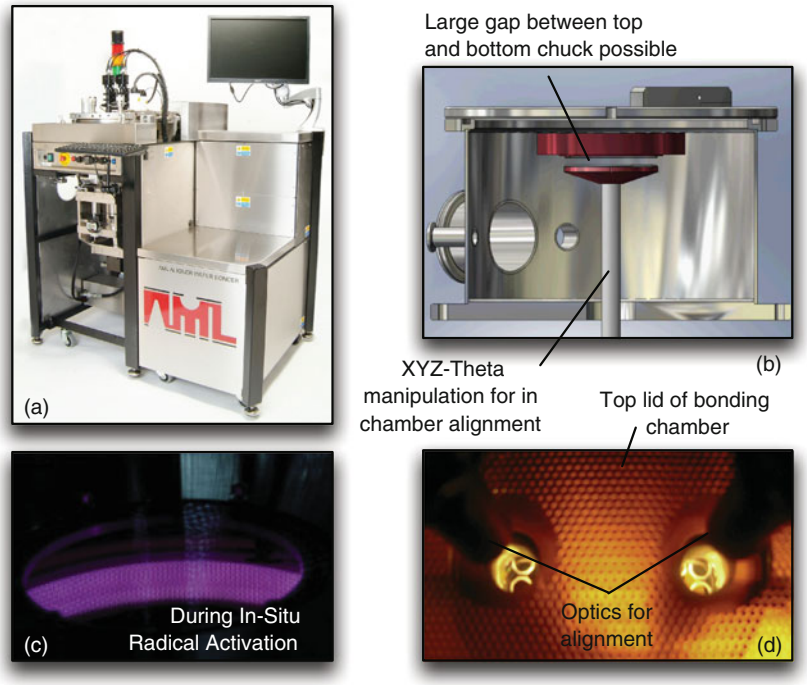

Fig. 11.25 (**a**) AML's versatile wafer bonding platform (2–8 in.), which features alignment, activation, bonding, in situ UV curing, all in the same chamber without any handling steps between. (**b**) Bonding chamber from inside. (**c**) Tool during in situ radical activation for room temperature bonding; (**d**) Alignment optics (cameras) (Photos and drawings courtesy of Applied Microengineering Ltd. (AML), UK)

Upgrades for in situ radical surface activation, featuring room temperature direct bonding, are available (Fig. 11.25c), as well as the capability of in situ high-accuracy alignment with UV cure using UV LED array inside the chamber. Another upgrade is available for polymer embossing, imprinting, NIL, and other pattern transfer techniques. The machines have the flexibility for R&D and the throughput and automation for volume production as well. All wafer bonding types are supported. Stacks of up to 8 mm can be bonded.

11.8.2.2 EV Group (EVG), Austria

The company EVG offers several types of wafer bonding tools for the MEMS, 3-D–IC integration, and advanced packaging, as well as the compound semiconductor industries. The systems accommodate the demanding applications by bonding under high vacuum, precisely controlled fine vacuum, temperature or high-pressure conditions. EVG's tools support a wide variety of bonding processes such as anodic, thermocompression, glass frit, eutectic, diffusion, fusion, solder, adhesive, and UV bonds. Based on a modular bond chamber design, the systems can be configured for R&D, pilot line, or high-volume production.

A maximum level of automation and process integration is achieved by EVG's GEMINI® platform (Fig. 11.26). The automated production wafer bonding systems

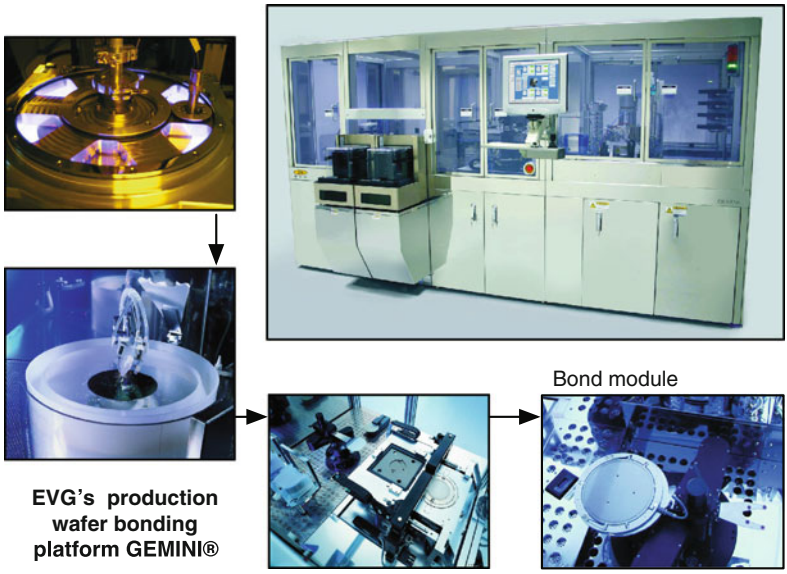

Fig. 11.26 The GEMINI® is EVG's production wafer bonding platform with up to four bond chambers for high throughput. The system is also available with more than four bond chambers and it supports wafer sizes up to 300 mm. The wafers first go through wafer surface preparation modules (plasma and cleaning), then to the SmartView® face-to-face-bond alignment module before the wafers are loaded into the bond chamber (bond module) (Photos courtesy of EV Group (EVG), Austria)

for high-volume applications support wafer-to-wafer alignment and wafer bonding processes with up to four bond chambers in parallel for high throughput. EVG's patented SmartView® face-to-face-bond aligner and various preprocess modules for wafer sizes up to 300 mm are available. Furthermore, for postbonding inspection compatible metrology equipment, such as IR inspection, is offered as well. EVG introduced and focuses on the concept of separation between wafer alignment and bonding.

11.8.2.3 Mitsubishi Heavy Industries Ltd. (MHI), Japan

The target market of Mitsubishi's latest 200 mm bonding tool (Fig. 11.27a) is the integration of CMOS and MEMS wafers. The tool allows performing direct bonding at room temperature for various material combinations, as illustrated by the examples shown in Fig. 11.27b–i.

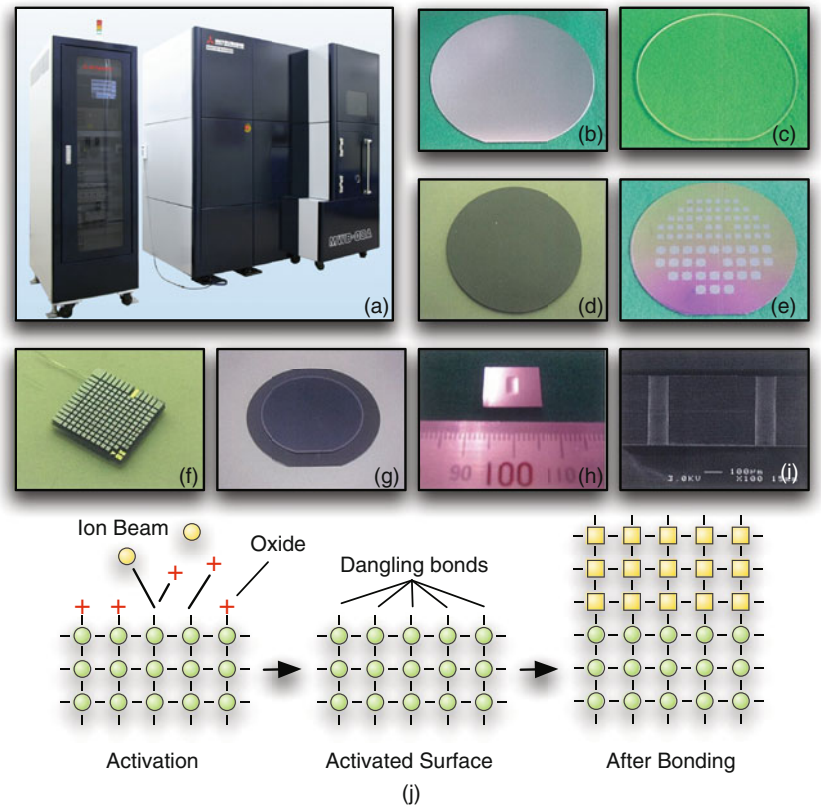

Fig. 11.27 (**a**) Mitsubishi's MWB-08A fully automated room temperature bonding machine for 8 in. wafer. Examples: (**b**) Si–Si; (**c**) Quartz–quartz; (**d**) GaAs–GaAs; (**e**) MEMS device; (**f**) Au–Au; (**g**) LiNbO3–Si; (**h**) vacuum leak test sample; and (**i**) Al TSV bonding. (**j**) Operation principle of room temperature bonding with ion beam under high vacuum conditions (Photos courtesy of Mitsubishi Heavy Industries Ltd. (MHI), Japan)

The achieved bonding strengths are comparable to those of the base material with the advantage that no heat treatment is required. The technology is based on a sophisticated surface activation step under high vacuum conditions. The disclosed main steps (Fig. 11.27j) are as follows. Oxide and other absorbed substances are removed from the wafer surface under high vacuum conditions by means of ion irradiation. This creates a highly reactive surface (dangling bonds), which then can be bonded at room temperature to another wafer.

For research and development, a semiautomatic model is available as well. The fully automated room temperature bonding machine for 8 in. wafers (Fig. 11.27a) features an alignment tolerance of 2 μm and a powerful bonding unit that features up to 100 kN force for metal–metal bonding. The degree of vacuum is 1 e–5 Pa.

11.8.2.4 SUSS MicroTec AG, Germany

SUSS MicroTec provides wafer bonding solutions for the R&D and low- and high-volume production needs of customers in the MEMS, semicompound/LED and

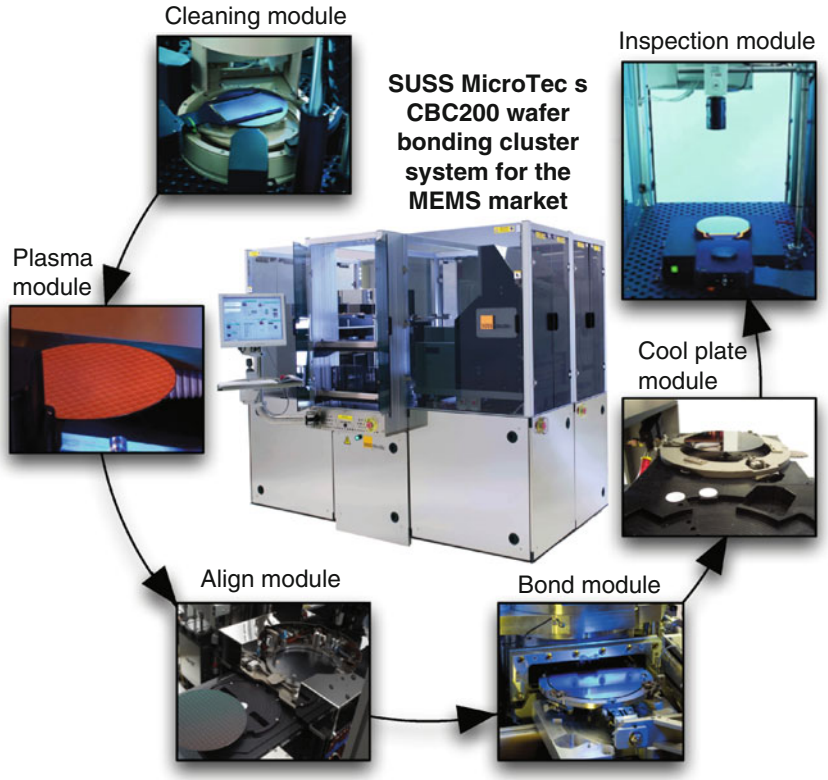

Fig. 11.28 SUSS MicroTec's CBC200 wafer bonding cluster system for MEMS market with process modules available. Listed are the modules the wafers run through from surface cleaning and conditioning, through aligning and bonding, finishing with cooling and postbond metrology (Photos courtesy of SUSS MicroTec AG, Germany)

3-D industries. The CBC200, featuring interchangeable modules to accommodate evolving process and production requirements, is SUSS MicroTec's 200 mm fully automated production wafer bonder platform for customers in the MEMS and 3-D industries (Fig. 11.28). SUSS MicroTec's bond modules have a closed bond chamber design for a contamination-free bonding environment. Wafers are loaded through a slot door and then the chamber is sealed throughout the bond process. The chamber is purged with nitrogen to keep moisture and particles out, reducing cycle time and cost. A gas overpressure up to 3 bars can be used to dampen the motion of accelerometers or other sensitive MEMS devices. The tool can be configured with a bond chamber that is ideal for glass frit, anodic, and direct bonding, or with a bond chamber that is ideal for providing high forces necessary for thermo-compression, eutectic, metal–metal bonding, and so on.

Further features of the bond module are: a pressure column technology (patent pending) that evenly distributes the force across the bond interface to ensure force uniformity, and multizone vacuum isolated heaters (patent pending) for temperature uniformity.

In addition to its wafer bonding capabilities, the CBC200 has highly advanced bond aligner modules, which utilize face-to-face ISA, TSA (topside), or BSA (backside) alignment methods for flexible and precise alignment capability.

11.9 Summary and Outlook

In the last decades, wafer bonding has served as one of the dominant tools in the field of microfabrication. Not only can it be seen as an enabling technology for the field of MEMS, it also pushes 3-D–IC integration technology and the compound semiconductor industry forward, and, thus, will be an integral part of the semiconductor industry in the future.

Wafer bonding is best known for advanced wafer-level packaging applications for various fields, such as sensors. It is accepted that often the packaging cost on a chip level is the highest cost of the product.

Wafer bonding is often the only approach to fabricate specific MEMS devices, mainly because bridging large gaps with sacrificial release methods is often impractical if not impossible. A good example is the fabrication of micromachined pressure sensors or capacitive micromachined ultrasonic transducers for lower frequencies needed for airborne applications, just to name two examples.

It is essential that the MEMS product engineer is fluent in all aspects of wafer bonding. Only then can the best fabrication process for a certain problem statement be found and the best equipment chosen for a certain fabrication task. The infrastructure and knowledge are available in the form of commercially available bonding equipment, wafer bonding service, and the literature.

Wafer bonding is still being heavily researched to improve the technology. One good example is the recent progress in providing commercial wafer bonding tools that allow reliable direct wafer bonding without any heat treatment. The value

in such technology lies in the fact that heat treatment can cause problems when different materials are direct bonded due to different thermal expansion coefficients or thermal budget limits such as found in IC circuitry. Such tools will extend the range of possible material combinations, and, thus, open the door to new applications. It will be only a matter of time that all wafer bonding tool vendors provide such additional features in their product palette.

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References

1. F. Lärmer, A. Schilp: Method for anisotropic etching of silicon, US patent 5501893 (1996)
2. Y. Huang et al.: Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology, J. Microelectromech. Syst. 12, 128–137 (2003)
3. M.W. Messana et al.: Packaging of Large Lateral Deflection MEMS Using a Combination of Fusion Bonding and Epitaxial Reactor Sealing, to appear in Proceedings Solid-State Sensors, Actuators, and Microsystems Workshop, June 6–10, 2010, pp. 336–339 (Hilton Head Island, South Caroline, 2010)
4. S. Li et al.: Fabrication of micronozzles using low-temperature wafer-level bonding with SU-8, J. Micromech. Microeng. 13, 732–738 (2003)
5. J.A. Dziuban: Bonding in Microsystem Technology, Springer Series in Advanced Microelectronics (Springer, Heidelberg, 2006)
6. Q.-Y. Tong, U. Gösele: Semiconductor Wafer Bonding: Science and Technology (Wiley, New York, NY, 1999)
7. M. Alexe, U. Gösele: Wafer Bonding: Applications and Technology (Springer, Berlin, 2004)
8. A. Plößl, G. Kräuter: Wafer direct bonding: Tailoring adhesion between brittle materials, Mater. Sci. Eng. R25, 1–88 (1999)
9. F. Niklaus, G. Stemme, J.-Q. Lu, R.J. Gutmann: Adhesive wafer bonding, J. Appl. Phys. 99, 1–27 (2006)
10. M.A. Schmidt: Wafer-to-wafer bonding for microstructure formation, Proc. IEEE 86, 1575–1585 (1998)
11. K.T. Turner: Wafer Bonding: Mechanics-Based Models and Experiments, Doctoral thesis, MIT (2004)
12. D. Tabor: Macroscopic properties and interatomic forces, Phys. Educ. 10(7), 487–490 (1975)
13. K. Kendall: Adhesion: Molecules and mechanics, Science 263, 1720–1725 (1994)
14. G. Binning et al.: Atomic force microscope, Phys. Rev. Lett. 56, 930–934 (1986)
15. N. Miki, S.M. Spearing: Effect of nanoscale surface roughness on the bonding energy of direct-bonded silicon wafers, J. Appl. Phys. 94, 6800–6806 (2003)
16. C. Gui et al.: Fusion bonding of rough surfaces with polishing technique for silicon micromachining, Microsyst. J. Technol. 3(3), 122–128 (1997)
17. W. Kern: Handbook of Semiconductor Wafer Cleaning Technology – Science, Technology, and Applications (Noyes Publications, Westwood, NJ, 1993)

18. K.A. Reinhardt, W. Kern: Handbook of Silicon Wafer Cleaning Technology, 2nd ed (William Andrew, Norwich, NY, 2008)
19. Z. Liu et al.: Micromechanism fabrication using silicon fusion bonding, J. Robot. Comput. Integr. Manuf. 131–137 (2001)
20. G.-L. Sun et al.: Cool plasma activated surface in silicon wafer direct bonding technology, J. Phys. 9, 79–82 (1988)
21. J. Köhler et al.: Silicon fusion bond interfaces resilient to wet anisotropic etchants, J. Micromech. Microeng. 11, 359–363 (2001)
22. A.F. Sarioglu, O. Solgaard: Cantilevers with integrated sensor for time-resolved force measurement in tapping-mode atomic force microscopy, Appl. Phys. Lett. 93, 023114-1-3 (2008)
23. K.K. Chan et al.: Low temperature fusion bonding with high surface energy using a wet chemical treatment, US Patent, US 7566631 B2 (2009)
24. Y.L. Chao et al.: Ammonium hydroxide effect on low-temperature wafer bonding energy enhancement, J. Electrochem. Soc. 8(3), G74–G77 (2005)
25. T. Rogers, N. Aitken: Low temperature bonding using in-situ radical activation, ECS Trans. 16, 507–516 (2008)
26. K.Y. Byun et al.: Effect of free radical activation for low temperature Si to Si wafer bonding, J. Electrochem. Soc. 157(1), 109–112 (2010)
27. K.Y. Byun et al.: Low temperature germanium to silicon direct wafer bonding using free radical exposure, Appl. Phys. Lett. 96, 102110-1-3 (2010)
28. C. Harendt et al.: Wafer fusion bonding and its application to silicon-on-insulator fabrication, J. Micromech. Microeng. 1(3), 145–151 (1991)
29. Y. Bäcklund et al.: A suggested mechanism for silicon direct bonding from studying hydrophilic and hydrophobic surfaces, J. Micromech. Microeng. 2(3), 158–160 (1992)
30. G. Wallis, D.I. Pomerantz: Field-assisted glass-metal sealing, J. Appl. Phys. 40, 3946–3949 (1969)
31. K.B. Albaugh: Electrode phenomena during anodic bonding of silicon to sodium borosilicate glass, J. Electrochem. Soc. 138, 3089–3094 (1991)
32. K.B. Albaugh, D.H. Rasmussen: Rate processes during anodic bonding, J. Am. Ceram. Soc. 75, 2644–2648 (1992)
33. S.J. Cunningham, D.R. DeReus, J.W. Borninski: An Electro-mechanical Analysis of the Anodic Bond Process for Microelectromechanical Systems, In Semiconductor wafer bonding: Science, Tech., and App., Proceedings of the Electrochemical Society, 196th Meeting, Oct 17–22, pp. 326–337 (Honolulu, HI, 1999)
34. S. Cunningham, S. Tatic-Lucic, J. Carper, J. Lindsey, L. Spangler: A High Aspect Ratio Accelerometer Fabricated Using Anodic Bonding, Dissolved Wafer, and Deep RIE Processes, Transducers 99, Sendai, Japan, pp. 1522–1525 (1999)
35. L. Spangler, C. Kemp: ISAAC: Integrated Silicon Automotive Accelerometer, Transducers 95 and Eurosensors IX, June, 25–29, pp. 585–588 (Stockholm, Sweden, 1995)
36. L. Spangler, C. Kemp: ISAAC: Integrated silicon automotive accelerometer, Sens. Actuators A Phys. 54, 523–529 (1996)
37. M.J. Wild, A. Gillner, R. Poprawe: Locally selective bonding of silicon and glass with laser, Sens. Actuators A Phys. 93, 63–69 (2001)
38. C.H. Tsau, S.M. Spearing, M.A. Schmidt: Fabrication of wafer-level thermocompression bonds, J. Microelectromech. Syst. 11, 641–647 (2002)
39. R.F. Wolffenbuttel, K.D. Wise: Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature, Sens. Actuators A 43, 223–229 (1994)
40. F. Niklaus, P. Enoksson, P. Griss, E. Kälvesten, G. Stemme: Low-temperature wafer-level transfer bonding, J. Microelectromech. Syst. 10, 525–531 (2001)
41. F. Niklaus, P. Enoksson, P. Griss, E. Kälvesten, G. Stemme: Low-temperature full wafer adhesive bonding, J. Micromech. Microeng. 11, 100–107 (2001)

42. F. Niklaus, P. Enoksson, E. Kälvesten, G. Stemme: Void-free full wafer adhesive bonding, IEEE MEMS 2000, The Thirteenth Annual Int. Conf. on Micro Electro Mechanical Systems, 23–27 June 2000, pp. 247–252 (Miyazaki, Japan, 2000)
43. G. Roelkens, J. Brouckaert, D. Van Thourhout, R. Baets, R. Nötzel, M. Smit: Adhesive bonding of InP/InGaAsP dies to processed silicon-on-insulator wafers using DVS-bis-benzocyclobutene, J. Electrochem. Soc. 153, G1015–G1019 (2006)
44. R. Puligadda, S. Pillalamarri, W. Hong, C. Brubaker, M. Wimplinger, S. Pargfrieder: High performance temporary adhesives for wafer bonding applications, Mater. Res. Soc. Symp. Proc. vol. 970, pp. 239 (2007)
45. H.S. Kim, K. Najafi: Wafer Bonding Using Parylene and Wafer-Level Transfer of Free-Standing Parylene Membranes, Transducers 03 12th International Conference on Solid State Sensors, Actuators, and Microsystems, Boston, MA, pp. 790–793 (2003)
46. H. Kim, K. Najafi: Characterization of low-temperature wafer bonding using thin-film parylene, J. Microelectromech. Syst. 14, 1347–1355 (2005)
47. H.-S. Noh, K.-S. Moon, A. Cannon, P.J. Hesketh, C.P. Wong: Wafer bonding using microwave heating of parylene intermediate layers, J. Micromech. Microeng. 14, 625–631 (2004)
48. I. Christiaens, G. Roelkens, K. De Mesel, D. Van Thourhout, R. Baets: Thin-film devices fabricated with benzocyclobutene adhesive wafer bonding, J. Lightwave Technol. 23, 517–522 (2005)
49. A. Jourdain, X. Rottenberg, G. Carchon, H.A.C. Tilmans: Optimization of 0-level packaging for RF-MEMS devices, Transducers 03, 12th International Conference on Solid State Sensors, Actuators and Microsystems, Boston, MA, pp. 1915–1918 (2003)
50. C.T. Pan: Selective low temperature microcap packaging technique through flip chip and wafer level alignment, J. Micromech. Microeng. 14, 522–529 (2004)
51. D. Pasquariello, K. Hjort: Plasma-assisted InP-to-Si low temperature wafer bonding, IEEE J. Quantum Electron. 8, 118–131 (2002)
52. C.B. Eom, L. Huang, R.A. Rao, Q.-Y. Tong, U. Gösele: Fabrication of double sided $YBa_2Cu_3O_7$ thin films on 2 inch diameter LaAlO3 wafers by direct wafer bonding, IEEE Trans. Appl. Supercond. 7, 1244–1248 (1997)
53. J. Jasinski, Z. Liliental-Weber, S. Estrada, E. Hu: Microstructure of GaAs/GaN interfaces produced by direct fusion bonding, Appl. Phys. Lett. 81, 3152–3154 (2002)
54. P. Kopperschmidt, Senz, St. Kästner, D. Hesse, U. Gösele: Wafer bonding of gallium arsenide on sapphire, Appl. Phys. A64, 533–537 (1997)
55. B.E. Roberds, K.D. Choquette, K.M. Geib, S.H. Kravitz, R.D. Twesten, S.N. Farrens: Wafer Bonding of GaAs, InP, and Si Annealed Without Hydrogen for Advanced Device Technologies, Proceedings of the Electrochemical Society, Paris, France (1997)
56. P. Kopperschmidt, G. Kästner, D. Hesse, N.D. Zakharov, U. Gösele: High bond energy and thermomechanical stress in silicon on sapphire wafer bonding, Appl. Phys. Lett. 70(22), 2972–2974 (1997)
57. G. Taraschi, T.A. Langdo, M.T. Currie, E.A. Fitzgerald: Relaxed SiGe-on-insulator fabricated via wafer bonding and etch back, J. Vac. Sci. Technol. B 20, 725–727 (2002)
58. G. Taraschi, A.J. Pitera, L.M. McGill, Z.-Y. Cheng, M.L. Lee, T.A. Langdo, E.A. Fitzgerald: Ultrathin strained Si-on-insulator and SiGe-on-insulator created using low temperature wafer bonding and metastable stop layers, J. Electrochem. Soc. 151, G47–G56 (2004)
59. G. Taraschi, A.J. Pitera, E.A. Fitzgerald: Strained Si, SiGe, and Ge on-insulator: Review of wafer bonding fabrication techniques, Solid-State Electron. 48, 1297–1305 (2004)
60. T. Akatsu, A. Plößl, H. Stenzel, U. Gösele: GaAs wafer bonding by atomic hydrogen surface cleaning, J. Appl. Phys. 86, 7146–7150 (1999)
61. S. Farrens, P. Lindner, V. Dragoi, G. Mittendorfer: Integrating MEMS devices using low-temperature wafer bonding, Solid State Technol. 49(2), (2006)

62. H. Lin, A.J. Walton, C.C. Dunare, J.T.M. Stevenson, A.M. Gundlach, S. Smith, A.S. Bunting: Test structures for the characterization of MEMS and CMOS integration technology, IEEE Trans. Semicond. Manuf. 21, 140–147 (2008)
63. L. Parameswaran, C. Hsu, M.A. Schmidt: A merged MEMS-CMOS process using silicon wafer bonding, IEEE IEDM, Washington, DC, pp. 613–616 (1995)
64. S. Sedkey, A. Witvrouw, H. Bender, K. Baert: Experimental determination of the maximum post-process annealing temperature for standard CMOS wafers, IEEE Trans. Electron Devices 48, 377–385 (2001)
65. S. Van der Groen, M. Rosmeulen, P. Jansen, K. Baert, L. Deferm: CMOS Compatible Wafer Scale Adhesive Bonding for Circuit Transfer, Transducers 97, Intl. Conf. on Solid-State Sensors and Actuators, Chicago, IL, pp. 629–632 (1997)
66. A.B. Frazier: Low Temperature IC-Compatible Wafer-to-Wafer Bonding with Embedded Micro Channels for Integrated Sensing Systems, Proceedings of the 38th Symposium on Circuits and Systems, Rio de Janeiro, Brazil, pp. 505–508 (1996)
67. R. Ghodssi, L.G. Frechette, S.F. Nagle, X. Zhang, A.A. Ayon, S.D. Senturia, M.A. Schmidt: Thick Buried Oxide in Silicon (TBOS): An Integrated Fabrication Technology for Multi-Stack Wafer-Bonded MEMS Process. Transducers '99, 10th International Conference on Solid-State Sensors and Actuators, Sendai, Japan, pp. 1456–1459 (1999)
68. Y.T. Cheng, L. Lin, K. Najafi: Localized silicon fusion and eutectic bonding for MEMS fabrication and packaging, J. Microelectromech. Syst. 9, 3–8 (2000)
69. Y.-T. Cheng, L. Lin, K. Najafi: A hermetic glass-silicon package formed using localized aluminum/silicon-glass bonding, J. Microelectromech. Syst. 10, 392–399 (2001)
70. Y.T. Cheng, L. Lin, N. Najafi: Localized Silicon Fusion and Eutectic Bonding for MEMS Fabrication and Packaging, Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, pp. 233–236 (1998)
71. L. Lin: MEMS post-packaging by localized heating and bonding, IEEE Trans. Adv. Packaging 23, 608–616 (2000)
72. L. Lin, Y.-T. Cheng, K. Najafi: Formation of silicon-gold eutectic bond using localized heating method, Jpn. J. Appl. Phys. 37, L1412–L1414 (1998)
73. L. Lin: Thermal challenges in MEMS applications: phase change phenomena and thermal bonding process, Microelectron. J. 34, 179–185 (2003)
74. H.-A. Yang, M. Wu, W. Fang: Localized induction heating solder bonding for wafer level MEMS packaging, J. Micromech. Microeng. 15, 394–399 (2005)
75. N. Ito, K. Yamada, H. Okada, M. Nishimura, T. Kuriyama: A Rapid and Selective Anodic Bond Method, Transducers 95, 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Stockholm, Sweden, pp. 277–280 (1995)
76. E.M. Chow, H.T. Soh, A. Partridge, J.A. Harley, T.W. Kenny, C.F. Quate, S. Abdollahi-Alibeik, J.P. McVittie, A. McCarthy: Fabrication of High-Density Cantilever Arrays and Through Wafer Interconnects, Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, pp. 220–224 (1998)
77. A. Doll, F. Goldschmidtboeing, P. Woian: Low temperature Plasma-Assisted Wafer Bonding and Bond-Interface Stress Characterization, IEEE MEMS, Maastricht, pp. 665–668 (2004)
78. G. Kräuter, A. Schumacher, U. Gösele: Low temperature silicon direct bonding for application in micromechanics: bonding energies for different combinations of oxides, Sens. Actuators A 70, 271–275 (1998)
79. U. Gösele, Y. Bluhm, G. Kästner, P. Kopperschmidt, G. Kräuter, R. Scholz, A. Schumacher, St. Senz, Q.-Y. Tong, L.-J. Huang, Y.-L. Chao, T.H. Lee: Fundamental issues in wafer bonding, J. Vac. Sci. Technol. A 17, 1145–1152 (1999)
80. J.E. Semmens, B.P. Scackmuth: Evaluation of Silicon on Insulator (SOI) Bonded Wafers Using Automated Acoustic Micro Imaging, SMTA Pan Pacific Symposium, Feb 10–12, pp. 1–4 (Oahu, HI, 2004)
81. M. Reiche, S. Hopfe, U. Gösele, H. Strutzberg, Q.-T. Tong: Characterization of interfaces of directly bonded silicon wafers: A comparative study of secondary ion mass spectroscopy

multiple internal reflection spectroscopy, and transmission electron microscopy, Jpn. J. Appl. Phys. 35, 2102–2107 (1996)
82. R.H. Esser et al.: Directional diffusion and void formation at a Si (001) bonded wafer interface, J. Appl. Phys. 92(4), 1945–1949 (2002)
83. X.X. Zhang, J.-R. Raskin: Low-temperature wafer bonding: A study of void formation and influence on bonding strength, J. Microelectromech. Syst. 14, 368–382 (2005)
84. T. Suni, J. Kiihamäki, K. Hettinen, I. Suni, J. Mäkinen,: Characterization of Bonded Interface by HF Etching Method, Science, Tech, and Appl. VII ECS, Electrochemical Society Meeting, pp. 70–75 (Orlando, FL, 2003)
85. M. Nese, A. Hanneborg: Anodic bonding of silicon to silicon wafers coated with aluminum, silicon oxide, polysilicon or silicon nitride, Sens. Actuators A 37–38, 61–67 (1993)
86. E. Obermeier: Anodic Wafer Bonding, Proceedings of the 3rd International Symposium on Semiconductor Wafer Bonding, ECS, Electrochemical Society Meeting, pp. 212–220 (Reno NV, 1995)
87. R. DeReus, M. Lindahl: Si-to-Si Wafer Bonding Using Evaporated Glass, Proceedings of Transducers '97, Chicago, IL, USA, pp. 661–664 (1997)
88. D.V. Kubair, S.M. Spearing: Cohesive zone modeling of wafer bonding and fracture: Effect of patterning and toughness variations, J. Phys. D: Appl. Phys. 39, 1050–1057 (2006)
89. S. Tatic-Lucic, J. Ames, B. Boardman, D. McIntyre, P. Jaramillo, L. Starr, M. Lim: Bond-quality characterization of silicon-glass anodic bonding, Sens. Actuators A 60, 223–227 (1997)
90. T. Stratton, D. Burns, B. Speldrich: IEEE Workshop on Sensors and Actuators, p. 82 (Hilton Head Island, SC, 1992)
91. M. Madou: Fundamentals of Microfabrication (CRC Press, Boca Raton, FL, 1997)
92. W.P. Maszara: Silicon-on-insulator by wafer bonding: A Review, Journal of Electrochem. Society. 138, 341–347 (1991)
93. D. Hurd, R. Caretta, W. Gerberich: An experimental fracture mechanics study of a strong interface: The silicon/glass anodic bond, J. Mater. Res. 10, 387–400 (1995)
94. S. Go, Y. Cho: Experimental evaluation of anodic bonding process based on the Taguchi analysis of interfacial fracture toughness, Sens. Actuators A 78, 52–57 (1999)
95. K.N. Chen, C.S. Tan, A. Fan, R. Reif: Morphology and bond strength of copper wafer bonding, Electrochem. Solid-State Lett. 7, G14–G16 (2004)
96. E. Reedy Jr, T. Guess: Comparison of butt tensile strength data with interface corner stress intensity factor prediction, Int. J. Solids Struct. 30, 2929–293 (1993)
97. E. Reedy Jr, T. Guess: Butt joint strength: Effect of residual stress and stress relaxation, J. Adhesion Sci. Technol. 9, 33–45 (1996)
98. E. Reedy Jr, T. Guess: Interface corner failure analysis of joint strength: Effect of adherend stiffness, Int. J. Fracture 4, 305–314 (1998)
99. M. Dunn, W. Suwito, S. Cunningham: Fracture initiation at sharp notches under mode I, mode II, and mild mixed mode loading, Int. J. Fracture 84, 367–381 (1997)
100. W. Suwito, M.L. Dunn, S.J. Cunningham, D.T. Read: Elastic moduli, strength, and fracture initiation at sharp notches in etched single crystal silicon microstructures, J. Appl. Phys. 85, 3519–3535 (1999)
101. M. Dunn, S. Cunningham, P. Labossiere: Initiation toughness of silicon/glass anodic bonds, Acta Mater. 48, 735–744 (1999)
102. P. Labossiere, M. Dunn: Stress intensities at interface corners in anisotropic bimaterials, Eng. Fract. Mech. 62, 555–576 (1999)
103. P.E.W. Labossiere, M.L. Dunn, S.J. Cunningham: Characterization of wafer bond toughness. In Semiconductor wafer bonding: Science, Technology, and Applications, Proceedings Electrochemical Society, 196th Meeting, Oct 17–22, pp. 338–349 (Honolulu, HI, 1999)

Chapter 12
MEMS Packaging Materials

Ann Garrison Darrin and Robert Osiander

Abstract This chapter discusses the differences between the heritage microcircuit packaging world and the still evolving MEMS packaging arena. Materials used in the packaging of MEMs are reviewed and their respective applications. The packaging schemes for these devices owe their infrastructure base to the body of knowledge surrounding semiconductors and microcircuits. MEMS devices yield new complexities which drive new packaging solutions. As opposed to traditional microcircuit chips, MEMS often include moving structures along with the need to have contact with the external environment, driving the requirements for packaging such components. Thus, some functions include interaction with the surrounding environment, such as pressure sensors. This imposes new requisites on packaging, since in regular microelectronics the chip must be protected completely from any impact from the environment. Packaging also provides mechanical support to the sensitive chip, facilitating the handling of the chip, and simplifying assembly. This chapter emphasizes the materials involved in packaging MEMS devices and the addresses the challenges involved. Included in this chapter are several case studies demonstrating novel packaging/material solutions.

12.1 MEMS Packages and Applications

Packaging for MEMs provides for power and signal paths; thermal management; mechanical support; and environmental protection and/or interface protection. MEMS pose numerous packaging challenges that often drive custom solutions by the very nature of their configurations and applications. Commercialized MEMS products such as inkjets and airbag sensors use simple packaging solutions; but devices that involve environmental interface have special requirements that drive

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novel approaches (i.e., bio-MEMS packages that need to handle fluids). MEMS packaging can be roughly divided into two areas: protection at the package level and protection at the wafer or device level. At the package level, MEMS are often manufactured following traditional military specifications that require robust hermetic sealing technologies. This branch of the packaging industry transferred almost intact from the semiconductor/microelectronics industry. However, this approach is in rapid decline with the main trend being away from military specifications and their high reliability electronics toward less expensive commercial, off-the-shelf (COTS) electronics. The wafer-level packaging and protection of MEMS structures enable low cost, high volume production packages that are not hermetically sealed; e.g., plastic packages or tailored RF packages with optimized electrical performance. The fact that MEMS often must be in contact with the operating environment is the most important distinction between packaging of MEMS and microelectronics.

MEMS packaging protects the mechanical structures during wafer dicing, assembly, and operation [1]. For example, during the singulation step, a mask or a wafer-level technique is used to protect vulnerable motion components as the most common MEMS packaging requirement is protection without restricting mechanical action in a cavity device. Microcircuit packaging techniques are often over molded with encapsulant contacting the chips and restricting motion and cannot be used as a MEMS packaging technique without redesign.

The hermetic cavity package used extensively in the microcircuit world, especially in critical end item applications, has been adopted for the packaging of MEMS. These standard hermetic packages are a costly solution but do offer full hermetic isolation. With respect to cost, a prevailing opinion has been that MEMS packaging is expensive. This has caused developers to question the application and the requirements, especially when hermetic packaging is specified. For example, is hermetic packaging truly required or just a dry, hydrophobic package or perhaps only a constant atmosphere is needed [1]? Early MEMS accelerometer packages were hermetic cavity designs that allowed space for motion, although these ceramic packages have since been replaced with more cost effective designs. Inertial sensor applications require only electrical inputs and outputs and do not have the packaging challenges such as in bio-MEMS where fluid transport is incorporated. MEMS packaging options range from full hermetic, near-hermetic, and non-hermetic single packages to wafer-level packaging techniques. The materials for each of these packaging classes are discussed.

12.1.1 Packaging Classes

Protection at the package level is provided by full hermetic, near-hermetic, and non hermetic packaging solutions. Full hermetic packages evolved from glass to metal and ceramic in the semiconductor/microcircuit world and are used in MEMS packaging schemes. The near-hermetic package is used where full hermetic seal is either not required or is driven by a specific product application. The non-hermetic plastic package is widely used in the microcircuit community for high volume low cost

packaging. In a plastic package, the chip is typically attached to a metal leadframe by wire bonding followed by epoxy overmolding. The overmolding compound is a mix of solid epoxy resins, hardeners, fillers and additives that is heated to polymerize the material. This mold compound makes direct contact with the die, wire bonds and leadframe. This technique cannot be translated directly to MEMS without an intermediate protection solution such as capping the chip. Capped chips may then be packaged using this technique.

Protecting chips at the wafer-level is normally done through capping and a multi step partial packaging process. Caps are passive with no electrical paths and must allow access to chip bond pads. In this partial wafer level packaging the most common solution is to singulate caps first using a multi-step process and later singulate the MEMS wafer. To eliminate the extra steps of the multi step partial wafer level package, full wafer level packaging (WLP) involves incorporating the interconnect structure through the chip or cap. This allows the cap layer to be singulated during the MEMS sawing step. For applications requiring gas and fluid transport, the capping wafer level solutions have yet to be developed.

12.1.2 MEMS Versus Microcircuit or Integrated Circuit Packaging

The highly integrated circuits of today have evolved after generations of iterations that started with the germanium transistor. The packaging schemes for MEMS devices owe heritage to the body of knowledge surrounding semiconductors and microcircuits. However, the MEMS device yields new complexities that drive new packaging solutions. Table 12.1 demonstrates these differences between the microcircuit and the MEMS world.

As opposed to traditional microcircuit chips, MEMS packaging must consider moving structures and contact with the external environment. Some applications include direct interaction with the surrounding environment, such as pressure sensors. This imposes new requirements on packaging, since in traditional microelectronics the chip must be protected completely from any impact from the environment. MEMS packaging can also provide mechanical support to the sensitive chip, facilitate handling of the chip, and simplify assembly.

12.1.3 Application Drivers and Interfaces

The process of selecting materials, packages, processes and techniques for MEMS is driven by the end item application. For example, in an RF end item application, a major design problem is to have controlled impedance of the input and output signals. Therefore, the package should not limit the electrical performance of the MEMS components.

Another application driven requirement is the need for hermeticity. Designers must decide if their components need to be isolated from oxygen, nitrogen, ambient

Table 12.1 Microcircuits packaging versus the complexity of MEMS packaging

Microcircuit	Microcircuit packaging solutions	MEMS	MEMS packaging solution
Structures with no moving parts and may be stacked	Easy to assemble and mass produce	3-D structures which may involve delicate components and precision movements	Require application specific packaging often with cavities or vacuum spaces
Packaging styles are often generic or independent of application	Industrial and military standards exist	Applications are a variety of specific functions such as biological, chemical, electromechanical and optical	Packaging styles are application driven and custom to unique functions
Packaging techniques are mature	Paths to follow for design, material selections, fabrication processes and reliability and assurance testing	Mature packaging techniques may not work for most applications	New packaging schemes must be developed at the design concept phase
IC are protected from the environment	Environmental protection is straightforward and provided by sealed encapsulation	In many applications sensitive moving or stationary components are interfaced with with the environment	Complex balance of protection from and access to the environment is required
IC transmits power for specific electrical operations	Only external ties are through inductive or conduction coupling	Many components and functions are required within the package	Increased complexity and interfaces provide new failure mechanisms

moisture, etc. before making a decision on what level of hermetic packaging is necessary. For example, ambient moisture often deteriorates MEMS devices, however, in the instance the package needs only to be a dry package and not fully hermetic. Then, the use of appropriate getters will suffice; but if long-term reliability is a requirement, the packages still need to be near hermetic since the getters have a limited capacity [1]. Figure 12.1 shows a variety of ceramic package structures for sensor applications.

12.1.4 Interfaces to Other System Components

As the package is the primary interface between the MEMS and the system, it must be capable of transferring operating power and a multitude of signals. In addition, the package may be required to distribute both operating power and other signals to other components inside the package. The integration of more MEMS devices and

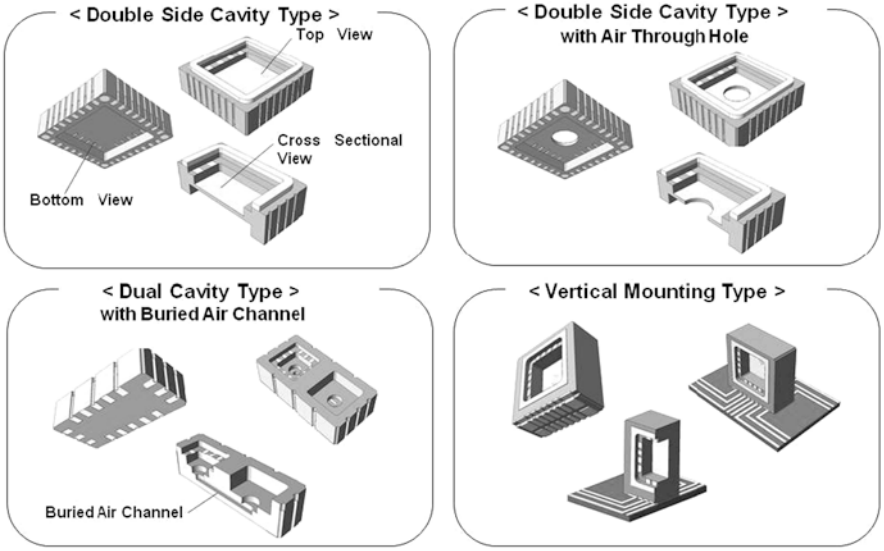

Fig. 12.1 A variety of ceramic package structures for sensor applications (Reprinted with permission of the Kyocera Corporation)

other components into a single package increases the packaging complexity as the number of interconnects within the package increases.

12.1.4.1 Power and Signals Interface

When designs require high frequency RF signals, they can be introduced into the package along metal lines passing through the package walls, or they may be electromagnetically coupled into the package through apertures in the package walls. RF energy losses between the MEMS device and the system can be due to radiation, by reflection from components that are not impedance matched, or from discontinuities in the transmission lines. The final connection between the MEMS and the DC and RF lines is usually made with wire or ribbon bonds; although flip-chip die attachment and multi-layer interconnects, using thin dielectrics have also been used.

12.1.4.2 Optical Interface

In the rapid telecom growth period of the late 1990's and into the 2000's, optical MEMS devices gained considerable attention in the telecommunications industry, particularly in the optical networking and switching arenas. Since optical MEMS are micro-systems, which rely on high precision optics, electronics, and mechanics working in close concert, these emerging devices pose some unique packaging challenges yet to be addressed by the general packaging industry.

Optical MEMS packaging differs from traditional semiconductor/microelectronics packaging in several ways. Optical MEMS packages often are required to provide optical and electrical access, hermeticity, mechanical strength, dimensional stability and long-term reliability. Hermetic optical access necessitates the use of metalized or glass sealed and anti-reflection coated windows. In addition, the ever-increasing electrical I/O count has prompted the use of higher density substrate/package technologies [2]. The reason for hermetic packaging is to ensure the long-term reliability of the expensive, state-of-the-art optical systems. Traditional FR-4 laminate-based technology is eliminated and packaging choices are restricted to mostly ceramic-based technologies such as high temperature co-fired ceramic (HTCC), low temperature co-fired ceramic (LTCC), and thin-film ceramic technologies. Since frames and windows are first sealed together, their mechanical properties, especially their coefficient of thermal expansion (CTE), have to be well matched to those of mating package materials. These requirements limit the material choices; frames are often made of Kovar^{TM}, and windows are often made of sapphire. Some windows are wedge-shaped to avoid Fabry-Perot effects. In general, optical MEMS packages are mounted to metal housings to maintain critical optical alignments. They have to be rigid and dimensionally stable over all operating temperatures to have optimized and repeatable optical performance. Any misalignments between the optics and the MEMS devices can easily translate into losses that may result in out of tolerance conditions that degrade system performance.

12.1.4.3 Microfluidic Interface

For microfluidic systems, the diverse range of applications often dictates custom designs in packaging. A microfluidic system typically integrates both fluidic and electrical components while also requiring mechanical integrity. The technical challenges with integrating micro-scale devices into macro-scale fluidic sources are: (1) obvious dimensional incompatibilities as the introduction of fluid samples and reagents into microfluidic devices in precise quantities from the macroscopic world creates a grand challenge; and (2) stability issues (including mechanical such as pressure and hermeticity) in the micro-scale caused by physical stresses arising from macro-scale fluidic connections. Apart from the challenges associated with chip-to-world fluidic interconnections, other major problems with packaging of microfluidic devices arise from the leakages of fluids. Fluidic leakages occur due to two reasons: (1) failure to handle the fluidic pressures from interconnect components; and (2) the use of an incorrect clamping force for proper sealing between various layers of the device. To avoid such issues, epoxy has been utilized to permanently attach fluidic tubing in many microfluidic packages, while a sealed connection among microfluidic interconnects has been achieved by interlinking the machined top part of the fluidic tubing to an O-ring, a custom made ring, or a coupler. As there are diverse structures and applications of microfluidic devices, it is difficult to develop a generic fluidic interconnect and packaging system [3].

12.1.4.4 Environmental Interface

Unique to many MEMS applications is the need for environmental contact, and in some cases, physical interaction with the surroundings. Pressure sensors, optical devices, and nozzles that typically require direct contact between the MEMS and the environment are often "non-capped" components. In such systems, a sealed lid/cap is not optimal, and instead, an unsealed gel lid/cap may be used to protect interconnect wires and other MEMS component parts. As an example, a typical pressure sensor detects changes in strain signals as pressure is applied on two sides of a diaphragm. On one side of the diaphragm is a fixed and sealed reference volume, while on the opposite side, environmental pressure is sensed by a strain gauge differential pressure sensor that measures diaphragm deflection.

12.2 Package Selection

Material selection is an important step in packaging and must be addressed from the early stages of development as it can affect manufacturing. When packaging microcircuits, a chip can be placed in any one of several hermetic packages. For example, it is common to procure a chip in any of a number of off-the-shelf ceramic packages, such as leadless chip carriers (LCC), dual-in-line packages, flat packs, quad flat packs, and quad chip carriers, each with various lead or leadless configurations. Although these styles are also common for MEMS components, these ceramic package configurations are sometimes not appropriate for wafer technologies that are geared for unique applications. As a rule, package choices for MEMS are more restrictive than for microcircuits because of the many unique functions offered by MEMS devices. Figure 12.2 shows a typical ceramic MEMS sensor package.

Material Compatibility with the Component and Application. Materials are chosen based on chemical, mechanical, electrical, and optical compatibilities. The

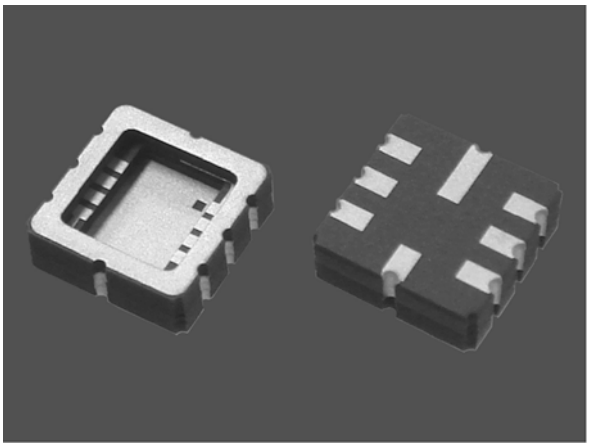

Fig. 12.2 Ceramic sensor package for MEMS (courtesy Kyocera Corporation)

performance of a complex system composed of packaging, MEMS, and attach materials can be adversely affected by either manufacturing or service conditions. Some difficult packaging challenges have been encountered with optical MEMS in particular.

Cleanliness of the Process. Contamination during assembly and joining, as well as from aging, could adversely affect the device, especially those devices with open and exposed moving components. Thus, control of particulate matter during the attachment, joining, and curing processes should be carefully chosen during manufacturing to avoid contamination.

Single Level or Die Stacking. A growing trend to deliver more functional performance per square centimeter of a packaged area poses a great challenge to manufacturing. To meet these demands, die are often stacked on top of one another to save area. Stacking is achieved in a single pass through automated placement of a die proceeded by application of an adhesive.

Flip Chip or Face Up/Wire Bond. The choice between flip chip and face up/wire bonding affects many of the areas discussed above and must be considered carefully for cost and reliability [4].

Examples of material properties for various packaging materials are found in Table 12.2; metal and ceramic properties are found in their respective sections.

12.2.1 Metal

Metal packages have commonly been used for microwave multi-chip modules and hybrid circuits as they provide both good thermal dissipation and electromagnetic shielding in addition to isolating the contents from harmful contact with surroundings. These packages, developed for semiconductors, can have a large internal volume while maintaining mechanical reliability. Metal package materials are dictated primarily by integrity of the glass or ceramic feedthroughs, restricting choices to low expansion metals that minimize thermal expansion mismatches. Properties of some typical materials used with metal packages is given in Table 12.3 [5].

Materials such as CuW (10/90), Silvar-K®, CuMo (15/85), and CuW (15/85) have superior thermal conductivities and higher CTE values than silicon, making them popular choices for shims between the silicon and the package. Materials like Kovar™ and other high nickel alloys are used because their thermal expansion properties are a close match to ceramics and sealing glasses. Packages are usually finish plated with nickel, silver, or gold.

Corrosion or reactivity, through trapped or absorbed gases or moisture, becomes a concern with metal packages. Such effects are usually eliminated by baking prior to final hermetic sealing, which is done by either welding or solder sealing a lid to the base. As a rule, assembly process temperatures are decreased with each assembly step to minimize manufacturing stresses.

Hermeticity in metal packages is affected by the quality of both the package lid seal and the feedthroughs. Feedthroughs using glass to metal or ceramic (HTCC). High temperature cofired ceramic package (HTCC) is a multilayered, sealed

Table 12.2 Properties of non metal/ceramic packaging materials

	Silicone	Polyurethane	Acrylic	Epoxy, silicone	Epoxy, Novolak	Epoxy bisphenol A	Epoxy, electrically conductive	Polyimide	Epoxy phenolic
Volume resistivity (Ω m)	10^{13}–10^{15}	0.3×10^{9}	7×10^{11}		10^{13}–10^{16}	10^{14}–10^{16}		10^{12}	
Dielectric constant @ 1 MHz	2.9–4.0	5.9–8.5	–		3.4–3.6	3.2–3.8			3.4
Dielectric strength (kV/mm)	8–27.6	12.9–23.6	–		–	–			15.8
Dissipation factor @ 1 MHz	0.001–0.002	0.005–0.06	–		0.016	0.013–0.024		–	0.32
Tensile strength MPa	10.5	urethane 5.5–55	12.4–13.8		55.0–82.7	43–85	3.4–34	–	–
Shear strength MPa		urethane 15.5	–	12.7	26.2	–	–	16.5	
Modulus of elasticity GPa	2.21	–	0.069–10.3	–	2.76–3.45	2.7–3.5		3.0	
Elongation (%)	100–800	urethane 250–800	100–400	–	2–5	4.40–12.0	—		
Specific gravity	1.06–1.2	urethane 1.1–1.6	1.09		1.2	1.15			
Hardness	20–90A	urethane 10A–800	40–90A			106RM			
Thermal conductivity (W/m °C)	6.4–7.5	1.9–4.6		13–26			0.17–1.5	0.2	25.0–74.7
CTE (ppm/°C)	262–300	90–450		60–80				40–50	33
Heat Capacity (J/kg-°C)	–	–							1674–2003
Max Temperature (°C)	260	65.6	93.3	260					87.8

A=Shore; D=Shore; RM=Rockwell M

Table 12.3 Common materials used in metal packages

Material	CTE (ppm/°C)	Thermal conductivity (TC)(W/m °K)	Density (g/cc)
CuW/15–85	7.0	180	16.40
AlSiC	6.7	180	3.00
CuMo/15–85	6.6	184	10.00
Silvar-K^{TM}	7.0	110	8.80
CuW/10–90	6.5	209	17.00
BeO	6.4	250	2.78
Kovar^{TM}	5.9	14	8.42
Molybdenum	5.1	140	10.25

package created using layers of ceramic tape with thicknesses ranging from 5 to 25 mm, which are laminated together. The cofired ceramic packages' tape layers, consisting of 92% aluminum oxide ceramic, tungsten and moly-manganese, have metalized circuit patterns. Conductive vias pierce the tape layers, forming electrical interconnects between circuits. The ceramic packages' tape layers are laminated under pressure and the ceramic and metallization are co-sintered at 1600°C, creating a monolithic structure with a three dimensional wiring system to which metal seals can be applied. A challenge for ceramic feedthroughs is the conductor that is generally metalized must seal with the ceramic. Complete wetting of the conducting pin to the ceramic during metallization must be achieved. Otherwise, incomplete wetting may result in failure during thermal cycle testing.

12.2.2 Ceramic

Ceramic packages have several features that make them especially useful for MEMS and microelectronic packaging. Ceramic packages can be made hermetic and can withstand harsh operating conditions. With high modulus of elasticity and flexural strength, ceramics can be a rigid base for devices that require accurate sensing. Ceramics can have multiple layers of signal distribution lines and can have multiple mounting orientations. A single package can be designed to be mounted both horizontally and vertically. Multilayer ceramic packages also allow reduced size and total system cost, especially over metal-walled packages, by integrating multiple MEMS and/or other components in a single, hermetic package through the use of cavities and internal signal routing. Figure 12.3 shows a typical multilayer package cross section.

Lastly, ceramics have high thermal conductivity and low coefficient of thermal expansion, which minimizes the stress placed on the MEMS device over a large operating ranges and also efficiently transfers heat away from the device without the use of thermal vias or heat spreaders. These multilayer packages also offer significant size and mass reduction over metal-walled packages. Most of this advantage

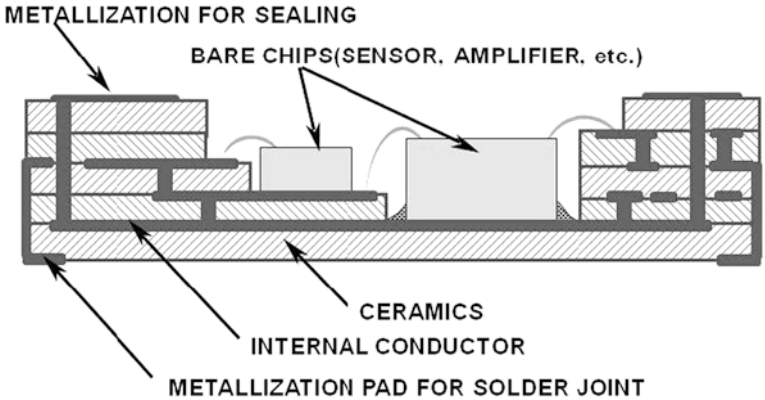

Fig. 12.3 Typical structure for a multilayer ceramic package (Reprinted with permission of the Kyocera Corp)

is derived by the ability to use three dimensions instead of two for interconnect lines. Table 12.4 gives the material properties for two common ceramic packages [6].

Ceramic packages have flexural strengths between 400 and 620 MPa, thermal conductivities between 14 and 21 W/mK, and thermal coefficients of expansion ranging between 6.9 and 7.2 ppm/°C. The ceramic package can provide a stable platform for sensor mounting and yet be sensitive to external stresses. Furthermore,

Table 12.4 Ceramic package materials properties (courtesy the Kyocera Corporation) material characteristics

Items	Units	Alumina	
		A440	A443
Bulk density		3.6	3.7
Electrical			
Dielectric constant (1 MHz)	–	9.8	9.6
Dissipation factor (1 MHz)	(1×10^{-4})	24	5
Volume resistivity (25°C)	Ωm	10^{11}	$>10^{12}$
Thermal			
CTE (RT −400°C)	(ppm/K)	7.1	6.9
Thermal conductivity	W/mK	14	18
Specific heat	$(1 \times 10^{3}$ J/KgK)	0.77	0.77
Mechanical			
Flexural strength	MPa	400	460
Young's modulus of elasticity	GPa	310	310
Conductor material	–	W. Mo	W. Mo
Feature	–		High Strength
Color of ceramics	–	Brown/Black	Brown/Black

Note: Material characteristics mentioned above are typical values. These values may change upon further improvement or modification of these materials and processes

capable of meeting a maximum leak rate requirement of 1×10^{-8} atm cc^3/s He (at 1 atm), these packages can also offer a hermetic seal for sensors that are degraded by atmospheric contact. To meet the demands of miniaturization, ceramic packages can provide multiple die packaging arrangements; internal cavity structures and lines/spaces; footprints as small as 3 mm × 3 mm; and package profiles less than 1 mm in height [7]. Table 12.5 shows properties of typical package materials [7].

Table 12.5 Comparison of typical package materials used in ceramic packages

	Alumina (HTCC)[a]	Glass ceramics (LTCC)	Mold resin	Glass epoxy (FR-4)
Flexural strength	400–620 MPa	170–400 MPa	170 MPa	550 MPa
Elastic modulus	260–315 GPa	75–190 GPa	19 GPa	25 GPa
Coefficient of thermal expansion	6.9–7.2 ppm/°C	5.4–8.4 ppm/°C	12 ppm/°C	12–15 ppm/°
Thermal conductivity	14–21 W/m°K	1.5–3.6 W/m°K	0.8 W/m°K	0.2 W/m°K
Dielectric constant (@ 1 MHz)	9.0–9.8	4.9–7.8	4.2	4.8
Glass transition temperature	N/A	N/A	130°C	170°C

HTCC is comprised of alumina (90–92%), but it can easily be confused with post-fired alumina blanks. Post-fired alumina has application in electronic packaging, but for thick-film and thin-film products, and post-fired alumina typically ranges at 96–99.6% purity

Co-fired ceramic packages are constructed from thin pliable films of ceramic material in the "green" or unfired state. Metal lines are deposited on the surface using a screen printed thick-film process; "via" holes to connect the layers are drilled or punched in the "green" state. The unfired pieces are stacked and aligned using registration holes before they are laminated together and fired at high temperatures; plating adds the proper metal surfaces. The MEMS or other components are then attached using epoxies or solders; wire bond connections are made using the same methods as for metal packages.

Normal shrinkage during the firing step of green-state ceramics may induce design dependent stress in the finished package. Since the unfired metals and green ceramics shrink at different rates during firing, the number and position of via holes and the line direction and metal fraction of each layer has to be balanced; also, because ceramic-to-metal adhesion is weaker than ceramic-to-ceramic adhesion, metal grids rather than solid planes are used for power/ground planes and shielding. For conventional multilayer ceramics, only refractory (W or Mo) metals can be used because of ceramic firing temperatures (approx. 1600°C). Ag, AgPd, Au, and AuPt conductors can be used with low temperature co-fired ceramic (LTCC) packages that fire at thick film temperatures (approx 850°C).

12.2.3 Plastic

Although plastics were used earlier for discrete transistors, plastic packages became mainstream products with the introduction of dual-in-line packages (DIP). Such packages remained as the most common commercial products throughout the integrated circuit revolution of the late 20th century. Low manufacturing costs of such materials have them widely used by the electronics industry and other applications. However, questions regarding their use in high reliability applications have been raised. Plastic packages are permeable to water vapor and often do not consistently provide the robust seals required in high reliability applications. Products are also susceptible to cracking ("popcorning") in humid environments and during PWB soldering or rapid temperature cycling. For these reasons, plastic packages have been slow to gain wide acceptance in aerospace applications.

However, some newer semiconductor designs that are only available in plastic packages are beginning to be flown in space applications. Programs such as Commercial off the Shelf (COTS), which include Plastic Encapsulated Microelectronics (PEMs), are gaining acceptance. For example, suitable PEMs were used for The Applied Physics Laboratory's Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics (TIMED) program. The size, cost, and weight constraints of the TIMED mission were achieved only with commercially available devices [8].

Since MEMS devices have moving parts, direct contact with encapsulants is not an option unless specially capped MEMS chips are used. In the plastic package, the chip is typically connected to a metal lead frame (MLF) by wire bonding followed by transfer overmolding with epoxy molding compound (EMC). Molding compound is a mix of solid epoxy resins, hardeners, fillers, and additives that is easily liquefied by modest heating to allow the melt to be forced into a mold that holds the lead frame assembly. The heated thermoset EMC polymerizes to a permanent solid and comes into direct contact with the chip, wire bonds, and MLF. The Ball Grid Array (BGA) style package can use a similar overmolding method but an organic (plastic) substrate typically is used in place of the MLF. However, overmolding of capped MEMS can stress-degrade their performance because of epoxy shrinkage around the device. Some capped MEMS products have moved away from thermoset overmolding to thermoplastic cavity packages [9]. Table 12.6 shows typical thermoplastics used in packaging [9].

Table 12.6 Typical thermoplastics used in packaging

Plastic	Water abs. (%)	Melting point (°C)	Flammability (Class UL94)	CTE/30% glass (ppm)
LCP – Liquid crystal polymer	0.02–0.10	280–352	V-O	0–12
PEEK – Polyetheretherketone	0.15	340	V-O	16
PPA – Polyphthalamide	0.15–0.29	310–332	H-B V-O	22–40
PPS – Polyphenylene sulfide	0.01–0.04	280	V-O	19–27

12.2.4 Array Packaging Materials/Wafer Level Packaging

Wafer Level Packaging (WLP) involves bonding of silicon structures. Such processes usually entail capping of fragile structures to ensure proper isolation from the surrounding environment. Processes vary by applications, and custom solutions are dictated by MEMS chips. Concerns for the damages that arise during assembly operations of wafer level packaging need to be addressed. Fabrication steps include dicing, pick-and-place die mounting, wire bonding, soldering, and sealing. Structural support and protection are provided by the use of a capping technique. Two approaches for encapsulation are currently in use: wafer-to-wafer bonding, and die-to-wafer bonding. The general idea of wafer-to-wafer bonding is to cap the wafer containing the MEMS structures with a separate, micromachined wafer in which a small cavity is made or a standoff ring is present. Wafer bonding uses anodic, fusion, or glass-frit sealing which is discussed in Section 12.4.2. For die-to-wafer bonding, preprocessed and diced caps are placed on the wafer by means of a flip chip bonder. With larger die, the approach offers economical advantages over wafer-to-wafer bonding; the longer bonding process time for mounting individual caps is balanced by making the wire bond pads readily accessible. This technique can be used for low-temperature sealing materials, including solder seals with hermeticity below 10^{-11} mbar 1/s (1 (torr/1)/s $= 1.31578947 \times 10^{-6}$ (atm/cc)/s). It can also be used for thin caps [10].

12.2.5 Custom Packaging

Most packaging methods discussed in this chapter must be customized for specific applications. WLP is evolving to applications for 3D interconnect in addition to capping, shifting its application forward in the manufacturing process. Through-silicon vias are being used to connect MEMS, CMOS image sensors and memory devices. The newest requirement for wafer bonding arises from 3D integrated bonding. Two emerging packaging applications involve CMOS image sensors with backside illumination and DRAM stacking utilizing polymer adhesive bonding or direct oxide bonding. Integration of metallic bonding techniques, such as Cu diffusion, for next-generation 3D CMOS is also currently advancing rapidly. Recent packaging advances include the integration of silicon through implementation of system-in-package (SiPs) and 3D stacking of both dies and packages [11].

12.2.6 Silicon Encapsulation

As a wafer packaging approach, sputtered silicon encapsulation is viable for MEMS devices requiring isolation. Devices that do not require interaction with the surroundings to function, such as accelerometers, RF switches, inductors, and filters can be fully encapsulated at the wafer level after fabrication. In one example, a MEMSTech 50 g capacitive accelerometer was used to demonstrate a sputtered

encapsulation technique. Encapsulation with a very uniform surface profile was achieved using spin-on glass (SOG) as a sacrificial layer, SU-8 as a base layer, RF sputtered silicon as the main structural layer, eutectic gold-silicon as a seal layer, and liquid crystal polymer (LCP) as the outer encapsulant layer. SEM inspection and capacitance tests indicated that the movable elements were released after encapsulation [12]. SU-8 is a commonly used epoxy-based negative photoresist. It is a very viscous polymer that can be spun or spread over a thickness ranging from 0.5 micrometer up to 2 mm and still be processed with standard contact lithography. SU-8 was originally developed as a photoresist for the microelectronics industry to provide a high resolution mask for fabrication of semiconductor devices. SU-8 is frequently used in the fabrication of microfluidics and MEMS parts. It is also a biocompatible material and is often used in bio-MEMS. Other examples include the use of epitaxially deposited polysilicon as an encapsulation structure for piezoresistive accelerometers [13]; plasma enhanced chemical vapor deposition of polysilicon [14]; and the use of permeable polysilicon to fabricate a vacuum shell over movable elements of a MEMS resonator [15]; and the use of a silicon cap bonded with glass frit over an accelerometer as shown in the case studies in Section 12.11.1. With such methods, use of an outer encapsulant should be considered to strengthen the initial encapsulation structure to withstand the subsequent transfer molding process, and care should be taken to assure that using any additional glob top does not further induce stress, especially during the hardening and curing steps.

12.2.7 Glass Encapsulation

Glass is predominantly used in capping operations and considerations in the use of glass include the matching of the coefficients of thermal expansion. Glass has high strength, especially in compression applications, and good electrical properties. Localized stress concentrations are usually related to the base material imperfections. The use of a glass cap process is extremely flexible and allows MEMS devices with different designs to be packaged on one chip or wafer. In contrast to silicon ($\varepsilon_r = 11.9$) as packaging material, a glass cap ($\varepsilon_r = 4.6$) has a low dielectric constant and usually has a negligible influence on the RF performance. Furthermore, glass is transparent, allowing optical control of the packaged device. A typical glass cap consists of a 300 μm thick glass plate diced from a wafer, and a cavity 100 μm in depth is precisely milled into its center to accommodate the MEMS component. The design of the glass caps is extremely flexible, since almost any shape and size can be fabricated. It is possible to cover a single chip or even a whole wafer with one single glass cap [16]. An example of an optically encased window is shown at the end of this chapter in Section 12.11.1.

12.3 Lids and Lid Seals

There are five major methods of sealing packages: seam or projection welding, high temperature (AuSn) or low temperature soldering, low temperature glass sealing,

and epoxy sealing – all but epoxy form hermetic seals [17]. Of these methods, welding is the most expensive because of the fixturing/tooling needed. Sealing glass requires higher temperatures in the range of 330–450°C, whereas both epoxy and seam welding are done at lower temperatures. Kovar™ or Alloy 42, electroplated with nickel and gold, is used for most lids for hermetic MEMS applications. For AuSn solder sealing, the lids often have a solder preform tacked on, making solder quantity control and alignment easy. The nickel underlayer serves as a very effective barrier to corrosion, while the gold surface layer preserves solderability of the nickel surface. For glass sealing, glass is usually pre-applied onto for the lid for MEMS, opto-electronic and other devices, and glass is often used in larger array packaging. Material properties of some solder preform materials are included in Section 12.4.1. The application of glass lids for optical systems is discussed in the case study in Section 12.11.2.

12.3.1 Optical Applications

Optical communications and sensors require hermetically sealed packages that allow transmission of optical, infrared, and ultraviolet signals. Sapphire, germanium and special glasses such as BK-7 allow the direct transmission of optical data. For maximum transmission efficiency, anti-reflective coatings are applied to the transparent component of the sealing lid. These coatings are nanometer thick layers of highly refractive fluoride and oxide compounds that are alternately evaporated or sputtered. These antireflective coatings can be tailored to allow specific wavelengths to pass through the lid with less than a 1% reflection loss of signal strength [18]. Properties of window materials that allow optical and infrared transmission are shown in Table 12.7.

Table 12.7 Optical and IR transmission of materials as MEMS "windows"

Material	CTE, ppm/°C	Modulus of elasticity, Gpa	Wavelength transmittance, μm
Sapphire	5.3	335	0.25–5.5 >80%
C-1737	3.8	71	0.35–2.6 >90%
BK-7	8.3	82	0.35–1.9 >90%
Ge	6.1	103	1.8–15.0 >50%
Si	4.2	102	1.2–10.0 >50%

12.4 Die Attach Materials and Processes

The methods used to attach a MEMS device to a package are the same as those used with Integrated Circuit devices. Such "*die attach*" media serve several functions: mechanical support, heat dissipation, and possibly electrical contact between the MEMS device and the package.

Electrically conductive attachment materials include silver-filled epoxies, silver-filled glasses and low melting solders. The stability and reliability of the attachment material is largely dictated by the ability of the material to withstand thermomechanical stresses created by the differences in the CTE between the MEMS silicon and the package base material. Silicon has a CTE between 2 and 3 ppm/°C while most package bases have higher CTE between 6 and 20 ppm/°C.

MEMS packages use solders, adhesives or epoxies for die attach. Each method has advantages and disadvantages that affect the overall MEMS reliability. Generally, when a solder is used, the silicon die would have a gold backing. Au-Sn (80–20) solder generally is used and forms an Au-Sn eutectic when the assembly is heated to approximately 250°C in the presence of a forming gas. When this method is applied, a single rigid assembled part with low thermal and electrical resistances between the MEMS device and the package is obtained. One problem with this attachment method is that the solder attach is rigid (and brittle) which means it is critical for the MEMS device and the package CTEs to match since the solder cannot absorb the stresses.

Adhesives and epoxies are comprised of a polymer bonding material filled with metal flakes such as silver since it has good electrical conductivity and has been shown not to migrate through the die attachment material [19, 20]. These die attachment materials have the advantage of lower process temperatures. Generally, temperatures between 100 and 200°C are required to cure the material. They also have a lower built-in stress from the assembly process as compared to solder attachment. Furthermore, since the die attachment does not create a rigid assembly, shear stresses caused by thermal cycling and mechanical forces are relieved to some extent [21, 22]. One particular disadvantage of the soft die attachment materials is that they have a significantly higher electrical resistivity which is 10 to 50 times greater than solder and a thermal resistivity which is 5 to 10 times greater than solder. Lastly, humidity has been shown to increase the aging process of the die-attachment material [20, 23].

12.4.1 Conductive Die Attach

The eutectic bonding process occurs when the substrate is secured just below the eutectic melting point on a heated work stage. The die and preform are placed on the substrate, and a light scrubbing motion is made with modest pressure by the bond head. This scrub generates a rise in the temperature of the bond to the eutectic melting point. The melted material solidifies, and creates the bond. Nitrogen is used as a cover gas in order to prevent oxidation due to the high heat. In some cases, the die may have a eutectic alloy pre-plated on its back omitting the need for a preform. The perform is a thin foil of a solder alloy of two or more dissimilar metals placed in the spacet between the die and substrate. The preform has a melting point that is lower than the melting point of its base materials. Consider a typical preform composed of gold and silicon. The melting point of gold is 1640°C, and the melting point of silicon is 1414°C. However, when the materials are combined into a

Table 12.8 Selected eutectic solder preform materials

Materials	Melting point, °C
Au97-Si3	363
Au88-Sn12	350
Au80-Sn20	280
Pb63-35Sn-1.8Sb	230

preform, the melting point becomes 363°C. Table 12.8 shows examples of eutectic preform materials. The actual bonding temperature is about 20°C higher than the eutectic point. Gold-based eutectics have high flow stresses and offer excellent fatigue and creep resistance. The high flow stress is a result of lack of early onset of plastic flow. This lack of plastic flow can lead to high stresses in the MEMS chip due to the thermal conductive mismatch between the chip and substrate.

12.4.2 Metal-Filled Glasses and Epoxies

A glass bond is formed by adhering the die to the substrate using glass in the form of a paste. In some cases, such as in silver-glass die attach, the pastes contain silver particles that enhance thermal and electrical conductivities. A mix of lead borate-based glass frit with 80 volume% Ag is a typical glass die attach paste.. The glass bonding process is similar to adhesive bonding, although differences in bonds arise from the type of material and process temperatures. Glass bonds are heated to 350–450°C, forming a low viscous liquid. As it cools, the glass hardens to form a bond.

Benefits of using a metal filled epoxy include relative insensitivity to substrate metallization, low void content, and low contamination. In addition, the resulting bonds have good thermal and electrical conductivities and limited stress relaxation. However, drawbacks such as higher oxidation rates during high temperature processing should be noted.

12.4.3 Other Die Attach Materials

Non-conducting epoxy adhesives and insulating polyimides may be filled with metals, solders, or solders filled with glasses. Epoxies filled with 70–80% (vol) silver with improved thermal and electrical conductivities are commonly used in industry. Non-conductive adhesives may also be used for their electrically insulating properties, especially for bonds between the die and substrate and other chip to package connections. In addition to conductive fillers, other agents such as wetting agents are used to improve manufacturability. Dispensing is conducted at room temperature with some typical adhesives being acrylic thermoplastic resins, epoxy thermoset resins, and silicone resins. In the adhesive bonding process, the substrate or package is secured to an unheated work stage. The wet adhesive material is contained in a reservoir and a small amount is metered out onto the substrate, usually in a pattern

conforming to the shape and size of the die. The die is picked up and placed onto the adhesive, making the wet bond, bonding is complete once the adhesive dries. This approach has many advantages: ease of automation, low-curing temperatures, low cost, wide range of die sizes, and option to rework. The downside includes out-gassing, contamination/bleed, inferior thermal conductivity, and sensitivity to harsh environments.

Polymer Adhesive Bonding. Polymer or adhesive bonding involves curing temperatures of up to 300°C with low forces applied to the substrates in low vacuum conditions. Intermediate layers, with thicknesses ranging from a few sub microns up to tens of microns, may consist of photo-patternable polymers such as Benzocyclobutene (BCB) or resists like SU-8. Low-*k* dielectric polymers, like BCB, are gaining more attention as an adhesive as these allow the creation of electrical interconnects between different functional modules (system-on-package). Although adhesive bonding compensates for surface roughness and topographical anomalies, material vapor pressures make it unsuitable for high vacuum encapsulation (below 10^{-2} torr) within MEMS devices. Low alignment accuracy during bonding poses another disadvantage to this method. Despite such complications, adhesive bonding is used in many applications that involve low-temperature wafers.

Anodic Bonding. Anodic bonding uses heat and an electric field to join a silicon wafer together with an alkali-doped glass wafer. At elevated temperatures, the alkali oxides in the glass dissociate. The so-formed mobile ions (e.g., sodium) are driven by the electric field toward the cathode, creating an oxygen-rich layer at the Si-glass interface. The oxygen ions are driven to the Si surface by the electric field, resulting in oxidation of silicon. The bond strength is high and the process is irreversible. Typical process parameters for Pyrex (borosilicate glass with a sodium oxide content of ~3.5% and a closely matching CTE over a wide temperature range) involve temperatures between 350° to 500°C, high vacuum conditions, and voltages up to 1000 V. The packages resulting from this process typically are used for hermetic sealing of MEMS and MOEMS, where elevated bonding temperatures, high voltages and sodium contamination do not affect on-chip electronics.

Glass-frit Bonding. A paste made from glass powder, solvent, and a temporary bonder (that fires away) is deposited on a wafer surface by screen printing. In general, the glass frit is applied to the wafer cap and is softened by heating to temperatures above the glass softening point. The glass material is then glazed between 300°C and 500°C. Subsequent cooling under high pressure solidifies the glass frit. Glass frit bonding is used for the caps in Sections 12.11.1 and 12.11.2.

Hermeticity is an important parameter for many MEMS devices. To achieve high vacuum encapsulation, bonding methods with low out-gassing materials, precise wafer gap control, and compatible bonding temperatures should be considered. Table 12.9 provides an overview of bonding technologies [24].

12.4.4 Flip-Chip Bonding

Controlled Collapse Chip Connection (C4) was developed by IBM in the 1960s as an alternative to manual wire bonding. Often termed "flip-chip," electrical and

Table 12.9 Overview of different bonding techniques for hermetic sealing of packages

Bonding technology	Suitability for high vacuum (<10^2 torr)	Precise gaps	Processing Temp. (°C)	Limitations
Silicon fusion bonding	√	√	>1000	• Good surfaces needed (micro roughness, TTV, cleanliness)
Plasma activated bonding	√	√	200–400	• Good surfaces needed (micro roughness, TTV, cleanliness)
Anodic bonding	√	√	200– 400	• Limited material choice (Glass – Si) • Sodium contamination
Eutectic bonding				
Au-Si	√	√	390	
Au-Sn	√	√	310	
Thermo compression bonding with intermediate layers				
Epoxy	×	×	150–250	• Out gassing of bond material
Polymers	×	×	150 –250	• Out gassing of bond material
Glass Frit	×	×	350–500	• Out gassing of bond material
Au-Au Comp	√	√	400–450	

mechanical interconnects are created by plating solder bumps between bond and metal pads of the package substrate. Chip-to-substrate misalignments are corrected by the surface tension of the molten solder, making the flip-chip process self-aligning. Unlike wire bonding which requires placement of bond pads around the periphery of the die, the flip-chip process allows the placement of bond pads anywhere on the entire chip, therefore increasing the interconnect density. Having the ability to unite distinct chips into a single package, flip-chip technology has become especially attractive in the MEMS industry [25]. Furthermore, the method also provides the option of rework. Prior to underfill chips may be removed and replaced when needed with minimal risk. For improved reliability, a chip underfill may be injected between the joined chip and the package substrate, although care should be taken so that the underside is covered entirely by the underfill without air pockets and voids. Complete edge fillets must be formed around all four sides of the chip to avoid high-stress concentrations [23].

12.4.5 Tape Interconnects

Tape Automated Bonding (TAB) was originally conceived as a rapid and robust alternative to the slow and manual process of wire bonding [26]. Materials used for

the tape carrier base include polyimide, polyester, polyethersylfone (PES) and polyparabanic acid (PPA). Tape Automated Bonding is applied between MEMS devices and substrates. Instead of single wires, this process uses a prefabricated carrier tape with etched and finish-plated copper leads that can be made for many pad configurations. Such tapes consist of perforated polyimide films, similar to those used for camera films, with stamped openings for device and connection leads. A copper foil structured by photolithography is then glued on these films. This package style is enjoying resurgence in the MEMS community and many successful applications exist [27]. Usually, TAB involves cantilevered beam leads connected to IC pads. Although such a technique is widely used, derivations connect flex inner leads to the IC. The flexible outer leads are soldered to a PWB. In newer array packages, the outer leads are replaced with metal posts, connection bumps, or solder balls, which enable surface mounting. Flex-based BGAs are therefore lightweight, low in profile, and easily assembled by SMT. The common theme in all of the TAB type packages is the direct bonding of inner lead flex conductors to chip pads. IBM's Tape Ball Grid Array (TBGA) and Tessera's μBGA are both flex-based packages and numerous variations of these two TAB concepts exist [28].

12.5 Wire Bonding

Tape Automated Bonding (TAB), Direct Chip Attachment (DCA), and wire bonding are the options available to interconnect MEMS die. While there are many subsets and derivatives, all IC interconnections can be classified into one of these three basic systems [28]. This section covers the most commonly used method of chip connection, wire bonding. Most often, this technique uses small gold wires; however, aluminum or occasionally copper are also used. Wire diameters range from 15 μm to several hundred micrometers. There are two main classes of wire bonding: ball and wedge. Ball bonding is used with gold or copper wires and requires modestly elevated temperatures. Gold wires are far more common since its does not oxidize to impede micro-welding. Both gold and aluminum wires are used for wedge bonding, with heat being required only for gold. In wire bonding, the wire is attached at both ends using some combination of heat, pressure, and ultrasonic energy to make a weld. It is generally considered the most cost-effective and versatile interconnect technology. Wire materials properties that affect wire bonding include yield strength, ultimate tensile strength, elongation, and purity.

12.5.1 Gold Wire Bonding

Gold wires are used extensively for thermocompression and thermosonic bonding. As such, most common systems involve placing gold wires between a package and the aluminum bond pads on an IC; with RF devices, gold ribbons are often used to control parasitic inductance. It is the purity of the gold that controls the mechanical

Table 12.10 Typical mechanical properties

Diameter	Elongation (%)	Break strength (g) minimum	Elongation (%)	Break strength (g) minimum	Elongation (%)	Break strength (g) minimum
Automatic gold wire bonding						
0.0007″	0.5–2	6	2–5	45.8	5.8	3.5
0.0008″	0.5–2	8	2–5	5.5	5–8	5
0.0009″	0.5–2	12	2–5	6.5	5–9	6
0.0010″	0.5–2	15	2–5	9	5–10	8
0.00125″	0.5–2	22	2–5	14	5–11	10
0.0015″	0.5–3	32	2–5	19	5–12	16
0.002″	0.5–3	42	2–5	37	5–13	33
Manual gold wire bonding						
0.0007″	0.5–2	5	2–5	3.5	5.8	2.5
0.0008″	0.5–2	7	2–5	5	5–8	4
0.0009″	0.5–2	11	2–5	5.5	5–8	65
0.0010″	0.5–2	12	2–5	7.5	5–8	6.5
0.00125″	0.5–2	20	2–5	12.5	5–8	10
0.0015″	0.5–3	28	3–7	17.5	7–11	14.5
0.002″	0.5–3	40	3–7	35	7–11	30
Gold ribbon (bonded to 99% aluminum 1% silicon pad by thermosonic techniques)						
0.0007″	0.5–2	5	2–5	3.5	5.8	2.5
0.0008″	0.5–2	7	2–5	5	5–8	4
0.0009″	0.5–2	11	2–5	5.5	5–8	65
0.0010″	0.5–2	12	2–5	7.5	5–8	6.5
0.00125″	0.5–2	20	2–5	12.5	5–8	10
0.0015″	0.5–3	28	3–7	17.5	7–11	14.5
0.002″	0.5–3	40	3–7	35	7–11	30

properties of the wire, such as elongation and break strength. For example, small amounts, 5–10 ppm by weight, of beryllium or 20–100 ppm by weight of copper are added. Table 12.10 show typical wire strength values for automated system (HBX), manual system (HBXL), and ribbon wire bonds, respectively [29].

12.5.1.1 Au-Al System

The gold-aluminum (Au-Al) system is the most common in microelectronics. This method utilizes the metallization of aluminum to create a bond and does not require any additional processing steps. Au-Al thermosonic bonding requires elevated temperatures of about 125°C. At this temperature, the needed intermetallics form quickly between the Au ball and Al bond pad.

Although intermetallic formation is necessary to form the Au to Al weld, a life limiting factor can be excessive growth of these Au/Al intermetallic compounds. Over time, Kirkendall voids can form because of differences in diffusion rates between Al and Au; these voids along the Al-Au interface weaken the brittle intermetallic layer, allowing fracturing to occur. As this is a diffusion related process,

composition of the wire and bond pad can be varied to impede interdiffusion, but at the cost of making initial bonding more difficult – a clear production versus reliability tradeoff.

12.5.1.2 Au-Ag System

The gold-silver (Au-Ag) system is a bonding scheme that is primarily used for secondary bonds (i.e., off-die). Such bonding is found in most leadframe-based package technologies where a wedge bond is formed between gold wire and a silver-plated package lead. Bond formation may also be enhanced through thermosonic means at elevated temperatures of about 250°C. Thermosonic processes sweep aside surface oxide or sulfide films to raise the bondability of the silver pad.

12.5.1.3 Au-Au System

Au-Au bonding schemes are often found in MEMS packaging. Risks such as interface corrosion, intermetallic formation, and other mechanisms that degrade the bond strength are avoided by using this monometallic system. Au-Au bonding is usually performed at elevated temperature by thermocompression or thermosonic means, although cold ultrasonic Au-Au wire bonding can also be achieved.

12.5.1.4 Au-Cu System

Gold-copper (Au-Cu) bonding metallurgy is usually employed in bonding gold wires to bare copper lead frames. Gold wire-copper leadframe bonding produces three ductile intermetallic phases (Cu_3Au, AuCu, and Au_3Cu), that at high temperatures, tend to form voids which degrade the bond strength and lower its reliability. Cleanliness of the bonding surface is therefore imperative in gold-copper systems to ensure reliable bonding [30].

12.5.2 Aluminum Systems

Although not as common as gold systems, aluminum systems are used throughout the industry with Al-Al being the most common. Table 12.11 shows typical mechanical properties for aluminum wires [31].

Table 12.11 Typical mechanical strength for aluminum wires

	Al wire	
Diameter	Elongation %	Break strength (min.g.)
0.0007″	0.5–3.5	7–10
0.001″	1–4	13–16
0.00125″	1–4	16–19

12.5.2.1 Al-Al System

For critical end item usage the monometallic bonding scheme of Al to Al is widely utilized. Al-Al systems are used primarily in hermetic packaging, for bonding aluminum wires onto the aluminum bond pads of the die. As this bonding scheme avoids intermetallic formation and corrosion, it is also a reliable wire bonding metallurgical system. Aluminum wire on aluminum bond pad is achieved ultrasonically at room temperature. Pure aluminum is too soft to be a fine wire and is often alloyed with 1% Si or 1% Mg to provide strength.

12.5.2.2 Al-Ag System

The aluminum-silver (Al-Ag) system is most commonly used in lower-cost thick-film hybrid technologies to bond an aluminum wire onto a thick-film silver alloy (with Pt or Pd) bonding pad of a ceramic substrate. The Al-Ag phase diagram has several different intermetallic phases that may cause degradation as a result of excessive interdiffusion between the Al and Ag. Al-Ag bonds exhibit accelerated corrosion in the presence of moisture, which most often is the result of an ionic contaminant such as chlorine. The risk of corrosion in the field is usually mitigated by using large diameter aluminum wires and thick silver alloy bonding sites.

12.5.2.3 Al-Ni System

For power device and high temperature applications, aluminum-nickel systems are often used. This metallurgical system usually consists of a large diameter aluminum wire and nickel bonding pads or package posts plated by electroless plating methods.

Al-Ni wire bonding systems may present some bondability problems because of the tendency of the nickel surface to oxidize quickly. Wire bonding is performed in an inert atmosphere after the pads are nickel-plated. To improve bondability, abrasive cleaning may be required. Some substrate manufacturers deposit a very thin layer of gold over the nickel surface to prevent it from oxidizing.

12.5.3 Copper Systems

The Cu-Au system is vulnerable to void formation at high temperatures, and requires bonding surface cleanliness. In the Cu-Au system, void formation may be a particular issue due to intermetallic growth. In addition, an intermetallic $CuAl_2$ phase can form which is brittle and can cause failure of the bond. These systems are also vulnerable to corrosion in the presence of chlorine and moisture.

12.6 Electrical Connection Processes

Both power and signal connections must be made from the MEMS chip to outside electronics. The main types are cable connectors, board connectors, chip connectors and probe testers. Cable connectors make a (normally demountable)

connection between two electrical cables. They are referred to as in-line connectors, if the connection is made by insertion of a male part into a female part, in a direction parallel to the cable axis. The cable may have many conductors. If these lie parallel in a plane, the connector is often known as a ribbon connector. In a ribbon connector, the connecting elements (often known as tongues) are normally arranged on a substrate. The tongues may then deflect in plane (i.e., parallel to the substrate plane) or out-of-plane (perpendicular to the substrate). Thus, it is possible to have an in-line connector with in-plane deflection of the connector tongues [32]. A typical device package is composed of a flat lead frame with numerous leads at the interior die position. The MEMS device is positioned and aligned with the interior opening of the lead frame, after which it is electrically connected to the interior of the lead frame by small wires.

12.7 Encapsulation

Encapsulants come in two physical forms, solids and liquids, but with similar compositions. Solid types are epoxy molding compounds (EMC) and are blends of solid epoxy resin, hardener, flame retardant, filler, and several additives. EMC preforms or "hockey pucks" are used in transfer-molding machines. Similar in composition, liquid encapsulants are formed from liquid forms of resin and hardeners. In this form, the material may be dispensed and applied directly instead of molded onto the chip and interconnect. Polyimides, polyamide-imides, silicones, acrylics, polyurethanes, fluoropolymers, parylenes and epoxies are typical materials that could be used for encapsulation or conformal coatings. Except for parylenes, which are vapor deposited, the coatings are usually applied in liquid form and are cured using infrared or ultraviolet radiation. This section will discuss both encapsulants and conformal coatings.

12.7.1 Polyurethane

Polyurethanes are available as one or two component resins for conformal coatings. Electronic components are often protected from environmental influence and mechanical shock by enclosing them in polyurethane. Typically, polyurethanes are selected for excellent abrasion resistances, good electrical properties, excellent adhesion and impact strength, and low temperature flexibility. The disadvantage of polyurethanes is the limited upper service temperature (typically 250°F (121°C)). In production, the manufacturer would purchase a two part urethane (resin and catalyst) that would be mixed and sprayed or poured onto the circuit. In most cases, the final circuit board assembly would be unrepairable after the urethane has cured.

12.7.2 Polyimide

Polyimides are a family of thermoset and thermoplastic resins characterized by repeating imide linkages. There are four types of aromatic polyimides: (1) condensation products formed by the reaction of pyromellitic dianhydride (PMDA)

and aromatic diamines such as 4,4′-diaminodiphenyl ether; (2) condensation products of 3,4,3′,4′-benzophenone tetracarboxylic dianhydride (BTDA) and aromatic amines; (3) the reaction of BTDA and a diisocyanate such as 4,4′-methylene-bis(phenylisocyanate); and (4) a polyimide based on diaminophenylindane and a dicarboxylic anhydride such as carbonyldiphthalic anhydride. Thermoset polyimides are produced from condensation polymers that possess reactive terminal groups capable of subsequent cross-linking through an addition reaction [33]. Polyimides have excellent mechanical and electrical properties and can be used in a wide range of temperatures. They are widely used in electronics for their excellent high temperature and chemical resistance, but may not be ideal for use in high temperature curing and high pressure applications.

12.7.3 Polydimethylsiloxane (PDMS)

Polydimethylsiloxane (PDMS) is the most commonly used elastomer in MEMS, especially in microfluidic systems. Although available in an array of formulations, polydimethylsiloxanes have limited mechanical properties, but are balanced by good chemical and thermal degradation resistance. In comparison, polyurethanes can be either mechanically softer or stiffer than PDMS, offering better adhesion and tear resistance. These are available in biocompatible formulations that exhibit excellent chemical resistance. So far, polyurethanes are used as encapsulating structures for chemical sensors and numerous bio-MEMS applications.

12.7.4 Epoxy

Almost all of these encapsulants use epoxies that are not all that different from the original ones developed in 1927. Epoxies react with many kinds of molecules, and those that are useful for producing products are called hardeners. Anhydrides are one of the most important reactants, or hardeners, and are used in many encapsulants and underfills. Epoxies are noted for versatility and balanced properties but are rather average in general characteristics. Additives are required to bring their properties to a level where they can function as encapsulants. Flame retardants, especially bromine-containing epoxies, are added to reduce flammability and to meet specifications. The average epoxy coefficient of thermal expansion (CTE) is too high for encapsulation and acceptable levels are achieved by adding low CTE fillers such as silica. Both liquid and solid epoxies must be thoroughly polymerized to be useful for package enclosures. Epoxy molding compounds (EMCs) are actually low melting mixtures of resins and other constituents, and must be polymerized into non-melting structures that have good mechanical strength and thermal stability to survive the solder assembly process. The same is true for liquid encapsulants. Polymerization, the formation of high molecular weight structures by chemical reactions, occurs when heat is applied to a system that contains epoxy resin, hardener,

and usually an accelerator to increase the reaction rate. The resulting thermoset is a 3D structure that is highly cross-linked and non-melting. Excessive heating, however, can cause the polymer to degrade by thermal decomposition, a present concern with the increasing temperatures required for many lead-free solders. Epoxies also absorb significant amounts of moisture, and the explosive release of steam, termed popcorning, is exacerbated by higher soldering temperatures [34].

12.7.5 Fluorocarbon (Polytetrafluoroethylene)

Polytetrafluoroethylene (PTFE, trade name Teflon) has a wide range of unique and desirable physical, electrical, and chemical properties. Its tribological properties are well-suited to anti-stiction applications, and its chemical inertness commends it as a barrier and passivation layer. However, conventional thin-film techniques are not suited for depositing Teflon films on microstructures. Spin coating is impossible because of the well-known insolubility of PTFE. Plasma polymerization of fluorocarbon monomers, ion beam and RF sputtering produce PTFE films that are deficient in fluorine. Pulsed laser deposition (PLD) use of excimer and Ti:sapphire lasers is unsatisfactory because UV or near-IR laser ablation "unzips" the PTFE and high-temperatures are required to re-polymerize the deposited monomeric film. It has been demonstrated that a completely dry, vapor-phase coating technique – resonant infrared pulsed laser deposition (RIR-PLD) at a wavelength of 8.26 μm – produces crystalline, smooth Teflon films at low process temperatures. Films deposited on microscale structures show good adhesion, excellent smoothness, and a high degree of conformability to the structures [35].

12.7.6 Acrylic (PMMA)

Poly(methyl methacrylate) (PMMA) is a thermoplastic and transparent plastic. Chemically, it is the synthetic polymer of methyl methacrylate. Acrylic coatings have numerous benefits from a high volume and cost effectiveness perspective. Acrylics tend to be hard, rigid, and extremely tough. Combined with excellent electrical properties, acrylics can be considered for commercial high volume applications. As opposed to epoxy, acrylics exhibit little shrinkage during the curing process. They have excellent moisture resistance and can endure weak acids and bases. Decreased dielectric constants with increasing frequencies make them good candidates for high frequency applications. However, acrylics offer poor abrasion resistance and can be attacked by strong solvents and acids.

12.7.7 Parylene

Parylene is the tradename for a variety of chemical vapor deposited poly(p-xylylene) polymers used as moisture barriers and electrical insulators. Among them, Parylene

C is the most popular due to its combination of barrier properties, cost, and other manufacturing advantages. Parylene's low permeability to moisture and gases and hydrophobic nature makes it advantageous in electrical applications. Parylene is often used as a conformal coating in critical applications. Parylene C is an inert, hydrophobic, optically clear biocompatible polymer coating material used in a wide variety of industries, and, because it is deposited by vapor deposition, Parylene provides a conformal coating on virtually any substrate which is not achievable by other means. Its lubricity is close to that of Teflon but can be applied uniformly in much thinner coatings, making them ideal for MEMS and bio-MEMS-based applications. Parylene's pinhole free conformal coating protects coated substrates from moisture, chemicals, and electric charge. While Parylene is typically used to coat circuit boards or immobilize particles, it can also be removed from the original surface and used as a microstamp allowing MEMS patterns to be reproducibly transferred to polymers with various properties (Parylene properties are available from the manufacturer at www.scscookson.com/parylene_knowledge/index.cfm).

12.7.8 Liquid Crystal Polymer

Liquid crystal polymers (LCPs) are a class of aromatic polyester polymers. They are unreactive, inert, and highly resistant to fire. LCP has been identified as an excellent candidate to control the humidity in nonhermetic packaging and is used in RF MEMS. LCPs have the following advantages [36]:

(1) Near-hermetic permeability to moisture keeping the MEMS dry for months even in humid environments;
(2) Low RF loss properties allowing excellent RF performance after packaging;
(3) Excellent moldability allowing high-speed glob-top encapsulation.

12.8 Electrical and Thermal Requirements

12.8.1 Electrical Considerations

Electrical interfaces, based on the long history of the microelectronics industry, are the most standardized. For hermetic components feedthroughs are glass matched, glass compression, or ceramic. Glass matched seals rely on glass and metal combinations with similar coefficients of thermal expansion to form an oxide bond that results in a hermetic seal. Compression seals rely on glass and metal combinations that have greater thermal expansion coefficients, thus allowing the creation of a compression seal providing hermeticity. Al_2O_3 ceramic seals are used as an alternative

to glass. Integrated ceramic feedthroughs that are sometimes referred to as co-planar or strip-line connectors, can contain conductors designed for RF, DC, and/or ground signals.

Standard leadframes are used primarily for flatpacks although some machined housings utilize them as well. The standard leadframe consists of co-planar parallel leads connected to a common tie bar that is used for electroplating contact. Typically, the lead portion of the leadframe is 0.010″ thick and 0.015″ wide and has an overall length of either 0.743″ or 1.000″ (including the 0.125″ wide tie bar). The leads are spaced either 0.050″ or 0.100″ center-to-center. Special leadframes with varying dimensions such as thinner cross sections, longer overall lengths, non-standard lead spacings, etc., may be obtained. Round pins, sometimes called straight pins, are used for all package styles but are most commonly used in plug-in type packages. Round pins are typically 0.018″ in diameter but other sizes are available. Pin length can range from 0.100″ to as long as 1.000″. When round pins are used in flatpacks, they usually will have one end flattened to create a small area for wire bonding. High power leads are used to transmit high current signals through sealed conductors. These usually have copper-core under a sealing alloy like Kovar or Alloy 51. There are many materials that are able to conduct high current but many are not suitable for glass sealing.

12.8.2 Thermal Considerations

For independent small signal circuits, the temperature of the device junction does not increase substantially during operation, and thermal dissipation from the MEMS is not a problem. However, with highly integrated System-in-Package applications, MEMS devices share thermal paths with other components, such that the temperature rise in the device junctions can be substantial causing the circuits to operate in an unsafe region. Clearly, such distributed thermal dissipation requirements for such highly integrated packages can place severe design constraints on the package design.

Three thermal resistances that must be minimized: the resistance through the package substrate, the resistance through the die-attach material, and the resistance through the carrier or package base. Furthermore, the thermal resistance of each is dependent on the thermal conductivity and the thickness of the material. A package base made of metal or metal composites has very low thermal resistance and does not add substantially to the total resistance. When electrically insulating materials are used for bases, metal-filled via holes are routinely used, under the MEMS, to provide a thermal path to the heat sink. Although thermal resistance is a consideration in the choice of the die attachment material, adhesion and bond strength are even more important. To minimize the thermal resistance through the die-attachment material, the material must be thin, void-free, and the two surfaces to be bonded should be smooth [37].

12.9 Hermeticity and Getter Materials

12.9.1 Hermeticity and Pressurized Packaging

The definition of hermeticity comes from the United States Department of Defense specification for Microelectronic Packaging (MIL-STD-883) stating that a seal that prevents the entry of contaminants or reactive gasses into the internal cavity is deemed hermetic. In practice, small gas molecules may enter the cavity over long time scales through diffusion or permeation. Table 12.12 comes from the Military Standard and defines the leak rate limit by package volume. To test to this specification, the package is placed in a pressurized Helium atmosphere for the specified time followed by a dwell time between pressure release and measurement. The unit is then placed in a calibrated Helium mass spectrometer that measures its helium leak rate.

Table 12.12 Leak rate testing to cavity size from MIL-STD-883

Pkg Volume, cm^3	PSIG	Exposure time, h	Dwell, h	Reject limit atm-cm^3/s He
V <0.40	60±-2	2 +0.2,–0	1	5×10^{-8}
V. ≥0.40	60±2	2 +0.2, –0	1	2×10^{-7}
V.≥0.40	30±2	4 +0.4, –0	1	1×10^{-7}

12.9.2 Hermeticity and Vacuum Packaging

Some special applications require wafer-level packaging with hermetic cavities under vacuum, creating the need for bonding equipment that can be used in high- or ultra-high-vacuum environments. These include:

- High-accuracy accelerometers and gyroscopes;
- MEMS switches and oscillators;
- High-frequency resonators; and
- Optical switches and infrared (IR) imaging sensors

A wafer bonding technique developed to accommodate these requirements uses getter materials to ensure suitable vacuum (total pressure $< 1\times10^3$ mbar) and long-term stability in MEMS devices. Gettering is essential for removing unwanted gases out of the MEMS package to create the desired final atmosphere.

12.10 Quality and Reliability

As was discussed in the first section and shown in Table 12.1, the flat world view of integrated circuits and microcircuits does not fully address the MEMS packaging

schemes. However, failure mechanisms seen in the microcircuit world may be evident in the MEMS realm. Common failure modes seen in microcircuit packaging are:

(a) Die and passivation cracking
(b) Delamination between the die, die attach, die pad, and plastic passivation
(c) Fatigue failure of interconnects
(d) Fatigue fracture of solder joints
(e) Warping of printed circuit board

Most of the failures as described above are due to the following sources:

(a) Mismatch of coefficients of thermal expansion between the attached materials.
(b) Fatigue fracture of materials due to thermal cycling and mechanical vibration.
(c) Deterioration of material strength due to environmental effects such as moisture.
(d) Intrinsic stresses and strains from microfabrication processes such as thermal oxidation, diffusion, and depositions [38].

Suffice it to say that the MEMS packaging engineer must consider all of the above and then more.

12.10.1 MEMS Packaging Reliability Concerns

As discussed in earlier chapters, virtually all MEMS devices require microfabrication techniques such as surface micromachining. All future processing steps including bonding depend on proper surface treatment prior to actual bonding. Any improper treatment in surface conditioning would leave voids at the bonded interfaces. These imperfections can act as crack initiators or stress concentrators for subsequent delamination of the interfaces [38]. Any improper selection of materials will be apparent in the temperature dependent mismatch failures. Thus, precision control of all processes e.g. temperature, contact pressure and applied voltages in anodic bonding process is fundamental to successful packaging scenarios. Once packaged, the device sees reliability and quality assurance screens and application stresses. Any imperfections at the interfaces and delamination of the bonding surfaces will be exacerbated and may lead to failure.

At all fabrication steps, the concerns of material compatibilities need to be addressed. During packaging of MEMS, stresses will be distributed within the die attachment, die and substrate the reliability of the packaging structure. Numerous studies in the literature discuss stress during processing steps [39].

Outgassing may cause environmental contamination that leads to clogging or material build up. The device may then become inoperable depending on its

function. Contamination binding and build up have been found to cause device failures in strategic active areas [40].

The inner surfaces of micro-conduits used for electro-osmotic and electrophoresis pumping require coats of special polymers, allowing for the release of ions under the influence of electrical fields. These ions interact with those released from the contacting fluids via electromigration and thus results in fluid capillary flow. These delicate thin film coatings, often a few nanometers thick, can be attacked by free ions, reducing their effectiveness over long electric field exposure times. This reliability issue is difficult to resolve [38].

Multiple stresses may be more detrimental to reliability than the effects of a single factor. In the design process, both design factors and test criteria must consider both individual and/or combined life cycle stresses to produce the robustness needed to withstand the hazards identified in the system profile. The synergistic effects of typical combined environments can be illustrated in a matrix relationship, which shows combinations where the total effect is more damaging than the cumulative effect of each environment acting independently. For instance, an item may be exposed to a multitude of environmental factors such as temperature, humidity, altitude, shock, and vibration while it is being transported. Demonstrating adequate end of life service must include combined effects. For example, many delicate MEMS device components, such as the thin silicon diaphragms used in micro pressure sensors, are in contact with corrosive or reactive gases whose is to be sensed. Many of these gases, such as the exhaust gases from internal combustion engines, are hot and contain corrosive chemical compounds. Extended exposure to these hot media may cause serious damage to delicate components [38].

12.10.1.1 Thermal Effects

High temperatures impose a severe stress on most electronic devices including MEMS, often causing mechanical failure or resulting in deterioration due to chemical effects. MEMS design inherently requires small sizes with high part densities. This generally requires a cooling system to provide a path of low thermal resistance from heat-producing elements to a heat sink. Adequate life with such thermal stresses usually demand the use of heat dissipation devices, cooling systems, thermal insulation, and heat-resistant materials.

Conversely, low temperatures experienced by MEMS can have a reliability impact. These problems usually are typically associated with mechanical system elements. They include mechanical stresses produced by differences in the coefficients of expansion (contraction) of metallic and nonmetallic materials, embrittlement of nonmetallic components, mechanical forces caused by freezing and expansion of entrapped moisture, stiffening of fluid constituents, etc. Typical examples include cracking, delaminations, binding of mechanical linkages, and excessive viscosity of lubricants. Reliability improvement techniques for such low temperature stresses include the use of heating devices, thermal insulation, and cold-tolerant materials.

Additional stresses are produced when MEMS are exposed to sudden changes of temperature or rapidly changing thermal cycling conditions. These conditions generate large internal mechanical stresses in structural elements, particularly when dissimilar materials are involved. Effects of thermal shock-induced stresses include cracking of seams, delamination, loss of hermeticity, leakage of fill gases, separation of encapsulating materials from components and enclosure surface leading to the creation of voids, and distortion of support members.

A thermal shock test may be specified to check the integrity of solder joints since such a test creates large internal forces due to differential expansion. Repetitive stress may create segregation effects in solder alloys leading to the formation of lead-rich zones, which are susceptible to cracking effects.

12.10.1.2 Shock and Vibration

MEMS often are subjected to environmental shock and vibration during both normal use and testing. Such environments can cause physical damage when deflections cause mechanical stresses that exceed the allowable working stress of the constituent parts.

Natural frequencies of the MEMS parts are important parameters that must be considered in the design process since a resonance can result if any such natural frequency is within the vibration frequency range encountered. The resonance condition will greatly amplify subsystem deflections and may increase stresses beyond the safe limit.

The vibration environment can be particularly stressful for electrical sliding connections, since it may cause relative motion between members of the connector. In combination with other environmental stresses, this motion can produce frit corrosion which can generate wear debris and cause large variation in contact resistance. Mitigation techniques for vibrational stress include the use of stiffening, control of resonance, and reducing freedom of movement.

12.10.1.3 Humidity

Humidity can cause degradation of MEMS as discussed previously. Mitigation techniques for humidity and salt environments include use of hermetic sealing, moisture-resistant materials, dehumidifiers or desiccants, protective coatings/covers, and reduced use of dissimilar metals.

Deleterious effects are often exacerbated with high humidity. For example, package crack growth has a dependence on moisture that is well documented [41]. Also, electrical performance may change as moisture condenses in gaps causing surface tension that may induce a piezoresistive stress effect [42]. Perhaps best known is the relationship of adhesion and friction of polycrystalline silicon MEMS [43]. This dependence is reduced, but not eliminated, when molecular coatings are applied to the surfaces. Such anti-stiction coatings have the ability to penetrate into the intricate side wall and under-surface spaces in three dimensions. Thus, these coatings extend the operating life of MEMS devices by reducing stiction [44].

12.10.2 MEMS Packaging and Quality Assurance

We return to our first table of the chapter discerning differences in the microcircuit and MEMS arenas in respect to packaging. The hermetic packaging segment of the United States grew out of the US military's use of hermetic packaging. The two documents that serve as a starting point for developing qualification and assurance tests for MEMS packaging are MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification and MIL-STD-883 Test Method Standard.

MIL-PRF-38535 specification establishes general reliability requirements for integrated circuits or microcircuits. The quality and reliability assurance requirements must be met for their acquisition. The intent of this specification is to allow the device manufacturer the flexibility to implement best commercial practices to the maximum extent possible while still providing a product that meets military performance needs. MIL-STD-883 Microcircuit Test Methods establishes uniform methods, controls, and procedures for testing microelectronic devices suitable for use within military and aerospace electronic systems including basic environmental tests. These tests determine robustness to deleterious effects of natural elements and conditions surrounding military and space operations; mechanical and electrical tests; and workmanship and training procedures. This standard applies only to microelectronic devices. However, MEMS devices in microcircuit packages may be tested in accordance with MIL-STD-883.

Package tests should be defined and tailored in respect to the final application, usage, life expectancy, shelf life time, and criticality. Table 12.13 offers some suggested tests to be considered for screening MEMS packages.

Whether following the above prescriptive assurance specifications or deriving new specifications, it is important to consider the application and to then apply the appropriate test. As an example, Analog Device have developed stress tests called "Random Drop" and "Mechanical Drop". "Random Drop" is the random-orientation batch drop of packaged devices from a height of 1.2 m onto a marble surface. The drop is repeated for 10 times, with a basic functionality check done between each drop. In a "Mechanical Drop" test, devices are dropped one by one from a height of 0.3 m onto a marble surface, first in the X-axis, then the Y-axis, and finally the Z-axis directions. An electrical screen is performed, and the drop test procedure repeated from a height of 1.2 m [45]. This work by Analog Devices™ is an excellent example of the need to tailor test plans to achieve a reliable program.

12.11 Case Studies

It is rather difficult to show packaging cases as examples, since most MEMS devices require their own individual package design, matching, for example, the application, the interface, or the environment it will be used. There can be hundreds of examples found in the literature for MEMS packages, each one unique. In this section, we will discuss some of the commercial success stories: the Analog Devices accelerometer,

Table 12.13 Mechanical, electrical and environmental packaging tests for tailoring

Mechanical considerations	
Hermeticity	Specify leak rate of helium (cc/s) at certain pressure differential (atm)
Pin pull test	Specify (lbs, kg, Newtons, or ounces) with direction of force applied
Pin bend test	Specify an angle of bend, direction of bends, no. of cycles. Where to support the pin (P = distance of pivot point from glass) during the test must be defined
Pressure	Specify in (psi, bars, or atm) at certain temperature with pressure differential
Torque	Specify in (in-lbs, ft-lbs, N-cm); definition of support the body and length of engagement of torque wrench to the part is required
Mechanical shock	Specify with a profile of pulse (g) and time (milliseconds)
Vibration	Specify a spectrum and power density
Durability	Specify in no. of mate/un-mate cycles
Thermal cycling	Specify hot (+ °C or °F) and cold temps (−°C or °F), holding time at each temperature (hours or minutes), dwell time between hot and cold zones, and no. of cycles
Thermal shock	Specify with hot and cold temperatures, and holding time at each temperature
Drop test	Specify height, surface, orientation and no. of drops
Electrical considerations	
Insulation resistance (IR)	Specify in ohms (Ω) at a certain voltage level (volts)
Dielectric withstanding voltage (DWV or HI-POT)	Specify current leakage (milliamps) at certain voltage level (volts)
Contact resistance	Specify in (micro-ohms)
Impedance	Specify in ohms (Ω) at appropriate frequencies
Conductivity	Typically known as current carrying capacity and specified in (amps or milliamps)
Environmental considerations	
Solderability	Refers to a military or industry standard, which may require steam aging before testing for specific period of time (h)
Corrosion resistance	Refers to a military or industry standard, which specifies exposure to test chamber for a period of time (h) and salt content (%)
Plating adhesion	Specify as peel-off tape test or bend test. Acceptance criteria must be defined such as "must not peel off" or "must not crack". Baking step may be required before the adhesion test at temperature (°F or C) for a period of time (hours or minutes)
Wire bond strength	Specify in (grams, lbs, or ounces) with a specific wire size and bond surface material
Outgassing	Applies to all components except glass. Glass does not outgas. Specify the type of gases exposed in and around the parts
Ozone exposure	Applies on space applications. Specified exposure time (h), ozone concentration (%)

the TI micro-mirror array, MEMS RF devices, and MEMS microphones, as well as more special applications such as biomedical and space applications.

12.11.1 MEMS Accelerometer

MEMS inertial systems such as accelerometers and gyroscopes can probably be considered the MEMS devices with the largest commercial impact. Driven by the air bag technology, Analog Devices introduced the ADXL50 as the world's first integrated MEMS accelerometer [46, 47]. While the accelerometer is a moving device, the packaging requirements were relatively standard with respect to electronics packaging, e.g. providing electronic interconnects, mechanical and environmental protection, and heat dissipation. A TO5 metal can package, which had demonstrated good reliability in the semiconductor industry, was chosen for the ADXL50.

One of the challenges for the accelerometer industry was the integration of electronics. Two fundamental approaches were followed: integrated single chip solutions using, for example, Analog Device's *i*MEMS® process, and two chip processes, with separate MEMS and electronics die. Motorola has taken the second approach, packaging a capped surface micromachined MEMS structure and an integrated circuit chip in the same plastic package. This is essential since processing the MEMS is not compatible with the processing of the microprocessor control unit. The requirements for the MEMS package are hermetic wafer-level packaging to provide damping control and to protect the MEMS devices from the subsequent dicing and testing; to provide mechanical support; and to isolate stress. In particular, stresses induced by thermal loading due to thermal expansion coefficient mismatches between different packaging materials must be kept at a minimum.

Before the accelerometer can be packaged in a conventional leadframe-and-mold assembly, it must be sealed at the wafer level to be protected. Motorola's wafer-level packaging uses frit-glass bonding [48, 49]. A glass frit/epoxy paste is applied via a screen process, dried and sintered. The cap and the MEMS die are then aligned, pressed together and simultaneously heated above the softening point of the glass. This thermo-compression creates a hermetic seal.

After capping the MEMS die, the accelerometer die and the control signal circuit are mounted to a leadframe flag by standard die bonding techniques and connected via standard wire bonding. The transducer die is passivated with a thin layer of silicone gel die coat. In a final step, the two chips are encapsulated in a standard epoxy mold compound. During cooling, the die coat shrinks faster than the mold, and a 25 μm air gap is created which isolates the transducer die from the surrounding stress.

With the increased use of accelerometers and gyroscopes in the automotive and consumer electronics industry, there was a drive to make smaller devices at a lower cost. Analog Devices developed a wafer-level capping process for their *i*MEMS accelerometers which allows packaging of the device in a very small and thin standard IC package [50, 51]. Matched with the MEMS wafer, sensor and die cut cavities

are etched into the bottom of the cap wafer. Then, a seal glass is screen-printed onto the cap wafer, and the cap wafer is aligned and bonded to the sensor wafer. At that point, the wafer can be diced and the devices are ready for standard assembly in a wide variety of packages, such as the small footprint LFCSP. Using back-grinding of the MEMS wafer, the device can even be packaged in very thin packages [52]. Figure 12.4 shows three methods for packaging an accelerometer.

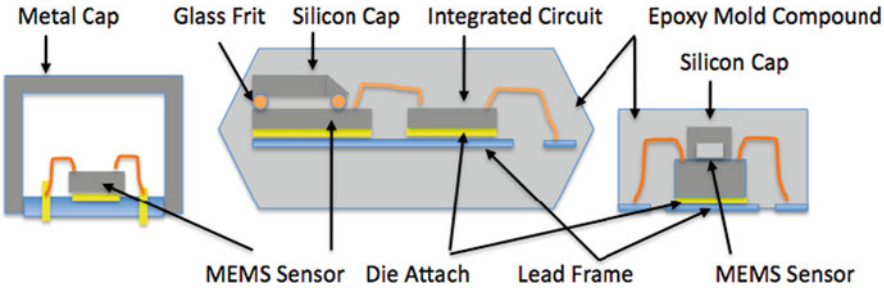

Fig. 12.4 Schematic for an accelerometer packaged in (from *left*): a TO5 metal can, as capped two-chip package, and after wafer-level capping

12.11.2 Micro-mirror Array

One of the biggest success stories in Micro-Opto-Electro-Mechanical Systems or MOEMS is the Texas Instruments Digital Mirror Display (DMD). First invented in 1987 and introduced in 2000, the technology now powers more than 1,500,000 projectors [53, 54]. DMD is an array of mirror-switches, each 16 μm squared, which reflect light in and out of the optical path. Major challenges for this system to be overcome are reliability related, hinge fatigue and memory, stiction, and environmental robustness. The package and its optical window in part provide the environmental robustness. The packages for the TI DMD are metal packages with a lid with a high quality optical window seam-welded hermetically to the package. The package itself contains a getter to absorb residual moisture.

For other applications such as optical routers, several ceramic packages such as high-temperature co-fired ceramic (HTCC) as well as low-temperature co-fired ceramic (LTCC) are being used. Advantages of the LTCC are the lower ceramic processing temperatures (850–1000°C), which allows the use of high conductivity metals instead of refractory metals, as well as the good match of the thermal expansion coefficient with silicon [55].

When greater hermeticity is required, especially in cases where the MEMS devices require vacuum seals and high quality windows, some other packages have been designed attaching windows with a gold/titanium/platinum seal ring on a leadless ceramic chip carrier [56]. The glass window thickness is determined by the package size as well as by the allowable diffusion of hydrogen and helium into the package. Compared to commercial metal–glass covers, these approaches offer better

and undistorted optical transmission and the strains and stresses in the transmission windows of such packages have been modeled and measured.

For wafer-level packaging, a similar approach can be taken for packaged accelerometers, using glass frits to bond a cap on the die. For optical transparency, one proposed approach is to anodic bond a silicon frame onto the cover glass, which then is used as the cap over the MEMS die. An hermetic package using this approach has been reported [57].

12.11.3 MEMS Microphone

A commercial MEMS application with special packaging requirements is the MEMS microphone. The Knowles SiSonic™ MEMS microphone is targeted towards high volume consumer electronic products where cost is a key factor [58]. The advantage of MEMS microphones over low cost electret condenser microphones is the ability to withstand lead-free solder reflow cycles. This ability permits the MEMS microphone to be picked and placed like any other component and thus leads to significantly lower manufacturing costs.

The microphone itself is a fully clamped round polysilicon membrane, about 0.5 mm in diameter and 1 μm thick, micromachined on a standard silicon wafer. The silicon below the membrane has been removed using Deep Reactive Ion Etch (DRIE). The die size is 1.65×1.65 mm. The electronics for the microphone consisting of a series of different amplifiers is built on a separate CMOS chip.

Both die need to be packaged in a single package. This approach is extremely low cost, exposes the MEMS die to the environment, and still protects the MEMS and CMOS die both physically and from unwanted noise. A schematic of the package is shown in Fig. 12.5. It consists of a base, a wall, and a lid laminated together from FR4 PCB material. All inside surfaces are plated to provide a Faraday shield against EMI interference. The MEMS and CMOS die are adhesively bonded to the base and wire bonded with gold wire together as well as to the base. In order to protect the CMOS die from corrosion and incident light, the CMOS die is also encapsulated. A small port, offset from the MEMS die to prevent dirt accumulation or physical damage to the die, serves as acoustic interface. Packaging is performed on 4″ by 4″ panels containing hundreds of microphones and only standard semiconductor packaging equipment is used in the assembly of these microphones.

12.11.4 MEMS Shutters

Many MEMS devices are uniquely designed for special systems. Such an example is the shutters used for the ST-5 MEMS radiator [59, 60] and the James Webb Space Telescope [61]. In both of these systems, large MEMS arrays had to be built, assembled, packaged and tested for space.

For the MEMS package to fly on the New Millennium Program ST-5 Spacecraft by NASA Goddard Space Flight Center and the Johns Hopkins University Applied

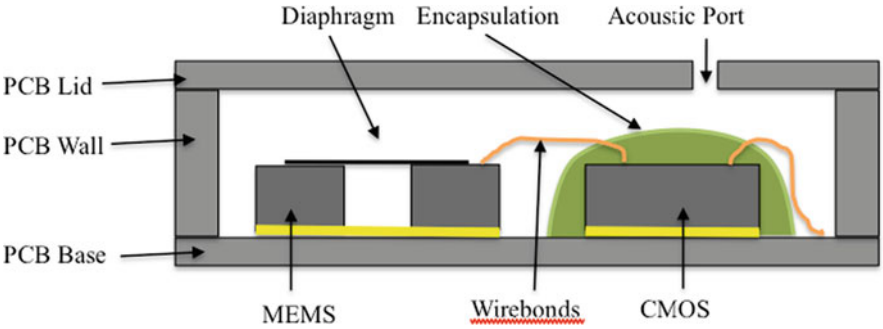

Fig. 12.5 Microphone package cross section

Physics Laboratory, novel packaging techniques were needed to place MEMS based thermal control devices on the skin of a satellite for the Variable Emittance Coating Instrument.

Some unique packaging challenges included the need to protect the shutter elements from particulate contamination during launch due to exterior mounting; to consider the spacecraft electrical surface grounding requirements; and to meet the requirements for thermal operation – high and low emissivities – for the different substrate/surface materials.

The micro-shutter-array (MSA) radiator is located on the bottom deck of the spacecraft. The gold-coated shutters open and close over the substrate and change the apparent emittance of the radiator. The shutter die, each 12.65 × 13.03 mm, consists of arrays of 150 μm long and 6 μm wide shutters driven by electrostatic comb drives, needed to cover as large an area as possible of a 9 cm x10 cm radiator, in order to expose their low emissivity top surface or, when open, the high emissivity substrate.

In order to manage the thermal expansion mismatch between Al and Si for the survival temperature range, – 45 to 65°C, an intermediate carrier made from aluminum nitrite was used. Sets of six die, with wire bonds connecting all the common inputs, were attached to an aluminum nitride substrate with conductive epoxy. Six of these sets were then themselves attached to the aluminum radiator with epoxy. The thermal results associated with opening and closing the shutters are measured by thermistors that are co-located on the underside of the MSA radiator chassis with a heater to allow control of the radiator temperature. A top-view picture of the radiator is shown in Fig. 12.6 and an exploded view of the MSA radiator assembly is shown in Fig. 12.7. The package went through a full space qualification including thermal vacuum, vibration, shock, and acoustic testing at NASA Goddard and finished its mission successfully in 2006, working for the full 3 months of the mission life.

The MEMS shutters for the James Webb Space Telescope (JWST) are of even higher complexity and demonstrate a system which had to be designed around the MEMS device. These shutters expose an infrared spectrometer to different sections

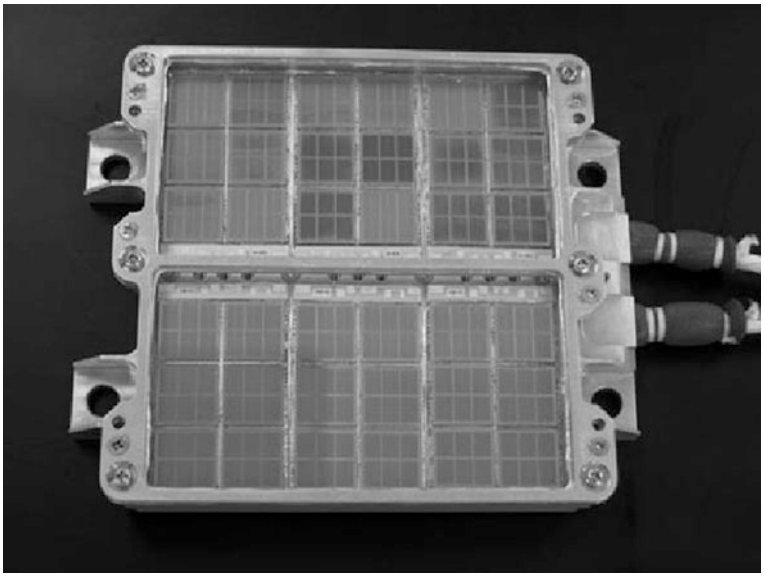

Fig. 12.6 MEMS radiator packaged on six substrates of six chips each

of the image to perform spectroscopy on up to 100 targets simultaneously. One of the requirements was an open fill-factor of more than 70%. The solution was a shutter array, made of silicon with a magnetic coating on the shutters, which is opened by a magnet moving across. The shutters are kept open by an electrostatic electrode, which can be addressed individually for each shutter to keep it open to view or block a portion of the sky. Each of the four micro-shutter arrays contains 171 × 365 shutters and each shutter is 200 micron-long and 100 micron-wide. Besides achieving space qualification (thermal vacuum, shock, vibration and acoustic testing), these shutters have to work at cryogenic temperatures (35 K) and have the ability to open and close more than 100,000 times. One of the challenges, unlike the ST-5 shutters, which are all on a common signal line, is that all shutters on the 38 mm × 35 mm die need to be individually addressed via rows and columns, which requires a large number of connections between the shutter die and the mother board. These connections also need to survive the transition to cryogenic temperatures. NASA's solution was the use of Indium bump bond pads to connect the shutter array to the substrate. A picture of the shutter array mounted into one of the quadrants is shown in Fig. 12.8.

12.12 Summary

This chapter has emphasized the differences between the heritage microcircuit packaging world and the still evolving MEMS packaging arena. The packaging schemes for these devices owe their infrastructure base to the body of knowledge

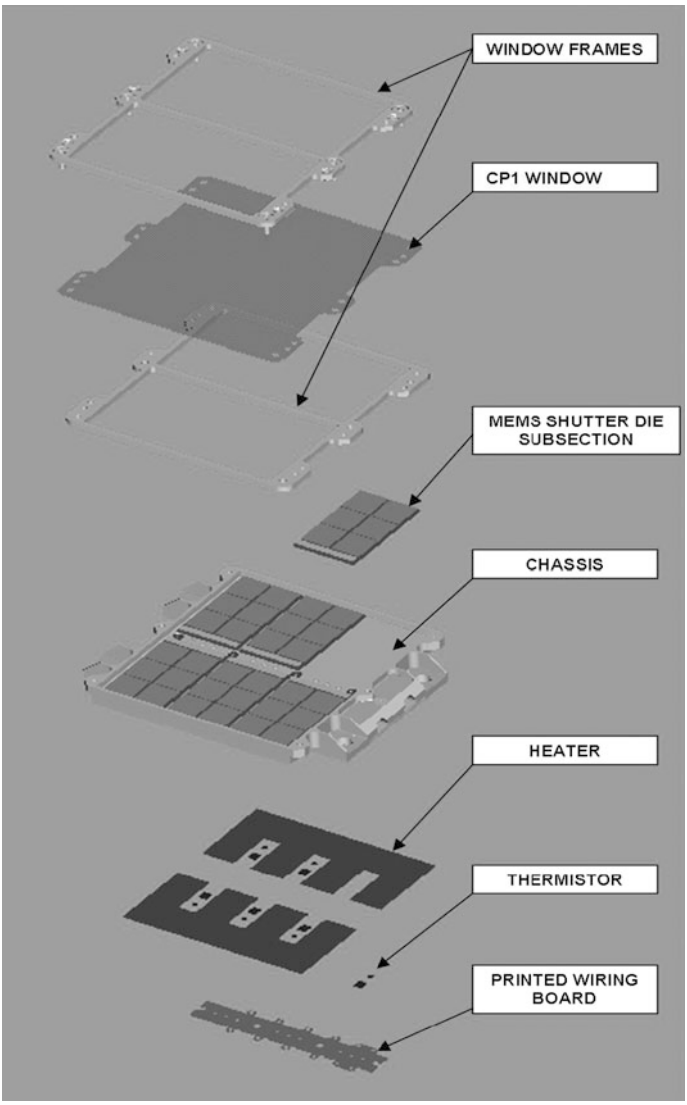

Fig. 12.7 Exploded view of the MSA radiator assembly

surrounding semiconductors and microcircuits. However, the MEMS device yields new complexities which drive new packaging solutions. As opposed to traditional microcircuit chips, MEMS often include moving structures along with the need to have contact with the external environment, driving the requirements for packaging such components. Thus, some functions include interaction with the surrounding environment, such as pressure sensors. This imposes new requisites on packaging, since in regular microelectronics the chip must be protected completely from any

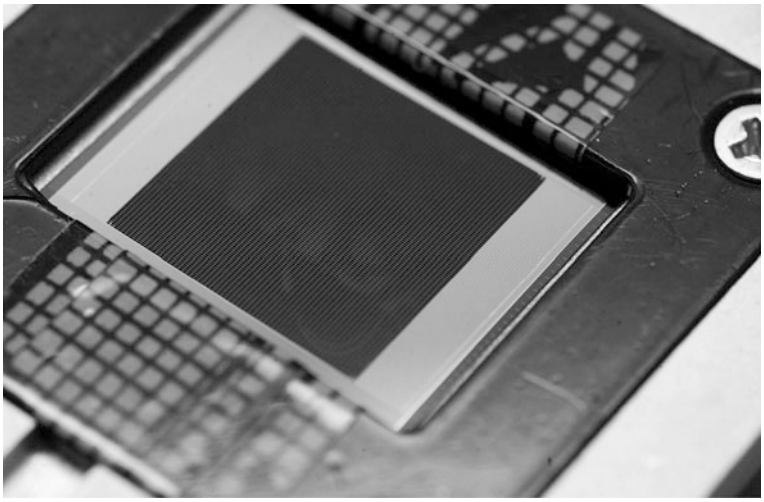

Fig. 12.8 8 JWST shutter array mounted into one quadrant (NASA)

impact from the environment. Packaging also provides mechanical support to the sensitive chip, facilitating the handling of the chip, and simplifying assembly. It will be many years until standardized packaging is the rule rather than the exception with MEMS components.

References

1. K. Persson: Fundamental requirements on MEMS packaging and reliability, advanced packaging materials, 2002 Proceedings, 8th International Symposium, Stone Mountain, GA, pp. 1–7 (2002)
2. Y.L. Low, R.E. Scotti, D.A. Ramsey, C.A. Bolle, S.P. O'Neill, K.C. Nguyen: Packaging of optical MEMS devices, J. Electron. Packaging 125(3), 325 (2003)
3. N.S. Korivie: A Generic Chip-to-World Fluidic Interconnect System for Microfluidic Devices, System Theory, 2007, SSST'07 39th Southwestern Symposium, Macon, GA (2007)
4. D.D. Evans Jr: Advances in MEMS packaging design considerations, Adv. Packaging, April (2004)
5. http://www.spectrum-semi.com/resource/pdf/SO_Material_Properties.pdf (accessed August 11, 2009)
6. http://global.kyocera.com/application/automotive/product/compo/sensor_p.html (accessed August 10, 2009)
7. A. Schubring: Ceramic package solutions for MEMS sensors, Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium, 32nd IEEE, pp. 268–272 (IEEE, San Jose, CA, 2007)
8. A.F. Moor: The case for plastic encapsulated microcircuits in space flight applications, The Johns Hopkins University Applied Physics Lab Technical Digest, Vol. 20, No. 1 (JHUAPL, Laurel, MD, 1999)
9. K. Gilleo: Packaging Materials, Time to Consider Thermoplastic Materials for Electronic Packaging. (2005) http://www.thomasnet.com/white-papers/abstract/100965/time-to-consider-thermoplastic-materials-for-electronic-packaging.html#null (accessed August 11, 2009)

10. K. Baert, P. De Moor, H. Tilmans, J. John, A. Witvrouw, C. Van Hoof, E. Beyne: Trends in Wafer Level Packaging of MEMS, MEMS Packaging Solutions, 29 June, Advanced Packaging (2009)
11. P. Lindner: http://ap.pennnet.com/display_article/334827/36/ARCHI/none/INDUS/1/Packaging-Requirements-Key-to-Advancing-Wafer-Bonding-Technology/
12. A.A. Hamzah, J. Yunas, B.Y. Majlis, I. Ahmad: Sputtered encapsulation as wafer level packaging for isolatable MEMS devices: A technique demonstrated on a capacitive accelerometer, Sensors 8(11), 7438–7452 (2008)
13. A. Partridge, A.E. Rice, T.W. Kenny, M. Lutz: New Thin Film Epitaxial Polysilicon Encapsulation for Piezoresistive Accelerometers, Proceedings of the 14th IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2001), Interlaken, Switzerland pp. 54–59 (2001)
14. C. Rusu, S. Sedky, B. Parmentier, A. Verbist, O. Richard, B. Brijs, L. Geenen, A. Witvrouw, F. Lärmer, F. Fischer, S. Kronmuller, V. Leca, B. Otter: New low-stress PECVD poly-SiGe layers for MEMS, J. Microelectromech. Syst. 12(6), 816–825 (2003)
15. K.S. Lebouitz, A. Mazaheri, R.T. Howe, A.P. Pisano: Vacuum encapsulation of resonant devices using permeable polysilicon, Proceedings of the 12th International Conference on Micro Electro Mechanical Systems (MEMS'99), Orlando, FL pp. 470–475 (1999)
16. A. Stehle, G. Georgiev, V. Ziegler, B. Schoenlinner, U. Prechtel, H. Seidel, U. Schmid: Glass cap packaged high isolating Ka-band RF-MEMS switch, Mikrosystemtechnik, Produktion von Leiterplatten und Systemen. 11(2009)
17. A. Schubring: Ceramic package solutions for MEMS sensors, Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium, 32nd IEEE, pp. 268–272 (IEEE, San Jose, CA, 2007)
18. M.J. Zasowski, G. Lovitz, J.J. Alfano: Visi-LidTM: Transparent Combo-Lids®Heiner Lichtenberger, Abstract http://www.williams-adv.com/documents/visilid.pdf (accessed November 1, 2010)
19. H.L. Hvims: Conductive adhesives for SMT and potential applications, IEEE Trans. Compon. Packaging Manuf. Tech. B 18(2), 284–291 (1995)
20. O. Rusanen, J. Lenkkeri: Reliability issues of replacing solder with conductive adhesives in power modules, IEEE Trans. Compon. Packaging Manuf. Tech. B 18(2), 320–325(1995)
21. T. Tuhus, A. Bjomeklett: Thermal Cycling Reliability of Die Bonding Adhesives, 1993 IEEE Annual International Reliability Physics Symposium Digest, March 23–25, pp. 208 (1993)
22. K. Yalamanchili, A. Christou: Finite Element Analysis of Millimeter Wave MMIC Packages Subjected to Temperature Cycling and Constant Acceleration, 1993 GaAs REL Workshop Programs and Abstracts, October 10 San Jose, CA (1993)
23. R.D. Gerke, D.M. Wesolek: MEMS packaging for space applications in MEMS and microstructures in aerospace applications (R. Osiander, M.A. Darrin (Eds.) CRC Press/Taylor and Francis, Boca Raton, FL, pp. 269–288 2006)
24. R. Pelzer, D. Teomim, G. Perlberg, V. Dragoi: Technologies for Microdevice Packaging Requirements for MEMS and MOEMS, http://ap.pennnet.com/display_article/209837/36/ARTCL/none/none/1/Technologies-for-Microdevice-Packaging/ (accessed 31 Aug 2009)
25. N. Maluf: An Introduction to Microelectromechanical Systems Engineering (Artech House, Boston, MA, 2000)
26. E. Weise: Tape Automated Bonding, a forgotten interconnect technology? Microbonding SA, 2103 Noiraigue Scopehttp://www.microbonding.com/tldpap.PDF
27. N.P. Kim, M.J. Holland', M.H. Tanielian, R. Poff: MEMS Sensor Multi-chip Module Assembly with TAB Carrier Pressure Belt for Aircraft Flight Testing, Boeing Phantom Works, Boeing Commercial Airplane Group, Flight Test, Seattle, WA (2002)
28. K. Gilleo: Flex-Based Packaging Solutions – From CSPs to MEMS ET-Trends, gilleo@ieee.org
29. http://www.williams-adv.com/packagingMaterials/bonding-wire-ribbon.php (accessed 8-10-2009)

30. M.G. Pecht, R. Agarwal, P. McCluskey, T. Dishough, S. Javadpour, R. Mahajan: Electronic Packaging Materials and Their Properties (CRC Press, Boca Raton, FL, 1998)
31. http://www.williams-adv.com/packagingMaterials/bonding-wire-ribbon.php (accessed 8-10-2009)
32. Michael P. Larsson, Richard R.A. Syms: Self-aligning MEMS in-line separable electrical connector, J. Microelectromech. Syst. 13(2), 365 (2004)
33. http://www.packaginggraphics.net/plastic-resins.htm (accessed 8-10-2009)
34. K. Gilleo, G. Pham Van Diep: Step 10: Encapsulation Materials, Processes and http://ap.pennnet.com/Articles/Article_Display.cfm?Section=Articles&Subsection=Display&ARTICLE_ID=213896 advanced packaging (accessed August 11, 2009)
35. V. Danelle, M. Tanner, R. Ramesham (Eds.): Infrared Laser Deposition of Teflon Coatings on Microstructures, Proceedings, Vol. 6111, Reliability, Packaging, Testing, and Characterization of MEMS/MOEMS 611104(2006)
36. F.F. Faheem, K.C. Gupta, Y. Lee: Flip-chip assembly and liquid crystal polymer encapsulation for variable MEMS capacitors, IEEE Trans. Microwave Theory Techn. 51(12), 2562–2568 (2003)
37. R.D. Gerke, D.M. Wesolek: MEMS Packaging for Space Applications in MEMS and Microstructures in Aerospace Applications (R. Osiander, M.A. Darrin (Eds.) CRC Press Taylor and Francis Group, Boca Raton, FL, 2006)
38. T. Hsu: Reliability in MEMS packaging microsystems design and packaging laboratory, Department of Mechanical and Aerospace Engineering San Jose State University, San Jose, CA 95192-0087
39. S.S. Walwadkar, P.W. Farrell, L.E. Felton, J. Cho: Effect of die-attach adhesives on the stress evolution in MEMS packaging, Proc. SPIE – Int. Soc. Opt. Eng. 5288, 847 (2003); L. Starman Jr, J. Busbee, J. Reber, J. Lott, W. Cowan, N. Vandelli: Stress Measurement in MEMS Devices, 2001 International Conference on Modeling and Simulation of Microsystems – MSM 2001, p. 398 (2001); X. Zhang, K.-S. Chen, S.M. Spearing: Residual Stress and Fracture of Thick Dielectric Films for Power MEMS Applications, Proceedings of the IEEE Micro Electro Mechanical Systems (MEMS), pp. 164 (2002); S.S. Walwadkar, J. Cho, L.E. Felton, P.W. Farrell: Tailoring of stress development in MEMS packaging systems, Mater. Res. Soc. Symp. Proc. 741, 139 (2002)
40. J.A. Walraven: Failure Mechanisms in MEMS, IEEE International Test Conference (TC), Charlotte, NC p. 828 (2003)
41. S.B. Brown, W. Van Arsdell, C.L. Muhlstein: Materials reliability in MEMS devices, Int. Conf. Solid-State Sens. Actuators Proc. 1, 591 (1997)
42. J.A. Chiou, S. Chen, J. Jiao: Humidity-induced voltage shift on MEMS pressure sensors, J. Electron. Packaging, Trans. ASME 125(4), 470 (2003)
43. M.P. de Boer, J.A. Knapp, J.M. Redmond, T.A. Michalske, R. Maboudian: Adhesion, Adhesion Hysteresis and Friction in MEMS Under Controlled Humidity Ambients, American Society of Mechanical Engineers, Materials Division (Publication), MD 84, Anaheim, CA, p. 127 (1998)
44. N. Gunda, S.K. Jha, S.A. Sastri: Anti-stiction coatings for MEMS devices, Adv. Mater. Process. 162(9), 27 (2004)
45. K.M. Delak et al.: Analysis of manufacturing scale MEMS reliability testing, Proceedings of SPIE MEMS Reliability for Critical and Space Applications, vol. 3880, p. 165 (Sep 21–22, Cambridge, MA 1999)
46. K.P. Harney: Standard semiconductor packaging for high reliability low cost MEMS applications, Proceedings of SPIE 571, 1–8 Reliability, Packaging, Testing and Characterization of MEMS/Moems IV (2005)
47. F. Goodenough: Airbag Boom When IC Accelerometer sees 50G, Electronic Design August 8, 45–56(1991)
48. Gary Li, Ampere A. Tseng: Low stress packaging of a micromachined accelerometer, IEEE Trans. Electron. Packaging Manufact. 24(1), 104–108 (2001)

49. S.A. Audet, K.M. Edenfeld, P.L. Bergstrom: Motorola wafer-level packaging for integrated sensors, Micromach. Dev. 2, 1–3 (1997)
50. L.E. Felton, M. Duffy, N. Hablutzel, P.W. Farrel, W.A. Webster: Low Cost Packaging of Inertial MEMS Devices, Proceedings of the 36th International Symposium on Microelectronics, Boston, MA, pp. 402–406 (2003)
51. L.E. Felton, N. Hablutzel, W.A. Webster, K.P. Harney: Chip scale packaging of a MEMS accelerometer, Proceedings of the 54th Electronic Component and Technology Conference, vol. 1, pp. 869–873 (2004)
52. E.S. Lacsamana, R.M. Navarro, M.G. Mena, L.E. Felton, W.A. Webster: Very thin packaging of capped MEMS accelerometer device, Proceedings of the 7th Electronic Packaging Technology Conference, vol. 1, pp. 5, 7–9 (2005)
53. P.F. Van Kessel, L.J. Hornbeck, R.E. Meier, M.R. Douglass: MEMS-based projection display, Proc. IEEE, 86(8), 1687–1704 (1998)
54. M.R. Douglass: DMD reliability: A MEMS success story, Proc. SPIE – Int. Soc. Opt. Eng. 4980, 1–11 (2003)
55. Y.L. Low, R.E. Scotti, D.A. Ramsey, C.A. Bolle, S.P. O'Neill, K.C. Nguyen: Packaging of optical MEMS devices, J. Electron. Packaging, Trans. ASME 125(3), 325–328 (2003)
56. T.F. Marinis, J.W. Soucy, J.G. Lawrence, R.T Marinis, R.J. Pryputniewicz: Vacuum sealed MEMS package with an optical window, Proceedings – Electronic Components and Technology Conference (ECTC) D, pp. 804–810 (2008)
57. C. Yang, A. Xu, Y. Wang: Wafer level hermetic packaging of MOEMS devices, Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium, San Jose, CA, pp. 294–297 (2007)
58. Peter V. Loeppert, Sung B. Lee: SiSonicTM – The First Commercialized MEMS Microphone, Technical Digest of the 2008 Solid-State Sensors, Actuators, and Microsystems Workshop, Lyon, FR, pp. 27–30 (2008)
59. R. Osiander, J.L. Champion, M.A. Darrin: MEMS in aerospace applications – Thermal control shutters, Proc. SPIE – Int. Soc. Opt. Eng. 4587, 7–13 (2001)
60. R. Osiander, S.L. Firebaugh, J.L. Champion, D. Farrar, M.A. Darrin: Microelectromechanical devices for satellite thermal control, IEEE Sens. J. 4(4), 525–531 (2004)
61. M.J. Li, I.S. Aslam, A. Ewin, R.K. Fettig, D. Franz, A.S. Kutyrev, S.H. Mosley, C. Monroy, D.B. Mott, Y. Zheng: Fabrication of microshutter arrays for space application, Proc. SPIE – Int. Soc. Opt. Eng. 4407, 295–303 (2001)

Chapter 13
Surface Treatment and Planarization

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Abstract Released structures, structures that move, free surfaces, and surfaces that contact one another in operation are all common in MEMS devices. Free surfaces on MEMS elements are crucial to device performance; hence, surface characteristics must be well controlled during release processes. In this chapter, materials and processes pertinent to device surfaces are discussed in seven main sections. Case studies and examples illustrate the processing details. The first section centers on release processes that create the free device surface, including surface treatments to prevent stiction. Tools for surface analysis are discussed in the second section, and the third section focuses on (undesired) adhesion of MEMS structures, i.e. stiction (Sections "Release Processes and Surface Treatments to Prevent Stiction", "Surface Analysis", and "Adhesion and Friction of MEMS", in this chapter).

As MEMS diversify into chemical, analytical, and biomedical applications, MEMS devices interface with chemical and biological environments, making the free surface between MEMS elements and the environment crucial to performance. The chemistry of surface treatments and the variety of substrate materials constitute a distinct field for surface design and processing of MEMS devices. The functionalized surface must respond to changes in the environment and translate those changes into measurable signals. Accordingly, the fourth and fifth sections describe chemical and biological treatments to create appropriately functionalized surfaces (Sections "Chemical Modification of MEMS Surfaces" and "Surface Considerations for Biological Applications", in this chapter).

As light interacts with MEMS devices, three optical parameters are relevant to performance: reflection, transmission, and absorption. The design of optical coatings to meet the optical requirements of MEMS applications is discussed in Section "Surface Coating for Optical Applications", in this chapter. The materials and processes for optical coating and surface requirements are also discussed.

The final section, Section "Chemical Mechanical Planarization", in this chapter, concerns chemical mechanical planarization (CMP) for MEMS applications. MEMS structures with high aspect ratios are often created to achieve specific

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performance objectives, creating raised topography. CMP is required to level the surface for subsequent microlithography. Details of the CMP process for various materials and design criteria are also described.

13.1 Release Processes and Surface Treatments to Prevent Stiction

As described in earlier chapters, a number of fabrication techniques are employed in microsystems technology. Among them are bulk micromachining, surface micromachining, and LIGA [1–3]. Although these methods employ lithographic, etching and deposition techniques that are substantially similar to those employed in IC device fabrication, the mechanical nature of MEMS devices introduces new production and reliability issues. Foremost among these is stiction-related failure. The inherently large surface area-to-volume ratio of surface microstructures causes these devices to be vulnerable to adhesion, either to the underlying substrate or to adjacent microstructures [4–13]. The term *stiction*, borrowed from the disk-drive industry, is used to describe this phenomenon, because the restoring forces in micromechanical devices generally have both tangential and vertical components.

Stiction can occur both in the production phase and during device operation. Consider, for example, the process of surface micromachining, which is probably the most flexible and widely used fabrication method. The basic steps in the process are illustrated in Fig. 13.1. The final step of sacrificial layer removal is called the "release step." If the release process occurs from solution, the surface tension

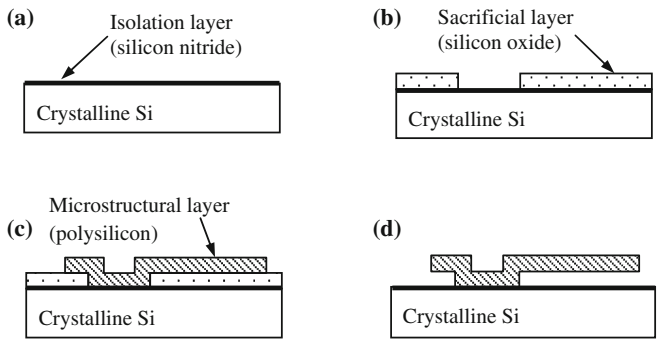


Fig. 13.1 Schematics of basic steps employed in a surface micromachining fabrication process. First, the substrate is typically coated with an isolation layer (**a**) that protects it during subsequent etching steps. A sacrificial spacer layer is then deposited on the substrate and patterned (**b**). The microstructural film is then deposited and etched (**c**). Finally, selective etching of the sacrificial layer releases the microstructures, creating the freestanding micromechanical structures such as the cantilever beam shown in cross section in (**d**) [8]. Reprinted with permission. Copyright 1993 Elsevier

of the draining rinse liquid draws the microstructure into contact with the underlying substrate, leading to "release stiction." Stiction occurring later during operation is generally called "in-use stiction" and is due to intentional or accidental contact between microscopic parts. As implied by the term stiction, MEMS surfaces generally undergo both normal and sliding contact, so friction and wear are also important issues [14–17], limiting both the production yield and the useful lifetime of many microdevices.

Strong adhesion is generally caused by capillary, electrostatic and van der Waals forces, and in some cases by "chemical" forces such as hydrogen bonding and solid bridging. Treatments that render the surfaces hydrophobic can be used, eliminating capillary forces. Such treatments offer varying degrees of thermal and chemical stability, surface hardness, wear resistance, and electrical conductivity. Electrical properties and chemical stability are factors to consider when trying to minimize electrostatic forces (e.g., charge trapping). Lastly, van der Waals forces are results of the polarizability of a medium and as such cannot be eliminated. Their effect can, however, be mitigated by appropriate surface texturing. We mention only in passing that retardation effects transform the van der Waals force into the so-called Casimir force at large body separation (several tens of nm). Therefore, while the Casimir force, by definition, *does not act at contact*, and thus cannot strictly be considered a player in stiction failure, it can contribute significantly to the contact pressure in those cases when the microstructure contact occurs at high aspect ratio asperities (e.g., for very rough surfaces) [18].

Fabrication processes severely constrain surface treatments [19]. This implies that the first and most important factor in stiction prevention is good design. A good design considers the mechanical response of a device, in order to avoid or minimize surface contacts. A secondary factor is a good material choice, but this is often constrained by various other considerations (including cost and available infrastructure). The approach of last resort is to treat surfaces during, or right after, the microstructure release. It is the easiest approach, since it has the least impact on the front-end fabrication steps, but it is also the approach that carries the highest risk of compromising reliability and production yield. A back-end coating process must be *conformal* to ensure uniform deposition in areas that are not in the line of sight. It must also account for the thermal budget of eventual packaging and bonding processes (which often require thermal stability in excess of 300°C). Finally, one cannot overemphasize that all too often, stiction failure is the unintended (but foreseeable) consequence of poor design. The surface treatments discussed in this chapter are not intended as a substitute for good design practice.

Release processes and their specific recipes must be developed and optimized based on the combinations of structural and sacrificial materials involved. Examples include metal and polymer (e.g., aluminum and hardened photoresist), metal and metal (e.g., nickel and copper), semiconductor and oxide (e.g., silicon and silica), or semiconductor and semiconductor (e.g., silicon carbide and silicon) [1–3, 13, 20, 21]. Polycrystalline silicon, deposited by low-pressure chemical vapor deposition (LPCVD), is used frequently in surface micromachining, with an oxide film as the sacrificial layer and an oxide or nitride film as the isolation layer. We will discuss

this combination of materials in detail to illustrate the subtleties involved in the choice of a release process.

13.1.1 Wet Chemical Release Techniques

Silicon oxide sacrificial films are etched by liquid hydrofluoric acid (HF). HF also etches silicon nitride, although relatively more slowly, and usually has a negligible effect on polysilicon. If long etch times are needed in order to etch hard to reach, recessed areas, hydrochloric acid is added to the etching solution in a 1:1 ratio with HF to prevent chemical attack of the silicon nitride insulation layer. This is followed by one or more rinses in water to displace the etch solution and etch residue, and drying. The oxidized polysilicon surface that results from the rinse and dry process is hydrophilic, with a water contact angle in the range from zero to 30°. Capillary forces are thus generated by the meniscus formed between the suspended structure and substrate. These forces may be sufficiently strong to collapse the microstructure onto the substrate. The oft-ensuing permanent adhesion is called release stiction. Release stiction can be further magnified by solid bridging of dissolved sacrificial residues from the rinse solution [5–7].

Several release approaches, such as freeze-sublimation drying and supercritical drying, can help to minimize or eliminate release-related stiction [22–31]. These approaches share the common feature of avoiding meniscus formation. The most commonly adopted approach is supercritical drying using CO_2 [24], with commercial tools now available for realizing this process at the wafer level [30]. However, it is preferable to use freeze-sublimation drying [23] because it is a simpler process. An alternative approach to wet release is to make the microstructure surfaces hydrophobic or nonwetting, e.g., by formation of an organic self-assembled monolayer (SAM) film [29]. These coatings eliminate the capillary attraction that collapses the microstructures upon drainage of the wetting liquid phase, and have the additional appeal of providing in-use stiction relief.

13.1.2 Dry Release Techniques

The difficulties inherent in the drying of microstructures can be avoided altogether if a dry release process is available. This is generally the case when the sacrificial material is a polymer, which can be removed by an oxygen plasma etch. A wet-dry hybrid release scheme is sometimes also employed, whereby a partial undercutting of the surface microstructure is performed and the voids are backfilled with a polymer layer. The polymer holds the microstructures in place after the wet etch of the sacrificial layer and can be removed with a dry etch [25, 26].

Increasingly popular is the use of vapor HF to etch away sacrificial SiO_2 [27, 28]. This process is an attractive alternative to liquid phase HF etch, not only because it eliminates the need for drying the microstructures, but also because it is more

cost effective and generates much less chemical waste. As a consequence, a variety of commercial tools are now available to carry out this process. Note that vapor HF is particularly aggressive toward nitride, so with this approach, exposed silicon nitride must be absolutely avoided. Despite this limitation, vapor HF release [31] is successfully employed by large-volume manufacturers like Bosch in their inertial sensors technology.

Other dry release chemistries are enabled by suitable choices of sacrificial materials. For example, polysilicon can be used as a sacrificial, rather than structural, layer in the fabrication of ceramic devices, such as silicon carbide MEMS. (SiC is used as structural material in high value applications, such as MEMS for harsh environment.) In this case, xenon difluoride can be used very effectively as a dry etchant for the sacrificial polysilicon [32].

In summary, dry release processes are recommended because they are economical and environmentally friendly. Consideration of the choice of release process must take place at the design level, given the materials selection limitations imposed by the relatively small number of dry release chemistries that are commercially available for large scale, high volume production.

13.2 Surface Analysis

A number of analytical techniques have been utilized to monitor surfaces and thin films at various stages of the microfabrication process (Fig. 13.1), including the release process. Here we briefly summarize several techniques that are most commonly employed, starting with those used for chemical characterization, followed by those used for physical characterization of surfaces.

13.2.1 Surface Chemical Composition

13.2.1.1 X-Ray Photoelectron Spectroscopy (XPS or ESCA)

X-ray photoelectron spectroscopy (XPS, or sometimes called ESCA for electron spectroscopy for chemical analysis) is a powerful technique used to determine the chemical composition and the bonding state of atoms in the near surface region of solids [33]. In an ESCA experiment, X-rays are directed onto a surface, and electrons in the core levels and in the conduction or valence bands are excited. If the electrons have momentum towards the surface and sufficient energy to overcome the surface potential barrier, they escape into the vacuum (photoelectric process), where they are monitored by an energy analyzer to determine their kinetic energy. For a given photon energy and work function of the spectrometer, a measurement of the photoelectron kinetic energy immediately yields its binding energy. The binding energy of core-level photoelectrons is specific to individual elements, and varies slightly but often measurably according to bonding configuration. ESCA data thus provides information about chemical composition bonding for the surface being

analyzed. Since X-ray photons can penetrate solids to a depth of microns, the surface sensitivity of XPS is limited by the mean free path of the photoelectrons exiting the solid. The mean free paths of the photoelectrons are typically in the range of a few nm, and consequently, the sensitivity of XPS is also of this order. Lower take-off angles can be chosen to further enhance the surface sensitivity; maximum sensitivity is achieved for grazing angles.

A sample XPS spectrum for as-is silicon is shown in Fig. 13.2, in which the intensity recorded by the electron multiplier is plotted as a function of the secondary electron binding energy [34]. The main peaks visible in this plot indicate the presence of silicon, carbon, and oxygen. The peak labels 1s, 2 s, and 2p indicate the core level from which the photoelectron was ejected for that particular element. The results indicate that the silicon surface is hydrogen terminated (i.e. Si-H bonds on surface) and no Si-O bonds exist on the surface.

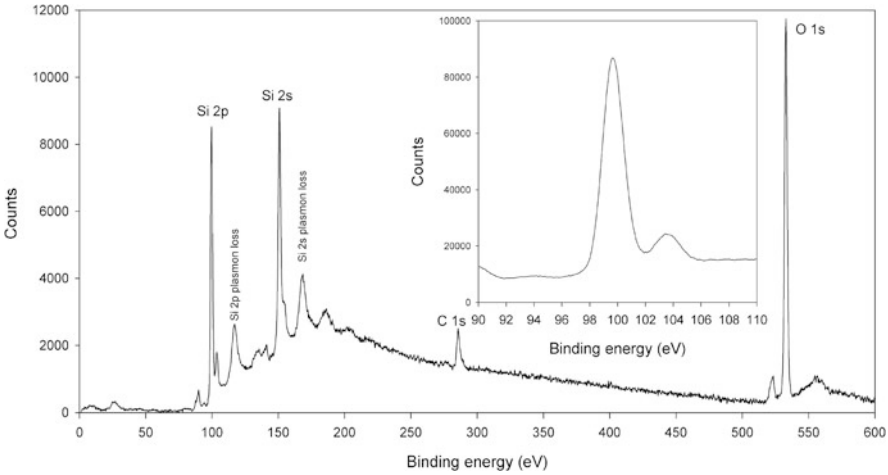


Fig. 13.2 X-ray photoelectron spectrum obtained on Si(100) sample, identifying the presence of carbon and oxygen in addition to Si. The *inset* shows a close-up of the Si 2p region of the spectrum. The small peak at ~103.5 eV signifies Si in a silicon-oxide matrix, highlighting that the sample has a thin layer of oxide on it

13.2.1.2 Scanning Auger Electron Spectroscopy (AES)

Scanning Auger electron spectroscopy (AES) allows one to obtain a chemical image of a surface. The Auger effect is at the heart of this technique [33, 35]. When a material is irradiated by a beam of photons or a beam of electrons with energies in the range of 2–50 keV, a core state electron may be removed, leaving behind a charged vacancy or "core hole". The core hole may be filled by an outer shell electron. The energy lost by the electron transitioning to the lower energy level, which equals the difference in the energies of the two orbitals, may be coupled to a second outer shell electron. If the energy transfer is greater than the electron

binding energy, the electron can be emitted from the solid. Since orbital energies are unique to an atom of a specific element, analysis of the ejected electrons can yield information about the chemical composition of a surface.

Scanning Auger electron microscopy (SAEM) involves rastering a focused electron beam across a sample surface and measuring the intensity of the Auger peak corresponding to a particular element. In this way, high resolution, spatially resolved chemical images of the surface are obtained. In addition, sputtering can be coupled with Auger spectroscopy to perform depth-profiling experiments. Sputtering is typically performed by bombardment with Ar ions of energies up to a few kV. In this case, sputtering removes thin outer layers of the surface so that AES can be employed to evaluate the underlying composition. AES is often used as an evaluation tool on and off fabrication lines in the microelectronics industry, while the versatility and sensitivity of the Auger process makes it a standard analytical tool in research laboratories.

While Auger electron and X-ray photoelectron spectroscopies provide similar information, there are distinct differences between the two techniques. Since the incident electron beam in Auger can be tightly focused, the spot size (or sampling size) in Auger is much smaller than that in XPS, and thus has the capability of identifying fine features on the surface. On the other hand, XPS has the capability to provide detailed information regarding surface chemical structure and bonding through the use of chemical shifts. Although Auger lines also exhibit chemical shifts, these are not generally as large or as well documented as those obtained by XPS. In addition, X-ray radiation used in XPS imparts less damage to the sample surface than does the electron beam used in SAEM. This feature becomes particularly important when using these techniques to analyze soft samples (such as self-assembled monolayers). As mentioned above, the spatial analysis and imaging capabilities of the scanning Auger microprobe make it a very useful complementary technique to XPS.

13.2.1.3 Energy Dispersive X-Ray Spectroscopy (EDS or EDX)

Energy dispersive X-ray spectroscopy is another analytical technique used for the elemental analysis or chemical characterization of a sample [36]. Most commonly, a high-energy electron beam (e.g., in a scanning electron microscope, where EDS is often offered as an accessory) is focused onto the sample. The incident beam may eject an electron from an inner shell, creating a hole. An electron from an outer, higher-energy shell then fills the hole, and the difference in energy between the two shells may be released in the form of an X-ray. The number and energy of the X-rays emitted from a specimen can be measured by an energy dispersive spectrometer. As the energy of the X-rays is characteristic of the difference in energy between the two shells, and of the atomic structure of the element from which they are emitted, this technique allows the elemental composition of the specimen to be measured. A chemical map of the surface is obtained by scanning the electron beam across the sample and measuring X-ray intensity.

13.2.1.4 Secondary Ion Mass Spectroscopy (SIMS)

Secondary Ion Mass Spectroscopy can be used to determine the chemical composition of the near surface region [37]. The technique involves the removal of surface species by the process of sputtering, collecting the ejected (so-called secondary) ions and analyzing them with a mass spectrometer. Sputtering is performed by bombarding the sample with energetic ions. The incident ions set off a series of collisions within and between target atoms (the so-called "collision cascade"). If atoms reach the target surface with an energy greater than the surface binding energy, they can be ejected. SIMS is arguably the most sensitive surface analysis technique, capable of detecting elements present in the parts per billion or less range. It can also detect all elements, including hydrogen. Since it involves the removal of surface species, one can also obtain a depth profile of the sample (i.e., composition as a function of depth). For the same reason, however, it is a destructive technique.

13.2.2 Surface Structure and Morphology

13.2.2.1 Atomic Force Microscopy (AFM)

Atomic force microscopy is a powerful technique for surface analysis [38]. It employs a sharp probe tip mounted at the end of a compliant cantilever. With the cantilever held fixed, the surface of a sample is brought close to the tip by a piezo-driven motorized stage. (The opposite situation is also possible, where the sample is held fixed and the cantilever brought close to it by the piezo stage.) At short enough surface-tip separation, surface forces (such as dispersion forces, electrostatic forces, capillary forces, hydrogen bonding and other chemical forces, magnetic forces and forces of entropic origin, like solvation forces) become effective and can be measured. Indeed, a surface-tip force leads to a deflection of the cantilever which is measurable, e.g., by optical means, whereby a laser beam is reflected from the top surface of the cantilever and detected by a photodiode array. Other detection methods include optical interferometry, capacitive sensing, or piezoresistive AFM cantilevers.

Constant force imaging is preferred to constant height imaging, in order to avoid the tip crashing into a sample with abrupt topographic features. This imaging mode is achieved by a feedback loop. With proper calibration, the feedback response is converted to a topographic image of the sample, normally with sub-nm resolution. The AFM can be operated in several modes, which may be divided into static and dynamic modes. The static mode measurements are usually done in "contact" regime (where the tip senses the repulsive core of the surface potential). In the dynamic "noncontact" mode, the cantilever is made to vibrate at or near one of its resonance frequencies. The oscillation amplitude, phase, and resonance frequency are affected by the tip-sample forces; these changes provide information about the surface force, and thus, about the chemical and topographic characteristics of the sample. Atomic force microscopy can also be used to measure the adhesion or

pull-off force for a given tip-surface combination. The data obtained using this technique is in the form of an AFM force curve, in which the deflection of the cantilever beam holding the AFM tip is measured as the tip approaches, makes contact with, and withdraws from a surface. Additionally, AFM can be used to measure frictional properties of the sample by tracking the lateral deflections of the cantilever as the probe tip is scanned perpendicular to the longitudinal axis of the cantilever at various applied loads. A hardened AFM tip (e.g., diamond or diamond-like carbon coated) can also be used to estimate the hardness of the sample through nanoindentation experiments.

13.2.2.2 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) employs an electron beam, which typically has an energy ranging from a few hundred eV to 40 keV [36]. The beam is focused onto the sample to a spot size in the range of a few to less than 1 nm. The energy exchange between the electron beam and the sample results in the reflection of high-energy electrons by elastic scattering, emission of secondary electrons by inelastic scattering and the emission of electromagnetic radiation, each of which can be detected by specialized detectors. The beam is scanned across the sample while the secondary electrons are detected synchronously.

When compared to optical microscopy, this technique offers several advantages, including a larger depth of focus and higher magnification, which are of great value for MEMS inspection. The electrostatic interaction between the electron beam and MEMS structures is sometimes employed to actuate the structures, thus allowing researchers to probe MEMS dynamics while directly observing the structures under high magnification.

13.2.3 Surface Energy Measurements

Contact angle measurements can be used to estimate surface energy of solids by measuring the contact angle, θ, of a liquid drop on a solid surface [39, 40]. This is the angle formed by the liquid-vapor surface and the solid-vapor surface, measured in the liquid such that a zero value of the contact angle denotes complete wetting of the solid surface by the liquid. A common method for contact angle measurements is the "sessile drop" method, in which a liquid drop is placed onto a solid surface and the resulting tangent angle at the liquid/solid/vapor intersection point determines the contact angle. The interaction energies between solid and vapor, solid and liquid and liquid and vapor are related through Young's equation [39]. Contact angle measurements are typically made with pure liquids in saturated vapor, and often advancing and receding angles (the angles measured when the liquid drop is advancing or receding over the surface), or the average of the two, are reported. If the liquid interacts strongly with the solid surface (e.g., water on oxidized silicon, a hydrophilic surface), the droplets spread out on the solid surface, yielding a water contact angle close to 0°. If the liquid is water, the wetted surface is said to

be completely hydrophilic. Less strongly hydrophilic solids exhibit water contact angles up to 90°. A hydrophobic surface is one on which the water contact angle is larger than 90°. On very hydrophobic surfaces, water contact angles as high as 150° can be observed [41], reaching almost 180° in extreme cases. These surfaces are termed "superhydrophobic," and can be obtained in situations where surfaces have been appropriately micropatterned to achieve multiscale roughness. The contact angle provides information about the interaction energy between surface and the liquid. Unlike XPS, this technique probes large (mm-sized) surface areas, typically larger than MEMS devices; therefore, it needs to be implemented on suitably prepared surfaces that are representative of the real devices.

13.3 Adhesion and Friction of MEMS

13.3.1 Measurements of Adhesion and Friction

A number of microinstruments have been specifically developed to examine the surface-surface interaction involved in silicon microstructures [42–53]. These are described below.

13.3.1.1 Cantilever Beam Array Technique

To quantify the adhesion characteristics of microstructures, Mastrangelo and Hsu developed a simple microinstrument to measure the work of adhesion between two contacting surfaces [42]. The instrument involves an array of single-clamped beams with varied lengths parallel to the surface. This is commonly referred to as a cantilever beam array (CBA) test structure, a SEM picture of which is shown in Fig. 13.3b. A schematic side-view of a single cantilever beam is shown in Fig. 13.3a.

To measure the work of adhesion, the beams are brought into contact with the underlying substrate. Once the applied actuation force is removed, the beams begin to peel themselves off the surface. In the original analysis [42], beams shorter than a characteristic length (so-called detachment length, ℓ_d) were stiff enough to free themselves completely from the underlying surface, while beams longer than this characteristic length remained adhered to the surface. Based on this definition, the beams in the transition region were adhered to the substrate only at their tips. By balancing the elastic energy stored within the beam and the beam-substrate interfacial energy, the work of adhesion, W, between the two surfaces can be calculated using the following equation:

$$\mathsf{W} = \frac{3}{8}\frac{\mathsf{E}h^2t^3}{\ell_d^4} \tag{13.1}$$

where E is Young's modulus, h is the spacing between the beam and the substrate, and t is the thickness of the polysilicon beams. Since then, a number of different schemes have been developed to relate the measurements to the work of adhesion

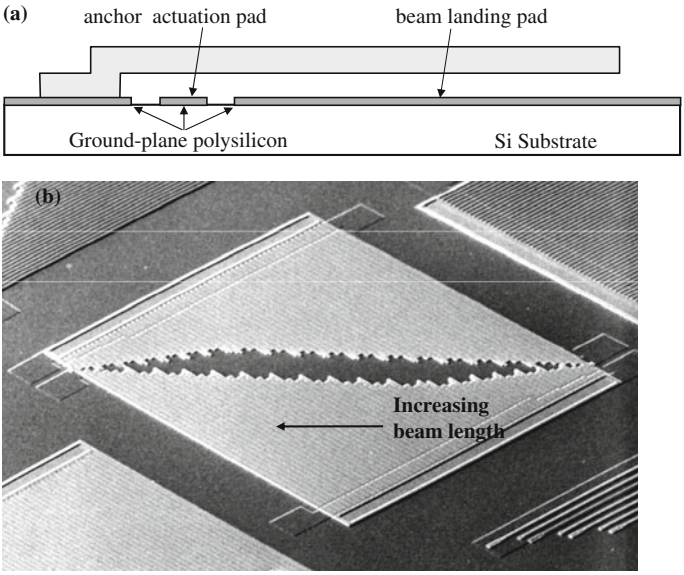


Fig. 13.3 Cantilever beam array: (**a**) schematic side-view of a single cantilever beam, and (**b**) SEM picture [6]. Reprinted with permission. Copyright 1997 AIP

[43–45]. If the two contacting surfaces are perfectly flat and indistinguishable, then the measured work of adhesion is twice the surface energy of the individual surfaces [40, 43]. However, the polysilicon surfaces used in micromachining are most often rough, and thus the CBA method provides information about the *apparent* work of adhesion since the actual area of contact is different from the projected area of contact.

13.3.1.2 Double-Clamped Beam Array Technique

Another test structure used to probe adhesion in MEMS consists of an array of double-clamped cantilever beams with varying lengths [46]. By bringing the beams in contact with the underlying substrate and removing the external actuation, a transition is observed between adhered and freestanding beams. Since the stored elastic energy in the double-clamped beam contains a stretching term in addition to the bending term, the equation relating detachment length to work of adhesion is modified accordingly:

$$\mathsf{W} = \frac{\pi^4}{4}\frac{\mathsf{Eh}^2\mathsf{t}^3}{\ell_{\mathrm{d}}^4} + \frac{\pi^2}{4}\frac{\varepsilon\mathsf{Eh}^2\mathsf{t}}{\ell_{\mathrm{d}}^2} \tag{13.2}$$

where ε is the residual strain in the beams. By measuring the detachment length, the work of adhesion can be found, assuming the other parameters are known. In contrast to the cantilever beam array microinstrument, this test structure requires an independent measure of the residual strain in the beams. As described in [49], this

microinstrument can also be used to determine the adhesion *force*, which from the design point of view is sometimes more desirable than adhesion *energy*.

13.3.1.3 Friction Test Structures

A number of microinstruments have been developed to study friction in MEMS [50–53]. As an example, here we describe a device that allows the measurement of the static coefficient of friction between in-plane surfaces. The instrument consists of a shuttle that is suspended above an underlying electrode by a folded beam suspension [50]. The application of a voltage, V_{DC}, to the comb drives causes the shuttle to be displaced by a specified amount. Applying a voltage between the shuttle and the underlying substrate, V_c, pulls the shuttle downwards until the dimples contact the landing pads. By reducing the V_c bias, a threshold voltage, V_t, is reached, at which point the shuttle snaps back to equilibrium. The normal applied force is calculated from the threshold voltage. The tangential force is calculated using the initial displacement of the shuttle and its spring constant. The friction coefficient can then be determined from the normal and tangential forces.

13.3.2 Effects of Surface Roughness

One method used to reduce adhesion is to reduce contact area, as done by Fan et al. by fabricating a micromechanical bushing, or dimple [54]. Another approach is to intentionally roughen (texture) one or both of the contacting surfaces. In this way, the average separation at contact is reduced and hence adhesion is reduced. Examples of this approach include texture etch-back techniques [55] and preferential oxidation of silicon grains at their boundaries [56] to obtain very rough polysilicon surfaces. Yet another scheme is to grow silicon carbide (SiC) nanoparticles (in the tens of nm range) using SiO_2 films deposited from tetraethylorthosilicate [57, 58].

13.4 Chemical Modification of MEMS Surfaces

13.4.1 Treatments for Low Surface Energy

The release solutions described in Section 13.2 do not help alleviate the problem of in-use adhesion. This problem can be addressed by adapting one or a combination of the following strategies:

(i) conservative designs to prevent surfaces from coming into contact whenever possible;
(ii) physical modification of surfaces, as discussed in Section 13.3.2;
(iii) chemical modification of surfaces to reduce surface energy.

The third strategy, referred to as "boundary lubrication," is the most versatile and probably the most actively pursued approach, and will be discussed next.

13.4.2 Siloxane and Silane Treatments

Self assembled monolayers are thin organic films that spontaneously adsorb or bond on solid surfaces [59]. The precursor molecule has three parts. One is a surface-active head group; because of this group, the molecule has the propensity to adsorb on surfaces through covalent or electrostatic interactions. Second is an alkyl chain, which helps in the formation of a densely packed array, due to the resulting van der Waals interaction between the adjacent chains. Third is the tail group that can be varied to impart a variety of functions, such as hydrophobicity or hydrophilicity. For modification of the silicon surface, several monolayer systems have been developed, including alkyl- and perfluoroalkyl-trichlorosilane SAMs ($R\text{-}SiCl_3$), dichlorosilane monolayer films ($R_2\text{-}SiCl_2$), and alkene-based molecular films. Schemes for applying self-assembled monolayers to microstructures have been developed. These monolayers have been shown to eliminate release adhesion, and to significantly reduce in-use adhesion. This approach has been recently reviewed [60, 61]. Specific examples of these films and their resulting properties are summarized in Table 13.1. In addition, a number of two-step monolayer processes have been investigated for MEMS applications [62, 63].

Early schemes for SAM coating of microstructures involved deposition from the liquid phase. However, due to challenges associated with scale-up, vapor-based coating processes have been pursued more recently, although these approaches require a successful release as the starting point. Indeed, SAM deposition from vapor phase has been demonstrated following a separate release process using supercritical CO_2 drying [64–66]. Table 13.2 lists the properties achieved via the vapor phase deposition process. Tools that implement vapor phase antistiction coatings are commercially available [67, 68]. One such tool is referred to as MVD, Molecular Vapor Deposition [67]. It utilizes plasma surface cleaning and proprietary seed layer

Table 13.1 Physical property data for several surface treatments [taken from Ref. 53]

Surface treatment	Water contact angle (°)	Work of adhesion (mJ/m^2)	Static friction coefficient	Thermal stability in air (°C)	Particulate formation
OTS	110	0.012	0.07	225	High
FDTS	115	0.005	0.10	400	Very high
DDMS	103	0.045	0.28	400	Low
1-octadecene	104	0.009	0.05	200	Negligible
Oxide	0–30	20	1.1	–	–

1H,1H,2H,2H-perfluorodecyltrichlorosilane (FDTS); octadecyltricholorosilane (OTS); dimethydichlorosilane (DDMS); 1-octadecene; untreated oxidized silicon

Table 13.2 Selected properties of the DDMS and FDTS monolayers deposited from vapor phase versus liquid phase

Surface treatment	Water contact angle (°)	Work of adhesion (mJ/m^2)	Static friction coefficient	Thermal stability in air (°C)	Particulate formation
V-FDTS	111	0.003	0.12	400	Low/none
L-FDTS	115	0.005	0.10	400	Very high
V-DDMS	102	0.062	0.35	400	
L-DDMS	103	0.045	0.28	400	Low
Oxide	0–30	20	1.1	–	–

Oxide values are given for comparison. V- (L-) denotes deposition from vapor (liquid) phase

deposition to increase the number of active sites on the surface. This is then followed by the vapor deposition of the precursor of interest, based on the intended surface property. In addition to FDTS and DDMS listed in Table 13.2, the tool can deposit coatings based on a wealth of monolayers. Some examples include *1H,1H,2H,2H*-perfluorooctyltrichlorosilane (FOTS), which has properties that are rather similar to those of FDTS. Another monolayer commonly used for surface functionalization is 3-aminopropyltrimethoxysilane (APTMS), which is an example of a hydrophilic surface treatment. Lastly, 3-mercaptopropyltrimethoxysilane (MPTMS) is a mercapto-terminated silane that is useful in thiol based chemistries or as an adhesion layer for deposition of smooth gold.

Another vapor coating approach with enhanced thermal stability was reported by Analog Devices, Inc. [69, 70]. It is based on phenyl-methyl silicone or diphenyl siloxane that has good resistance to temperature and oxidation. A small amount of liquid is placed onto each package before the die is sealed. At elevated temperatures, the liquid evaporates, and the molecules contacting the surface chemically react and bond to it. This process results in a monolayer coating with a high organic content.

13.4.3 Weakly Chemisorbed Surfactant Films

Up to this point, we have emphasized the use of silicon as the structural material, due to its continued dominance. However, many metals and alloys have long been used in applications requiring high reflectivity or low contact resistance. Moreover, metal deposition methods such as electroforming are gaining favor as inexpensive and versatile fabrication methods, and recent research [71] has validated their use in applications in which semiconductor or ceramic materials have been traditionally believed to yield superior performance (such as high Q resonators). Functionalization schemes are readily available for many of these metals, and they can be used to render the surfaces hydrophobic in order to avoid microstructure

adhesion caused by surface forces [72]. Unlike silane coupling, these schemes usually rely on weaker chemisorbed headgroups, such as thiol (suitable for binding to most noble metals, including copper and its oxide) and carboxyl (suitable for binding to aluminum and its oxides, and notably employed in the Texas Instruments digital micromirror device, also known as DMD). Weakly chemisorbed species such as alkanethiols or alkanoic acids possess many advantages with respect to the strongly chemisorbed siloxanes, including the inability to crosslink (which leads to clean, particle-free surfaces after treatment) and the ability to self-heal in response to mild wear. For the latter property to take effect, the presence of a reservoir of precursor molecules is required. This can be accomplished by hermetically packaging the device under the pressure of the precursor. In the case of the TI DMD device, a standard 5-year warranty on a DLP^{TM} (Digital Light Processing) chip implies hundreds of billions of stiction-free impacts, a feat made possible by vapor phase lubrication of the kind just discussed. Additional thiol and silane related surface treatments are discussed in Section 13.5.

13.4.4 Materials Properties and Process Selection Guidance

Despite the large number of coatings now available, it is difficult to identify one treatment as the best surface coating. Tables 13.1 and 13.2 provide a variety of properties for some anti-stiction coatings. As evident from the table, one can choose from a wide range of molecular coatings yielding different degrees of thermal stability, particulate susceptibility and tribological performance. Other considerations that affect the choice of coating are selectivity, lubricity and the very presence of an oxide layer. Because of the wide ranges of film properties and deposition methodologies, and due to the greatly varying end-use applications and processing requirements, no one specific coating technology can be claimed to be "universal". Ultimately, it is the performance of the micromechanical device that will dictate which anti-stiction coating should be utilized, if any. Because it is performance that drives design, this underscores the need to plan for the coating at the microstructure design level.

13.5 Surface Considerations for Biological Applications

BioMEMS is a specialized branch of MEMS dedicated to the design, fabrication and application of MEMS devices that contain or handle broadly-defined biological materials, ranging from natural or synthetic biomolecules, biochemical complexes, and cellular entities to tissue masses. Unlike most conventional MEMS devices that primarily operate in liquid-free environments, BioMEMS devices often operate under conditions that require parts of the devices' solid surfaces to contact liquid media and interact with biological materials. Therefore, specific challenges related

to the interactions between BioMEMS device surfaces and biological materials at solid-liquid interfaces are of special interest in BioMEMS.

Although BioMEMS is recognized as a specialized field, and can be distinguished from conventional MEMS, BioMEMS still utilizes many fundamental concepts, raw materials and processing techniques employed in conventional MEMS. Indeed, in the past several decades, the principles of conventional MEMS have contributed to the rapid development of BioMEMS. However, it should be noted that to ensure proper functioning of BioMEMS devices, some restrictions must be considered when applying principles of conventional MEMS to BioMEMS. First of all, the raw structural materials chosen must be inert and stable when exposed to the liquid media (mainly buffered aqueous media). Additionally, the selected materials must be compatible with biological materials, and non-toxic to living biological entities. The raw materials commonly used to fabricate BioMEMS devices include noble metals (Au, Ag, Pt, etc.), polymers (PMMA, SU-8, PDMS, etc.), silicon, silica (glass, quartz, etc.), and silicon nitride. As these materials are also commonly used in conventional MEMS, it is advantageous that most of the processing techniques well-established in conventional MEMS can be readily applied for the fabrication of BioMEMS devices. Essentially, the diversified and sophisticated physical architectures for BioMEMS devices can be fabricated by the processing techniques developed in conventional MEMS. However, for BioMEMS applications, beyond elaborate architectural designs, the performance and functions of BioMEMS devices are also highly dependent on the interactions of biological materials with device surfaces. Therefore, the surface modification of the pristine surfaces of conventional MEMS materials is a major research topic in the BioMEMS area.

The two main purposes of surface modification in BioMEMS are (i) to reduce undesired non-specific adsorption of biological materials which can cause device degradation or interfere with device transduction and (ii) to generate desired surface properties which can promote device performance or expand device functions. To reduce non-specific adsorption, surface coatings based on bovine serum albumin (BSA) or poly(ethylene glycol) (PEG) are commonly used. To prepare biologically active surfaces, immobilization of biological molecules, such as oligonucleotides, peptides, carbohydrates or proteins (including enzymes and antibodies), is required. Modification of MEMS surfaces for BioMEMS applications is mainly based on bottom-up molecular engineering. The surface modification procedure can be a single-step process. However, for the construction of robust and/or complex structures, multi-step processes are commonly applied. Surface modification by molecular engineering can cause changes in surface wettability and/or surface functionality. Altering surface wettability can generate new surfaces with desired adsorption behaviors, while altering surface functionality can create new surface functional groups for desired chemical reactions.

Surface modification by molecular engineering utilizes the interactions between molecules. The interactions can be covalent or non-covalent. Non-covalent interactions include van der Waals interactions, electrostatic interactions, hydrogen-bonding and certain biological interactions (such as antigen/antibody conjugation, DNA hybridization, etc.). Covalent interactions involve the formation of covalent

bonds. Covalent interactions frequently used for surface modification in BioMEMS are primarily based on certain chemical reactions involving the following five major functional groups: −OH, $-NH_2$, −COOH, −SH, and −CHO. These functional groups are commonly found in natural biomolecules. Moreover, those functional groups can be derivatized to chemical compounds of non-biological origin, and thus can also be found in synthetic biomolecules, cross-linkers, and on modified substrate surfaces. The cross-linkers are defined as the chemical compounds used to generate the linkage between the pristine surface (i.e. the original MEMS device surface) and the outermost materials. The cross-linkers can be heterobifunctional (two different functional end groups) and homobifunctional (same functional groups at the both ends).

13.5.1 Surface Modification Techniques

A generalized surface modification procedure is illustrated in Fig. 13.4. The pristine substrate is the original, clean substrate prior to the surface treatment. After the surface treatment, the chemical compounds containing desired terminal groups are placed at the outermost layer. In general, the outermost chemical species on the device surfaces provide the functionalities of BioMEMS devices. The outermost chemical species can be biological materials, biocompatible materials or mixtures of both. However, the performance of BioMEMS devices can also be affected by other factors. For example, the layers underneath the outermost layer could affect the robustness, durability and reliability of the outermost layer. In addition, the untreated pristine surface areas should be properly blocked or passivated to prevent non-specific binding (see Case studies 1 and 2).

Chemical compounds that can react with the surfaces of chosen substrate materials, such as organosilanes (for silica-based surfaces), are often used for the first

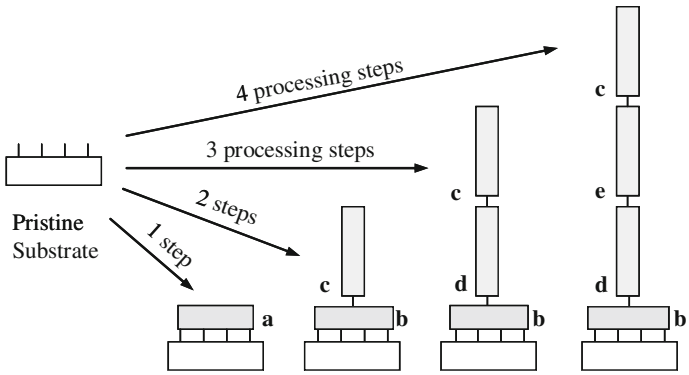


Fig. 13.4 Schematic illustration showing a single-step or multi-step surface modification procedure. The *letters* correspond to interactions or reactions used to create linkage between the substrate surface and a chemical species or between chemical species represented by blocks

reaction to get a firm anchoring on the pristine surface. As shown in Fig. 13.4, there are several different ways to create the linkage in a given modification procedure. In a one-step procedure, the interaction occurs between the pristine substrate surface and the outermost material (Reaction a). The two-step procedure involves the pristine substrate surface reacting with a cross-linker (Reaction b), and then with the outermost material (Reaction c). Multiple-step procedures ($n \geq 2$) include multiple reactions with cross-linkers (Reactions b, d, and/or e), and then with the outermost material (Reaction c). The modification techniques can be categorized as (i) techniques for modifying pristine substrate surfaces (i.e. general MEMS device surfaces created with typical clean room fabrication tools), such as Reactions a and b, and (ii) techniques for modifying pre-treated substrate surfaces (i.e. treated pristine surfaces that require additional steps to complete the entire process), such as Reactions c, d and e. Following the categorization, the techniques commonly used for surface modification in BioMEMS are summarized and discussed in the following sections. Many examples are accompanied by the reaction principles, to provide the materials and processing details.

13.5.2 Modification of Pristine Substrate Surfaces

13.5.2.1 Plasma Treatment

Plasma treatment can be applied to a variety of substrate materials and surfaces that can withstand plasma bombardment. Plasma treatment can be used to change the surface wettability or to generate reactive surface-bound functional groups for chemical reactions. For example, NH_3 (ammonia) plasma can be used to generate surface-bound amino groups, while H_2O or O_2 plasma can be used to generate surface-bound peroxide, hydroxyl, carbonyl, and/or carboxyl groups.

EXAMPLE 1:

As shown in Fig. 13.5, NH_3 plasma was applied by Salber et al. to introduce amino groups on polydimethylsiloxane (PDMS) surfaces [73]. After the treatment, the contact angle with water was slightly decreased (from 107° to 93°). X-ray photoelectron spectroscopy (XPS) on the treated surface showed about 2 atom % of N, indicating that amino group formation was concurrent with the NH_3 plasma treatment on the surface. NH_2 functionalization enables the subsequent immobilization of isocyanate-terminated star-shaped polyethylene glycol (PEG). This PEG coating system can prevent non-specific cell adhesion.

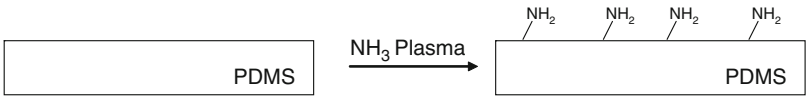


Fig. 13.5 Schematic illustration showing surface modification on a PDMS surface by NH_3 plasma treatment

EXAMPLE 2:

A PMMA-based capillary electrophoresis microchip was fabricated using the Si wafer imprint techniques [74]. Prior to the plasma treatment, the PMMA substrate was annealed at 100°C for 1 h and rinsed with methanol and water, and then dried with nitrogen. Plasma was generated at 13.56 MHz/80 W and at a pressure of 100 mTorr for a 3 min treatment. The ionized oxygen or oxygen radicals reacted with the PMMA chains, creating oxygen-containing groups such as hydroxyl and carboxyl groups on the microchannel surface (Fig. 13.6). These functional groups were used for subsequent surface polymerization of PEG polymer to improve the efficiency of protein and peptide separation [74].

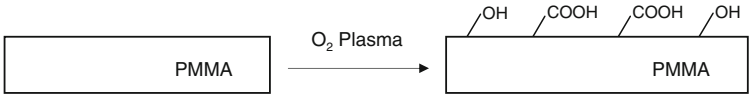


Fig. 13.6 Schematic illustration showing surface modification on a PMMA surface by O_2 plasma treatment

13.5.2.2 Physical Adsorption

Physical adsorption is a method of surface modification via non-covalent interactions (hydrogen-bonding, van der Waals interaction, electrostatic interaction, etc.) between the substrate surface and the applied material. Physical adsorption can be applied to various substrate materials or surfaces, as long as the applied material is compatible with the substrate material or underlying surface. Many proteins, including antibodies and some enzymes, BSA, etc. can be coated onto substrate surfaces via the weak physical interactions between protein molecules and substrate surfaces.

EXAMPLE 3:

A PDMS microfluidic system with trypsin membrane reactor for protein digestion was fabricated by Gao et al. [75]. A porous poly(vinylidene fluoride) (PVDF) membrane (0.45 μm pore size, obtained from Millipore) was used to form an enzyme reactor via non-covalent adsorption of trypsin molecules, a serine protease that hydrolyzes proteins. The high surface-to-volume ratio of the PVDF membrane allows high trypsin concentration in the membrane, resulting in rapid protein digestion. The adsorption was carried out by pumping a trypsin solution (2 mg/ml, in pH 8.0 Tris buffer) through the membrane at a flow rate of 0.2 μL/min for 2 h. The membrane was then flushed with a Tris buffer for 20 min to remove any unbound trypsin. This miniaturized membrane reactor combined with microfluidic channels on a PDMS substrate enables the rapid digestion of trace amounts of protein samples (1 ng or less) in minutes for subsequent mass spectrometry analysis [75].

13.5.2.3 Covalent Linkage

Surface modification of pristine MEMS substrates via covalent linkage has been applied for many BioMEMS applications. Depending on the substrate materials,

the techniques include (i) treatment of silica or silicone surfaces by organosilanes, (ii) treatment of noble metal surfaces (Au, Pt, Ag, etc.) by thiol or dialklydisulfide compounds, and (iii) treatment of silicon or silicon nitride surfaces with alkenes.

Silanization of Silica or Silicone Surfaces

Organosilanes are commonly used in MEMS fabrication as adhesion promoters or antistiction layers (see also Section 13.4.2). They can modify substrate surfaces such as silica (e.g. glass, quartz) or silicone (e.g. PDMS) via the covalent Si-O-Si linkage between organosilanes and the substrate surface. Although some silanol groups (-SiOH) may originally exist on the PDMS surfaces, an O_2 plasma treatment on the PDMS can produce more silanol groups for a more effective silanization reaction. Examples of some commonly used organosilanes are shown in Fig. 13.7, which include alkyl-substituted alkoxysilanes (1–6, 9) and alkyl-substituted chlorosilanes (7, 8, 10, 11). Some chemicals in Fig. 13.7 (such as FOTS, No. 10) have similar characteristics as those mentioned in Tables 13.1 and 13.2 (such as FDTS). FOTS is commercially available for producing hydrophobic and non-stick surfaces using a molecular vapor deposition tool (such as MVD-100, by Applied Microstructures). The same tool can also be used to deposit self-assembled coatings based on APTMS (No. 3 in Fig. 13.7), MAOPTS (No. 8), or MPTMS (No. 5) to enhance adhesion, change hydrophobicity, and/or to create functional groups on the surface for subsequent reactions. The organosilanes can be monofunctional, bifunctional, or trifunctional, depending on the number of the silanol groups (Si-OH) that can be converted upon hydrolysis (Fig. 13.8).

In general, coatings are more robust when organosilanes contain multifunctional silyl groups. However, silanization involving trifunctional silyl groups usually results in rougher surfaces because of the complex cross-linking reactions (Fig. 13.9a). Silanization using organosilanes with monofunctional silyl groups results in smoother surfaces (Fig. 13.9b), but they are more vulnerable to hydrolytic desorption in a high-pH alkaline buffer.

Thiolation of Noble Metal Surfaces

As shown in Fig. 13.10, thiols or dialkyldisulfides can be used to modify the surfaces of noble metals such as Au, Ag, or Pt, to form self-assembled monolayers (SAMs) [76, 77]. These modifications can yield excellent systems to study the interactions of proteins with organic surfaces. Some examples of thiol compounds [76] and disulfide compounds [77] are shown in Figs. 13.11 and 13.12, respectively. Typically, to prepare SAMs on the surfaces of noble metals, a thiol or disulfide solution in an organic solvent (e.g. ethanol or methanol) with a very dilute concentration, i.e. 0.2–20 mM, is prepared and then used to treat the surfaces of noble metals. SAMs comprising mixtures of two or more components can also be prepared by chemisorption from solutions containing mixtures of these components [76]. Consequently, the surface properties (e.g. hydrophobicity) can be tailored according to the ratio of the different alkanethiolates on the modified surfaces.

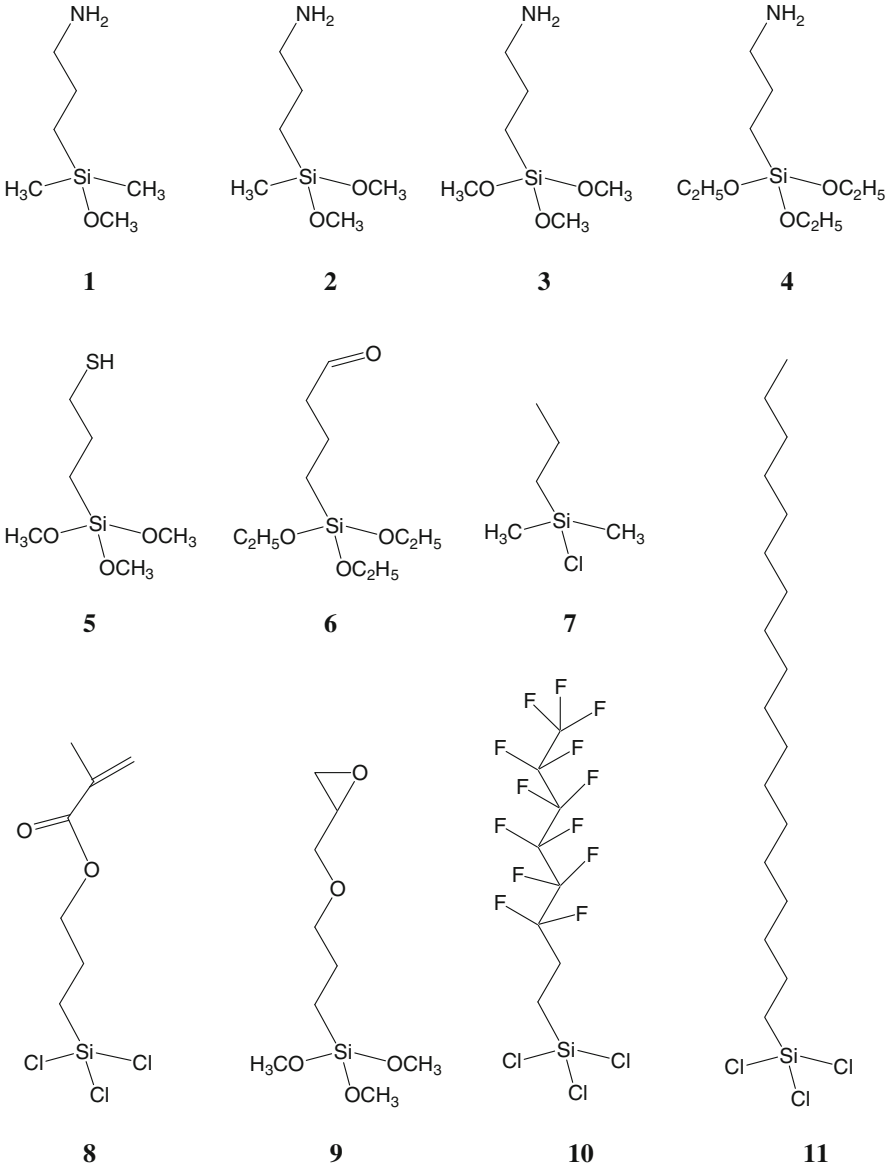


Fig. 13.7 Examples of organosilanes: **(1)** 3-aminopropyldimethylmethoxysilane, **(2)** 3-aminopropylmethyldimethoxysilane, **(3)** 3-aminopropyltrimethoxysilane (APTMS), **(4)** 3-aminopropyltriethoxysilane (APTES), **(5)** 3-mercaptotrimethoxysilane (MPTMS), **(6)** triethoxysilylbutyraldehyde, **(7)** propyldimethylchlorosilane, **(8)** 3-methacryloxypropyltrichlorosilane (MAOPTS), **(9)** 3-glycidoxypropyltrimethoxysilane (GPTMS), **(10)** *1H,1H,2H,2H*-perfluorooctyltrichlorosilane (FOTS), and **(11)** octadecyltrichlorosilane

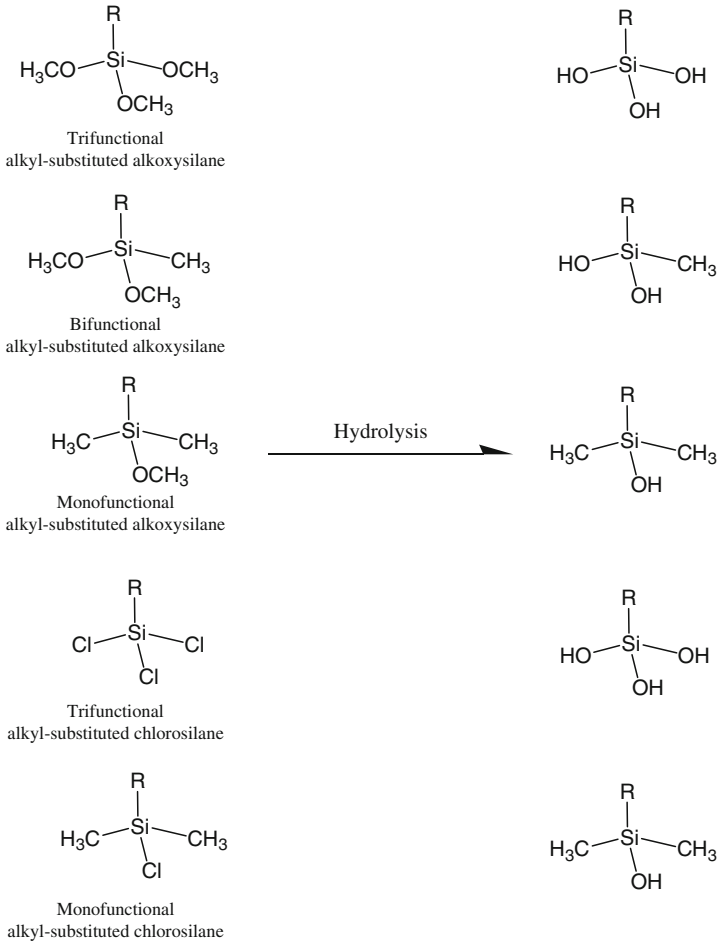


Fig. 13.8 Hydrolysis of organosilanes

Hydrosilylation of Silicon or Silicon Nitride Surfaces

Alkenes can be used to modify substrate materials based on single crystalline silicon, porous silicon, or silicon nitride via Si-C bonding (Fig. 13.13) [78]. Prior to hydrosilylation, the native SiO_2 layer on silicon must be removed (e.g. by HF). Dilute (1–2%) HF solution treatment of a single crystalline Si (100) wafer yields dihydride (-SiH_2) on the surface, and a 40% NH_4F solution treatment on Si (111) results in monohydride (–SiH) groups. Similar etching treatments can also be applied to silicon nitride substrates. For porous Si (created by electrochemical HF etching), etching yields a –SiH_x terminated silicon surface with x ranging from 1 to 3. The freshly prepared silicon hydride terminated surface is chemically homogeneous (>99% H terminated) and is a useful precursor because the Si-H bonds can be further functionalized.

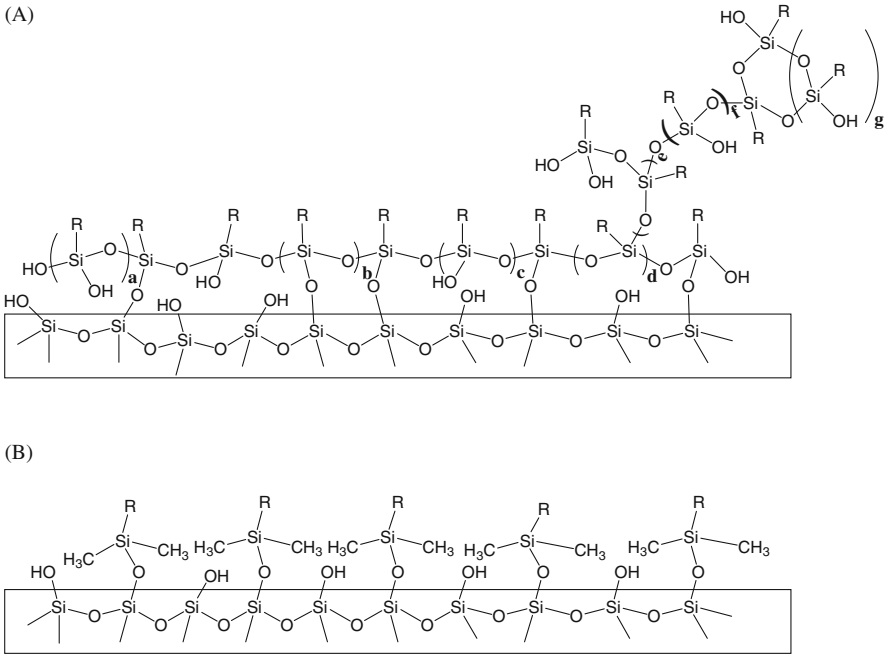
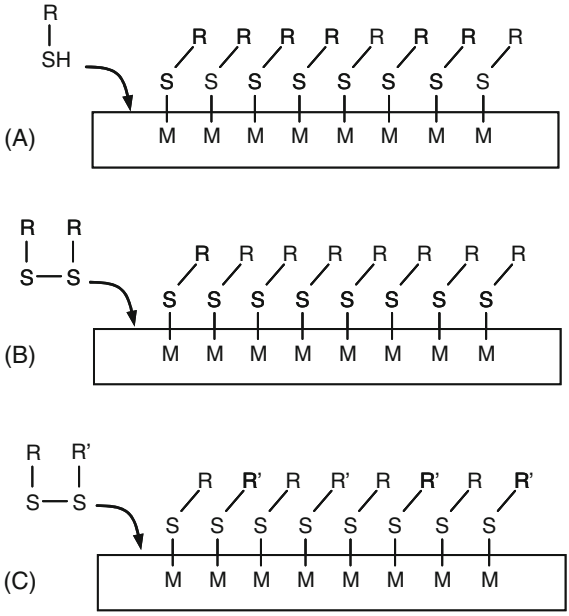


Fig. 13.9 A silica surface subjected to silanization treatment by (**a**) a trifunctional organosilane and (**b**) a monofunctional organosilane

Hydrosilylation between C=C and Si-H can be started using radical initiators such as diacyl peroxide at ~100°C. However, thermally induced hydrosilylation of porous silicon at 110–180°C, without initiators, has also been reported. Alternatively, UV irradiation (185 and 253.7 nm wavelength UV light; 2 h) can also be used to start hydrosilylation on the Si-H surface at room temperature. Some examples of alkenes [78] are shown in Fig. 13.14.

13.5.3 Modification of Pre-treated Substrate Surfaces

After the pristine surface has been modified using one of the methods described in Section 13.5.2, the surface is either ready for use or requires further modification. To perform further modification, the methods described in the previous section can still be used. The modified surfaces may have exposed functional groups such as –OH, -NH2, -COOH, -SH, or −CHO that are ready for further modification. Therefore, it is advantageous and convenient to exploit those chemical reactions for further surface modification in a multi-step procedure. The commonly employed chemical reactions involving −OH, $-NH_2$, −COOH, −SH, and −CHO functional groups on MEMS device surfaces for BioMEMS applications are summarized and elaborated on in the sections that follow.



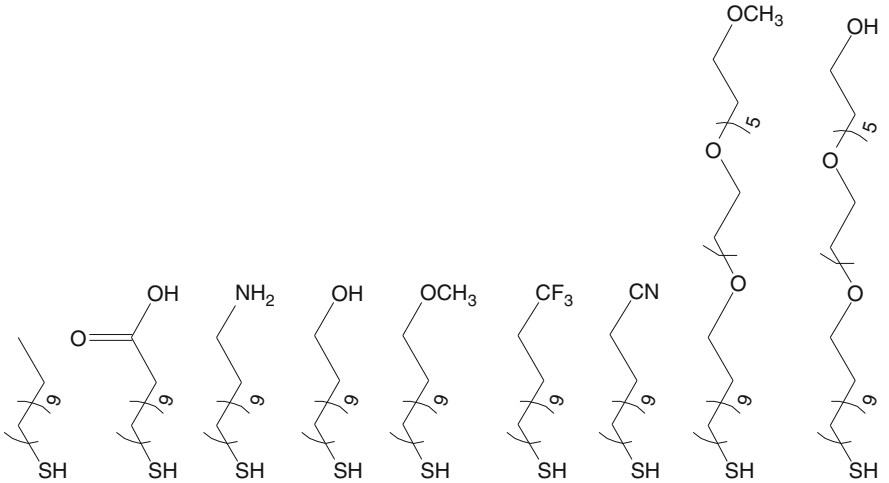
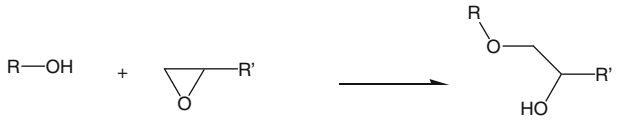


Fig. 13.10 A noble metal surface subjected to a thiolation treatment by (**a**) a thiol, (**b**) a homodialkyldisulfide, and (**c**) a heterodialkyldisulfide

Fig. 13.11 Examples of thiols

13.5.3.1 Chemistry of Hydroxyl Groups (R-OH: Alcohols)

The chemical reaction shown in (13.3) allows an alcohol to form a covalent linkage with another chemical compound containing an epoxy group.



(13.3)

EXAMPLE 4:

A three-step surface modification process was used by Moorcroft et al. to modify the PDMS substrate for in situ oligonucleotide synthesis on the surface of PDMS microchannels [79]. First, PDMS channels were prepared by soft lithography using SU-8 as a mold [80]. The PDMS was cured at room temperature overnight, and then at 70°C for 1 h. The PDMS channels were initially oxidized by an ozone cleaner (UVO Cleaner®, by Jelight Co.). Secondly, vapor-phase silanization was

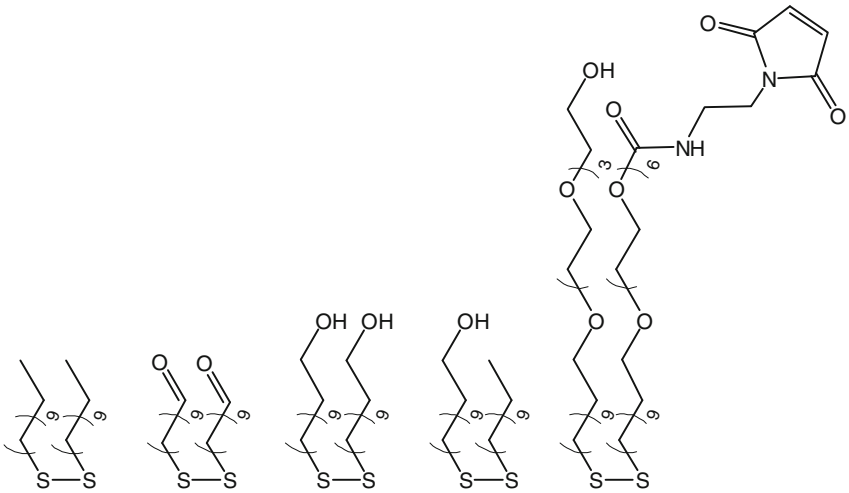


Fig. 13.12 Examples of dialkyldisulfides

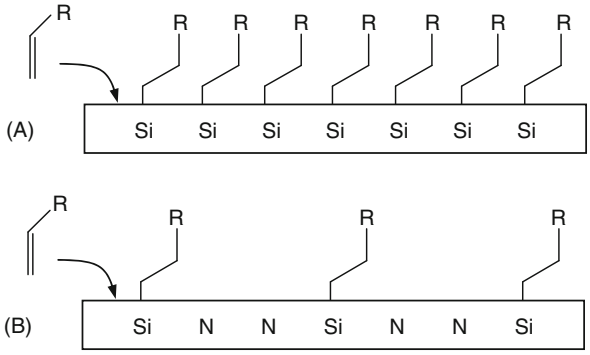


Fig. 13.13 Hydrosilylation of (**a**) a silicon surface and (**b**) a silicon nitride surface

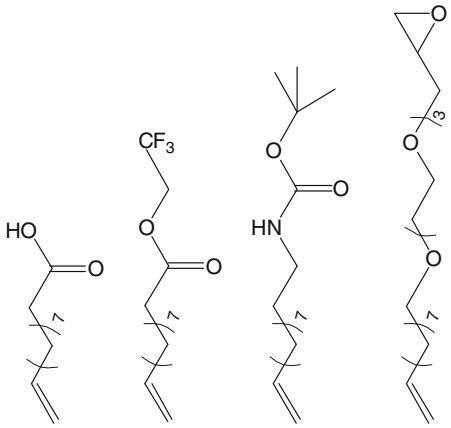


Fig. 13.14 Examples of alkenes

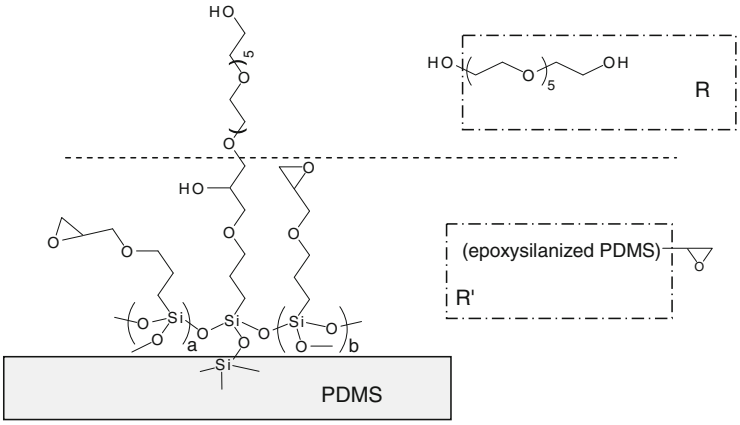


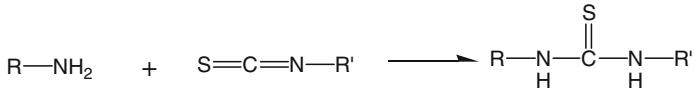
Fig. 13.15 Reaction of the hydroxyl group of HO-$(C_2H_4O)_5$-C_2H_4-OH with the epoxy group of an epoxysilanized PDMS substrate, as described in Example 4 and reaction (13.3)

carried out in a vacuum oven with 3-glycidoxypropyltrimethoxysilane (GPTMS, No. 9 in Fig. 13.7) to functionalize the substrate surface with epoxy groups. In the third step of the surface modification process (Fig. 13.15), the reaction (13.3) was involved to create the covalent linkage between the surface-bound epoxy group on the silanized PDMS substrate and the hydroxyl group of PEG spacer (HO-$(CH_2CH_2O)_5CH_2CH_2OH$). The oligonucleotides can be in situ synthesized on the PEG surface using the conventional phosphoramidite chemistry with a DNA synthesizer [79].

13.5.3.2 Chemistry of Amino Groups (R–NH_2: Amines)

In this section, four different types of amine reactions are described, and each reaction is accompanied by an example. The chemical reaction shown in (13.4) allows

an amine to form a covalent linkage with another chemical species containing an isothiocyanate group.

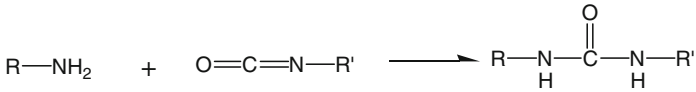


(13.4)

EXAMPLE 5:

A three-step surface modification process was used by Charles et al. to fabricate DNA chips for DNA hybridization efficiency studies [81]. First, the glass substrates were acid-cleaned, and then the substrate was treated with a 2% acidic-methanol solution of 3-aminopropyltriethoxysilane (APTES, No. 4 in Fig. 13.7). In the second step of the surface modification process (Fig. 13.16), the reaction (13.4) was used to generate the covalent linkage between the surface-bound amino group (on APTES) and the isothiocyanate group of the bifunctional cross-linker, 1,4-phenylene diisothiocyanate (PDC). In the third step, the modified surfaces (isothiocyanate groups) reacted with amine-modified single strand DNA molecules (also shown in Fig. 13.16) [81].

A more popular chemical reaction (13.5) for an amine is to form a covalent linkage with an isocyanate group. Aromatic isocyanates are more reactive than the aliphatic isocyanates, and thus are more commonly used.



(13.5)

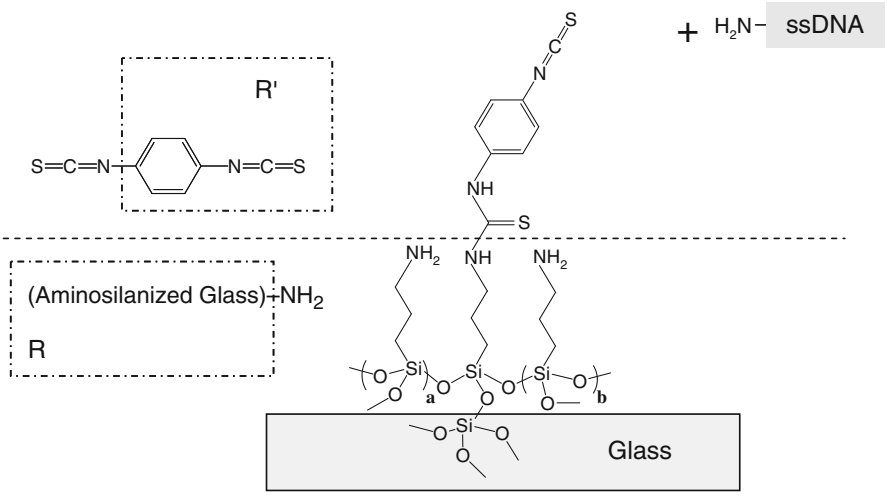
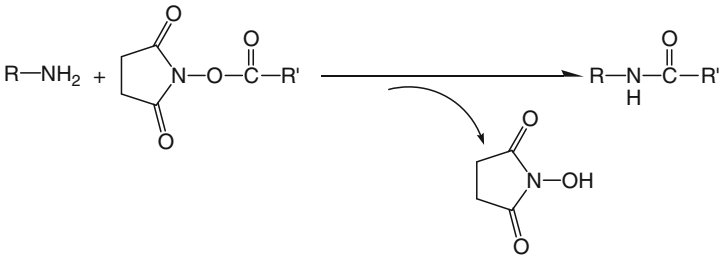


Fig. 13.16 Reaction of the isothiocyanate group of 1,4-phenylene diisothiocyanate with the amino group of an aminosilanized glass substrate, as described in Example 5 and reaction (13.4)

EXAMPLE 6:

A three-step surface modification process was used by Jin et al. to fabricate DNA chips for DNA hybridization efficiency studies [82]. Similarly to Example 5, the silica surface was first modified with 3-aminopropyltriethoxysilane (APTES, in Fig. 13.7). This was performed by soaking the silica in 1 wt% (40 mM) APTES solution in anhydrous toluene at room temperature for 30 min. In the second step of the surface modification process (Fig. 13.17), a maleimide-presenting surface was generated using the reaction in (13.5). That is, the isocyanate group of the heterobifunctional cross-linker, *p*-maleimidophenyl isocyanate (PMPI), formed a urea linkage with the APTES amines. The reaction was carried out in a 70 mM solution of PMPI in anhydrous acetonitrile at room temperature for 30 min. The outermost functional group became the maleimide group after this PMPI-APTES reaction. The final step was the immobilization of the thiol terminated DNA strands with the surface maleimides.

The next example is the chemical reaction shown in (13.6), in which an amine reacts with an *N*-hydroxysuccinimide ester (NHS-ester) to form an amide linkage.



(13.6)

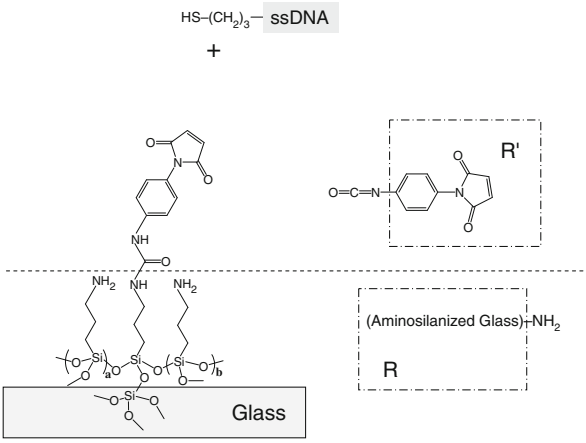


Fig. 13.17 Reaction of the amino group on an aminosilanized glass substrate with the isocyanate group of *p*-maleimidophenyl isocyanate, as described in Example 6 and reaction (13.5).

EXAMPLE 7:

Microfluidic channels made with PDMS (from SU-8 molds) and glass slides were used to study the amyloid formation and fibril growth [83]. Prior to bonding, the glass slides were cleaned in piranha solution of 70% H_2SO_4/30% H_2O_2 (v/v) at 60°C for 15 min. A three-step surface modification process was used to covalently attach the insulin molecules to the glass and PDMS walls of the microchannels. First, the microchannels were injected with a 3% solution of APTES in ethanol/water (95/5 by volume) for 1 h; then they were washed with ethanol and cured at 100°C. To activate the microchannel with *N*-hydroxysuccinimide (NHS) ester, a solution of 20 mM *N,N'*-disuccinimidyl carbonate (DSC) in a sodium bicarbonate buffer (50 mM, pH 8.5) was injected for 3 h at room temperature [83].

In the third step of the surface modification process (Fig. 13.18), the reaction (13.6) was involved to create covalent attachments between the amino group of insulin molecules and the microchannel walls containing surface-bound NHS ester groups. The insulin monomer solution was prepared by dissolving fresh insulin (1 mg/mL) in 40 mM HCl solution to dissociate hexamers into monomers, and the solution was flushed through the microchannels for 10 min to covalently bond the insulin monomers.

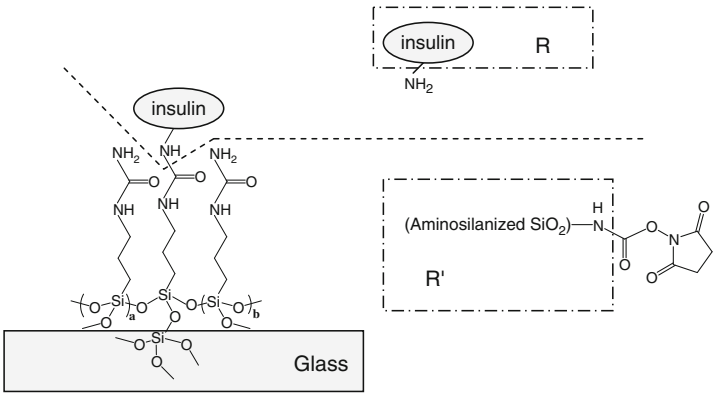
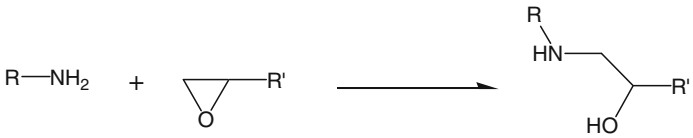


Fig. 13.18 Reaction of the amino group of an insulin molecule with the *N*-hydroxysuccinimide ester group on an aminosilanized glass-based substrate, as described in Example 7 and reaction (13.6)

The chemical reaction (13.7) allows an amine to form a covalent linkage with another chemical species containing an epoxy group. This reaction is similar to reaction (13.3), except that an amino group replaces the hydroxyl group in the reaction. Both groups are commonly used for the ring opening reaction with the epoxy group



(13.7)

EXAMPLE 8:

It is increasingly important to build BioMEMS devices with the capability of detecting antigens or viruses. A two-step surface modification process was used by Li et al. to fabricate antibody chips for the detection of HIV-1 antigen [84]. The first step was to bond GPTMS (No. 9 in Fig. 13.7 and Example 4) to the glass slides. After cleaning in ethanol, the slides were immersed in a 2.5 vol% GPTMS ethanol solution containing 10 mM acetic acid for 1 h at room temperature. In the second step of the surface modification process (Fig. 13.19), the reaction (13.7) occurred between the epoxy group on a silanized glass substrate and the amino group of a goat anti-HIV-1 p24 polyclonal antibody molecule [84].

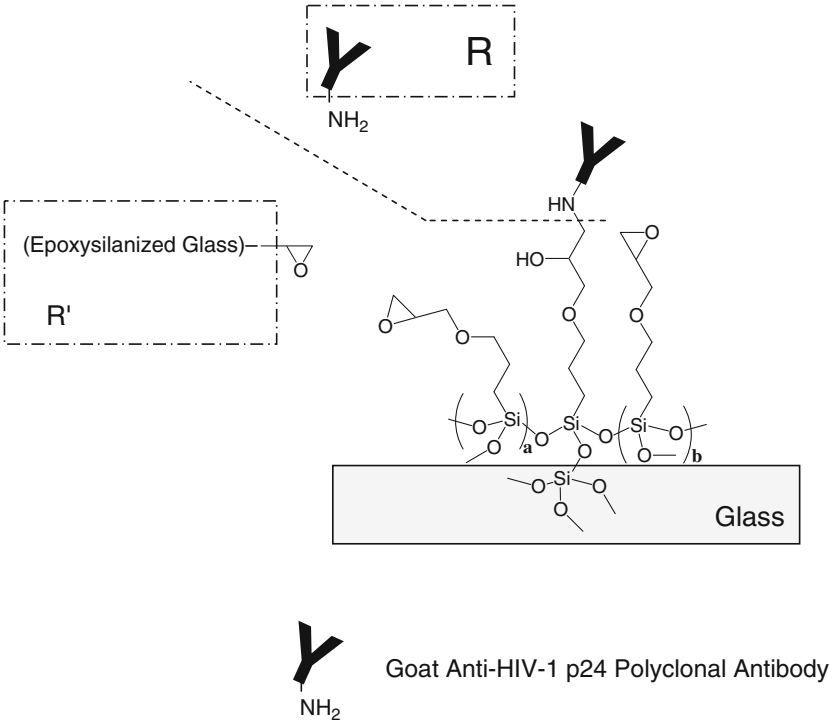
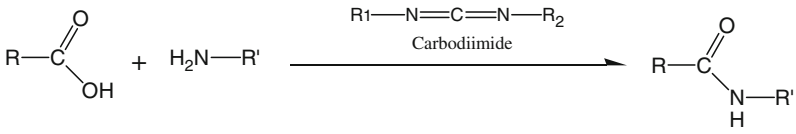


Fig. 13.19 Reaction between the amino group of a goat anti-HIV-1 p24 polyclonal antibody molecule and the epoxy group on an epoxysilanized glass-based substrate, as described in Example 8 and reaction (13.7)

13.5.3.3 Chemistry of Carboxyl Groups (R–COOH: Carboxylic Acids)

The carbodiimide-facilitated condensation shown in (13.8) allows a carboxylic acid to form a covalent amide bond with an amino group. Examples of carbodiimides are dicyclohexyl carbodiimide (DCC; $H_{11}C_6{-}N{=}C{=}N{-}C_6H_{11}$) and diisopropyl carbodiimide (DIC; $H_7C_3{-}N{=}C{=}N{-}C_3H_7$).



(13.8)

EXAMPLE 9:

As illustrated in Fig. 13.10, thiols can react with noble metals such as gold. A two-step surface modification process was used by Davis et al. to construct gold electrodes covalently attached with cytochrome *c* molecules [85]. First, as shown in Fig. 13.20, the gold surface was coated with self-assembled monolayers (SAMs) having a mixture of $HS-(CH_2)_6-COOH$ and $HS-(CH_2)_4-OH$. The ratio of COOH/OH was adjusted to control the surface reactivity, since the hydroxyl groups were relatively non-reactive with the amines in the next reaction. The SAMs were formed by submerging the gold surface in a 2 mM thiol solution for 12–16 h at room temperature. In the second step of the surface modification process (Fig. 13.20), the reaction (13.8) was involved to generate the covalent amide linkage between the carboxyl group of $Au-S-(CH_2)_6-COOH$ and the amino group of cytochrome *c* molecules. The biochips containing immobilized cytochrome *c* molecules were used for electron-transfer studies.

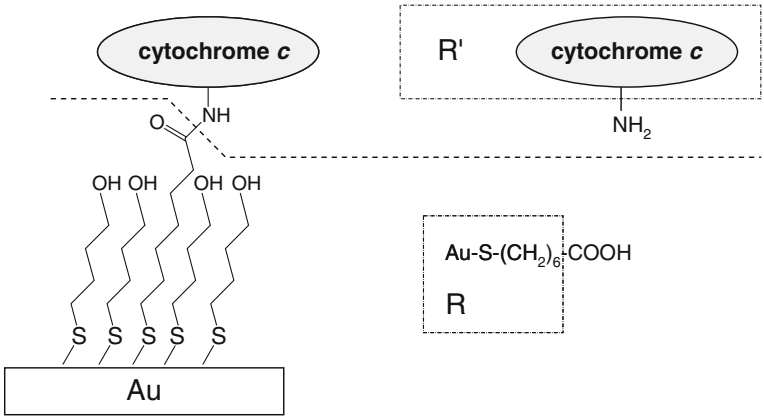
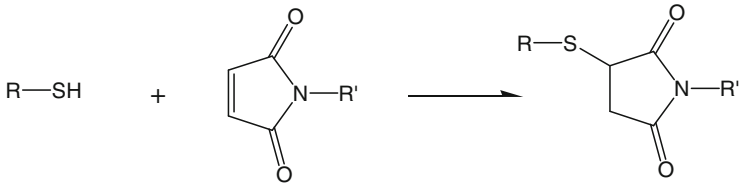


Fig. 13.20 Reaction of the amino group of a cytochrome *c* molecule with the carboxyl group on an Au-based substrate, as described in Example 9 and reaction (13.8)

13.5.3.4 Chemistry of Mercapto Groups (R–SH; Thiols)

The addition reaction shown in (13.9) allows a thiol to react with a maleimide to form a covalent carbon-sulfur (thioether) linkage. Maleimides are excellent reagents for thiol-selective modification, and the reaction is useful for the fabrication and development of biosensing surfaces and microarrays. Maleimides linked to polyethylene glycol (PEG) chains are often used as flexible crosslinkers to attach proteins or oligonucleotides (DNA) to surfaces.



(13.9)

EXAMPLE 10:

DNA immobilization on maleimide-ethylene glycol self-assembled monolayers was performed by Lee et al. [86]. A two-step surface modification process was used to construct DNA chips for the studies on DNA probe surface orientation and target hybridization efficiency. First, 0.1 mM of maleimide-ethylene glycol-terminated disulfide [$HO(C_2H_4O)_4(CH_2)_{11}$-SS-$(CH_2)_{11}(OC_2H_4)_6$-OCH_2-CONH-$(CH_2)_2$-$C_4H_2NO_2$] (MEG) was prepared in an ethanolic solution. The gold-coated surface was then immersed in the MEG solution at room temperature for 1 h. As shown in Fig. 13.10c, heterodialkyldisulfide reacts with the gold surface and can create two different functional groups (one hydroxyl group and one maleimide group, as shown in this example). In the second step of the surface modification process (Fig. 13.21), the reaction (13.9) took place, generating the covalent linkage between the surface-bound maleimide group of Au-S-$(CH_2)_{11}$-$(OC_2H_4)_6$-OCH_2-CONH-C_2H_4-maleimide and the thiol group of thiolated single-strand DNA (HS-ssDNA) molecules. The HS-ssDNA solution was prepared in pH 7 buffer at concentrations from 5 to 500 μM to study the effect on immobilized DNA density using XPS and TOF-SIMS surface analysis tools.

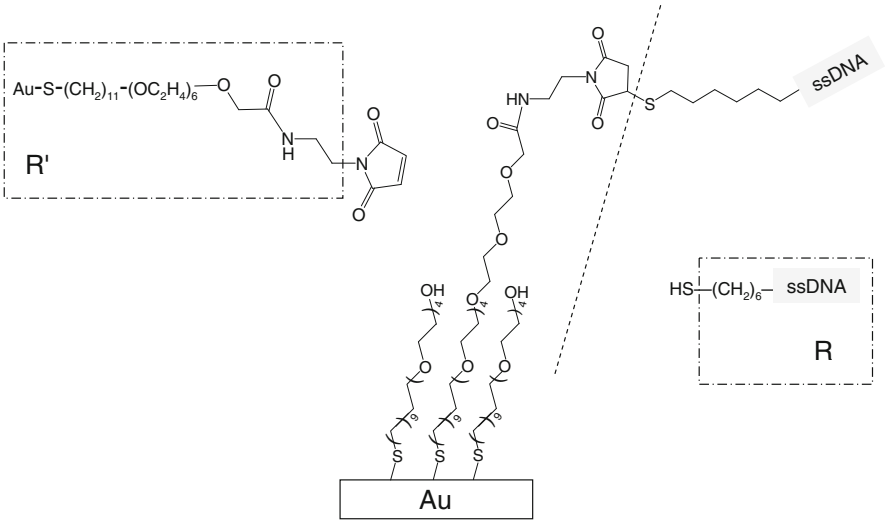
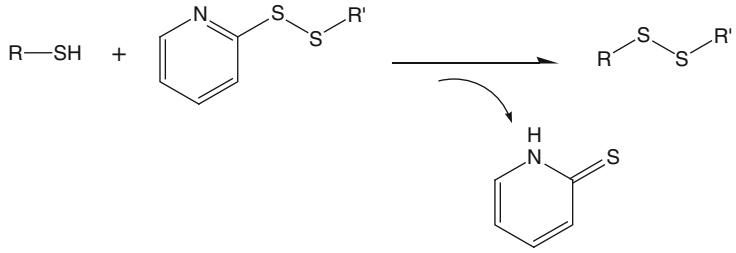


Fig. 13.21 Reaction of the thiol group of a thiolated ssDNA molecule with the maleimide group on an Au-based substrate, as described in Example 10 and reaction (13.9)

The exchange reaction shown in (13.10) allows a thiol to react with a pyridyl disulfide to form a covalent linkage. The exchange reaction can be performed at physiologic pH, but the optimum reaction rate is at pH 4–5.



(13.10)

EXAMPLE 11:

A two-step surface modification process was used by Neff et al. to control surface peptide density and protein adsorption on polystyrene (PS) substrates for cell adhesion studies [87]. First, a 2-pyridyl disulfide derivative of a PEO/PPO/PEO triblock copolymer (Pluronic^{TM} F108 [HO-$(C_2H_4O)_{129}$-$(C_3H_6O)_{56}$-$(C_2H_4O)_{129}$-H]) was prepared. The modified F108 was then adsorbed onto the PS substrate surface by soaking PS in a diluted aqueous solution (0.4 w/v%) for 24 h. The adsorbed F108 2-pyridyl disulfide derivative formed stable and strong hydrophobic interactions between PPO segments and PS. In the next step of the surface modification process (Fig. 13.22), the reaction (13.10) was used to generate the covalent linkage via the exchange reaction between the surface-bound pyridyl disulfide group of the modified F-108 and the thiol group of the peptides [87]. The peptide surface density

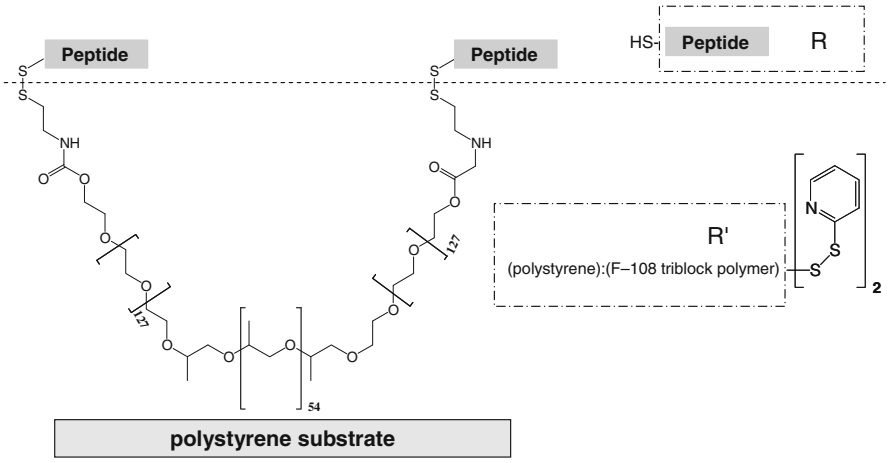
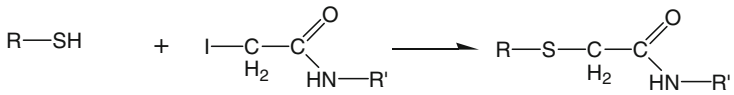


Fig. 13.22 Reaction of the thiol group of an RGD analogue peptide molecule with the pyridyl disulfide group on a polystyrene-based substrate, as described in Example 11 and reaction (13.10)

on the PS surface could be varied by mixing the unmodified hydroxyl-terminated F108 with the disulfide-derived F108 during the adsorption process.

The chemical reaction shown in (13.11) allows a thiol to form a covalent linkage with an iodoacetyl group in alkaline conditions.



(13.11)

EXAMPLE 12:

The example shown in Fig. 13.23 illustrates a technique for the construction of high-density DNA chips for nucleic acid hybridization and detection by MALDI-TOF mass spectrometry [88]. A three-step surface modification process was carried out for SiO_2 surface modification on silicon wafers [88]. First, the SiO_2 surface was immersed in a 25 vol% anhydrous toluene solution of 3-aminopropyltriethoxysilane (APTES, No. 4 in Fig. 13.7) for 3 h. This step was similar to the one described in Examples 5 and 6. Secondly, after washing with toluene and dimethyl sulfoxide (DMSO), the wafer was soaked in a 10 mM DMSO solution of *N*-succinimidyl(4-iodoacetyl)aminobenzoate [SIAB, $(C_4H_4O_2N)$-O-CO-C_6H_4-NH-CO-CH_2I]. The reaction is the same as reaction (13.6) shown in Example 7. In the third step

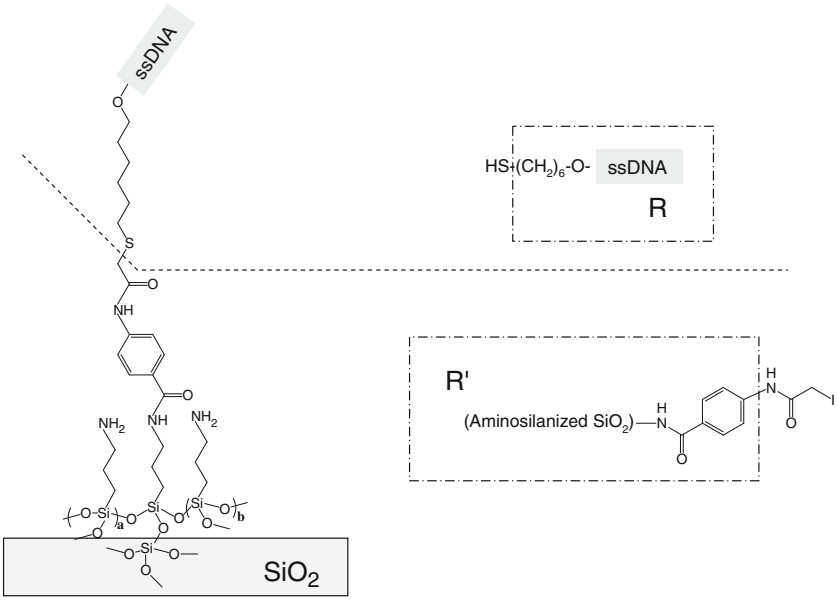
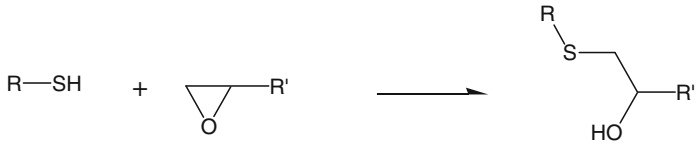


Fig. 13.23 Reaction of the iodoacetyl group on a SiO_2/Si-based surface with the thiol group of a thiolated ssDNA molecule, as described in Example 12 and reaction (13.11)

(Fig. 13.23), the reaction (13.11) took place to immobilize DNA probes via the coupling of the surface-bound iodoacetyl group and the thiol group of thiolated single strand DNA (ssDNA). This coupling was carried out in 100 mM phosphate buffer of pH 8 at room temperature for 5 h.

The chemical reaction in (13.12) shows that a thiol group forms a covalent linkage with an epoxy group.



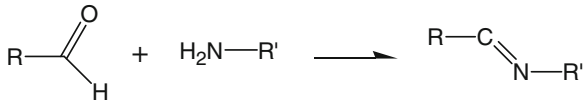
(13.12)

EXAMPLE 13:

DNA chips were fabricated by Böcking et al. for hybridization efficiency studies [89]. First, Si (111) wafers were cleaned in concentrated H_2SO_4/30% H_2O_2 (3:1, v/v) for 30 min at 90°C. To prepare for a hydrogen-terminated Si surface, the wafers were then etched in deoxygenated 40% solution of NH_4F for 20 min. The Si surface was then immersed in the solution of epoxy-terminated alkene in 1,3,5-triethylbenzene under an inert atmosphere at 200°C for 2–6 h (the alkene-Si reaction is illustrated in Fig. 13.13). In the next step of the surface modification process (Fig. 13.24), the reaction (13.12) was carried out by placing drops of the DNA solution (10 μM in 0.1 M $NaHCO_3$ buffer at pH 8.3) on the epoxy-terminated surface for 12 h at 40°C. This reaction generated the covalent linkage between the surface-bound epoxy group on the silicon substrates and the thiol group of thiolated single strand DNA (HS-ssDNA).

13.5.3.5 Chemistry of Formyl Groups (R–CHO: Aldehydes)

The chemical reaction in (13.13) shows that an aldehyde forms a covalent linkage (-C=N-) with an amino group. To make the covalent linkage more stable, a reducing agent such as $NaBH_3CN$ can be used to turn the Schiff base formed via reaction (13.13) into a secondary amine (13.14).



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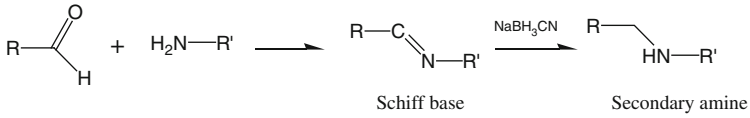

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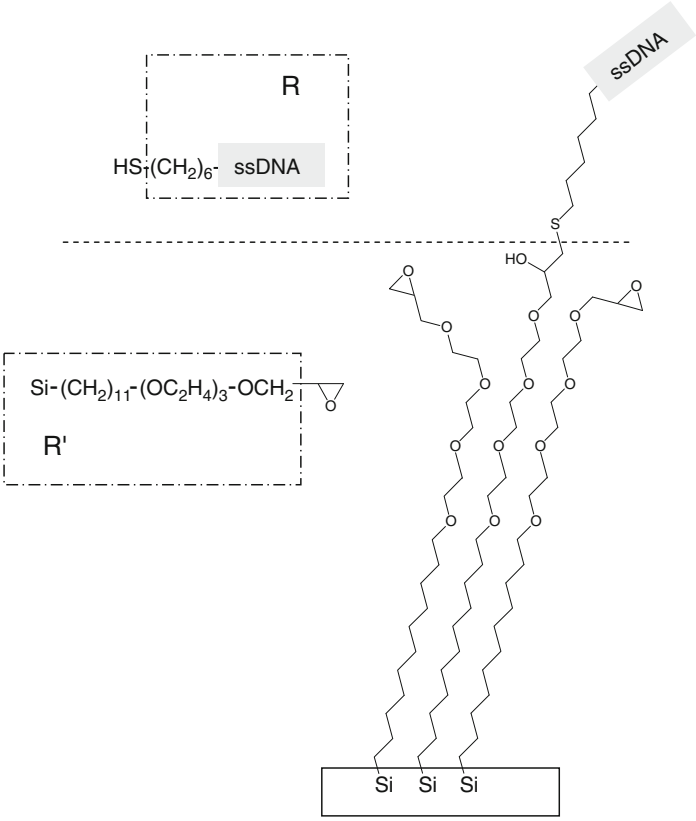


Fig. 13.24 Reaction of the thiol group of a thiolated ssDNA molecule with the epoxy group on a Si-based substrate, as described in Example 13 and reaction (13.12)

EXAMPLE 14:

A four-step surface modification process was used by Eteshola et al. to construct a PDMS microfluidic device for enzyme-linked immunosorbent assay (ELISA) with improved sensitivity [90]. ELISA (also called enzyme-linked immunoassay, or EIA) is an analytical technique used in immunology for the detection of an antibody or an antigen. First, PDMS microchannels made from SU-8 molds were coated with bovine serum albumin (BSA) solution (1 mg/ml in sodium phosphate buffer) for 3.5 h. In the second step of the modification process (Fig. 13.25), the reaction (13.13) occurred between glutaraldehyde and the amino group of BSA on the surface of the PDMS microchannels, i.e., the BSA-coated microchannels were allowed to react with 0.1% glutaraldehyde aqueous solution for 1 h. In the third step of the modification process, the same reaction (13.13) occurred again between the "glutaraldehyde-activated BSA" and the amino group of protein A molecules (Fig. 13.25). The reaction (13.13) was used twice for this surface modification. Protein A solution (20 μg/ml in sodium phosphate buffer) was prepared

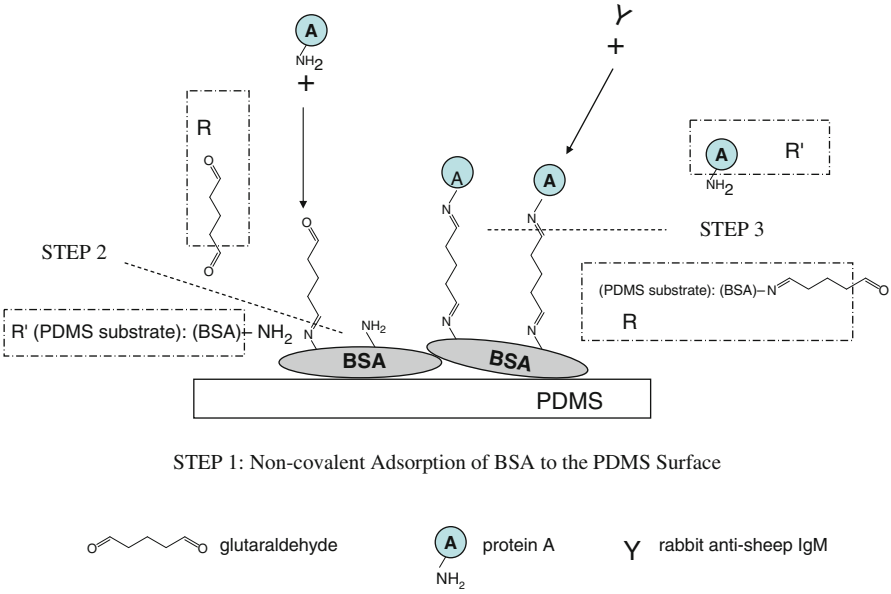


Fig. 13.25 Reaction of the amino groups of proteins (BSA and protein A) with the formyl groups of glutaraldehyde, as described in Example 14 and reaction (13.13)

for this reaction and glutaraldehyde acted as a crosslinker and spacer for protein A. The protein A molecules immobilized on the wall of the microchannel could be functionalized with antibodies (e.g. rabbit anti-sheep IgM) for ELISA experiments.

EXAMPLE 15:

Microarray technology has been broadly used for a variety of purposes, from oligonucleotides and proteins to living cells to study gene activity, protein expression, and interactions between cell surface receptors and ligands [91]. In this example, cell chips were fabricated using aldehyde-terminated self-assembled monolayers (SAMs) on gold-coated glass substrates to study the interactions between bFGF proteins and bFGF receptors on the membranes of BHK-21 cells [92]. First, thin Au/Cr layers (25 nm/1 nm) were deposited on glass, and were still transparent enough for optical microscopy. As shown in step 1 (Fig. 13.26), self-assembled monolayers were formed on the gold surface by immersing it in 1–10 mM di(10-decanal) disulfide [$(CHO\text{-}(CH_2)_9\text{-}S\text{-})_2$] in ethanol for 24 h. In step 2, the reaction (13.14) was used to generate the covalent linkage between the surface-bound aldehyde group and the amino group of bFGF proteins. For protein immobilization, bFGF solution (1 mg/mL in 10 mM HEPES buffer, pH 8.5) was placed on the aldehyde-terminated surface and incubated overnight at room temperature. In

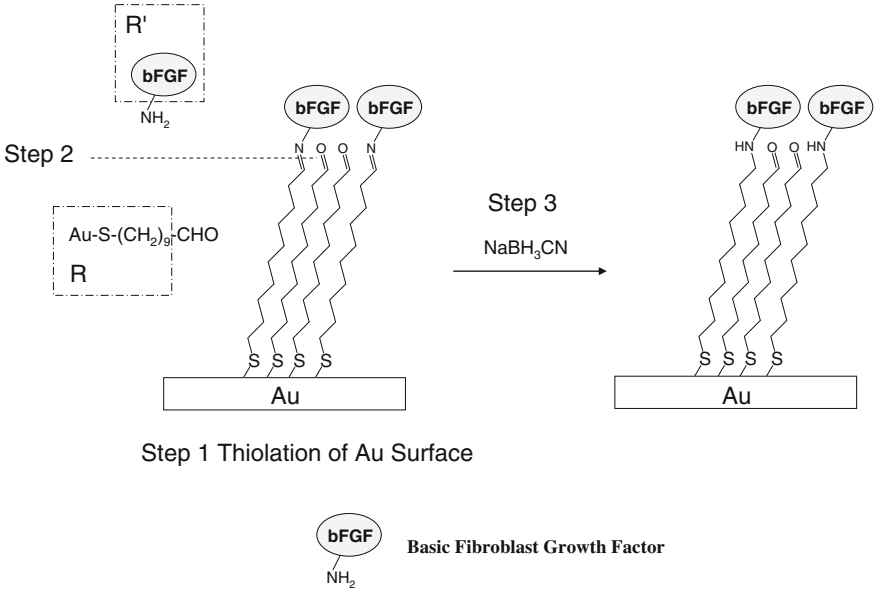


Fig. 13.26 Reaction of the amino group of the bFGF molecule with the formyl group on an Au-based substrate, followed by the treatment with a reducing agent, $NaBH_3CN$, as described in Example 15 and reaction (13.14)

step 3, a reducing agent, $NaBH_3CN$, was used to reduce the formed imine (a Schiff base) into a more stable secondary amine.

13.5.4 Case Studies

Sections 13.5.2 and 13.5.3 describe most of the commonly used surface modification techniques in BioMEMS. However, in view of the broad scope and diversity of chemical reactions, it must be emphasized that the contents of Sections 13.5.2 and 13.5.3 should only be considered to be a general introduction, covering the basic concepts necessary to understand surface modification techniques by bottom-up molecular engineering in BioMEMS. In other words, wherever the laws of chemistry allow, alternative plausible reaction schemes can also be developed. Moreover, when a surface modification scheme is selected, other factors such as reaction kinetics, molecular orientation, reactivity of functional groups etc, should be taken into consideration as well.

In this section, several case studies are used as examples to address broader issues in the modification processes. Issues related to surface blocking/passivation of biochips will be discussed in case studies 1 and 2. A series of studies aimed at improving AFM tip coatings for protein interaction studies will be summarized in case study 3. The use of a specialized cross-linking scheme for peptide immobilization and surface patterning by microcontact printing will be described in case studies 4 and 5, respectively.

13.5.4.1 Case Study 1: Promotion of Immobilized Bioactive Proteins' Biological Activity

Some key requirements for biochip fabrication are to ensure that the sensing molecules survive the processing steps, remain in the patterned location, and maintain maximum sensitivity compared to background noise. After immobilizing the bioactive molecules (e.g. protein A in Fig. 13.27a) on specific areas, bovine serum albumin (BSA) is commonly used to cover the non-sensing substrate surfaces to reduce undesired adsorption and background noise. For example, the desired protein A molecules are immobilized to the substrate surface by non-covalent adsorption; then BSA is applied, also by non-specific adsorption, to block the surface not occupied by the bioactive protein molecules (Fig. 13.27a). Although this method is easy to apply, the BSA can also block the active protein A sites, and protein A can be severely denatured when they are adsorbed directly to a hydrophobic surface. These drawbacks will significantly reduce the reactivity of the protein A with the antibody (the Y-shaped molecule).

To increase the reactivity between protein A and the antibody (Y), a better blocking strategy was demonstrated by Eteshola et al. [90], as shown in Fig. 13.27b. In this study, the BSA layer was first deposited by adsorption on the substrate surface.

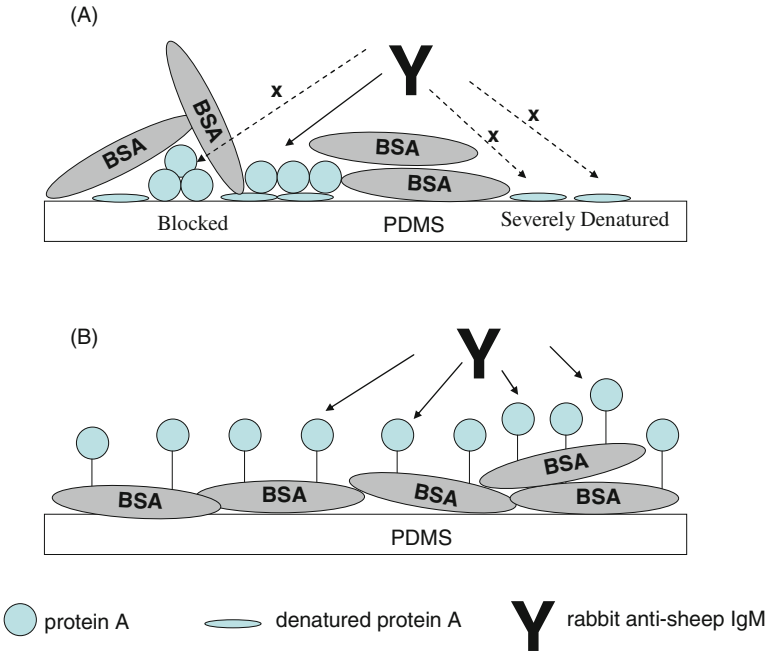


Fig. 13.27 Immobilization of protein A molecules by (**a**) non-covalent adsorption on a PDMS substrate followed by non-covalent BSA blocking, and (**b**) covalent immobilization via glutaraldehyde on the PDMS substrate coated with non-covalently adsorbed BSA

Then a cross-linker was used to immobilize the bioactive proteins on a pre-adsorbed BSA layer, with the chemistry as shown in Example 14. The employed strategy (Fig. 13.27b) results in less blocking of protein A on the surface, and higher reactivity with the antibody (Y). This new method significantly improves the ELISA detection efficiency using the same PDMS microfluidic system.

13.5.4.2 Case Study 2: Effective Enhancement of Fluorescence Detection Efficiency Using Alternative Blocking Process in Protein Microarray Assays

Aminosilanized silica substrates are used to prepare protein microarrays because of their strong binding affinity for proteins. In a typical microarray preparation procedure, after the probe proteins are spotted on an aminosilanized silica substrate, the background surface of the spotted silica substrate needs to be blocked to prevent nonspecific adsorption of target proteins. Conventionally, protein-based blocking solutions, such as albumin solutions (e.g. BSA solution), non-fat milk solutions, casein solutions or serum solutions are used. Although aminosilanized silica surfaces can be passivated by protein-based blocking solutions, a wet blocking process often causes smearing of individual protein spots and cross-contamination among probe spots (Fig. 13.28, steps c1 to f1). To eliminate the smearing and cross-contamination issues caused by conventional blocking processes using protein-based blocking solutions, Hsieh et al. employed a vapor-phase blocking process [93]. This method employs a highly fluorinated organosilane, FOTS (see No. 10 in Fig. 13.7), as the blocking agent to passivate the background surfaces of protein arrays prepared on aminosilanized glass slides (Fig. 13.28, step c2 to f2). As shown in Fig. 13.28 h and i, upon hydrolysis, FOTS can be made reactive, and bonds to the APTS (also called APTES, in Fig. 13.7) surface. During the vapor-phase FOTS blocking treatment, the exterior protein molecules extensively exposed to the FOTS vapor can serve as sacrificial materials to protect the interior protein molecules. Moreover, these loosely bound exterior protein molecules can be subsequently washed off from the spotted areas without causing undesired contamination on the background surface that has been passivated by the vapor-phase FOTS treatment.

Compared to several conventional blocking processes that use protein-based solutions, it was demonstrated that the vapor-phase blocking process could significantly reduce the smearing of protein spots and effectively enhance fluorescence detection efficiency by up to ~64 times [93].

13.5.4.3 Case Study 3: Control of Specific Reaction Kinetics Involving Bifunctional Cross-Linkers

AFM probes can be made into sensitive, chemically selective biosensors by attaching ligand molecules to the tips of the probes [94]. Many model systems that utilize ligands on AFM probes and complementary receptors on substrates have

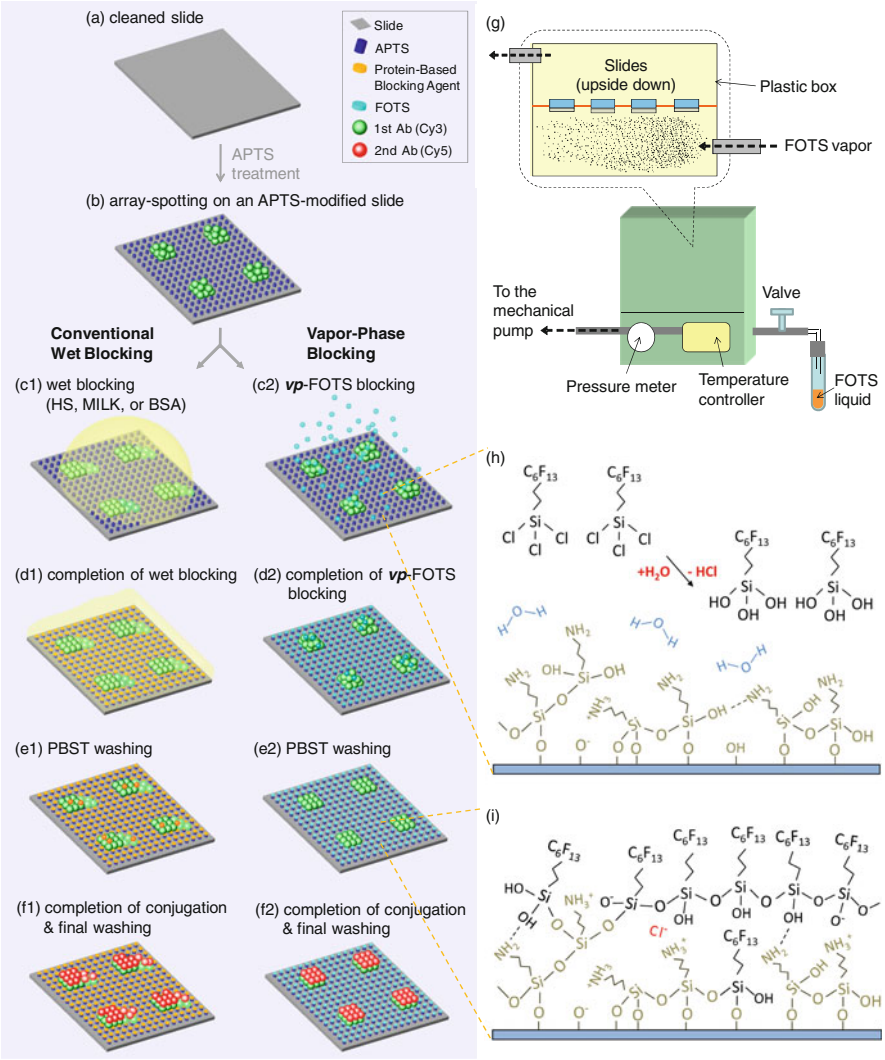


Fig. 13.28 Background blocking of protein arrays by a conventional protein-based wet blocking process vs. a vapor-phase blocking process using a highly fluorinated organosilane, *1H,1H,2H,2H*-perfluorooctyltrichlorosilane (FOTS) [94]. Reprinted with permission. Copyright 2009 American Chemical Society

been developed to study the dynamics of molecular interactions. The tips of AFM probes are made of polysilicon or silicon nitride. These surfaces are typically covered with a natural silicon oxide layer, and contain many reactive -SiOH groups. As described in Section 13.5.2.3, to start a multi-step modification on such type of surfaces, organosilanes with amine (such as APTES) or other functional groups

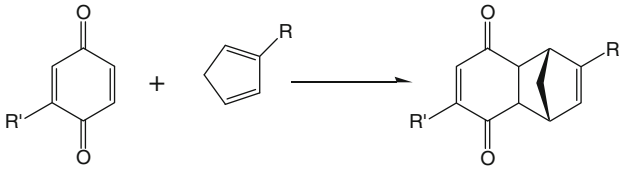
are required. After surface silanization of the AFM tip, a bifunctional cross-linker is needed to bond the ligand (or antibody) to the AFM tip. The cross-linkers must have a very flexible chain, and PEG (polyethylene glycol) is typically used to provide sufficient chain flexibility. As several surface modification schemes with different combinations of organosilanes and PEG-based bifunctional cross-linkers are possible, the reaction profiles and kinetics can differ from one scheme to another. To address how to handle these issues, five different schemes for AFM tip coating are provided as examples, and a discussion follows.

First, the linkage to the antibody is through the disulfide exchange reaction. Ebner et al. has been working on the synthesis and application of PEG-based heterobifunctional cross-linkers for the immobilization of antibodies onto AFM tips [95]. In their earlier study, PDP-PEG-NHS was used as the cross-linker to react with aminosilanized AFM tips [PDP is 3-(2-pyridyl)-dithiopropionyl, which contains a disulfide bond, i.e. PDP can undergo the exchange reaction described in reaction (13.10) with a thiol group; NHS is *N*-hydroxysuccinimide group, see reaction (13.6)]. Because there are no free thiol groups on antibodies, the thiol groups need to be introduced to the antibody first. The thiolated antibody needs to be purified before usage because the residual reagents and byproducts from the thiolation process can also react with the PDP group on the cross-linkers. To avoid the extra purifying process, another strategy is to treat the aminosilanized AFM tips with NHS-PEG-NHS to immobilize the antibodies. Compared to PDP-PEG-NHS, NHS-PEG-NHS is preferred because there is no need to add thiol groups to the antibody. However, the NHS-PEG-NHS has two amine-reactive NHS groups, and it can lose them both if they each react with the surface-bound amino groups. To prevent this, Ratto et al. developed another strategy, in which a mixture of APTES (see Fig. 13.7) and MTES [CH_3-Si-$(OC_2H_5)_3$] was used in the ratio of 1:250 to prepare an aminosilanized surface diluted by the methyl groups of MTES [96]. This would reduce the reaction kinetics of the amino groups on APTES towards the NHS group of the cross-linker, NHS-PEG-NHS. Using this strategy, one NHS group in the cross-linker could remain to react with the antibody.

Alternatively, the AFM tip can be treated with 3-mercaptopropyltrimethoxysilane to produce reactive thiol groups, and a maleimide-PEG-NHS cross-linker can be used to react with the AFM tip via a reaction between the maleimide and thiol groups. Although a thiol functional group reacts with maleimide relatively quickly, it still can react with NHS to some extent, though less favorably. Thus this technique cannot completely prevent the cross-linker from forming a loop on the AFM tip. Another strategy that was recently developed by Ebner employed NHS-PEG-CHO as a cross-linker to react with aminosilanized AFM tips [95]. Although both NHS and CHO can react with the amino group, the kinetics of amine with NHS overwhelms the kinetics of amine with CHO; as such, NHS-PEG-CHO preferentially reacts with the surface-bound amino group via the NHS group. Following the treatment of the AFM tips with NHS-PEG-CHO, the free CHO group can be exploited to react with the amino group of the antibody for the preparation of biofunctional AFM tips.

13.5.4.4 Case Study 4: Surface Modification Using Elaborately Derivatized Functional Groups

To exploit alternative chemical reactions for surface modification in BioMEMS, organic synthesis can be performed to prepare chemical species derivatized with special functional groups for desired chemical reactions to occur. For example, Houseman et al. exploited the Diels-Alder reaction (13.15) to perform mediated conjugation between the cyclopentadiene group derivatized on a peptide analogue and the benzoquinone group immobilized on a gold surface (Fig. 13.29) [97]. Although substantial synthetic work is required to synthesize a cyclopentadiene-derivatized peptide analogue and a benzoquinone-derivatized thiol, this study shows that chemical conjugation via the Diels-Alder reaction is highly efficient and selective for the



(13.15)

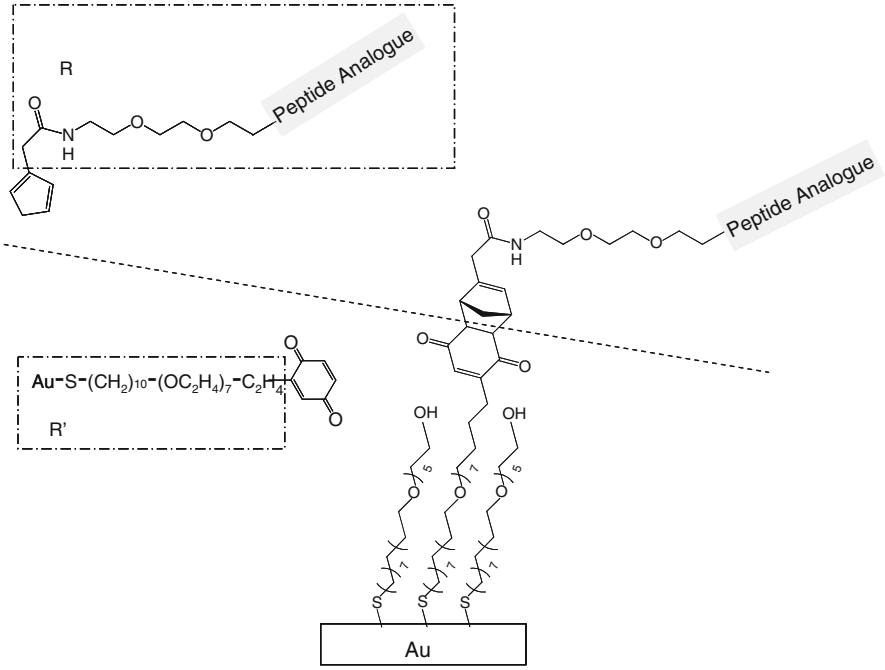


Fig. 13.29 Mediated conjugation of a peptide analogue to a Au-based substrate via Diels-Alder reaction, as demonstrated by Houseman et al. [97]

preparation of peptide chips. As mentioned in Case study 3, the cross-linking reactions are sometimes not very specific and can cause different side reactions. If a very specific and efficient reaction is required, preparation of certain compounds or reagents with desired functional groups by elaborate synthesis may be necessary.

13.5.4.5 Case Study 5: Surface Patterning by Microcontact Printing

Microcontact printing is a surface patterning technique that can be conveniently employed for many applications [98–105]. The basic working principle of microcontact printing is illustrated in Fig. 13.30. To perform surface modification by microcontact printing, a patterned elastomer stamp (usually a PDMS stamp) must be fabricated. Then an "ink" solution containing a chemical (or a mixture of chemicals) that can react with the target substrate surface (e.g. organosilanes for silica surfaces, thiols for noble metal surfaces) is applied to the patterned stamp surface. Depending on the nature of the "ink" solution, (e.g. viscosity, reactivity, stability etc.), some precautions must be considered during the preparation, handling and/or

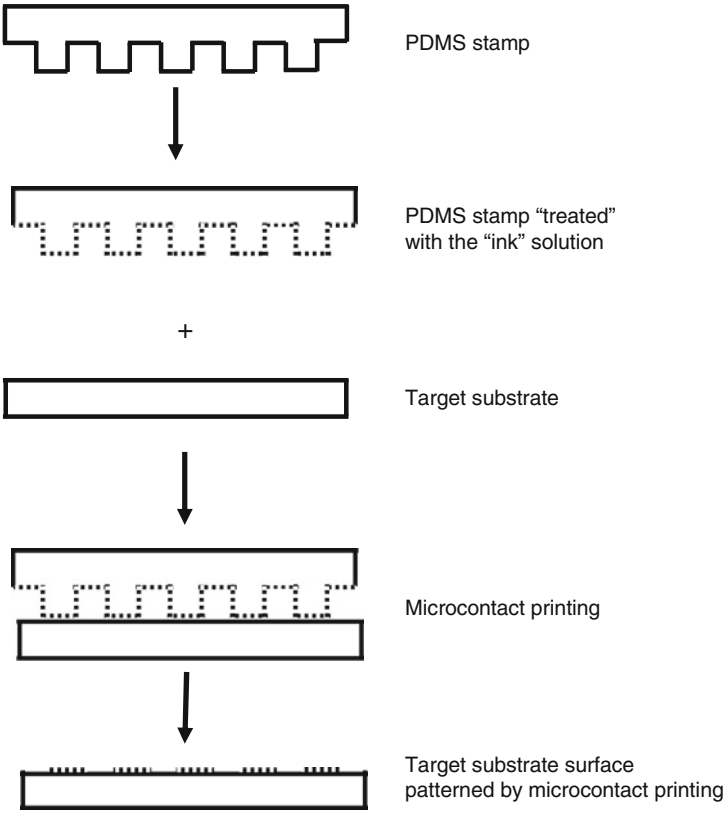


Fig. 13.30 Schematic illustration of microcontact printing

application of the "ink" solution (e.g. concentration of the "ink" solution, extent to which the solvent of the "ink" solution should evaporate after the "ink" has been applied to the patterned stamp surface, etc). Ideally, only a thin physically adsorbed layer of the surface-reactive chemical on the patterned stamp surface is desired after the elastomer stamp is "treated" with the "ink" solution. Then the stamp is brought into contact with the target substrate surface. As shown in Fig. 13.30, the surface-reactive chemical reacts with the target substrate surface in the areas that contact the patterned stamp surface. After the stamp is removed from the target substrate surface, a geometrically and chemically defined pattern can be obtained on the target substrate surface for further use.

Because of its ease and convenience, microcontact printing is widely used for the preparation of patterned bioactive surfaces [106]. For example, Chen et al. prepared gold surfaces with patterned bioactive proteins (fibronectin, vitronection, collagen etc.) to study the growth and apoptosis of bovine capillary endothelial cells [107]. The gold surface was first patterned with hexadecanethiol by microcontact printing. The patterned gold surface was then treated with a tri(ethylene glycol)-terminated hexadecanethiol solution to passivate the rest of the unpatterned gold surface. When the above patterned/passivated gold surface was immersed in a protein solution, preferential adsorption of the protein occurred on the area with hydrophobic hexadecyl SAM coating. Finally, cell cultures grown on the gold surfaces with various patterned bioactive proteins were investigated and compared. From this study, Chen et al. found that it was the extent of cell spreading, not the area of adhesive contact, that controlled the life and death of bovine capillary endothelial cells.

13.6 Surface Coating for Optical Applications

MEMS devices have been applied to optical sensing applications and lightwave communications including optical switches, waveguides, tunable filters, and reconfigurable wavelength add and drop multiplexers. Components in these MEMS devices interact, receive, and transport light. As light interacts with MEMS devices, three optical functions are relevant to performance: reflection, transmission, and absorption. The surfaces on the MEMS devices have strong effects on these optical functions.

Many optical materials can be processed in MEMS fabrication, including non-crystalline materials (such as glasses and metals), crystalline materials (such as silicon, quartz, and germanium wafers), and polymers (plastics, photoresist, and elastomers). The fabrication techniques used to obtain the desired optical properties – such as physical vapor deposition, chemical vapor deposition, sol-gel, spin coatings, self assembly, phase separation, and imprinting – are discussed in the other chapters of this book.

This section begins with theory and design concepts related to the optical phenomena of surface films, including refraction, dispersion, absorption, internal/

external reflection, polarization by reflection, and antireflection. The material properties and fabrication processes of these coatings and structures are discussed in the second part of this section, along with their corresponding advantages and challenges. Several useful case studies related to antireflection, absorption, and refraction of designated light waves will be discussed as examples of the design and fabrication of optical MEMS devices. Lastly, surface roughness and control will be summarized.

13.6.1 Fundamentals of Optical Phenomena on Surface Coatings

The performance of optical MEMS devices usually relies on functional optical properties such as antireflection, high absorption, refraction, and polarization of device surfaces. The desired properties are usually achieved by applying special coatings or material structures to the surface. Most optical property transformations through surface coatings and structures are based on the scattering or interference of light waves at the interface [108, 109]. The interface is very sensitive to film thickness relative to the wavelength of the incident light, which can range from tens of nanometers to several microns. As a result, surface planarization properties [109] have strong effects on the phenomena occurring at the incident interfaces. Since the design and selection of coatings and structures are typically the first things to consider, we will start with optical theory and design concepts in this section.

13.6.1.1 Index Variation of Materials Versus Wavelength [108]

Dielectric Materials

When light transmits in the medium of bulk matter, for example in a homogeneous, isotropic dielectric material, the phase speed of the light in the medium can be expressed by

$$v = \frac{1}{\sqrt{\varepsilon\mu}} \tag{13.16}$$

where ε is the permittivity and μ is the permeability of the medium. As a result, the ratio of the speed of an electromagnetic wave in a vacuum to its speed in matter is defined as the absolute index of refraction, n:

$$n \equiv \frac{c}{v} = \sqrt{\frac{\varepsilon\mu}{\varepsilon_0\mu_0}} \tag{13.17}$$

where c is the light speed, ε_0 is the permittivity, and μ_0 is the permeability in free space.

The index n can also be expressed in terms of the relative permittivity and relative permeability of the medium:

$$n = \sqrt{K_E K_M} \approx \sqrt{K_E} \tag{13.18}$$

where $K_E = \varepsilon/\varepsilon_0$ is the dielectric constant or relative permittivity, and $K_M = \mu/\mu_0$ is the relative permeability. Since K_M does not usually deviate much in the visible regions of the spectrum, it can be neglected.

This relation is only valid for a few simple gases such as air, helium, and hydrogen. The approximate refractive indices of some commonly used materials are listed in Table 13.3, and in other sections (Tables 13.4, 13.5, 13.6, and 13.7). However, the indices of dielectric materials are often frequency-dependent. This is called "dispersion", and can be expressed by the dispersion equation for a dielectric material:

$$n^2(\omega) = 1 + \frac{Nq_e^2}{\varepsilon_0 m_e}\left(\frac{1}{\omega_0^2 - \omega^2}\right) \tag{13.19}$$

where q_e is the electron charge, m_e is the electron mass, N is the number of contributing electrons per unit volume, and ω_0 is the resonance frequency. The index n increases as ω approaches ω_0 from below, but drops to less than 1 when ω is larger than ω_0. The index of an optical material varies with wavelength (index dispersion), as indicated in Fig. 13.31. The region with a large index jump corresponds to the absorption bands of the material. After the jump, the index starts to decrease as wavelength increases, until the wavelength reaches the next absorption band. Jumps may be located in different regions of the spectrum, for example one in the infrared (ω_i) region and the other in the ultraviolet (ω_u) region. The targeted visible spectra lie between these regions.

Metals

When light interacts with bulk metal, the conduction electrons undergo oscillation and collisions with the lattice, and thereby generate absorption. The electrical field

Table 13.3 Approximate indices of refraction of various substances [108]

Air	1.00029	Light flint glass	1.58
Ice	1.31	Polystyrene	1.59
Water	1.333	Carbon disulfide (CS_2)	1.628
Ethyl alcohol (C_2H_5OH)	1.36	Dense flint glass	1.66
Fused silica (SiO_2)	1.4584	Lanthanum flint glass	1.80
Carbon tetrachloride (CCl_4)	1.46	Zircon (ZrO_2SiO_2)	1.923
Turpentine	1.472	Fabulite ($SrTiO_3$)	2.409
Benzene (C_6H_6)	1.501	Diamond (C)	2.417
Plexiglass	1.51	Rutile (TiO_2)	2.907
Crown glass	1.52	Gallium phosphide	3.50
Sodium chloride (NaCl)	1.544	Silicon nitride (Si_3N_4)	2.04

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Table 13.4 Properties of antireflection coating materials [109, 110]

Material	Refractive index at $\lambda = 546\,\text{nm}$	Evaporation temperature (°C)	Comments
Aluminum oxide (Al_2O_3)	1.66	2045	E-beam evaporation with substrate at 200°C, hard and chemical resistant film
Cadmium sulphide (CdS)	2.42	800	E-beam evaporation in high vacuum, requires care
Cadmium telluride (CdTe)	2.69		E-beam evaporation
Ceric oxide (CeO_2)	1.95	1600	Thermal evaporation, soft film
Cerous fluoride (CeF_3)	1.63	1342	E-beam evaporation with substrate at 200°C
Hafnium oxide (HfO_2)	2.05		
Cryolite (Sodium aluminum fluoride, Na_3AlF_6)	1.22	1000	Thermal evaporation, soft film
Lanthanum fluoride (LaF_3)	1.55	1490	Thermal evaporation
Lead fluoride (PbF_2)	1.75	855	Thermal evaporation, soft film
Lithium fluoride (LiF)	1.303	870	Thermal evaporation in high vacuum, soft transparent film
Magnesium fluoride (MgF_2)	1.38	1266	Thermal evaporation in high vacuum
Magnesium oxide (MgO)	1.68	2800	E-beam evaporation, hard film
Neodymium fluoride (NdF_3)	1.55	1410	Thermal evaporation, very hard and transparent film
Neodymium oxide (Nd_2O_3)	1.79	1900	Thermal evaporation, very hard and transparent film
Silicon monoxide (SiO)	1.49–1.80	1250	Depends on the rate of deposition, thermal evaporation at O_2 environment, hard film
Silicon-silica mix (Si-SiO_2)	1.49		Thermal evaporation, hard and transparent film
Sodium fluoride (NaF)	1.29	988	Thermal evaporation, soft and transparent film, easily to be attacked by moisture

Table 13.4 (continued)

Material	Refractive index at $\lambda = 546\,\text{nm}$	Evaporation temperature (°C)	Comments
Thorium oxide (ThO_2)	1.86	3050	E-beam evaporation with substrate at 200°C
Thorium oxyfluoride ($ThOF_2$)	1.50	1100	Thermal evaporation, good adhesion to substrate
Titanium monoxide (TiO)	2.08–2.32	1750	Depends on the rate of deposition, slow thermal evaporation at O_2 environment, hard and transparent film
Yttrium oxide (Y_2O_3)	1.79	2410	E-beam evaporation, very hard film
Zinc selenide (ZnSe)	2.57	900	Thermal evaporation, soft and transparent film
Zinc sulfide (ZnS)	2.35	1000	Thermal evaporation, soft and transparent film
Zirconium oxide (ZrO_2)	2.05	2714	E-beam evaporation with substrate at 200°C
Germanium (Ge)	4.0[a]		E-beam evaporation
Silicon	3.50[a]		E-beam evaporation

[a]not transparent in visible spectrum

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Table 13.5 Properties of some commercial optical glasses [109]

Type	n_d	n_f	n_c	V_d	α (10^{-6}/K)	T_g (°C)	d (g/cm^3)	HK	T_i
BK7	1.51680	1.52283	1.51432	64.17	7.1	559	2.51	520	0.991
K5	1.52249	1.52910	1.51982	59.48	8.2	543	2.59	450	0.984
BaK1	1.57250	1.58000	1.56949	57.55	7.6	602	3.19	460	0.976
SK4	1.61272	1.62059	1.60954	58.63	6.4	643	3.57	500	0.973
KF6	1.51742	1.52492	1.51443	52.20	6.9	446	2.67	420	0.985
SSK4	1.62765	1.62611	1.61427	55.14	6.1	639	3.63	460	0.972
LaK8	1.71300	1.72298	1.70898	53.83	5.6	640	3.78	590	0.950

n_d: index at helium d line (587.5 nm); n_f: index at hydrogen f line (486.1 nm)
n_c: index at hydrogen c line (656.3 nm); α: thermal expansion coefficient
V_d: Abbe V-number (reciprocal relative dispersion), $V_d = (n_d - 1)/(n_f - n_c)$
T_g: glass transition temperature; d: density; HK: Knoop hardness
T_i: internal transmittance at 0.4 μm for a thickness of 25 mm
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Table 13.6 Properties of some crystalline materials [109]

Material	Transmission range, nm	Index	Applications
Crystal quartz (SiO_2)	120–4500	1.544	Birefringence
Calcite ($CaCO_3$)	200–5500	1.658	Birefringence
Rutile (TiO_2)	430–6200	2.62	Birefringence
Sapphire (Al_2O_3)	140–6500	1.834	
Strontium titanate ($SrTiO_3$)	400–6800	2.490	IR immersion lens
Magnesium fluoride (MgF_2)	110–7500	1.378	IR optics, low reflection coatings
Lithium fluoride (LiF)	120–9000	1.429	Prisms, windows, apochromatic lens
Calcium fluoride (CaF_2)	130–12,000	1.442	Prisms, windows, apochromatic lens
Barium fluoride (BaF_2)	250–15,000	1.512	windows
Sodium chloride (NaCl)	200–26,000	1.791	Prisms, windows
Silver chloride (AgCl)	400–28,000	2.096	
Potassium bromide (KBr)	250–40,000	1.590	Prisms, windows
Potassium iodide (KI)	250–45,000	1.922	
Cesium bromide (CsBr)	300–55,000	1.709	Prisms, windows
Cesium iodide (CsI)	250–80,000	1.806	Prisms, windows
Silicon (Si)	1200–15,000	3.498	IR optics
Germanium (Ge)	1800–23,000	4.102	IR optics
Zinc selenide (ZnSe)	500–22,000	2.489	
Zinc sulfide (ZnS)	500–14,000	2.292	
AMTIR (Ge/As/Se)	700–14,000	2.606	
Gallium arsenide (GaAs)	1000–15,000	3.317	
Cadmium telluride (CdTe)	200–30,000	2.307	
Magnesium oxide (MgO)	250–9000	1.722	

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Table 13.7 Properties of some optical polymers [109, 110, 177]

Material	n_d	V_d	Light transmitance (%) 3 mm	Deflection temperature (°C) ASTM D648	Tensile Modulus (MPa)	Density (g/cm^3)	Water Absorption (%) 24 h, 23°C	Coefficient of thermal expansion, ([a]10^{-5})1/k	Suitability for vacuum coating
Poly (methylmetharcrylate) (Plexiglas 7 N)	1.491	58	92	95	3200	1.19	0.3	6.8	No
Polycarbonate (Makrolon LQ2647)	1.585	30	91	124	2400	1.2	0.12	6.6	Yes
Polycycloolefin (Topas 5013)	1.533	58	92	123	3100	1.02	<0.01	6	Yes
Polysulfone (Udel P-1700)	1.634	23	84	174	2480	1.24	0.3	5.6	Unknown
Polyethersulfon (Ultrason E2010)	1.65		80	208	2700	1.37	2.1	5.5	Yes
Polyamide (Trogamid CX 7323)	1.516	45	89	122	1400	1.02	0.3	9	Yes
[a]SU-8 3050 (UV)	1.57		93	200	73	1.15	0.55	5.2	Yes
[a]PMMA (x-ray)	1.491		92	180	3240	1.19	2	6.8	Yes
[b]NOA 63 (UV)	1.56		99		1655	1.2			Unknown
[a]AZ 9620 (UV)						1.07			No
[a]JSR THB-130 N (UV)						1.4			Yes

[a]Photoresist for different spectrum
[b]UV curable material
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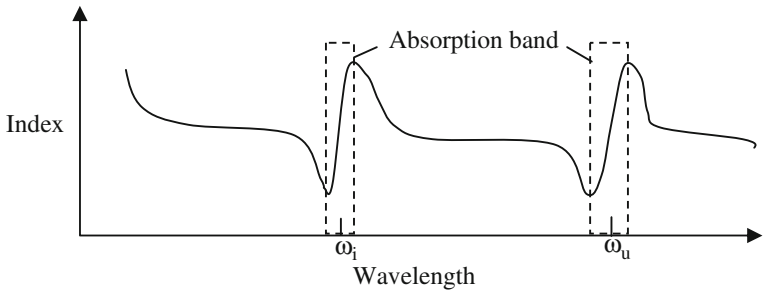

Fig. 13.31 Index dispersion of an optical material [108]. Reprinted with permission. Copyright 2002 Addison Wesley

of light, E, in the y direction is expressed by the following equation with a complex refractive index:

$$\vec{E} = \vec{E}_0 \mathrm{e}^{-\omega n_\mathrm{I} \mathrm{y/c}} \mathrm{e}^{\mathrm{i}\omega(t - n_\mathrm{R} y/c)} \tag{13.20}$$

where n_R and n_I are the real and imaginary parts of the refractive index, respectively. Thus, when the wave progresses into a conductor, the amplitude $\vec{E}_0 \mathrm{e}^{-\omega n_\mathrm{I} \mathrm{y/c}}$ is exponentially attenuated and the penetration depth $y = c/2\omega n_\mathrm{I}$ becomes very shallow. For copper, for example, the penetration depth is about 3 nm when the wavelength is about 500 nm. Since the incident waves cannot effectively penetrate the material, bulk metal materials are opaque. However, light can partially penetrate metal when the metal film is thin enough.

For thin films, the dispersion equation for metal becomes:

$$n^2(\omega) = 1 - \frac{N q_\mathrm{e}^2}{\varepsilon_0 m_\mathrm{e} \omega^2} \tag{13.21}$$

At high frequencies, the free electrons and positive ions in a metal will carry out many oscillations between each collision and can be thought of as a plasma with a density oscillating at a natural frequency of $\omega_\mathrm{p} = (N q_\mathrm{e}^2/\varepsilon_0 m_\mathrm{e})^{1/2}$. Therefore, when the index of the metal becomes complex in the case of $\omega < \omega_\mathrm{p}$ the transmission of the light wave drops off exponentially, and the reflection from the surface greatly increases. In contrast, metal becomes transparent when $\omega > \omega_\mathrm{p}$, e.g. when X-rays are encountered. Since the index of refraction of a metal is usually complex, incident light will also encounter a frequency dependent absorption when impinging on a metal.

13.6.1.2 Fresnel Equation for Reflection [108]

Reflection from a Dielectric

The relationships between electric fields for reflection and transmission are shown in Fig. 13.32.

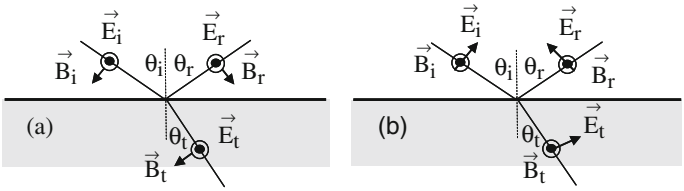

Fig. 13.32 The reflection and transmission of an electromagnetic wave incident on an optical material with electrical field (**a**) normal to, or (**b**) in the plane-of-incidence

The reflectance R is defined as

$$R \equiv \frac{I_r A\cos\theta_r}{I_\mathrm{i} A\cos\theta_\mathrm{i}} = \frac{I_r}{I_\mathrm{i}} = \frac{v_r \varepsilon_r E_{0r}^2/2}{v_\mathrm{i}\varepsilon_\mathrm{i} E_{0\mathrm{i}}^2/2} = \left(\frac{E_{0r}}{E_{0\mathrm{i}}}\right)^2 = r^2 \tag{13.22}$$

where I is the intensity of light, r is the reflection coefficient, and θ_i and θ_t are incident and transmission angles, respectively. The transmittance T is defined as

$$T \equiv \frac{I_\mathrm{t}\cos\theta_\mathrm{t}}{I_\mathrm{i}\cos\theta_\mathrm{i}} = \frac{n_\mathrm{t}\cos\theta_\mathrm{t}}{n_\mathrm{i}\cos\theta_\mathrm{i}}\left(\frac{E_{0\mathrm{t}}}{E_{0\mathrm{i}}}\right)^2 = \frac{n_\mathrm{t}\cos\theta_\mathrm{t}}{n_\mathrm{i}\cos\theta_\mathrm{i}}\mathrm{t}^2 \tag{13.23}$$

where t is the transmission coefficient. Assuming no absorption, it can be simply expressed as $R + T = 1$. It can also be expressed in component form as

$$R_\perp = r_\perp^2 = \left(\frac{\sin(\theta_\mathrm{i} - \theta_\mathrm{t})}{\sin(\theta_\mathrm{i} + \theta_\mathrm{t})}\right)^2 \tag{13.24}$$

$$R_\mathrm{ll} = r_\mathrm{ll}^2 = \left(\frac{\tan(\theta_\mathrm{i} - \theta_\mathrm{t})}{\tan(\theta_\mathrm{i} + \theta_\mathrm{t})}\right)^2 \tag{13.25}$$

$$T_\perp = \left(\frac{n_\mathrm{t}\cos\theta_\mathrm{t}}{n_\mathrm{i}\cos\theta_\mathrm{i}}\right)\mathrm{t}_\perp^2 = \left(\frac{n_\mathrm{t}\cos\theta_\mathrm{t}}{n_\mathrm{i}\cos\theta_\mathrm{i}}\right)\left(\frac{2\sin\theta_\mathrm{t}\cos\theta_\mathrm{i}}{\sin(\theta_\mathrm{i} + \theta_\mathrm{t})}\right)^2 \tag{13.26}$$

$$T_\mathrm{ll} = \left(\frac{n_\mathrm{t}\cos\theta_\mathrm{t}}{n_\mathrm{i}\cos\theta_\mathrm{i}}\right)\mathrm{t}_\mathrm{ll}^2 = \left(\frac{n_\mathrm{t}\cos\theta_\mathrm{t}}{n_\mathrm{i}\cos\theta_\mathrm{i}}\right)\left(\frac{2\sin\theta_\mathrm{t}\cos\theta_\mathrm{i}}{\sin(\theta_\mathrm{i} + \theta_\mathrm{t})\cos(\theta_\mathrm{i} - \theta_\mathrm{t})}\right)^2 \tag{13.27}$$

where $r_\perp$, r_ll are the reflection coefficients in the normal/parallel directions and $\mathrm{t}_\perp$, t_ll are the transmission coefficients in the normal/parallel directions to the plane-of-incidence, respectively. The reflectance R and transmittance T are functions of the angle of incidence θ_i, angle of transmissionθ_t, and the indices of the two media, n_i and n_t.

Furthermore, reflectance and transmittance also have the following relationship

$$R_\perp + T_\perp = 1 \text{ and } R^\mathrm{ll} + T^\mathrm{ll} = 1 \tag{13.28}$$

If the incident light is non-polarized and can be represented by two orthogonal, incoherent, and equal-amplitude plane polarized light components, the amount of energy in either of the two states is the same as that in the other. Therefore, the reflectance in natural light, $R = I_r/I_\mathrm{i}$, becomes

$$R = \frac{I_{r\mathrm{ll}} + I_{r\perp}}{I_\mathrm{i}} = \frac{1}{2}(\mathrm{R}_\mathrm{ll} + R_\perp) \tag{13.29}$$

When the incident angle θ_i is zero, the reflectance and transmittance are

$$R = R_\mathrm{ll} = R_\perp = \left(\frac{n_\mathrm{t} - n_\mathrm{i}}{n_\mathrm{t} + n_\mathrm{i}}\right)^2 \tag{13.30}$$

$$T = T_\mathrm{ll} = T_\perp = \frac{4\mathrm{n_t}n_\mathrm{i}}{(n_\mathrm{t} + n_\mathrm{i})^2} \tag{13.31}$$

Reflection from a Metal

When a light wave propagates at some angle to the normal of a high-conductivity metal surface, the wave fronts align with the surface of constant amplitude. As a result, in a good conductor the transmitted wave propagates in a direction normal to the interface regardless of the incident angle. The reflectance R of normal incidence on a metal becomes:

$$R = \frac{(n_\mathrm{R} - n_\mathrm{i})^2 + n_\mathrm{I}^2}{(n_\mathrm{R} + n_\mathrm{i})^2 + n_\mathrm{I}^2} \tag{13.32}$$

where n_R and n_I are the real and imaginary parts of the refractive index.

If the conductivity of the material is zero, i.e. $n_\mathrm{I} = 0$, the reflectance is the same as that of a dielectric material. However, in a good conductor, in which n_I is large and n_R is small, the reflectance is large. For example, at an incident wavelength of $\lambda_0 = 589.3$ nm, n_R and n_I for bulk tin are 1.5 and 5.3, respectively, giving an R value of 0.8. The reflectance R is also frequency dependent. For example, gold and silver can transmit at wavelengths well below 530 and 316 nm, respectively.

13.6.1.3 Principle of Antireflection (AR) [108]

Antireflection by Thin Film Coatings

Figure 13.33 shows a plot for a linearly polarized light incident on a thin dielectric film (with reflective index n_1) between two semi-infinite transparent media (n_0 and n_s),

In the case of normal incidence of light, i.e. $\theta_\mathrm{iI} = \theta_\mathrm{tI} = \theta_\mathrm{tII} = 0$, the reflectance R_1 can be simplified to

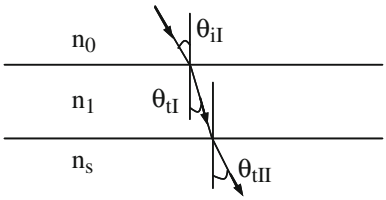

Fig. 13.33 Passage of light through a thin film

$$R_1 = \frac{n_1^2(n_0 - n_s)^2\cos^2 k_0 h + (n_0 n_s - n_1^2)^2\sin^2 k_0 h}{n_1^2(n_0 + n_s)^2\cos^2 k_0 h + (n_0 n_s + n_1^2)^2\sin^2 k_0 h} \tag{13.33}$$

where k_0 is $2\pi/\lambda_0$ and h is the thickness of the film. When $k_0 h = \pi/2$, the optical thickness h of the film is an odd number of quarter wavelengths ($h = \lambda_0/4$), and the reflectance reduces to

$$R_1 = \frac{(n_0 n_s - n_1^2)^2}{(n_0 n_s + n_1^2)^2} \tag{13.34}$$

If a zero reflection from the surface is desired, the required reflective index is

$$n_1 = \sqrt{n_0 n_s} \tag{13.35}$$

Thus the first and simplest way to create an antireflection surface is to choose a coating material with its index equal to the geometric mean of the top and bottom media (n_0 and n_s, respectively), and to use a coating thickness of one quarter wavelength. For an antireflection coating layer on a glass plate of index 1.5, the required index of the AR layer is $\sqrt{1 \times 1.5} = 1.225$. However, this value is much below that of commonly used low index materials, such as MgF_2, which has an index of 1.38. As a result, a single antireflection layer of MgF_2 cannot thoroughly eliminate reflection from the glass surface. The reflectance is around 10%, according to Equation (13.34) at normal incidence. Multiple layer coatings can be used to further reduce the reflection from the surface. For a double layer (with indices n_1 and n_2 for the first and second layers), the reflectance at normal incidence becomes:

$$R_2 = \frac{(n_2^2 n_0 - n_s n_1^2)^2}{(n_2^2 n_0 + n_s n_1^2)^2} \tag{13.36}$$

For zero reflection, R_2 must vanish and thus we require:

$$n_2/n_1 = \sqrt{n_s/n_0} \tag{13.37}$$

If the same n_0 and n_s values are used as previously mentioned, n_2/n_1 must equal 1.225. In this case, it is much easier to find a proper set of n_2 and n_1 instead of searching for only one value as in the single layer case. The two-layer system is a

(glass)-(high index)-(low index)-(air) system, and the two coating materials may be selected from many different choices, as shown in Table 13.4. For example, we can select hafnium oxide (HfO_2, $n_2 = 2.05$) as the high index material, and aluminum oxide (Al_2O_3, $n_1 - 1.62$) as the low index material. The index ratio n_2/n_1 for these choices is 1.265, much closer to 1.225 than the single layer index of 1.38 (for MgF_2) considered earlier. R_2 is reduced to 0.107%.

Using a similar concept, one can establish a quarter-wave stack by stacking a number of quarter-wave layers, such as the (glass)$(HL)^p$(air) system shown in Fig. 13.34. Here p indicates the number of pairs of stacks. With proper design, the reflectance can be further reduced for broader wavelength regions and incident angles. The coating can also be tailored for high pass filters (e.g. attenuating lower frequencies, such as (glass)(0.5L)$(HL)^p$(0.5L)(air) system) or low pass filters (such as (glass)(0.5H)$(HL)^p$(0.5H)(air) system) [111, 112]. An example is also provided in Section 13.6.2.1.

Antireflection by Nano-scale Surface Structures: Moth Eye Structures

In addition to the use of multiple film coatings as antireflection (AR) layers, the fabrication of submicron structures on a dielectric/polymer surface can also effectively eliminate reflective light from the surface in a wide viewing angle and broad spectrum [113]. These structures were first observed on the eyes of some night-flying moths, on which thousands of rows of bump-like protrusions around 200–300 nm in height and pitch are accommodated inside hexagonal sectors [113, 114]. These nanostructures reduce light reflection by creating a refractive index gradient between the air-eye interface, which can gradually change the light speed from the airside to the eye side and hence eliminate reflection. The low reflection from the moth's eyes enables the moth to effectively protect itself from predators as it flies in the moonlight. The moth eye has motivated many AR applications recently, including solar panels, windows, computer screens, flat-panel displays, vehicle dashboards, and optical elements [115]. Usually AR structures accompany a hydrophobic surface

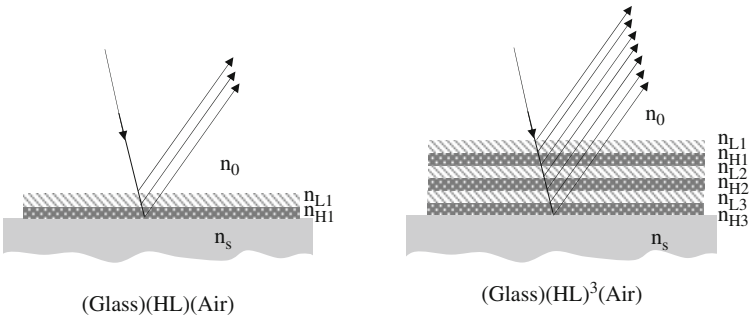

Fig. 13.34 Stacks of quarter layers for antireflection coatings. (**a**) A double layer quarter wavelength antireflection coating (**b**) a six-layer antireflection coating

coating to prevent environmental contamination such as dust, bacteria, and aerosols [115].

The continuous nanostructures on moth eyes can be modeled as a stack of many layers, with each layer having a slightly different refractive index as a result of the fractional area each layer occupies on the substrate material [116–118], as shown in Fig. 13.35. In the limit of a continuously varying surface profile, the nano-scale structures are analogous to a coated film with a continuous variation of index from that of the surrounding medium to that of the underlying substrate. The nanostructures can also be considered as an impedance matching material at optical wavelengths [116]. The spacing, depth, and cross-sectional geometry of the nano-scale layered structures determine the AR properties and the band width for operation [116–118].

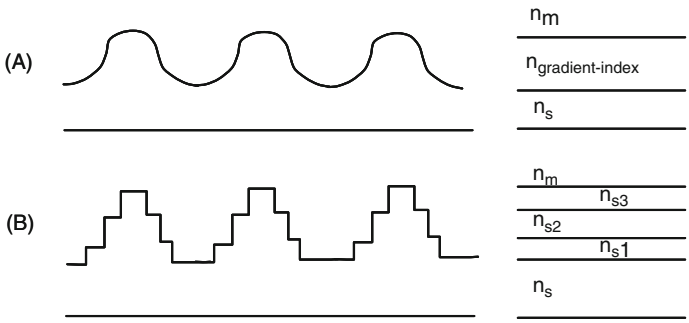

Fig. 13.35 Model of moth eye structures (**a**) continuous moth eye nano structure (**b**) discretized stacking structure (n_s: index of substrate, n_m: index of medium, n_{s1}~n_{s3}: index of each stacking layer)

Moth eye structures can be designed using different materials for the spectrum in ultraviolet, visible, or infrared region. Three important rules need to be followed for the design of effective AR structures [116]. First, to avoid significant diffraction and surface scattering effects, the period (P) of the nano-structures must be smaller than the shortest wavelength of operation (λ_{min}) divided by the index of refraction of the substrate (n_s) [116].

$$P \leq \frac{\lambda_{min}}{n_s} \tag{13.38}$$

This means that only the zeroth order reflected and transmitted waves can propagate into the substrate with no aberration or distortion. If the pitch is too large, the structures will behave like a conventional diffraction grating and scatter most of the light into higher orders. Second, the height (h) of the nano-structures needs to be at least 40% of the longest operating wavelength λ_{max} [116–118]. Note that the optimum depth is a function of the substrate material index and the reflectance will increase quickly when the depth is larger than λ_{max} [117].

$$0.4\lambda_{max} \leq h \leq \lambda_{max} \tag{13.39}$$

This criterion is a rough estimate for cases with light normally incident on a surface with continuous surface area variation, and might be varied with different viewing angles, surface structures, and spectrums [116]. Third, the optimal profile will be close to a pyramid structure with straight or curved sidewalls [116].

13.6.1.4 Principle of Absorption [108, 109]

The transmission of a material usually involves two effects. The surface transmission T_s occurs at the interface and is affected by the reflection at the material surface. The internal transmission T_i occurs within the material and is affected by the absorption of light. The total transmission T of the material can be expressed as the product of the surface and internal transmissions.

The surface transmission T_s can be estimated from Equation (13.31) for normal incident light. For light transmitting from air into the material, the surface transmission will be

$$T_s = \frac{4n}{(n+1)^2} \tag{13.40}$$

The internal transmission, usually correlated to the absorption, can be formulated as

$$T_i = t^x \tag{13.41}$$

where t is the transmission of a unit thickness of material, and x is the thickness. For example, if a 1 mm thick layer of a material has a transmission efficiency of 30% for red light, a 2 mm thickness of this material will give $0.3^2 = 9\%$ transmission.

If the light transmitted through the first surface of the material is partially transmitted at the second interface, and partially reflected and transmitted in the material several times, the resulting maximum transmission T_{max} for a non-absorbing plate will be:

$$T_{max} = \frac{2n}{(n^2+1)} \tag{13.42}$$

The reflection of the uncoated plate of index n will be

$$R = 1 - T_{max} = \frac{(n-1)^2}{(n^2+1)} \tag{13.43}$$

It is also noted that the transmission of a material is a wavelength-dependent property, and cannot be treated as a simple value over a large spectrum.

13.6.1.5 Surface Plasmon Resonance

A special phenomenon in optical reflection called surface plasmon resonance (SPR) has been reported as a sensitive technique for surface change monitoring [119]. As mentioned previously, light reflects and transmits at the interface of two transparent media. Total internal reflection occurs if the light approaches from the side of high reflective index with an incident angle higher than the critical angle. One popular setup for SPR, proposed by Krestchmann [120] in 1971, involves depositing a thin metal film on top of a prism, as shown in Fig. 13.36a. As the angle of the incidence changes, the intensity of the reflected light reaches a dip (minimum) at a specific angle called the SPR angle (Fig. 13.36b). This minimum occurs when photons of p-polarized light interact with the free electrons of the metal layer, introducing charge density oscillations (called plasmons) and thus reducing the intensity of the reflected light. Surface plasmons (or surface plasmon polaritrons, SPP) are surface electromagnetic waves that propagate in parallel along a metal/dielectric interface. When a light beam impinges onto a metal film at a specific (resonance) angle, the surface plasmons are set to resonate with the light. The fully reflected beam leaks an electrical field intensity (i.e. evanescent field wave) a short distance (tens of nanometers) into a medium of a lower refractive index (Fig. 13.36a).

SPR has been shown to be sensitive to very low levels of material adsorbed onto a surface (much less than a monolayer). Typical metals that support surface plasmons are silver and gold. A SPR-based biomolecular interaction monitoring system was first demonstrated by Liedberg [122]. The monitoring of the surface plasmon

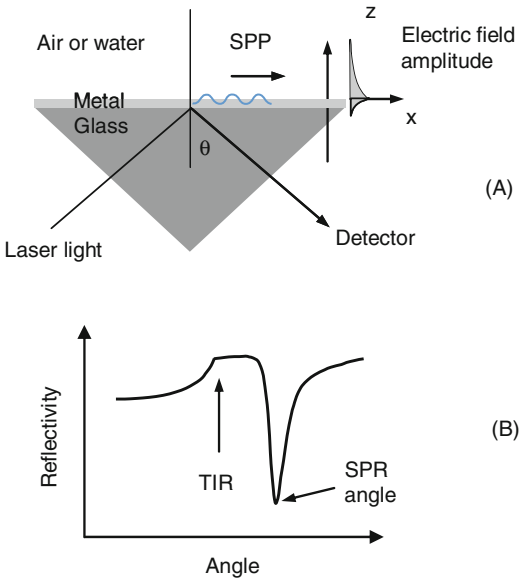

Fig. 13.36 Reflectivity of the exciting beam for surface plasmon resonance [121]; (**a**) schematic drawing of SPR measurement setup; (**b**) the reflectivity. Reprinted with permission. Copyright 2006 University Press, Cambridge

reflectivity curve, especially the position of the SPR angle, is shown in Fig. 13.37a. The SPR angle depends strongly on the change in refractive index on the metal surface. As a result, the surface is often coated with a monolayer of active molecules and is used to study the mass absorbed on the surface, such as protein and DNA. The SPR angle shift as function of time can also be observed. Monitoring the angle shift in real time allows the study of the kinetics of molecular interactions on the surface at different conditions, for example during the injection of another chemical (Fig. 13.37b). This means that the association and dissociation of biomolecules can be observed, and the rate constants and equilibrium constants can be calculated.

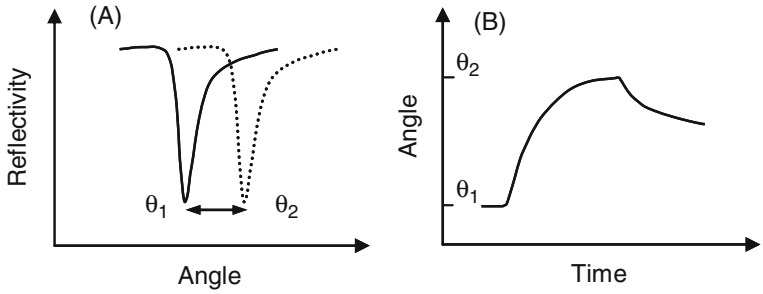

Fig. 13.37 (**a**) The SPR angle changes as the surface absorption changes; (**b**) the time-dependent SPR angle changes

As mentioned, the position of the reflectivity minimum is very sensitive to the properties of the liquid-metal interface surface, such as refractive index (down to 10^{-5}) and molecule absorption (up to a few hundred nanometers) [121, 123, 124]. No photons exit the reflecting surface, but the electric field decreases exponentially with distance from the interface, decaying over a distance of about a quarter of the light wavelength beyond the surface. In the case of gold and glass with a light wavelength of 633 nm, the SPP propagation decay length is calculated to be 9.98 μm in the *x*-direction, and in the z-direction, 27.6 nm into gold and 213.5 nm into glass. This illustrates the much shorter decay length in gold than in glass. The penetration depth of the evanescent field depends on the wavelength of the incident light. Factors such as metal film thickness, surface adsorbed species, and liquid dielectric properties can affect the SPR results. A background run is often performed as a baseline prior to the study of the mass change on the surface.

SPR offers several advantages. First, it is a label-free detection technique. Second, it is sensitive enough to distinguish surface interaction as opposed to bulk interaction. It can be used to study kinetics by monitoring molecular interactions in real time. Third, the detection is not affected by sample color. Lastly, many self-assembly monolayers (SAMs) can be coated on gold or silver for various interfacial interaction studies (see Section 13.4).

13.6.2 Material Properties and Process Selection Guidelines

In many Optical MEMS or BioMEMS applications, surface coatings are effective in creating new optical and chemical properties on the surface while retaining the mechanical and optical properties in the bulk. These surface condition modifications can be employed to manipulate light or to control bio and chemical/ and physical interactions in the devices. Surface properties are often the determining factors for the performance of a MEMS device. In terms of optical properties, many phenomena can be manipulated on the surface of the MEMS devices, such as light reflection, transmission, absorption, and polarization. These functional optical properties are directly related to the fabrication methods and processing conditions. To achieve the desired optical properties, many design and fabrication limitations must be considered thoroughly in advance, including the surface topography and roughness, material selection and compatibility, fabrication process, and integration associated interface issues. Therefore, this section will focus on methods for selecting and arranging optical thin films on a surface to provide the optical properties desired for MEMS applications.

13.6.2.1 High Reflection Applications

The control of surface reflection of light is one the most common uses of surface coatings. Two extremes of light reflection are often required, i.e. very high surface reflection (high reflection) and very low surface reflection (antireflection). High reflection is suitable for applications that require directional manipulation of light, while antireflection is necessary for the maximum light intensity to pass through the surface. Optical design considerations for these two extremes are relevant, and considerations for each case will be discussed in the next two sections.

To achieve a very high surface reflection rate, one can either choose a thin metal film or multi-layers of coating. For metal thin films, Equation (13.32) gives the reflectance R of a metal with good conductivity. Usually the values of n_{R} and n_{i} are close, but both are much smaller than n_I. As a result, an estimate of the reflectance is given by

$$R = \frac{(n_{\mathrm{R}} - n_{\mathrm{i}})^2 + n_{\mathrm{I}}^2}{(n_{\mathrm{R}} + n_{\mathrm{i}})^2 + n_{\mathrm{I}}^2} \approx \frac{1}{(2n_{\mathrm{R}}/n_{\mathrm{I}})^2 + 1} \approx 1 - 4(\frac{n_{\mathrm{R}}}{n_{\mathrm{I}}})^2 \tag{13.44}$$

If n_{R} is 20% of n_{I}, a reflectance of 0.84 can be easily achieved. For a metal with very good conductance, i.e. a very low $n_{\mathrm{R}}/n_{\mathrm{I}}$ ratio, the reflectance approaches 100%. For example, Al ($n_{\mathrm{R}}/n_{\mathrm{I}} = 1.3/7.11 = 0.183$ at 650 nm) and Ag ($n_{\mathrm{R}}/n_{\mathrm{I}} = 0.07/4.2 = 0.017$ at 650 nm) have very high reflectances of 90.5 and 98.8%, respectively, at 650 nm, and Au ($n_{\mathrm{R}}/n_{\mathrm{I}} = 0.142/3.74 = 0.042$ at 650 nm) has a reflectance of 99% in the infrared range (1500 nm). These metals have been coated on the surfaces of MEMS devices to obtain high reflection.

On the other hand, to enhance the reflection efficiency, multiple layers can be arranged together in a (glass)$(HL)^m$H(air) system [125]. The multiple layers form a high-reflectance central zone at ω_0, and the width of the central zone increases with the value of n_H/n_L. The maximum reflectance can be close to 1.0 with an additional H-layer on top of the periodical structures, as the shown in Fig. 13.38. As a result, mirror-like surfaces can be achieved with high reflectance in the visible spectrum via the proper arrangement of multilayer periodic systems.

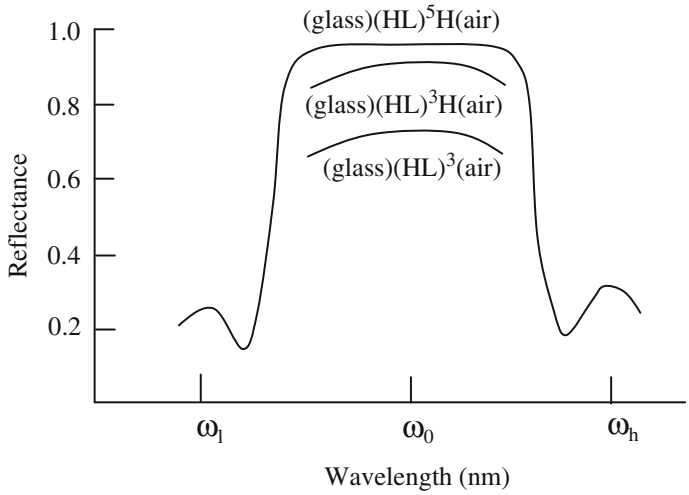

Fig. 13.38 Reflectance of multiple structures [125]. Reprinted with permission. Copyright 2008 Institute of Physics

Many MEMS mirror structures use Au on Si to reflect light. The reflectivity typically depends on the polarization. This is known as polarization dependent loss (PDL) for optical switch applications. One example [126] showed that s-polarized light (in transverse electromagnetic field) reflected more strongly than p-polarized light. To reduce the PDL, a multilayer dielectric coating on top of the gold mirror was used. A gold film, 60–100 nm thick, deposited over an underlying Ti or Cr adhesion layer about 10 nm in thickness, was used as the reflective surface. Both layers were deposited by thermal evaporation or sputtering. Finally, a multi-layer dielectric overcoat was deposited using an e-beam evaporator. This multi-layer coating contained 4 pairs of SiO_2/Ta_2O_3 thin film layers and had a total thickness of 2.037 μm. The PDL was reduced and the overall reflectivity was also improved with this multi-layer coating [126].

13.6.2.2 Antireflection Applications

Antireflection coatings have been widely used in optical MEMS for reflection reduction and increased transmission of light into the materials [127–133]. AR coatings

have a positive effect on energy efficiency (e.g. in solar cells), light transmission (in micro display panels), light accumulation (in micro IR detectors), and photon enrichment (in optical based bio-sensors) [127–133]. Many applications including micro lenses [133], micro mirrors [125, 131, 134], micro prisms [124, 130], and micro beam splitters [131, 134] have been reported. Antireflection coatings are also widely employed to maximize light transmission into the active regions of solar cell systems [135–147]; to lengthen polymer lifetime in outdoor applications such as UV protection [148]; to lower energy consumption, for example by using thermochromic glazings on building windows [149]; and to increase IR transmission in sensitive infrared spectrometers and radiometers [150].

In MEMS related optical systems, dielectric and polymer materials are both commonly used in optical components. However, the surface treatment methods for each type of material are distinct and must be considered carefully in the design phase. Principles of antireflection for two different surface treatment methods (multi-layer coatings and nano-structure fabrication) were described in Section 13.6.1.3.

Material Properties and Selection

For dielectric optical substrates, one of the most widely adopted methods for surface thin film coating is the vacuum coating process, including physical and chemical vapor deposition. Physical vapor deposition, especially sputtering, is the method employed most often for thin film coatings because it provides highly accurate thickness control (in the nanometer range), good film quality for both metal and dielectric materials, and conformal coatings on structures [109]. Vacuum coating processes for dielectric materials are mature processes and the process considerations are described in detail in Chapter 4 (Section 4.2).

The properties of several dielectric substrate materials, such as commercially available optical glasses and crystalline materials, are listed in Tables 13.5 and 13.6 as design references.

Case Study 6: Nanostructure on Surface for Antireflection (Moth Eye Effect)

In addition to thin film coatings, nanostructures fabricated on the substrate surface can also be used for antireflection. These structures are in the submicron range for visible light (wavelength ranging from about 400 nm to about 700 nm) and can create an effective index gradient from the substrate to the incident media [151]. The phenomenon of antireflection by sub-wavelength structures was first observed on moths' eyes for night vision [113], and has the advantage of low sensitivity to the variation of light incidence angle, a characteristic that would usually require a complex design for a multi-film system. In the visible spectrum, the structure sizes must be smaller than 300 nm and the total depth should be in the range of several hundred nms. Several methods have been developed for the fabrication of nanostructures on the substrate, including the interference of two coherent beams, holographic optical process [152], stochastic dry etching processes [153], hot embossing/casting on a nano mold [154, 155], rough PVD coating [156], nano phase separation [157–160],

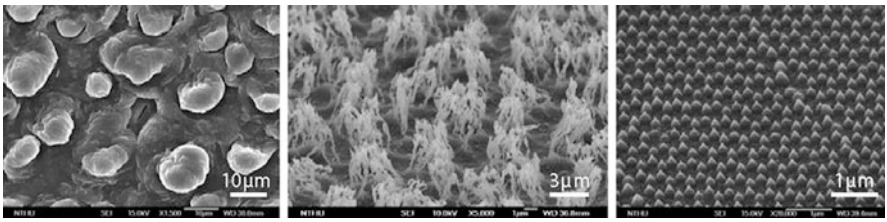

Fig. 13.39 Nano structures fabricated by different technologies (**a**) nano casted PDMS structures from Lotus leaf, (**b**) SU-8 nano fibers made with the Self-Masked High-Aspect-Ratio (SMHAR) process, and (**c**) self masked silicon oxide nano cones [155, 162]. Reprinted with permission. Copyright 2008 Institute of Physics

the use of self assembled nanostructures [157, 161], and self nano masking processes [162]. Some of the fabricated nanostructures are shown in Fig. 13.39 [155, 162].

The proposed mechanism of nanostructure formation in Fig. 13.39b is schematically depicted in Fig. 13.40 [162]. In conventional RIE etching (without a shielding cover glass), short nanopillars were produced due to the nonhomogeneity of the polymer material as prepared during the fabrication process. The aspect ratio of the nanopillars remained low (usually smaller than 5) even with increased etching time. This was because the etching rate at the top of the nanopillars was similar to that on the bottom surface in RIE. However, in the Self-Masked High-Aspect-Ratio (SMHAR) process [162], nanomasks were created from the cover glass and deposited onto a Parylene C surface to help with the formation/passivation of the HAR nanopillars. In the early stages of RIE etching in the SMHAR process, short nanopillars (seed structures) were generated, and a small number of nanomasks were produced simultaneously with no obvious passivation effect on the seed structures (Fig. 13.40b). As the etching progressed, a sufficient number of nanomasks were produced to accumulate on the seed structures, thereby extending the length of the seed structures and forming HAR nanopillars (Fig. 13.40c). This is preferred to the substrate shown in Fig. 13.40d, which might result from the higher surface curvature and thus, the higher charge density of the seed structures [162]. Nanomasks were found to reduce the etching rate in RIE for shielded nanopillars, as indicated by the slope difference. In addition, fluorocarbon was also generated in the RIE process, and it provided sidewall passivation. The bottom surface has a stronger etching rate than the sidewalls due to the direct physical ion bombardment during the RIE process. Therefore, multiple effects were incorporated to induce both top and sidewall surface passivation of the nanopillars. Consequently, the height of the nanopillars continually increased as the RIE process proceeded, as shown in Fig. 13.40c, d. The density distribution of nanopillars illustrated a gradient correlated with the distance from the cover glass [162].

Most of the processes are cost effective and easy to use for batch fabrication, and thus have high potential for commercial applications. However, the intrinsic problems with nanostructure-based AR surfaces are the relatively weak mechanical

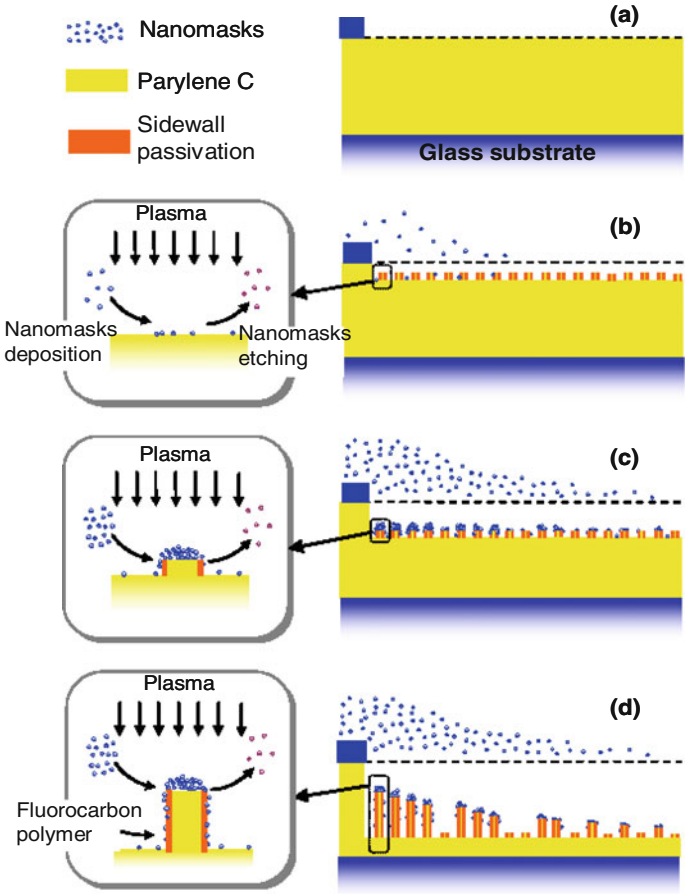

Fig. 13.40 The mechanism by which SMHAR nanopillars form [162]: (**a**) cover glass partially shields the Parylene C; (**b**) short nanopillars (seed structures) form initially, and only a small number of nanomasks are deposited; (**c**) more nanomasks are generated, and passivation masks form during the RIE etching process; (**d**) HAR nanopillars form in RIE; the tops and sidewalls are both protected by the deposited nanomasks. Reprinted with permission. Copyright 2008 Institute of Physics

properties of the film and the difficulty of surface cleaning. These must be further addressed before practical use is made.

The simplest one-dimensional AR nanostructure surface design is a binary structure, similar to an array of square rods extruded from the substrate surface, as illustrated in Fig. 13.41a. The analogous thin film coating is illustrated in Fig. 13.41b, with the effective index n_{eff} equal to the average index of the nanorod array in (a). The fraction factor of the rod array can be expressed as $f = b/P$, where b is the width and P is the period of the rod structure. From the Fresnel equation, for zero reflection from the film, the depths of the binary structures must satisfy:

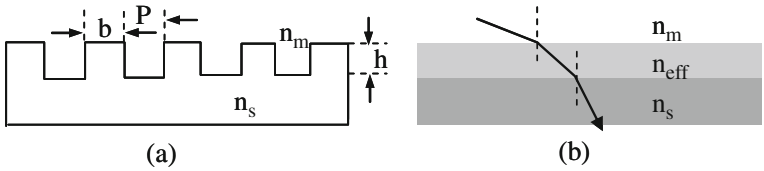

Fig. 13.41 (**a**) One dimensional binary AR surface (**b**) effective thin film coating on substrate, analogous to the binary surface

$$\mathrm{h} = \frac{\lambda}{4\sqrt{n_\mathrm{m} n_\mathrm{s}}} \tag{13.45}$$

where λ is the operation wavelength, and n_s and n_m are the indices of substrate and medium, respectively. The effective index n_{eff} also needs to satisfy the following condition:

$$n_\mathrm{eff} = \sqrt{n_\mathrm{m} n_\mathrm{s}} = n_\mathrm{s}\left(\frac{b}{P}\right) + n_\mathrm{m}\left(1 - \frac{b}{P}\right) \tag{13.46}$$

The nanostructures also need to satisfy the following conditions according to Equations (13.38) and (13.39):

$$\mathrm{P} \leq \frac{\lambda}{n_\mathrm{s}} \text{ and } 0.4\lambda_\mathrm{max} \leq h \leq \lambda_\mathrm{max}$$

For example, considering the design of AR nanorod structures on a glass substrate (index of 1.5) in air for green light at 530 nm, the required period P is:

$$\mathrm{P} \leq \frac{\lambda}{n_\mathrm{s}}\ 353\,\mathrm{nm} \quad \text{and} \quad 212\,\mathrm{nm} \leq h \leq 530\,\mathrm{nm} \tag{13.47}$$

Assuming that the maximum P (353 nm) is to be used for easier fabrication, the width of the square nanorod, b, is calculated to be about 159 nm and the height of the nanostructures, h, is about 108 nm. These calculations are based on very simple and perfect nanostructures. In a real process, the shape, size, roughness, aspect ratio, and distribution of the nanostructures all affect antireflection results. The estimated height may deviate from the range estimated by Equation (13.39) because of the very simple two-layer design. For more complex designs, see references [116–118] for more detailed calculations and simulations.

13.6.2.3 Considerations for Surface Smoothness and Roughness

When using microstructures for optical applications such as mirrors, prisms, or lenses, the surface roughness must be controlled sufficiently to meet at least one Rayleigh Limit (RL) for high optical performance. That is, the peak to valley optical

path difference (PV-OPD) of the wavefront reflected or diffracted from the optical component must be smaller than λ/4 [109]. As a result, the corresponding root mean square optical path difference (RMS-OPD) needs to be smaller than λ/14 [109]. For example, for a mirror in an integrated DVD pick up head in the blue ray region ($\lambda = 405$ nm), the RMS-OPD or surface roughness must be controlled to less than 29 nm. Therefore, surface smoothness is a key parameter for micro optical components.

Many methods for surface smoothing following microfabrication have been reported for optical applications, including spin coating [163–169], surface pressurization [170], thermal annealing [171, 172], ion-beam/RIE etching [173–176], and chemical mechanical polishing (CMP). The CMP process will be introduced in detail in Section 13.7.

Among these surface planarization processes, spin coating is one of the most commonly used methods due to its simplicity, low temperature, and effectiveness in surface planarization. Spin coating is often used for planarization of polymers [163, 164, 166–168] and spin on glasses [165]. For polymers, the control of spin speed, number of layers, material properties (viscosity, volatility, and shrinkage), and annealing conditions are important parameters. In general, low spin speed, low viscosity, low shrinkage, and non-volatile polymer content contribute to improved smoothness [163]. Annealing can induce reflow dominated by surface tension effects for the planarization of thermoplastic type polymers. The application of multiple layers can also improve the surface flatness [164, 166, 167]. Many polymer materials have been reported such as nonvolatile photopolymer Si-14 [163], PC403 photopolymer [164], photoresist ORDYL PR125 [166], polyimide [166], BCB polymeric resin [168], and polyimide-silica microcomposite films [169]; in those materials, the degree of planarization (DOP) has been shown to approach 95% [163], 75% [164], 99% (for deep trench) [116], and 80% [118], respectively. Here the DOP is defined as:

$$\mathrm{DOP} = 1 - \frac{S_\mathrm{p}}{S_0} \tag{13.48}$$

where S_0 and S_p represent the step height of the surface before and after planarization [163, 168]. The degree of planarization (DOP) for spin on glass approaches 99% for very thin photonic crystal structures 160 nm thick [165].

In addition to polymers, metal thin films can also be planarized by applying a high pressure to the metal film against a flat surface [170]. For example, a pressure of 600 MPa was applied to a 100 nm Ag film against a (100)-oriented silicon wafer [170] that had been polished on both sides to reduce the original 13 nm RMS roughness on the Ag film to less than 0.1 nm RMS. Bumps, asperities, rough grains and spikes in vacuum-deposited metal films can be thoroughly flattened.

As for semiconductor/dielectric materials, such as silicon [171] and sol-gel glass [172], thermal annealing is an effective surface smoothing technique. For example, in one study [171], a hydrogen atmosphere was introduced during a high temperature (1000–1100°C) annealing process, promoting silicon atom migration and thus

smoothing the surface [171]. The surface RMS roughness was reduced from 20 nm after dry etching to 0.26 nm following the annealing process [171]. Annealing can also be used to smooth the surface of a sol-gel glass structure; annealing at 1260°C for 10 min was found to effectively smooth the surface without much structural change [171]. As a result, very low scattering waveguide structures can be fabricated using the annealing processes [171, 172].

Although adding material and rearranging surface atoms are effective methods for surface planarization, removing material from the surface using etching is an alternative technique for surface roughness reduction. Etching is usually performed either by ion-beam etching [173, 174, 176] or by reactive ion etching (RIE) [175]. Small particles as large as 50 nm can be smoothed to 1 nm by in situ ion beam etching during thin film deposition [173]. The direction of the beam is also important for surface smoothness; smoothness can be attained either by using a grazing incident angle [176], or by rotating the sample to achieve a smaller incident angle [174]. Average surface roughness can be reduced from 40 to 10 nm [176] and from 2 into 0.2 nm [174], respectively. The latter is suitable for the smoothing of high precision lenses, extreme-ultraviolet lithography, and X-ray optics [174]. RIE processes have also been employed to smooth the surface of a CVD deposited diamond thin film. To increase the smoothing effectiveness, rapid thermal chemical vapor deposition (RTCVD) was used to deposit a thin film of SiO_2 onto the diamond film [175]. Surface roughness was reduced from 40 to 14 nm by the RIE process; the treated surface was suitable for X-ray lithography [175].

13.6.2.4 Polymer Materials for Optical Applications

Vacuum coatings on polymer materials are relatively new and have been developed for only about 20 years [177]. Since the use of polymer optical components in MEMS is becoming increasingly popular, this field will become more important in the future. Due to significant differences in physical and chemical properties between polymers and dielectric materials, special efforts are required to determine the proper substrate materials and process conditions for reliable surface coatings. For precision optical parts, transparent polymers such as poly-methylmethacrylate (PMMA) and biophenol-A polycarbonate (PC) have been the most commonly used substrates for more than 50 years [177]. Other polymers such as polyamides, polyether sulfones, and cycloolefin polymers have been developed more recently [177, 178]. These thermoplastic materials can be processed by injection molding, hot embossing, or dry etching. Photo patternable polymers such as photoresists and SU-8 have also been adopted for optical MEMS applications owing to their ease of patterning and reshaping for optical component fabrication [131–134]. The properties of some polymers used in optics are listed in Table 13.7.

13.6.2.5 Surface Coatings for Polymer Materials

Surface coatings can increase the performance of optical plastics for many applications such as antireflection, mechanical protection, chemical resistance, reduction

of gas permeability, antistatic, and surface wetting angle control [110, 179, 180]. Usually coatings used on optical plastics consist of an optical interface, protective layers, and outer surface layers [110]. The materials used for building up antireflection coating layers usually contain metal oxides. The most frequently used low index material is silicon dioxide ($n = 1.5$), while high index metal oxide materials range from alumina ($n = 1.67$) to titanium dioxide ($n = 2.4$). Selection of the coating material is critical to minimize unwanted effects such as heat or ultraviolet light emission during the evaporation/sputtering processes, which can cause thermal stresses and optical property changes.

Two technologies are often used in the preparation of thin film coatings on plastic materials: vacuum coatings and wet-chemical coatings. A low temperature process (<120°C) is required for vacuum coating of most thermoplastics [110]. However, low temperature processes usually produce thin film coatings with undensified porous structures, which can cause adhesion problems on the substrate. As a result, the optical properties of the thin film are not stable when the coating is exposed to moisture in the atmosphere [110]. To solve this problem, plasma ion-assisted deposition (plasma-IAD, in Fig. 13.42) was developed to bombard the substrate with ions during thin film deposition [110, 181, 182]. An ion source used in one study [177] was a low pressure plasma source with an ion energy level ranging from 70 to 150 eV. The material properties of the thin film, including surface energy, adhesion, refractive index, hardness, and surface topography, can be varied by adjusting the surface ion bombardment [110, 183].

Other processing methods for vacuum coatings include plasma-impulsed chemical vapor deposition (PICVD) and plasma enhanced chemical vapor deposition

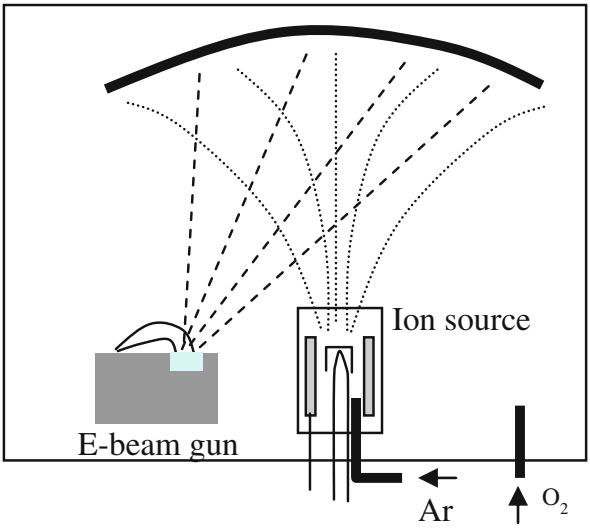

Fig. 13.42 Schematic setup of Plasma-IAD [110]. Reprinted with permission. Copyright 2006 Optical Society of America

(PECVD) [110, 184]. The gaseous precursor is decomposed using either a pulsed microwave or a radio-frequency plasma; the reaction and deposition can then take place at the surface [185, 186]. These processes can provide a partially-organic coating with a hardness and elasticity gradient [187], thus improving adhesion and reducing stress.

Although very popular for thin film coatings on dielectric materials, sputtering is not preferred for direct thin film deposition on plastic materials because of the high emissions of heat and UV radiation during the process. As a result, a protective layer such as lacquer or a PECVD thin protection film is usually required prior to sputtering [188, 189].

Process Considerations for Vacuum Coatings

There are several intrinsic issues related to vacuum coatings on polymer materials, including plasma/polymer interactions, types of polymer chosen, stresses in the coatings, and testing methods [110].

As for the interactions between plasma and polymer, the basic problem comes from high-energy ions, radicals, and short-wavelength radiation produced by plasma ion sources, glow-discharge equipment, and electron beam evaporation. These high-energy sources can break the chemical bonds in polymers and cause chemical and/or physical modifications. On the other hand, the advantage of bond-breaking is that it can increase the interaction forces between the substrate and the coating film via crosslinking, interfacial diffusion, or changes in surface wettability, thus improving the adhesion [190, 191]. Additionally, polar groups formed on the polymer surface can reduce the surface hydrophobicity of the polymer [110, 192], which is beneficial for moving liquids in microfluidic systems due to the high surface tension [193–195]. However, the wettability of the polymer surfaces is not permanent, i.e., the wetting property disappears completely in an atmospheric environment over a couple of months. This can be attributed to the orientation rearrangement of surface polar groups and/or the recovery of polymer non-polar groups in a non-polar environment such as atmosphere [191]. Hence, if the plasma treatment is not performed properly, small fractures will form on the bulk substrate and thus produce a weak boundary layer between the substrate and the thin film. Therefore, shortening the plasma treatment time or using a pulse treatment is necessary to minimize this issue [110].

Aside from plasma/polymer interactions, material specific properties including heat distortion, thermal expansion, UV absorption, and degassing, may cause problems in thin film coatings. Oxide layers deposited using plasma-ion-assisted electron-beam evaporation (PIA E-beam) can exhibit excellent adhesion on polycycloolefins, polyamides, and polyether sulfones [196]. On the other hand, PMMA usually forms a weak adhesive layer because it degrades after contacting plasma [197]. Therefore, deposition of a vacuum UV protective layer prior to the plasma coating process is required to protect the surface from degradation [151].

In some cases, stresses induced during the deposition process, in the coating or at the interface between thin film and substrate, may cause cracking or delamination of the coatings. Two major sources of this type of defect are related to stress build-up. One is from the ion-bombardment on the substrate surface, which usually causes compressive stresses in coatings [151]. The other is the thermal stress resulting from the coefficient of thermal expansion mismatch between the coating and the polymer substrate [151]. The thermal expansion coefficient of polymers is usually an order of magnitude higher than that of metal oxides. For example, if a high-index oxide is deposited onto a polymer surface, high temperature conditions are often encountered during the fabrication process, either in e-beam evaporation or in sputtering systems. Therefore, fabrication parameters such as temperature, process time, and thin film thickness must be well controlled and characterized to achieve successful coatings.

Process Considerations for Wet Chemical Coatings

In addition to the deposition of inorganic materials onto polymers using the vacuum coating technique, polymers can also be deposited onto polymer substrates as antireflection layers using wet processes. Two common processes, dip coating and spin coating, are primarily adopted for the deposition of low aspect ratio micro-scale structures over rigid flat substrates. However, for complex or high aspect ratio microstructures, spraying processes are more suitable for providing uniform coatings. In the wet coating process for polymer thin films, it is important to limit both curing temperature and the number of radiation-induced cross-linking reactions to protect the substrate surface. Wet coatings applied to polymers for antireflective purposes are generally restricted to one or two layers because of the increasing difficulty of thickness control for multilayer thin films. Several systems have been developed for wet coating processes, including silicate-based inorganic-organic hybrid polymers [198], sol-gel alkoxide polymeric materials, and colloidal indium tin oxide [151]. Silicate-based inorganic-organic hybrid polymers contain organic components that can covalently bond to the polymer substrate as well as to the inorganic network. Thus they offer both the desired optical properties and enhanced mechanical properties [198]. Sol-gel alkoxide polymer and colloidal indium tin oxide usually require several cycles of deposition and hardening, making precise control of thickness very difficult. In order to obtain good quality and precisely controlled thickness films in the nanometer range, the sol-gel process requires a controlled environment such as a clean room with well-controlled temperature and humidity. Some successful applications of wet coating polymers have been commercialized as AR coatings on PMMA by Nagase & Co. Ltd. and YTC America Inc.

Case Study 7: Surface Coatings for Interferometry Biosensors

To illustrate the optical utility of thin film coatings, here we give an example in which a thin film coating was used as an interferometer for bio-sensing applications.

To enhance the interference signal for an immune sensing fiber, the tip of the optical fiber was coated with thin metal films as well as gold nano particles (GNP) to increase the optical path for detection (Gold NanoParticle enhanced Fiber Optic Interferometry, GNPFOI, sensor) [199, 200]. The light source was generated by a broadband edge-emitting light emitting diode (ELED, PD-LD Inc., USA) driven by a current controller (LDC210, Profile Optische System, Germany) with a peak wavelength of 1550 nm, a spectrum half-width of 70 nm, and an emission power of 15 μW. The light emitted from the ELED was transmitted by a single mode optical fiber (FS-SC-7324, 3MTM, USA) with a 125 μm fiber and 8 μm core diameter, respectively, and directed into the immune-sensing probe to carry the interferometry signal through the coupling of the splice. A three-port optical circulator (FOCI, Taiwan) was used to guide interfered light to an optical spectrum analyzer (MS9710C, Anritsu, Japan) to record and analyze the interference spectrum.

The interference immune sensing probe was mainly composed of a resonant cavity of transparent polymer, and two thin reflective layers of gold (Fig. 13.43a). To prepare the probe, first a cleaved fiber was cleaned with a 95% alcohol solution in an ultrasound bath. A 3 nm gold film was then deposited on the tip surface by e-beam evaporation. The interfering resonant cavity was formed by dip-coating the probe with a 30 μm thick layer of polydimethylsiloxane (PDMS, Sylgard 184, Dow

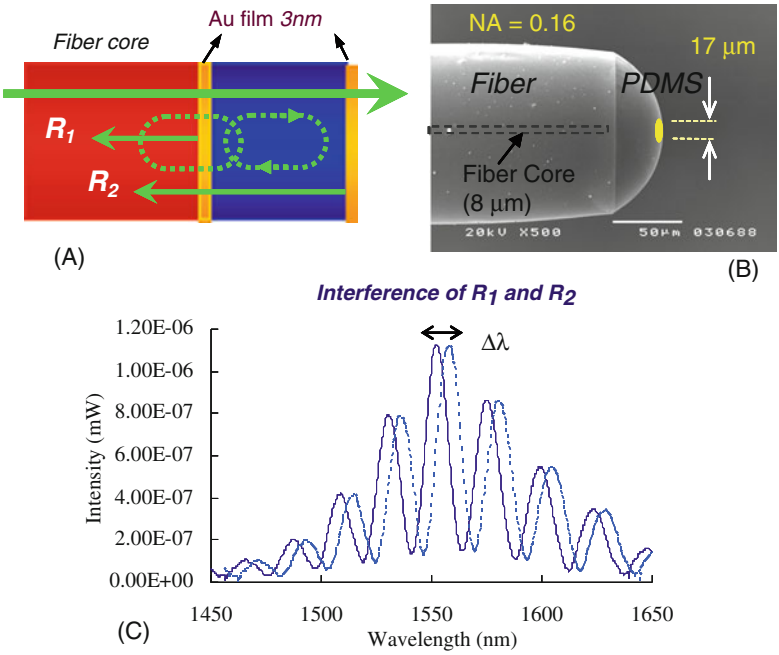

Fig. 13.43 (**a**) Operating principle of the interference sensor on a fiber tip; (**b**) SEM side view of this sensor with 125 μm outer diameter and 8 μm core; (**c**) interference spectrum of the fiber sensor [199]. Reprinted with permission. Copyright 2009 Institute of Physics

Corning Corp., USA) and curing the probe at 90°C for 10 min. A second gold film, 3 nm thick, was deposited onto the PDMS surface to serve as a second reflection surface and as the interface for bio-molecule immobilization. This film actually consisted of gold islands (20–30 nm wide and 4–5 nm high) on the surface. These spreading islands made the gold thin film partially transparent to electromagnetic waves. Finally, the completed probe was annealed at 200°C for 2 h to enhance the adhesion between the gold film and PDMS layer.

The appearance of the resonant cavity is shown in the SEM image of Fig. 13.43b. The sensing area can be considered to be a flat plane due to the very small incident spot on the outermost surface (17 μm in diameter) compared to the fiber diameter of 125 μm.

Immunological detection was conducted by immobilizing rabbit IgG on the thiol self-assembly-monolayers (SAMs) surface as the antigen, to conjugate with anti-rabbit IgG-Cy3 modified with 13 nm GNPs (Taiwan Advance Nanotech Inc., Taiwan). The anti-rabbit IgG-coated GNPs were used to demonstrate the effects of signal enhancement on immune sensing. In this experiment, the stable interference signal in PBS solution was first recorded as a reference for the binding signal. After obtaining a baseline in PBS buffer, a 17 nM anti-rabbit IgG-coated GNPs solution was introduced and an interference fringe shift was observed (Fig. 13.43c).

As shown in Fig. 13.43a, there are two partially transparent gold films with reflections R_1 and R_2, respectively, on each interface. The films are separated by a cavity with length L_0 and refractive index n_0. As the light (I_0) passes through the m_1 film, light is partially reflected as R_1 and the transmitted light T_1 going through the resonant cavity is partially reflected back as R_2 by the m_2 film. The phase difference (ϕ) between the two reflections R_1 and R_2 yields the interference R, which can be estimated from the reflection coefficients r_1 and r_2 [199]:

$$R = \frac{(r_1^2 + 2r_1 r_2 \cos\varphi + r_2^2)}{(1 + 2r_1 r_2 \cos\varphi + r_1^2 r_2^2)} \text{ and } R_1 = r_1^2 = \left(\frac{n_0 - n_1}{n_0 + n_1}\right)^2; R_2 = r_2^2 = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \tag{13.49}$$

where the magnitude of R represents the interfering reflectance from the wave coupling of R_1 and R_2. The phase difference φ can be expressed as:

$$\varphi = \frac{4\pi n_0 L_D 0}{\lambda} \tag{13.50}$$

where λ is the wavelength of the incident light. After inserting values for the parameters, such as $\lambda = 1550$ nm, $L_0 = 30\,\mu$m, $n_0 = 1.45$, $n_{\text{bio}} = 1.44$, $n_{\text{GNPs}} = 2.56$, and $L_{\text{bio}} = 1$ nm for thiol self-assembly-monolayers (SAMs) and a cysteine molecule layer, Equation (13.50) can be rewritten as follows [199]:

$$\Delta\lambda = 0.0513 + 0.0912 \cdot k \cdot D_{GNP} \cdot N \tag{13.51}$$

where D_{GNP} is the diameter of the GNPs, N is the binding number of GNPs, and k is a constant. An empirical equation of the interference fringe shift can be obtained to

show the linear relationship between the diameters of GNPs (D_{GNP}) and the binding number of GNPs (N). This linear relationship, which was further verified by experiments [199], shows that with GNPs on the sensor surface, the signal can be enhanced by at least two orders of magnitude, depending on the size of GNP applied [199, 200].

13.6.2.6 Applications for Light Absorption

The property of light absorption can play a very important role in optical components, especially in photo patterning applications. Unlike antireflection coatings, which are on top of the surface, light absorption thin films or structures are typically applied beneath the photo-patternable films. The purpose of these layers is to prevent light reflection at the bottom surface, minimizing structure defects. Two case studies in this section will illustrate the design and fabrication of light absorption layers. The first case study is a light absorption coating for embedded fluidic channels [201, 202]. The second case study discusses the production of inclined structures without defects using light reflection [125, 131].

Case Study 8: Light Absorption Layer for Microfluidic Channels

In embedded micro channel formation, we typically want to take advantage of the dosage gradient of UV light along the vertical direction of the photoresist. When the top part of the negative photoresist receives adequate exposure dosage while the bottom part does not, an embedded micro channel can form after the bottom portion of the photoresist has developed. However, the reflection of light from the very flat and smooth surface underneath the photoresist imposes greater exposure on the bottom portion and thus prevents the partial exposure process from creating embedded micro channels, as shown in Fig. 13.44a. As a result, channel height is very hard to control by partial exposure in the presence of reflection from the underlying substrate. The process window for channel formation is very narrow and hard to reproduce. An antireflection layer on the photoresist-wafer interface can be used to absorb reflected UV light, as shown in Fig. 13.44b. The antireflection layer absorbs excess UV energy, allowing the exposure window to become much wider and enabling accurate control of exposure depth.

Fabrication starts with spin coating of SU-8 resist on top of the FujiFilm CK-6020L resist, the antireflection coating commonly used as a filter for UV light. After the first exposure, which defines the through hole, a partial second exposure is applied to define the channel top region. Multilayer channel structures can be obtained simply by repeating the processes. It is noted that the antireflection layers must be removed with solvents during the developing process to open up paths for the lower channels to develop. This simple process has been routinely employed to fabricate channels with accurate top wall thickness and channel structures [201]. Figure 13.45 shows four different channel top-wall thicknesses of 14, 23.2, 27.2, and 31 μm, which were exposed to UV light (365 nm) for 122.5, 161.7, 176.4, and 191.1 mJ/cm^2, respectively.

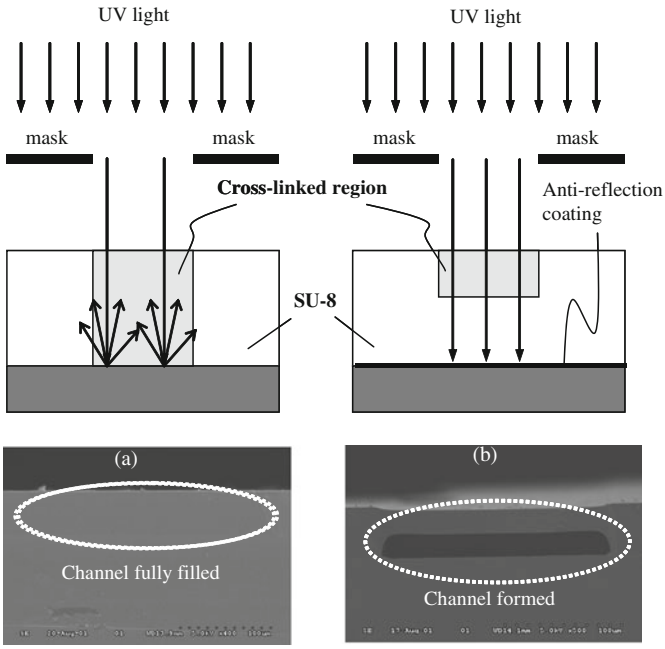

Fig. 13.44 UV exposure under (**a**) normal situation with reflection off the substrate; (**b**) with anti-reflection coating [201]. Reprinted with permission. Copyright 2003 Elsevier Science

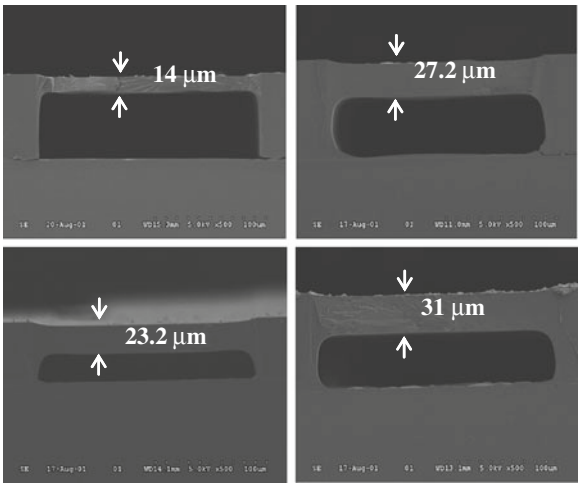

Fig. 13.45 Fabrication process of thickness control by different UV dosage [201]. Reprinted with permission. Copyright 2003 Elsevier Science

Case Study 9: Inclined Structures with Light Absorption Layers

Inclined exposure technology [125, 131] can be used to fabricate optical microstructures using several-millimeter-thick polymer layers on glass substrates. A film

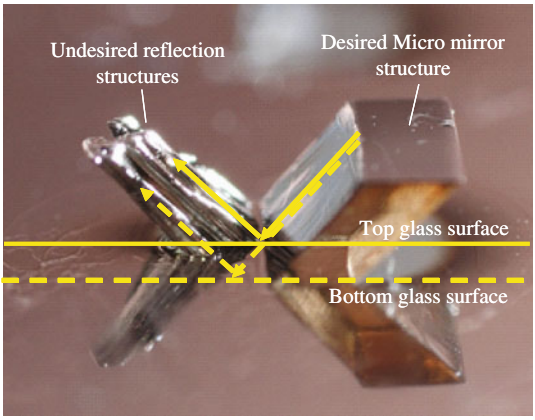

Fig. 13.46 Irregular reflection structures of an inclined SU-8 micro mirror generated from multiple reflection surfaces (1.4 mm thick) [125]. Reprinted with permission. Copyright 2008 Institute of Physics

(e.g. SU-8) with a thickness of 1.4 mm requires an exposure energy of about 14,000 mJ/cm^2. Reflection of such high energy light at the film/substrate interface causes unwanted exposure and partial photopolymerization in the reflective direction, resulting in undesirable V-shaped structures inside the thick SU-8 films, as shown in Fig. 13.46. The reflection effect at each interface is calculated using Fresnel equations. An absorption layer can be applied to absorb the undesired reflection to eliminate this problem.

The transmitted and reflected optical energy at each interface in accordance with the layer order and refractive indices are shown in Fig. 13.47, where $E_0 r_{21}$ is the reflected lightwave energy at the interface of n1 and n2, and $E_0 t_{21}$ is the transmitted lightwave energy at the interface of n1 and n2. Because irregularities on the SU-8 photoresist surface can cause an air gap to form between mask and photoresist, an inclined exposure will lead to a strong reflection at the air/SU-8 interface [125, 131]. As a result, glycerol was employed to compensate for the index mismatch between the mask and SU-8 resist [131]. To allow for a large incident angle for 45° mirror fabrication, the whole setup was also immersed in a glycerol container to compensate for the refraction effect [131].

The Fresnel equations that describe the reflection and transmission of electromagnetic waves at an interface were derived in Equations (13.22) to (13.28). The results of these calculations are shown in Table 13.8 [125]. It can be seen from the results in Table 13.8 that the most severe reflection occurred at the Glycerol/SU-8 (n2'/n3) and SU-8 photoresist/glass (n3/n4) interfaces. Energy reflection between the glycerol/SU-8 interface reduces the exposure of SU-8, but does not affect the structure shape.

As shown in Table 13.8, although the total reflection at the glycerol/SU-8 interface has been eliminated, there is not much improvement at the SU-8/glass substrate interface – as much as 2.15 and 1.49% of the perpendicular component of incident light energy are reflected at the SU-8/glycerol interface and SU-8/glass substrate interface, respectively. Since the reflection at the glass mask/SU-8 interface does not

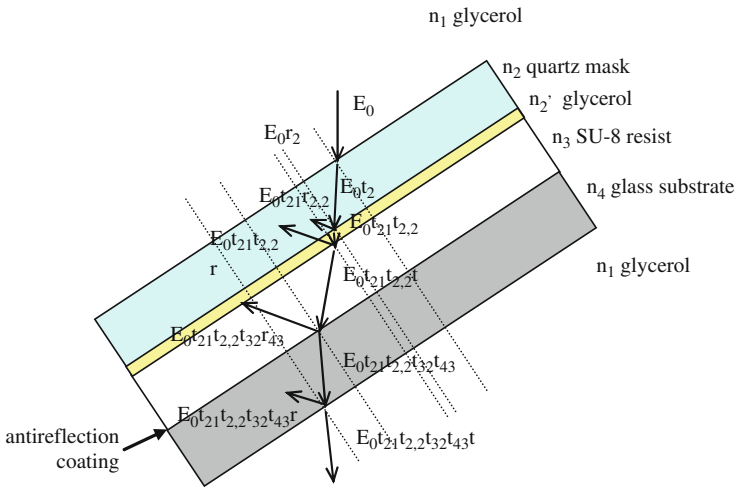

Fig. 13.47 Schematic light paths of UV exposure on SU-8 thick resist supported by a glass substrate through a contact quartz mask inside an index matching medium with or without a removable anti-reflection layer (between the n3 and n4 layers) [125]. Reprinted with permission. Copyright 2008 Institute of Physics

Table 13.8 Reflectance and transmittance on each interface layer for Fig. 13.47. The parameters are defined and calculated in Equations (13.22), (13.23), (13.24), (13.25), (13.26), (13.27), and (13.28)

Interface	θ_i	θ_t	$R_\parallel$ (%)	$T_\parallel$ (%)	$R_\perp$ (%)	$T_\perp$ (%)
n1/n2	53.45	50.66	0.015	99.985	0.252	99.748
n2/n2′	50.66	53.45	0.015	99.985	0.252	99.748
n2′/n3	53.45	45.12	0.049	99.951	2.147	97.853
n3/n4	45.12	52.08	0.024	99.976	1.492	98.508
n4/n1	52.08	53.45	0.004	99.996	0.062	99.938

n1: glycerol refractive index 1.473 at 598 nm, n2: quartz mask index 1.53, n2′: glycerol refractive index 1.473 at 598 nm, n3: SU-8 refractive index 1.67 at 365 nm, n4: glass substrate index 1.5 [125]
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affect the SU-8 structure, the reflection at the SU-8/glass substrate interface should be eliminated. Therefore, a removable anti-reflective layer (optical absorption layer, as shown in Fig. 13.47) is employed to absorb reflected light at the SU-8/glass substrate interface (between n3 and n4). Once the SU-8 has developed, the antireflection layer in the open area can be removed with solvents.

After applying an antireflection layer at the interface between the SU-8 resist and the glass substrate, as shown in Fig. 13.47, the reflection of light was almost completely eliminated, and clean SU-8 dove prisms were obtained, as illustrated in Fig. 13.48. The slanted surface on the SU-8 structures was very smooth and flat,

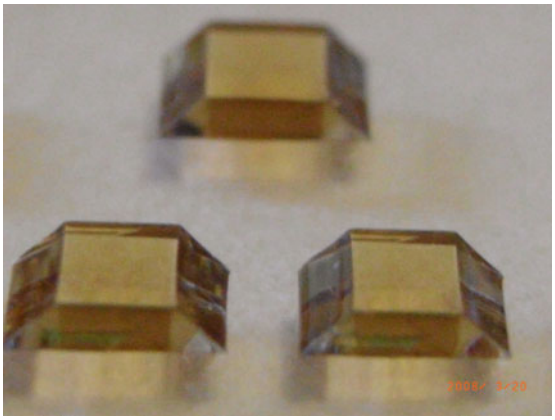

Fig. 13.48 Optical micrograph of SU-8 dove prisms fabricated in a batch. The size of the prism is approximately 3 nm (l) × 2 mm (w) × 0.5 mm (t). The surface roughness as determined by the WYKO is approximately 20 nm [125]. Reprinted with permission. Copyright 2008 Institute of Physics

with less than 20 nm variation in flatness over a 100 μm length, and less than 20 nm in average roughness, making it suitable for optical applications.

13.7 Chemical Mechanical Planarization

13.7.1 Overview

Chemical Mechanical Planarization (CMP) has been successful as an enabling technology in integrated circuit (IC) manufacturing, particularly when the minimum feature size is much below 0.5 μm, in which case the ultra smooth surface is required to match the sharply reduced depth of focus in photolithography. Outside of the IC industry, CMP also has important applications in the fabrication of microelectromechanical systems (MEMS) such as sensors, actuators, R/W heads for hard drive disks, and inkjet print heads. CMP was first used to planarize interlayer dielectrics in microelectronics manufacturing in the 1980s. Later, the technology was adapted for the manufacture of more complicated structures, such as damascene for copper metallization. Owing to its excellent performance, CMP is now widely used for planarization in a variety of materials including polymers, metals, dielectrics, and ceramics.

13.7.1.1 Chemistry of CMP

CMP applications can be generally classified into two categories: metal CMP and non-metal CMP. In this section, we will demonstrate the role of chemistry in silicon dioxide and copper CMP, as representative of these two main categories.

Oxide polishing techniques have been studied in the field of optical glass for more than 40 years (see Holland [203] or Izumitani [204] for a review of major developments). Izumitani examined glasses of various hardnesses and chemical durabilities that were polished with different media, and found that oxide polishing

occurs as a combination of mechanical abrasion and chemical reactions. Izumitani also proved that water is important in the oxide polishing process, a finding that was confirmed by others [205, 206]. Cook [205] suggested that during oxide polishing, loads imposed by abrasive particles enable water to enter the oxide network via the general reaction:

$$\text{Si - O - Si} + H_2O \leftrightarrow \text{Si - OH} \tag{13.52}$$

During the polishing process, hydration of the oxide softens the surface; the softened layer can be easily removed by mechanical abrasion. Hydration of all four Si-O bonds on a given silicon atom produces $Si(OH)_4$, which is highly soluble in water at high pH (>10). Thus, hydration causes dissolution of the network on the surface.

Among abrasives commonly used in glass polishing (such as TiO_2, ZrO_2, Cr_2O_3, Al_2O_3, SiO_2, and others), ceria (CeO_2) has the fastest polishing rate [205]. Tetssuya and co-workers [207] studied the polishing mechanism in SiO_2 by CeO_2 particles. The proposed model is illustrated by Fig. 13.49. First, chemical tooth bonds are formed between the CeO_2 particles and the SiO_2 film. Then, the CeO_2 particle with attached SiO_2 lump is removed from the SiO_2 film. The Ce-O-Si bonding and the cleaving of Si-O-Si bonds are believed to be the polishing rate-limiting steps. In this process, mechanical tearing has a significant effect on the cleaving of Si-O-Si bonds.

Metal CMP requires a more complex chemical system to maintain stable material removal and planarization. It is generally understood that metal slurries chemically modify the surface to be polished, yielding a softer, porous complex layer. This layer is easily removed through the application of mechanical force in the contact region. Meanwhile, the protection imparted on the recess region is sufficient to prevent dissolution. The combination of these effects results in planarization of the surface. Typical metal CMP slurries contain an oxidant, a chelating agent, a passivation agent, abrasive particles, and a surfactant or other chemical additives. Various models have been proposed for the chemical reaction in metal CMP. Steigerwald

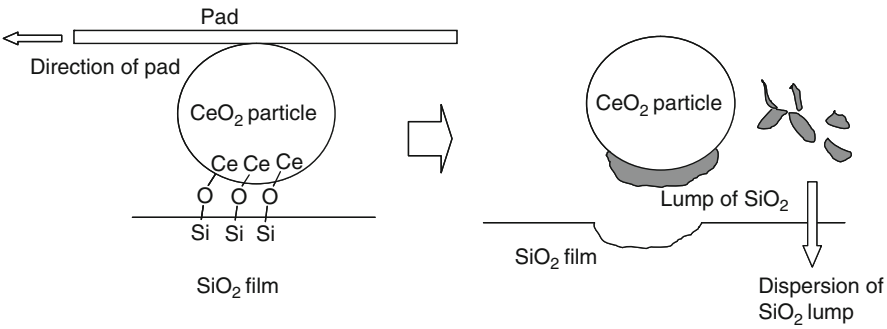

Fig. 13.49 The polishing mechanism in SiO_2 by CeO_2 particles. Reprinted with permission from [207] Reprinted with permission. Copyright 2001 Elsevier

[208] investigated copper CMP in alkaline conditions and proposed that successful copper CMP slurry should ensure that all materials dislodged from the copper surface are dissolved, to avoid the re-deposition of copper oxide particulates. Re-deposition significantly reduces the effectiveness of mechanical abrasion and thus lowers the material removal rate. Seal [209] and Park [210] studied the effect of H_2O_2 on the copper CMP process in acidic conditions. The results demonstrated that slurry chemistry can change the polishing mechanism in CMP. More specifically, at low H_2O_2 concentrations, the copper removal is strongly dissolution-dependent. At higher H_2O_2 concentrations, a protective oxide film rapidly forms on the copper surface and prevents heavy dissolution. In this case, the process is controlled by mechanical removal of copper and subsequent dissolution. At intermediate concentrations of H_2O_2, both polishing mechanisms coexist and compete. Kikkawa [211] studied the effect of slurry chemistry on mechanical abrasion during copper CMP with the *in situ* frictional force measurement technique. Slurry chemistry was found to strongly affect the formation of a passivation film on the copper surface and thus change the friction force of the surface.

13.7.1.2 Mechanics of CMP

During the CMP process, the wafer, pad, and slurry constitute a classical tribological system, normally regarded as a three-body interface with two solids in relative motion and slurry at the interfaces [212, 213]. The Preston Equation is the most frequently referenced expression for polishing rate in CMP [214, 215]. The equation states:

$$R = \mathrm{KPV} \tag{13.53}$$

where R is the removal rate, P is the pressure, V is the linear velocity of the pad relative to the workpiece, and K is the Preston coefficient. According to Equation (13.53), polishing rate is directly proportional to both the velocity of the pad and the pressure. However, this equation does not agree with experimental results when the velocity and/or pressure approaches zero. In order to account for this phenomenon, Steigerwald et al. [208] proposed the following modified Preston Equation:

$$\mathrm{P} = (\mathrm{K\,P} + \mathrm{B})V + R_{\mathrm{C}} \tag{13.54}$$

where B is a proportionality constant and R_c is the chemical removal rate.

The correlation between polishing conditions and polishing results is widely studied. Figures 13.50–13.53 show results from several representative studies for silicon dioxide, tungsten, and copper polishing.

In oxide polishing (Fig. 13.50), water reacts with the wafer surface and converts some Si-O-Si molecules to Si-OH. The hydrated sites are softer than the original surface [216]. Figure 13.50 shows the variation in normalized material removal rate with respect to the diffusion coefficient of water and the applied pressure. When using a high diffusion coefficient, a higher material removal rate

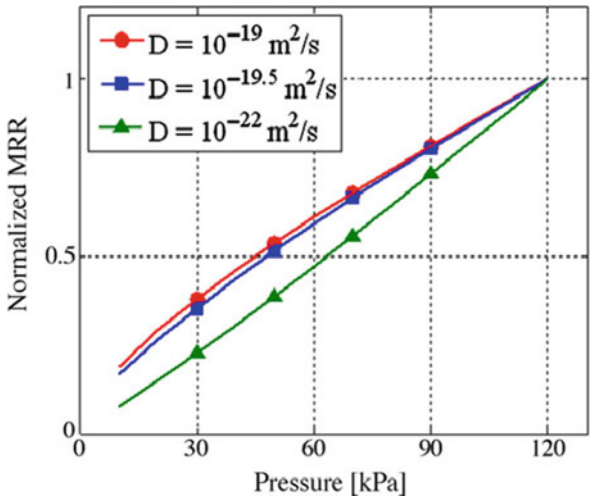

Fig. 13.50 Normalized oxide polishing rate vs. polishing pressure for slurries of various diffusion coefficients [216]. Reprinted with permission. Copyright 2009 Elsevier

was achieved, as the soft hydrated layer formed faster than it could be removed. Under these conditions, the change in material removal rate with respect to applied pressure gradually decreased with increasing pressure. In the low diffusion coefficient regime, lower material removal rates were observed. In this case, the material removal rate depended primarily on the mechanical action of the abrasive particles, resulting in near-Prestonian behavior. Figure 13.51 shows contours of the polishing rate and process temperature for IC-1400 pads (top) and Politex pads (bottom) in tungsten CMP. Polishing rate and process temperature increased with applied pressure and table rotation rate.

Figures 13.52 and 13.53 demonstrate the dependency of polishing rate on table speed and applied pressure in copper CMP. While the linear behavior is consistent with the Preston Equation (13.53), close inspection of the curves reveals that the Preston Equation is not applicable. The removal rate has a non-zero intercept at both zero rotation rate and zero pressure. The modified Preston Equation (13.54) accounts for these results.

Table 13.9 shows several examples of polishing condition setups for materials used in MEMS fabrication. The platen speed refers to the table or pad speed, whereas the carrier speed is the wafer rotation speed.

The Stribeck curve (Fig. 13.54) was developed to monitor tribological processes [219]. The Sommerfeld number (S_f) is defined as

$$S_f = \frac{\mu U}{p\delta_{eff}} \tag{13.55}$$

where μ is the viscosity of the lubricant, U is the relative velocity, p is the applied pressure, and δ_{eff} is the effective lubricant film thickness.

In the three-body interface system, i.e., the wafer-slurry-pad system, the solid bodies may interact in three lubrication regimes, as shown in Fig. 13.54: (1)

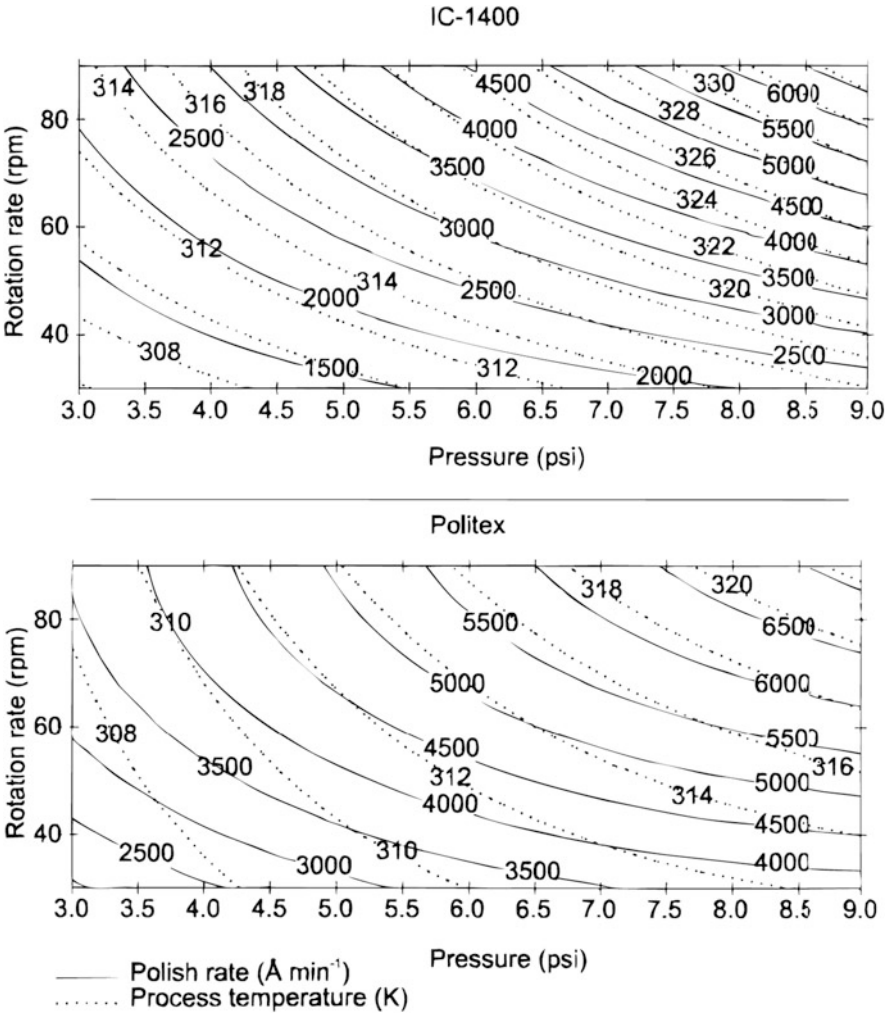

Fig. 13.51 Material removal rate and process temperature for tungsten polishing with commercial slurries [217]. Reprinted with permission. Copyright 1999 ECS

boundary lubrication (solid-solid contact), (2) partial lubrication (semi-direct contact), or (3) hydrodynamic lubrication (hydroplanes interacting with each other). In boundary lubrication, the wafer and pad are involved in solid-solid interaction, and the material removal rate is determined by surface abrasion only. In this regime, the transport of slurry under the wafer is poor, resulting in limited chemical activity. Also, the elevated temperature and aggressive abrasion of pad and particles can cause severe surface damage on the polished substrate. In the mixed (or partial) lubrication regime, a thin slurry film partially supports the applied pressure, preventing aggressive abrasion of the polished surface. The thin slurry layer is beneficial

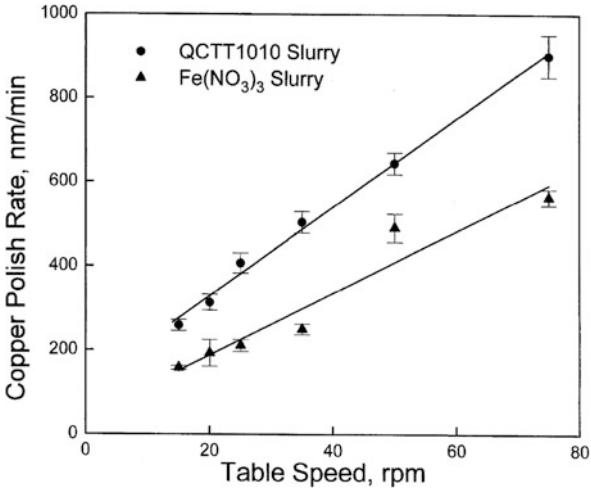

Fig. 13.52 Effect of table speed on copper polishing rate with QCTT1010 commercial slurry and $Fe(NO_3)_3$ slurry. Polisher settings: 0 in. oscillation, 210 ml/min slurry flow rate, SUBA IV pad and 30 KN/m^2 downward pressure [218]. Reprinted with permission. Copyright 1998 Elsevier

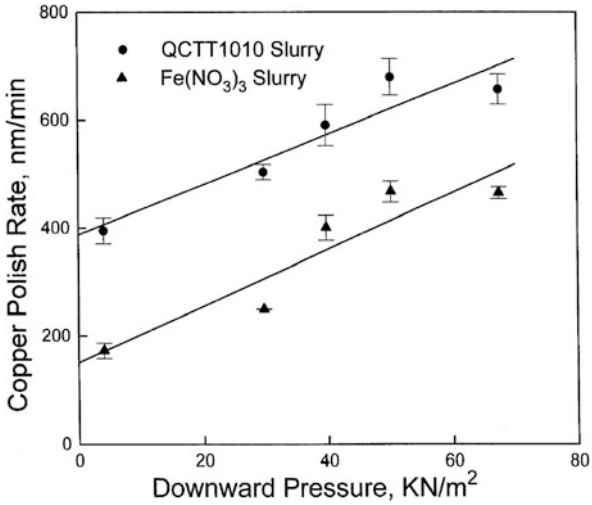

Fig. 13.53 Effect of applied pressure on copper polishing rate using QCTT1010 commercial slurry and $Fe(NO_3)_3$ slurry. Polisher settings: 0 in. oscillation, 210 ml/min slurry flow rate, SUBA IV pad and 35 rpm of the table. $Fe(NO_3)_3$ slurry: 0.005 M BTA, 0.1 M $Fe(NO_3)_3$, pH 1.35, 100 nm α-alumina particles [218]. Reprinted with permission. Copyright 1998 Elsevier

for two reasons. First, it acts as lubricating agent and conducts heat away from the surface; second, slurry transport is more efficient when such a fluid layer exists. In the hydrodynamic (hydroplaning) regime, the applied load is completely supported by a thick slurry layer at the interface. This layer may significantly reduce the material removal rate due to the low coefficient of friction. Philipossan et al. [220] investigated the effect of surfactant, abrasive size, abrasive content, wafer pressure, and sliding velocity on the frictional and kinetic attributes of copper CMP. It was shown that although abrasive content did not affect the tribological mechanism of the process, abrasive size was a significant factor. Surfactant-containing slurries dramatically reduced the coefficient of friction. Wang et al. [221] studied the effect of

Table 13.9 Examples of CMP settings for different materials on 200 mm wafer

Material	Platen speed (rpm)	Carrier speed (rpm)	Down pressure (psi)	Slurry flow (ml/min)
SiO2	95	87	3–5	200
W	75	70	4–7	200
Cu	85	75	1.5–2	200
Ta, TaN	100	100	1.5–2	200
Poly Si	50	50	2	200
NiFe	80	70	4–8	200

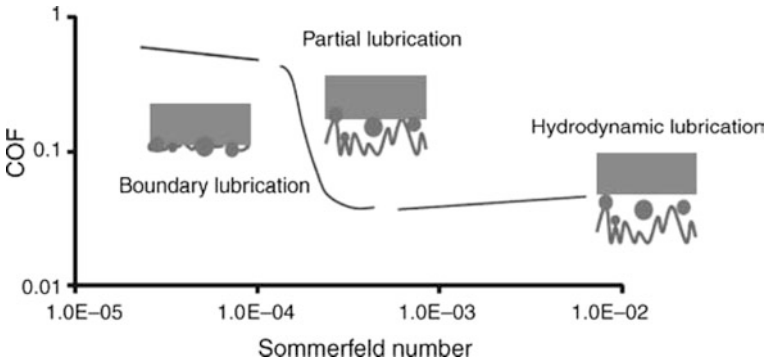

Fig. 13.54 Three modes of contact experienced during CMP [222]. Reprinted with permission. Copyright 2003 JJAP

pad grooves on slurry flow at the pad-wafer interface. It was demonstrated that the pad groove generally increased slurry flow rate and slurry suction at the pad-wafer interface.

13.7.2 Applications

Many MEMS fabrication techniques have been adopted from the field of microelectronics manufacturing, while a significant number of fabrication methods have also been developed to fulfill functional requirements for mechanical, electrical, optical, and sensor structures. Bulk micromachining, surface micromachining, and micromolding are commonly used in MEMS fabrication. During these processes, high surface topography is created and hinders subsequent processes such as thin film deposition and microlithography. Thus, CMP is an enabling technology when smooth or planar surfaces are required. Planarization can be categorized into three levels, as shown in Fig. 13.55: smoothing, local planarization, and global planarization [208, 220, 223].

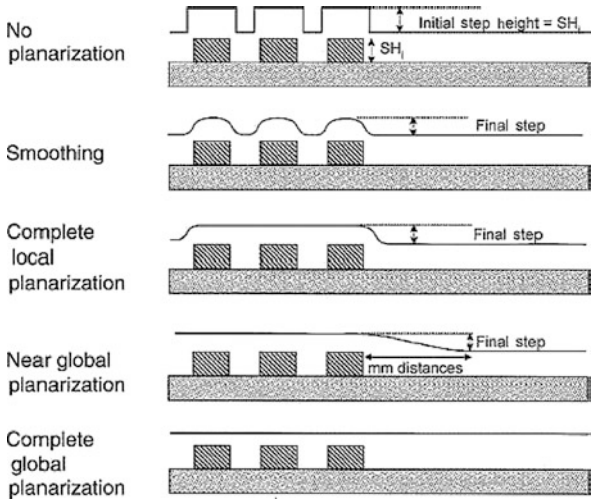

Fig. 13.55 Degree of planarization in the CMP process [208]. Reprinted with permission. Copyright 1997 John Wiley & Sons, Inc

The degree of planarity is determined by considering the geometry of the polished surface, as shown in Fig. 13.56. The planarity is ranked using the values of planarization length R and planarization angle θ [224]:

- Surface smoothing: $0.1\,\mu\text{m} < R < 2.0\,\mu\text{m}$ and $30° < \theta$.
- Local planarization: $2.0\,\mu\text{m} < R < 100\,\mu\text{m}$ and $0.5° < \theta < 30°$.
- Global planarization: $100\,\mu\text{m} << R$ and $\theta < 0.5°$.

13.7.2.1 Smoothing and Local Planarization

Smoothing is the lowest level of planarization, in which sharp features are smoothed and high aspect ratio holes are filled. For sub-micron metallization schemes, CMP

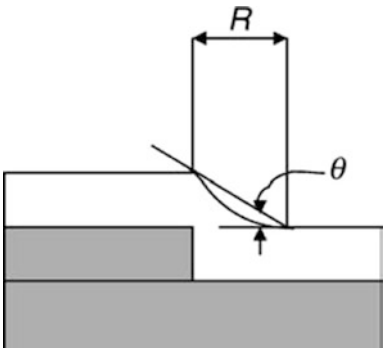

Fig. 13.56 Quantified measurement of planarity [224]. Reprinted with permission. Copyright 1991 ECS

is utilized to smooth the surface and to fill contact and via holes, avoiding poor step coverage, which can lead to high current density and electromigration. In multilevel metallization, simple smoothing is insufficient, since uneven topography can be cumulative through many metal layers. Therefore, local planarization must be achieved.

13.7.2.2 Global Planarization

In the microelectronics industry, the critical dimensions of circuits are constantly reduced as technology advances. This adds to the challenges of the lithography process. In order to minimize the focusing inaccuracy, many enhancement techniques, such as phase-shift masks and immersion lenses, are utilized along with deep UV (193 nm wavelength) lithography tools. However, the introduction of these enhancement techniques significantly reduces the depth of focus in lithography. Typically, lithography tools need to work at a depth of about 270 nm across a 20 mm by 20 mm stepper field. Smoothing or local planarization is not adequate in this regime, and global planarization is required for successful patterning. With finite depth of focus in lithography, any uneven topography and roughness will lead to a reduction in focusing accuracy and inaccurate patterning [220]. Figure 13.57a, b show a comparison between planarized and non-planarized surface topography. In practice, the pattern density within the die significantly affects the results in global planarization. In order to avoid variations in removal rate or step height caused by varied pattern densities, the selection of suitable consumables and process optimization is essential. One method used to minimize variations in pattern density is to mix dummy structures with the main patterns [225].

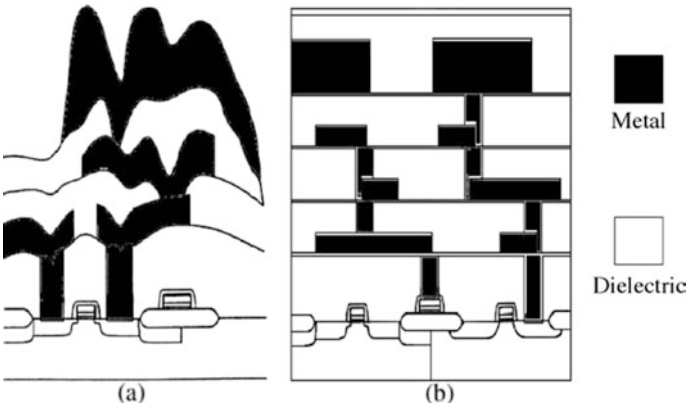

Fig. 13.57 Schematic of a MLM structure (**a**) without and (**b**) with planarization [226]. Reprinted with permission. Copyright 2003 Peter Walters

13.7.2.3 Trench Fill

Trench fill technology was first developed for microelectronics manufacturing. LOCOS (local oxidation of silicon) and Shallow Trench Isolation (STI) are the two main lateral isolation techniques. When dimensions are smaller than 0.25 μm, the so-called "bird's beak" in LOCOS limits its applications, and STI with CMP is adopted as a replacement. The first step of the STI process is etching of the silicon substrate to form trenches; this process is followed by refilling the trenches with oxide. After the trenches are refilled, CMP is used to remove the overburden oxide and achieve a planar surface. The implementation of copper interconnects on chips is realized by damascene technology. Damascene is conceptually similar to STI technology, comprising trench etching, copper refill, and CMP.

MEMS technologies rely largely on developments in microelectronics manufacturing. The above-mentioned technologies have thus found their way into various MEMS applications. However, trenches in MEMS fabrication are much deeper than those encountered in integrated circuit fabrication, and CMP processes must be adjusted to fulfill MEMS-specific requirements. Three-dimensional integration by chip stacking has recently gained much interest. Through-silicon via (TSV) has been adopted as one possible solution to achieve vertical interconnections. TSV relies on the same basic concept as copper damascene, but the vias are deeper and larger (20–100 μm in diameter) than the interconnect trenches on chips. After the vias have been filled, the copper overburden is removed by CMP; requirements for this process are comparable to those in MEMS applications [227].

13.7.3 Pads and Slurry

As discussed in Section 13.7.1.2 (Mechanics of CMP), pad, slurry, and wafer constitute the most important three-body interfaces in the CMP process. CMP involves both chemical and mechanical effects, and therefore polishing pads must have sufficient chemical inertness and mechanical resistance to survive the rigors of polishing. The preferred mechanical properties for polishing pads include high strength (to resist tearing during polishing), suitable hardness, and good abrasion resistance to minimize pad wear during polishing and conditioning. In terms of pad chemistry, the pad must be inert enough to survive aggressive slurry chemistries used in CMP without becoming damaged through degradation or delamination. Another important criterion is pad wettability. The pad must be hydrophilic, to ensure the spread of slurry on the platen. Otherwise, the slurry will be swept away before forming the hydroplane that allows the synergistic combination of chemical effects and mechanical abrasion. Researchers have investigated a number of polymers as polishing pad materials, including polyethylene, PTFE, and others. Polyurethane stands out due to its durability, excellent chemical stability, and adaptability of properties and micro/macro structures.

There are four types of pads currently available, grouped by microstructure and physical and mechanical properties:

Type I: Felts and polymer-impregnated felts
Type II: Porometrics (microporous synthetic leathers)
Type III: Filled polymer sheets (films)
Type IV: Unfilled textured polymer sheets (films)

Key features, properties and typical applications for the four main pad types are summarized in Table 13.10.

The relationship between polishing performance and pad properties is complex and not yet fully understood. First, polishing performance is measured by several parameters that are not only related to pad properties, but are also dependent on polished feature size and substrate size. Second, other factors such as slurry (pH, abrasive size, additives), polishing tool (polisher, conditioner, retaining ring), and polishing conditions (platen speed, flow rate, pressure) also have significant effects on polishing results. Nevertheless, the major relationship between pad properties and polishing performance are still important as guidelines in CMP applications, and are summarized in Table 13.11. In practice, a stiff pad is preferred

Table 13.10 Key features, properties and applications for different pad types [228]

	Type I	Type II	Type III	Type IV
Structure	Felted fibers impregnated with polymeric binder	Porous film coated on supporting substrate	Microporous polymer sheet	Nonporous polymer sheet with surface macrotexture
Microstructure	Continuous channels between fibers	Vertically oriented open pores	Closed-cell foam	None
Inherent microtexture	High	High	Medium	Low
Slurry holding	Medium	High	Low	Minimal
Example of commercial pads	Suba™ STT 711™ Pellon™	Politex™ Surfin™ UR100™ WWP3000™	IC1000™ IC1010™ IC1040™ FX9™ MH™	OXP3000™ OX4000™ NCP-1™ IC2000™
Compressibility	Medium	High	Low	Very low
Stiffness/hardness	Medium	Low	High	Very high
Typical applications	Si stock polishing, Tungsten CMP	Si final polishing, Tungsten CMP, post CMP buff	Si stock, ILD CMP, STI, metal damascene CMP	ILD CMP, STI, metal dual damascene

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Table 13.11 Relationship between pad property and polishing performance [228]

Polishing scale				
Pad property	Wafer	Die	Feature	Conditionability
Density (porosity)	Removal rate, nonuniformity	Defectivity	Dishing, erosion	Yes
Hardness	Macroscratches	Defectivity	Defectivity, roughness, dishing, erosion	Yes
Tensile strength	Pad life			Yes
Abrasion resistance	Pad life			Yes
Modulus (stiffness)	Edge effects	Planarization		Yes
Thickness	Pad life			
Top pad compressibility		Planarization	Dishing	
Pad texture	Pad life, removal rate, nonuniformity, edge effects			
Pad roughness	Removal rate, nonuniformity	Planarization	Dishing, erosion	Yes
Hydrophilicity	Removal rate			Yes

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to achieve ideal planarization and avoid unwanted results such as dishing in metal polishing, which is related to pad bending. However, wafers are not perfectly flat and typically have some degree of curvature due to the stresses introduced during manufacture and coefficient of thermal expansion mismatch in the deposited oxide and metal layers. Therefore, sufficient pad flexibility is required to account for variability in wafer flatness. The solution used in industry is to laminate a stiff pad onto a flexible base pad. One representative example of such a combination is the IC1000/SUBA IV pad, which is widely used in both oxide and metal CMP.

Slurry plays a very important role in the CMP process. Though many advanced technologies are currently employed to prepare high performance slurries, slurries all consist of the same major components: a solution and an abrasive [223]. The abrasive in slurry mechanically abrades the wafer surface and removes surface material. Chemical additives in the slurry react with surface material to enable planarization of the substrate. Also, chemical additives work along with abrasives to minimize the redeposition of polishing debris onto the substrate. An ideal slurry is expected to simultaneously produce a high material removal rate, few surface defects (scratches, corrosion, and other defects), high wafer uniformity, and high selectivity with respect to the underlying layers [228]. Other important slurry

features include ease of handling during use and in waste disposal, long-term stability, and low sensitivity to pattern density and line width effects (which may vary by up to 5 orders of magnitude in different patterned areas on a single wafer).

CMP slurries can be generally categorized into two groups: dielectric slurries and metal slurries. The most commonly used dielectric thin film in IC and MEMS processing is silicon oxide. Slurries for oxide CMP processes have been developed from those used in the optical industry, in which silicate glasses must be finely polished to fabricate optical devices such as lenses and mirrors. Normally, oxide slurries consist of a colloidal suspension of fine fumed silica particles with chemical additives for pH adjustment, typically KOH or NH_4OH. Researchers have also concentrated their efforts on developing ceria-based oxide slurries. Ceria interacts chemically with oxide at a higher rate than silicon oxide does, and thus ceria slurries are able to produce high material removal rates with low abrasive content.

Metal slurries typically contain abrasive particles such as silica, and a number of chemical additives such as oxidizers (H_2O_2, $Fe(CN)_3$), inhibitors, complexing agents, surfactants, and polymer additives. As the minimum feature size shrinks, the tolerance for CMP defects drops dramatically. Since hard abrasives like silica can be a significant source of defects and dielectric loss due to the aggressive mechanical abrasion, researchers have investigated so-called "hybrid abrasive systems," i.e. the incorporation of silica with flexible polymer particles [229]. Pure polymer particles are also intensively studied as potential replacements for conventional inorganic abrasives [230].

Table 13.12 summarizes the effect of slurry variables on CMP performance. This information can be used as a reference when a slurry must be tuned to meet specific performance requirements.

Table 13.12 Effect of slurry variables on CMP performance

Slurry variables	Effect
pH	Dissolution rate of the surface being polished or polishing debris; stability of the abrasive suspension
Buffering agents	Prevent pH drifting
Oxidizers	Induce reduction-oxidation reaction on substrate (metals), leading to metal dissolution or surface film formation
Complexing agents	Enhance dissolution of the surface (metals) being polished or polishing debris
Viscosity	Transport of abrasive and chemicals to and from wafer surface
Slurry abrasive type	Abrasion models
Slurry abrasive size	Removal rate, surface quality (scratches)
Slurry abrasive hardness	Removal rate, surface quality
Slurry abrasive concentration	Removal rate
Slurry stability	Abrasive agglomeration, surface damage

13.7.3.1 Summary of Slurry and Pad

In order to meet specific requirements for MEMS and microelectronic fabrication, commercial suppliers of slurries and pads have developed various dedicated products. Normally, slurries optimized for use in microelectronics manufacturing can be adopted for use in MEMS CMP. However, due to the different wafer structures and materials, these slurries cannot generally be used as-is in MEMS fabrication. Further optimization is required to adapt slurries designed for use in microelectronics manufacturing for use in MEMS. Pads used in MEMS fabrication, meanwhile, are essentially the same as those used in microelectronics manufacturing. Table 13.13 lists some information about commercial slurries and pads used in MEMS polishing.

13.7.4 Polishing Considerations for Different Materials

The main concerns in CMP processes are polishing rate, planarization capability, within die non-uniformity, within-wafer non-uniformity, wafer-to-wafer non-uniformity, removal selectivity, defects, and contamination. Though some of these issues, such as defect control, are common to all CMP processes, each CMP process also has specific issues. In general, CMP processes in MEMS fabrication can be grouped into three areas: dielectrics (including semiconductors), metals, and polymers. In this section, major considerations for each of these materials will be discussed.

13.7.4.1 Rate Comparison and Selectivity

In many CMP applications, it is desirable that material removal should continue only until a certain interface has been reached, at which point the process should stop. Therefore, a crucial consideration in slurry development is the differential removal rate for the target and underlying layers. For example, in copper polishing, an important interfacial concern is erosion: removal of the supporting inter-layer dielectric (ILD) after the barrier layer has been removed [231]. Erosion is dependent on ILD polishing rate, barrier removal rate selectivity, pattern density, and pad hardness. As shown in Fig. 13.58, features with high pattern density are under high local pressure due to the reduced supporting area for the polishing force. Therefore, smaller features experience a higher material removal rate. Consequently, increased ILD exposure time leads to erosion [231]. Erosion can be minimized by improving slurry selectivity; with enhanced selectivity, the polishing process can effectively stop when the ILD layer has been reached. CMP processes with endpoint detection can also reduce erosion by sensing that the ILD layer has been exposed, either through changes in polishing table current or through optical signals [232]. Endpoint detection systems improve process control, combatting variations such as pad-to-pad variations, slurry instability, and pad wear. Erosion in other metal polishing processes, such as tungsten CMP, has also been studied [233].

Table 13.13 Pads and slurries for CMP in microfabrication [228]

Material	Pads	References	Slurries	References	Remarks
Si-oxides (SiO_2, TEOS, PETEOS, doped oxides)	IC1000™ Series, Politex™ Prima	Rohm and Haas	Klebosol® 1501-50, Klebosol® 1508-50	Rohm and Haas	
			EP-MD-8052, EP-MD-8073 EP-MD-8080, EP-MD-8090	Cabot Microelectronics	Fumed silica, for stack heights ≤ 1 μm; colloidal silica, for larger stack heights
			Planerlite-4000 Series	Fujimi	
			Levasil 50CK/30%, Levasil 50CN/30%, Levasil 100 K/30%	H.C. Starck	
			SS 25 from Cabot	Fraunhofer ISIT	
SiN	Suba™ 500, Politex™ Regular	Rohm and Haas	Nalco® 2360	Rohm and Haas	
Al_2O_3	MH Series	Rohm and Haas	Eminess UltraSol™ M5D4 (main) Eminess UltraSol™ 500 (final)	Rohm and Haas	
Sapphire	IC1000™ Perforated, Suba™ 1250, Politex™ Regular	Rohm and Haas	6 μm/3 μm diamond (1), 1 μm diamond (2), UltraSol 500 (3)	Rohm and Haas	
SiC	IC1000™ Perforated, Suba™ 1250, Politex™	Rohm and Haas	Nalco 2360	Rohm and Haas	

Table 13.13 (continued)

Material	Pads	References	Slurries	References	Remarks
Silicon	Suba Series, SPM pads	Fraunhofer ISIT	Glanzox series	Fujimi	
	Fixed abrasive pads	VTT, 3 M	Levasil 50/50%, Levasil 100/45%, Levasil 200/30%-WALM	H.C. Starck	
Polysilicon	IC1000™ Series, Politex™ Prima, WWP3	Rohm and Haas	Klebosol® PL 1509-35, Klebosol® PL 1509-12, Klebosol® PL 1618	Rohm and Haas	
			SS 25 from Cabot	Fraunhofer ISIT	
			Planerlite-6000 Series	Fujimi	
			EP-MP-8010, EP-MP-8188	Cabot Microelectronics	for stack heights ≤ 1 μm for larger stack height removal
Germanium	Suba™ X, Politex™ embossed	Rohm and Haas	Nalco® 2360	Rohm and Haas	
SiGe	Politex™ Regular, SPM3100	Rohm and Haas	Levasil 50CK/30%-V1, Levasil 50CK/30%-V2	H.C.Starck	Abrasive for metal slurry formulation

Table 13.13 (continued)

Material	Pads	References	Slurries	References	Remarks
Copper	IC1000™ Series, VisionPad™ Series, Politex™ Prima	Rohm and Haas	EPL2361	Rohm and Haas	
			EP-MH-870, EP-MH-883 EP-MM-8042, EP-MM-8043	Cabot Microelectronics	for stack height ≤ 5 μm for stack heights ≥5 μm
			Planerlite-7000 Series	Fujimi	
			iCue® Slurries from Cabot	Fraunhofer ISIT	
Tantalum, TaN, TiN	IC1000™ Series, Politex™ Regular	Rohm and Haas	CUS Series, LK Series, SSA Series	Rohm and Haas	
Tungsten	IC1000™ Series, Politex™ Series, FBP Series	Rohm and Haas	e.g. W2000 from Cabot	Fraunhofer ISIT	
NiFe	IC1000™ Series, Politex™ Prima, WWP3000	Rohm and Haas	MSW1500/2000	Rohm and Haas	
ZnCu	IC1000™ Series	Rohm and Haas	MSW1500	Rohm and Haas	
			Compol Series	Fujimi	
			Levasil 50/50%, Levasil 100/45%	H.C. Starck	Abrasive for slurry formulation

Table 13.13 (continued)

Material	Pads	References	Slurries	References	Remarks
AlN	Suba™ 500	Rohm and Haas	Nalco® 2370	Rohm and Haas	
GaAs	Suba™ X embossed, Suba™ 500, OPC6350, SPM3100	Rohm and Haas	Nalco® 2360	Rohm and Haas	
InP	Suba™ 500, Suba™ X, SPM3100	Rohm and Haas	Nalco® 2360 w/bleach	Rohm and Haas	
$LiNbO_3$	Suba™ 1250, Politex™ embossed	Rohm and Haas			
Glass	MH Series, Suba™ X, GS	Rohm and Haas	Ceria based (main), Nalco® 2360 (final)	Rohm and Haas	
Polyimide			EP-MI-8005, EP-MI-8006	Cabot Microelectronics	alumina based slurry alumina based, low defects

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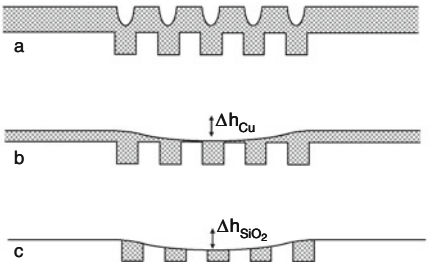

Fig. 13.58 (**a**) Regions of low and high copper pattern density (PD); (**b**) copper polishes faster in regions of high PD, so the copper in those regions is cleared first; (**c**) consequently, the underlying dielectric layer SiO_2 receives more polishing time in regions of high PD and therefore experiences more erosion [231]. Reprinted with permission. Copyright 1994 ECS

13.7.4.2 Dielectrics

As an enabling technology for lithography, etching and metallization, oxide CMP is the most commonly used and studied CMP process [208]. In order to improve interconnect reliability and yields, global planarization must be achieved in oxide CMP. In addition to the improvements in lithography, oxide global planarization also assists in the subsequent etching of the contacts and vias. Global planarization depends mainly on underlying feature density. A number of studies of oxide CMP have investigated the effect of the pattern density on global planarization efficiency [234–236]. CMP process variables and consumables were each found to have a significant effect on global planarity. Process parameters that affected global planarity included platen speed, downward force, and carrier speed [234]. Properties of consumables such as pad hardness and fluid dynamics also affected global planarity [235, 236].

Bulk oxide polishing, such as ILD CMP, does not involve a material interface as a stopping layer. Therefore, within wafer non-uniformity is solely dependent on removal rate controls in the CMP process, tool, and consumables. In general, within wafer non-uniformity is determined by non-uniformities in the removal rate and in the film thickness. On the die scale, the removal uniformity depends on pattern density, while on the wafer scale, the edge effect has a large impact on the uniformity, as the wafer size increases from 150 to 200–300 mm [237, 238]. It is possible to manipulate the CMP removal rate distribution to compensate for the known non-uniformity of the wafer.

Another concern in oxide CMP is the presence of defects. The most common defect associated with oxide CMP is scratching [239]. Scratches can result from pad/wafer contact, abrasive particle/wafer contact, and wafer handling errors. Depending on the size and depth of the scratch, such a defect might cause various failures, including shorting between adjacent lines if metal fills in a wide scratch. Buff CMP processes are used to reduce scratches on the wafer. In buff CMP, wafers are typically polished under low stress on a soft pad to remove small amounts of

oxide, helping to remove the sharp edges associated with a scratch. Although buff CMP can improve yields by smoothing scratches, it cannot be used to repair deep scratches. Therefore, the best option to avoid yield loss caused by scratching is to eliminate the source of defects from CMP processes and consumables. Another common source of defects in oxide CMP is contamination of wafer surfaces by particles or chemical contaminants during the CMP process. Post-CMP cleaning can be performed to remove these contaminants from wafers.

13.7.4.3 Metals

Tungsten CMP and copper CMP are currently the mainstream fabrication techniques for metal interconnect structures in semiconductor devices. Tungsten interconnects can be divided into two categories: contacts, which serve as the interconnect between the front-end of the device and back-end metallization, and vias, which connect metal layers, as shown in Fig. 13.59. In order to overcome the high resistance associated with decreasing metal line size, copper is introduced due to its low resistivity to replace the conventionally-used aluminum in metallization. Conceptually, tungsten plug fabrication and copper damascene are quite similar. Figure 13.60 shows the process of forming copper lines and vias using the damascene technique. Specifically, oxide is etched to form the patterns for wires and lines. A barrier layer is deposited to enhance the adhesion of the metal line and to avoid the diffusion of copper ions into the underlying dielectric layer. Copper is then deposited, and the overburden of copper is removed with CMP. In both tungsten and copper CMP, the two main interfacial concerns are dishing and erosion.

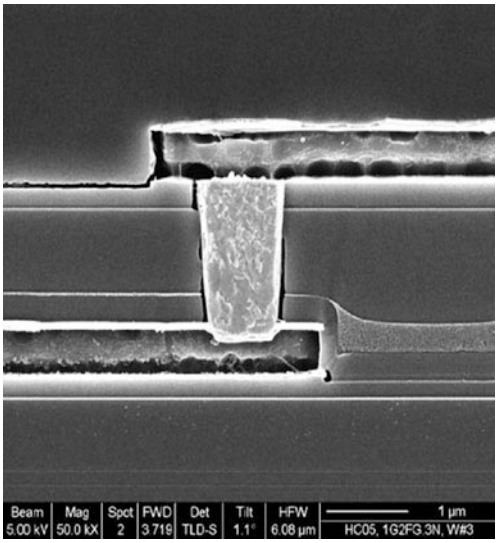

Fig. 13.59 Cross-sectional SEM image of a representative tungsten plug between two metal lines [240]. Reprinted with permission. Copyright 2004 CMP MIC

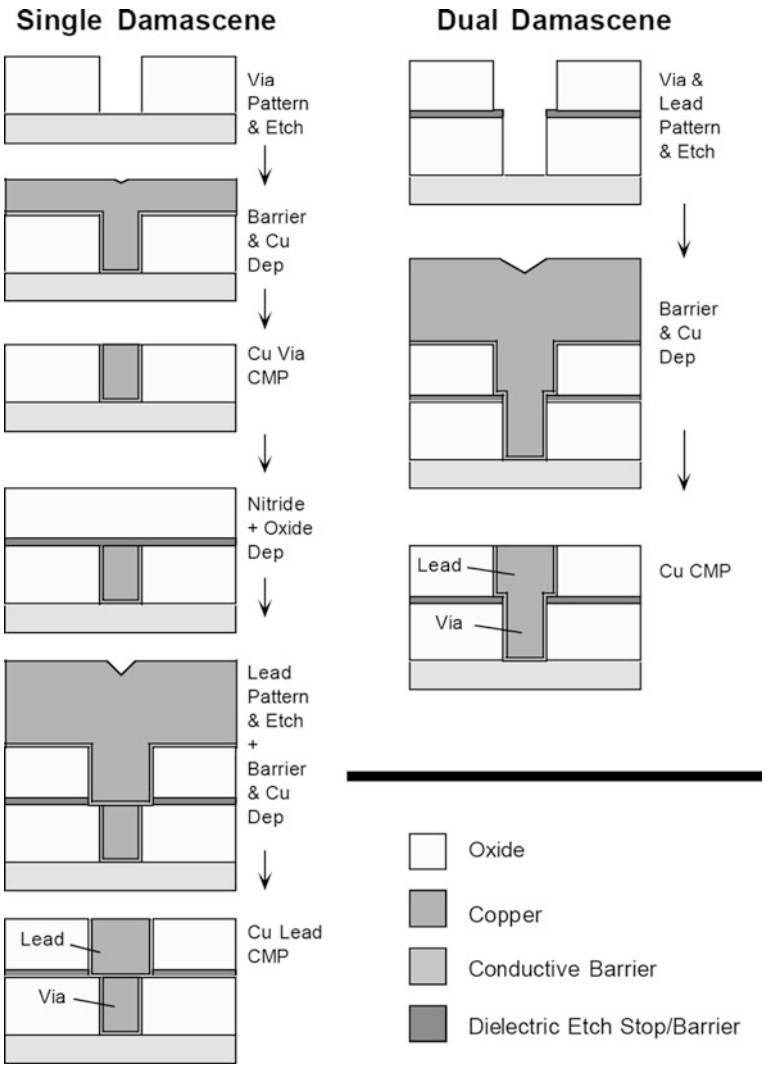

Fig. 13.60 Damascene and dual damascene technology

In tungsten CMP, dishing refers to the removal of tungsten inside the via below the ILD surface, while in copper CMP dishing refers to the removal of copper in the trench below the ILD surface. In either case, erosion is the removal of material from the supporting ILD after clearing the barrier layer [231]. Figure 13.61 illustrates the differences between dishing and erosion in copper CMP. Dishing is dependent on line width [231], copper removal rate selectivity, and pad hardness. At large feature size, high copper removal rate selectivity for barrier or dielectric increases

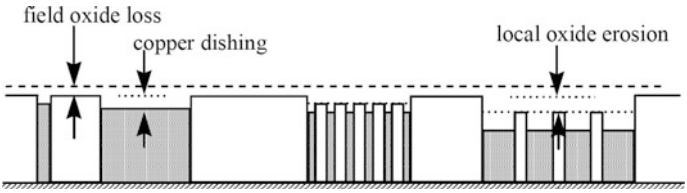

Fig. 13.61 Schematic diagram of dishing and erosion in copper CMP

the dishing rate. Softer pads allow the force to penetrate into the trench, which also leads to dishing. As mentioned in 13.7.4.1, erosion is highly dependent on pattern density, removal selectivity, and pad hardness.

13.7.4.4 Polymers

In order to minimize interconnection delays, various polymeric low-k dielectric materials have been introduced in microelectronics [241]. In MEMS fabrication, a wide range of polymeric materials has been used depending on the specific application. For example, polycarbonate (PC) and polyimide (PI) are often used in biomedical devices due to their suitable interface with biological tissues [242]. Polymethyl methacrylate (PMMA) substrates are used to fabricate microfluidic devices with an inprinting technique [243]. Global planarization is required on the polymeric layer. The major challenge for the planarization of low-k dielectrics and other polymers is their inferior mechanical strength and hardness as compared with silica. This directly affects the CMP process because force and rotation rate must be reduced to avoid mechanical damage and scratching. Requirements on slurry chemistry are quite specific to the polymer substrates, as they depend strongly on the chemical properties of the material. Furthermore, control of large particles in the slurry must be more restrictive, because large agglomerates can easily indent polymers due to their soft nature [244].

13.7.5 Cleaning and Contamination Control

An inseparable part of the CMP process, post-CMP cleaning determines the final defect level on the polished wafer, and thus significantly affects the yield. During CMP, wafer surfaces exposed to the aggressive chemicals and pressures inherent in the process are easily contaminated with polishing residues, trace metals, organic additives, and so forth. Resulting modifications and damage to the wafer surface can adversely affect the device's properties and performance. For example, polishing residue can cause patterning and/or deposition errors in subsequent processes. These errors may lead to shorts and incomplete circuits in the interconnect. An effective post-CMP cleaning process can minimize this type of fault, reducing the frequency

of defects and improving device yield, when combined with an optimized polishing process [208, 245]. While the purpose of CMP cleaning is to efficiently remove contaminants on a polished wafer, it also must not degrade any material properties. Although defect requirements in MEMS fabrication are less stringent than those encountered in IC manufacturing due to larger feature sizes in MEMS, post-CMP cleaning still plays a key role in ensuring high production yields.

There are two types of post-CMP cleaning: contact mode and non-contact mode. Double-sided polyvinyl alcohol (PVA) brush scrubbing is the most widely used contact cleaning process. As shown in Fig. 13.62, the wafer is sandwiched between a pair of double-sided brush scrubbers, so that both sides of the wafer are cleaned simultaneously. The efficiency of the process is tunable by adjusting the scrubbing speed or by adding chemical additives to the cleaning solution.

Non-contact cleaning methods include using megasonics or spray processes to remove contaminants from the wafer's surface [247]. Many cleaning equipment suppliers offer systems utilizing a combination of contact and non-contact cleaning, increasing cleaning efficiency.

A variety of wet-cleaning chemicals are used in semiconductor manufacturing. Table 13.14 lists examples of cleaning solutions. As described in the table, cleaning solutions formulated with different chemicals are used for different applications. Cleaning solutions are also commonly formulated with organic acids, such as oxalic acid, citric acid, and various surfactants. Organic acids can serve as complexing agents to dissolve metal contaminants into the solution. Another function of organic acids is to control the surface zeta potential by adjusting the pH of the solution [248].

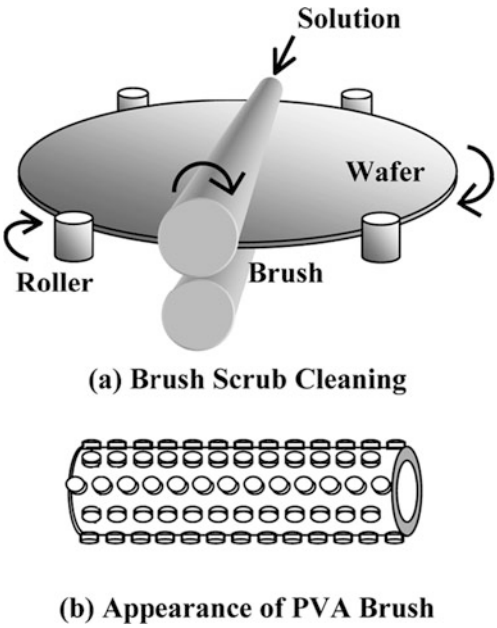

Fig. 13.62 Post-CMP cleaning system. (**a**) Brush-scrub cleaning. (**b**) Appearance of PVA brush [246]. Reprinted with permission. Copyright 2005 IEEE

Table 13.14 Typical cleaning solutions

Cleaning solution	Composition	Typical application
APM (SC1)	$NH_4OH/H_2O_2/H_2O$	Removal of organic contaminants and particles
HPM (SC2)	$HCl/H_2O_2/H_2O$	Removal of metallic ions; surface passivation by native oxide formation
DHF	HF/H_2O	Removal of native oxide film and metallic ions
SPM	H_2SO_4/H_2O_2	Removal of organic contaminants and metallic ions

Table 13.15 Summary on post CMP cleaning processes for various materials

CMP	Typical defects	Technique	Chemicals	Consideration
Oxide	Slurry particles, scratches	Brush scrubbing, spray	NH_4OH, HF	Over exposure to cleaning solution may deepen scratches
W	Slurry particles, scratches, residual metal	Brush scrubbing, buffing	DHF	Removal of slurry residual from recessed plug
STI	Slurry particles, organic contaminants	Brush scrubbing	NH_4OH, HF	Removal of contaminants from both oxide surface and nitride surface
Poly-Si	Pad debris, Organic contaminant	Brush scrubbing	SC1	Avoiding water marks
Cu/low-k	Slurry particles, organic contaminants, residual metal	Brush scrubbing	BTA[1], NH_4OH, TMAH[2], Citric acid, Oxalic acid	Avoiding corrosion

BTA: Benzotriazole; TMAH: Tetramethylammonium hydroxide

Surfactants are widely used in cleaning solutions to modify surface interactions by influencing the surface zeta potential [249].

Specific concerns exist for post-CMP cleaning, due to the interactions between slurry and different surfaces. Table 13.15 lists common cleaning solutions and concerns for typical materials used in semiconductor manufacturing.

13.7.6 Case Study

CMP technology has been applied in MEMS fabrication for many years. CMP can be used to flatten sacrificial layers, such as oxides, and improve the uniformity of oxide across a wafer's surface [250]. The 5-level polysilicon surface micromachining technology developed by Sandia National Labs would be virtually impossible

without planarization [250, 251]. In MEMS-CMOS integration, MEMS wafers can be bonded to COMS wafers with Al as the interconnect between the two wafers. After the Al sputtering process, Al CMP can be used to remove excess Al and define the contact via areas, ensuring good wafer bonding [252]. CMP can also serve as an alternative to reactive ion etching (RIE) for patterning thin films. In one study, ZnO was deposited onto a patterned Si surface using radio frequency (RF) sputtering and CMP was used to remove excess ZnO in un-patterned areas [253]. Multi-layered poly-silicon carbide (poly SiC) for micro-mirrors has also been fabricated with CMP on poly SiC, using patterned silicon oxide as a sacrificial layer [254, 255]. A few examples of CMP processes used in MEMS fabrication will be discussed in the following case studies.

13.7.6.1 Case Study 10: Magnetic Microdevice

Most MEMS transducers are driven electrostatically, mainly because of the ease of fabrication and integration [256, 257]. However, magnetic microdevices are also of interest, due to their unique advantages including their capability for maintaining large forces over long distances, low voltage operation, no snapdown, low hysteresis, and linear torque-current relationship [258]. Magnetic microdevices are used in applications such as optical switches, magnetic microparticle manipulation, microfluidic mixing, and micro-mirror actuation.

The key component in a magnetic microdevice that requires CMP is the conductive microcoil. Typically, microcoils are fabricated by depositing a thick film of conductor material onto the Si surface with/without a core. Figure 13.63 shows a typical process flowchart for the fabrication of an inductive coil with a copper conductor. In this case, the coil is fabricated with damascene technology. A few microns of copper are plated onto the etched pattern, followed by CMP to achieve a planar surface. Similar to copper interconnect CMP in microelectronic manufacturing, dishing and defects such as erosion pits are the main concerns in this CMP process. Uniformity is another important consideration for process optimization, since coils are fabricated on wafer level. Using a stacked pad, such as IC1000/SUBA IV, is one option to avoid severe dishing and erosion and to achieve good uniformity. Figures 13.64 and 13.65 shows various designs of conductive coils fabricated on a wafer via the CMP process. In Fig. 13.65, a core is incorporated into the center of the conductive coil to enhance magnetic field intensity and to increase the magnitudes of magnetic field gradients in that area.

13.7.6.2 Case Study 11: A Drug-Delivery Probe with an In-line Flow Meter

A silicon drug delivery probe integrated with an in-line flowmeter is discussed in this case study [260]. The silicon probe includes a microchannel built into the probe for drug delivery. A polysilicon-based in-line thermal flowmeter is positioned on top of the microchannel. As shown in Fig. 13.66, a triangular channel is formed by layered LPCVD oxide/nitride/oxide sidewalls (labeled as dielectrics) and a

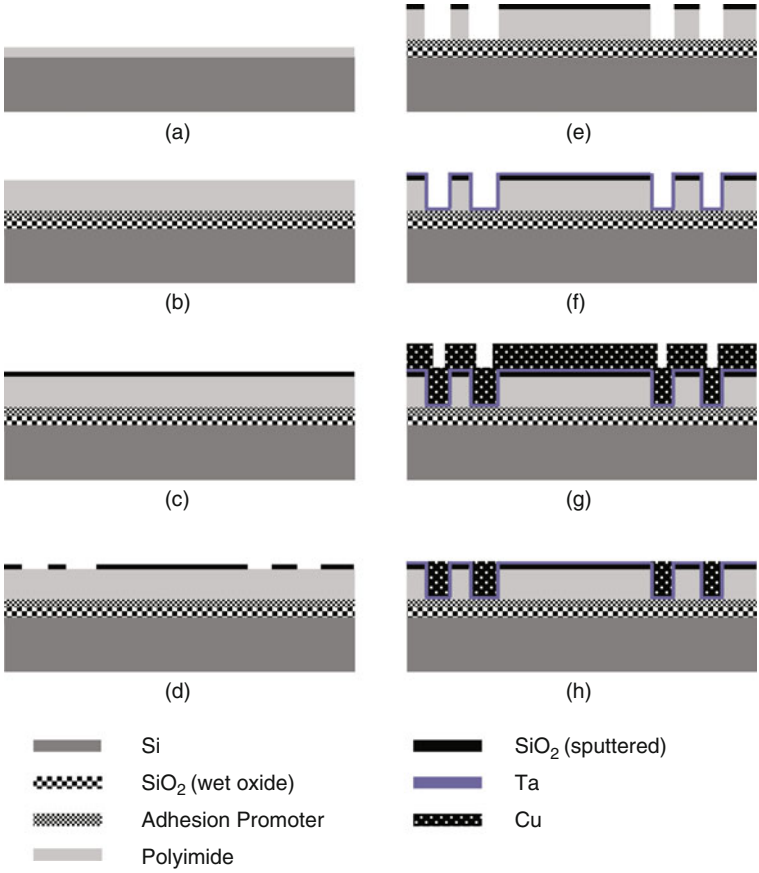

Fig. 13.63 Typical process flow for coil fabrication [259]. Reprinted with permission. Copyright 2008 IEEE

lightly-doped polysilicon resistor is formed on a dielectric diaphragm over the flow channel. Doped polysilicon is used to connect the resistor. A vacuum gap of 2 μm is used to cap the dielectric window to minimize heat escape to the surroundings and maximize heating efficiency. During the operation, constant current is applied to heat the sensor. When liquid flows through the channel, convective heat transfer reduces the sensor temperature, leading to increased sensor resistance [260, 261]. Compared to boron-doped silicon sidewalls for the probe [261], the dielectric sidewalls offer about 20% better heating efficiency and flowmeter sensitivity.

Figure 13.67 shows the processing steps with a combination of trench refill and CMP to fabricate microfluidic channels with dielectric sidewalls. A triangular trench (at least 15 μm wide) is formed by ethylenediamine pyrocatechol (EDP) etching,

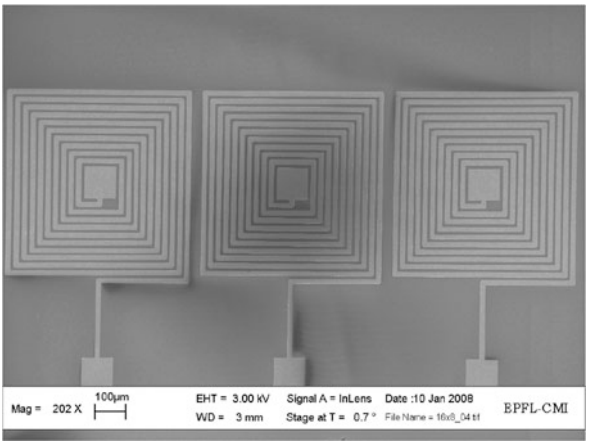

Fig. 13.64 Coil structure on a wafer after CMP [259]. Reprinted with permission. Copyright 2008 IEEE

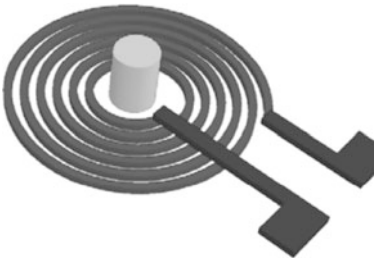

Fig. 13.65 A spiral micro-coil with a magnetic pillar in the center [258]. Reprinted with permission. Copyright 2006 IEEE

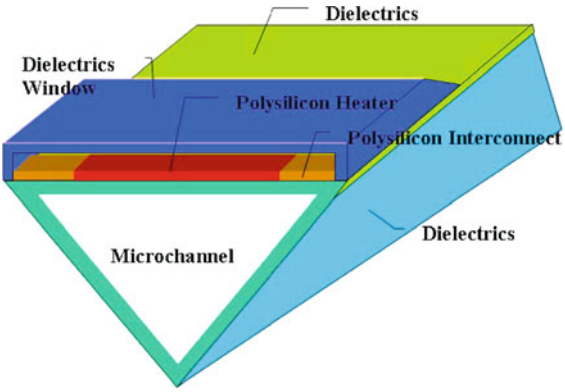

Fig. 13.66 The structure of a vacuum-isolated thermal in-line flowmeter located on a dielectric diaphragm over the microchannel [260]. Reprinted with permission. Copyright 2007 IEEE

followed by shallow boron doping and deposition of dielectric layers as the sidewalls. Polysilicon was then deposited (about 13 µm) to fill the trench as a sacrificial material, and a damascene CMP process was used to planarize the top surface so that polysilicon remained only within the channel– that is, polysilicon in non-trench areas was polished down to the oxide layer. A layer of masking oxide was deposited

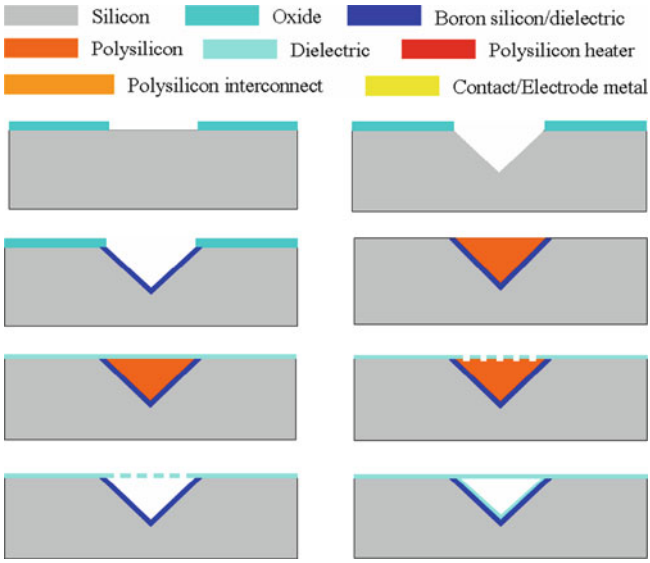

Fig. 13.67 Fabrication process for a drug delivery probe with in-line flowmeters based on trench refill and CMP techniques [260]. Reprinted with permission. Copyright 2007 IEEE

to cover and pattern the trench, and the sacrificial polysilicon was removed using EDP to form the channel. The channels were then sealed with LPCVD dielectric materials.

After the channels were sealed, a polysilicon heater was positioned on top of the channel's surface, followed by regular surface micromachining to complete the in-line thermal flowmeter. The main purpose of the CMP process in this case was to remove 13 μm of polysilicon. Selectivity of polysilicon over oxide during this CMP process is critical. Another key consideration is dishing, which must be controlled to ensure flatness of the top surface of the channel. Highly selective slurry for polysilicon over silicon dioxide has been reported for use in this application [262]. By adding additives such as arginine into colloidal- or ceria-based slurry, removal rates up to 550 nm/min can be achieved for polysilicon. The selectivity ratio of polysilicon over silicon oxide is about 130.

13.7.6.3 Case Study 12: Nanomechanical Optical Devices

Integrated optical devices have been designed and fabricated to take advantage of the fact that the effective refractive index of a waveguide can be modulated by a movable element that is driven into the evanescent field over a distance of about 100 nm [263]. The applications of such devices include optical intensity modulators, tunable filters, and optical pressure sensors. A schematic cross-section of the device is shown in Fig. 13.68. The waveguide is fabricated at the lower wafer, and the moving element is positioned on the top wafer using KOH etching. The gap between the moving element and the waveguide is determined by the thickness of the PECVD

SiO_2 spacer layer on top of the waveguide. Prior to wafer bonding, the PECVD SiO_2 spacer layer must be polished, since it is critical for controlling gap distance and smoothness.

A MECAPOL E460 tool was used with Semisphere 25 slurry and UR 100 pad for the CMP process. PECVD SiO_2 (1 μm) was deposited and patterned prior to CMP. Processing conditions used were a working pressure of 14.5 psi and a rotation speed of 60 rpm; these conditions resulted in a removal rate of 300 nm/min for PECVD SiO_2. Atomic force microscopy (AFM) data showed that the root mean square roughness was reduced by a factor of 10 (from 2.2 to 0.2 nm) after 30 s of polishing. After CMP, the wafer underwent brushing, DI water rinsing, and RCA cleaning to remove residual slurry particles and possible sodium hydroxide contamination.

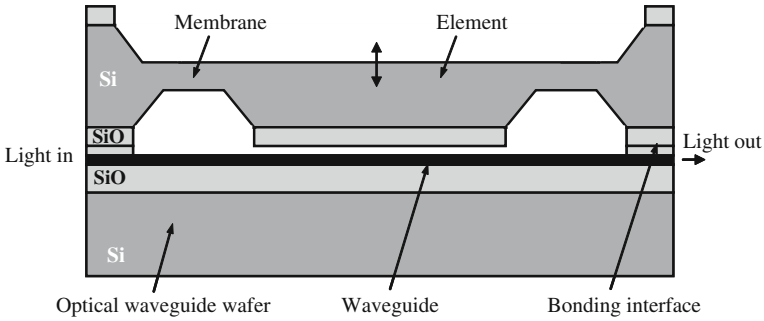

Fig. 13.68 Schematic cross section of the integrated optical nanomechanical device [263]. Reprinted with permission. Copyright 1998 IEEE

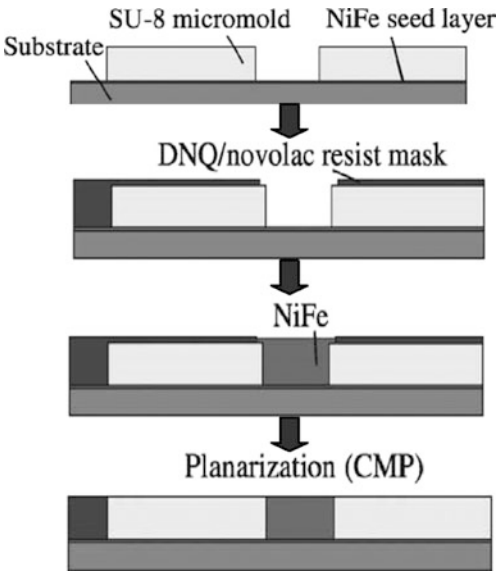

Fig. 13.69 Model of electroforming and metal CMP

13.7.6.4 Case Study 13: CMP of SU-8/Permalloy Combination in MEMS Devices

Polymer materials are widely used in MEMS fabrication to create high aspect ratio structures. This case study investigates the applications of CMP for planarization of electroplated permalloys (NiFe 81/19) in micromolds using epoxy SU-8. This polymer serves as a stopping layer during CMP, and remained in the structure as an insulation layer. The SU8/permalloy combination was designed to fabricate magnetic MEMS devices.

Figure 13.69 shows a schematic view of the cross-section of a typical magnetic MEMS device. A SU-8 micromold of about 20 μm was patterned on top of a suitable plating base. The NiFe was electroplated onto the microforms, filling the molds completely. The NiFe overburden had to be polished to achieve surface planarity. In order to selectively fill the SU-8 micromolds, a novolac photoresist mask was applied before electroplating. Polishing conditions and slurry information are listed in Tables 13.16 and 13.17.

The mechanical properties of SU-8 depended on post-bake treatment. In this study, the polymer was treated at 95, 120, and 150°C. Figure 13.70 shows the correlation between removal rate and polishing pressure for SU-8 treated at different temperatures. Polymers treated with higher post-bake temperatures showed better resistance to abrasion, and thus had low material removal rates. An AFM study showed scratches on the polymer surface, indicating mechanical abrasion during polishing. However, the overall surface quality met the requirements for the intended application.

The removal rates of permalloy under different pressures are shown in Fig. 13.71. The results indicate that permalloy has about half of the removal rate of SU-8 baked at 150°C. AFM analysis showed mottled free surfaces, indicating well balanced chemical and mechanical effects during polishing. Based on these polishing rates of SU-8 and permalloy, optimal CMP conditions were selected for the NiFe/SU-8

Table 13.16 Polishing conditions for NiFe

Polishing conditions	
Polisher	Peter Walters 3R40
Platen diameter	400 mm
Pad	IC1400 stacked
Platen speed	18 rpm
Carrier speed	18 rpm
Slurry flow	15 ml/min

Table 13.17 Slurry specifications for NiFe CMP

Slurry specifications	
Abrasive particle	Al_2O_3
Median particle size	225 nm
pH at 25°C	4.1
Abrasive content	6.9 wt%

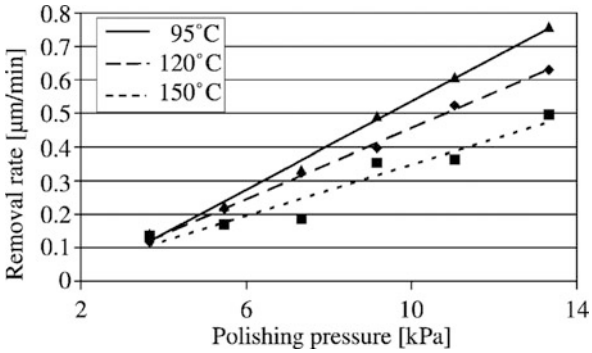

Fig. 13.70 SU-8 removal rate as a function of polishing pressure for different hard bake times [264]. Reprinted with permission. Copyright 2003 Elsevier

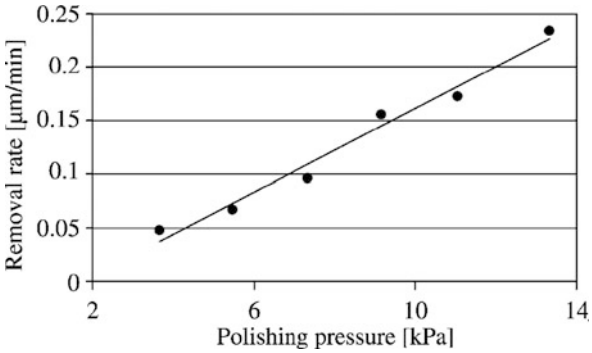

Fig. 13.71 Permalloy removal rate as a function of polishing pressure [264]. Reprinted with permission. Copyright 2003 Elsevier

structures. Step height was reduced to about 20 nm after planarization, which was sufficient for the intended application of the device.

References

1. R.T. Howe: Surface micromachining for microsensors and microactuators, J. Vac. Sci. Technol. B 6, 1809–1813 (1988)
2. R.S. Muller: Microdynamics, Sens. Actuators A 21, 1–8 (1990)
3. K. Petersen: Silicon as a mechanical material, Proc. IEEE Electron Devices 70, 420–457 (1982)
4. N. Tas, T. Sonnenberg, H. Jansen, R. Legtenberg, M. Elwenspoek: Stiction in surface micromachining, J. Micromech. Microeng. 6, 385–397 (1996)
5. K. Komvopoulos: Surface engineering and microtribology for microelectromechanical systems, Wear 200, 305–327 (1996)
6. R. Maboudian, R.T. Howe: Critical review: Adhesion in surface micromechanical structures, J. Vac. Sci. Technol. B 15, 1–20 (1997)
7. C.H. Mastrangelo: Adhesion-related failure mechanisms in micromechanical devices, Tribol. Lett. 3, 223–238 (1997)
8. R. Maboudian: Surface processes in MEMS technology, Surf. Sci. Rep. 30, 207–269 (1998)
9. B. Bhushan: Tribology Issues and Opportunities in MEMS, Proceedings of the NSF/AFOSR/ASME Workshop on Tribology Issues and Opportunities in MEMS held in Columbus, Ohio, USA, 9–11 November 1997 (Kluwer, Dordrecht, 1998)

10. Z. Rymuza: Control tribological and mechanical properties of MEMS surfaces. Part 1: Critical review, Microsystems Technol. 5, 173–180 (1999)
11. J.J. Sniegowski, M.P. de Boer: IC-compatible polysilicon surface micromachining, Annu. Rev. Mater. Sci. 30, 299–333 (2000)
12. R. Maboudian, C. Carraro: Surface engineering for reliable operation of MEMS devices, J. Adhesion Sci. Technol. 17, 583–591 (2003)
13. R. Maboudian, C. Carraro: Surface chemistry and tribology of MEMS, Ann. Rev. Phys. Chem. 55, 35–54 (2004)
14. S. Henck: Lubrication of digital micromirror devices, Tribol. Lett. 3, 239–247 (1997)
15. S.L. Miller, M.S. Rodgers, G. La Vigne, J.J. Sniegowski, P. Clews, D.M. Tanner, K.A. Peterson: Failure modes in surface micromachined microelectromechanical actuation systems, Microelectron. Reliab. 39, 1229–1237 (1999)
16. D.M. Tanner, T.B. Parson, A.D. Corwin, J.A. Walraven, J.W. Wittwer, B.L. Boyce, S.R. Winzer: Science-based MEMS reliability methodology, Microelectron. Reliab. 47, 1806–1811 (2007)
17. A.D. Romig, M.T. Dugger, P.J. McWhorter: Materials issues in microelectromechanical devices: science, engineering, manufacturability and reliability, Acta Mater. 51, 5837–5866 (2003)
18. F.W. DelRio, M.P. de Boer, J.A. Knapp, E.D. Reedy, P.J. Clews, M.L. Dunn: The role of van der Waals forces in adhesion of micromachined surfaces, Nat. Mater. 4, 629–634 (2005)
19. R. Maboudian, R.T. Howe: Stiction reduction processes for surface micromachines, Tribol. Lett. 3, 215–221 (1997)
20. M. Madou: Fundamentals of Microfabrication (CRC Press, New York, NY, 1998)
21. M. Gad-el-Hak: MEMS – Introduction and Fundamental (CRC Press, Boca Raton, FL, 2006)
22. C.-J. Kim, J.Y. Kim, B. Sridharan: Comparative evaluation of drying techniques for surface micromachining, Sens. Actuators A 64, 17–26 (1998)
23. H. Guckel, J.J. Sniegowski, T.R. Christenson, F. Raissi: The application of fine-grained, tensile polysilicon to mechanically resonant transducers, Sens. Actuators A21–A23, 346–351 (1990)
24. G.T. Mulhern, D.S. Soane, R.T. Howe: Supercritical carbon dioxide drying of microstructures, Proceedings of the 7th International Conference on Solid-State Sensors and Actuators – Transducers'93, Yokohama, Japan, pp. 296–300 (1993)
25. C.H. Mastrangelo, G.S. Saloka: A dry-release method based on polymer columns for microstructure fabrication, Proceedings of the IEEE Microelectromechanical System Workshop, Ft. Lauderdale, FL, pp. 77–81 (1993)
26. D. Kobayashi, C.-J. Kim, H. Fujita: Photoresist-assisted release of movable microstructures, Japan J. Appl. Phys. 32, L 1642–L 1644 (1993)
27. F. Kozlowski, N. Lindmair, T. Scheiter, C. Hierold, W. Lang: A novel method to avoid sticking of surface micromachined structures, Proceedings of the 8th International Conference on Solid-State Sensors and Actuators – Transducers'95, Stockholm, Sweden, pp. 220–223 (1995)
28. J.H. Lee, Y.I. Lee, W.I. Jang, C.S. Lee, H.J. Yoo: Characterization of anhydrous HF gas-phase etching with CH3OH for sacrificial oxide removal, Sens. Actuators A 64, 27–32 (1998)
29. U. Srinivasan, M.R. Houston, R.T. Howe, R. Maboudian, J Microelectromech Syst. 7, 252–260 (1998)
30. Tousimis Research Corporation, http://tousimis.com/ (accessed in 2009)
31. Idonus, Sarl, http://www.idonus.com/ (accessed in 2009)
32. C.R. Stoldt, C. Carraro, W.R. Ashurst, D. Gao, R.T. Howe, R. Maboudian: A low-temperature CVD process for silicon carbide MEMS, Sens. Actuators A 97–98, 410–415 (2002)

33. D. Briggs, M. P. Seah (Eds.): Practical Surface Analysis by Auger and X-ray Photoelectron Spectroscopy (Wiley, New York, NY, 1983)
34. M.R. Houston, R. Maboudian: Stability of ammonium fluoride-treated Si 100, J. Appl. Phys. 78, 3801–3808 (1995)
35. C.L. Hedberg (Ed.): Handbook of Auger Electron Spectroscopy (Physical Electronics Publishing, Eden Prairie, MN, 1995)
36. J.I. Goldstein, D.E. Newbury, P. Echlin, D.C. Joy, C.E. Lyman, E. Lifshin, L.C. Sawyer, J.R. Michael: Scanning Electron Microscopy and X-Ray Microanalysis (Springer, The Netherlands, 2003)
37. A.F. Benninghoven, G. Rüdenauer, H.W. Werner: Secondary Ion Mass Spectrometry: Basic Concepts, Instrumental Aspects, Applications, and Trends (Wiley, New York, NY, 1987)
38. F. Giessibl: Advances in atomic force microscopy, Rev. Mod. Phys. 75, 949–983 (2003)
39. A.W. Adamson, A.P. Gast: Physical Chemistry of Surfaces, 6th edn (Wiley, New York, NY, 1997)
40. J.N. Israelachvili: Intermolecular and Surface Forces (Academic, London, 1985)
41. D. Quere: Wetting and roughness, Annu. Rev. Mater. Res. 38, 71–99 (2008)
42. C.H. Mastrangelo, C.H. Hsu: A simple experimental technique for the measurement of the work of adhesion of microstructures, Proceedings of the IEEE Solid-State Sensor and Actuator Workshop – Hilton Head'92, Hilton Head, SC, pp. 208–212 (1992)
43. M.R. Houston, R.T. Howe, R. Maboudian: Effect of hydrogen termination on the work of adhesion between rough polycrystalline silicon surfaces, J. Appl. Phys. 81, 3474–3483 (1997)
44. M.P. de Boer, T.A. Michalske: Accurate method for determining adhesion of cantilever beams, J. Appl. Phys. 86, 817–827 (1999)
45. M.P. de Boer, J.A. Knapp, T.A. Michalske, U. Srinivasan, R. Maboudian: Adhesion hysteresis of silane coated microcantilevers, Acta Mater. 48, 4531–4541 (2000)
46. R. Lechtenberg, H.A.C. Tilmans, J. Elders, M. Elwenspoek: Stiction of surface micromachined structures after rinsing and drying: model and investigation of adhesion mechanisms, Sens. Actuators A 43, 230–238 (1994)
47. W.R. Ashurst, M.P. de Boer, C. Carraro, R. Maboudian: An investigation of sidewall adhesion in MEMS, Appl. Surf. Sci. 212–213, 735–741 (2003)
48. S.J. Timpe, K. Komvopoulos: An experimental study of sidewall adhesion in microelectromechanical systems, J Microelectromech. Syst. 14, 1356–1363 (2005)
49. S. Majumder, N.E. McGruer, G.G. Adams, P.M. Zavracky, R.H. Morrison, J. Krim: Study of contacts in an electrostatically actuated microswitch, Sens. Actuators A, 93, 19–26 (2001)
50. M.G. Lim, J.C. Chang, D.P. Schultz, R.T. Howe, R.M. White: Polysilicon Microstructures to Characterize Static Friction, Proceedings of the IEEE Micro-Electro-Mechanical Systems Workshop, Napa Valley, CA, pp. 82–88 (1990)
51. D.H. Alsem, M.T. Dugger, E.A. Stach, R.O. Ritchie: Micron-scale friction and sliding wear of polysilicon silicon thin structural films in ambient air, J. Microelectromech. Syst. 17, 1144–1154 (2008)
52. E.E. Flater, A.D. Corwin, M.P. de Boer, R.W. Carpick: In-situ wear studies of surface micromachined interfaces subject to controlled loading, Wear 260, 580–593 (2006)
53. X.B. Tan, A. Modafe, R. Ghodssi: Measurement and modeling of dynamic rolling friction in linear microball bearings, J. Dyn. Syst. Meas. Control – Trans. ASME, 128, 891–898 (2006)
54. L.S. Fan, Y.C. Tai, R.S. Muller: Integrated movable micromechanical structures for sensors and actuators, IEEE Trans. Electron Dev. 35, 724–730 (1988)
55. R.L. Alley, P. Mai, K. Komvopoulos, R.T. Howe: Surface roughness modification of interfacial contacts in polysilicon microstructures, Proceedings of the 7th International Conference on Solid-State Sensors and Actuators – Transducers'93, Yokohama, Japan, pp. 288–291 (1993)

56. Y. Yee, K. Chun, J.D. Lee: Polysilicon Surface Modification Technique to Reduce Sticking of Microstructures, Proceedings of the 8th International Conference on Solid-State Sensors and Actuators – Transducers'95, Stockholm, Sweden, pp. 206–209 (1995)
57. F.W. DelRio, M.L. Dunn, B.L. Boyce, A.D. Corwin, M.P. de Boer: The effect of nanoparticles on rough surface adhesion, J. Appl. Phys. 99, 104304 (2006)
58. F.W. DelRio, M.L. Dunn, M.P. de Boer: Growth of silicon carbide nanoparticles using tetraethylorthosilicate for microelectromechanical systems, Electrochem Solid-State Lett. 10, H27–H30 (2007)
59. A. Ulman: An Introduction to Ultrathin Organic Films: From Langmuir-Blodgett to Self-Assembly (Academic, San Diego, CA, 1991)
60. R. Maboudian, W.R. Ashurst, C. Carraro: Self-assembled monolayers as anti-stiction coatings for MEMS: characteristics and recent developments, Sens. Actuators A 82, 219–223 (2000)
61. R. Maboudian, W.R. Ashurst, C. Carraro: Tribological challenges in MEMS, Tribol. Lett. 12, 95–100 (2002)
62. X.Y. Zhu, J.E. Houston: Molecular lubricants for silicon-based microelectromechanical systems (MEMS): A novel assembly strategy, Tribol. Lett. 7, 87–90 (1999)
63. X.Y. Zhu, V. Boiadjiev, J.A. Mulder, R.P. Hsung, R.C. Major: Molecular assemblies on silicon surfaces via Si-O linkages, Langmuir 16, 6766–6772 (2000)
64. W.R. Ashurst, C. Carraro, R. Maboudian, W. Frey: Wafer level anti-stiction coatings with superior thermal stability, Sens. Actuators A 104, 213–221 (2003)
65. W.R. Ashurst, C. Carraro, R. Maboudian: Vapor phase anti-stiction coatings for MEMS, IEEE Trans. Dev. Mater. Reliab. 3, 173–178 (2003)
66. T.M. Mayer, M.P. de Boer, N.D. Shinn, P.J. Clews, T.A. Michalske: Chemical vapor deposition of fluoroalkylsilane monolayer films for adhesion control in microelectromechanical systems, J. Vac. Sci. Technol. B 18, 2433–2440 (2000)
67. Applied MicroStructures Inc. http://www.appliedmst.com/products_mvd150.htm (accessed in 2009)
68. Memsstar Technology, http://www.memsstar.com/products/ (accessed in 2009)
69. E. Bhattacharya, J. Kuang, M. Judy, J. Martin: Stiction in surface micromachined structures, Proceedings of the International Workshop Physics of Semiconductor Devices, Delhi, India, pp. 485–489 (2001)
70. E. Bhattacharya, J. Kuang, M. Judy, J. Martin: A three terminal test structure to measure stiction force using I–V data, Proceedings of SPIE International Symposia on MEMS, Adelaide, Australia, pp. 252–256 (2001)
71. W. Huang, Z. Ren, C. Nguyen: Nickel vibrating micromechanical disk resonator with solid dielectric capacitive-transducer gap, Proceedings of the 2006 International Frequency Control Symposium and Exposition (IFCS'06), Piscataway, NJ, pp. 839–847 (2006)
72. C. Carraro, L. Magagnin, R. Maboudian: Selective metallization of Si micromechanical devices, Electrochim. Acta 47, 2583–2588 (2002)
73. J. Salber, S. Gräter, M. Harwardt, M. Hofmann, D. Klee, J. Dujic, J.H. Huang, J.D. Ding, S. Kippenberger, A. Bernd, J. Groll, J.P. Spatz, M. Möller: Influence of different ECM mimetic peptide sequences embedded in a nonfouling environment on the specific adhesion of human-skin keratinocytes and fibroblasts on deformable substrates, Small 3, 1023–1031 (2007)
74. J.K. Liu, T. Pan, A.T. Woolley, M.L. Lee: Surface-modified poly(methyl methacrylate) capillary electrophoresis microchips for protein and peptide analysis, Anal. Chem. 76, 6948–6955 (2004)
75. J. Gao, J. Xu, L.E. Locascio, C.S. Lee: Integrated microfluidic system enabling protein digestion, peptide separation, and protein identification, Anal. Chem. 73, 2648–2655 (2001)
76. K.L. Prime, G.M. Whitesides: Self-assembled organic monolayers – model systems for studying adsorption of proteins at surfaces, Science 252, 1164–1167 (1991)

77. C.D. Bain, H.A. Biebuyck, G.M. Whitesides: Comparison of self-assembled monolayers on gold – coadsorption of thiols and disulfides, Langmuir 5, 723–727 (1989)
78. J.M. Buriak: Organometallic chemistry on silicon surfaces: Formation of functional monolayers bound through Si-C bonds, Chem. Commun. 1051–1060 (1999)
79. M.J. Moorcroft, W.R.A. Meuleman, S.G. Latham, T.J. Nicholls, R.D. Egeland, E.M. Southern: In situ oligonucleotide synthesis on poly(dimethylsiloxane): A flexible substrate for microarray fabrication, Nucleic Acids Res. 33, e75 (2005)
80. D.C. Duffy, J.C. McDonald, O.J.A. Schueller, G.M. Whitesides: Rapid prototyping of microfluidic systems in poly(dimethylsiloxane), Anal. Chem. 70, 4974–4984 (1998)
81. P.T. Charles, G.J. Vora, J.D. Andreadis, A.J. Fortney, C.E. Meador, C.S. Dulcey, D.A. Stenger: Fabrication and surface characterization of DNA microarrays using amine- and thiol-terminated oligonucleotide probes, Langmuir 19, 1586–1591 (2003)
82. L. Jin, A. Horgan, R. Levicky: Preparation of end-tethered DNA monolayers on siliceous surfaces using heterobifunctional cross-linkers, Langmuir 19, 6968–6975 (2003)
83. J.S. Lee, E. Um, J.K. Park, C.B. Park: Microfluidic self-assembly of insulin monomers into amyloid fibrils on a solid surface, Langmuir 24, 7068–7071 (2008)
84. J.W. Li, W.J. Xie, N. Fang, E.S. Yeung: Single-molecule immunosorbent assay as a tool for human immunodeficiency virus-1 antigen detection, Anal. Bioanal. Chem. 394, 489–497 (2009)
85. K.L. Davis, B.J. Drews, H. Yue, D.H. Waldeck, K. Knorr, R.A. Clark: Electron-transfer kinetics of covalently attached cytochrome c/SAM/Au electrode assemblies, J. Phys. Chem. C, 112, 6571–6576 (2008)
86. C.-Y. Lee, P.-C.T. Nguyen, D.W. Grainger, L.J. Gamble, D.G. Castner: Structure and DNA hybridization properties of mixed nucleic acid/maleimide-ethylene glycol monolayers, Anal. Chem. 79, 4390–4400 (2007)
87. J.A. Neff, P.A. Tresco, K.D. Caldwell: Surface modification for controlled studies of cell-ligand interactions, Biomaterials 20, 2377–2393 (1999)
88. M.J. O'Donnell, K. Tang, H. Koster, C.L. Smith, C.R. Cantor: High density, covalent attachment of DNA to silicon wafers for analysis by MALDI-TOF mass spectrometry, Anal. Chem. 69, 2438–2443 (1997)
89. T. Bocking, K.A. Killan, K. Gaus, J.J. Gooding: Single-step DNA immobilization on antifouling self-assembled monolayers covalently bound to silicon (111), Langmuir 22, 3494–3496 (2006)
90. E. Eteshola, D. Leckband: Development and characterization of an ELISA assay in PDMS microfluidic channels, Sens. Actuators B, 72, 129–133 (2001)
91. M.F. Templin, D. Stoll, J.M. Schwenk, O. Potz, S. Kramer, T.O. Joos: Protein microarrays: Promising tools for proteomic research, Proteomics 3, 2155–2166 (2003)
92. D. Peelen, V. Kodoyianni, J. Lee, T. Zheng, M.R. Shortreed, L.M. Smith: Specific capture of mammalian cells by cell surface receptor binding to ligand immobilized on gold thin films, J. Proteome Res. 5, 1580–1585 (2006)
93. H.-Y. Hsieh, P.-C. Wang, C.-L. Wu, C.-W. Huang, C.-C. Chieng, F.-G. Tseng: Effective enhancement of fluorescence detection efficiency in protein microarray assays: Application of a highly fluorinated organosilane as the blocking agent on the background surface by a facile vapor-phase deposition process, Anal. Chem. 81, 7908–7916 (2009)
94. W.T. Johnson: Attaching antibodies to AFM probes with sulfhydryl reactive PEG tether, NHS-PEG18-PDP, Agilent Technologies Application Note (2007)
95. A. Ebner, L. Wildling, A.S.M. Kamruzzahan, C. Rankl, J. Wruss, C.D. Hahn, M. Hölzl, R. Zhu, F. Kienberger, D. Blaas, P. Hinterdorfer, H.J. Gruber: A new, simple method for linking of antibodies to atomic force microscopy tips, Bioconjug. Chem. 18, 1176–1184 (2007)
96. T.V. Ratto, K.C. Langry, R.E. Rudd, R.L. Balhorn, M.J. Allen, M.W. McElfresh: Force spectroscopy of the double-tethered concanavalin-A mannose bond, Biophys. J. 86, 2430–2437 (2004)

97. B.T. Houseman, J.H. Huh, S.J. Kron, M. Mrksich: Peptide chips for the quantitative evaluation of protein kinase activity, Nat. Biotechnol. 20, 270–274 (2002)
98. O. Akbulut, A.A. Yu, F. Stellacci: Fabrication of biomolecular devices via supramolecular contact-based approaches, Chem. Soc. Rev. 39, 30–37 (2010)
99. Z.Y. Huang, P.-C. Wang, A.G. MacDiarmid, Y.N. Xia, G.M. Whitesides: Selective deposition of conducting polymers on hydroxyl-terminated surfaces with printed monolayers of alkylsiloxanes as templates, Langmuir 13, 6480–6484 (1997)
100. E. Menard, M.A. Meitl, Y.G. Sun, J.U. Park, D.J.L. Shir, Y.S. Nam, S. Jeon, J.A. Rogers: Micro- and nanopatterning techniques for organic electronic and optoelectronic systems, Chem. Rev. 107, 1117–1160 (2007)
101. M. Geissler, Y.N. Xia: Patterning: Principles and some new developments, Adv. Mater., 16, 1249–1269 (2004)
102. A.P. Quist, E. Pavlovic, S. Oscarsson: Recent advances in microcontact printing, Anal. Bioanal. Chem. 381, 591–600 (2005)
103. S.A. Ruiz, C.S. Chen: Microcontact printing: A tool to pattern, Soft Matter 3, 168–177 (2007)
104. P.-C. Wang, R.E. Lakis, A.G. MacDiarmid: Morphology-correlated electrical conduction in micro-contact-printed polypyrrole thin films grown by in situ deposition, Thin Solid Films, 516, 2341–2345 (2008)
105. Y.N. Xia, G.M. Whitesides: Soft lithography, Annu. Rev. Mater. Sci. 28, 153–184 (1998)
106. R.S. Kane, S. Takayama, E. Ostuni, D.E. Ingber, G.M. Whitesides: Patterning proteins and cells using soft lithography, Biomaterials 20, 2363–2376 (1999)
107. C.S. Chen, M. Mrksich, S. Huang, G.M. Whitesides, D.E. Ingber: Geometric control of cell life and death, Science 276, 1425–1428 (1997)
108. E. Hecht: Optics, 4th edn (Addison Wesley, San Francisco, CA, 2002)
109. W.J. Smith: Modern Optical Engineering, 4th edn (McGraw-Hill, New York, NY, 2008)
110. P.H. Lissberger: Optical applications of dielectric thin films, Rep. Prog. Phys. 33, 197–268 (1970)
111. U. Schulz: Review of modern techniques to generate antireflective properties on thermoplastic polymers, Appl. Opt. 45(7), 1608–1618 (2006)
112. Georgia State University, Fresnel's Equations, http://hyperphysics.phy-astr.gsu.edu/Hbase/phyopt/freseq.html (accessed in 2009)
113. S.J. Wilson, M.C. Hutley: The optical-properties of moth eye antireflection surfaces, Opt. Acta 29(7), 993–1009 (1982)
114. P.B. Clapham, M.C. Hutley: Reduction of lens reflection by moth eye principle, Nature 244(5414), 281–282 (1973)
115. T. Ootsuka, Z. Liu, M. Osamura et al.: Studies on aluminum-doped ZnO films for transparent electrode and antireflection coating of [beta]-$FeSi_2$ optoelectronic devices, Thin Solid Films 476(1), 30–34 (2005)
116. B. MacLeod, G. Sonek: Motheye surfaces reflect little light, Laser Focus World 35(8), 109–113 (1999)
117. D.H. Raguin, G.M. Morris: Antireflection structured surfaces for the infrared spectral region, Appl. Opt. 32(7), 1154–1167 (1993)
118. D.H. Raguin, G.M. Morris: Analysis of antireflection-structured surfaces with continuous one-dimensional surface profiles, Appl. Opt. 32(14), 2582–2598 (1993)
119. R.B.M. Schasfoort, A.J. Tudos: Handbook of Surface Plasmon Resonance (RSC Publishing, Cambridge, 2008)
120. E. Kretschmann: Z. Phys. 241, 313 (1971)
121. Lukas Novotny, Bert Hecht: Principle of Nano-optics (University Press, Cambridge, 2006)
122. B. Liedberg, C. Nylander, I. Lundstrom: Sens. Actuators, 4, 299–304 (1983)
123. N. W. Ashcroft and N.D. Mermin: Solid State Physics (Saunders College Publishing, Philadelphia, PA, 1976)

124. H. Raether: Surface Plasmons on Smooth and Rough Surfaces and on Gratings, Springer Tracts in Modern Physics, vol. 11 (Springer, Berlin, Heidelberg, 1988)
125. K.Y. Hung, J.C. Liao: The application of Fresnel equations and anti-reflection technology to improve inclined exposure interface reflection and develop a key component needed for Blu-ray DVD-micro-mirrors, J. Micromech. Microeng. 18(7), 9 (2008)
126. M. Li, P.S. Chung, M.T. Yeung, P.S. Chan, T.K. Liang, C. Shu, K.W.C. Lai, W.J. Li, F. Tong, H.K. Tsang: Mirror Coating and Packaging for a Horizontal MEMS Optical Switch Array, Proceedings of the 54th Electronic Components and Technology Conference, vol. 2, pp. 1400–1405 (2004)
127. H.A. Macleod: Thin-Film Optical Filters (Hilger, Bristol, UK, 1986)
128. Y. Kanamori, K. Hane: Broadband antireflection subwavelength gratings for polymethyl methacrylate fabricated with molding technique, Opt. Rev. 9(5), 183–185 (2002)
129. R. Bilyalov, L. Stalmans, J. Poortmans: Comparative analysis of chemically and electrochemically formed porous Si antireflection coating for solar cells, J. Electrochem. Soc. 150(3), G216–G222 (2003)
130. C.L. Tseng, M.J. Youh, G.P. Moore et al.: Mechanism for the increased light transmission through Ni/Au/ZnO contacts on p-GaN for high power optoelectronic devices, Appl. Phys. Lett. 83(18), 3677–3679 (2003)
131. K.Y. Hung, H.T. Hu, F.G. Tseng: Application of 3D glycerol-compensated inclined-exposure technology to an integrated optical pick-up head, J. Micromech. Microeng. 14(7), 975–983 (2004)
132. K.Y. Hung, F.G. Tseng, H.P. Chou: Application of 3D gray mask for the fabrication of curved SU-8 structures, Microsyst. Technol. 11(4–5), 3 (2005)
133. K.Y. Hung, F.G. Tseng, T.H. Liao: Electrostatic-force-modulated microaspherical lens for optical pickup head, J. Microelectromech. Syst. 17(2), 370–380 (2008)
134. K.Y. Hung, T.H. Liang: Application of inclined-exposure and thick film process for high aspect-ratio micro-structures on polymer optic devices, Microsyst. Technol. 14(9–11), 1217–1222 (2008)
135. B.C. Chakravarty, J. Tripathi, A.K. Sharma et al.: The growth kinetics and optical confinement studies of porous Si for application in terrestrial Si solar cells as antireflection coating, Sol. Energy Mater. Sol. Cells 91(8), 701–706 (2007)
136. T.L. Chu, S.S. Chu, J. Britt et al.: 14.6% efficient thin-film cadmium telluride heterojunction solar cells, IEEE Electron Dev. Lett. 13(5), 303–304 (1992)
137. Z. Chen, P. Sana, J. Salami et al.: A novel and effective PECVD SiO_2/SiN antireflection coating for Si solar cells, IEEE Trans. Electron Dev. 40(6), 1161–1165 (1993)
138. P. Menna, G. Di Francia, V. La Ferrara: Porous silicon in solar cells: A review and a description of its application as an AR coating, Sol. Energy Mater. Sol. Cells 37(1), 13–24 (1995)
139. A. Krotkus, K. Grigoras, V. Pacebutas et al.: Efficiency improvement by porous silicon coating of multicrystalline solar cells, Sol. Energy Mater. Sol. Cells 45(3), 267–273 (1997)
140. D. Bouhafs, A. Moussi, A. Chikouche et al.: Design and simulation of antireflection coating systems for optoelectronic devices: Application to silicon solar cells, Sol. Energy Mater. Sol. Cells 52, 79–93 (1998)
141. S.G.F. de, S. Alves Jr, B.J.P. da Silva et al.: A novel fluorinated Eu(III) [beta]-diketone complex as thin film for optical device applications, Opt. Mater. 11(1), 23–28 (1998)
142. R.R. Bilyalov, L. Stalmans, L. Schirone et al.: Use of porous silicon antireflection coating in multicrystalline silicon solar cell processing, IEEE Trans. Electron Devices 46(10), 2035–2040 (1999)
143. R.R. Bilyalov, R. Ludemann, W. Wettling et al.: Multicrystalline silicon solar cells with porous silicon emitter, Sol. Energy Mater. Sol. Cells 60, 391–420 (2000)
144. B.S. Richards: Single-material TiO_2 double-layer antireflection coatings, Sol. Energy Mater. Sol. Cells 79, 369–390 (2003)
145. U. Gangopadhyay, K. Kim, D. Mangalaraj et al.: Low cost CBD ZnS antireflection coating on large area commercial mono-crystalline silicon solar cells, Appl. Surf. Sci. 230(1–4), 364–370 (2004)

146. J. Lee: Comparison of CdS films deposited by different techniques: Effects on CdTe solar cell, Appl. Surf. Sci. 252(5), 1398–1403 (2005)
147. G. Crotty, T. Daud, R. Kachare: Front surface passivation of silicon solar cells with antireflection coating, J. Appl. Phys. 61(8), 3077–3079 (1987)
148. U. Schulz, K. Lau, N. Kaiser: Antireflection coating with UV-protective properties for polycarbonate, Appl. Opt. 47(13), C83–C87 (2007)
149. M.H. Lee, J.S. Cho: Better thermochromic glazing of windows with anti-reflection coating, Thin Solid Films 365(1), 5–6 (2000)
150. R.R. Phillips, V. Haynes, D.A. Naylor et al.: Simple method for antireflection coating ZnSe in the 20 μm wavelength range, Appl. Opt. 47(7), 870–873 (2008)
151. U. Schulz: Review of modern techniques to generate antireflective properties on thermoplastic polymers, Appl. Opt. 45(7), 1608–1618 (2006)
152. A. Gombert, W. Glaubitt, K. Rose et al.: Subwavelength-structured antireflective surfaces on glass, Thin Solid Films 351, 73–78 (1999)
153. A. Kaless, U. Schulz, P. Munzert et al.: NANO-motheye antireflection pattern by plasma treatment of polymers, Surf. Coat. Technol., 200(1–4), 58–61 (2005)
154. T. Sawitowski, N. Beyer, F. Schulz: Bio-inspired anti-reflective surfaces by imprinting processes, in The Nano-Micro Interfaces, pp. 263–280 (H.-J.Fecht, M. Werner (Eds.) Wiley-VCH, Weinheim, 2004)
155. M.-H. Chen, Y.-J. Chuang, F.-G. Tseng: Fabrication of superhydrophobic surface by nanomolding, In Proceedings of μTAS conference, Tokyo, Japan, pp. 161–163 (2006)
156. F. Brumeister, W. Doell, G. Kleer: Method for producing a tool which can be used to create structures in the sub-micrometer range, EP1307604B1, E. Patent (1998)
157. M.S. Park, Y. Lee, J.K. Kim: One-step preparation of antireflection film by spin-coating of polymer/solvent/nonsolvent ternary system, Chem. Mater. 17(15), 3944–3950 (2005)
158. S. Walheim, E. Schaffer, J. Mlynek et al.: Nanophase-separated polymer films as high-performance antireflection coatings, Science 283(5401), 520–522 (1999)
159. J. Hiller, J.D. Mendelsohn, M.F. Rubner: Reversibly erasable nanoporous anti-reflection coatings from polyelectrolyte multilayers, Nat. Mater. 1(1), 59–63 (2002)
160. M. Ibn-Elhaj, M. Schadt: Optical polymer thin films with isotropic and anisotropic nano-corrugated surface topologies, Nature 410(6830), 796–799 (2001)
161. H.Y. Koo, D.K. Yi, S.J. Yoo et al.: A snowman-like array of colloidal dimers for antireflecting surfaces, Adv. Mater. 16(3), 274 (2004)
162. M.H. Chen, Y.J. Chuang, F.G. Tseng: Self-masked high-aspect-ratio polymer nanopillars, Nanotechnology 19(50), 7 (2008)
163. M.W. Lin, B. Chao, J. Hao et al.: Simulation and design of planarizing materials for reverse-tone step and flash imprint lithography, J. Micro/Nanolithography, MEMS MOEMS 7(2), 023008-19 (2008)
164. N. Liu, H. Guo, L. Fu et al.: Three-dimensional photonic metamaterials at optical frequencies, Nat. Mater. 7(1), 31–37 (2008)
165. G. Subramania, S.Y. Lin: Fabrication of three-dimensional photonic crystal with alignment based on electron beam lithography, Appl. Phys. Lett. 85(21), 5037–5039 (2004)
166. Y.S. Yoon, K.D. Bae, J.H. Kim et al.: A low voltage actuated micromirror with an extra vertical electrode for 90° rotation, J. Micromech. Microeng. 13(6), 922–926 (2003)
167. C.J. Chen, K.K. Choi, W.H. Chang et al.: Corrugated quantum well infrared photodetectors with polyimide planarization for detector array applications, IEEE Trans. Electron Dev. 45(7), 1431–1437 (1998)
168. M.H. Schuck, D.J. McKnight, K.M. Johnson: Spin-cast planarization of liquid-crystal-on-silicon microdisplays, Opt. Lett. 22(19), 1512–1514 (1997)
169. E. Breval, M.L. Mulvihill, J.P. Dougherty et al.: Polyimide-silica microcomposite films, J. Mater. Sci. 27, 3297–3300 (1992)
170. V.J. Logeeswaran, M.L. Chan, Y. Bayam et al.: Ultra-smooth metal surfaces generated by pressure-induced surface deformation of thin metal films, Appl. Phys. A: Mater. Sci. Process. 87(2), 187–192 (2007)

171. M.-C.M. Lee, M.C. Wu: Thermal annealing in hydrogen for 3-D profile transformation on silicon-on-insulator and sidewall roughness reduction, J. Microelectromech. Syst. 15(2), 338–343 (2006)
172. R.R.A. Syms, A.S. Holmes: Reflow and burial of channel waveguides formed in sol-gel glass on Si substrates, IEEE Photon. Technol. Lett. 5(9), 1077–1079 (1993)
173. P.B. Mirkarimi, E. Spiller, S.L. Baker et al.: Developing a viable multilayer coating process for extreme ultraviolet lithography reticles, J. Microlithography, Microfabrication, Microsyst. 3(1), 139–145 (2004)
174. F. Frost, R. Fechner, D. Flamm et al.: Ion beam assisted smoothing of optical surfaces, Appl. Phys. A: Mater. Sci. Process. 78(5), 651–654 (2004)
175. C. Vivensang, L. Ferlazzo-Manin, M.F. Ravet et al.: Surface smoothing of diamond membranes by reactive ion etching process, Diam. Relat. Mater. 5(6–8), 840–844 (1996)
176. S. Ilias, G. Sen, P. Moller et al.: Planarization of diamond thin film surfaces by ion beam etching at grazing incidence angle, Diam. Relat. Mater. 5(6–8), 835–839 (1996)
177. U. Schulz, N. Kaiser: Vacuum coating of plastic optics, Progr. Surf. Sci. 81(8–9), 387–401 (2006)
178. K. Minami: Optical plastics, in Hanbook of Plastic Optics, pp. 109–147 (S. Baumer (Ed.) Wiley-VCH, Frankfurt, 2005)
179. H. Chatham: Oxygen diffusion barrier properties of transparent oxide coatings on polymeric substrates, Surf. Coat. Technol. 78(1–3), 1–9 (1996)
180. F. Samson: Ophthalmic lens coatings, Surf. Coat. Technol. 81(1), 79–86 (1996)
181. S. Pongratz, A. Zoller: Plasma ion-assisted evaporative deposition of surface-layers, Annu. Rev. Mater. Sci. 22, 279–295 (1992)
182. S.A. Mohan, M.A. Ghanashyam Krishna: A review of ion beam assisted deposition of optical thin films, Vacuum 46(7), 645–659 (1995)
183. P. Munzert, U. Schulz, N. Kaiser: Transparent thermoplastic polymers in plasma-assisted coating processes, Surf. Coat. Technol. 174–175, 1048–1052 (2003)
184. M. Kuhr, S. Bauer, U. Rothhaar et al.: Coatings on plastics with the PICVD technology, Thin Solid Films 442, 107–116 (2003)
185. G. Dennler, A. Houdayer, M. Latreche et al.: Studies of the earliest stages of plasma-enhanced chemical vapor deposition of SiO_2 on polymeric substrates, Thin Solid Films 382(1–2), 1–3 (2001)
186. A. Hofrichter, A. Constantinescu, S. Benayoun et al.: Study of the mechanical behavior of plasma-deposited silica films on polycarbonate and steel, J. Vac. Sci. Technol. 18, 2012–2016 (2000)
187. D. Poitras, L. Martinu: Interphase in plasma-deposited films on plastics: Effect on the spectral properties of optical filters, Appl. Opt. 39(7), 1168–1173 (2000)
188. R. Kukla, D. Hofmann, G. Ickes et al.: Sputter metallization of plastic parts in a just-in-time coater, Surf. Coat. Technol. 74–75(1–3), 648–653 (1995)
189. H. Grunwald, R. Adam, J. Bartella et al.: Better aluminum mirrors by integrating plasma pretreatment, sputtering, and plasma polymerization for large-scale car headlight production, Surf. Coat. Technol. 111(2–3), 287–296 (1999)
190. C.-L. Wu, M.-H. Chen, F.-G. Tseng: SU-8 hydrophilic modification by forming copolymer with hydrophilic epoxy molecule, In Proceedings of μTAS, Squaw Valley, CA, pp. 1117–1120 (2003)
191. H.S. Khoo, F.-G. Tseng: Morphological controlled growth of three-dimensional self-assembled methylsiloxane films: Their impact on hydrophobic behaviors, Nanotechnology 19, 345603–345612 (2008)
192. F. Garbassi, M. Morra, E. Occhiello: Polymer Surfaces (Wiley-VCH, Weinheim, 1998)
193. F.-G. Tseng, K.-H. Lin, H.-T. Hsu et al.: A surface-tension-driven fluidic network for precise enzyme batch-dispensing and glucose detection, Sens. Actuators A 111, 107–117 (2004)
194. C.E. Ho, F.G. Tseng, S.C. Lin et al.: Characterization of the surface tension and viscosity effects on the formation of nano-liter droplet arrays by an instant protein micro stamper, J. Micromech. Microeng. 15, 2317–2325 (2005)

195. C.-E. Ho, C.-C. Chieng, M.-H. Chen et al.: Rapid micro array system for passive batch-filling and in-parallel-printing protein solutions, J. Microelectromech. Syst. 17(2), 309–317 (2008)
196. U. Schulz: Coating on Plastics, in Handbook of Plastic Optics, pp. 149–180 (S. Baumer (Ed.) Wiley-VCH, Frankfurt, 2005)
197. O. Chiantore, L. Trossarelli, M. Lazzari: Photooxidative degradation of acrylic and methacrylic polymers, Polymer 41(5), 1657–1668 (2000)
198. G. Schottner, K. Rose, U. Posset: Scratch and abrasion resistant coatings on plastic lenses – State of the art, current developments and perspectives, J. Sol-Gel Sci. Technol. 27(1), 71–79 (2003)
199. Y.-T. Tseng, C.-S. Yang, Y.-C. Wu, M.-C. Wang, F.-G. Tseng: Gold-nanoparticle enhanced in-situ immunosensor based on fiber-optical fabry-perot interferometry, Nanotechnology 19, 345501–345510 (2008)
200. Yuan-Tai Tseng, Chung-Shi Yang, Fan-Gang Tseng: A perfusion-based micro opto-fluidic system (PMOFS) for continuously in-situ immune sensing, Lab Chip 9, 2673–2682 (2009)
201. Y.J. Chuang, F.G. Tseng, J.H. Cheng et al.: A novel fabrication method of SU-8 stacked micro channels by UV dosage control, Sens. Actuators A 103, 64–69 (2003)
202. S.H. Huang, W.H. Tan, F.G. Tseng et al.: A monolithically three-dimensional flow-focusing device for formation of single/double emulsions in closed/open microfluidic systems, J. Micromech. Microeng. 16(11), 2336–2344 (2006)
203. L. Holland: The Properties of Glass Surfaces (Chapman & Hall, London, 1964)
204. T. Izumitani: Treatise on Materials Science and Technology (Academic, New York, NY, 1979)
205. L.M. Cook: Chemical processes in glass polishing, J. Non-Cryst. Solids 120, 152–171 (1990)
206. H. Dunken: Surface chemistry of optical glasses, J. Non-Cryst. Solids 129, 64–75 (1991)
207. T. Hoshino, Y. Kurata, Y. Terasaki et al: Mechanism of polishing of SiO_2 films by CeO_2 particles, J. Non-Cryst. Solids 283, 129–136 (2001)
208. J.M. Steigerwald, S.P. Murarka, R.J. Gutmann: Chemical Mechanical Planarization of Microelectronic Materials (Wiley, New York, NY, 1997)
209. T. Du, D. Tamboli, V. Desai et al.: Mechanism of copper removal during CMP in acidic H2O2 slurry, J. Electrochem. Soc. 151, G230–G235 (2004)
210. D.H. Eom, I.K. Kim, J.H. Han et al.: The effect of hydrogen peroxide in a citric acid based copper slurry on Cu polishing, J. Electrochem. Soc. 154, 38–44 (2007)
211. A. Ishikawa, H. Matsuo, T. Kikkawab: Influence of slurry chemistry on frictional force in copper chemical mechanical polishing, J. Electrochem. Soc. 152, G695–G697 (2005)
212. K. Ludema: Friction, Wear and lubrication: A Textbook in Tribology (CRC Press, New York, NY, 1996)
213. B. Bhushan: Introduction to Tribology (Wiley, New York, NY, 2002)
214. F. Preston: The theory and design of plate glass polishing machines, J. Soc. Glass Technol. 11, 214 (1927)
215. J.J. Brown, P.C. Baker, R.T. Maney: Optical polishing of metals, Proc. SPIE 306, 42–57 (1981)
216. O. Seunghee, S. Jongwon: An integrated material removal model for silicon dioxide layers in chemicalmechanical polishing processes, Wear 266, 839–849 (2009)
217. J.S. David, L.H. Dale, L.C. Joseph: Investigation of the kinetics of tungsten chemical mechanical polishing in potassium iodate-based slurries I. Role of alumina and potassium iodate, J. Electrochem. Soc. 146, 376–381 (1999)
218. Q. Luo, S. Ramarajan, S.V. Babu: Modification of the Preston equation for the chemical-mechanical polishing of copper, Thin Solid Films 335, 160–167 (1998)
219. R. Stribeck: Characteristics of plain and roller bearing, Zeit Ver Deut Ing 46, 1341–1348 (1902)

220. Z. Li, K. Ina, P. Lefevre et al.: Determining the effects of slurry surfactant, abrasive size, and abrasive content on the tribology and kinetics of copper CMP, J. Electrochem. Soc. 152, G299–G304 (2005)
221. Y.C. Wang, T. Shiang: Effects of pad grooves on chemical mechanical planarization, J. Electrochem. Soc. 154, H486–H494 (2007)
222. A. Philipossian, S. Olsen: Fundamental tribological and removal rate studies of interlayer dielectric chemical mechanical planarization, Jpn J. Appl. Phys. 42, 6371–6379 (2003)
223. M.R. Oliver: Chemical-Mechanical Planarization of Semiconductor Materials (Springer, New York, NY, 2004)
224. S. Sivaram, K. Monnig, R. Tolles et al.: Overview of planarization by mechanical polishing of interlevel dielectrics. Proceedings of the 3rd International Symposium on ULSI Science and Technology, Pennington, NJ, The Eletrochemical Society Inc., pp. 606–616 (1991)
225. M.R. Oliver: Chemical-Mechanical Planarization of Semiconductor Materials, pp. 285–349 (Springer, New York, NY, 2004)
226. Peter Wolters, Internet web site, http://www.peter-wolters.com/cmp/cmpmultilevel.htm (accessed in 2009)
227. J.Q. Lu, G. Rajagopalan, M. Gupta, T.S. Cale, R.J. Gutmann: Planarization issues in wafer-level three-dimensional (3D) integration, MRS Symposium Proceedings, 816, pp. 217–228 (2004)
228. Y.Z. Li: Microelectronic Applications of Chemical–Mechanical Planarization (Wiley, NJ, 2007)
229. S. Armini, C.M. Whelan, M. Moinpour et al.: Copper CMP with composite polymer core–silica shell abrasives: A defectivity study, J. Electrochem. Soc. 156, H18–H26 (2009)
230. M. Masayuki, K. Nobuo: Method of Chemical Mechanical Polishing, USA, JSR Corporation, US007153369B2 (2006)
231. J.M. Steigerwald, R. Zirpoli, S.P. Murarka et al.: Pattern geometry effects in the chemical-mechanical polishing of inlaid copper structures, J. Electrochem. Soc. 141, 2842–2848 (1994)
232. P. Holzapfel, K. Murella, J. Schlueter et al.: VMIC Conference, IMIC, Tampa, p. 307 (1997)
233. M.R. Oliver: Chemical-Mechanical Planarization of Semiconductor Materials, pp. 373–386 (Springer, New York, NY, 2004)
234. C. Oji, B. Lee, D. Ouma et al.: Wafer scale variation of planarization length in chemical mechanical polishing, J. Electrochem. Soc. 147, 4307–4312 (2000)
235. C.H. Yao, D.L. Feke, K.M. Robinson et al.: Modeling of chemical mechanical polishing processes using a discretized geometry approach, J. Electrochem. Soc. 147, 1502–1512 (2000)
236. C.H. Yao, D.L. Feke, K.M. Robinson et al.: The influence of feature-scale surface geometry on CMP processes, J. Electrochem. Soc. 147, 3094–3099 (2000)
237. R.R. Divecha., B.E. Stine, D.O. Ouma et al.: A novel statistical metrology framework for identifying sources of variation in oxide chemical-mechanical polishing, J. Electrochem. Soc. 145, 1052–1059 (1998)
238. A.E. Braun: Copper metrology, gain complexity, capabilities, Semicond. Int. 24, 56–58, 60, 64, & 70 (2001)
239. J.F. Simon, G. Santos, H.L. Guo et al.: Optimization of the chemical mechanical polishing process for premetal dielectrics, J. Electrochem. Soc. 147, 682–286 (2000)
240. R.L. Rhoades: Rapid low-cost development of a planarized 3-level interconnect module, Proceeding 9th International CMP-MIC, Los Angeles, CA (Feb. 2004)
241. M.R. Oliver: Chemical-Mechanical Planarization of Semiconductor Materials, pp. 404–407 (Springer, New York, NY, 2004)
242. B. Ziaie, A. Baldi, M. Lei et al.: Hardand soft micromachining for BioMEMS: Review of techniques and examples of applications in microfluidics and drug delivery, Adv. Drug Deliv. Rev. 56, 145–172 (2004)

243. B.H. Veigl, R.L. Bardell, C.R. Cabrera: Lab-on-a-chip for drug development, Adv. Drug Deliv. Rev. 55, 349–377 (2003)
244. R.K. Singh, F.C. Chang, S. Tanawade, G. Scheiffele: Effect of pump induced particle agglomeration on CMP of ultra low k dielectrics, Levitronix CMP Users Conference (2006) http://www.levitronix.com/Levitronix_Conference_Papers.html
245. J.D. Larios, J. Zhang, E. Zhao et al.: Evaluating chemical mechanical cleaning technology for post CMP applications, Micro 5, 61 (1997)
246. N. Junji, K. Nobuhiro, Y. Youhei: Influence of post-CMP cleaning on Cu interconnects and TDDB reliability, IEEE Trans. Electron Dev. 52, 934–941 (2005)
247. A. Hu, X. Zhang, E. Sachs, P. Penteln: Application of Run by Run Controller to the Chemical-Mechanical Planarization Process, Part I, IEEE Proceeding of the 15th International Electronics Manufacturing Technology Symposium, pp. 235–240 (1993)
248. J. Luo, D.A. Dornfeld: Effects of abrasive size distribution in chemical mechanical planarization: Modeling and verification, IEEE Trans. Semicond. Manuf. 16, 469–476 (2003)
249. Y.K. Hong, D.H. Eom, S.H. Lee et al.: The effect of additives in post-Cu CMP cleaning on particle adhesion and removal, J. Electrochem. Soc. 151, G756–G761 (2004)
250. M.A. Michalicek, J.H. Comtois, C.C. Barren: Design and Characterization of Next-Generation Micromirrors Fabricated in a Four-Level, Planarized Surface-Micromachined Polycrystalline Silicon Process, Proceedings of 2nd Annual IEEE International Conference on Innovative Systems in Silicon, pp. 144–154 (Austin, TX, USA, 1997)
251. J.J. Sniegowski, M.S. Rodgers: Multi-Layer Enhancement to Polysilicon Surface-Micromachining Technology, International Electron Devices Meeting (IEDM), Technical Digest, vol. 8, pp. 903–906 (Washington, DC , USA, 1997)
252. H. Lin, A.J. Walton, C.C. Dunare et al.: Test Structures for the Characterization of MEMS and CMOS Integration Technology, IEEE Transactions on Semiconductor Manufacturing 21, pp. 140–147 (2008)
253. V. Bhatt, S. Chandra: Planar Microstructures in Surface Micromachining Process Using RF Sputtered ZnO as Sacrificial Layer, Optoelectronic and Microelectronic Materials and Devices Conference, pp. 129–132 (Perth, Australia, 2006)
254. S. Zairi, G.Y. Tian: Design of Buried Hinge Based 3D Torsional Micro Mirrors, Proceedings of the Sixth IEEE CPMT Conference on High Density Microsystem Design and Packaging and Component Failure Analysis, pp. 164–170 (Shanghai, China, 2004)
255. A.A. Yasseen, C. Wu, C.A. Zorman, M. Mehregany: Fabrication and testing of surface micromachined silicon carbide micromotors, J. Microelectromech. Syst. 644–649 (1999)
256. A.A. Yasseen, C. Wu, C.A. Zorman et al.: A design methodology for a bulk-micromachined two-dimensional electrostatic torsion micromirror, J. Microelectromech. Syst. 12, 692–701 (2003)
257. U. Krishnamoorthy, L. Daesung, O. Solgaard: Self-aligned vertical electrostatic combdrives for micromirror actuation, J. Microelectromech. Syst. 12, 458–464 (2003)
258. Q. Ramadan, V.D. Samper, D.P. Puiu et al.: Fabrication of three-dimensional magnetic microdevices with embedded microcoils for magnetic potential concentration, J. Microelectromech. Syst. 15, 624–638 (2006)
259. S. Merzaghi, P. Meyer, Y. Perriard: Development of Planar Microcoils for an Electromagnetic Linear Actuator Fabricated in Batch-Type Wafer Technology, pp. 1–6 (IEEE, Edmonton, Canada, 2008)
260. Y. Li, K. Baek, M. Gulari et al.: A Drug-Delivery Probe with an In-Line Flowmeter Based on Trench Refill and Chemical Mechanical Polishing Techniques, IEEE Sensors Conference, pp. 1144–1147 (Atlanta, GA, 2007)
261. J. Chen, K.D. Wise, J.F. Hetke et al.: A multichannel neural probe for selective chemical delivery at the cellular level, IEEE Trans. Biomed. Eng. 44, 760–769 (1997)
262. P.R. Dandu Veera, A. Natarajan, S. Hegde et al.: Selective polishing of polysilicon during fabrication of microelectromechanical systems devices, J. Electrochem. Soc. 156, H487–H494 (2009)

263. C. Gui, G.J. Veldhuis, T.M. Koster, P.V. Lambeck, J.W. Berenschot, J.G.E. Gardeniers, and M. Elwenspoek: Nanomechanical optical devices fabricated with aligned wafer bonding, Eleventh Annual International Workshop on Micro Electro Mechanical Systems, MEMS, Heidelberg, Germany, 482–487 (1998)
264. C. Kourouklis, T. Kohlmeier, H.H. Gatzen: The application of chemical–mechanical polishing for planarizing a SU-8/permalloy combination used in MEMS devices, Sens. Actuators A 106, 263–266 (2003)

Chapter 14
MEMS Process Integration

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Abstract In this chapter we provide a concise understanding and appreciation of MEMS *process integration* – the technique by which processing steps are combined into an ordered sequence with the goal of creating a methodology that allows the production of functional MEMS devices with acceptable yields and cost levels. Process integration is one of the most important topics in MEMS technology because the choices made about how to produce a MEMS device have a large impact on the success or failure of any MEMS-related product development activity or business venture. This chapter describes why process integration is important in MEMS, what it entails, and how it is done. A review of the similarities and differences between MEMS and the related integrated circuit technology is provided, along with some guidance on how MEMS process sequences are successfully developed. We also review many of the most noteworthy and important MEMS process sequences and technologies that have been developed to date, showing examples both with and without microelectronics integrated with MEMS. In addition to being a general reference guide, these wide ranging examples can bolster a designer's experience base by illustrating MEMS process integration strategies that have been successfully demonstrated. A general strategy for MEMS cost analysis is also provided. We hope that we can give the reader at least a sufficient understanding to appreciate the importance of this topic with the "real-life" examples of process integration to the extent possible. The important process integration issues such as design for manufacturability is also highlighted in this chapter.

14.1 Introduction

This chapter is the culmination of the preceding chapters of this book and is directed at the extremely important topic of process integration. *Process integration* is the technique by which processing steps are combined into an ordered sequence

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with the goal of creating a methodology that allows the production of functional MEMS devices with acceptable yields and cost levels. In general, process integration involves the selection of processing steps to be used in device fabrication. But it also entails the understanding, characterizing, and optimizing of these steps and their interrelationships with the goal of having them effectively work together as a standardized production method to meet a specific acceptable performance, yield, and cost level. Process integration is one of the most important topics in MEMS technology because the choices made about how to produce a MEMS device have a large impact on the success or failure of any MEMS-related product development activity or business venture. This chapter describes why process integration is important in MEMS, what it entails, and how it is done. It also reviews a number of notable examples of successfully developed MEMS process technologies and presents some of the economic issues involved. Realistically, it is nearly impossible to teach a reader how to become a "process integration expert" in only one chapter of a book. However, our hope is that we can give the reader at least a sufficient understanding to appreciate the importance of this topic as well as highlight some of the important process integration issues that occur in any MEMS development endeavor. Our approach is to use "real-life" examples of process integration to the extent possible.

14.2 What Is Process Integration?

It is best to begin by establishing some definitions in order to help clarify the terminology. We have already defined what the term process integration means in the introduction above; let's now expand our vocabulary.

A *processing step* is defined as a single process that is performed on a substrate or a set of substrates in order to advance the fabrication of some device. This book has provided the reader with a review of a number of examples of processing types and capabilities in the previous chapters including depositions, etches, photolithography, electrochemical plating, and so on. An example of a processing step under this definition would be the deposition of polycrystalline silicon (polysilicon) on a batch of wafers using LPCVD. More exactly, the processing step would be limited to only the actual deposition of the polysilicon thin-film material on the wafers and not to the cleaning and preparation steps performed on the wafers prior to the deposition or the metrology that would be performed after the deposition was completed. The wafer cleaning and preparation steps as well as the metrology steps would rightly be considered processing steps on their own. Having said that, one must be careful because these distinctions are often made somewhat arbitrarily by many fabricators and it is common to see several steps grouped together and labeled as a process step. Using the example from above, it would be common practice to see the individual process steps of cleaning, deposition, and metrology lumped into a group and then called a process step.

A *process module* is defined as a grouping of processing steps that have been assembled into an ordered sequence and which have been characterized and standardized, and are reused on a periodic basis in the production of devices, but which is not sufficient in and of itself to result in functional devices. Therefore, under this definition a process module could be applied to anything ranging from two or more process steps up to any number of processing steps just shy of the complete fabrication of a device. Building on the example of polysilicon deposition illustrated above, the term "process module" could be used to describe the collection of the processing steps including cleaning and preparation of the wafers, followed by the deposition of polysilicon on the wafers, followed by the performance of metrology on the wafers to measure the thickness and index of refraction of the thin-film polysilicon, if this collection of processing steps or process module were used on a repeated basis for the production of devices. In practice most process modules in foundries involve the grouping of several major processing steps (e.g., deposition of polysilicon, or photolithography, etc.) and therefore would be much more complicated than merely a clean, deposition, and inspection cycle.

A *process sequence* is defined as a grouping of processing steps that have been assembled into an ordered sequence and which have been characterized and standardized, and are reused on a periodic basis in the production of devices, and which is sufficient to result in functional devices. Obviously, the distinction between a process module and process sequence is a matter of degree. A process module does not result in a functional MEMS device, whereas a process sequence does.

The term "process sequence" is frequently used interchangeably with *process technology*. For our purposes, the distinction between a process sequence and a process technology relates to its maturity, particularly in the commercial sense. A process technology is defined as a well-developed and standardized process sequence, which is used in the commercial production of devices. The term is typically applied to a process sequence developed by a research and development or academic fabrication laboratory, whereas a process technology would be used to describe the manufacturing method used to produce specific MEMS devices in a commercial foundry. Additionally, it is frequently the case that a process technology has an associated set of design rules and technology files that will aid in developing a suitable design and mask set.

Figure 14.1 is an example of a very simple process sequence for fabricating a polysilicon cantilever that is held to the substrate at one end and free on the other. This would be classified as a "polysilicon surface micromachining process sequence." This illustration shows a cross-section of the wafer at various important points in the process sequence. These types of visual aids are extremely useful for designing a process for any MEMS device and are commonly used by MEMS designers, particularly in the early stages of a development effort. These types of illustrations are also frequently used to describe many of the example process sequences that we review later in this chapter. As can be seen, the first step (Fig. 14.1a) is describing the starting wafer as a single crystal silicon wafer. Subsequently, a thermal oxide is grown on the surface of the wafer (Fig. 14.1b).

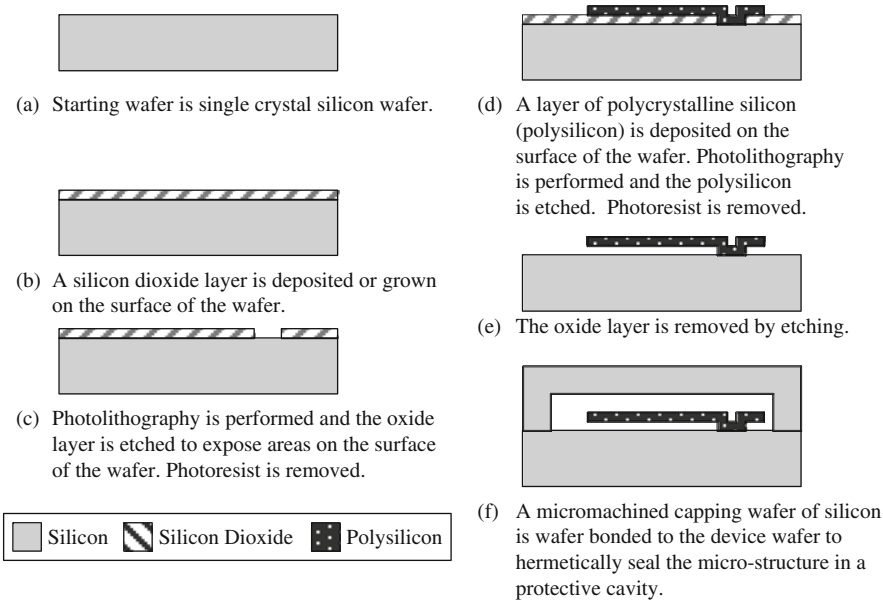


Fig. 14.1 Example of a very simple surface micromachined process sequence surface

Next, this thermal oxide layer is patterned and etched using photolithography (Fig. 14.1c) to open up areas in the oxide to expose the underlying silicon wafer surface. A layer of polycrystalline silicon (polysilicon) is then deposited on the surface of the wafer and this layer is patterned and etched in the shape of the cantilever (Fig. 14.1d). The oxide is then removed from the wafer (Fig. 14.1e) and a micromachined capping wafer is wafer bonded to the device wafer. The capping wafer has cavities cut into its surface that will encapsulate the polysilicon cantilevers (Fig. 14.1f).

The description of the above process is highly simplified and leaves out many of the important details, including: thickness of the deposited layers; depth of the etches; type of photolithography process performed to pattern the layers; what type of mask was used, or whether a mask was even used at all; as well as the critically important process step parameters. Process step parameters include the exact details of the equipment that is used to perform the process step, the temperature and chemistries used in the process step, and so on. Obviously, the fabrication of a MEMS device has many levels of detail that must be specified before implementation can begin. Process sequences are commonly defined in what are called *process runcards* or *process travelers*. These are documents that define the processing steps and modules for the fabrication of a device. The level of detail on runcards is usually sufficient to capture a high level of detail, such as process steps employed (including the identifier of the process recipe), thickness of layers, equipment that the process step is performed on, specification of the mask and wafer to be used, and the like,

but would not provide a complete and exhaustive level of detail. The higher level of detail would be implied by the specification of the process recipes and the tools to be used and these would usually be documented elsewhere. In a production-level facility, this hierarchy of documentation would be kept on a computerized manufacturing support system that would be integrated with the production equipment.

Figure 14.2 shows an example of a process runcard for the polysilicon surface micromachining process sequence described above. As can be seen, it starts with a specification of the masks to be used in the process sequence, details the wafer descriptions to be used, and then lists each of the processing steps in the process sequence, numbered Step 1 through Step 11. Some of the processing steps, such as Steps numbered 1, 2, 5, 6, and 10, are actually metaprocess steps and are composed of several individual processing steps, such as 2.1 through 2.10. A document such as this would be conveyed from the MEMS designer to the foundry to specify the fabrication of any MEMS device.

Run: Simple Surface Micromachining

Masks

Polysilicon Layer

Equipment type	contact	**Substrate material**	soda lime	**Coating**	chromium
Magnification	1.0	**Field**	bright	**Source**	customer
Length	5 inch	**Width**	5 inch	**Thickness**	0.09 inch

Oxide Layer

Equipment type	contact	**Substrate material**	soda lime	**Coating**	chromium
Magnification	1.0	**Field**	dark	**Source**	customer
Length	5 inch	**Width**	5 inch	**Thickness**	0.09 inch

Wafer Descriptions

Group 1

Number of wafers	10	**Material**	silicon	**Diameter**	150 mm
Surface finish	single side polish	**Thickness**	625 μm	**Orientation**	100
Doping type	none	**Quality**	prime	**Resistivity**	10 Ω*cm

Process Sequence

Step 1: Wet oxidation

Material	silicon dioxide	**Thickness**	1 μm ±10%

1 Piranha Clean
2 HF 10:1 Batch Etch
3 Wet oxidation
4 Spectrophotometric film thickness measurement

Instructions	1) Wafer loaded into furnace with flats up. 2) 20 point metrology

Step 2: Contact photolithography (Automated)

1 HMDS Vapor Prime
2 Photoresist Spin Coat ACS200 (AZ 5214E)
3 Photoresist Softbake ACS200
4 Edge bead removal
5 Contact flat alignment and exposure
6 Photoresist Develop (5214E)
7 Linewidth Microscope Measurement
8 Microscope inspection
9 Stylus profilometer 1-D step measurement
10 Manual Photoresist Hardbake (hotplate)

Step 3: BOE Etch

Depth	1 μm ±10%	**Etch type**	wet isotropic	**Material**	silicon dioxide

Step 4: Resist strip

Depth	1.5 μm ±10%	**Material**	AZ 5214e

Step 5: Undoped polysilicon LPCVD

Excluded materials	gold (category), copper	**Material**	polysilicon	**Thickness**	1 μm ±10%

1 RCA clean with HF Dip (Pre-furnace clean)
2 Undoped polysilicon LPCVD
3 Spectrophotometric film thickness measurement

Step 6: Contact photolithography (Automated)

1 HMDS Vapor Prime
2 Photoresist Spin Coat ACS200 (AZ 5214E)
3 Photoresist Softbake ACS200
4 Edge bead removal
5 Contact flat alignment and exposure
6 Photoresist Develop (5214E)
7 Linewidth Microscope Measurement
8 Microscope inspection
9 Stylus profilometer 1-D step measurement
10 Manual Photoresist Hardbake (hotplate)

Step 7: Silicon ICP Etch

Batch size	1	**Etch rate**	1.1 μm/min	**Material**	silicon
Depth	1 μm ±1%	**Gas**	SF6, Ar	**Temperature**	25 °C

Step 8: Resist strip

Depth	1.5 μm ±10%	**Material**	AZ 5214e

Step 9: BOE Etch

Depth	1 μm ±10%	**Etch type**	wet isotropic	**Material**	silicon dioxide

Instructions	Release Etch.

Step 10: Anodic bonding (vacuum, with alignment)

Alignment type	optical	**Bonded materials**	silicon, Pyrex (Corning 7740), glass (Hoya)
Batch size	2	**Pressure**	0.1 mTorr

1 Megasonic clean
2 Anodic bonding (vacuum, with alignment)

Step 11: Wafer dicing

Batch size	1	**Diced wafer material**	silicon (single crystal)	**Ship wafer on dicing frame**	yes

Fig. 14.2 Example of process runcard or process traveler for the simple example of the polysilicon surface micromachined cantilever surface (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)

14.3 What Is an Integrated MEMS Process?

Process integration, as defined in the previous section, does not have the same meaning as an *integrated process*. An *integrated MEMS process* is one wherein the MEMS device(s) is (are) fabricated on the same substrate as microelectronics. Many MEMS devices require some type of electronics interface in order to be functionally useful. So the natural question is: when does it make sense to produce a MEMS device and microelectronics on the same wafer? This is a difficult question to answer, but always depends on whether such integration provides the best system solution in terms of performance and cost. There are other issues as well, such as the magnitude of the development cost and the length of time associated with developing a manufacturable integrated MEMS process technology.

In cases where the system-level tradeoffs do point to the need for merging MEMS and electronics on the same substrate, an integrated process must be designed and developed. At first blush this may seem relatively straightforward, however, the complexities of such integration are quite significant and often drive the development cost up very significantly. Some of the key difficulties in developing an integrated process technology are topography and photolithography accuracy, layer-to-layer alignment, materials incompatibility, and thermal budget problems (see discussion below). In any case, this is a fundamentally important system-level question of MEMS design. And although there is no single answer because each individual case depends on performance, size, cost, and packaging requirements, among others, of that particular product and market, we examine some of these issues and tradeoffs to give an appreciation of the important decisions related to the partitioning of the system design.

We show several examples of both nonintegrated and integrated MEMS process sequences later in this chapter, as well as examine how to develop a production-cost estimation for these different scenarios. With the matter of definitions established, let's now discuss the importance of process integration.

14.4 Differences Between IC and MEMS Fabrication

MEMS technology has its roots in and heavily leverages the fabrication technologies developed by the integrated circuits industry and therefore is often associated with IC technology. This association is valid because MEMS and IC share common attributes related to some of the fabrication methods and materials used. However, there are several very important differences between IC and MEMS fabrication and reviewing these differences will help to better understand some of the process integration issues related to MEMS.

The first difference is that the microelectronics domain has converged to a relatively small number of "standardized" or "fixed" process technologies, such as CMOS (complementary metal–oxide semiconductor), bipolar, BiCMOS (bipolar and CMOS), and so on, for making integrated circuits. Although each manufacturer usually has a proprietary process technology for their ICs, in reality there are very

few and they have very subtle differences between them. In comparison, the MEMS domain tends to use a totally different process sequence for each device type. That is, the sequence of processing steps to implement an accelerometer may have little in common with a process technology to implement a lab-on-a-chip. This is partly due to the fact that microelectronics primarily has only three basic device types, namely transistors, resistors, and capacitors, which are wired together into circuits using metal interconnect layers. In comparison, MEMS technology has an extremely large number of different types of devices. Some examples include: pressure sensors, accelerometers, gyroscopes, vibration sensors, inkjet heads, magnetic sensors, microvalves, micropumps, optical switches, modulators, and so on. It is important to note that each MEMS device usually requires its own specialized process sequence in order to meet the performance requirements for a given application. As a result, there is a tremendous amount of customization involved in the fabrication of MEMS devices and, therefore, process integration is an extremely important issue in the implementation of MEMS.

Another major difference between MEMS and IC fabrication is the vast array of processing capabilities and materials used to make MEMS devices. MEMS fabrication leverages conventional process capabilities borrowed from the IC world such as oxidation, LPCVD, and photolithography and combines these processes with highly specialized "micromachining" techniques. These micromachining techniques have been reviewed in previous chapters of this book and include bulk micromachining, surface micromachining, wafer bonding, and LIGA, among others. In fact, each of these micromachining techniques actually includes a very broad spectrum of different processing technologies depending on the materials used and exact ordering of the processing steps.

Consequently, MEMS developers have a much richer range of choices regarding materials and fabrication techniques than is commonly available in the IC domain. This has many advantages, but also poses some challenges as well. A major advantage is that MEMS developers have considerably more design and processing freedom to obtain outstanding device performance. On the other hand, the MEMS developer has comparatively little in the way of standard process technologies from which to leverage. This means that the MEMS designer must choose from an enormous range of process options without a priori knowledge of exactly which processing steps will work best for the fabrication of a given device, not to mention how to integrate these processing steps into a viable process sequence. Moreover, MEMS designers very often need to develop from scratch one or more of the individual processing steps used in the process sequence. In short, there is an enormous amount of customization that routinely takes place in MEMS fabrication, which results in a tremendous number of variables that must be understood and controlled in order to develop a process sequence that meets the performance requirements, provides an acceptable yield, and meets the product cost goals. Most MEMS development efforts are necessarily focused on the development of working devices in the early stages of a venture, which means that the efforts are really directed at developing a viable process sequence that allows devices to be made that meet the design performance and cost objectives.

Another significant difference between MEMS and IC fabrication (and one that is extremely important to the success of a business venture) relates to the scale of production. Specifically, the production volumes in the two technologies are often quite different. The volume of IC wafers typically produced in a commercial foundry each year is truly enormous. ICs are produced using batch-fabrication and continuous flow manufacturing techniques whereby large numbers of wafers are processed in an identical fashion (i.e., a fixed process technology such as CMOS) and each wafer may have hundreds or even thousands of individual, but identical, integrated circuits.

The advantage of batch fabrication is that the cost is spread over millions of die, and therefore large economies of scale can be obtained thereby allowing a comparatively low die cost. High volumes are essential for IC manufacturing because the investments that must be made in order to enable state-of-the-art IC manufacturing are now in excess of several billion dollars. Consequently, there is a strong incentive in IC production to move toward larger diameter substrates as well as smaller devices in order to lower the cost per die. The industry is now at the 300 mm diameter level with linewidths of tens nanometers. High volumes are typical in IC manufacturing because microelectronic circuit process technologies are sufficiently generic to cover a wide number of applications (e.g., TSMC's foundry model) or the production volumes (and margins) are sufficiently high (e.g., Intel's microprocessor production) to recoup the investment and still make a profit.

For MEMS the situation is most often quite different. Typically, the volumes in MEMS are inherently lower due to the specialized nature of the specific devices. For example, a MEMS inertial sensor designed for automobiles as a crash air bag deployment sensor is very useful for that specific application, but the process technology used to make this device may not be suitable for most other applications. As a consequence of the specialization of MEMS devices the overall market size for a given device type, as measured by the number of devices manufactured annually to satisfy the market need, is frequently quite small in comparison to microelectronic production volumes. Indeed, many MEMS devices have market sizes that are very small (e.g., hundreds or thousands of devices per year). Therefore, the production volumes in MEMS vary over a huge range. As a general rule, MEMS devices with higher production volumes tend to be manufactured using essentially the same methodology used in IC production, namely batch fabrication and continuous flow manufacturing techniques, whereas MEMS devices with low production volumes are usually manufactured using job-shop production methods. Clearly, a good understanding of the production volumes required to satisfy the expected market demand as well as the approach taken for the development and production of MEMS devices (e.g., outsource or insource) are critically important.

14.5 Challenges of MEMS Process Integration

There are substantial challenges associated with MEMS process integration. Perhaps most important, the properties of materials used in MEMS fabrication, particularly their mechanical properties, can be highly dependent on the process

sequence as well as the specific processing conditions. It is well known in microelectronics fabrication that the electrical properties of materials used must be very well controlled to achieve good transistor device performance. However, in order to achieve good performance in MEMS devices, mechanical as well as electrical, and potentially other material properties (e.g., optical, thermal, etc.) must also be tightly controlled. This can be particularly challenging for thin-film materials used in MEMS fabrication because the properties of these materials can have a very large impact on the resultant performance of MEMS devices. Moreover, these materials will typically possess a range of values in the "as-deposited state" depending on the exact processing conditions (i.e., deposition rate, temperature, etc.) used during the deposition of the thin-film material.

Consequently, if a thin-film layer used in a MEMS device is in the as-deposited state, then knowledge of the properties of that material layer would be required, but may not be available until they are measured. It is also important that these material properties be reproducible. Models for the properties of these materials are extremely useful in this regard. Additionally, it is often the case that more processing will be performed after a thin-film layer has been deposited. Any subsequent processing steps can significantly modify the material properties of thin-film materials. That is, the processing steps performed after the thin-film was deposited can substantially change the material properties from their as-deposited values. Moreover, the amount of change in these material properties can vary depending on the nature and type of the subsequent processing steps performed. Obviously, this makes it extremely difficult to predict the properties of these materials with any reasonable level of certainty unless the exact same process sequence has been previously characterized (i.e., the material properties are known for the process sequence) and is reproducible. Consistent control of these effects is often critical and therefore must be part of the process integration method used from the outset.

Another challenge that must be addressed is to determine how and where to develop and manufacture a MEMS device. Because of the enormous number of MEMS fabrication methods (including processing technologies and materials), it is virtually impossible for any single MEMS foundry to have all of the needed methods within their capabilities. Most microelectronics foundries provide one-stop shopping for all of the frontend processing (i.e., fabrication up to packaging and test) such that everything needed to implement an IC according to a standardized process technology resides within a single foundry. On the other hand, the fabrication core competencies in the MEMS field tend to vary, and sometimes quite significantly, from foundry to foundry.

Given the enormous diversity in materials and processes, it is prohibitively expensive for individual MEMS foundries to have all the techniques, and therefore the design and process freedom at any one MEMS foundry can be constrained. To overcome this problem, distributed fabrication, whereby the wafers are processed by multiple foundries, is becoming more widespread in the MEMS industry. For example, it is becoming more commonplace for the production of integrated MEMS to form a split-manufacturing scenario between an IC and MEMS foundry wherein the individual foundry capabilities complement each other. A CMOS foundry

may perform the fabrication of microelectronics on substrates and then send the substrates to a MEMS foundry that performs the MEMS fabrication.

The business benefits of such an approach can be quite significant. First, it avoids the huge development costs associated with developing a standalone microelectronics process. Second, it avoids the problem of matching the production capacity for microelectronics with that of the MEMS devices, which can be difficult. Third, it allows continuous access to state-of-the-art microelectronics process technologies without incurring the enormous development and capital costs that this would involve.

Given the difficulty, cost, and risk associated with the approach of complete customization it should be obvious that the first step of any MEMS development activity should be to determine if an existing process technology can be used or leveraged (by leveraging we mean to make relatively simple modifications or to use any portions of an existing process technology) because this will often be the most efficient and effective approach available. Nevertheless, the leveraging of existing process technologies in commercial MEMS foundries has frequently not been a viable option for designers. There are several reasons for this, including: (1) most MEMS process technologies in existence were developed by captive foundries that are not interested in making their capabilities available to outside entities; (2) MEMS is a relatively new field and has an enormous range of applications and therefore the number of existing process technologies available is quite limited; and, (3) most MEMS process technologies in existence were not designed with the intent to be generic for a range of applications, but instead were developed and optimized for a single device and application area. Historically, the leveraging of an existing process sequence requires that the intended application be closely aligned to the original or else the development of a customized process sequence will be warranted.

We now discuss some of the more detailed technical challenges that arise related to MEMS process integration.

14.5.1 Topography

In standard front-line CMOS electronics fabrication, thicknesses of the material layers are very thin, usually on the order of nanometers to tens of nanometers in thickness. As a consequence, topographies are small and photoresist thicknesses can be correspondingly thin. In fact, the thicknesses of photoresists scale to some degree with the resolution of the linewidths: thinner photoresists must be used to obtain smaller resolution linewidths. MEMS structures, on the other hand, often tend to be comparatively thick. This causes photolithographic constraints on the device's planar dimensions and limits the layer-to-layer alignment accuracy that can be achieved. For example, if one tries to embed MEMS fabrication steps into a microelectronics fabrication process sequence to create an integrated MEMS process sequence, the inherent constraints of the MEMS processing steps will add constraints to the electronics processing steps that would

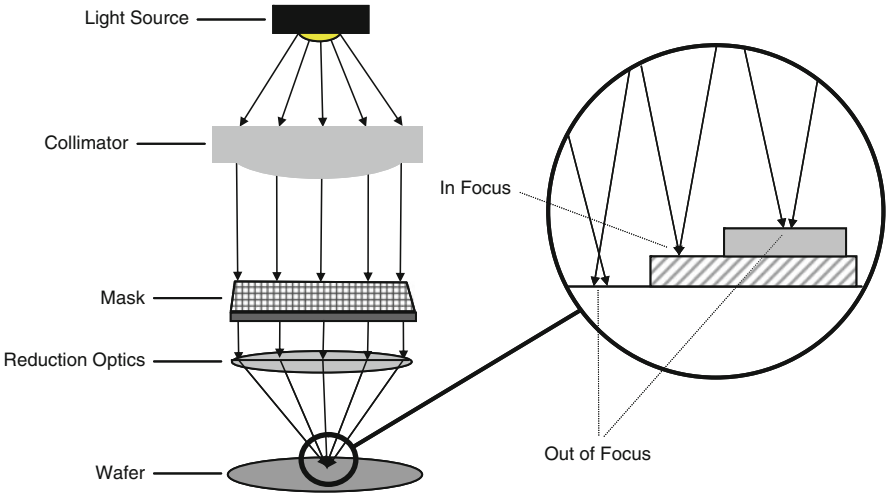


Fig. 14.3 Illustration of how various regions of the photolithographic pattern can be in or out of focus based on the topography of the substrate surface (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)

not otherwise occur in the microelectronics process sequence. This is demonstrated in the illustration below (Fig. 14.3), which shows a projection optical system being used for photolithography on a wafer. As can be seen in the insert to the right, even though the mask image is in focus in certain locations, other locations on the wafer surface are out of focus and this is due to the topology of the surface.

In addition, the alignment structures typically used in an electronics process are generally insufficient for the alignment needs of the MEMS layers, so additional alignment strategies must be designed into the integrated process flow. For example, many MEMS processes will pattern and etch the backside of the wafer for a subsequent through-wafer etching process that requires special alignment marks. Another common mistake for deep anisotropic etches (e.g., deep RIE) is that any alignment marks in the silicon can be easily erased during processing. Therefore, care must be taken to ensure that alignment marks in the silicon will either survive the etch or the alignment marks are made in a different material layer that will not be etched.

The large topology seen in MEMS fabrication also causes problems with continuity of layers after thin-film depositions. At the edge of high topology structures where there is a large dropoff, the material layer after thin-film deposition may be thinner than in the field regions (Fig. 14.4a). At worst case, there may even be a discontinuity in the layer across large variations of topography. Additionally, it can be difficult to obtain a conformal and continuous coverage of a thin film deposition in the deep high-aspect-ratio trenches that are frequently seen in MEMS fabrication (Fig. 14.4b).

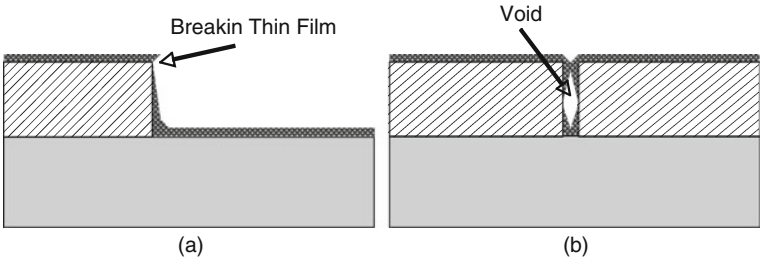


Fig. 14.4 Illustration of the problems caused in thin-film deposition during MEMS fabrication due to the large topography

14.5.2 Material Compatibility

A more difficult process integration challenge is material compatibility. The importance of this issue is perhaps best illustrated in the case of integrated MEMS process technologies. Standard CMOS electronics fabrication uses a very limited set of materials whose electrical properties are very well known. On the other hand, one of the great strengths of MEMS fabrication is the availability of an extremely broad and diverse range of material types. The introduction of atypical materials into a CMOS electronics flow can have dramatic and unforeseen consequences. A classic example is the use of gold. In the MEMS context, gold can have extremely useful material properties; very high electrical conductivity, very high thermal conductivity, good surface-to-surface bonding capability, and excellent chemical inertness. However, it does not adhere well to silicon dioxide and it can poison transistor devices (it is a rapidly diffusing element that causes deep level traps and degrades the minority carrier lifetime). Therefore, most CMOS foundries would not permit wafers that have gold on them to be processed on any of the equipment used for microelectronics fabrication. Moreover, most CMOS foundries would also not allow wafers that had been processed on equipment that had ever touched wafers having gold on them to be processed on any of the equipment used for microelectronics fabrication. This example also illustrates the importance of partitioning or segregating the process sequence between processing tools used for microelectronics fabrication from those used for MEMS fabrication (see discussion below).

Material compatibility is an extremely important issue for nonintegrated MEMS process sequences as well. Perhaps the most obvious example of this is when the existing materials on the substrate are modified or destroyed during subsequent processing steps to which the materials on the substrate are exposed. For example, any aluminum metal (commonly used as an electrical interconnect material layer in microfabrication) that is exposed to potassium hydroxide (KOH) (an often-used anisotropic wet chemical etchant for MEMS bulk micromachining) will result in the aluminum being destroyed. Therefore, either another metal, such as gold, or another etchant solution, such as tetramethylammonium hydroxide (TMAH), or a protective layer must be used in the process sequence.

It should also be noted that material compatibility issues can be extremely subtle and difficult to uncover and understand. As an example, a MEMS process sequence may call for the deposition of a layer of LPCVD silicon nitride over a previously deposited PECVD glass layer. However, this may result in the blistering of the silicon nitride layer due to the outgasing from the CVD glass layer. The solution may be to anneal the CVD glass layer at a temperature in excess of the silicon nitride deposition (in fact, it is advisable to perform the anneal at a temperature higher than any subsequent processing steps in the entire process sequence) in order to densify and outgas the glass material prior to the deposition of the silicon nitride layer. As another example, thin-film deposited gold does not adhere well to silicon dioxide layers. Instead, a thin adhesion layer such as chrome needs to be deposited prior to the gold deposition. As these examples demonstrate, given the enormous range and diversity of materials and processes used in MEMS, successful handling and management of process compatibility issues in process integration can be very challenging.

14.5.3 Thermal Compatibility

Thermal budget, which refers to the temperature level and length of time that a substrate is exposed to during processing, must also be addressed in MEMS process integration because it has an enormous impact on the resultant material properties. Management of the thermal budget is often extremely critical for integrated MEMS processes. The thermal budget must be carefully controlled in order to maintain appropriate doping levels in, for example, the CMOS channel. Also, the temperature of any subsequent processing of microelectronics wafers with metallization must be performed at low temperatures.

In MEMS fabrication, on the other hand, long, high-temperature annealing steps are often required to control morphologies of polycrystalline materials or reduce built-in residual stresses and stress gradients within material layers. Therefore, any integration of MEMS and electronics process steps requires careful consideration of the thermal requirements of the transistors and MEMS structures as well as the materials used to implement them. These requirements often severely restrict the order in which materials can be deposited in an integrated MEMS process flow. For example, the use of many metals (as circuit interconnects or as MEMS structural layers) must occur after any processing steps requiring high-temperature processing.

Thermal compatibility issues are also very important in nonintegrated MEMS process sequences. As was described above, the properties of MEMS materials on a substrate can be significantly modified by the subsequent steps in the process sequence. For example, a thin-film layer of gold that is directly deposited onto silicon that is subsequently heated above the gold–silicon eutectic temperature, which is about 360°C, will alloy with the underlying silicon and appear to have disappeared. The gold does not disappear per se, but instead diffuses into the silicon. The effects of thermal budget are perhaps the most significant determinant of many of the most important resultant material properties, such as residual stress in a thin-film used in the implementation of a MEMS device.

14.5.4 Circuit/MEMS Partitioning of Fabrication

How the processing steps in a MEMS process sequence are partitioned is very important. Depending on the restrictions of each individual item of equipment, location within a foundry, or from foundry to foundry, there are often issues such as wafer cleanliness and cross-contamination when transferring wafers among tools and foundries that must be addressed.

Many MEMS processes are not considered to be compatible with most microelectronics processes. As discussed above, MEMS uses a much broader and diverse (i.e., different) spectrum of materials than microelectronics fabrication and some of the materials often used in MEMS are known to pose contamination problems for integrated circuits (e.g., gold). In addition, during processing MEMS wafers can generate particulates that can degrade the yield of microelectronics processes. For example, a MEMS process technology may involve the etching of silicon or some other material to create very thin membranes across the surface of the wafer. These membranes may be extremely fragile and susceptible to breakage during subsequent processing. They may even break during normal wafer handling in the cleanroom. The breakage of membranes on the MEMS wafers would likely create a large amount of particulate contamination that would be very problematic for wafers undergoing integrated circuit fabrication. For example, a large amount of particulate matter on the surface of the wafer would seriously degrade the yield of any subsequent photolithographic process step, and this degradation would increase as the linewidth resolution is decreased. As a general rule, the process restrictions for integrated circuits will always be more restrictive than for MEMS. Consequently, the processing equipment used for MEMS fabrication is frequently physically separated from the equipment used to make integrated circuits for most integrated MEMS process sequences.

Many microelectronics foundries, as discussed above, are operated as continuous flow manufacturing environments wherein every wafer is processed according to exactly the same ordered sequence of steps from start to finish. This coupled with the highly strict controls on contamination and particulates dictates that the wafers cannot easily be removed from a manufacturing line, have one or more MEMS processing steps performed, and then reinserted into the integrated circuit processing line. In contrast, the customized nature of MEMS processing sequences requires that some wafers are processed according to one process sequence, another group of wafers are processed according to a different process, and so on. This customization usually requires that the wafers jump from one type of process and the associated equipment tool to another. This has a large impact on the partitioning of the process and equipment for an integrated MEMS process. Due to the concerns of contamination and particulates from MEMS processing steps as well as the restrictive nature of integrated circuit fabrication, it should be obvious that often the most practicable approach for integrated MEMS manufacturing is to perform the microelectronics fabrication first (i.e., start fabrication within facilities having the strictest restrictions) and then transfer the wafers to a less restricted foundry (i.e., a MEMS foundry) wherein the remaining portion of the fabrication is completed.

14.5.5 Tooling Constraints

MEMS fabrication often poses many unique challenges and constraints with respect to the tooling of the processing equipment used. For example, it is not uncommon in MEMS fabrication to process nonstandard wafers including wafers that are much thinner or thicker than a standard wafer, wafers that have holes etched through them, wafers that have extremely fragile structures on their surface, wafers that have features on both sides of the substrate, wafers that have enormous topology (see discussion above), or wafers that have nonstandard shapes (e.g., square or rectangular) or sizes. MEMS-processed wafers are often micromachined in such a way that the mechanical stiffness and robustness of the wafer is compromised. Moreover, some of the micromachined areas create "stress risers" that when combined with the crystalline nature of most semiconductor wafers pose significant risk of fracture. This applies to integrated or nonintegrated MEMS.

Also, much of the semiconductor processing equipment in a modern foundry is highly automated. For example, a typical foundry processing tool will have a load lock mechanism wherein a cassette of wafers is placed, a robotic arm that takes the wafers from the cassette and places them one at a time in a process chamber, and a wafer chuck that applies a vacuum to the wafer inside the process chamber to hold it securely prior to the processing step being performed. The attempt to process a wafer that has previously undergone MEMS (or any micromachining) processing on such a system without ensuring that the tool will not damage the wafer and vice versa may result in a catastrophic outcome. For example, a process sequence may require that a DRIE etch be performed entirely through the whole wafer. However, inasmuch as many DRIE process tools use backside helium cooling, a through-wafer etch would result in the helium leaking into the process chamber unless some remedy were employed. Most often, the device wafer that is being etched is mounted to another (called handle) wafer while the through wafer is being performed. The device wafer is then carefully removed from the handle wafer (one hopes) without breaking it.

There is often a specific tooling compatibility issue that arises in the case of integrated MEMS process technologies. Most state-of-the-art CMOS foundries produce microelectronics on wafers that are 300 mm in diameter. In contrast, many of the specialized MEMS processes are performed on tools that can only accommodate up to 200 mm diameter substrates, with 150 mm equipment being more common. Clearly, this presents a problem on how to process a wafer on both CMOS and MEMS equipment. One solution (which only works for the case where the CMOS fabrication is performed prior to the MEMS fabrication) is to core out the middle of the CMOS wafer with a core diameter matched to the MEMS process tools, and then perform the MEMS fabrication on the cored-out substrate (Fig. 14.5).

Although this may be the best available solution to overcoming this tooling problem, it does have several disadvantages. A large number of CMOS die will be unusable and thrown away (essentially the CMOS die within an annular ring having an outer diameter of the CMOS wafer and an inner diameter equal to the coring diameter). Also, the wafer coring process removes the beveling of the wafer edges

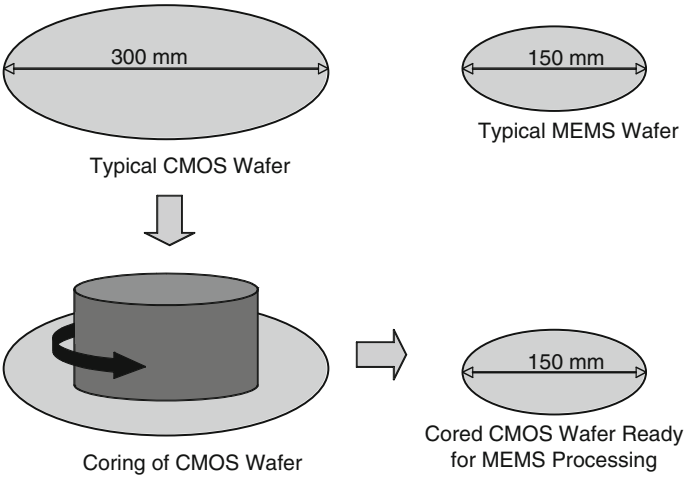


Fig. 14.5 Coring of CMOS wafer so that it can be processed on MEMS equipment

which help protect against wafer breakage. In short, a MEMS fabricator cannot just use the items of equipment that are specified in a process sequence without resolving the constraints that process equipment tooling presents.

14.5.6 Circuit/MEMS Physical Partitioning

The physical partitioning or separation and location of the MEMS device(s) on the substrate is also an important consideration. The most important question that must be answered is whether to develop an integrated or nonintegrated MEMS process sequence. This decision must be carefully and thoroughly researched and depends on many factors, some of which are relatively easy to obtain or estimate, whereas others will require a fair amount of speculation. Some of the factors that must be considered include: comparing the development cost and time associated with integrating or not integrating MEMS with microelectronics, comparing performance levels of both approaches to the performance requirements of the product, comparing the manufacturing costs of both approaches, comparing the capital investments that would be required in both approaches, determining whether there are existing foundries and process technologies from which to leverage for either approach, the cost and difficulty of packaging with respect to both approaches, and so on.

In some situations the integration of MEMS with electronics is necessary. We review a few examples below, such as Texas Instruments' DLP technology, in which this is certainly the case given the huge number of mirrors that have to be independently controlled. Usually the most prudent approach for integrated MEMS is to fabricate the microelectronics first and then the MEMS. However, even in the cases where the microelectronics are fabricated first, the metallization, materials

constraints, dimensions, doping profiles, and the like, of the electronics will place severe limits on the type of MEMS fabrication that can be performed as well as the materials that can be employed. Moreover, it will also restrict the substrate material to whatever the electronics are made from. However, it is often a better choice to go with a nonintegrated approach wherein the MEMS are fabricated on one substrate and the microelectronics are fabricated on another. Often the two die, the CMOS die and the MEMS die, are packaged together in what is called a *hybrid package* and electrically connected inside the package using wire-bonding or a similar technology. The advantages of a nonintegrated approach from the standpoint of reduced development time, development cost, and risk can be dramatic. However, there are other, perhaps less obvious, advantages as well. For example, the nonintegrated approach of MEMS fabrication will allow much more design and process freedom than can be achieved in the integrated MEMS approach. In addition, the yields of hybrid MEMS can be increased due to the fact that "known good CMOS and MEMS die" can be preselected for the hybrid package.

Partitioning as it relates to where the MEMS is located on the die or wafer is also an important consideration. That is, care must be taken in locating the MEMS device(s) on the substrate. As an example, consider the limitations concerning partitioning of a MEMS device on a die as illustrated in Fig. 14.6. In this figure (both left and right) we portray a die (shown in light gray) containing both microelectronics and MEMS on the same substrate wherein the die is larger than the area consumed by the MEMS sensor device (shown in dark gray). The MEMS device may be a sensor that is designed and built to be highly sensitive to strains. (Even if it is not designed as a stress sensor, virtually all MEMS devices are affected by stress.) When the MEMS die is attached to a package using any common die-attach technology (e.g., epoxy, solder, etc.), stresses will be applied to the die and these stresses will likely result in a nonuniform stress field across the die that varies from the center to the edge of the die. Consequently, it will be a prudent design choice to locate the MEMS device on the die wherein these die-attach induced stresses are more uniform, that is near the center of the die (Fig. 14.6, left), as opposed to

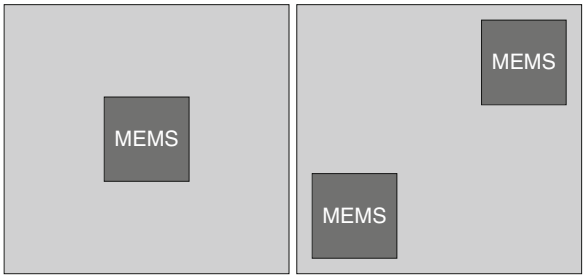


Fig. 14.6 Plan view of two integrated MEMS device die. The one on the *left* has the MEMS device in the center of the die where the packaging and die attach stresses will be uniformly distributed to the MEMS sensor. The die on the *right* has the MEMS devices at the edge of the die and more prone to the effect of any packaging and die attach stresses

locating the MEMS device at the edge of the die (Fig. 14.6, right). As this example demonstrates, both partitioning and packaging should always be addressed as early as possible in any MEMS device development effort.

14.5.7 Die Separation, Assembly and Packaging

How the wafers with MEMS devices are to be diced, handled, assembled, and packaged also poses challenges for MEMS developers. Often MEMS devices are located on the surface of the wafer and are extremely fragile once they are released and free to move (Fig. 14.7a). The standard method in the semiconductor industry of dicing wafers into die using a high-speed diesaw, wherein pressurized water is sprayed at the location of the cutting action, may not be suitable for a wafer with MEMS devices. In such situations, some other method to separate the die must be devised, such as laser cutting. Alternatively, an increasingly popular method is to enclose the MEMS device inside a sealed cavity using what is termed wafer-scale packaging, as shown in Fig. 14.7b. This process is performed at the wafer level (i.e., before die separation) and completely protects the MEMS device during subsequent die separation, assembly, and packaging procedures. However, this will require the process to be designed and developed such that the MEMS device and potentially any microelectronics are not degraded during the process, and space must be dedicated on the die to allow the bonding of the capping wafer and the more complex sawing operation.

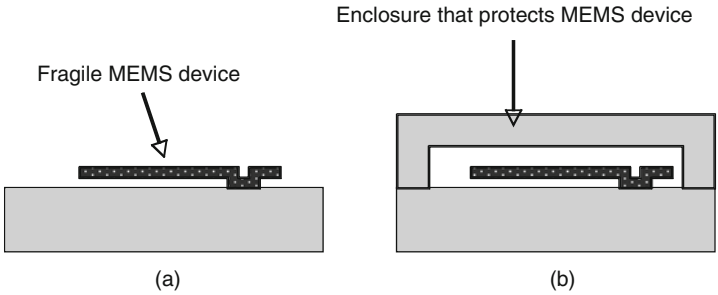


Fig. 14.7 Illustration of fragile MEMS device on the top surface of the wafer that could be broken during die separation and assembly processes

Automated pick-and-place operations are commonly used in the semiconductor industry to transport the die from a diced wafer to a package or other intermediate container. Usually they are composed of a movable tube within which a vacuum is applied to create a suction effect to hold the die on the end of the tube. These types of assembly machines may not be suitable for die containing MEMS inasmuch as the mechanical forces (i.e., contact and vacuum pressure from the tube being placed in contact with the die) may damage or destroy the MEMS devices. Therefore, the location of the MEMS devices on the die will need to be considered beforehand.

A solution may involve locating the MEMS devices on the die where the wand will not contact during pick-and-place operations. The disadvantage of this is that it may require the die to be larger (thereby resulting in a higher cost). Another alternative may be to use a protective enclosure such as the wafer-scale packaging discussed above and shown in Fig. 14.7b.

MEMS packaging tends to be much more complex and challenging than that used in microelectronics, but it must be considered as part of the process integration effort as well. Although microelectronics are usually sealed within a hermetic package and completely isolated from the environment with only the electrical leads penetrating from inside the package to the outside world, a MEMS package must not only protect the die, but simultaneously must allow the die to interact with the environment outside of the package in some limited fashion and provide for the device output signal to be conveyed to the outside world. For example, a MEMS pressure transducer package must have one or more ports whereby the pressure to be measured can be applied through the package to the sensor die and also several electrical leads from the die to outside the package. The pressure sensor die is relatively fragile, therefore the package must also adequately protect the die from damage during handling and while in use.

Although the microelectronics industry has a standard set of off-the-shelf packaging technologies, the enormous diversity of MEMS device types and applications combined with the different ways in which the devices interact with the environment means that MEMS packaging, like the MEMS devices themselves, also tend to be very customized (and can also be very costly) [1]. Furthermore, the package must take the output leads, which are usually electrical, from the MEMS device and route them to the outside of the package in a standardized format that can be connected to a larger system. Another complication that frequently arises in MEMS packaging that can be illustrated in the example of the pressure sensor is that the pressure sensor device is highly sensitive to strain, and consequently any strain built into the sensor as a result of encapsulating a package around the sensor must be appropriately managed. The complexities of MEMS packaging coupled with the fact that there exists no standard or universal package for MEMS die, often results in the packaging being one of the most expensive cost elements in MEMS device production. Even the use of a conventional package may place many restrictions on the design of the MEMS device as well as the process sequence used to implement it.

Ultimately, the decisions about die separation, assembly, and packaging of MEMS devices involve a complex interplay of technical and business analysis and advisably all should be carefully addressed in concert with the device design and process sequence early in any development effort.

14.6 How Is Process Integration Performed?

The development of a MEMS process sequence is very hard work and to be successful at this endeavor requires the careful balance of creative ideas tempered with objective and judicious decision making, plus some amount of good fortune (i.e.,

luck). The technologies employed as well as the people involved must all be carefully selected and may vary considerably in specific skill sets from one type of development project to another. A successful effort requires the fortitude to overcome the constant stream of problems and disappointments that often occur on any MEMS development effort. This requires experienced technologists led by people with both strong leadership skills and technical understanding, who can direct the team to focus on the most practical and timely solutions to these problems. It is important that the process designers and developers be brought into the development effort very early (e.g., day one) and work closely with the device and product designers to provide their guidance on the implementation of the device and product. It is also important that the decision makers for the process approaches be "process agnostics."

It would be incorrect to assume that there is a one-size fits all, fool-proof, or even "well-proven and demonstrated" strategy or set of principles for successfully developing a MEMS process sequence. The skills for successful process development include: very creative instincts, an encyclopedic knowledge of what has been demonstrated in the art, a high level of intuition, good device design capability, the ability to correlate facts from different domains, the ability to handle multivariable spaces with ease, and years or decades of hands-on experience. In short, these are not skills that can be easily conveyed or taught in one book, let alone one chapter of a book. It should be understood that even for the most gifted (or lucky) process developer, MEMS process development entails a considerable amount of iteration and perfecting, based on the ability to quickly learn from previous experiments (i.e., mistakes), and developing strategies for advancing the process development to a successful conclusion.

Figure 14.8 is a simple high-level illustration of the general approach taken for developing a MEMS process sequence. In the first phase, the Conceptual Phase, the device design and process sequence for implementing the design are created. This work will involve several stakeholders including device designers and fabrication

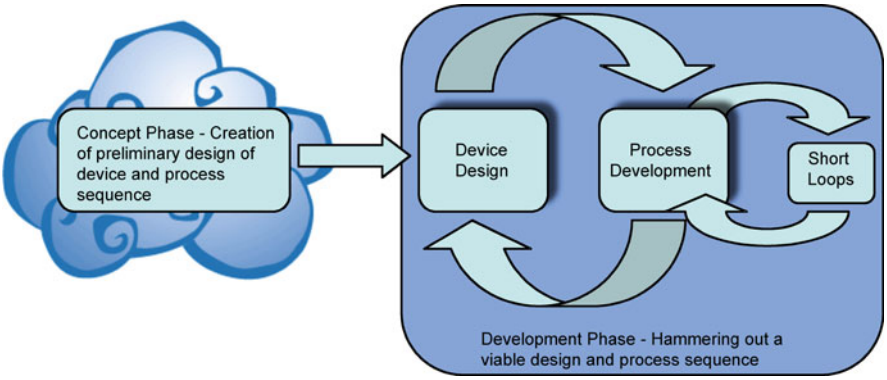


Fig. 14.8 The strategy for MEMS process development (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)

experts as well as business and marketing people. Many compromises will be discussed and made by these stakeholders in order to obtain an outcome that will be thought to meet the performance, cost, and time-to-market goals. It is often prudent to have several potential approaches for the implementation of the MEMS device at the conclusion of this stage. It is important to note that the design models, whether analytical or numerical, are not likely to be based on accurate values for the material properties because these are process dependent (see discussion above). Therefore, the designers will need to make reasonable estimates of these values in their design, with the goal of "bounding the problem." The output of the designer's efforts will be a set of models, a preliminary process sequence(s), and a prototype mask layout set.

Similarly, the fabrication experts will not be able to predict the outcome of either the process sequence(s) or even each processing step with certainty, but will use their experience and judgment to point out the individual processing steps and portions of the processing sequence(s) that will need the most development work and have the highest risk. The fabricators will formulate a strategy, based on the principles of design of experiments (DOE) to develop the individual processing steps that will need to be generated. They will design short-loop runs (i.e., subsets of steps) also based on statistical methods such as DOE to develop portions of the process (i.e., process modules) as well as the entire sequence. In addition, they will work with the designers to create the designs for a set of test structures that will be useful for measuring the properties of the materials used in the process sequence as well as diagnostic structures and devices to help with the process development. The output from the fabrication experts at this stage will be a set of DOEs for all process steps and short loop process runs for the sequences.

With the designs in hand, along with a set of planned process experiments, the work in the fabrication laboratory begins to develop the processing steps, modules, and ultimately the sequence. Much of this work is iterative at many levels. The development of process steps varies the processing parameters over a set of reasonable values, followed by measurement of the outcomes, which are then documented and statistically analyzed. Similarly the efforts to develop modules and sequences will rely on the outcome of a number of short loop experiments, which will also be documented and statistically analyzed. The benefit of well-thought-out, statistically significant experiments for such work cannot be overemphasized!

Once parts of the process sequence are beginning to mature, test structures will be fabricated and measurements taken to determine accurate dimensions and the material property values. These values will be fed back into the design models and new models will be created. Once the process sequence starts to come together and working devices are beginning to be yielded from the runs, the design and models are further refined, new mask sets are created and the iterations continue. It is reasonable to expect that the first two or more cycles of a new and customized process sequence may not initially yield any working devices. It is also reasonable to expect that once working devices are beginning to be yielded on the runs, that the yields will be below 25%, although higher yields are possible. During subsequent process runs, various quality improvement methods (e.g., pareto, histograms, etc.) can be employed to increase the yield to above 50%. At some point, the process

of volume learning begins whereby a large enough volume of wafers has been run that the small yield-killers can be reduced or eliminated. Obviously, the cost and development time are heavily influenced by the complexity of the process sequence for any device type. It is not uncommon to see very large development costs (e.g., in excess of $100 M) for complex MEMS process technologies, such as integrated MEMS devices.

14.6.1 Integrated MEMS Process Integration Strategies

In the case where integrating MEMS with electronics, for example, CMOS, is a necessity, there are several basic ways in which electronics and MEMS processes can be integrated: (1) fabricate the CMOS first and then fabricate the MEMS; (2) fabricate the MEMS first and then fabricate the CMOS; or (3) interleave the process flow. The CMOS first approach usually starts with a commercially produced CMOS wafer. It is then postprocessed to produce the MEMS devices. The benefits of this approach are that the CMOS can be made cheaply in a commercial foundry that uses the most up-to-date CMOS process technology, and it also allows the MEMS device to be fabricated directly on top of CMOS circuitry. The main drawback is that this approach restricts the MEMS processing to materials and thermal cycles that are consistent with the already completed CMOS circuitry. Other challenges with this approach are the ability to lithographically align the MEMS to the underlying CMOS circuitry with high accuracy and the ability to make electrical connections from the microelectronics to the MEMS devices.

The MEMS first approach allows much more flexibility in the MEMS process flow than the alternatives for an integrated MEMS process sequence. However, it then requires a circuit process to be performed on a preprocessed and potentially nonflat wafer. Such a process often requires physical partitioning of the MEMS and circuit areas and methods such as CMP to provide a uniform flat area for circuit processing. It also requires that the MEMS materials used and the wafer cleanliness be consistent with introduction into a circuitry line (see Section 14.5.2).

An interleaved integration process has the benefit of the greatest level of process flexibility. The process can be intricately tailored to the specific needs of the device to be constructed. This may or may not lead to the most efficient process solution, but in general it will lead to the smallest system footprint. However, this flexibility is at the expense of maximum integration complexity, higher development cost, and longer development times. And because it does not force the discipline of a full circuit/MEMS partitioning, it has the highest likelihood of leading to unforeseen process interactions. In addition, it is inconsistent with fabrication in commercial circuit foundries. Thus, the process must be supported without the economies of scale and ongoing improvement associated with standard foundry processes. For example, polysilicon is very commonly used as the main structural material for MEMS devices. However, the thickness of polysilicon in MEMS fabrication is typically much thicker than that used in the fabrication of IC devices. Therefore, instead of developing different process recipes for IC and MEMS, it is common for

microfabrication foundries to deposit polysilicon multiple times for MEMS using existing IC recipes to achieve the required thickness. This example illustrates that MEMS fabricators often strive for simplicity in process development because this helps to reduce errors and hence, increase the quality and the yield, even though such simplicity may not yield optimal properties.

The pros and cons of the approaches to integrate MEMS with microelectronics have been debated for more than a decade. The first commercially viable integrated MEMS process technology was developed by Analog Devices Inc. in the early 1990s (see Section 14.8.3). It is an interleaved process flow where the MEMS process steps are integrated into a standard BiCMOS process flow. This process has been in production for automotive inertial sensor products for over a decade. However, as MEMS moved into the commercial marketplace, which constantly requires lower-and-lower-priced products, this process technology has become comparatively too complex and costly. But for higher-performance, higher-cost sensors it remains a viable process. This example indicates the core conclusion in the MEMS integration debate; that is, the integration strategy of choice needs to balance the requirements of performance, size, and cost. No one approach is inherently better than the others. The decision of which approach to pursue requires careful system-level design thinking as was discussed at the beginning of this section. As sizes and costs for MEMS products continue to shrink, the premiums paid for the added performance and flexibility of integrated processes are expected to become more and more difficult to support.

14.7 Design for Manufacturability

14.7.1 Overview

The performance of any MEMS device is strongly linked to the device design, the fabrication process sequence, the package and assembly methods, and to the environment in which the device is used. As a consequence, the variations associated with all of these areas must be taken into account in both the system-level design and the MEMS device-level design. Unfortunately, design for manufacturability is not an easy thing to either describe or teach. It requires a deep understanding of the device subsystems and a thorough multidomain thinking process. In short, it requires considerable experience to do well. Nevertheless, there are some recommended practices that can be employed that will allow a MEMS developer to achieve a basic level of design for manufacturability which we cover in this section.

The basic goal in designing for manufacturability is to desensitize the system's behavior from the manufacturing variations. Therefore, the first requirement is to understand where the manufacturing variations originate. For example, the manufacturing variations that are typically most important in MEMS are the geometric variations caused by the inherent inaccuracies of the fabrication processes. There are three major sources for geometric variations: planar dimension changes (from

lithography and etching), planar location offsets (from misalignment), and vertical dimension changes (from thin-film or substrate thickness variation).

Consider the lithographic processes that produce the inplane geometry of most MEMS devices. In general, this lithography is performed using a patterned mask in optical equipment that transfers the desired pattern to a chemical photoresist on the device wafer. This process has limited resolution due to the fundamental resolution of the mask and the focusing ability of the optical system. Moreover, there will be alignment or registration errors between the mask and the features on the substrate that are used to align to the mask. The geometric resolution is further reduced by the optical and chemical properties of the photoresist material. In addition, the underlying material layer that is to be patterned will not have a perfectly uniform thickness across the substrate. And finally there is the behavior of the etch process itself to transfer the mask pattern into a layer on the substrate. No etch process is perfectly anisotropic and therefore there will invariably be some difference between the mask and the underlying etch profile. In practice, the inaccuracy of the transfer between the CAD drawing of the design and the actual as-fabricated structure is the cumulative sum of these collective errors. The idea of design for manufacturability in this context is to understand this cumulative sum of errors and to develop a device and system design that is as insensitive to these variations as possible and meets the required manufacturing yields, which in turn will be dependent on the product performance requirements.

Understanding the source and magnitude of manufacturing variations that come from a multitude of physical processes can be extremely difficult. The fundamental methods employed to understand these variations are a good understanding of processing technologies, a good quality statistical data-gathering mechanism, and appropriate modeling to connect design expectations to physical behavior. The purpose of the remainder of this section is to provide a high-level review of the major areas of MEMS fabrication that often result in device variations that can degrade device performance and manufacturing yield. We also provide some general recommendations regarding design for manufacturability at the end of this section.

14.7.2 Device Design for Manufacturability

The planar dimensions in most MEMS devices are defined by a photolithographic process. This process typically has three pattern transfer steps: from layout database to mask, from mask to photoresist, and from photoresist to the desired layer pattern, usually through an etching process. At each step there can be both registration and scaling errors. The result of these errors is that the MEMS device as fabricated will not be a perfectly precise representation of the device design as drawn in the mask layout in either its dimensions or shape. Significantly, there is a very strong coupling between device design for manufacturability and process design for manufacturability (see below).

The key to designing for manufacturing is to experimentally understand the variations observed in the fabrication processes and feed them back into the device

design and models so as to scale the dimensions accordingly. For example, if one is designing a comb-finger-based variable capacitance structure, the width of the gaps between the fingers is directly proportional to the capacitance. A typical photolithography-defined pattern followed by a chemically based etch process will result in comb-fingers that are slightly narrower than as drawn in the mask layout. Moreover, the amount by which the comb-fingers are thinner will vary from device to device, from wafer to wafer, and from lot to lot.

Understanding the mean and standard deviation of the as-etched comb-finger width allows the designer to translate this geometrical variation to a device behavior and performance variation. This understanding of performance in light of manufacturing variations gives the designer the information on which to develop methods to desensitize the design to these variations. In the current example, imagine that the comb-finger variable capacitor is part of an accelerometer whose mechanical stiffness is formed from the same material layer as the comb-fingers. In that case the same manufacturing variation that causes a reduced sensitivity due to an increase in the comb-finger gap may also result in an increased sensitivity due to reduced suspension stiffness. Careful design can partially balance these effects and desensitize the design to this manufacturing variation [2].

Another way to desensitize the fabrication variation is to avoid using the undesirable aspects of a fabrication process to define a device's critical dimensions. For example, the dry etching sidewall is typically somewhat vertical, but the smoothness and sidewall angles are usually not well controlled. In the case of a device design requiring a perpendicular sidewall with 0.5° variation or mirrorlike sidewall to achieve the critical performance, it will take an enormous amount of process development effort to obtain these process requirements and therefore would not be considered a robust design. Similarly, if the thickness variation in a sacrificial silicon oxide layer is critical to the performance, a robust design at the device level and system level should accommodate the resulting thickness variation expected from the process technology used (a few percent thickness variation is common for LPCVD). When considering process design for manufacturability, a thermal oxidation process will typically exhibit much less thickness variation than either LPCVD or PECVD processes. Thus, we can consider a thermal oxide process that minimizes the thickness variation as a robust design choice if that would desensitize the device's behavior from thickness variations.

14.7.3 Process Design for Manufacturability

Given the strong coupling between design and fabrication in MEMS development, it should not come as a surprise that the methods for understanding and desensitizing the device performance to geometric variations due to processing methods overlap the issues discussed in the previous section. Building on the example discussed above of making comb-fingers in a material layer, the manufacturing variations in the fingers will also be strongly dependent on the process methods used to

implement the fingers. For example, the amount of lateral etch observed in a material layer (i.e., the amount of undercut of the masking layer) will vary depending on the material used in the layer, the type of etch process used (both equipment and process recipe), the depth of etch, the amount of overetch required, and loading effects due to the amount of substrate area being etched.

Most wet chemical etchants are isotropic and will undercut the masking layer very significantly during an etch process. In comparison, RIE, particularly ICP RIE processes such as DRIE, are highly anisotropic and therefore the amount of undercutting of the mask will be greatly reduced. In addition, because the dry etch rate varies within the wafer and from wafer to wafer, it would be difficult to control etch depth using a timed etch as a robust design. As a result, the design with half-etched depth as the critical parameter may have a large variation.

Etches of all types have a characteristic called "loading." This refers to the effect on the material etch front due to the presence or lack of adjacent material also being etched. The etch of a finely spaced pattern of lines and spaces will be different than the etch of a material edge with no other etch faces in the local area. One way to minimize the loading effect is to design a layout with the same etching size so that the etching rate is approximately the same everywhere. For example, if 10 μm are the desired etch feature size, all patterns are created by etching a 10 μm wide contour. Another way is to have at least 15% of overetch to allow complete etching even at the smallest feature size. It would depend on the side effect of overetching to determine which way would give better results in a given situation.

As with the planar dimensions described above, variations in material thicknesses can have a strong effect on device performance. In many MEMS processes, the thicknesses of the material layers are highly dependent on the type of process employed to deposit the layer. For example, many thin-film deposition methods, such as LPCVD and PECVD have an across-wafer thickness nonuniformity of at least a few percent or more. Additionally, there will be some variation from the nominal film thickness desired and the actual thickness after deposition. Similarly, methods of wafer bonding and thinning-back to create single-crystal silicon layers having a thickness of a few microns or more, can often have a variation from wafer to wafer of at least 0.5 μm or more, which can translate into relatively large relative tolerances for thin device layers.

The manufacturing variations in the critical dimensions of MEMS devices will also be highly dependent on the process sequence that is used to implement the MEMS device. That is, all processing steps before and after, and the processing step used to define a critical layer's dimensions may also have an effect on the dimensions of that layer and must be considered. Therefore, as can be appreciated, there are truly myriad complicated physical mechanisms that can give rise to geometric manufacturing variations in MEMS. The key to good design for manufacturability is to fully understand these variations in all of the key dimensions with the potential to affect the device performance. Developing this understanding requires considerable data gathering and statistical analysis.

In addition to geometric variations, MEMS devices are subject to significant variations in material properties. Typical properties with significant variations are

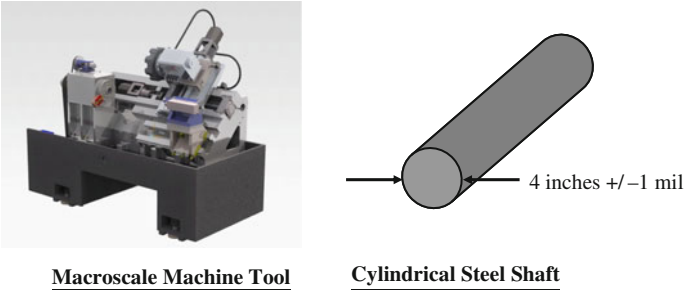
mechanical properties, such as the residual stress, stress gradient, elastic modulus, and electrical properties, such as the conductivity. Again, the key to good design is to fully understand the variations in all the key dimensions that affect device performance. Good process design can improve manufacturing variations caused by material variations. For example, a material's elastic modulus is intimately linked to its crystal structure. To obtain repeatable material properties, the process must be designed to produce repeatable material morphology. In addition to repeatability, the material properties can be engineered to be more or less isotropic, based on the uniformity of the material structure.

Another area that is closely linked to material properties is a film's stress state. This is mostly relevant to released MEMS structures, where the stress state is again strongly dependent on the film's crystal structure. In particular, variation of the crystal structure through the thickness of the film will cause bending moments, which cause the released structure to curl. This curvature can vary widely with small changes in the material's morphology. Thus, it can cause large manufacturing variations. Design for manufacturability requires careful process design to deposit a uniform film and anneal the film to reduce its residual stress, as well as device design to reduce the sensitivity of the device's performance to variations in curvature. As this discussion demonstrates, the design of a material deposition process is much more complicated than simply getting the desired thickness of a given material.

14.7.4 Precision in MEMS Fabrication

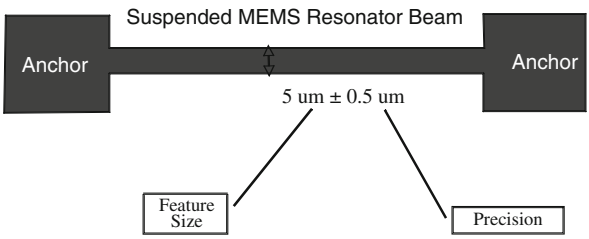
It is helpful at this point to discuss in general terms the relative precision of MEMS manufacturing methods. It is often incorrectly thought that MEMS allows the fabrication of microdevices with high levels of "precision." This is not the case because in general the relative tolerance, expressed as the ratio of the variation of the dimension of a critical element normalized to the absolute dimension of that same element, is far less precise than that which is routinely obtained in macroscale machining processes (i.e., that which is readily available in a typical machine shop). For example, it is quite easy to go to a machine shop and order a cylindrical drive shaft that a machinist can make to a fairly precise tolerance using standard machining tools and processes such as a lathe (Fig. 14.9). Let's say that the design required that the shaft have a nominal diameter of 4 in. (100 mm). The machinist would easily be able to make this shaft with a tolerance within ± 1 mil (± 25.4 μm) or better. This translates into a relative tolerance of 0.0254%.

In comparison, let us examine the relative tolerance of a MEMS device critical element such as the width of a surface micromachined resonator beam that is suspended between two anchors affixed to the substrate surface (Fig. 14.10). Let us assume that the desired design width of the resonator is 5 μm. A typical variation that would be seen in this dimension using standard micromachining methods would be around ± 0.5 μm or more. This translates into a relative tolerance of the MEMS device of 10% or nearly 400 times worse than obtainable with macroscale machining techniques! Moreover, depending on the physics of the device the relative



$$\text{Relative Tolerance} = \frac{25.4 \times 10^{-6}\,\text{m}}{100 \times 10^{-3}\,\text{m}} \times 100\% = 0.0254\ \%$$

Fig. 14.9 Illustration of relative fabrication tolerances using macroscale machining methods (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)



$$\text{Relative Tolerance (Precision)} = \frac{5\ \text{um}}{0.5\ \text{um}} = 10\%$$

Fig. 14.10 Illustration of the plan view of a resonator beam clamped at both ends (at the anchors) and suspended along its length, and showing the relative fabrication tolerances obtainable using micromachining methods

tolerances will often have a larger than simple linear impact on the performance of a MEMS device. Specifically, the order of the physics of the MEMS device can magnify the impact of the lack of precision on the device performance.

For example, the volumetric flow rate in a MEMS microchannel scales to the fourth power of the hydraulic diameter of the microchannel at a constant differential pressure assuming laminar flow. Therefore, any lack of precision in the diameter of the microchannel will have a fourth-order effect on the flow rate. Similarly, the stiffness of a beam is dependent on the thickness of the beam cubed if the motion is orthogonal to the substrate surface as in the example of the suspended resonator example in Fig. 14.10. The deflection of a thin membrane clamped along each side, which is a commonly used configuration for implementation of pressure sensors, varies to the fourth power of the edge length of the membrane and inversely to the cube power of the membrane thickness. As can be appreciated, the cumulative effect of all these variations can be very significant. It is also important to note that for

most MEMS machining processes, the dimensional control gets worse as the size of the critical elements is made smaller and therefore the precision decreases. As these examples serve to demonstrate, MEMS allows the implementation of miniaturized mechanical devices, but does not allow the dimensions of the devices to be made precisely.

The lack of precision in MEMS manufacturing tolerances has huge implications throughout MEMS technology and business. As shown in Fig. 14.11, the manufacturing process for the production of MEMS is essentially an open-loop manufacturing process. That is, the fabrication process sequence and the parameter settings of the process sequence (i.e., tool settings, process recipes, etc.) are first defined and set and then the MEMS devices are fabricated. Quality control during the manufacturing process typically involves performing metrology measurements of the critical dimensions using statistical sampling on various devices and wafers at preselected events during the process sequence. Only at the very end of the manufacturing process is the device performance measured. Any deviations seen in the metrology measurements of the critical dimensions taken during the manufacturing process can be used to tweak the process, but may come at the loss of the wafers partially processed up to that point in the process sequence.

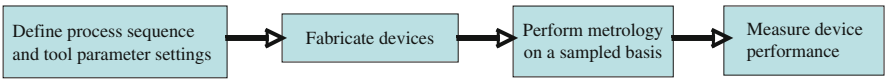


Fig. 14.11 Open-loop manufacturing process typically employed in MEMS production

More important, the ultimate performance is not known until after the manufacturing process for a batch is completed. This means that whole wafer lots can be lost if the performance falls out of the acceptance range. Additionally, there is significant time and cost required to adjust the manufacturing process in an attempt to increase the number of devices with an acceptable performance level (i.e., obtain a higher yield).

Ultimately the goal of MEMS manufacturing is to tighten the spread of the variations in the critical dimensions and to reduce the amount of bias offset. This is portrayed in Fig. 14.12 wherein in Fig. 14.12a is shown a Gaussian bell curve that would be the expected statistical variation seen in a large sampling of MEMS devices with respect to their performance levels. We have superimposed an acceptance range, that is, the range of devices having a performance level that is acceptable for a given application or product. As shown in Fig. 14.12a, the statistical variation is rather large (i.e., the Gaussian curve is wide) and there is a bias offset, that is, the centerline of the Gaussian curve does not line up with the centerline of the acceptance range. Consequently, the overlap of the acceptance range and Gaussian curve is rather minimal and the manufacturing yield will be very low. In contrast, the Gaussian curve of Fig. 14.12b has much less statistical spread (i.e., the width of the Gaussian curve is minimal) and the Gaussian curve centerline coincides with the acceptance range centerline resulting in a very high manufacturing yield.

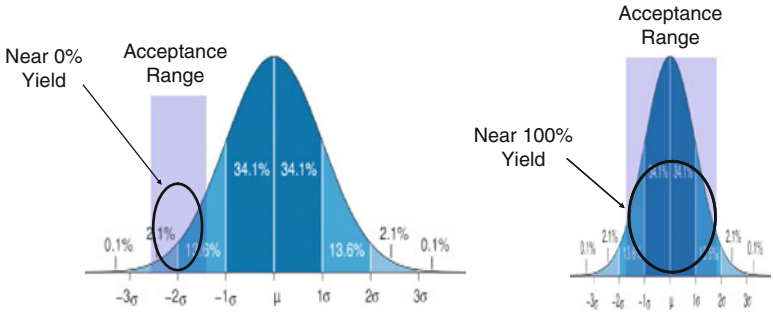


Fig. 14.12 The importance of precision and control of manufacturing processes on the yield. (**a**) Widely spread Gaussian curve for a manufacturing process that has significant variations and a bias offset error thereby resulting in a low yield given by the overlap of the acceptance range and the Gaussian curve. (**b**) Manufacturing process that has considerably less variation and no bias offset error and therefore has a high yield (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)

The important point of this discussion is that the designs of the device and the process sequence have an enormous impact on how easy it is to produce a device that meets its required performance specifications. Although very difficult to do in practice, it is extremely important to ensure that the process sequence, materials, equipment, and design all strive to the extent possible to reduce the variations in the fabrication process and the resultant device behavior.

14.7.5 Package Design and Assembly

Design for manufacturing in the area of package-device interactions can also be quite complex. The main area where package and assembly variations can translate into performance variations is stress. In the process of assembly, a MEMS die will be bonded to a substrate, wire bonded, and then either lid sealed or overmolded. All of these processes occur at elevated temperatures and impart stresses on the MEMS die. The chance that such a complex system would revert to a stress-free state at the device's operating temperature is very unlikely. Manufacturing variations are also caused by variations in the placement of the die in the package, which can change the stress state. It can also directly affect the device's cross-axis performance by causing variations in the package-to-device coordinate reference frames. Finally, the intra-package interconnect (e.g., wirebonds) can cause variation in parasitic capacitances that can affect device performance.

Clearly the variations caused by packaging and assembly are very complex. Designing to reduce these variations is similarly complex. Good design for manufacturability requires an understanding of these physical interactions. The most effective method for analyzing the variations and optimizing a design is through the use of 3-D simulation. This still requires an understanding of the underlying material properties as an input, but it allows the designer to examine material variations,

design geometry variations, and environmental use cases (i.e., temperature and humidity).

14.7.6 System Design for Manufacturability

Some of the major issues related to design for manufacturability of the system, such as whether to integrate the MEMS with microelectronics on the same substrate were discussed above. This may be the most important decision in any MEMS development effort, however, it is not the only design for manufacturability systems-related issue. Another systems-related issue is how to calibrate the device. Due to the large variations in the critical dimensions of MEMS sensors it is not uncommon that some postfabrication calibration must be performed. Often this is done by laser-cutting an array of "trim resistors" that are part of the sensor output signal circuitry. The design of the MEMS device and associated microelectronics must consider how any required calibration is to be performed. Moreover, at what stage the calibration and final testing are performed is also important. Although the yield at the completion of the frontend fabrication may be relatively high, the yield can be reduced dramatically in complex assembly and packaging processes and therefore it may be less expensive to trim the devices after they are assembled, packaged, and tested to be functional.

Some MEMS devices, such as liquid drop ejectors and micromirror diffraction gratings, contain an array of actuators that need to operate relatively equally in order to meet their performance requirements. Compared to the effort to fabricate every actuator with little variation, it is sometimes easier to take care of the variation at the system level. For example, the individual actuators can be calibrated and the input power for each actuator can be adjusted according to the calibration to have equal output. This is to consider the design for manufacturability from a system point of view.

14.7.7 Environmental Variations

Once the MEMS device is installed in the field, it will be subjected to a range of environmental conditions. The most widely encountered are variations in temperature and humidity. As we saw in the discussion of packaging variations, the complicated in-package stress state of a MEMS device is temperature-dependent, due to the differences in the coefficients of thermal expansion of all the materials in the device and its package. Variations in humidity can have a similar effect on the packaged device's stress state. Humidity variations have much more complex material interactions and time constants than temperature interactions, so modeling them can be much more difficult. There are many other environmental variations that can affect device performance, such as: electromagnetic interference (EMI), static charge, vibration, and so on. Design to reduce the effects of these variables is complex and requires a great deal of experience with the specific use environment of a given MEMS device.

14.7.8 Test Variations

Many MEMS devices are sensors whose scale factor is calibrated during a final test procedure. Variations in this test procedure can lead to variations in performance due to scale factor inaccuracy. Again, variations of this type can be very complex to model or understand. Most often this type of variation is reduced by having test guard-bands, which ensure that the device remains "in-spec" in spite of tester variation.

14.7.9 Recommendations Regarding Design for Manufacturability

Clearly, design for manufacturability in MEMS development and production is extremely complex and challenging. Nevertheless, there are some basic tenets that are generally applicable and useful to follow. The list below is a set of recommendations that a MEMS developer can employ in the pursuit of achieving design for manufacturability in her MEMS development efforts.

1. Keep the design and process sequence as simple as possible: More processing steps and a more complicated design will make for lower yields, longer development times, and higher costs.
2. Leverage from existing process modules and technologies to the extent possible: This will lower your development (nonrecurring engineering or NRE) cost and time as well as reduce risk.
3. Know the physics of your device and how they relate to the dimensions and fabrication process. Avoid fabrication processes that provide large relative tolerances of the dimensions for critical elements, particularly those having higher-order dependencies (i.e., to the square, cube, or fourth power). Use bistable mechanical elements to the extent possible; the large relative tolerances of MEMS devices make continuous-movement device types hard to implement and costly to calibrate.
4. Make critical mechanical elements from materials having reproducible properties: Making devices from materials such as single-crystal silicon can be far easier than making them from thin-film materials. Avoid designs that critically depend on the hard-to-control fabrication processes such as perpendicular etched sidewalls, timed etching depth, and sidewall smoothness.
5. Use processing recipes and tools that are well proven to the extent possible: Avoid new equipment and new process capabilities until they are well proven and shown to be reliable and able to deliver reproducible results. Use appropriate etch stop layers and endpoint detection to accommodate etch rate variations.
6. Minimize the number of materials and layers that comprise the critical mechanical elements: Stacking of multiple material layers of thin films is only asking for big challenges.
7. Understand and account for the respective relative tolerances in the precision of the fabrication methods employed.

8. Expect to make several design and process changes as well as multiple iterations in the development of a viable process sequence: Patience for multiple iterations is the name of the game in MEMS development.
9. Avoid merging MEMS with microelectronics on the same substrate unless the application demands it: Integrated MEMS is a costly and risky strategy.
10. Engage packaging, assembly, and test engineers into the device development effort at the beginning of the design process: All these parties must work closely together, listen, and be ready to compromise to achieve a successful outcome. The fabrication–validation cycle takes a long time. Perform as much multiphysics simulation as possible to optimize design critical parameters and reduce the development cycle time.
11. Embed smart test structures in the layout to determine material properties and performance: This is critical and useful when diagnosing the failure mode and understanding the fabrication problems.

14.8 Review of Existing Process Technologies for MEMS

It is very instructive to review some of the existing fabrication methods that have been successfully developed with an eye toward why they are structured in the way that they are. Therefore, we review a number of successful examples of MEMS process sequences and explain some of the issues and tradeoffs that were confronted during development. We begin reviewing nonintegrated MEMS process sequences and then move to examining several examples of integrated MEMS process sequences. To the extent possible, we have attempted to select examples of process sequences that have been developed for the commercial market and which represent as broad a sampling of implementation practices as possible.

14.8.1 Process Selection Guide

Table 14.1 is a listing of all of the nonintegrated and integrated MEMS process sequences that we review in this chapter. The name of the process sequence and the entity that developed it are provided followed by several high-level differentiators such as device application, whether it is integrated with microelectronics, the type of micromachining processes used, the functional material used in the device, the aspect ratio of the process, whether the process sequence is suitable for implementing moving or static elements, whether one or both sides of the substrate are processed, and whether the process sequence (or a derivative) has been used in commercial production.

14.8.2 Nonintegrated MEMS Process Sequences

14.8.2.1 PolyMUMPS™ (MEMSCAP)

Please note the nomenclature used below: ALLCAPS refers to the mask-level name; lower caps refers to the deposition layer name.

Table 14.1 Process sequences reviewed in this chapter

Process sequence name	Designer/developer	Device application	Nonintegrated or integrated	Technology employed	Functional material	Aspect ratio	Comm. production
PolyMUMPS™	MEMSCap	Variable	Non	Surface	Polysilicon	Low	Yes
FBAR	Avago	RF filters	Non	Bulk and surface	AlN	Low	Yes
SUMMiT V	Sandia	Variable	Non	Surface	Polysilicon	Low	Yes[a]
Microphone	Knowles	Acoustic sensor	Non	Bulk and surface	Polysilicon	Low	Yes
Resonator	SiTime	Timing oscillator	Non	Surface	Single-crystal silicon	Medium	Yes
Gyroscope	Draper	Inertial sensing	Non	Surface	Single-crystal silicon	Low	Yes[b]
THELMA	STMicroelectronics	Inertial sensing	Non	Bulk	Polysilicon	Medium	Yes
Pressure Sensor	Novasensor	Pressure sensing	Non	Bulk	Single-crystal silicon	Low	Yes
Bulk Accelerometer	Ford Microelectronics	Inertial sensing	Non	Bulk	Silicon	Low	Yes[c]
SCREAM	Cornell University	Variable	Non	Bulk	Polysilicon	High	Yes[d]
HARPSS	University of Michigan	Variable	Non	Bulk	SCS and polysilicon	High	Yes[e]
Hybrid MEMS	Infotonics	MOEMS	Non	Bulk and surface	Single-crystal silicon	Medium	No
Silicon-On-Glass (SOG)	University of Michigan	Variable	Non	Bulk	Single-crystal silicon	Medium	No
SOIMUMPS™	MEMSCap	Variable	Non	Bulk and surface	Single-crystal silicon	High	Yes
LIGA	CAMD	Variable	Non	Bulk	Nickel	High	No
RF MEMS Switch	MEMtronics	RF Switches	Non	Surface	Aluminum	Low	Yes

Table 14.1 (continued)

Process sequence name	Designer/developer	Device application	Nonintegrated or integrated	Technology employed	Functional material	Aspect ratio	Comm. production
MetalMUMPS™	MEMSCap	Variable	Non	Bulk and surface	Nickel	Medium	Yes
aMEMS™	Teledyne	Variable	Non	Bulk	Single-crystal silicon	High	No
Plastic MEMS	University of Michigan	Microfluidics	Non	Surface	Paralene	Low	No
Wafer-Level Packaging	ISSYS	Packaging	Non	Bulk	Silicon or glass	N/A	Yes
iMEMS	Analog Devices	Inertial Sensing	Integ.	Surface	Polysilicon	Low	Yes
DLP	Texas Instruments	Displays	Integ.	Surface	Aluminum	Low	Yes
Integrated Pressure Sensor	Freescale	Pressure Sensing	Integ.	Bulk	Single-crystal silicon	Low	Yes
Thermal Inkjet	Xerox	Printing	Integ.	Bulk and Surface	Single-crystal silicon	Medium	Yes
Microbolometer	Honeywell	Infrared sensing	Integ.	Surface	Vanadium oxide	Low	Yes
ASIM-X	CMU	Variable	Integ.	Bulk	SCS and/or CMOS layers	Low	Yes[f]
CMOS+MEMS	Wispry	RF	Integ.	Surface	Copper and gold	Low	Yes
Integrated SiGe MEMS	University of California at Berkeley	Variable	Integ.	Surface	Silicon germanium	Low	No
Integrated SUMMiT	Sandia	Variable	Integ.	Surface	Polysilicon	Low	No

[a]Licensed to Fairchild Semiconductor, but production has been discontinued
[b]A derivative of this process has been licensed for commercial production
[c]Developed for production and then discontinued
[d]A derivative of this process technology is in production at Kionix
[e]Licensed to Qualtre Inc. for commercial production
[f]Licensed to Akustica and a derivative of process technology is in production

The PolyMUMPS™ process is part of the MUMPs® (Multiuser MEMS processes) prototyping program that was originally developed by the Microelectronics Center of North Carolina (MCNC) under contract from the Defense Advanced Research Projects Agency (DARPA) and is now offered by MEMSCAP Inc. out of the same facility in Research Triangle Park, NC. The objective was to develop a standardized process that could be made available on a periodic basis to the research community in a multiuser environment. The PolyMUMPS process is a three-layer polysilicon surface micromachining process derived from work performed at the University of California at Berkeley in the late 1980s and early 1990s. This process is the most widely known and used process for implementing MEMS in the world and has been offered continuously since 1992. Over 80 PolyMUMPS process runs have been completed to date for hundreds of organizations around the world.

The process begins with 150 mm n-type (100) silicon wafers of 1–2 Ω cm resistivity (Fig. 14.13) [3]. The surfaces of the wafers are first heavily doped with phosphorus in a standard diffusion furnace using a phosphosilicate glass (PSG) sacrificial layer as the dopant source. This helps to reduce or prevent charge feedthrough to the substrate from electrostatic devices on the surface. Next, after removal of the PSG film, a 600 nm low-stress LPCVD (low pressure chemical vapor deposition) silicon nitride layer is deposited on the wafers as an electrical isolation layer. This is followed directly by the deposition of a 500 nm LPCVD polysilicon film, Poly 0. Poly 0 is then patterned by photolithography, a process that includes the coating of the wafers with photoresist, exposure of the photoresist with the appropriate mask, and developing the exposed photoresist to create the desired etch mask for subsequent pattern transfer into the underlying layer (Fig. 14.13a). After patterning the photoresist, the Poly 0 layer is then etched in a plasma etch system (Fig. 14.13b). A 2.0 μm phosphosilicate glass (PSG) sacrificial layer is then deposited by LPCVD (Fig. 14.13c) and annealed at 1050°C for 1 h in argon. This layer of PSG, known as First Oxide, is removed at the end of the process to free the first mechanical layer of polysilicon. The sacrificial layer is lithographically patterned with the DIMPLES mask and the dimples are transferred into the sacrificial PSG layer in an RIE (Reactive Ion Etch) system, as shown in Fig. 14.13d. The nominal depth of the dimples is 750 nm. The wafers are then patterned with the third mask layer, ANCHOR1, and reactive ion etched (Fig. 14.13e). This step provides anchor holes that will be filled by the Poly 1 layer.

After etching ANCHOR1, the first structural layer of polysilicon (Poly 1) is deposited at a thickness of 2.0 μm. A thin (200 nm) layer of PSG is deposited over the polysilicon and the wafer is annealed at 1050°C for 1 h (Fig. 14.13f). The anneal dopes the polysilicon with phosphorus from the PSG layers both above and below it. The anneal also serves to significantly reduce the net stress in the Poly 1 layer. The polysilicon (and its PSG masking layer) is lithographically patterned using a mask designed to form the first structural layer POLY1. The PSG layer is etched to produce a hard mask for the subsequent polysilicon etch. The hard mask is more resistant to the polysilicon etch chemistry than the photoresist and ensures better transfer of the pattern into the polysilicon. After etching the polysilicon (Fig. 14.13g), the photoresist is stripped and the remaining oxide hard mask is removed by RIE.

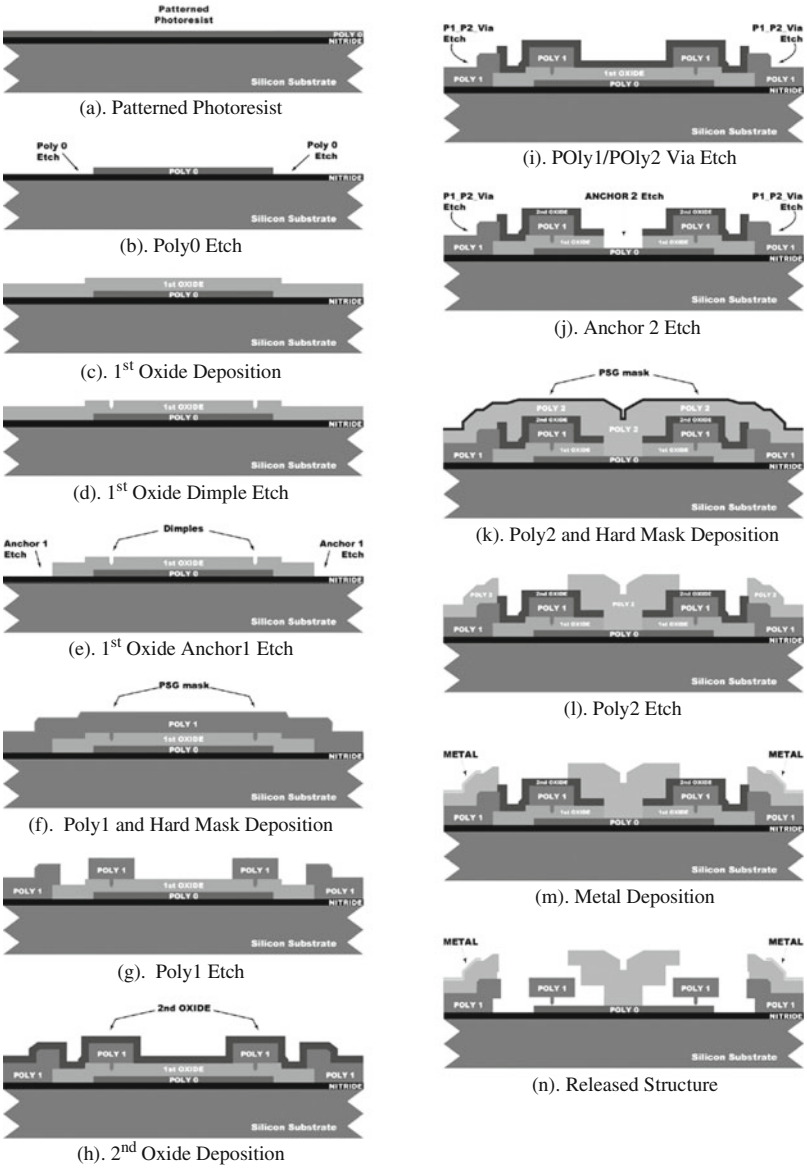


Fig. 14.13 Cross-section of wafer during processing steps of the MEMSCap PolyMUMPS process sequence (Reprinted with permission, copyright MEMSCap, Inc.)

After Poly 1 is etched, a second sacrificial PSG layer (Second Oxide, 750 nm thick) is deposited and annealed (Fig. 14.13h). The Second Oxide is patterned using two different etch masks with different objectives. The POLY1_POLY2_VIA level provides for etch holes in the Second Oxide down to the Poly 1 layer. This provides a mechanical and electrical connection between the Poly 1 and Poly 2 layers.

The POLY1_POLY2_VIA layer is lithographically patterned and etched by RIE (Fig. 14.13i). The ANCHOR2 level is provided to etch both the First and Second Oxide layers in one step, thereby eliminating any misalignment between separately etched holes. More important, the ANCHOR2 etch eliminates the need to make a cut in First Oxide unrelated to anchoring a Poly 1 structure, which needlessly exposes the substrate to subsequent processing that can damage either Poly 0 or Nitride. The ANCHOR2 layer is lithographically patterned and etched by RIE in the same way as POLY1_POLY2_VIA.

Figure 14.13j shows the wafer cross-section after both POLY1_POLY2_VIA and ANCHOR2 levels have been completed. The second structural layer, Poly 2, is then deposited (1.5 μm thick) followed by the deposition of 200 nm of PSG. As with Poly 1, the thin PSG layer acts as both an etch mask and dopant source for Poly 2 (Fig. 14.13k). The wafer is annealed to dope the polysilicon and reduce the residual film stress. The Poly 2 layer is lithographically patterned with the seventh mask (POLY2). The PSG and polysilicon layers are etched by plasma and RIE processes, similar to those used for Poly 1. The photoresist is then stripped and the masking oxide is removed (Fig. 14.13l).The final deposited layer in the PolyMUMPs process is a 0.5 μm metal (Au with Cr adhesion layer) layer that provides for probing, bonding, electrical routing, and highly reflective mirror surfaces. The wafer is patterned lithographically with the eighth mask (METAL) and the metal is deposited and patterned using liftoff. The final unreleased structure is shown in Fig. 14.13m; Figure 14.13n shows the device after sacrificial oxide release using HF.

Figures 14.14 and 14.15 are SEMs of MEMS devices made using the MUMPS process sequence. Figure 14.14 is a SEM of a comb-drive resonator and Fig. 14.15 is a SEM of an electrostatically actuated micromotor.

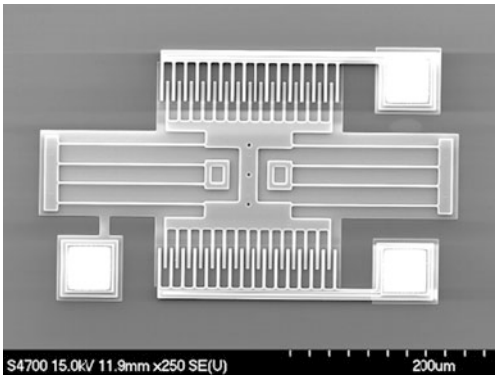


Fig. 14.14 SEM of a comb-drive resonator microstructure made using MEMSCap's MUMPS process sequence (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)

14.8.2.2 Film Bulk Acoustic-Wave Resonators (FBARs) (Avago)

Piezoelectric materials (see Chapter 5) are used to convert electrical energy into mechanical energy and vice versa. Thin-film bulk acoustic resonators (FBARs) are two-terminal devices that utilize a thin-film layer of a piezoelectric material sandwiched between two metal electrodes. In the limit of infinitesimally thin

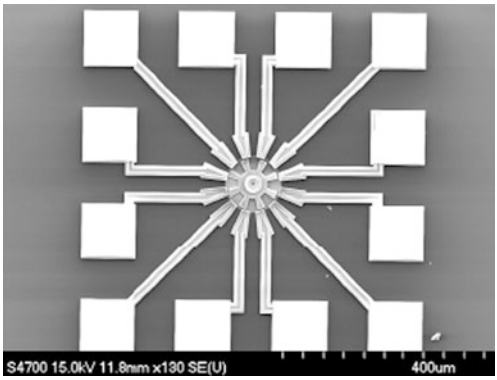


Fig. 14.15 SEM of an electrostatically actuated micromotor made using MEMSCap's MUMPS process sequence (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)

electrodes, a resonance condition is met when the thickness of the piezoelectric material is equal to an integer multiple of half of the acoustical wavelength of the piezoelectric material at the desired electrical driving frequency. More specifically, the fundamental resonant frequency is proportional to the ratio of the acoustic velocity in the piezoelectric material and twice the thickness of the resonator. With finite electrodes the resonant frequency shifts downward with the additional mass loading. Although there are different configurations of acoustic-wave devices, the FBARs use an electrical driving field through the thickness of the resonator to generate a longitudinal or compression acoustical wave along the same direction. The thicknesses of the thin-film piezoelectrics can be quite small, thereby allowing FBARs devices to resonate at high frequencies. The FBAR configuration with an air interface on either side combined with the ability to fabricate devices using materials having high-Q's (i.e., quality factors) provides for a resonator having very high intrinsic Q, a prerequisite for good filter performance. In addition, the air interface of FBARs also allows the effective coupling coefficient to be maximized compared to other configurations. Lastly, FBARs can handle relatively high powers and possess good thermal stability [4]. As a result of these advantages, FBAR technology has rapidly grown into a very large commercial market with the primary application area being electronic filters for cellular telephones [5]. The distinct advantages of FBARs over competitive technologies are its physical properties, specifically: a high resistance to electrostatic discharge (ESD); good temperature stability; and excellent insertion loss in the passband (due to high Q) combined with excellent rejection and isolation out-of-band. All of these features are provided in a very small-sized package footprint for use by handset manufacturers [6].

FBARs are an interesting process integration example because they employ a piezoelectric material, which is an exotic material type that requires special material and processing compatibility considerations. Moreover, the need to appropriately manage the inherently large acoustic impedance mismatch resulting from having the resonator structure located on the surface of the substrate presents several major design and fabrication challenges as well. This mismatch results from having one side of the resonator exposed to air and the other affixed onto the wafer surface.

Current approaches for managing this impedance mismatch usually involve either removing a large section of the wafer material from underneath the resonator structure or by using a suitably designed Bragg filter that reflects the acoustic energy of the resonator away from the wafer substrate interface [4].

Currently, the FBARs manufactured and sold for commercial applications are not integrated with microelectronics. This has to do with the economics of combining a piezoelectric process that is strongly material parameter-dependent (e.g., the coupling coefficient, frequency, and Q can significantly vary from required values by the processing conditions) for the FBAR with a CMOS process that is highly particle defect-dependent (while still maintaining acceptable yield levels). Furthermore, the economics of placing a few resonators per IC die where the die area used for the resonators are large, makes the cost of integrated resonators prohibitive.

We review the process technology for the most successful FBAR device in the marketplace, specifically the Avago Technology FBAR (original development began under Hewlett-Packard Laboratories and then under Agilent Technologies). Avago's process technology uses MEMS fabrication techniques to create an air cavity under the device to control the impedance mismatch on either side of the resonator that would otherwise severely degrade the resonator's performance.

The process begins with a high-resistivity silicon wafer [7] (See Fig. 14.16). Photolithography is performed to define an area where a cavity is etched on the top surface of the wafer. The resonator structure is fabricated so as to suspend across a cavity or "swimming pool" etched into the silicon substrate. A cavity depth of a few

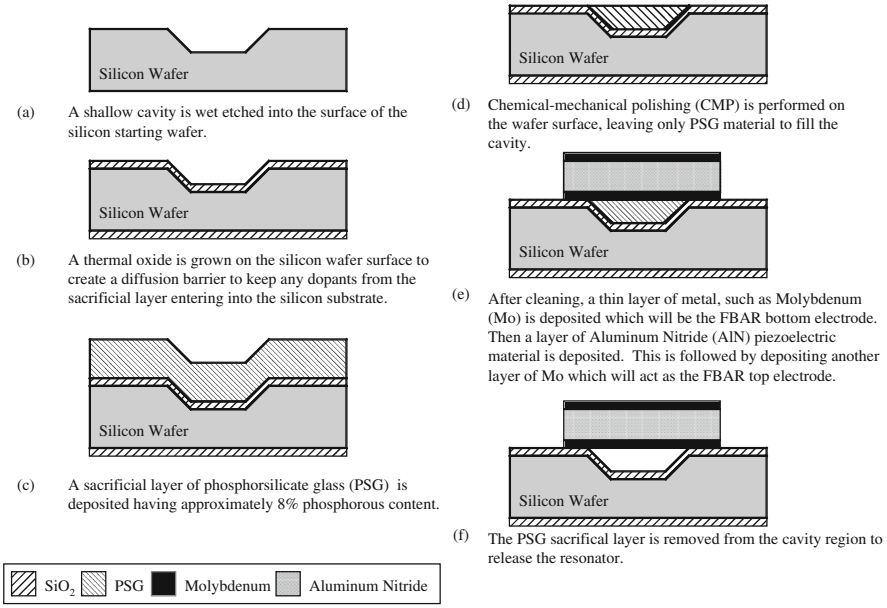


Fig. 14.16 Cross-section of wafer through the Avago FBAR process sequence

microns is sufficient. The cavity is formed in a high-resistivity wafer using conventional dry etching techniques (Fig. 14.16a). The wafer is then thermally oxidized to grow a thin layer of silicon dioxide (Fig. 14.16b). This silicon dioxide layer is added to create a diffusion barrier against any dopants or contaminants from diffusing into the silicon that would result in reducing its resistivity. This diffusion barrier is needed in the Avago process because the subsequent step deposits a highly doped glass onto the wafer surface. A layer of phosphorsilicate glass (PSG) having a thickness more than the cavity depth is deposited at 450°C using LPCVD (Fig. 14.16c). The phosphorous content of the PSG layer is approximately 8%. The PSG layer acts as a sacrificial layer in the process sequence and is preferred due to its very high etch rate in dilute hydrofluoric acid (HF). Moreover, the PSG is deposited at a relatively low temperature, which limits the amount of phosphorous diffusion into the thermal oxide diffusion barrier.

The surface of the as-deposited PSG layer is unsuited for deposition of the piezoelectric device due to its relative roughness and therefore must be made smooth. Specifically, a piezoelectric layer deposited on the as-deposited rough PSG layer results in randomly oriented crystal growth and this material morphology exhibits a highly reduced piezoelectric coefficient. A high-performance FBAR requires that the piezoelectric device layer have a highly textured columnar crystal growth wherein the crystals are perpendicular to the plane of the wafer. Also, the fabrication process requires that the PSG layer be removed from the top surface of the wafer and only remain within the etched cavity. Therefore, chemical-mechanical polishing (CMP) is performed on the wafer top surface to remove the excess PSG and to make the surface of the PSG atomically smooth (Fig. 14.16d). Subsequently, a thorough cleaning is performed to remove any residual contaminants on the wafer surface that may be left after the polishing process.

Next, a bottom electrode metal layer composed of molybdenum (Mo) or tungsten (W) is deposited using sputter deposition. Although other metals may be used for the FBAR electrodes, such as aluminum, gold, platinum, or titanium, the metal materials Mo or W are preferred because of their low thermoelastic loss and high acoustic impedance, which are important for creating a FBAR with a high Q and coupling coefficient. Next, the piezoelectric layer is deposited which is composed of aluminum nitride (AlN) using sputter deposition. Then the top electrode is deposited which is also a sputter deposited Mo (or W) layer. A thin mass loading step is performed whereby a layer is patterned using liftoff to allow the frequency of the shunt resonators to be lowered relative to the series resonators. This helps form the half-ladder filter topology used in designing filters with steep skirts. This multilayer stack is patterned and etched appropriately into the device structure and vias are etched to expose the sacrificial PSG layer within the cavity under the FBAR device structure (Fig. 14.16e). The wafer is then immersed into dilute hydrofluoric acid to completely remove the PSG material from the cavity thereby completing the device fabrication (Fig. 14.16f). Figure 14.17 is a SEM image of a completed FBAR device that has been cross-sectioned.

In as much as a number of FBAR devices are usually fabricated onto a single die each having different resonant frequencies (See Fig. 14.18), Avago has developed a

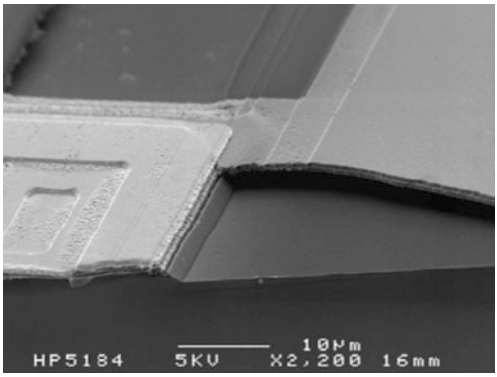


Fig. 14.17 SEM cross-section of Avago FBAR device (Reprinted with permission, copyright Avago Technologies, Inc.)

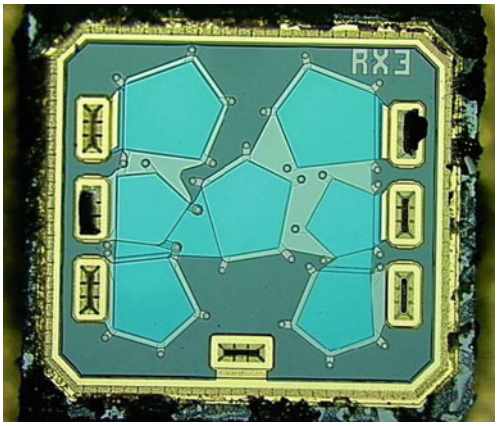


Fig. 14.18 Photograph of Avago filter composed of a number of FBARs made with the Microcap process with the silicon lid removed. The gold ring around the perimeter and each of the I/O connections form a hermetic seal between the individual resonators and the outside environment (Reprinted with permission, copyright Avago Technologies, Inc.)

number of methods for tuning the individual devices. These tuning methods involve either adding (as in mass loading) or subtracting material from devices thereby modifying the device's resonant frequency. These methods are described elsewhere [8]. Also, the FBARs are encapsulated by bonding a silicon lid to the die as shown in Fig. 14.19.

14.8.2.3 Summit V (Sandia)

Sandia National Laboratories has created a nonintegrated MEMS process technology that is called *Sandia Ultra-planar, Multi-level MEMS Technology 5,* (SUMMiT V^{TM}) [9]. Of the nonintegrated process technologies that have been developed in MEMS, SUMMiT V is perhaps the most sophisticated process technology to date. It is a five-layer polysilicon surface micromachined process composed

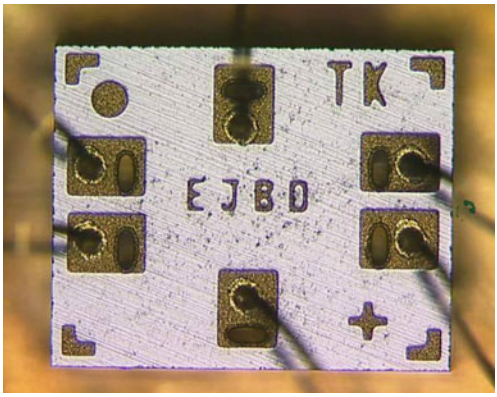


Fig. 14.19 A photograph of a typical FBAR filter after having been cap'd and singulated. This shows the die after wire bonding but, prior to overmold (Reprinted with permission, copyright Avago Technologies, Inc.)

of one ground plane/electrical interconnect polysilicon layer and four mechanical/structural polysilicon layers. The process sequence employs 14 photolithography masks and makes use of chemical-mechanical polishing to maintain substrate surface planarity as more mechanical/structural layers of polysilicon are added.

The SUMMiT V process has been successfully used for a diverse number of applications. It was used to fabricate MEMS devices for space launch as part of NASA's Space Technology 5 (ST5) Micro-Sats program whose mission is to explore concepts of building and operating miniaturized microsatellites. ST5 is the first step in developing missions of tens or hundreds of small spacecraft that would look at phenomena such as space weather. MEMS devices fabricated using the Sandia SUMMiT^{TM} V process were launched aboard NASA ST5 Micro-Sats, a constellation of three microsatellites. Devices were ejected at 3-min intervals during a launch aboard a Pegasus XL rocket on March 22, 2006. The spacecrafts' orbit is a "string of pearls", in a near-Earth polar elliptical orbit that ranges from approximately 300 (190 miles) to 4500 km (2800 miles) from the Earth. The SUMMiT V process was also licensed to Fairchild Semiconductor who transferred the technology to a commercial foundry in Portland, Maine where it was used to produce MEMS devices for several products in the marketplace. Sandia has been providing access to the SUMMiT^{TM} technology to the research and development community through its SAMPLES prototyping program that supports small quantities of MEMS devices.

The Sandia SUMMiT V process starts with n-type <100> oriented 150 mm diameter silicon wafers with a resistivity of 2–20 Ω cm (Fig. 14.20). A thermal silicon dioxide (SiO_2) layer is grown on the wafers having a thickness of 0.63 μm. This oxide layer serves as an electrical isolation. Next, a 0.80 μm thick layer of low-stress silicon nitride (SiN_x) is deposited to act as an etch stop layer. Photolithography is performed (Mask 1, nitride-cut mask) on the substrates whereby the silicon nitride and oxide layers are etched to create electrical contacts to the silicon substrate. A 0.3 μm thick layer of doped polycrystalline silicon is deposited (poly0) by LPCVD onto which photolithography is performed (Mask 2, mmpoly0 mask). The

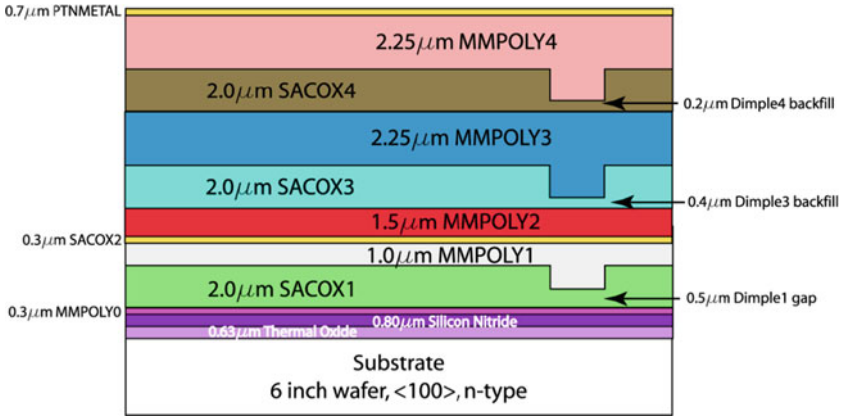


Fig. 14.20 Cross-section of wafer processed using Sandia's SUMMiT V process technology showing the structural and sacrificial layers in the stack (Reprinted with permission, copyright Sandia National Laboratories, SUMMiT^{TM} Technologies, www.mems.sandia.gov)

poly0 polysilicon layer is etched using reactive ion etching (RIE) to form areas for mechanical anchors, ground planes, or electrical wiring interconnections. The first sacrificial layer composed of silicon dioxide (SiO_2) is deposited which is 2.0 μm in thickness. Photolithography is performed (Mask 3, dimple-cut mask) on the surface of the wafer to pattern the underlying oxide layer. Subsequently, the oxide is etched using RIE to a depth of 1.5 μm; that is, the etch is not entirely through the oxide layer. This partial etch of the oxide is used to form dimples, which are essentially standoffs, in a mechanical/structural layer later deposited and etched in the process sequence. A subsequent photolithography on the oxide layer is then performed (Mask 4, sacox1-cut mask) and the oxide layer is etched using RIE completely through to the underlying polysilicon layer in the exposed areas to form anchor sites.

A 1.0 μm thick layer of polycrystalline silicon (poly 1) is deposited by LPCVD on the wafers, followed by another photolithography (Mask 5, mmpoly1 mask) and etching using RIE to pattern the polysilicon layer into a mechanical/structural layer. Photolithography is repeated on this layer (Mask 6, pin-joint-cut mask) and the layer is completely etched using RIE to form hubs in the polysilicon layer for rotating elements. A layer of 0.3 μm thick silicon dioxide (SiO_2) is deposited which is used in the process as a second sacrificial layer or as a hard mask for mmpoly1 polysilicon layer. Photolithography is performed (Mask 7, sacox2 mask) on this layer and it is etched through its thickness using RIE. A 1.5 μm thick layer of doped polycrystalline silicon is deposited by LPCVD. Photolithography is performed (Mask 8, mmpoly2 mask) and this layer is etched completely through using RIE. A 2.0 μm thick layer of silicon dioxide is deposited using the TEOS process. This layer is the third sacrificial layer of oxide in the process. Chemical-mechanical polishing is performed on the top of the wafers to planarize the surface. Photolithography is then

performed (Mask 9, dimple3-cut mask) on this layer followed by an etching using RIE completely through the oxide layer. A 0.4 μm thick layer of silicon dioxide is then deposited to backfill the dimple holes by LPCVD. Another photolithography on this sacrificial layer is performed (Mask 10, sacox3-cut mask) and the exposed oxide areas are completely etched through the layer using RIE to make anchors to the underlying polyilicon layer.

Next, 2.25 μm of doped polycrystalline silicon (poly3) is deposited also by LPCVD. Photolithography is then performed (Mask 11, mmpoly3 mask) on this deposited polysilicon layer and the underlying polysilicon layer is then etched to define the third mechanical/structural layer using RIE. A layer of silicon dioxide is then deposited that is 2.0 μm in thickness, which acts as a sacrificial layer between the third and fourth polysilicon layers. This layer is the fourth sacrificial layer of oxide in the process. Chemical-mechanical polishing is performed on the top of the wafers to planarize the surface. Photolithography is performed (Mask 12, dimple4-cut mask), followed by an etch using RIE completely through the layer. A 0.2 μm thick layer of silicon dioxide is then deposited to backfill the dimple holes between the third and fourth polysilicon (poly3 and poly4) layers. Photolithography is repeated on this oxide layer (Mask 13, sacox4-cut mask), followed by a complete etch through the layer using RIE to form openings between the third and fourth polysilicon layers. A layer of polycrystalline silicon (poly4) of 2.25 μm thickness is deposited by LPCVD which acts as the fourth and final mechanical/structural layer. Photolithography is performed (Mask 14, mmpoly4 mask) on this layer and the layer is completely etched through using RIE. A release etch is performed on the substrates using a wet etchant solution composed of 100 to 1, HF and HCl, to remove all exposed sacrificial oxide layers. Lastly, the substrates are dried using either air evaporation (this only works if the micromachined structures are very mechanically stiff), or supercritical dried using CO_2 (necessary for highly compliant structures). Optionally, a layer of metal can be deposited to a thickness of 0.7 μm and photolithography performed (Mask 15, ptnmetal-cut mask) to make electrical contact to the topmost polysilicon mechanical/structural layer. Figure 14.21

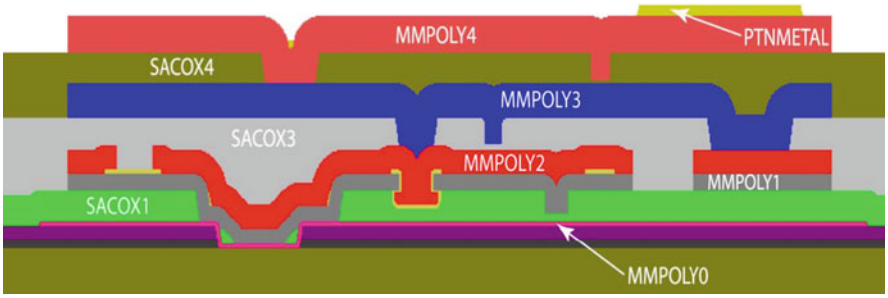


Fig. 14.21 Cross-section of SUMMiT V wafer showing how the individual layers stack up and features that can be realized in the process (Reprinted with permission, copyright Sandia National Laboratories, SUMMiT^{TM} Technologies, www.mems.sandia.gov)

illustrates more accurately how the layers stack up in the SUMMiT V process sequence.

There are several interesting process integration issues involved in the SUMMiT V process technology. First, there are no severe restrictions on thermal processing because there are no electronic devices or metals involved (at least until the very end of the process sequence). This allows LPCVD to be used for the multiple polysilicon and sacrificial oxide depositions. Moreover, high-temperature anneals which are required in order to reduce the residual stress in the polysilicon layers can be performed without degrading the other material layers.

Second, the totality of the polysilicon mechanical/structural layer thicknesses is over 7.0 μm and the totality of the sacrificial oxide layers is over 6.3 μm, which would result in an enormous topography of the wafer surface thereby severely restricting the dimensions and type of devices that could be fabricated with this process. The use of CMP to planarize the surface of the wafer after deposition of the third and fourth sacrificial oxide layer depositions helps to solve this problem and thereby allow higher levels of precision on the resultant device dimensions to be obtained.

Third, the technique used to make the dimples in the first sacrificial oxide layer is different from that used for either the third or fourth sacrificial layers. Specifically, the dimples in the first sacrificial oxide layer are made using the standard technique in surface micromachining of a timed partial etch through the entirety of the sacrificial oxide layer, whereas the dimples for the third and fourth sacrificial oxide layers are made by an etch completely through the thickness of the sacrificial layer followed by a deposition of oxide material to a thickness substantially less than that of the oxide layer, thereby resulting in a dimple height equal to that of the sacrificial oxide thickness minus the thickness of the dimple backfill deposition thickness. This technique for making dimples in the third and fourth sacrificial oxide layers is needed due to the wide variation in the resultant thicknesses of the sacrificial oxide layers after CMP is performed, thereby making it extremely difficult to control the dimple height using a timed etch process. Figures 14.22, 14.23, and 14.24 are SEM images of gear mechanisms made with this process, which demonstrate the level of mechanical complexity that can be obtained with the SUMMiT^{TM} V technology.

14.8.2.4 Microphone (Knowles)

The idea of constructing a MEMS-based acoustic transducer started quite early in the evolution of MEMS devices [10–12]. However, it took many years before the development of processes for commercial products began in earnest [12, 13]. The basic design requirement for a microphone is the construction of a low mass diaphragm offset a short distance from a stiff backplate. Typically these structures form the electrodes of a variable capacitance type microphone (although piezoresistance and other pickoff mechanisms are possible). The combination of the flexible diaphragm and the stiff backplate makes a variable capacitor whose capacitance is a function of the diaphragm deflection. To reduce the damping of this system, the backplate is generally perforated with holes.

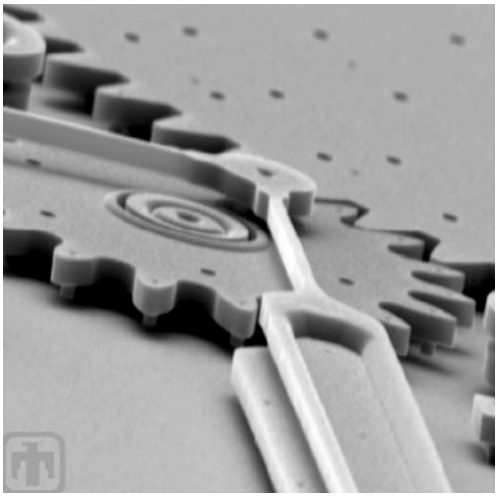


Fig. 14.22 A SEM of a gear mechanism fabricated using the Sandia SUMMiT V process technology (Reprinted with permission, copyright Sandia National Laboratories, SUMMiT^{TM} Technologies, www.mems.sandia.gov)

Fig. 14.23 A SEM of another gear mechanism fabricated using the Sandia SUMMiT V process technology (Reprinted with permission, copyright Sandia National Laboratories, SUMMiT^{TM} Technologies, www.mems.sandia.gov)

The earliest commercially successful MEMS microphone process technology was developed by Knowles, Inc. [14]. The Knowles 11-mask process technology fabricates its diaphragm and its backplate on a single wafer (Fig. 14.25). The wafer is KOH wet etched from the back side to expose the diaphragm and backplate. The diaphragm, which is 1 μm thick polysilicon, is released such that it is a freely floating plate. Thus, its stiffness is dependent on plate bending, requiring good thickness control to obtain consistent device-to-device sensitivity. The backplate is a 1.5 μm thick silicon-nitride layer, which is perforated to achieve the desired damping. A conducting polysilicon layer is deposited on the diaphragm side of

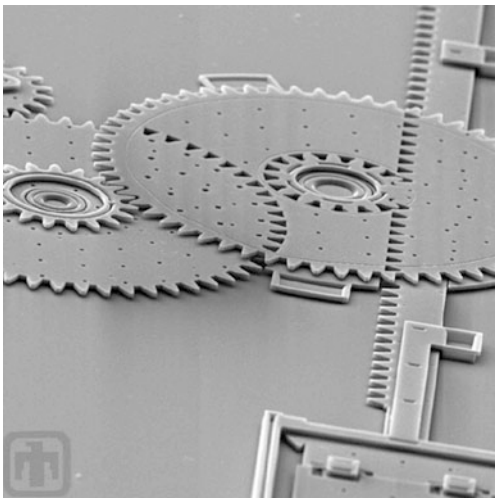


Fig. 14.24 A SEM of an overlaying gear mechanism fabricated using the Sandia SUMMiT V process technology (Reprinted with permission, copyright Sandia National Laboratories, SUMMiT^{TM} Technologies, www.mems.sandia.gov)

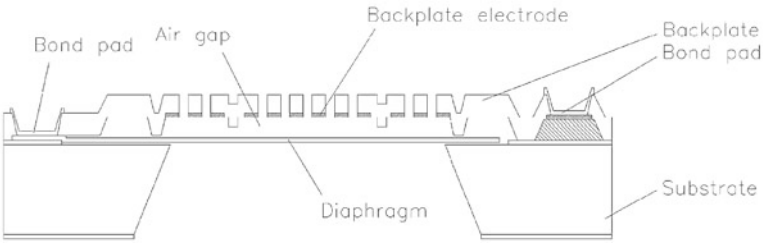


Fig. 14.25 Cross-sectional diagram of the Knowles, Inc. microphone sensor structure (Reprinted with permission, copyright Knowles, Inc.)

the backplate and acts as the capacitive counterelectrode. Support posts of 4 μm height are fabricated in the backplate to keep the diaphragm from collapsing into the backplate due to electrostatic forces. The sensor is then assembled, along with an associated readout ASIC, in an open cavity package.

Analog Devices developed a commercial MEMS microphone that has a similar structure to the one described above. ADI's microphone process is based on an SOI process developed at the University of California at Berkeley [15]. The process was first developed by ADI to fabricate optical MEMS and inertial sensors. In this original process, the MEMS structures were constructed first by DRIE etching trenches into the SOI layer and filling them with silicon dioxide and polysilicon. Circuits were then constructed after the MEMS with a 0.6 μm double-polysilicon, double-metal CMOS process. To convert this original process into a microphone process, the DRIE etched silicon layer becomes the perforated backplane [16]. Then, a set of spacer layers and a thin polysilicon diaphragm layer are added above the SOI layer. An interesting feature of this process is that the sacrificial material that is etched

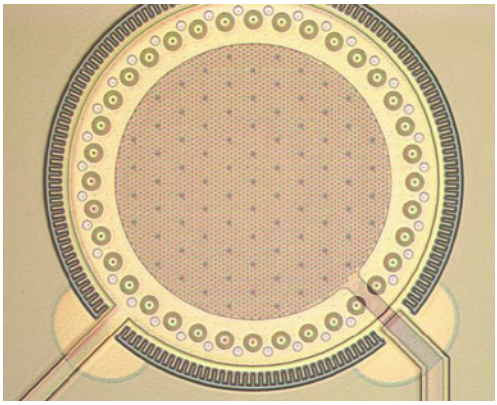


Fig. 14.26 Top-down optical micrograph of the Knowles, Inc. microphone sensor (Reprinted with permission, copyright Knowles, Inc.)

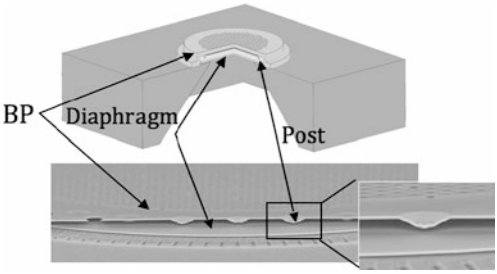


Fig. 14.27 Sensor diagram and SEM image showing the backplane (BP), diaphragm, and support posts (Post) (Reprinted with permission, copyright Knowles, Inc.)

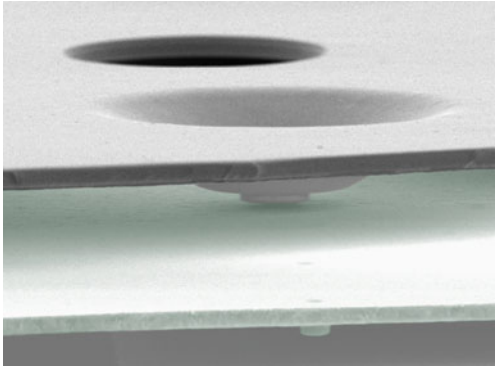


Fig. 14.28 SEM image showing backplane (*upper layer*) with etch hole, support post, and diaphragm (*lower layer*) with small contact dimple (Reprinted with permission, copyright Knowles, Inc.)

away to form the gap between the diaphragm and the backplate is also polysilicon. The process must isolate the diaphragm polysilicon layer from the sacrificial polysilicon in order to etch away one and leave the other. Figure 14.32 shows an optical micrograph of the sensor structure. In addition to the backplate perforation pattern, this image shows the 12 spring structures that support the polysilicon diaphragm.

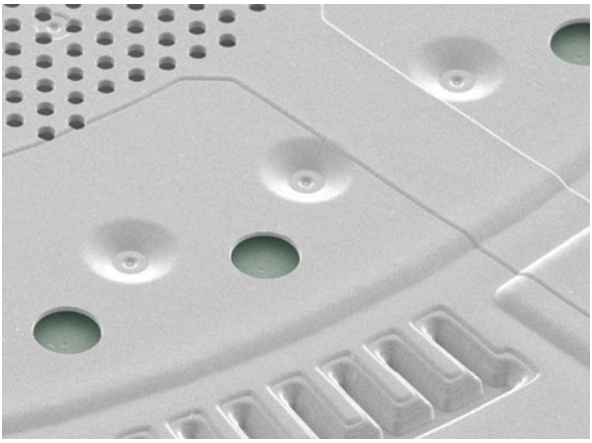


Fig. 14.29 SEM image of the backplate from above showing damping holes (small), support posts, and etch holes (large) (Reprinted with permission, copyright Knowles, Inc.)

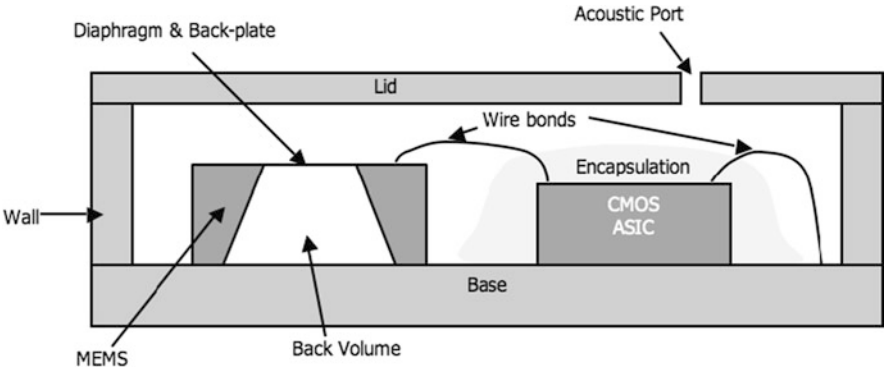


Fig. 14.30 Cross-section diagram of the MEMS microphone sensor and circuit ASIC in the open cavity package (Reprinted with permission, copyright Knowles, Inc.)

14.8.2.5 Silicon Resonator (SiTime)

Quartz crystal oscillators are mechanical resonator devices that exploit the piezoelectric effect in quartz material to create an electrical signal with an extremely precise frequency. These devices are used in a number of timing applications including quartz clocks and wristwatches, stable and precise clocks for most electronic systems, digital integrated circuits and computers, and frequency stabilization for communication systems. The market for quartz crystals is very large and is currently estimated to be over 17 billion devices sold each year.

Recently, silicon MEMS-based oscillators have been developed and introduced into the marketplace to compete with quartz oscillators. There are basically two approaches: one is to have a discrete MEMS oscillator that is pin-for-pin compatible

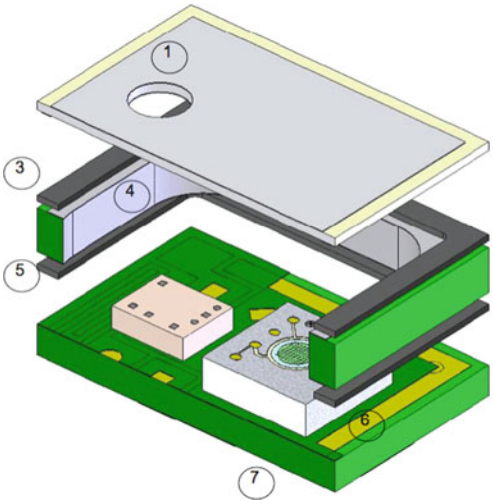


Fig. 14.31 Diagram showing the assembly of the Knowles, Inc. open cavity package (Reprinted with permission, copyright Knowles, Inc.)

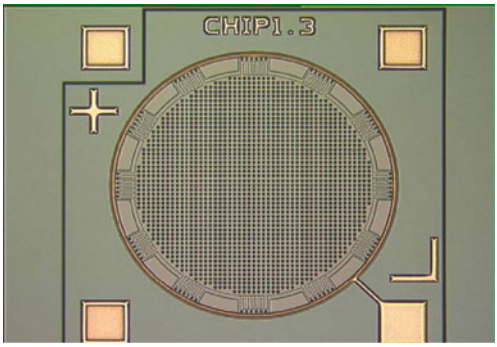


Fig. 14.32 An optical image of the ADI MEMS microphone sensor (Reprinted with permission, copyright Analog Devices Inc.)

with the quartz devices; and the other is to fully integrate the MEMS resonators onto the CMOS as a monolithic solution. SiTime has introduced several devices that take the first approach. Other companies have been developing fully integrated devices, but because this approach requires modification to the CMOS fabrication lines to make these devices, their introduction into the marketplace is expected to take longer.

One of the key issues for implementing MEMS oscillators is how to make the micromechanical resonator structure extremely stable. The SiTime solution is to use a novel wafer-level packaging technology that is part of the resonator fabrication process whereby each resonator is encapsulated within a microcavity vacuum chamber [17, 18].

The SiTime MEMS-based oscillator fabrication process begins with a 200 mm diameter p-type silicon-on-insulator (SOI) wafer with a 10-μm thick silicon device layer (Fig. 14.33a) [19]. Photolithography is performed to define the shape and

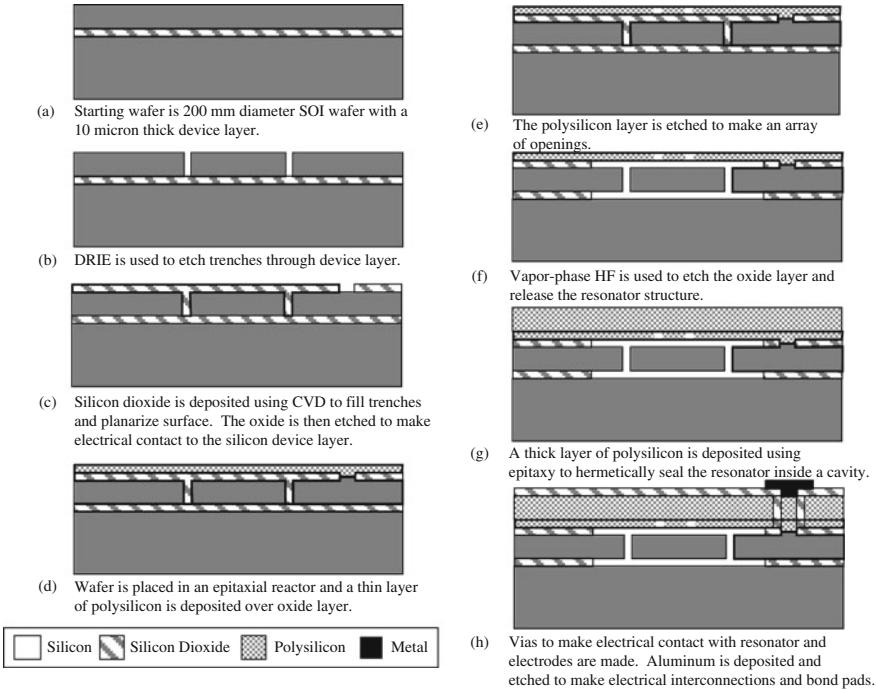


Fig. 14.33 Cross-section of wafer processed using SiTime's MEMS-based silicon oscillator process technology

geometry of the silicon resonators, which are patterned by DRIE etching 0.4 μm wide trenches completely through the silicon device layer (Fig. 14.33b). When the process is complete, the silicon resonators will vibrate horizontally on the surface of the wafer during operation.

A glass layer is deposited using CVD onto the surface of the wafer to a thickness sufficient to completely fill the previously etched trenches made in the silicon device layer and planarize the surface. Photolithography is performed, which is followed by an etching process to create openings through the glass layer through which electrical contacts will be made to the resonator and electrodes later in the process (Fig. 14.33c). The glass from the field areas surrounding the resonators is also removed. Next, the wafer is placed in an epitaxial silicon reactor wherein a layer of silicon is deposited (Fig. 14.33d). The silicon deposited on the glass is polycrystalline, whereas the silicon deposited on the contact area in the glass is single-crystal material. Photolithography is performed to define an array of openings through the epideposited silicon layer at the location above the silicon resonator (Fig. 14.33e). These openings will be used to remove the sacrificial oxide layer surrounding the silicon resonator structure.

The wafer is placed in a vapor-phase hydrofluoric (HF) acid etch system and a timed etch is performed to remove the oxide surrounding the silicon structure and

thereby release the resonator (Fig. 14.33f). The resonator is now cleaned, sealed, and encapsulated using the SiTime Epi-Seal^{TM} process. This process is critical in achieving a stable oscillator whereby the resonant frequency does not drift over time or with subsequent packaging and soldering processing steps. The cleaning process is performed in the epitaxial reactor at a temperature of over 1000°C and entails exposure of the wafer to a hot hydrogen and chlorine gas. This removes all contaminants from the resonator structure. Subsequently, in the same epitaxial reactor, a layer of polysilicon is deposited onto the surface of the wafer that seals off the openings that were made through the first epitaxial silicon layer in order to facilitate the release of the resonator (Fig. 14.33g).

At this point the resonators are sealed within a cavity that is at vacuum pressure. A polishing process is performed on the surface, after which the surface appears smooth and continuous. Photolithography is performed and the polysilicon is etched to isolate the vias to the resonators and electrodes. The trenches are filled with glass to planarize the surface. Contact holes are etched after contact photolithography. Aluminum is deposited and patterned (photolithography is performed) and etched to define metal electrical connections from the resonators and electrodes to bond pads. A layer of silicon dioxide and silicon nitride is deposited to provide a protective layer over the surface of the device (Fig. 14.33h). The resonators are diced, tested, and packaged.

The SiTime approach encapsulates the resonator in a sealed cavity at the wafer level and does so without consuming much space on the die. This approach provides a significant advantage on reducing packaging costs. However, because the temperature of the sealing process is far too high for microelectronics, this approach would not be suitable for an integrated MEMS resonator technology. Figure 14.34 is a SEM of a SiTime MEMS device that has been cross-sectioned to display the resonator within the wafer-level encapsulation.

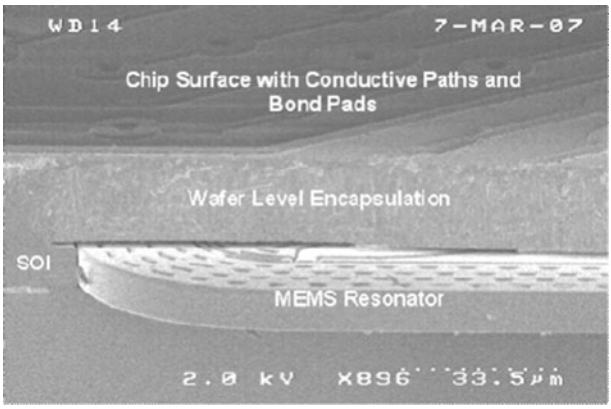


Fig. 14.34 SEM of a SiTime MEMS device that has been cross-sectioned to display the resonator within the wafer-level encapsulation (Reprinted with permission, copyright SiTime, Inc.)

14.8.2.6 Gyroscopes (Draper)

The Draper gyroscope is an example of a tuning fork gyro design whereby in-plane electrostatic forces are used to excite the microstructure, and angular rates are detected through the Coriolis forces which result in a differential out-of-plane force loading on the two identical resonant proof masses. This differential force causes the resonant proof masses to move relatively to one another and this movement is capacitively sensed by electrodes located on the surface of the substrate immediately underneath the resonant microstructures (Fig. 14.35). A derivative of the Draper gyroscope process technology is now in commercial production.

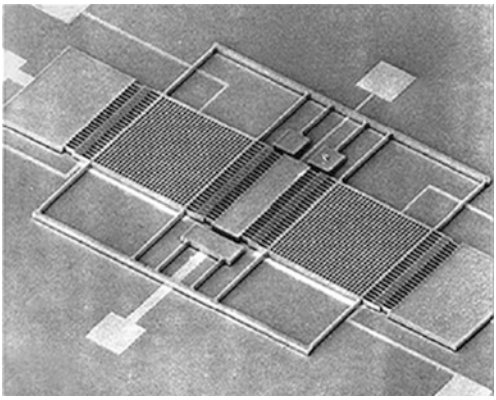


Fig. 14.35 SEM of Draper surface-micromachined gyroscope fabricated with the dissolved-wafer process technology (Reprinted with permission, copyright Charles Stark Draper Laboratory, Inc.)

The "dissolved-wafer" process sequence (developed at the University of Michigan) uses wafer bonding and high-aspect-ratio silicon surface micromachining [20]. The process begins with an n-type silicon wafer that has a recess etched into the surface using an anisotropic KOH etch (Fig. 14.36). This recess establishes the gap spacing from the capacitive sense electrodes and the resonant microstructure. Alternatively the gaps may be etched into the glass substrate wafer.

A deep boron diffusion is then performed to create a highly doped region in the surface of the silicon wafer at a depth, which will determine the thickness of the resonant microstructure, typically 5–20 μm (Fig. 14.36b). Alternatively, this layer of highly doped silicon may be grown epitaxially on the surface of the silicon wafer. After photolithography is performed to pattern the outline of the microstructure, a RIE etch is performed through the highly boron-doped region of the silicon surface and into the underlying lightly doped silicon substrate (Fig. 14.36c). This RIE etch is best performed using a high aspect and deep silicon etch, such as DRIE.

A glass wafer that will be mated to the silicon wafer is prepared as follows. First, a recess approximately 1600 Å is made into the surface of the Pyrex 7740 glass wafer by wet etching. A multiple layer metal stack is then deposited, consisting of 400 Å of titanium, 700 Å of platinum, and 1000 Å of gold. This metal stack is patterned using liftoff thereby leaving the metal stack only in the recessed areas on the glass surface (Fig. 14.36f). The multilayer metal stack is thicker than the glass

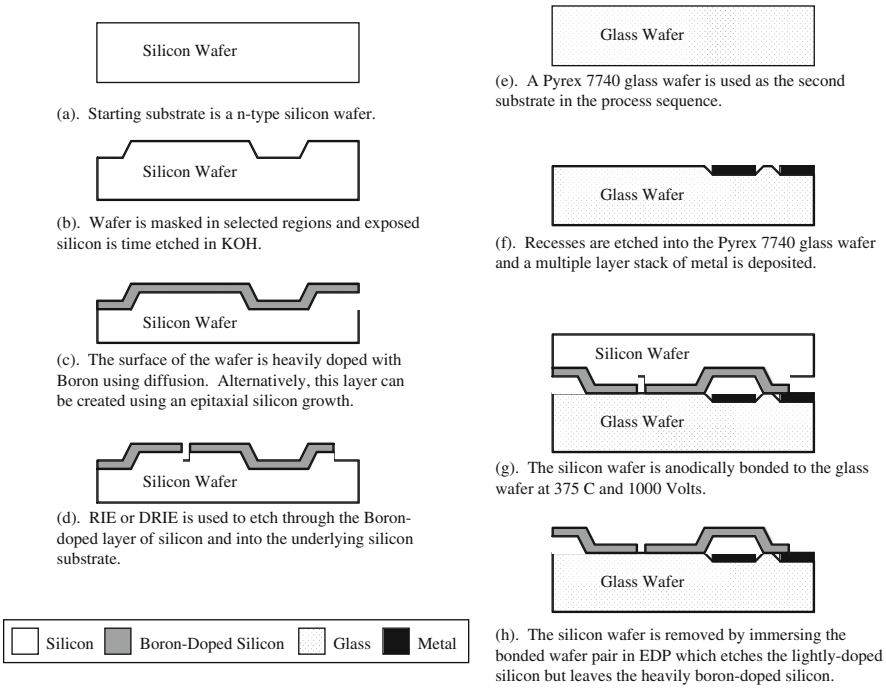


Fig. 14.36 Process sequence for the Draper silicon tuning-fork gyroscope

recess, therefore the metal protrudes about 500 Å above the surface of the glass wafer. This metal layer will form the capacitive sense electrodes and the output electrical interconnects for the device.

The glass and silicon wafer surfaces are then aligned and anodically bonded to one another using a temperature of 375°C and an applied voltage potential of 1000 V (Fig. 14.36g). Electrical contact to the silicon is made by overlapping the silicon rim of the device over a small area of the metal on the glass wafer. The bonded wafer is then placed into an ethylene–diamine–pyrocatechol (EDP) and water solution, which is an effective etchant solution for silicon, but has excellent selectivity with respect to the other materials used in the process sequence. The EDP etchant completely removes the silicon wafer but does not attack the highly boron-doped silicon layer, which acts as an etch stop (Fig. 14.36h). The wafer is then ready for packaging.

14.8.2.7 Bulk Accelerometer (STMicroelectronics)

STMicroelectronics, Inc. has very quickly captured a significant portion of the consumer electronics MEMS sensor market by introducing a line of inertial sensing devices that have excellent performance levels and are sold at extremely attractive prices, an absolutely essential requirement for most consumer applications. STMicroelectronics refers to their microdevices development effort as a “MEMS

Epiphany," which means that they claim to have married the best that MEMS technology has to offer for enabling smaller, cheaper, higher performance, and more functional devices (Technology Push) with a more innovative design approach (Design Driven Innovation) resulting in MEMS devices that are better suited for the consumer marketplace [21].

This strategy has been very successful and has allowed STMicroelectronics to rapidly become the world's largest producer of MEMS devices. STMicroelectronics' MEMS devices are currently used in such notable and highly recognizable consumer products such as Nintendo's Wii, Apple's iPhones and iTouch, and others [22]. For example, Nintendo's Wii product employs STMicroelectronics inertial sensors located in a handheld wand controller to sense the motion of a user who is playing tennis, golf, or any of the other available games thereby allowing the user to be immersed and participate in the action on the screen. This capability has radically advanced computer gaming from a purely passive activity to a much more exciting fully active gaming endeavor. Similarly the Apple iPhone uses STMicroelectronics MEMS sensors to detect the orientation of the handheld communication device to the user's perspective and adjusts the screen display accordingly, thereby allowing much more user freedom and functionality (Fig. 14.37).

Fig. 14.37 Photographs of products employing STMicroelectronics' inertial MEMS sensor technology that provide the customer with radically new capabilities in consumer products (Reprinted with permission, copyright MEMS and Nanotechnology Exchange)

The STMicroelectronics MEMS inertial products are based on their Thick Epitaxial Layer for Microactuators and Accelerometers (THELMA) process technology as shown in Fig. 14.38 [23]. The THELMA process is a nonintegrated MEMS process technology that is slightly more complex than a polysilicon surface micromachining process technology, but has the distinct advantage of allowing thicker structures to be implemented, which is extremely useful for capacitive-based

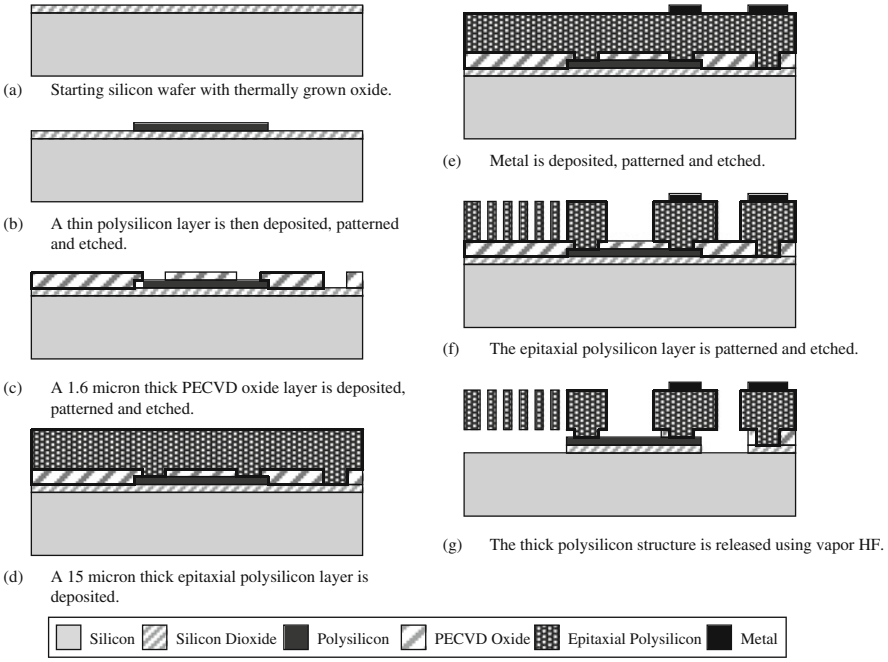


Fig. 14.38 STMicroelectronics' THELMA process technology that is used to manufacture their line of inertial sensors

inertial sensors. The THELMA process technology is used to implement capacitive-based inertial devices, but is sufficiently flexible to be used for the production of accelerometers, gyroscopes, and other MEMS device types.

The process begins with a silicon wafer onto which a 2.5 μm thick thermal silicon dioxide layer is grown (Fig. 14.38a). Next, a polysilicon layer (poly1) is deposited using LPCVD. This polysilicon layer is patterned and etched to form buried electrical interconnections that are used as pathways for the potential and capacitive signals from the device to the outside world (Fig. 14.38b). This layer can also be used as a structural layer for thin polysilicon micromachined devices depending on the device design as well. A 1.6 μm thick layer of silicon dioxide is then deposited using PECVD. This PEVCD oxide layer in combination with the 2.5 μm thick thermal oxide layer forms a composite 4.1 μm thick layer of oxide that acts as the sacrificial layer in the THELMA process technology. The deposited PECVD oxide layer is then patterned and etched forming anchor regions for the thick polysilicon devices that will be implemented later in the process (Fig. 14.38c). Next a thick layer of polysilicon is deposited using epitaxial deposition (Fig. 14.38d). The thickness of this layer can be tailored to the device design and can range from 15 to 50 μm. A metal layer is deposited, patterned, and etched that is used to make electrical connection to the sensor device (Fig. 14.38e). Subsequently, the thick polysilicon layer is patterned and etched using deep reactive ion etching stopping on the underlying

oxide layer (Fig. 14.38f). The DRIE allows very high-aspect-ratio structures to be made in the thick polysilicon layer. The sacrificial oxide layer is removed using vapor hydrofluoric acid to release the structural polysilicon layer (Fig. 14.38g).

One of the key aspects of the STMicroelectronics inertial sensors is the low-cost packaging approach that they have pioneered for high volume production. As stated earlier, packaging of MEMS devices can often be the most expensive element of the manufacturing process. The STMicroelectronics approach uses a glass frit low-temperature wafer-scale bonding process to seal the inertial device within an enclosed cavity between two wafers. This is followed by a land-grid array (LGA) matrix platform packaging technology that they have pioneered for final assembly and packaging. In this process, the individual sensor die can be placed next to the microelectronics die (the so-called side-by-side configuration) or the sensor and microelectronics die can be placed on top of one another (the so-called stacked chip approach) as shown in Fig. 14.39.

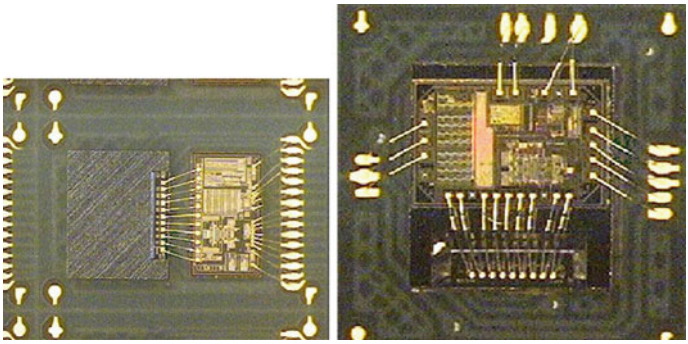


Fig. 14.39 Two configurations of STMicroelectronics's inertial sensor packaging: (*left*) the side-by-side configuration, and (*right*) the stacked chip approach (Reprinted with permission, copyright STMicroelectronics, Inc.)

In the stacked chip configuration, the sensor die are first bonded to a large-area substrate using an adhesive film (Fig. 14.40). Stacking of the microelectronics die and the MEMS die onto each other enables the package to be kept very small (Fig. 14.41). Wirebonding to the electrical pads on the die is performed and then the die are encapsulated using an injection molding plastic process. This packaging approach is performed on large-area substrates and is comparatively inexpensive. Packaging stress, particularly stresses introduced by the adhesive bonding and injection molding processes were significant challenges that STMicroelectronics needed to develop suitable solutions for in order for this approach to be successful. Figure 14.42 shows the evolution of STMicroelectronics device package for their ultracompact linear accelerometer that is commonly used in many consumer products.

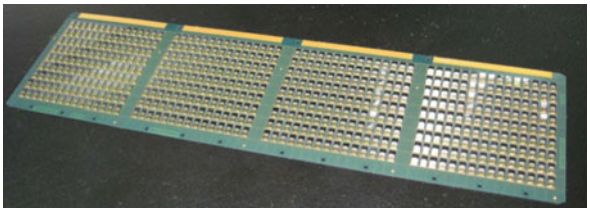


Fig. 14.40 STMicroelectronics' approach to low-cost and small profile packaging for their MEMS inertial sensor devices (Reprinted with permission, copyright STMicroelectronics, Inc.)

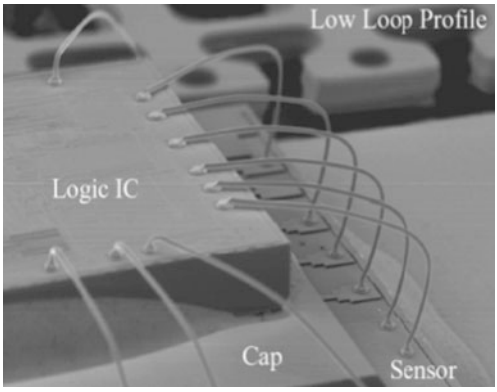


Fig. 14.41 A SEM showing the stacking of the microelectronics die on top of the MEMS sensor die followed by wirebonding and prior to injection molding to encapsulate the devices (Reprinted with permission, copyright STMicroelectronics, Inc.)

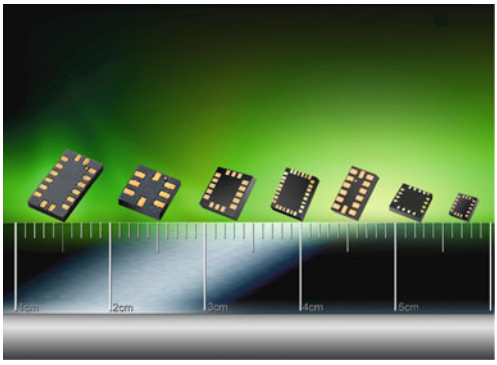


Fig. 14.42 A photograph of the evolution of the STMicroelectronics inertial sensor package (Reprinted with permission, copyright STMicroelectronics, Inc.)

14.8.2.8 Pressure Sensor (NovaSensor)

The pressure sensor was the first MEMS device of significant technological and economic importance. These types of sensor devices continue to represent a large and important part of the MEMS component industry with annual sales of well over $1 B for an enormous diversity of applications including: automotive, aerospace, industrial control, medical, environmental control, and so on. Essentially these devices are composed of a thin diaphragm of material that is usually made of silicon that deflects under the application of a differential pressure loading across the diaphragm. A number of schemes can be used for transduction of the diaphragm

deflection into an electrical signal including piezoresistive, optical, capacitive, and piezoelectric, among others. Nevertheless, it is most common to employ the piezoresistive effect of silicon in these sensors. The piezoresistive effect is demonstrated in semiconductors whereby a relatively large change in resistance occurs when the semiconductor is subjected to a strain; it was first reported by Smith in 1954 [24]. Basically, the piezoresistors are positioned on the diaphragm at locations where the strain is the largest as the diaphragm is deflected. This transduction mechanism is attractive due to the large size of the effect in semiconductors, the relative simplicity of implementation and readout circuitry required, and low cost.

These types of sensors have now been on the market for several decades. Given the length of time that these devices have been produced for the commercial marketplace, it should be no surprise that there has been a significant progression of technology development associated with silicon-based pressure sensors over the years. In fact, the historical development of pressure sensors in many ways reflects the broader development of silicon micromachining and MEMS technology with the first use of isotropic and anisotropic wet chemical etching, eutectic bonding, anodic bonding, and direct silicon fusion bonding.

Brysek et al. and Sze [25, 26] have excellent reviews of the history of MEMS pressure sensors. It is interesting to note that initially (circa 1958) the individual silicon piezoresistors were glued to diaphragms made of metal. This was before the capability of silicon micromachining had been developed and as a result, these combined silicon and metal sensors suffered from low yields and poor stability, mostly due to the large thermal mismatch between the silicon to glue to metal interface. Subsequently, in the early 1960s, dopants were selectively diffused into the silicon to make regions of piezoresistive material on a silicon substrate that was then epoxied to a metal constraint. This improved the yield and performance of the sensors as well as lowered the cost. The next improvement around 1970 was to replace the epoxied bond with a silicon–gold eutectic bond and to thin the silicon diaphragm using mechanical milling or chemical isotropic etching. Subsequently in 1975, the eutectic bond was replaced with a glass frit bond and the silicon diaphragm was machined using anisotropic wet chemical etchant solutions. This allowed the diaphragm to be made thinner and more uniform in thickness thereby increasing the sensitivity, performance and yield still further.

In the 1980s the piezoresistors were made using ion implantation rather than diffusion, which allowed increased control of the bridge resistance and offset. In addition, the glass frit bond was replaced with an anodic bond wherein the glass substrate was closely matched in its thermal expansion coefficient to that of the silicon substrate to which it was bonded. This helped to improve the temperature stability, improved yield, and allowed the die size to be reduced thereby reducing cost. In the late 1980s silicon-to-silicon direct bonding was introduced which allowed the thermal matching to be improved even more and the die size to be radically shrunk thereby reducing cost as well as opening up many additional application opportunities, inasmuch as high-performance pressure sensors having a die size of less than 1 mm could be produced with very high yields.

We only review one of the more recent types of nonintegrated pressure sensors reported in the literature that are sold in the commercial marketplace. The technology to fabricate the pressure sensor devices we review was developed by NovaSensor and first reported in 1988 [27]. It can be used to make both low- and high-range pressure sensors with some slight variations in the process sequence, but we review only the low-pressure sensor process technology. The reader can refer to [27] for information on the fabrication of the high-pressure sensor device.

The process begins with the use of a standard thickness silicon wafer with <100> orientation (Fig. 14.43). A thin-film layer is grown or deposited onto the surface of the wafer followed by a photolithography and etch to expose square openings in the masking layer. The wafer is then etched using an anisotropic wet chemical etchant to form pyramidal pits in the surface of the wafer (Fig. 14.43b). This resultant shape is due to the fact that the thickness of the wafer is nominally 525 μm and the masking openings are 250 μm, and therefore the anisotropic etchant self terminates on the exposed <111> crystallographic planes resulting in an etch pit depth of approximately 175 μm. The masking layer is removed and then a second silicon wafer that is p-type with an n-type epitaxial layer is directly bonded to the wafer having the previously etched pyramids on the surface (Fig. 14.43c).

The thickness of the epitaxial silicon layer will set the thickness of the diaphragm of the resultant pressure sensor. Subsequently, the bulk of the bonded top wafer is

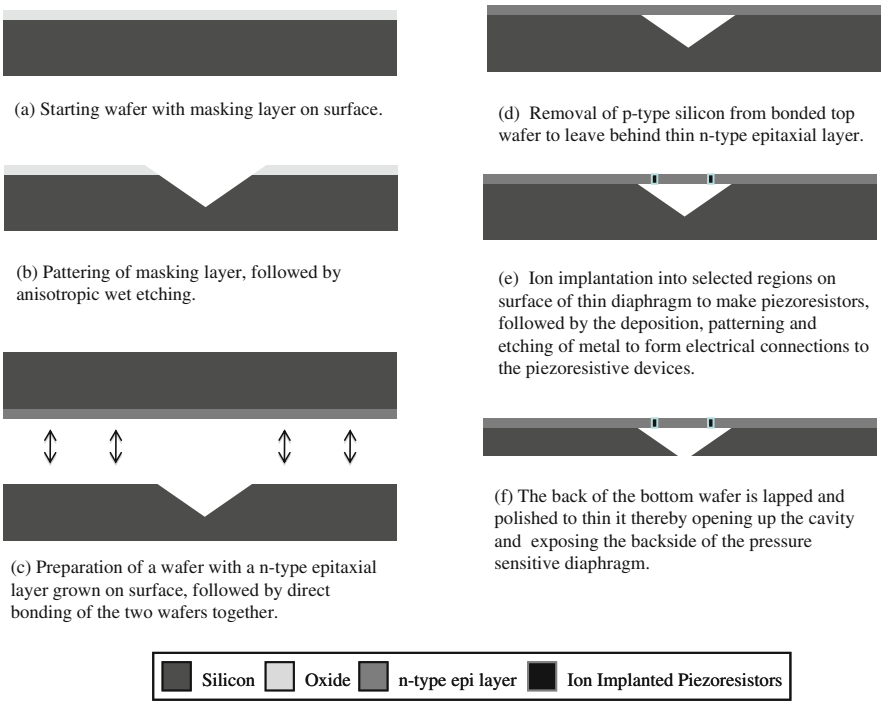


Fig. 14.43 Cross-section of the process technology for the NovaSensor pressure sensor

removed using a controlled-etch process thereby leaving only the bonded epitaxial layer on the bottom wafer (Fig. 14.43d). Piezoresistors are then made in selected regions on the silicon diaphragm using ion implantation (Fig. 14.43e). Metal is deposited, patterned, and etched to form electrical connections to the piezoresistors on the diaphragm. Next, the composite wafer is lapped and polished back to reduce its thickness to about 140 μm thereby opening up the cavity from the backside of the diaphragm (Fig. 14.43f).

14.8.2.9 Microelectronics Wafer-Bonded (Bulk) Accelerometer Process (Ford Microelectronics)

A multitude of process sequences have been developed over the last 20 years to fabricate accelerometers. In addition to surface micromachined process sequences, bulk micromachined and mixed surface–bulk micromachined process sequences have been developed. This section examines a mixed process technology developed by Ford Microelectronics, Inc. (FMI). The process contains wafer-level encapsulation that is a classic example of lateral electrical feedthroughs. The goals of this process were to provide a wafer-level, hermetic encapsulation of a silicon accelerometer. At the time of its development, it provided a technology that was robust to the stresses of the plastic packaging process and thus allowed low-cost plastic packaging. It also provided an inert environment (dry nitrogen, neon) that could be maintained for >15 years. The sensing principle is a torsional accelerometer where unequal masses are formed over a central fulcrum. The side with the larger mass moves more under the influence of acceleration, thus providing a net change in capacitance one side to the other.

The FMI process is a three-wafer process that includes a Pyrex® interconnect/electrode substrate, a silicon device wafer, and a silicon cap wafer [28]. Each of the three wafers includes shared unit process steps, but they can be processed independently and in parallel. Starting with the 7740 Pyrex substrate, the counterelectrodes and interconnects are a deposited metal stack comprised of Cr/Au/Pt/Au/Cr (1500 Å), which is deposited by evaporation and patterned by liftoff (see Fig. 14.44a). This thickness is acceptable for DC interconnection of the electrostatic MEMS device. In the next steps, Pyrex is sputtered (1.5 μm) over the interconnects to provide a semiplanarized bonding interface (Fig. 14.44b). It was found for these metal and Pyrex film thicknesses that the surface was adequately planarized to form a hermetic anodic bond. For thicker metal films necessary for RF performance (0.5–1 μm or thicker), the sputtered Pyrex layer would need to be thicker and a CMP process would need to be introduced. Following the sputtered Pyrex deposition, electrical vias are wet etched (Fig. 14.44c) and filled with an evaporated Cr/Au/Pt contact metallization (Fig. 14.44d).

The device wafer process begins with a silicon wafer that has an n-epitaxial silicon (epi) layer, which is grown above a p+ etch-stop layer. The epi layer is etched in two stages. First it is time-etched through part of its thickness leaving a protrusion that will become the central fulcrum. Photoresist is applied a second time to form the outline of the full structure. A further etch, which ends on the p+ etch stop layer, forms the moving mass's structure (Fig. 14.44f).

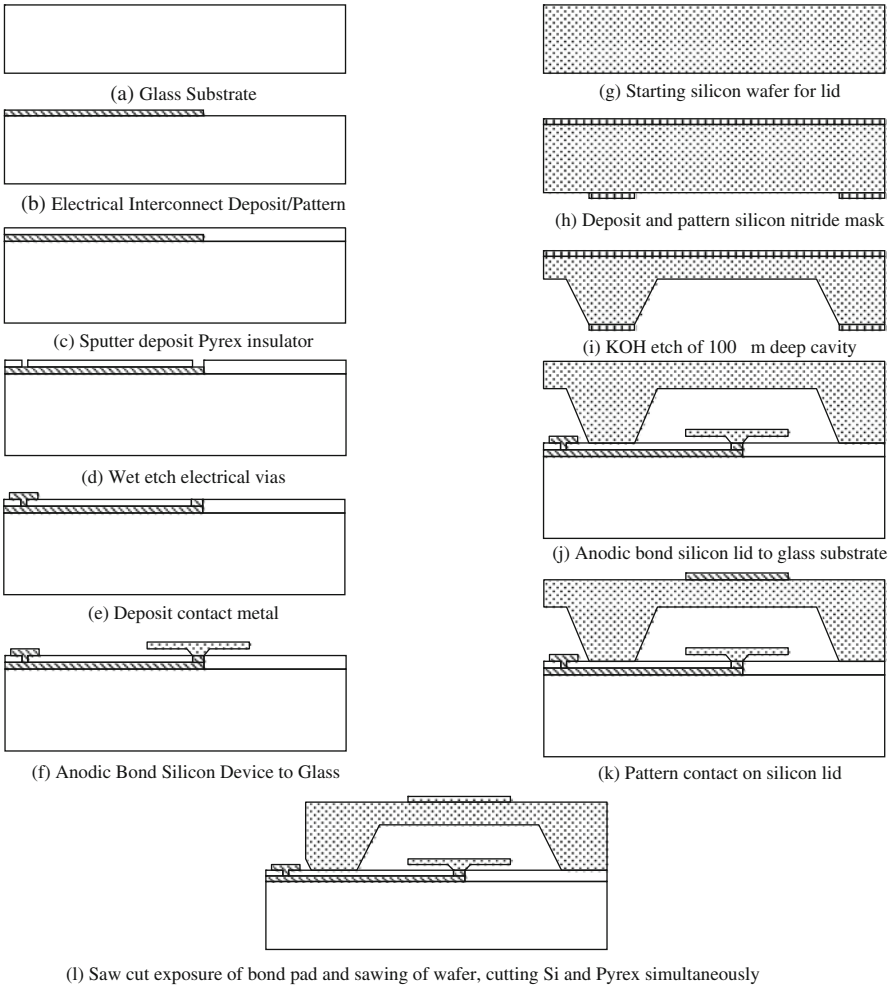


Fig. 14.44 Silicon micromachined wafer-bonded accelerometer and wafer-level encapsulation process: (**a**) starting glass substrate, (**b**) deposition of metallization, (**c**) Pyrex deposition for planarization, (**d**) etch to expose metallization for vias, (**e**) via deposition, (**f**) Pyrex wafer after the bonding and dissolved wafer etch back of the device wafer to yield the accelerometer proof mass's fulcrum bonded to the metallization, (**g**) starting silicon lid wafer, (**h**) deposition of backside etch mask, (**i**) backside KOH etch, (**j**) lid wafer bonded to the Pyrex wafer, (**k**) patterned lid metallization, (**l**) final structure showing saw cut used to expose the bond pads on the Pyrex wafer

The silicon wafer and the Pyrex wafer are then anodically (i.e., electrostatically) bonded together. The protruding central fulcrum contacts a metal pad on the glass wafer allowing an electrical connection to the moving mass. In order to release the moving mass, the n-"handle" portion of the wafer is completely etched away from the backside in a type of dissolved-wafer process. In this case the backside etch stops on the p+ layer. The p+ layer is then stripped leaving the structure shown in Fig. 14.44f.

The third wafer is a silicon wafer ((100) n-silicon) used as the lid (Fig. 14.44g). The first step deposits Si_xN_y on both sides of the wafer and patterns one side, such that the Si_xN_y acts as a masking layer for a KOH etch (Fig. 14.44h). The KOH etches a 100 μm deep cavity to provide a volume for the MEMS device and to provide standoff height for the sawing process to expose the bond pads (Fig. 14.44i).

At this point the silicon wafer can be stored until it is needed for a mating wafer, when the silicon nitride is stripped so the silicon wafer can be bonded to the Pyrex wafer. One consideration with this stack is the thermal mismatch between the silicon wafer and the Pyrex wafer. The bonding process is performed with 300 V and 315°C, where there is only a small difference in the CTEs of the two materials. The silicon lid is shown bonded to the Pyrex wafer including the MEMS devices in Fig. 14.44i. In Fig. 14.44j, a contact is deposited and patterned on top of the lid for electrical connection via wire bond.

During the wafer sawing process, the first saw cuts partially saw through the silicon wafer to expose the bond pads. With the bond pads exposed, a wafer-level electrical test can be performed to identify known good die and verify functionality. After the functional test, the sawing process is completed to singulate the die (Fig. 14.44k).

14.8.2.10 Single-Crystal Reactive Etching and Metallization (SCREAM) (Cornell University)

The SCREAM process was developed at Cornell University in the mid-1990s and is used to implement high-aspect-ratio single-crystal silicon microstructures that have metallized sidewalls [29]. It can be used for a variety of applications, but the primary application has been for inertial sensors because the sidewall capacitance of the high-aspect-ratio microstructures is relatively high compared to many other process technology approaches. The SCREAM process technology uses only a single mask thereby making it extremely simple and inexpensive. The low temperatures of the SCREAM process also make it compatible with CMOS integration.

The process begins with a single-crystal silicon wafer that has a layer of silicon dioxide grown or deposited on the top surface. The oxide layer varies between 1 and 2 μm in thickness. Photolithography is performed to pattern the oxide layer thereby exposing the underlying silicon in certain regions (Fig. 14.45a). A deep reactive ion etch is performed to a depth that depends on the structural height of the device, but usually varies between 4 and 20 μm. Next, a layer of conformal silicon dioxide is deposited by PECVD to a thickness of about 0.3 μm (Fig. 14.45b). A thinner oxide layer may be used if a higher aspect ratio is desired. The purpose of this oxide layer is to protect the top and sides of the structures made in the single crystal silicon using DRIE in the previous processing step. The oxide is removed from the bottom of the DRIE etched trenches using a RIE (Fig. 14.45c).

Another DRIE etch is performed to increase the depth of the trench into the silicon wafer by about 3–5 μm (Fig. 14.45d). This purpose of this silicon etch is to expose the silicon underneath the silicon structural elements. The silicon under the structural elements is then removed to release them using an isotropic plasma silicon

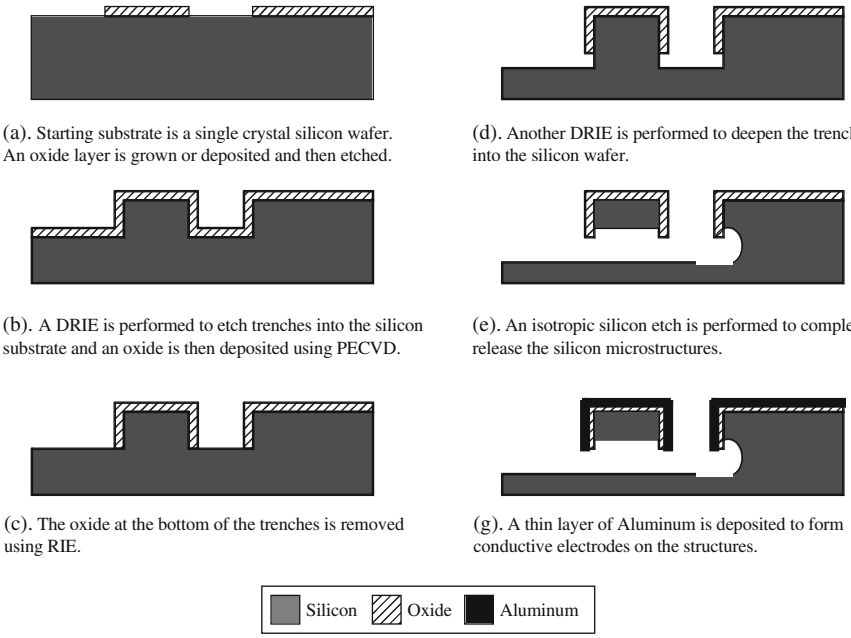


Fig. 14.45 SCREAM process sequence

etch (either a plasma isotropic SF_6 etch or a xenon di-fluoride [XeF_2]) as shown in Fig. 14.45e. This etch chemistry is highly selective to the oxide masking layer that is used to protect the silicon structural elements. A thin layer of aluminum having a nominal thickness of 3000 Å is then sputter deposited onto the wafer (Fig. 14.45f). The sputter deposition results in the metal coating the top of the structure as well as the sides to form conductive electrodes that can be used for capacitive sensing or electrostatic actuation. The devices are completed and the wafer can be diced and packaged.

14.8.2.11 High-Aspect-Ratio Combined Poly and Single-Crystal Silicon (HARPSS) MEMS Technology (University of Michigan and Georgia Tech)

The HARPSS process technology was originally developed at the University of Michigan [30] with further development performed at the Georgia Institute of Technology. It enables the fabrication of microstructures from polysilicon and single-crystal silicon having thicknesses varying from the tens to the hundreds of microns as well as creating microstructures having extremely narrow gaps between electrodes. The primary application of the HARPSS process technology has been for inertial sensors (i.e., accelerometers and gyroscopes) wherein the large electrode

areas of the thick sidewalls combined with the narrow gaps allows very large capacitance values to be realized. The HARPSS process derives some of its attributes from the hex–sil process technology wherein a mold made in silicon using DRIE has a thin layer of oxide deposited on the sidewalls and the mold trenches are filled with LPCVD polysilicon. Once the oxide is removed in HF, the polysilicon microstructures are completely released and free to move [31].

The HARPSS process is a six-mask process technology and begins with a single-crystal silicon wafer. A thin layer of silicon nitride (SiN) is deposited by LPCVD to a thickness of 2000–2500 Å. The SiN layer is patterned and etched to serve as an insulator between the bonding pads of the microstructure and the substrate. Deep high-aspect-ratio trenches are then etched into the silicon substrate using DRIE to a depth of 50 to a few hundred microns (Fig. 14.46a). The depth of the trench etch determines the height of the microstructures. Next, a highly conformal thin layer of silicon dioxide is deposited using LPCVD (Fig. 14.46b). A conformal layer of polysilicon is then deposited by LPCVD at 588°Celsius to refill the oxide-coated trenches etched into the silicon substrate. This layer of polysilicon will form a structural material layer for the devices made by this process and therefore must be doped to increase its electrical conductivity. Boron doping is preferred over phosphorus doping due to the slower etch rate of boron-doped polysilicon in HF during long release etches. The doping of the polysilicon is performed by diffusion of boron into the oxide trench coating layer prior to the polysilicon deposition. After the polysilicon is deposited, a drive-in diffusion is performed to diffuse the boron from the oxide into the polysilicon.

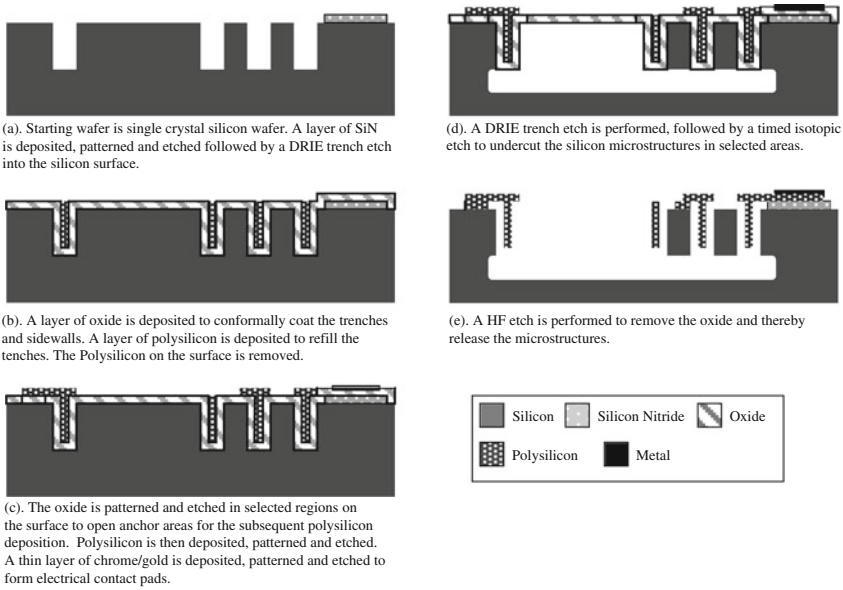


Fig. 14.46 HARPSS process sequence

After the trenches have been refilled with polysilicon and the drive-in diffusion has been performed, the polysilicon layer on the surface is patterned and etched. The underlying oxide layer is also patterned and etched to open up areas that act as anchor points for the microstructures. Another layer of polysilicon is deposited, doped, patterned, and etched on the surface. A metal layer of chrome/gold is deposited to a thickness of 3000 Å by evaporation and then patterned and etched to form electrical bonding pads (Fig. 14.46c). A DRIE etching is performed into the silicon substrate, followed by a timed dry isotropic SF_6 silicon etch to undercut the silicon microstructures (Fig. 14.46d). Lastly, a HF etch is performed to remove the oxide layer and thereby completely release the microstructures (Fig. 14.46e).

Figure 14.47 shows a SEM of a gyroscope fabricated using the HARPSS process technology wherein exotically shaped structures such as the meandering supporting tethers can be implemented rather easily.

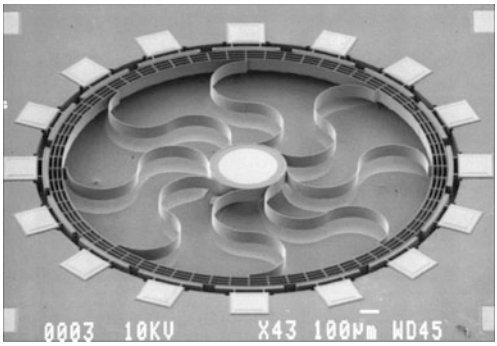


Fig. 14.47 SEM of a gyroscope fabricated using the HARPSS process technology. The meandering-shaped supporting tethers are 80 µm in height and 4 µm wide (Reprinted with permission, copyright Prof. Farrokh Ayazi at the Georgia Institute of Technology)

14.8.2.12 Hybrid MEMS (Infotonics)

There are many surface micromachining techniques such as the MUMPS and Summit processes that use multilayer polysilicon as the main structural materials for MEMS devices. A few SOI process modules such as SOI MUMPS (from MEMSCAP), *a*MEMS™ (from Teledyne, see also Section 14.8.2.18 in this chapter), MigraGem (from Micralyne), and MEMSOI (from Tronics Microsystems) processes have recently become available to create MEMS structures using the single-crystal silicon (SCS) layer on SOI wafers [32–35]. There are a couple of advantages of using the SCS layer as the MEMS structural material. First, compared to polysilicon, SCS has excellent and reproducible mechanical properties such as a high Young's modulus, a repeatable Poisson ratio, and no residual stress or stress gradients. Second, the conductivity of the SCS can be finely controlled over five orders of magnitude. The SCS also has better optical properties such as lower optical loss in infrared range than other materials like polysilicon. However, SOI wafers have only one SCS layer and it is difficult and costly to add more SCS layers later in the fabrication to build a MEMS structure. The SOI process modules mentioned

above are based on only one SCS layer. Thus, there is a limitation on the variety of MEMS devices that can be built by these SOI processes.

The hybrid MEMS process, initially developed at Xerox [36] and now available at Infotonics Technology Center [37], can be used to create MEMS structures from one polysilicon layer and one SCS layer on SOI wafers. Another hybrid process for fabricating inchworm motors and hinged SOI legs using five masks has also been developed at BSAC [38]. The advantage of the hybrid process is to combine the flexibility of polysilicon processing and the unique material properties of SCS for MEMS devices. Surface micromachining using polysilicon has been studied since the 1980s and the process capability of polysilicon has been widely accepted. The hybrid process can use the polysilicon as the mechanical support structures such as dimples and anchors, and use SCS for the critical structures such as optical waveguides. Compared to polysilicon surface micromachining, the challenges of this process are twofold. First, SCS and the buried oxide (BOX) layer already exist on the SOI wafer in the beginning. Many desired mechanical features such as dimples and anchors have to be added to the existing SCS layer. Second, depending on the thickness of the SCS layer, surface topography after patterning the SCS layer can be greater than the typical polysilicon micromachining.

The complete hybrid process is a 13-mask integrated process including a 3 μm polysilicon layer for static mechanical structures and anchoring, and a 5 μm SCS layer to provide optimum mechanical and optical performance for optical MEMS devices (waveguides and optical switches). Table 14.2 shows examples of MEMS and MOEMS designs that can be fabricated using the entire process or the subsets of the all-hybrid process. Because the optical devices are very sensitive to the

Table 14.2 Subsets of hybrid MEMS processes for different applications [37]

Mask names	Mask number	Advanced optical	Waveguide	Rapid optical	Rapid mechanical
SCS shallow etch	1				√
SCS doping	2		√		√
SCS anchor etch	3	√			√
SCS dimple etch	4	√			√
SCS gap fill		√			
SCS precise cut	5		√	√	
SCS medium etch	6		√	√	
SCS final cut	7	√	√		√
TEOS and CMP		√			
SCS expose	8	√			
Silicon nitride	9	√			
Polysilicon	10	√			
TEOS etch	11	√			
Bulk Si DRIE	12				
Metal	13	√			√
Total masks		8	4	2	6

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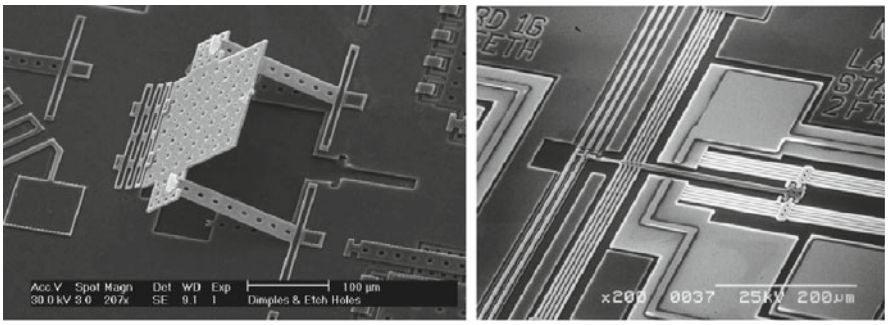
lithography dimension and alignment accuracy, six masks are used to etch the pattern on the SCS layer. Although extra masks increase the cost of the process, it is sometimes necessary to achieve the desired design intent. The advanced optical module, developed by the MOEMS Manufacturing Consortium, is an 8-mask subset of this process [39]. Another example is waveguide devices such as AWG, which is a 4-mask subset process [39]. An attractive feature of the Hybrid SOI Process is that many subsets of the entire process can be used independently. Each subset can carry a specific design function and can be made with a rapid turn-around time. Figure 14.48 shows some examples of optical MEMS devices fabricated using the hybrid MEMS process. The SCS layer was used to form an out-of-plane reflective micromirror in Fig. 14.48a, and the optical waveguide switch and latching structures using heat actuators is shown in Fig. 14.48b [37].



(a) (b)

Fig. 14.48 Optical MEMS devices fabricated using hybrid MEMS: (**a**) fixed reflective micromirror; (**b**) optical waveguide switch with heat actuators [37] (Reprinted with permission, copyright 2005, IEEE)

The starting SOI wafers consist of a 5 μm thick SCS layer on top of a 1 μm BOX layer. Figure 14.49 shows the schematic cross-section view of this process. The SCS layer is etched 0.3 μm deep using the first mask (SCS shallow etch, Fig. 14.49a). This etch is used to pattern the fiducial and functional structures such as optical gratings. The second mask (SCS doping, Fig. 14.49b) is for phosphorus doping to increase conductivity in the SCS layer. The doping in SCS will increase optical loss and this mask can confine the doping to the desired electrically conductive areas.

The third mask (SCS anchor) and the fourth mask (SCS dimple, Fig. 14.49c were used for DRIE on SCS. The anchor etch is completed through the entire BOX to provide mechanical connection to the underlying wafer. The dimples are antistiction structures and the dimple etch is only half-way through the BOX. A layer of polysilicon is deposited to fill the anchor and dimple holes. Polysilicon is then blanket-etched away to expose the SCS layer again (Fig. 14.49d). The next mask (SCS precision cut, Fig. 14.49e) is a high precision cut with all patterns under the same dimension to avoid loading effect in dry etching. The sixth mask (SCS medium etch, Fig. 14.49f) offers an intermediate SCS etch, that is, not all the way through to

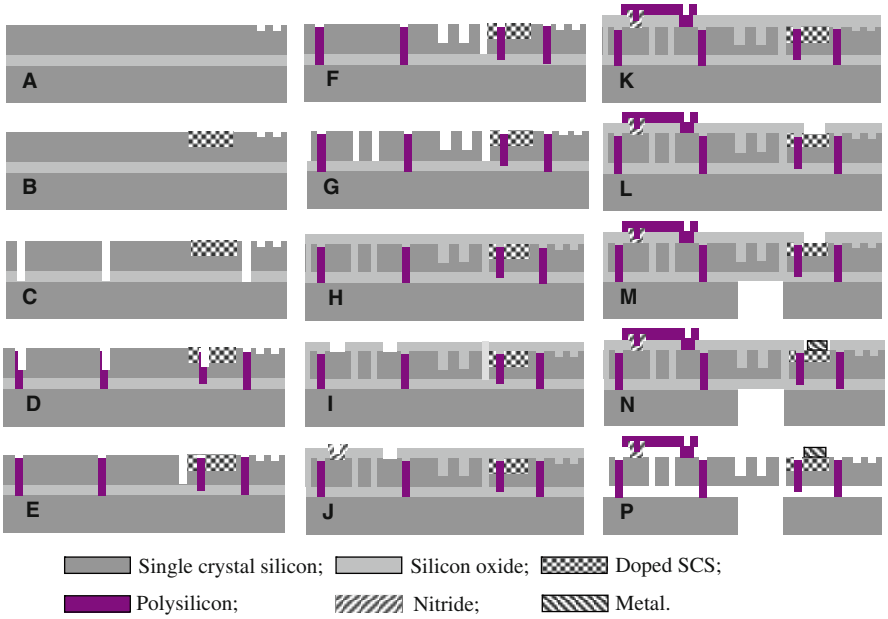


Fig. 14.49 Schematic cross-section view of fabrication process [37] (Reprinted with permission, copyright 2005, IEEE)

the BOX. It is used to pattern structures such as rib waveguides and gratings within the SCS layer. The last mask (#7) on the SCS layer (SCS final cut, Fig. 14.49g) is another DRIE on SCS for actuator patterns, which removes large areas in SCS. The pattern sizes can be in wide ranges and the loading effect can be eliminated by overetching.

One of the key challenges for MEMS fabrication is to overcome the topography created by DRIE on the SCS. After large areas of the SCS layer are etched away, it is very difficult to use thin photoresist for photolithography. Thus, 8 μm LPCVD low-stress tetraethylorthosilicate (TEOS) oxide was deposited and chemical-mechanical planarization was performed to minimize topography after DRIE in the SCS layer. A few cycles of deposition and a blank etch process have been developed to eliminate buried keyholes in the TEOS oxide layer. The thick oxide layer is then planarized using CMP, which uses a silicon nitride layer under the TEOS as a polishing stop. Hence, it is desired to select the slurry and pad for high selectivity between the oxide and nitride. Another 2 μm of TEOS oxide is deposited after CMP (Fig. 14.49h) as the sacrificial layer.

The eighth mask (SCS expose, Fig. 14.49i) opens up the 2 μm TEOS oxide. A layer of silicon nitride is deposited and patterned (mask #9) to provide electrical isolation (nitride, Fig. 14.49j). Mask #10 is for a 3 μm low-stress-doped LPCVD polysilicon (polysilicon, Fig. 14.49k). This polysilicon layer is used for static mechanical structures. Mask #11 (TEOS etch, Fig. 14.49l) is used to open

areas in the TEOS oxide for metal contact. The underlying wafer can be etched from the backside by DRIE using mask #12 (bulk Si etch, Fig. 14.49m). Metal such as Cr/Au is deposited using liftoff techniques with mask #13 (metal, Fig. 14.49n). The final release step can be a wet process (HF solution) or a dry process (HF vapor) (Fig. 14.49p).

In summary, six masks are used for patterning the SCS layer including three different etching depths in the SCS layer (shallow, intermediate, and full). The various etching steps enable designs such as optical gratings, channels, waveguides, and actuators. Although it may cost more for extra masks, there are a few advantages: (1) precise dimensional control (within ±0.2 μm error for optical devices), (2) dimples on released SCS structures (preventing stiction), and (3) anchoring of the SCS layer (for long release in HF). The mask for confining doping areas (mask #2) avoids the large loss of optical signals in waveguides due to doping. Polysilicon fill and TEOS oxide fill level the surface topography and enable the multilayer MEMS structures.

14.8.2.13 Silicon-On-Glass (University of Michigan)

The silicon-on-glass (SOG) process was developed at the University of Michigan [40] and has been used in applications requiring high-aspect-ratio and thick single-crystal silicon structures. The applications and devices that the SOG process has been used in include: inertial sensors (e.g., accelerators and gyroscopes for automotive, medical, industrial, and aerospace applications), microactuators (e.g., microvalves, micropumps, optical devices, comb drive actuator devices), and micromechanical resonators (e.g., RF MEMS devices, communication devices, optical devices), and several others.

The SOG process utilizes a relatively thick single-crystal silicon device layer (100–150 μm in thickness) and a high-aspect-ratio etch process (up to 50 to 1 as quoted as possible by the University of Michigan, but typically a 15 to 1 aspect ratio is more common) to realize thick and high-aspect-ratio microstructures. A major feature is that the single-crystal silicon layer is supported on an insulating glass substrate thereby eliminating the expense and complexity of using SOI wafers. The SOG process can be performed on standard microelectronic wafers (such as CMOS wafers made through an IC foundry process) or die using postprocessing steps that are compatible with microelectronics.

The SOG process starts with a 500 μm thick glass wafer, usually a borosilicate glass wafer such as Pyrex 7740 so as to have a thermal expansion coefficient matched to that of silicon (Fig. 14.50). Photolithography is performed (mask level 1) on the top surface of the glass wafer (and a protective photoresist is deposited on the wafer backside) and subsequently the wafer is etched in a wet chemical etchant solution (i.e., hydrofluoric acid) to form recesses approximately 10 μm in depth (Fig. 14.50b). This etch is isotropic in nature and therefore the undercut of the glass must be considered in the mask layout.

Typically, the first mask includes anchors that will be temporary and serve to support the silicon device layer during fabrication. These anchors will be removed

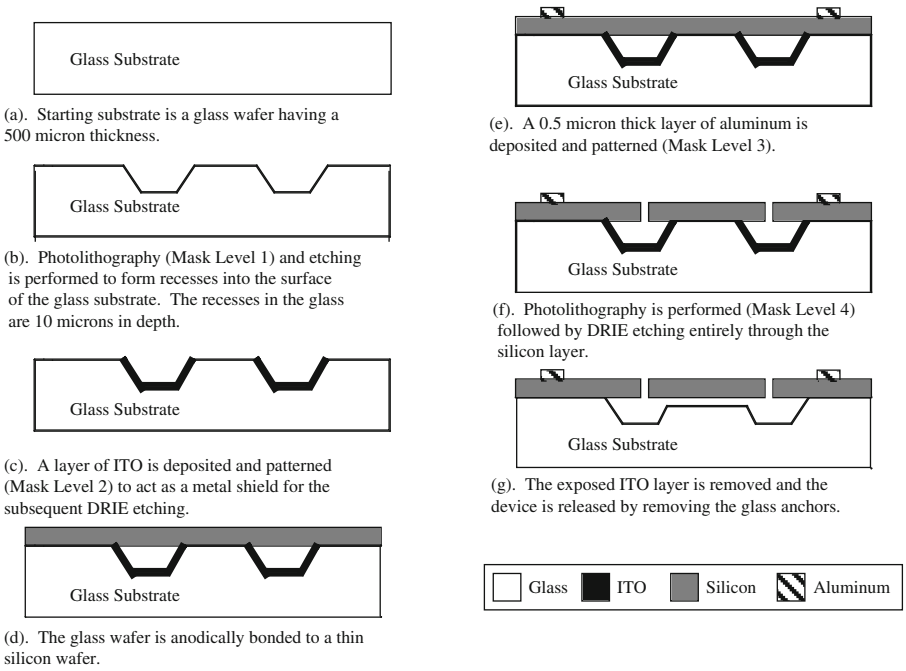


Fig. 14.50 Process sequence for the silicon-on-glass process

later in the process and have a 30 μm edge length dimension as drawn on the first mask level. Next a layer of indium tin oxide (ITO) is deposited at a thickness of 2000 Å. ITO is selected due to its properties of being both conductive and transparent. The transparency is important to allow inspection of the wafer during fabrication whereas the conductivity is important to prevent charge buildup on the glass wafer surface that would seriously degrade the quality of the subsequent DRIE processing steps used to define the silicon device layer. Photolithography is performed (mask level 2) to define the pattern in the ITO layer that can be etched or ion milled. Alternatively, liftoff can be used to pattern the ITO layer (Fig. 14.50c).

The glass wafer is then anodically bonded to a single-crystal silicon wafer having a nominal thickness of 100–150 μm. The silicon wafer having this thickness is extremely fragile and care must be exercised during handling to prevent yield loss. Alternatively, the glass wafer can be bonded to a thicker silicon wafer, but at the expense of having to thin down the silicon wafer using lapping and polishing. Also, because glass wafers do not have total thickness variations comparable to those of silicon wafers, the resultant silicon device layer using lapping and polishing to thin the wafer back will likely be of variable thickness (Fig. 14.50d).

The anodic bonding is performed at a voltage potential of 1000 V and a temperature of 350°C. A layer of aluminum of thickness of 0.5 μm is deposited on the silicon wafer surface. This metal layer will be used to make ohmic contact to

the MEMS devices. Photolithography is performed (mask level 3) to define the aluminum layer which is subsequently etched using a wet chemical etchant solution (Fig. 14.50e). Photolithography is performed (mask level 4) to define patterns to be etched into the silicon device layer. The silicon layer is then etched using a high-aspect silicon DRIE etch process all the way though the silicon layer and stopping at the glass substrate (Fig. 14.50f). The DRIE etch rate will vary depending on the amount of exposed silicon as well as the range of feature sizes. In general, smaller gaps etch considerably more slowly than large areas in DRIE and therefore a considerable overetch may be required in order to complete the etch. The exposed ITO layer is then removed using a wet etchant. Next, the glass anchors are removed using a wet chemical HF solution (Fig. 14.50g). Lastly, the wafer is then diced into individual die. Figure 14.51 shows the examples of different types of MEMS devices made with the SOG process sequence. MEMS implemented with the SOG process can be merged with microelectronics by flip-chip bonding of the CMOS die to the exposed electrical pads made on the silicon device layer. However, the relatively low doping (i.e., high resistance) of the silicon device layer must be considered in selecting the CMOS process and device design.

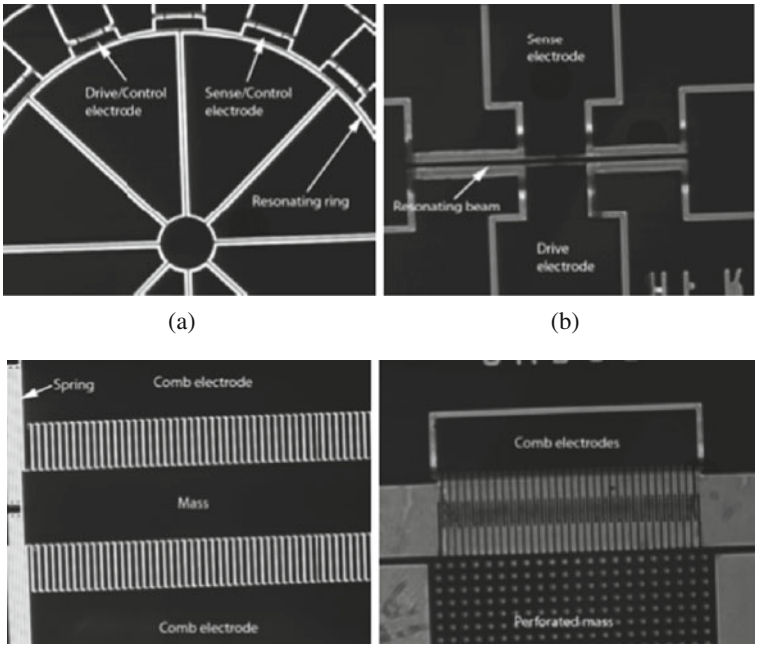


Fig. 14.51 Example of MEMS devices made using the SOG process: (**a**) a vibrating ring gyroscope; (**b**) a beam resonator; (**c**) a perforated mass with comb electrodes; (**d**) an accelerometer

14.8.2.14 SOI MUMPS™ (MEMSCap)

The SOIMUMPS™ process is a simple double-sided etch and two-step metal process that utilizes the predefined and fabricated layers found in silicon-on-insulator starting material (Fig. 14.52a) rather than grown layers one sees in the other MUMPs processes. By using this type of starting material, the process can be flexible enough to offer multiple thicknesses of etched silicon using the same mask set.

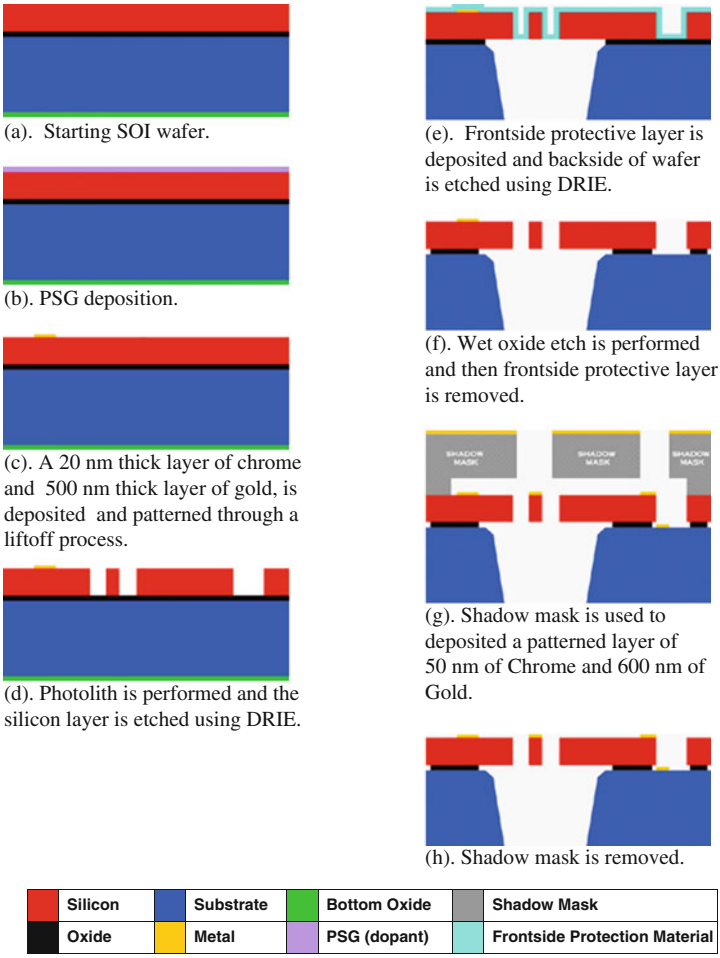


Fig. 14.52 MEMSCap's SOIMUMPS process sequence. (**a**) Starting SOI wafer. (**b**) PSG deposition. (**c**) A 20 nm thick layer of chrome and 500 nm thick layer of gold, is deposited and patterned through a liftoff process. (**d**) Photolith is performed and the silicon layer is etched using DRIE. (**e**) Frontside protective layer is deposited and backside of wafer is etched using DRIE. (**f**) Wet oxide etch is performed and then frontside protective layer is removed. (**g**) Shadow mask is used to deposited a patterned layer of 50 nm of Chrome and 600 nm of Gold. (**h**) Shadow mask is removed (Reprinted with permission, copyright MEMSCap, Inc.)

The process begins with doping of the SOI device layer using PSG which is subsequently stripped (Fig. 14.52b) [41]. The first metal layer, a metal stack of 20 nm of chrome and 500 nm of gold, is patterned through a liftoff process (PADMETAL) to define finer metal features for bond pads and routing lines (Fig. 14.52c). Because this metal is exposed to high temperature during the subsequent process, surface roughness tends to be higher and not suitable for low-loss optical mirror applications.

Silicon is lithographically patterned with the second mask level (SOI), and etched using deep RIE (Fig. 14.52d). This etch is performed using inductively coupled plasma (ICP) technology; a special SOI recipe is used to virtually eliminate any undercutting of the silicon layer when the etch reaches the buried oxide of the SOI substrate.

A frontside protection material is applied to the top surface of the silicon layer to protect frontside features from the rigors of the backside etch. The substrate layer is lithographically patterned from the bottomside using the third mask level, TRENCH. This pattern is then etched into the bottom side oxide layer using RIE. DRIE is subsequently used to etch these features completely through the substrate layer, allowing for through-hole structures (Fig. 14.52e). A wet oxide etch process is then used to remove the buried oxide layer in the regions defined by the TRENCH mask. The frontside protection material is then stripped in a dry etch process which "releases" any mechanical structures in the silicon layer that are located over through-holes defined in the substrate layer.

The remaining "exposed" oxide layer is removed from the wafers using a vapor HF process to minimize stiction. The exposed oxide layer is removed to allow for electrical contact to the substrate and to provide an undercut in the oxide layer that will prevent metal shorts between the silicon layer and the substrate layer (Fig. 14.52f). The blanket metal layer, consisting of 50 nm Cr + 600 nm Au, is deposited and patterned using a shadow masking technique (Fig. 14.52g). The shadow mask is prepared from a separate double-sided polished silicon wafer. Standoffs are incorporated into the side of the shadow mask that will contact the SOI wafer, to avoid any contact with patterned features in the silicon layer. The shadow mask is then patterned with the BLANKETMETAL mask, and through holes are DRIE etched. The shadow mask is then aligned and temporarily bonded to the SOI wafer, and the metal is evaporated using an e-beam tool. Metal is deposited on the top surface of the silicon layer only in the through hole regions of the shadow mask. After evaporation, the shadow mask is removed, leaving a patterned metal layer on the SOI wafer (Fig. 14.52h). Figure 14.53 is a SEM of some micromechanical structures fabricated using the MEMSCap SOIMUMP^{TM} process technology.

14.8.2.15 LIGA (CAMD, etc.)

LIGA is the German acronym for lithography, electroplating, and molding (*Lithographie, Galvanik, und Abformung*) and is a very useful process technology for making extremely high-aspect-ratio microstructures with high precision and smooth sidewalls. The LIGA process was developed in the late 1970s at the

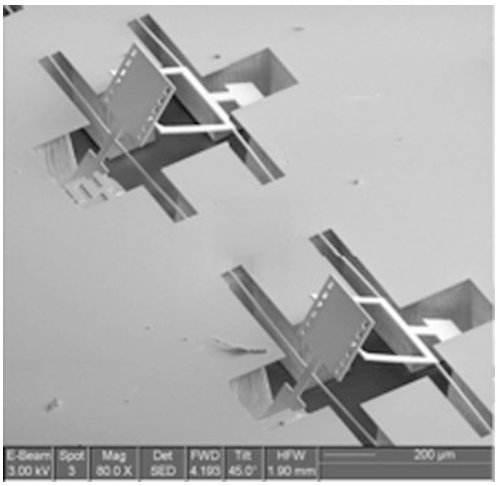


Fig. 14.53 SEM of some devices fabricated using MEMSCap's SOIMUMPS™ process sequence (Reprinted with permission, copyright MEMSCap, Inc.)

Institut für Kernverfahrenstechnik (IKVT), today the Institute for Microstructure Technology (IMT) in the Forschungszentrum Karlsruhe GmbH [42–44]. Several institutes now use the LIGA process for developing prototype structures and components often in collaboration with industry [45]. The benefits of LIGA principally derive from the use of deep X-ray lithography. Although LIGA-made parts are relatively demanding to fabricate, the technology is well suited for massive inexpensive replication whereby the first-made part is used as a metal mold insert for hot embossing or injection-molding replication of the pattern into another material. Some of the features and advantages of the LIGA process include: providing a large layout freedom for the mask geometry; high aspect ratios of 20 to 1 are typical and extreme ratios up to and beyond 100 to 1 have also been achieved; the sidewalls of the structures made with the process are extremely parallel and have nearly vertical sidewall angles (e.g., typical deviation of sidewalls is about 1 μm for structures 1 mm in height); the sidewalls of the LIGA structures are very smooth with R_a values ranging from a few 10 nm to about 200 nm suitable for optical micromirror surfaces; the precision in the lateral directions of LIGA-made structures is only a few micrometers even over distances of several centimeters; and, it is also possible to create multilevel structures using a double exposure process [46] as well as different sidewall angles by tilting and rotating the sample during exposure [47].

The complete LIGA process technology involves several main fabrication steps that are described below and illustrated in Fig. 14.54. The fabrication begins with the making of a suitable X-ray mask, which is typically composed of a thick gold layer patterned using optical lithography (not shown) [49]. The patterned gold layer will act as an absorber layer for the subsequent X-ray exposure. The X-ray mask is used to expose a thick resist layer on a substrate material (usually Si) that is composed of polymethylmethacrylate (PMMA) at a thickness ranging from a few 10 μm up to 3 mm. The PMMA layer is exposed on the substrate using deep X-ray lithography (Fig. 14.54b). The substrate will have a plating seed layer, typically a

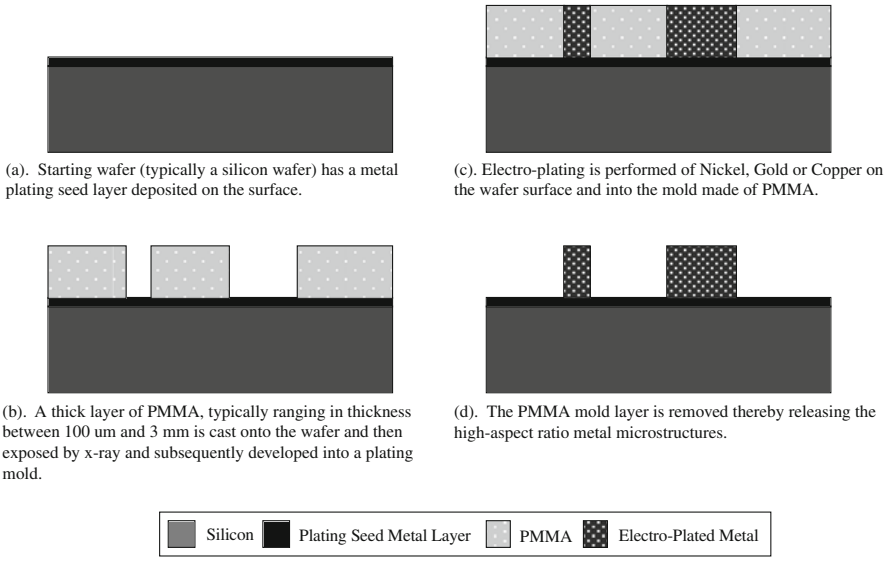


Fig. 14.54 Illustration of the basic LIGA process

titanium layer with a wet chemically etched TiO_2 layer deposited onto its surface prior to the deposition of the PMMA layer (Fig. 14.54a). High-energy X-ray photons are used for this exposure, therefore the developed resist pattern will have extremely smooth and nearly vertical sidewalls. Within the newly created high-aspect-ratio resist mold, a metal, such as gold, copper, or nickel, is electroplated into the features thereby forming metal structures having the dimensions and form factor, but reverse polarity, of the resist mold (Fig. 14.54c). The resist is then removed to release the metal high-aspect-ratio microstructures (Fig. 14.54d). A sacrificial layer may be made on the surface of the plating seed layer to create overhanging microstructures [11]. Optionally, the LIGA-made metal microstructure can be used as a tool insert for a hot embossing process to replicate the features into a polymer material. The polymer parts may be the final parts, or they may be used as molds for electroplating metal to replicate metal parts (also not shown) [50]. Figures 14.55 and 14.56 are SEM images of some structures made with the LIGA process sequence.

14.8.2.16 RF Switch (MEMStronics)

MEMS radio frequency (RF) switches have become of increasing interest for several military and commercial applications due to their low cost and high performance [51]. Most of the MEMS RF switches employ an electrostatically actuated movable electrode that is activated by a voltage potential placed across the movable electrode and a fixed counterelectrode. At a sufficiently high voltage, the electrostatic forces overcome the mechanical stiffness of the movable electrode and make contact with a fixed counterelectrode to close the switch. When the actuation potential is removed,

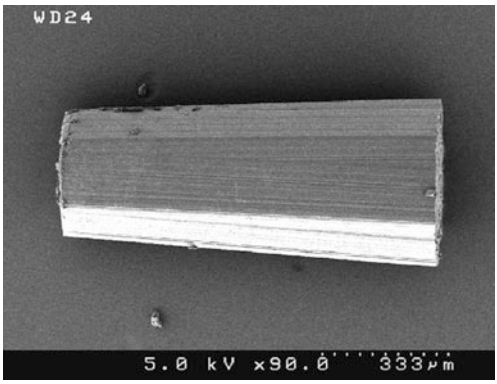


Fig. 14.55 SU-8 posts with slanted sidewalls, ~1 mm tall, ~350 μm diameter made by tilt-and-rotate X-ray lithography fabrication methods [8]

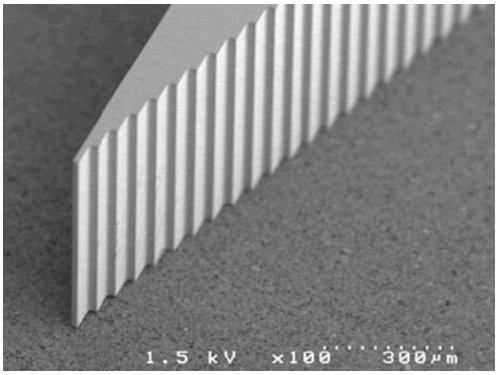


Fig. 14.56 SEM of a high-aspect-ratio grating structure (500 μm tall) with smallest step heights of about 20 μm made from PMMA using X-ray lithography at the CAMD wiggler source [9]

the mechanical stiffness of the movable electrode restores it to its open-state position. These devices possess several inherent advantages compared to competitive technologies such as FETs or p-i-n diode switches. First, the resistive losses are much lower because the MEMS switches are implemented from materials that have a very high conductance at microwave frequencies. This is compared to the much larger resistance levels associated with ohmic contacts of semiconductor-based switches. Second, the MEMS RF switches have nearly perfect I–V linearity which greatly improves their distortion characteristics and power handling as compared to semiconductor-based switches which inherently possess nonlinear I–V behavior. This enables MEMS RF switches to exhibit virtually no detectable harmonics or intermodulation distortion. Third, the electrostatic operation of MEMS RF switches requires negligible current consumption, in either the "on" or "off" states. The main disadvantage of MEMS RF switches is their switching speed, which is typically a few microseconds. Therefore, although MEMS RF switches are unsuited for some applications such as transmit and receive switching, they are highly attractive for applications involving electronic beam steering and forming, such as phased-array antennas.

There are several MEMS RF switches that have been recently introduced into the market. One example is from MEMtronics, a technology that originally was developed at Texas Instruments and then Raytheon Systems. The MEMtronics process technology is reviewed here, but it should be noted that there are not enormous differences between it and the other MEMS RF process technologies.

The process begins with a high resistivity (>5000 Ω cm) silicon wafer (Fig. 14.57) [52]. A thermal silicon dioxide layer is grown on the substrate surface having a thickness of 1 μm. This layer will act as an insulator layer between the metal conduction lines and the silicon wafer. Next, a layer of tungsten having a thickness of 0.5 μm is sputter deposited and then patterned and etched to define the switch electrodes (Fig. 14.57b). Subsequently, a layer of silicon nitride is deposited by PECVD having a nominal thickness of 2000 Å. This layer is patterned and etched to insulate the electrodes (Fig. 14.57c). The dielectric constant of the SiN film is controlled to be nominally 6.7.

Next, a relatively thick layer of aluminum is deposited by evaporation for a total thickness of 4 μm. This layer is then patterned and etched using a wet aluminum etch solution to define the transmission lines and the standoff posts for the top electrode (Fig. 14.57d). Due to the thickness of the aluminum layer combined with the isotropic nature of wet etching, the dimension on the aluminum mask needs to be

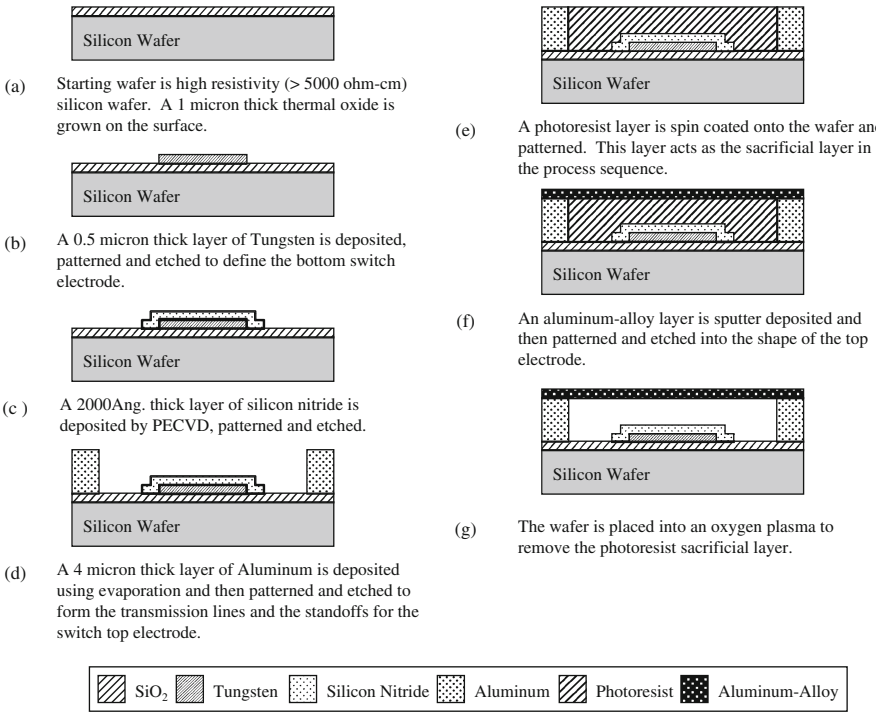


Fig. 14.57 Cross-section of the MEMStronics RF MEMS switch process technology

oversized by approximately 5 μm to compensate for the lateral etch of the aluminum. A photoresist layer that is relatively thick is spin coated onto the wafer and this layer will act as the sacrificial layer in the process sequence (Fig. 14.57e). Once the photoresist layer has been patterned, an aluminum alloy layer is sputter deposited and then patterned and etched into the shape of the switch top electrode (Fig. 14.57f). The sacrificial layer is then removed by placing the wafer into an oxygen plasma thereby releasing the switch (Fig. 14.57g). Small openings (i.e., vias) made in the top electrode metal layer allow the release etch time to be dramatically reduced.

14.8.2.17 MetalMUMPS™ (MEMSCap)

The MetalMUMPS™ process was developed by MEMSCAP. The process involves the electroplating of nickel to implement micromachined MEMS structures and has been used successfully to fabricate microrelays based on thermal actuator technology. The process features include: a nickel primary structural material layer that can also be used as an electrical interconnect layer, a doped polysilicon layer that can be used to make resistors or mechanical elements as well as cross-over interconnects for electrical routing, a silicon nitride electrical isolation layer, and a gold overplating layer that provides for low contact resistance.

The process begins with an n-type single-crystal silicon wafer with (100) orientation and a high resistivity (more than 4000 Ω cm) (Fig. 14.58a) [53]. A 2 μm thick layer of thermal oxide is grown on the wafer surface to provide electrical isolation on the surface, followed by a 0.5 μm thick layer of PSG deposited using LPCVD (Fig. 14.58b). This PSG layer (Oxide1) will act as a sacrificial layer to release the Nitride1 layer and define the trench at the end of the process sequence. Photolithography is then performed on the wafer surface to pattern the Oxide1 layer (mask level OXIDE1). To define the PSG layer features, a wet KOH etch is used that etches at a much higher rate than thermal oxide (Fig. 14.58c). After stripping the photoresist, a 0.35 μm thick layer of low-stress silicon nitride (Nitride1) and a 0.7 μm thick layer of polysilicon are deposited on the wafer using LPCVD (Fig. 14.58d). The polysilicon is doped using ion implantation and annealed to make it electrically conducting. Photolithography is performed (POLY) to pattern the polysilicon using RIE (Fig. 14.58e). After stripping the photoresist, a second layer of low-stress silicon nitride having a thickness of 0.35 μm is deposited by LPCVD (Fig. 14.58f). Photolithography is performed (NITRHOLE) to pattern both the first and second silicon nitride layers using RIE (Fig. 14.58g). The nitride layers serve several purposes: they provide a protective encapsulation for the polysilicon, they define a protective layer on the substrate that determines where Si trench etching occurs later in the process, and a released and patterned nitride area may also be used to provide a mechanical linkage between released metal structures that must be electrically isolated.

After stripping of the photoresist, a 1.1 μm thick layer of PSG (Oxide2) is deposited and annealed, but not released until the end of the process to free the metal mechanical layer (Fig. 14.58h). Photolithography is performed (METANCH)

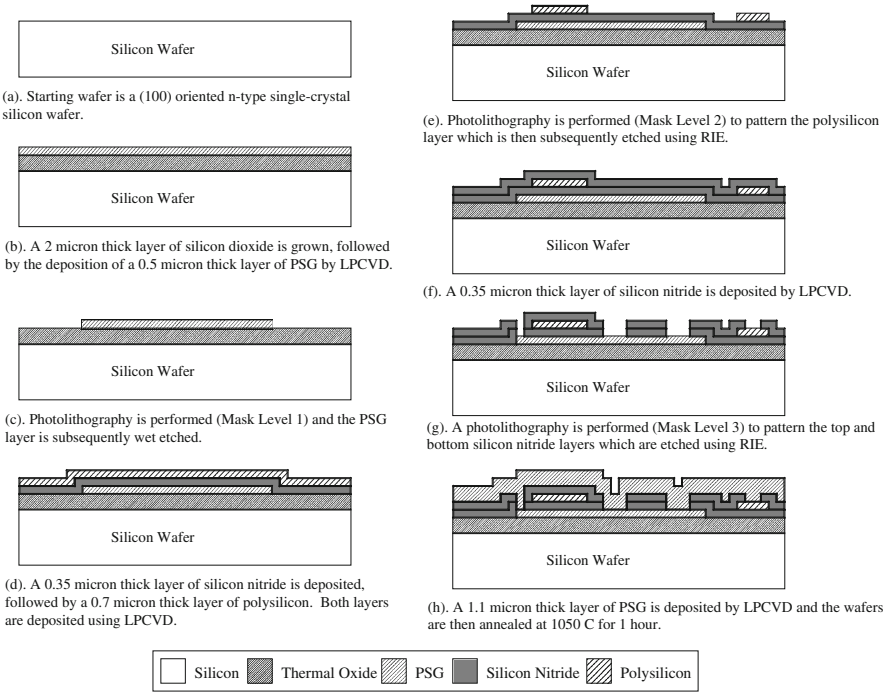


Fig. 14.58 First half of MEMSCap's MetalMUMPS process sequence

to pattern the PSG layer and the features are wet etched but the photoresist is left on the wafers and a stack of 10 nm of chrome and a 25 nm layer of platinum is deposited using evaporation. The metal is patterned using liftoff and remains only in the areas where the PSG layer was removed in the METANCH mask level processing, namely the bottom of the Oxide2 anchors which defines the metal structure anchors (Fig. 14.59a).

A plating base layer composed of a 500 nm thick layer of copper followed by a 50 nm thick layer of titanium is deposited to provide electrical continuity across the wafer surface during the subsequent electroplating process. The final two mask levels are for defining the thick metal features. The METAL mask level is patterned using a thick resist to form the stencil for the electroplated metal layer (Fig. 14.59b). A 20 μm thick layer of nickel is electroplated into the patterned resist (Fig. 14.59c). Subsequently a 0.5 μm gold layer is plated on top of the nickel to provide a suitable pad material for wire bonding of external electrical connections. This combination of 20 μm nickel and 0.5 μm gold forms the metal layer, which serves as the primary mechanical layer and electrical interconnect layer (Fig. 14.59d).

A final plated metal layer, sidewall metal, is a 1–3 μm gold layer plated on selected areas of the sidewall of the metal layer to provide a highly reliable, low-resistance electrical contact while also shrinking the gaps in adjacent electroplated nickel structures. This unique process sequence uses the same feature designs twice

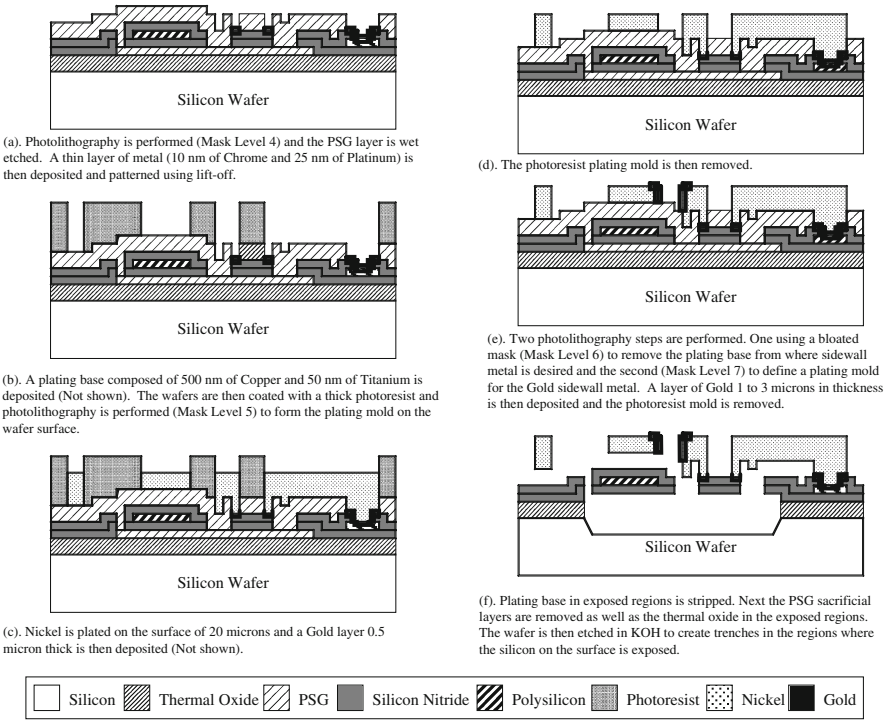


Fig. 14.59 Second half of MEMSCap's MetalMUMPS process sequence

(GOLDOVP) by "fattening up" the features on the first mask and using the as-designed feature sizes on the second mask. The first exposure opens up an oversized or "bloated" area in the thick photoresist layer where sidewall metal is needed followed by the "unbloated" version of GOLDOVP for the desired resist pattern for the actual sidewall metal. The 1–3 μm thick gold sidewall metal layer is then electroplated (Fig. 14.59e). The final steps are the release and Si trench etch. The release is a series of wet chemical etches to first remove the plating base and then the sacrificial layers and the isolation oxide layer over the trench areas. Finally, a wet chemical etch of the silicon, using KOH, is used to form a 25 μm deep trench in the silicon substrate. This occurs in the areas defined by the Oxide1 and NITRHOLE masks. This trench provides additional thermal and electrical isolation (Fig. 14.59f). Figure 14.60 shows a photograph of an electrical relay actuator device made with the MetalMUMPS™ process technology.

14.8.2.18 aMEMS™ (Teledyne)

The *a*MEMS™ process sequence was originally developed by Rockwell Scientific (now Teledyne Scientific and Imaging, LLC) and is a versatile fabrication process using silicon-on-insulator wafers. The process sequence involves the transfer of

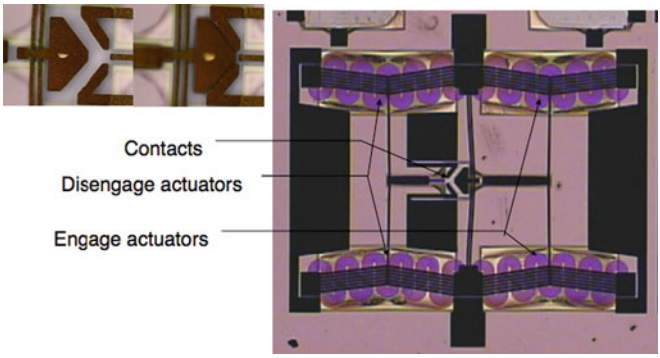


Fig. 14.60 Microactuator fabricated using the MetalMUMPS^{TM} process technology (Reprinted with permission, copyright MEMSCap, Inc.)

a silicon device layer to a receiving wafer using an adhesive layer. This process sequence has been used to implement MEMS devices for a wide variety of applications, including RF tunable capacitors, switches, industrial process sensors, inertial sensors, and many more [54–60].

Some of the key highlights of the *a*MEMS^{TM} process include:

- Single-crystal silicon device layer for uniform material properties and low stress levels for the structural layer.
- Silicon device layer is micromachined using DRIE enabling high-dimensional control, repeatability, and uniformity.
- Multiple substrate materials can be used (e.g., silicon; high-resistivity silicon; glass; etc.).
- All low-temperature processing (thermal budget is only 200°C).
- Simple two-mask step process enabling rapid fabrication cycles and prototyping.
- High level of process flexibility to implement wide variety of device types.

The *a*MEMS^{TM} process sequence begins with a 100 mm SOI wafer with a handle wafer thickness of 500 μm, a device layer nominally having a 20 μm thickness, and a buried oxide layer having a thickness of 0.5 μm (Fig. 14.61a) [61]. A thin-film layer of silicon dioxide having a nominal thickness of 1.6 μm is deposited using plasma-enhanced chemical vapor deposition (PECVD) on the top surface of the SOI silicon device layer at a temperature of 200°C (Fig. 14.61b). This PECVD silicon dioxide layer serves as a releasable insulator structural layer to thereby provide electrical isolation as well as mechanical connection between portions of the to-be-defined single-crystal silicon device structural layer. Photolithography is performed (Mask 1) on the top surface to pattern the silicon dioxide layer and the SiO_2 layer is etched using a reactive ion etch. Subsequently, the photoresist is removed from the wafer (Fig. 14.61c).

A second substrate having a nominal thickness of 500 μm is selected according to the intended application (Fig. 14.61d). For example, the second substrate

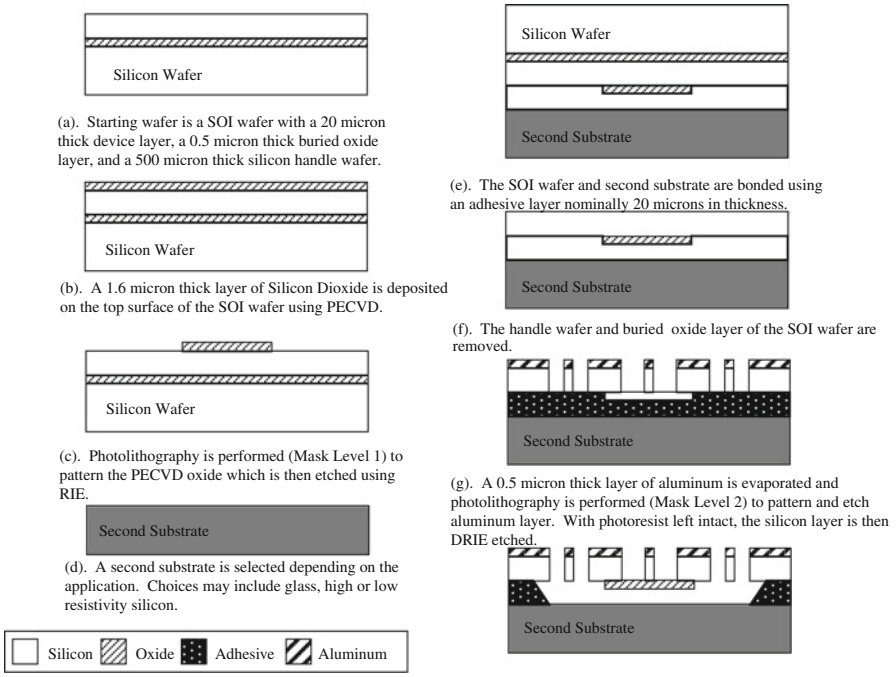


Fig. 14.61 Process sequence for the *a*MEMS^{TM} process

can be either of low- or high-resistivity silicon, Pyrex 7740, or some other choice. This second substrate is then bonded to the device layer of the SOI wafer using an adhesive material (Fig. 14.61e). The adhesive is cured at 190°C and has a cured thickness of approximately 20 μm (±5 μm). The silicon handle wafer of the SOI substrate is removed and subsequently the buried silicon dioxide layer is also removed (Fig. 14.61f).

A layer of aluminum having a nominal thickness of 0.5 μm is deposited on the silicon surface of the composite substrate using evaporation (Fig. 14.61g). This aluminum layer can be used to provide electrical contact to the silicon device layer. A second photolithographic step is performed on the top surface of the substrate followed by a RIE of the aluminum layer. Without removing the photoresist used to mask the aluminum layer, the substrate is etched using DRIE to transfer the pattern into the silicon device layer. The photoresist is then completely removed.

The substrate is then exposed to an oxygen plasma that selectively etches the exposed adhesive layer to release the silicon device. Given the isotropic nature of the oxygen plasma release, there is some undercutting of the silicon at the boundaries of the device (Fig. 14.61h). Lastly, the wafer can be diced and packaged.

Alternatively, the silicon device layer may be released subsequent to dicing. Although this approach requires the fabricator to handle and release individual die, there is some advantage in dicing the substrate before the release of the silicon devices.

The *a*MEMS^{TM} process sequence is applicable to implementing a diversity of different MEMS device types. Figure 14.62 is a SEM image of a tunable capacitor implemented using the *a*MEMS^{TM} process sequence. Tuning is achieved using electrostatic actuation by applying a voltage potential to interdigitated electrodes that are nominally 20 μm in height and have a gap spacing of 2 μm. When a voltage potential is applied to the device, the electrostatic forces move the structure thereby changing the capacitance (by changing the capacitor electrode gap spacing). The silicon capacitor structure is supported by silicon flexures and the stiffness of these flexures can be adjusted over a range according to the design requirements. Figure 14.63 is a SEM of very high-aspect-ratio structures made with the *a*MEMS^{TM} process sequence.

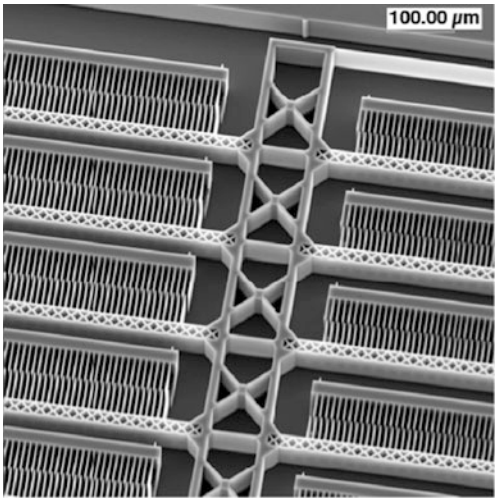


Fig. 14.62 SEM image of tunable capacitor fabricated using the *a*MEMS^{TM} process module (Reprinted with permission, copyright Teledyne Scientific and Imaging Company)

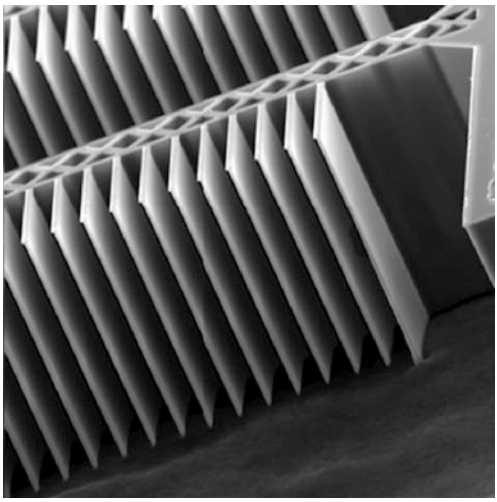


Fig. 14.63 Close-in view SEM image of tunable capacitor fabricated using the *a*MEMS^{TM} process module. The fingers are 80 μm in height and only 2 μm in width (Reprinted with permission, copyright Teledyne Scientific and Imaging Company)

14.8.2.19 Plastic MEMS (University of Michigan)

The plastic/polymer MEMS (PMEMS) process was developed at the University of Michigan [62] and has found application in implementing sensors (including chemical, gas, and biological sensors), capillary electrophoresis devices (including DNA analysis, gene research), and integrated microfluidic networks and systems (including drug analysis, drug synthesis, disease detection, and pharmaceutical research and development).

The PMEMS process utilizes surface micromachining techniques of polymer-based structural and sacrificial layers to implement a diversity of MEMS devices for applications for the microfluidics and bio/nano microsystems. Although the PMEMS process has mostly used Parylene-C as the polymer in fabrication, other polymers can be used depending on the intended application. Among the advantages of using Parylene in the PMEMS process include: parylene film used as a structural layer is highly conformal, pinhole free, and deposited at low temperatures; Parylene has a low outgasing and low permeability to both gases and fluids as compared to other polymers; Parylene is chemically inert; and is considered to be biocompatible. Furthermore, given these properties, specifically the low process temperatures, the PMEMS Parylene process can be relatively easily integrated with microelectronics. The disadvantages of the Parylene PMEMS process are that even though the Parylene has lower permeability than other polymers, it still has a finite permeability. Consequently, if Parylene is left in a strong acid, base, or solvent for any extended period of time, the solution will permeate through the Parylene film and attach to the adhesion layer, thereby resulting in the Parylene peeling from the substrate surface. In addition, devices and systems implemented using the Parylene PMEMS process are restricted to applications of less than 90°C. Temperatures higher than 90°C coupled with the high thermal expansion coefficient of Parylene will result in large thermal stress between the film and the substrate and the film will delaminate from the substrate.

The process is relatively simple, having only three masking steps in the basic process (five masking steps for the more advanced PMEMS process variation), and therefore can be used for very fast production cycle times as well as rapid prototyping. The PMEMS process can be performed on a variety of different substrate types including polycarbonate, silicon, glass, and others. The nominal process allows for channel heights typically ranging from 1 to 50 μm, channel widths up to 200 μm, and channel lengths up to 1.5 cm for sealed channels and 2.7 cm for channels with access holes. The PMEMS process is sufficiently simple and flexible that it can be relatively easily combined with additional processing steps and/or modules to implement other components such as microvalves and micropumps.

The generic PMEMS process utilizing Parylene-C as the channel material and the fabrication being performed on a glass substrate is described (See Figs. 14.64 and 14.65). A glass substrate, having a thickness of approximately 1 mm, is first cleaned using an appropriate cleaning solution such as a piranha etch to remove all organic materials and particulates from the surface (Fig. 14.64a). Subsequently, the substrate is then coated with a 6 μm thick layer of Parylene on both sides to

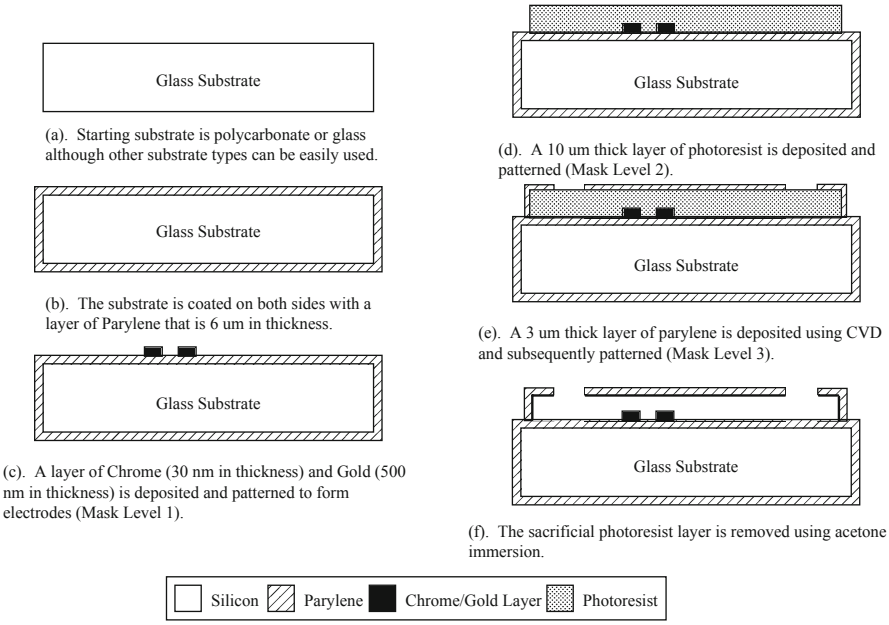


Fig. 14.64 Basic PMEMS process sequence

prevent substrate damage during fabrication (Fig. 14.64b). A layer of chrome having a thickness of 30 nm, followed by a layer of gold having a thickness of 500 nm is deposited on the top surface of the substrate using evaporation. This metal layer typically is used to make electrodes and microheaters in the devices. Photolithography is then performed (mask level 1) on the chrome and gold metal layers on the top surface to define these metal layers into the desired pattern (mask level 1) as shown in Fig. 14.64c.

A layer of photoresist having a thickness of 10 μm is then deposited on the top surface of the substrate using spin deposition (Fig. 14.64d). This layer acts as the sacrificial layer for making the channels and its thickness can be adjusted so as to vary the channel height. Photolithography is then performed to pattern the photoresist layer (mask level 2). A 3 μm thick Parylene layer is deposited onto the substrate at room temperature using chemical vapor deposition (CVD). Parylene deposition is extremely conformal over the topology of the sacrificial photoresist layer and is used to form the channel walls. Subsequently, a 10 μm thick layer of photoresist is spun deposited and patterned (mask level 3) to make openings in the top Parylene film layer. These openings are used to release the channels by removing the photoresist sacrificial layer. These release openings have a maximum spacing of 1.5 mm according to the release time of the standard process. After the masking photoresist is defined, the Parylene is etched using an oxygen plasma etch (Fig. 14.64e). The substrate is then immersed in acetone for approximately 8 h, followed by two additional acetone and isopropanol alcohol rinses to completely remove the photoresist sacrificial material from inside the channels (Fig. 14.64f).

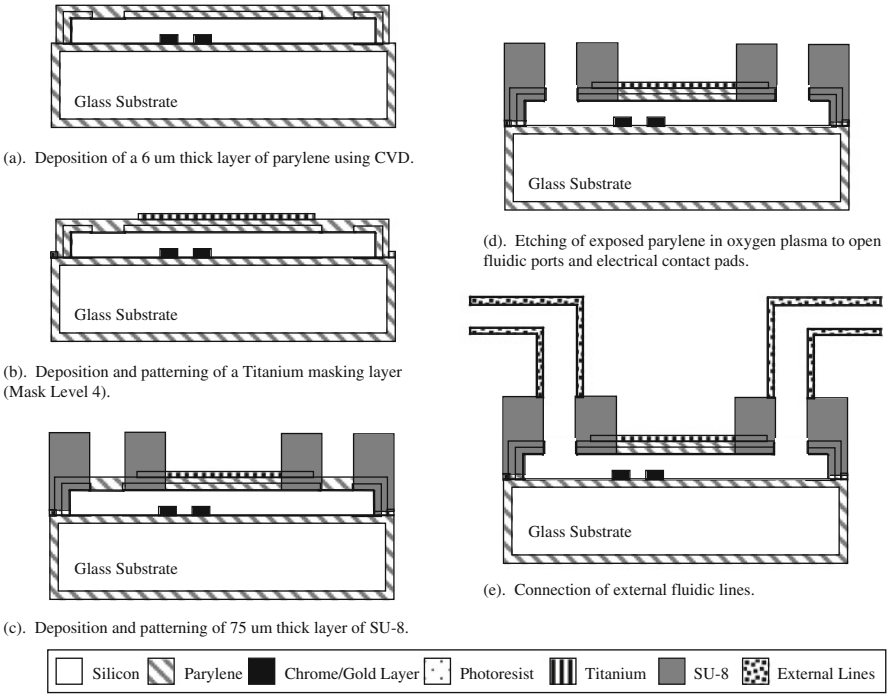


Fig. 14.65 Additional process steps for PMEMS process in order to make fluidic connections

For many applications it is desirable to apply pressure to the fluids inside the channels and the ability to do this requires additional processing to seal the release openings. Therefore, for this purpose a 6 μm thick layer of Parylene is deposited at room temperature using CVD (Fig. 14.65a). Next, a 0.5 μm thick layer of titanium is deposited using evaporation onto the top surface of the substrate and patterned using photolithography and wet etching (mask level 4; Fig. 14.65b). The titanium layer masks most of the substrate surface and is only exposed in the areas designated for fluid interconnects and electrical contacts. Subsequently, a 75 μm thick layer of SU-8 is spun deposited onto the top substrate surface. Photolithography is then performed on the SU-8 layer (mask level 5) to pattern the SU-8 layer (Fig. 14.65c). The substrate is then placed into a reactive ion etcher and using an oxygen plasma, the Parylene material exposed under the SU-8 and titanium layers is removed by etching (Fig. 14.65d). The titanium layer exposed on the substrate surface is then removed using a wet chemical immersion. Lastly, external fluidic connections are made to the SU-8 layer by pressing appropriate-sized fluidic tubing to the SU-8 device connections (Fig. 14.65e).

14.8.2.20 Wafer-Level Packaging (ISSYS)

The wafer-level packaging module developed by Integrated Sensing Systems (ISSYS) is one approach used to simplify, standardize, and lower the cost of

MEMS packaging (Fig. 14.66) [63]. The basic idea is to use MEMS processing technologies, including micromachining and wafer bonding, to build an effective ambient-controlled encapsulation around the MEMS device using batch-fabrication techniques. The features of the wafer-level packaging include: it simplifies the rest of the assembly and packaging, improves yield throughout the remainder of the production process, allows utilization of standard assembly, packaging and test equipment, and allows a sustainable vacuum-sealing of the MEMS to levels below 1 mtorr. This last feature is particularly important for MEMS devices such as inertial and resonator devices, which require high-vacuum levels that are able to be maintained for long periods of time [64].

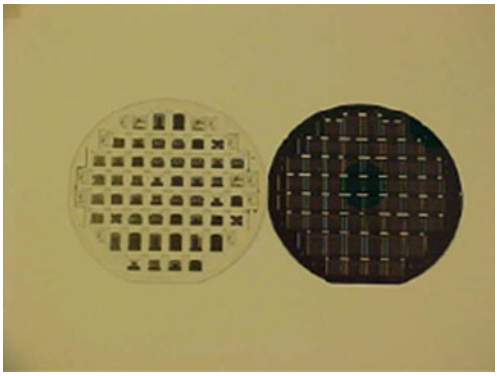


Fig. 14.66 MEMS device wafer (*left*) prior to bonding and capping wafer (*right*) (Courtesy of ISSYS Inc.)

The high-vacuum, wafer-level packaging technology is defined as a process module due to the fact that this sequence of processing steps is really only useful when combined with the fabrication of MEMS devices [65]. The process module can be used with a variety of MEMS process technologies including: surface micromachining, bulk micromachining, silicon-on-glass, LIGA, and others. The process module begins with either the choice of a silicon or Pyrex 7740 capping wafer having the same diameter as the substrate in which the MEMS devices are fabricated. This capping wafer will be used to bond and encapsulate the MEMS device wafer.

Micromachining is performed on the silicon or glass capping wafer to create a recess or cavity in the substrate (Fig. 14.67). The technique used to make the recess varies depending on the type of substrate material as well as the depth of the recess to be made, but as an example, DRIE anisotropic etching would be an appropriate method for creating the recess in a silicon capping wafer (Fig. 14.67b). Through-wafer vias are then etched through the silicon or glass capping wafer, which will allow electrical connection to the MEMS devices once they are encapsulated in the wafer-level package (Fig. 14.67b). Next, a sealing material, such as glass frit or solder, is deposited and patterned on the capping wafer (Fig. 14.67c). A proprietary NanoGetter^{TM} material is then applied and patterned such that it is located in the recesses made in the capping wafer (Fig. 14.67d). The capping wafer is then bonded to the MEMS device wafer using a vacuum ambient during the bonding procedure

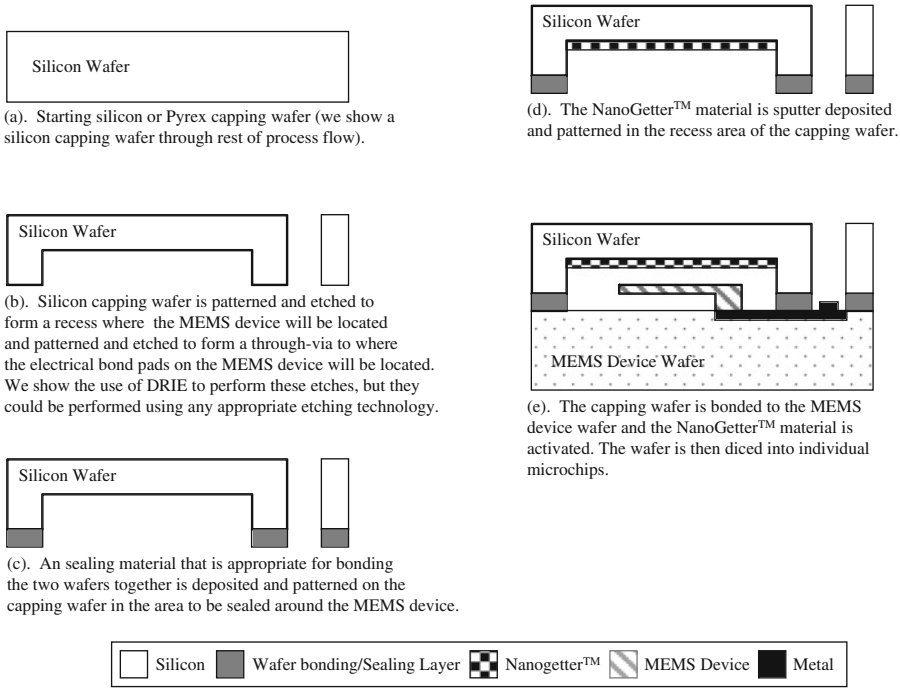


Fig. 14.67 Process flow for ISSYS wafer-level packaging process sequence

(Fig. 14.67e). The optimum bonding temperature varies depending on the sealing materials used, with higher temperatures (up to 425°C) usually necessary for glass frit bonding processes and lower temperatures for solder bonding processes. After the MEMS device wafer is bonded to the capping wafer and the gettering material has been activated, the composite bonded wafer pair is diced into individual die, which can then be attached and wirebonded or flip-chip bonded to connect to the intended system.

The material used for bonding the substrate together will play a large part in determining what kinds of devices can be packaged using this approach. Obviously, a solder material would be more suitable for the packaging of integrated MEMS devices because they are more susceptible to degradation upon exposure to higher temperatures.

14.8.3 Review of Integrated CMOS MEMS Process Technologies

14.8.3.1 iMEMS – Analog Devices

The Analog Devices, Inc. iMEMS process is the evolution of an integrated MEMS/circuit process that began its development in the late 1980s as a skunk-works project at Analog Devices, Inc (ADI) [66, 67]. The process was developed to

implement an interdigitated finger-based, variable capacitance accelerometer. The MEMS unit process steps were developed within a standard single-metal 3 μm BiCMOS process that had been running at ADI for many years. The MEMS structure portion of the process was a relatively straightforward 2 μm thick polysilicon, surface-micromachining process. The accelerometer application called for both thick polysilicon and narrow finger-to-finger gaps, in other words, a large aspect ratio for the main structural polysilicon etch. In the technology of the time, an aspect ratio of 1–2 was considered state of the art. The sensor design, with its large number of positive and negative polarity fixed fingers also required careful design of vias and electrical interconnect. Because the single metal could only be deposited at the end of the process for thermal reasons, the sensor interconnect was done with polysilicon layers and substrate diffusions.

Much of the complexity of the process was driven by the requirements for spatial segregation between the MEMS sensor and the circuitry and by the mechanism used to support the MEMS structure during release and subsequent process steps. The BiCMOS circuit process was fundamentally an analog process, and the bipolar transistors were the workhorses of the circuit designs. In recent years, the process has undergone two major revisions to increase the thickness of the structural poly-silicon to 4 μm and to include a self-assembled monolayer (SAM) coating for stiction reduction.

Process Flow Overview

The basic construction of the ADI iMEMS process is:

1. Build the circuit devices.
2. Build the MEMS sensor.
3. Wire the sensor and the circuit.
4. Release the sensor.

Build the Circuits

The BiCMOS process supports NPN and PNP bipolar transistors and PMOS and NMOS FETs. The process starts with a P+ substrate with a P epitaxial layer. N wells are defined and implanted to construct PMOS and NPN bipolar transistors. The transistor process is typical, including a thick oxide growth to separate the transistors. This thick oxide is also used to define the boundary between the MEMS sensor area and the circuit area. The first joint process step is an N+ diffusion that forms the N+ emitter of the NPN transistors and also a conductive interconnect between the sensor and the circuit areas. The transistor gate oxide is also used in the sensor area to isolate the N+ diffusion.

Build the Sensor

The sensor construction begins by stripping off the circuit passivation from the sensor area. A polysilicon ground-plane layer is deposited followed by a 2 μm

sacrificial oxide. The thickness of this sacrificial oxide is a critical design parameter, so considerable care must be taken to understand its deposition, densification, and etch characteristics. As with other polysilicon surface micromachining processes, a bump etch is employed to reduce the contact area between the released structure and the ground plane. Etches must also be made through the sacrificial oxide to allow contact to the ground plane and the N+ interconnect. Four microns of polysilicon are deposited to form the released structure (including its anchors). This material is heavily doped to produce a material that is a good conductor. Deposition and anneal conditions must be carefully designed to control stress and curvature in the released film. A dry RIE etch is used to pattern this film.

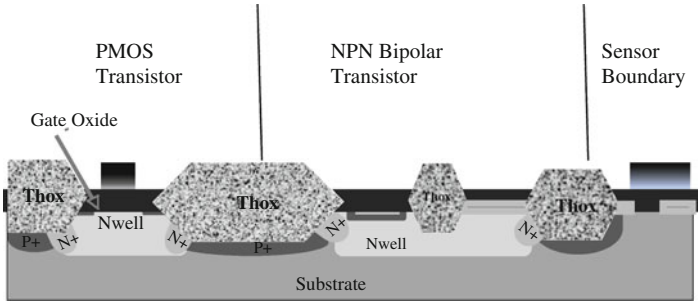


Fig. 14.68 The BiCMOS circuit area (Reprinted with permission, copyright Analog Devices Inc.)

Connect the Sensor and the Circuit

This part of the process starts by stripping the sensor sacrificial oxide from the circuit area. An etch is performed to open N+ diffusion contact areas at the periphery of the sensor area. Platinum is deposited and sintered to form platinum silicide in these contact areas. TiW is deposited as a barrier metal and then aluminum is deposited and patterned as in a typical circuit interconnect process.

Release the Sensor

The ADI iMEMS process uses a unique method of depositing and patterning photoresist, which will remain during the sacrificial oxide release etch. The key is that small, strategically placed areas of the sacrificial oxide are initially etched. These "holes" are then filled with photoresist, making a solid material between the sensor polysilicon and the ground plane. These photoresist supports remain in place and the sacrificial oxide is removed by a wet HF etch and subsequent drying to keep the sensor polysilicon layer from collapsing due to the very large surface tension forces associated with the drying process. After the release etch, the process is completed by depositing a self-assembled monolayer (SAM) coating to reduce stiction forces.

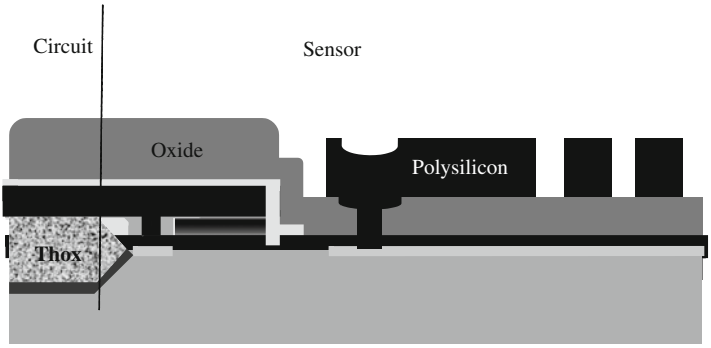


Fig. 14.69 Cross-section showing the patterned sensor. Note the via on the sensor that connects it to the interconnect layer below (Reprinted with permission, copyright Analog Devices Inc.)

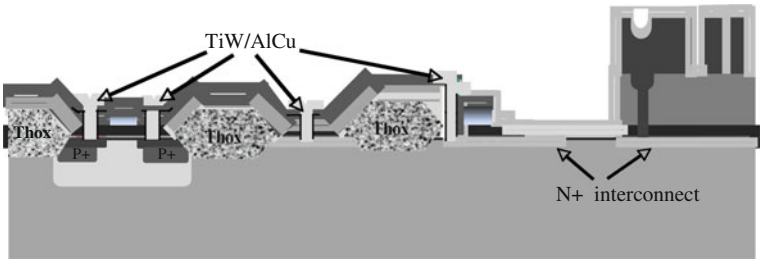


Fig. 14.70 Cross-section showing the circuit interconnect. Note that the N+ diffusion forms an interconnect layer between the circuit and the sensor (Reprinted with permission, copyright Analog Devices Inc.)

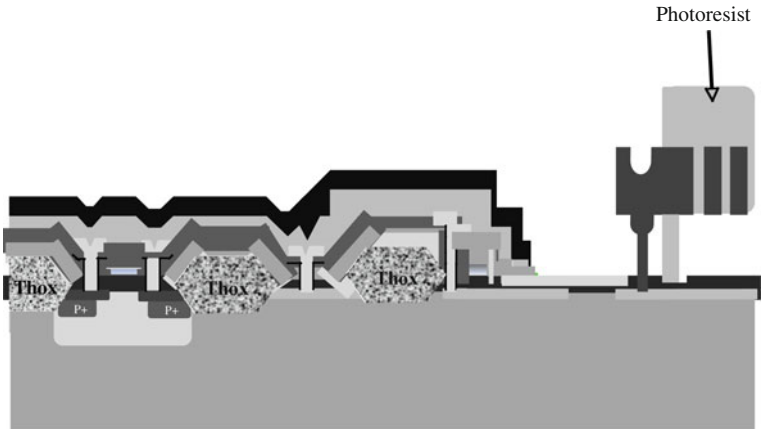


Fig. 14.71 Cross-section showing the final structure. The photoresist shown is removed to completely release the actuator structure (Reprinted with permission, copyright Analog Devices Inc.)

14.8.3.2 DLP (Texas Instruments)

Digital Light Processing technology developed by Texas Instruments Corporation is one of the most successful MEMS development endeavors to date with market sales of chip sets of nearly $1 B annually and is used in various large volume commercial markets such as projection televisions and projection display systems [68, 69]. DLP technology is a disruptive technology for movie theaters because it replaces the 100-year old celluloid film with a completely digital format. Already, DLP is currently used in more than 14,000 theaters, with over 7000 more advanced 3-D systems deployed in theaters. The key component of DLP® technology is the micromirror array chip (called the Digital Micromirror Device, or DMD for short [70]). Essentially the DMD chip is a large array of individually and digitally controlled MEMS micromirrors; there are up to 2 M mirrors in each chip array! Each mirror in the array measures just over 10 μm by 10 μm and is electrostatically actuated by the microelectronics physically located underneath the mirror array [71]. This enables the fill factor of the DMD to reach levels of over 90%, thereby allowing very high optical efficiency and contrast. Integrated microelectronics is a necessity in DLP technology inasmuch as the number, density, and size of the mirrors combined with individual addressability would preclude having all the electronics off-chip. The DMD fabrication is made using a "MEMS last" integrated process technology wherein the microelectronics are fabricated in the base substrate first and then the MEMS mirrors are fabricated on the surface of the microelectronics substrate [72].

Figure 14.72 is a SEM of a portion of the DMD device and Fig. 14.73 is a closer-view SEM of the DMD micromirror array showing the center pixel in the actuated state and the surrounding pixels in the unactuated state. As can be seen, the mirror rotates by approximately 12° in the actuated state and without actuation the mirrors (shown around the center pixel) are nominally flat. For a description of how DMDs are used in projection optical systems, see [70, 72]. The mirrors have a complex hinge mechanism to allow them to rotate by a sufficient angular displacement while keeping the strain in the hinges to an acceptable level. High levels of reliability are required for consumer electronics applications, which have been achieved by having exceptional control to reduce the hinge memory and stiction effects in the DMD. Remarkably, individual mirrors have been operated over 10^{12} full mechanical movements without failure and thereby have demonstrated an extremely high level of reliability [68]. Figure 14.74 is a cross-section illustration of the DMD showing the electromechanical elements underlying a DMD mirror which enable it to actuate and Fig. 14.75 is a SEM of a pixel with the mirror removed to exhibit the underlying structure.

The DMD pixel consists of a SRAM cell fabricated in the silicon substrate with a MEMS superstructure implemented on top. The MEMS-last process sequence requires that all post-CMOS processing steps used to fabricate the MEMS superstructure be compatible, both thermally and chemically, with the CMOS. Consequently, the thermal budget for these processing steps is quite restricted and no processing temperatures can exceed 400°C. This is achieved in the DMD

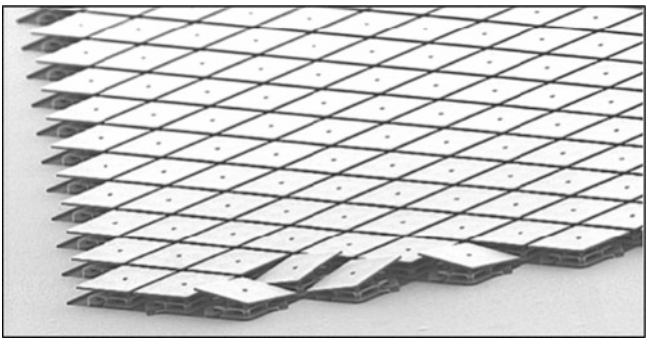


Fig. 14.72 SEM image of DMD chip shown with the pixels near the leading edge of the array in the actuated (i.e., nonflat) state (Reprinted with permission, copyright Texas Instruments, Inc.)

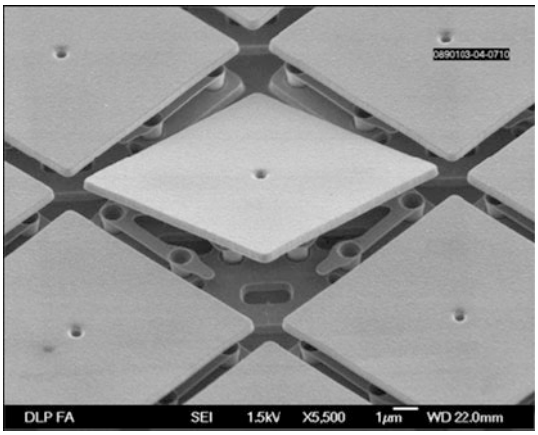


Fig. 14.73 Magnified SEM image of Texas Instrument's DMD device with center pixel in actuated (i.e., rotated) state (Reprinted with permission, copyright Texas Instruments, Inc.)

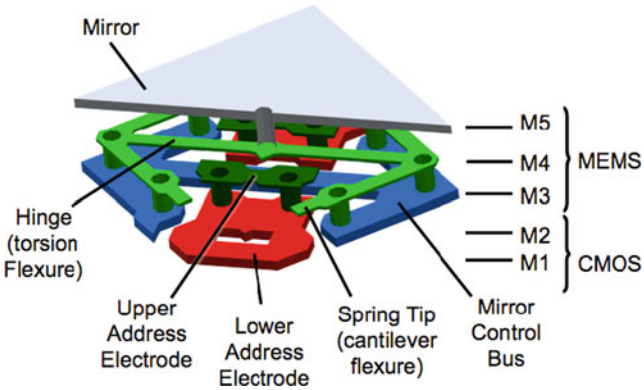


Fig. 14.74 DMD pixel showing the electromechanical components under the mirror that enables the device to actuate (Reprinted with permission, copyright Texas Instruments, Inc.)

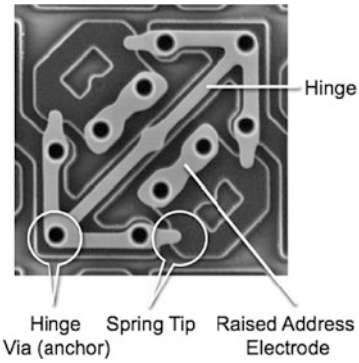


Fig. 14.75 SEM image of a DMD pixel with the top aluminum mirror layer removed to expose the underlying aluminum layers forming the hinge and electrode elements (Reprinted with permission, copyright Texas Instruments, Inc.)

process sequence by fabricating the MEMS superstructure utilizing a series of relatively low temperature deposition and etch processes. Consequently, the DMD is made using a low-temperature, surface micromachining, MEMS-last, monolithic, integrated MEMS process technology.

The DMD process sequence begins (see Fig. 14.76) with a relatively conventional 0.8 μm linewidth CMOS process technology having a two-layer metallization (M1 and M2) [72]. After the CMOS is completed, a relatively thick oxide layer is

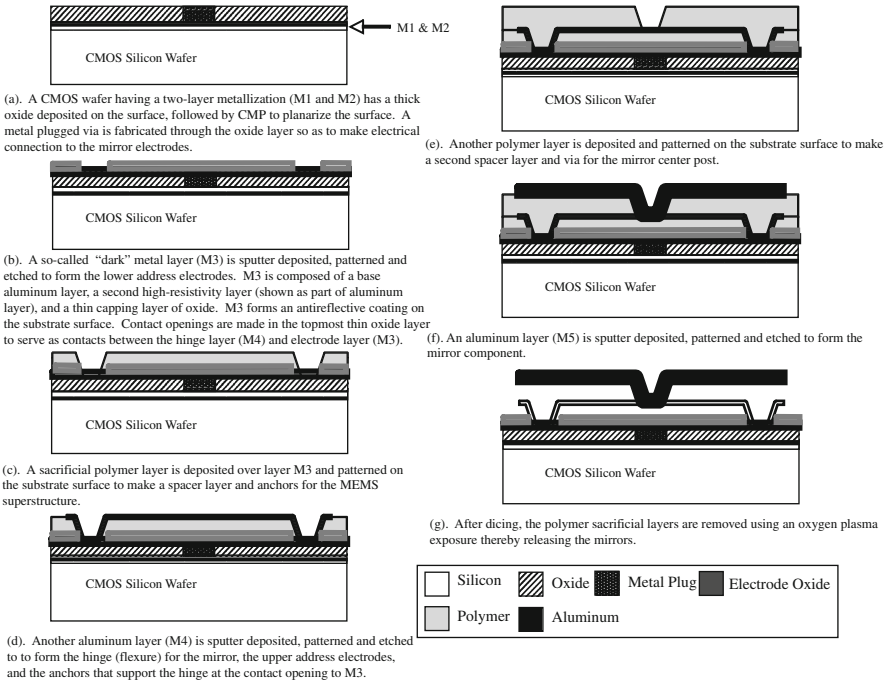


Fig. 14.76 Texas Instruments' DMD process technology

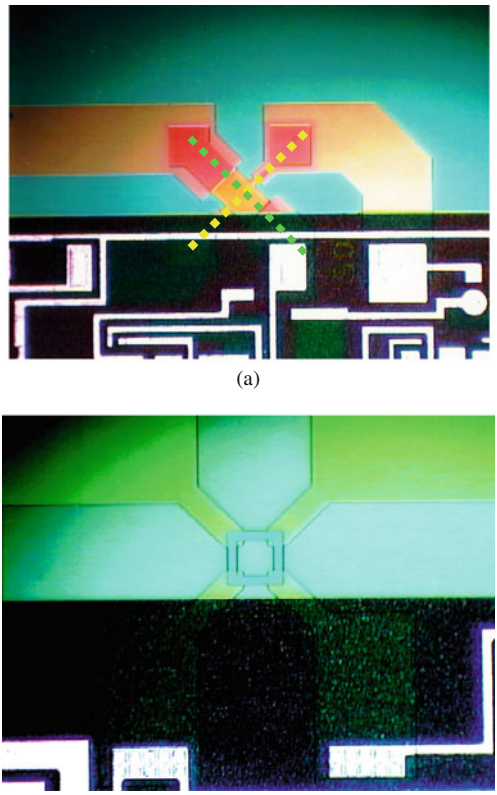
deposited on the wafers and subsequently planarized using chemical-mechanical polishing. The planarization of the surface of the CMOS wafer is very important to ensure that the wafer surface is completely flat prior to beginning the MEMS fabrication in order not to degrade the brightness uniformity or contrast ratio of the DMDs. The CMP oxide layer is patterned, etched, and filled with metal to form plugged vias to electrically connect the CMOS electronics to the actual mirror bus lines (Fig. 14.76a).

Next, a so-called "dark" metal layer (M3) is deposited, patterned, and etched to form the lower address electrodes (Fig. 14.76b). M3 is actually a stack composed of a base aluminum layer, a second high-resistivity film, and a capping layer of thin oxide. Together these three layers form an antireflective coating to reduce stray light reflections from the substrate. Contact openings are then patterned and etched in the thin cap oxide layer to serve as electrical contacts between the hinge layer (M4) and electrode layer M3. Next, a planarizing, sacrificial polymer layer is deposited over the M3 and subsequently patterned (Fig. 14.76c).

Another aluminum metal layer (M4) is then sputter deposited, patterned, and RIE etched to form the hinge (flexure) for the mirror, the upper address electrodes, and the anchors that support the hinge at the contact openings to M3 (Fig. 14.76d). After the hinge metal layer (M4) has been defined, another thick, planarizing sacrificial layer of polymer is deposited on the wafer surface (Fig. 14.76e). Subsequently, another aluminum metal layer (M5) is sputter deposited onto the patterned polymer sacrificial layer, followed by the patterning and etching of the aluminum layer to define the DMD mirrors. After the top metal aluminum layer has been etched using RIE (Fig. 14.76f), a layer of photoresist is deposited to protect the mirror surfaces during dicing (not shown). Lastly, the DMD mirrors are released by placing the substrates in an oxygen plasma etcher, which removes the sacrificial polymer layers, as well as the protective photoresist top coat, thereby leaving the functional MEMS mirrors (Fig. 14.76g) and completing the DMD fabrication.

14.8.3.3 Integrated MEMS Pressure Sensor (Freescale)

The Integrated Pressure Sensor (IPS) process technology was originally developed and put into production by Motorola (now Freescale Semiconductor) in 1991 and represents one of the most successful and long-standing high-volume MEMS products in the commercial market. The device is mostly used in automotive applications, but is also employed in medical devices and industrial control applications. This sensor employs the piezoresistive effect to measure the deflection of a thin silicon membrane and combines bipolar microelectronics for signal conditioning and calibration on the same silicon substrate as the sensor device, thereby making it a fully integrated MEMS product (actually the first fully integrated high-volume MEMS product since it went into production in 1991). The transduction approach taken to measure membrane deflection under pressure loading is somewhat unusual inasmuch as it uses a single piezoresistor element to measure strain as opposed to the conventional approach of using multiple, distributed piezoresistors (e.g., Wheatstone bridge). Freescale has used two types of piezoresistive transducers, the



(a)

(b)

Fig. 14.77 (**a**) Optical photograph of top surface of Freescale pressure sensor that employs the original X-ducer. An "X" has been added to show the transducer layout. (**b**) The newer "picture frame" piezoresistor configuration (Reprinted with permission, copyright Freescale Semiconductor Inc.)

X-ducer™ and the Picture Frame. The original "X-ducer" design resembles an "X" located at the edge of the pressure deflecting membrane (Fig. 14.77a). The X-ducer design had the benefit of reducing the offset distribution that is an undesirable attribute of some Wheatstone bridges.

The process technology has been improved over the years, tracking recent developments in micromachining and design, and Freescale now uses what is called a "picture frame" piezoresistor configuration that allows approximately 40% greater output signal than the X-ducer design (Fig. 14.77b). Other process improvements include using an electrochemical etch stop to precisely control the pressure-sensing membrane thickness and reduction of the area consumed by the sensor [73]. We review the most recent process flow for this device.

The process begins with a single crystal p-type silicon substrate (Fig. 14.78) [74]. A diffusion to create an n+ region is performed and this will be used to form the buried layer for the bipolar transistor devices. A 15 μm thick layer of n-type silicon is epitaxially grown on the surface of the wafer and this is followed by a deep diffusion to create p+ regions to electrically isolate the bipolar transistors (Fig. 14.78a, b). Subsequently, a diffusion is performed to create a p+ region that

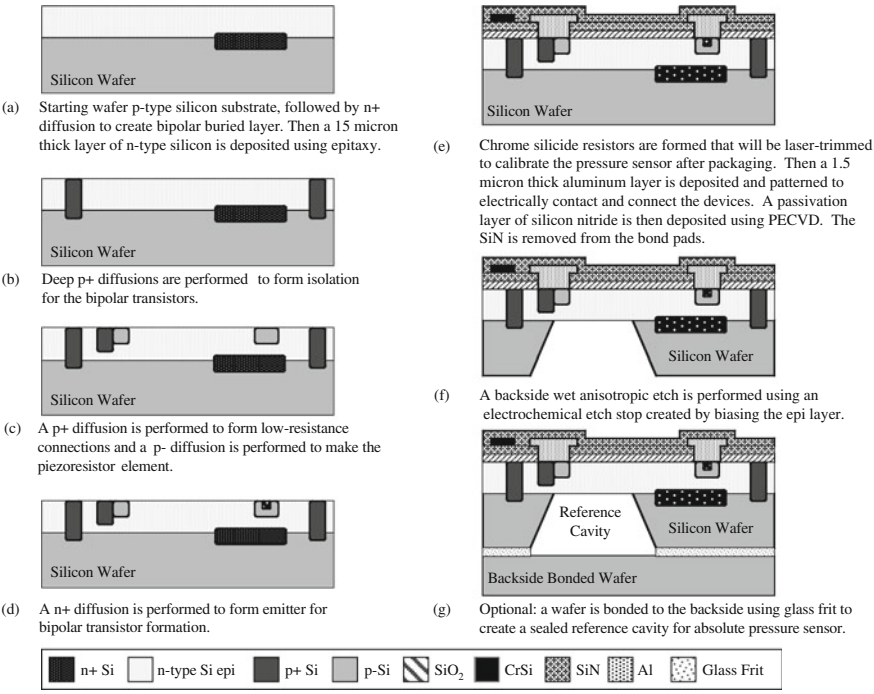


Fig. 14.78 Process technology for Freescale Manifold Air Pressure (MAP) sensor

will be used to make low-resistance connections. This is followed by performing another diffusion to form p- regions that will be used to make the piezoresistors of the sensor device (Fig. 14.78c). Yet another diffusion is performed to create an n+ region to make the bipolar transistor emitter and to provide ohmic contact to the n-type epi (Fig. 14.78d).

A layer of chrome–silicide (CrSi) is deposited and patterned and etched to form resistors. These CrSi resistors on the top surface of the substrate are laser trimmed after packaging to calibrate the sensor offset and adjust the sensor span. A 1.5 μm thick layer of aluminum is deposited, patterned, and etched to make electrical contact and connection to the transistors and sensor elements of the device. A layer of PECVD silicon nitride is then deposited to passivate and protect the top surface of the substrate. The SiN is removed only from the electrical pads by a photolithography and etch process (Fig. 14.78e). Then, the wafer is immersed into a wet anisotropic etch solution and electrical contact is made to the n-type silicon layer that was epitaxially grown to allow an electrochemical etch stop. As the etchant solution reaches the junction between the p-type silicon substrate and the n-type silicon epi layer the etching process terminates thereby allowing for precise control of the sensor membrane thickness (Fig. 14.78f). As an optional step, a silicon wafer may be bonded to the backside of the sensor wafer to create sealed pressure reference cavities for each sensor device (Fig. 14.78g). This would be used

for implementing an absolute pressure sensor. Wafer bonding is performed using a glass frit layer between the two substrates.

From a process integration standpoint, the Freescale pressure sensor example has several very interesting attributes. First, this technology is highly unusual because it integrates a bipolar transistor microelectronics process technology with a MEMS bulk micromachining process technology. The bipolar transistors form amplifiers that convert the millivolt-level transducer output into a volt-level device output. Nearly all other MEMS integrated process technologies that have been demonstrated merge CMOS with MEMS devices.

Second, control over the mechanical dimensions of MEMS devices made using bulk micromachining are typically not very precise; however, the Freescale technology employs an electrochemical etch stop that enables precise control of the membrane thickness which is extremely important for determining the mechanical stiffness of the pressure sensor membrane (i.e., the amount of membrane deflection to result from a certain level of pressure loading). This etch stop layer is an epitaxially grown n-type layer that is reverse-biased during the etching and when the etchant solution reaches this layer, the etch terminates. This same epitaxial layer in the process sequence is also used in the fabrication of the bipolar transistors.

Third, the microelectronics is fabricated first and then the MEMS are subsequently made. This is possible inasmuch as all of the MEMS processing steps subsequent to the microelectronics fabrication are performed at relatively low processing temperatures. Fourth, the process uses 100-oriented silicon wafers to enable the micromachining steps to be done. Normally, 111-oriented wafers are used for the fabrication of bipolar transistor devices and therefore Freescale needed to develop a special bipolar transistor process for this substrate orientation. Fifth, the device wafer can be bonded to another wafer to form a sealed reference cavity for implementing an absolute pressure transducer, or it can be left "as is" to implement a differential pressure transducer without any major changes to the process sequence. Lastly, the chrome silicide resistors enable the circuits and sensors to be easily trimmed for calibration, thereby allowing any offsets to be inexpensively eliminated.

The major disadvantages of this process are that it employs wet anisotropic bulk micromachining to implement the pressure sensor and therefore a large amount of die area is consumed by the sidewalls of the exposed crystallographic planes in the silicon substrate. This is costly compared to the area that would be used to implement a surface micromachined sensor having the same membrane dimensions. Also, the wet etch process must expose only the back of the wafer to etchant; this requires specialized etch fixturing. Lastly, bipolar transistors consume large amounts of power compared to CMOS electronics and therefore the Freescale integrated MEMS pressure sensor has higher power consumption levels than some other technologies. The bipolar circuitry cannot be used to form complex digital circuits, so this flow is limited to analog devices.

14.8.3.4 Thermal Inkjet Printhead (Xerox)

Thermal inkjet (TIJ) technology has emerged as the choice for low-cost desktop printing since the PC era in 1980s [75–77]. Typical TIJ printheads are used as

drop-on-demand printheads; that is, the ink is ejected from the nozzle only when there is a demand for an image on the paper. The printhead is operated by applying a short pulse (several microseconds) to the heater plates inside the nozzles. The ink in contact with the heater surface rapidly heats up and a vapor bubble is generated. This creates a great volume expansion (about 50 times) of the heated liquid and a pressure of about 100 atmospheres that is sufficient to eject the ink from the nozzles at a high velocity 5–10 m/s. By about 30 μs after the initial voltage pulse, the drops break off at the nozzles and the bubbles collapse back onto the heater. The ink then refills the channels from the ink reservoir through capillarity and the meniscus at the nozzle settles to the original state before the next drop is ejected. The refilling process typically takes on the order of 100 μs and is determined by the fluid dynamics and channel geometry. TIJ is also called bubble jet because it uses the bubble to force out the ink.

Canon, HP, and Xerox are three of the first companies that integrated MEMS with IC to manufacture the TIJ printheads. Attributed to the disposable ink cartridge packaging, it is by far the largest volume of MEMS chips ever produced. MEMS structures are created as the ink channels, reservoir, and nozzles, whereas the IC is the control of the demand of power to generate the thermal bubble. In addition to other examples of integrated MEMS described elsewhere in this chapter, TIJ printheads have many unique integration issues. First, ink fluid is relatively corrosive to many metals used in IC production. Second, the heat from the heater needs to be isolated from the temperature-sensitive microelectronics. A metal heat sink is commonly used in contact with the heater substrate. Third, the packaging of the integrated MEMS inkjet chips needs to be compatible with the ink chemistry. Fourth, the ink nozzle requires hydrophobic treatments to keep the nozzle clean from ink accumulation. The hydrophobic treatment can be done by solution or vapor phase coating on the nozzle surface. It is desired to keep this coating only on the outer surface of the nozzle and to keep hydrophilic surfaces inside the nozzle and ink channel. Lastly, the nozzle area needs to be flat after packaging and accessible by the printing media within the distance of a few hundred micrometers. The examples below describe the fabrication processes of the chamber wafer, heater wafer, and the bonding of these two wafers.

There are a couple of major designs for TIJ printheads [75]. One is called an edgeshooter where the droplets are propelled along trajectories that are parallel to the heating element surfaces. A typical edgeshooter design is shown in Fig. 14.79, which consists of a silicon channel wafer bonded to a heater wafer with a polyimide spacer layer [78]. The heater wafer is the silicon substrate with the array of hearing elements, logic circuits, and addressing electrodes. On the top surface of the heater wafer, a patterned thick polymeric layer such as polyimide is used to form the ink flow paths. A linear array of parallel grooves is formed on the channel wafer. One end of the grooves connects with the ink inlet manifold and the other end is open to form ink nozzles. A typical inkjet die is less than 1 in. in length and contains several hundreds nozzles. A 600 nozzles-per-inch printhead would have a pitch of about 42 μm which includes the nozzle width and the thickness of the wall between nozzles.

The other design is called a roofshooter where the ink is ejected in the direction perpendicular to the heater surface. The roofshooter design can be done similarly

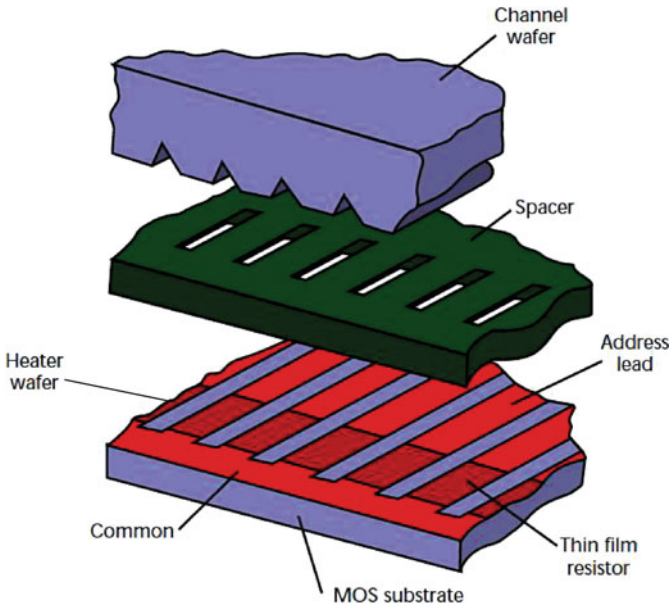


Fig. 14.79 Thermal inkjet printheads made of three components: channel wafer, spacer layer, and heater wafer [78] (Reprinted with permission, copyright 1997 IEEE)

with the nozzles open on the surface of the silicon channel wafer, rather than on the edge of the wafer. Another popular roofshooter design is to replace the silicon channel wafer with a flexible polyimide nozzle substrate and to have ink channels and fill holes anisotropically etched through the silicon heater wafer. The following section focuses on the design and fabrication of the edgeshooter printhead.

Heater Wafer

The heater wafer is produced from typical IC processes [79, 80]. It contains a linear array of heaters and MOS circuits that control ink ejection. Unlike the prediction of Moore's law, the IC for TIJ printhead is not state of the art compared to the current 45 nm technology. This is partly due to the low switching speed and high current/power requirements. To save cost, typical manufacturing foundries used for inkjet are those with excess capacity in the small wafer sizes such as 6 or 8 in. foundries. It is also common practice to reduce the packaging cost by integrating addressing and multiplexing logic on the heater wafer to minimize the number of external connections [81].

Although the heater wafer can be fabricated using most IC processes, several special fabrication steps are required [81]. One possible material choice for the heater is the polysilicon. Without protection, polysilicon lifetime is very limited due to the high pressure of the collapsing bubble (i.e., cavitations) and the corrosive property of the ink. A tantalum layer is deposited over the polysilicon heater for protection.

An insulating silicon nitride layer is usually placed between the polysilicon and tantalum to prevent a potential being applied to the tantalum surface in contact with the ink, which would cause electrolysis of the ink. The silicon nitride should be as thin as possible, consistent with absence of pinholes (about 50–150 nm). In addition, to achieve thermal efficiency, a thicker than usual field oxide is deposited to reduce the thermal losses to the silicon substrate. All MOS circuits are covered by polyimide to prevent exposure to the corrosive ink.

Channel Wafer

The channel wafer is mainly the mechanical and fluidic structures of the ink channel, reservoir, and nozzles and contains no integrated circuits. As shown in Fig. 14.79, the nozzle has a triangular shape created by anisotropic etching in KOH solution on the single crystalline silicon. As shown in Fig. 14.80, the nozzle can also have a rectangular shape created by ICP RIE etching. The advantages of anisotropic etching are the low cost and ease of the etch depth control. A rectangular shape offers more nozzle numbers per area and higher print resolution, but controlling the variation in etch depth is a challenge.

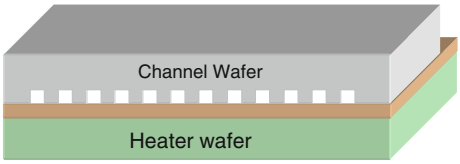


Fig. 14.80 Nozzle with rectangle shape for TIJ printheads [82] (Reprinted with permission, copyright 2004, IEEE)

It is often very desirable to have multiple etch depths in the channel wafer to control the ink ejection and refill process. With multiple masks, one can achieve different etch depths on the same wafer. It would be very difficult to handle wafers and perform precision lithography after deep etching, therefore it is recommended to pattern all the masking layers before the first KOH etching. Figure 14.81 shows the process of a two-mask channel wafer [76]. Silicon oxide serves as the ink channel mask and the silicon nitride layer serves as the masking layer for the ink inlet. The first step is to deposit silicon oxide and polysilicon as the masking layers for ink channels. The polysilicon layer provides scratch protection during wafer handling.

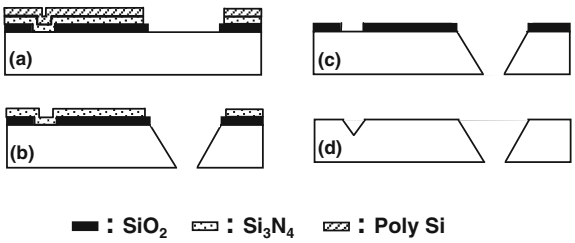


Fig. 14.81 Process of making channel wafers with triangle-shaped nozzle

After patterning the first mask on both polysilicon and silicon oxide, polysilicon is stripped and the second masking layer (silicon nitride and polysilicon) is deposited (Fig. 14.81a). After patterning the second masks on polysilicon and silicon nitride, wet etching in KOH is carried out (Fig. 14.81b). Polysilicon is etched away during the KOH etching and silicon nitride is removed using H_3PO_4 solution after etching (Fig. 14.81c). The silicon oxide is removed after forming the ink channels by the second KOH etching (Fig. 14.81d).

Figure 14.82 shows a more complicated design in channel wafers containing an ink inlet and ink chamber (by KOH etching) and ink nozzle (by dry RIE etching) [82]. Figure 14.82a shows that four masks are used to pattern the masking layers for two KOH etching (silicon nitride), one protection layer (polysilicon) and one RIE etching (silicon oxide). The first KOH etching forms the ink inlet and the silicon nitride is removed using a H_3PO_4 solution after etching (Fig. 14.82b). Polysilicon is patterned between two silicon nitride layers to protect the lower silicon nitride from the first KOH etching. The second KOH etching is a shorter duration than the first one to form the ink channels between the ink inlet and the ink nozzles. After KOH etching, the silicon nitride is also removed using H_3PO_4 solution (Fig. 14.82c). Silicon oxide is used as the masking material for the nozzles and is removed using an HF solution (Fig. 14.82d). The channel wafer is then ready to bond to the heater wafer (Fig. 14.82e).

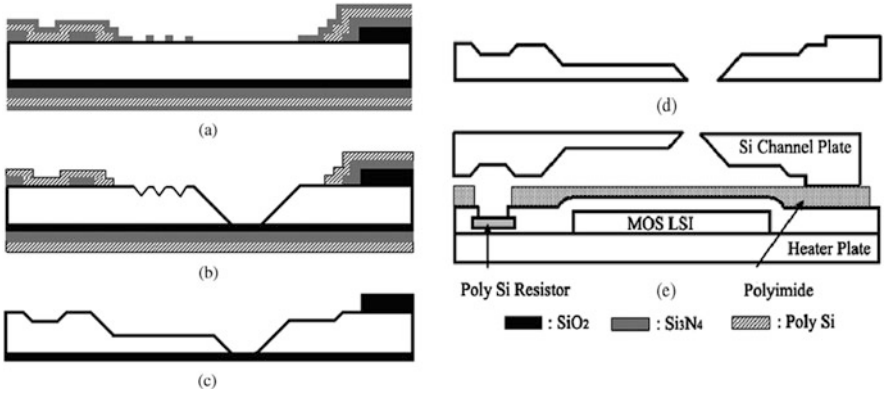


Fig. 14.82 Fabrication process of channel wafers with rectangle-shaped nozzle [82] (Reprinted with permission, copyright 2004, IEEE)

Polyimide and Packaging

The polyimide layer serves several functions. First, it creates a recess pit for the heater area, which helps confine the area for the bubble. Second, it creates a smooth surface on the heater wafer for better bonding. The polyimide surface is planarized using chemical mechanical polishing after patterning. Third, polyimide is also part of the ink channels that connect the ink nozzles and ink inlet. The ink flow resistance

can be fine-tuned by the polyimide pattern. Fourth, the polyimide on the heater wafer during dicing can protect the electronics from the silicon debris thrown off from the dicing blade. The small silicon shards can penetrate the passivation oxide and short out the underlying electronics. Finally, it serves as a cushion layer during the dicing. After wafer bonding, a half-way dicing cut is needed to cut the channel wafer only, not the heater wafer in order to expose the bond pads on the heater wafer. Typical polyimide thickness is about 15–50 μm.

The heater wafer and the channel wafer are bonded together using polymeric adhesives (such as EPON™ epoxy resin) and the infrared aligning tool [83]. During bonding, the polymeric adhesives may be adversely squeezed out of the contact areas under the pressure and heat, and spilled into the channels causing the blocking of the ink channels. To avoid this problem, a thin film of adhesive is first uniformly coated on an intermediate carrier substrate and then transferred onto the channel wafer for bonding. This adhesive transferring process can reduce the adhesive thickness to less than 2 μm and eliminate the blocking problem. The adhesive is cured under pressure at a temperature less than 200°C. Another method to bond the heater and channel wafers through the polyimide layer is electrostatic bonding by applying 1 kg/cm^2 clamping pressure and 100 V at 350°C (see Section 4.3.2.3 for more details).

Similar to the LED bar used in scanners, multiple TIJ chips can be butted together to make a long printhead, usually called a full width array. It has a full width of regular paper size such as 8.5 in. or larger. This is unique for TIJ MEMS chips inasmuch as most MEMS devices contain only one die in the system. A typical TIJ die length is less than 1 in. Thus, it would take about a dozen die to make a full width array printhead. The main advantage of a full width array is the increase of printing speed. The challenges of a full width array are the precision of dicing required for butting the die with less than 20 μm variation, the complex connection to the ink supply, and the required fast drying of the large amount of ink deposited on the print in a relatively short time.

Chip warping is a common problem for wafer bonding due to mismatch in the thermal expansion coefficients. By combining low temperature bonding and the same thermal expansion coefficients for both plates, chips longer than 1 in. can be produced in this design without much warping.

14.8.3.5 Microbolometer (Honeywell)

The uncooled MEMS microbolometer technology has been a revolution in long-wavelength infrared (LWIR) sensing applications [84]. LWIR is the infrared band from about 8 to 14 μm and coincides with an atmospheric window. Up to the time of this invention, infrared focal plane arrays (i.e., imager die composed of an array of pixels) were implemented using small bandgap semiconductors, such as mercury–cadmium–telluride (HgCdTe), which required that these sensors be continuously cooled to liquid nitrogen temperatures to prevent the incoming signal from being swamped out by thermally generated charge carriers. The requirement of refrigeration combined with a very expensive fabrication process to merge these exotic

semiconductors with integrated circuits for readout electronics meant that the cost of these infrared imagers was very high and also susceptible to failure mechanisms. Nevertheless, these cooled IR detectors have been extensively used for military applications where the ability to see in the dark is critical.

Using micromachining technology to create thermally isolated structures that simultaneously possess low thermal capacitance, have allowed uncooled infrared sensors to be demonstrated having noise equivalent delta temperatures (NEDTs) of 40 mK or better, which is a performance level that many thought was possible only with a cooled approach [84–86].

In the 1980s and 1990s, two companies pioneered the development of uncooled MEMS infrared devices. One of these companies was Texas Instruments, who developed a pyroelectric-based sensing scheme and the second was Honeywell, who developed a microbolometer approach. The Honeywell approach has been licensed to a number of companies who are producing focal plane array imager die for military, police, fire, and industrial applications. The basic mechanism by which the Honeywell microbolometer works is quite simple. Incoming infrared radiation is absorbed by a microstructure element (i.e., a detector pixel) and this absorbed radiation causes the microstructure to heat up. Contained within the microstructure element is a metal resistor that changes resistance as the temperature of the resistor changes. The key to the high performance of the microbolometer is that (1) the microstructure is thermally isolated from the substrate (Fig. 14.83), (2) the microstructure has a small thermal capacitance, and (3) the response of the temperature-sensitive resistor within the microstructure is very high. Specifically, the pixel temperature increases by a measurable amount even when the incoming infrared radiation is very small in magnitude. This is made possible by the high level of thermal isolation that is achieved in the microstructure. Also important is that the temperature of the microstructure changes relatively quickly as incoming infrared energy changes. This is made possible by the low thermal time constant of the

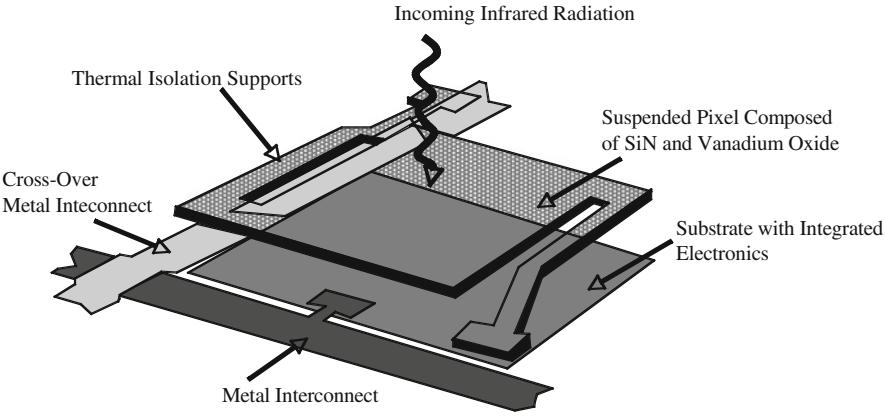


Fig. 14.83 Bolometer pixel that stands above the substrate to achieve thermal isolation

microstructure which is in turn made possible by the small thermal capacitance of the microstructure. Lastly, the transduction mechanism (how the incoming infrared energy is converted into an electrical signal) must be large. The microbolometer uses a resistor material (e.g., vanadium oxide (VOx) that has a very high temperature coefficient of resistance (TCR) value [84–86]. Figure 14.84 is a SEM of a section of a focal plane array of microbolometer devices.

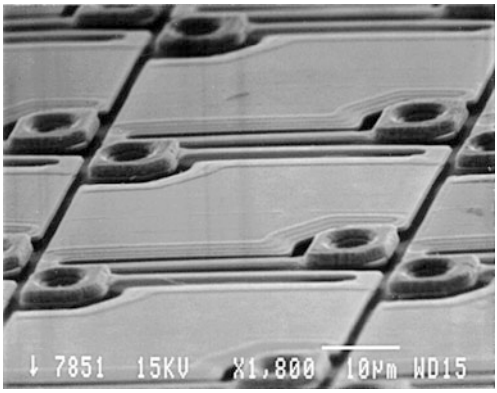


Fig. 14.84 SEM image of array of microbolometers (Reprinted with permission, copyright Honeywell International, Inc.)

Achieving the high performances demonstrated in the microbolometer is only made possible with MEMS technology. We review the process sequence used to produce the Honeywell microbolometer in order to demonstrate the benefits of MEMS fabrication (Fig. 14.85).

The fabrication of the microbolometers is an integrated MEMS process technology because it combines a large array of MEMS sensors on a microelectronics wafer. The first part of the fabrication of the microbolometers begins with a CMOS process sequence to implement the pixel readout and biasing electronics [84–86]. The microelectronics process includes those steps to implement the metallization interconnects for the devices. The MEMS is then fabricated on the surface of the CMOS wafer using low-temperature and processing steps chemically compatible to the microelectronics (Fig. 14.85). The desire for a high fill-factor focal plane array is a very important design consideration that drives an integrated MEMS process technology approach. The microbolometer fabrication is best classified as a "MEMS last" integration process technology. A number of different microelectronics foundry processes can be used so this portion of the process can be easily outsourced.

The CMOS starting wafer is suitably planarized (Fig. 14.85a). Next, the surface of the wafer is coated with a thin reflective material that is subsequently patterned to leave this material so that it will be located under the suspended microstructure pixels (Fig. 14.85b). A polymer material is then spin deposited onto the surface of the wafer. This polymer will act as a sacrificial layer during fabrication and will allow the microstructure to achieve excellent thermal isolation. The thickness of this layer is chosen to be 2.5 μm, which determines the gap between the microstructure

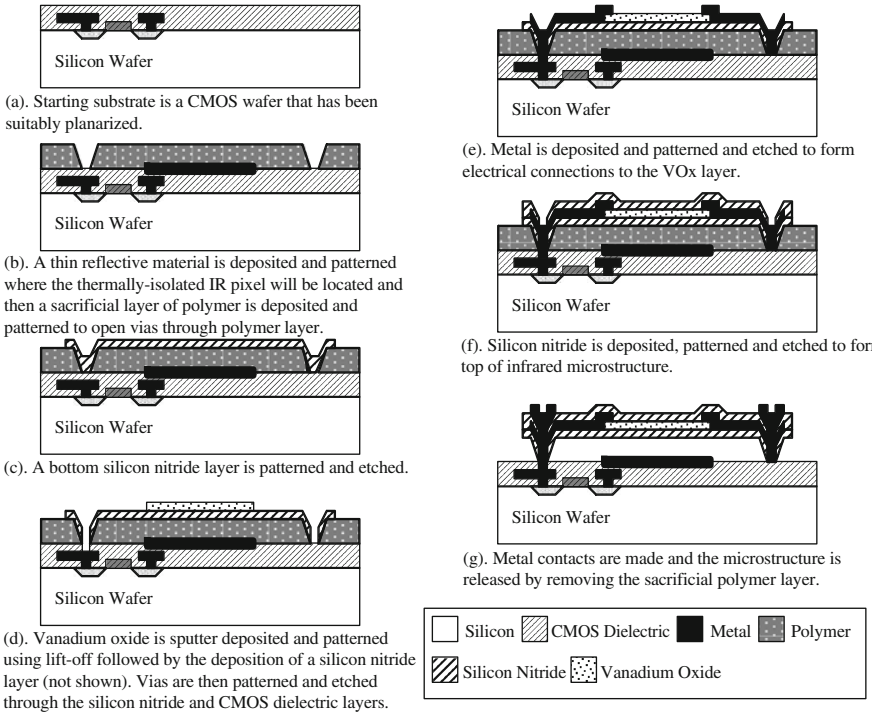


Fig. 14.85 Process sequence for fabrication of the infrared sensing microbolometer

sensor and the substrate surface. This gap spacing is driven by the desire to create an optically resonant cavity that is tuned to the middle of the 8–14 μm infrared bandwidth. The reflective material on the surface combined with the creation of an optical resonate cavity allows the absorption over the desired infrared band to be maximized at over 80%, even when the microstructure is less than 1 μm in total thickness.

Photolithography is then performed to pattern the polymer sacrificial layer into mesas that are located on the wafer surface where the pixels will be fabricated (Fig. 14.85b). Next, a thin layer of silicon nitride is sputtered onto the wafer to create the bottom layer of the suspended microstructure. Photolithography is performed to pattern the silicon nitride layer which is then etched using RIE (Fig. 14.85c). A layer of vanadium oxide (VOx) is then deposited by sputtering and photolithography is performed to pattern this layer. After the vanadium oxide layer has been etched, vias are made though the bottom silicon nitride and the CMOS dielectric layers in order to make electrical contact to the underlying CMOS electronics (Fig. 14.85d). A layer of metal is deposited, patterned, and etched to make electrical connection to the VOx sensors (Fig. 14.85e). Another layer of silicon nitride is then sputter deposited. This layer of silicon nitride will create the top layer of the microstructure. Photolithography is performed to pattern the silicon nitride layer, which is then

etched using RIE (Fig. 14.85f). Lastly, metal contacts are made to the devices and then the sacrificial layer of polymer is removed by exposing the wafer to an oxygen plasma etch to release the microstructure (Fig. 14.85g).

14.8.3.6 ASIMPS and ASIM-X (CMU)

The Application-Specific Integrated MEMS Processing Service (ASIMPS) and the closely related Application-Specific Integrated MEMS-Exchange (ASIM-X) are process technologies developed at Carnegie Mellon University that use micromachining on CMOS wafers produced on a commercial foundry IC process to make micromechanical devices integrated with microelectronics [87, 88]. The ASIMPS process uses the CMOS interconnect layers as the micromechanical material. We describe the ASIM-X process technology, which is similar to ASIMPS but incorporates bulk silicon under the CMOS interconnect layers to make relatively thick single-crystal silicon micromechanical devices. The commercial foundry processes that have been used in the ASIM-X process technology include: the Jazz Semiconductor 4-layer metal 0.35 μm SiGe60 BiCMOS; the Taiwan Semiconductor Manufacturing Company (TSMC) 4-layer metal 0.35 μm CMOS; and the IBM 5HPE SiGe BiCMOS using a 4-layer metal 0.35 μm linewidth CMOS. The ASIM-X process has found application for the implementation of resonators, inertial sensors, optical elements, and many other MEMS devices (See Fig. 14.86).

The ASIM-X process begins with the fabrication of the microelectronics at a commercial foundry (Fig. 14.87a) [87]. Upon receipt, the substrates are then mounted onto a handle wafer with the topside down using a resist layer as an adhesive.

Photoresist is then deposited on the CMOS substrate and photolithography is performed (Fig. 14.87b). Subsequently, a timed backside DRIE is performed through most of the thickness of the CMOS substrate leaving a single-crystal silicon layer of approximately 50 μm (Fig. 14.87c).

Next, a timed isotropic silicon etch is performed using xenon di-fluoride (XeF_2) as seen in Fig. 14.87d. The CMOS substrate is then debonded from the handle wafer

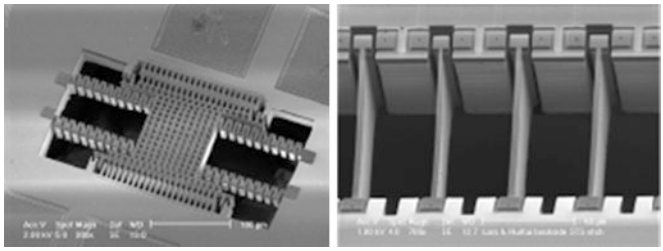


Fig. 14.86 SEM images of integrated MEMS devices implemented using CMU ASIMPS or ASIM-X process technologies. Device shown in *left* image is an integrated inertial sensor and device shown on *right* is a series of integrated micromechanical resonators (Reprinted with permission, copyright Prof. Gary Fedder at Carnegie Mellon University)

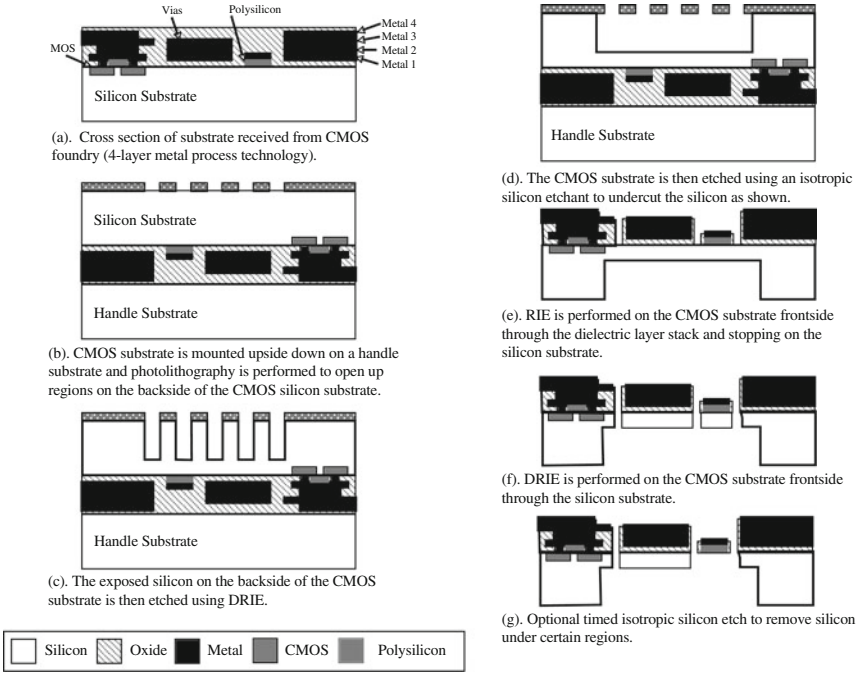


Fig. 14.87 Process sequence for ASIM-X process

and a photolithography step is performed on the top surface of the substrate. The exposed regions of the multiple-layer dielectric on the CMOS substrates are then etched using a RIE and stopping on the silicon substrate (Fig. 14.87e). Without performing additional photolithography, a DRIE is performed on the substrate front side (Fig. 14.87f). Optionally, an isotropic silicon etch may be performed to undercut the narrow beams made in the silicon etch process to create released structures of the multilayer CMOS metallization stack without silicon beams underneath (Fig. 14.87g). A derivative of the ASIMPS process is used by Akustica for the production of commercial microphones.

14.8.3.7 Integrated CMOS+RF MEMS Process (wiSpry)

A large number of RF MEMS processes have been developed over the last 10–15 years. In general, each of these processes has been developed to construct a specific RF MEMS device, such as a series switch, capacitive switch, variable capacitor, inductor, and so on [89–91]. Few of these processes have demonstrated the flexibility to produce the range of devices that would support a full RF subsystem, such as a phase shifter or tunable filter.

The materials required for RF MEMS have more specific requirements than are required for quasi-static electromechanical MEMS. Insulators require low dielectric constants and low loss-tangents. Depending on the application they can also

require high breakdown fields. Conductors in general require higher bulk conductivities than would be acceptable for a quasi-static application. In the case of contact switches, the contacting conductor's properties are critically important to both the electrical performance and the lifetime. A great deal of work has been done to try to understand the contact switching behavior of various MEMS metals and alloys [92]. Contact resistance as a function of contact force and contact wear characteristics must be well characterized and understood to provide a reliable high-performance device.

WiSpry, a start-up RF MEMS company, set out to develop a process that was flexible enough to support a full range of RF MEMS devices [93]. They focused on low deposition temperature CMOS-compatible processing steps with low stress and low loss materials. They chose silicon dioxide as the MEMS structural layer for its good mechanical properties and its ability to electrically isolate the signal and actuation areas within a device. They chose thick copper as the via and interconnect conductor to provide high conductivity and process compatibility. They chose thin gold as the surface electrode and switch contact conductor because of its low contact force and subsequent low contact resistance, and low self-adhesion leading to good contact wear performance.

The WiSpry process is a "CMOS first" process that starts with a commercial 0.18 μm HV CMOS process on a low-resistivity 200 mm silicon wafer. The MEMS process is divided into three sections: substrate connect, thick metal, and thin metal. The substrate connect process uses the standard CMOS metallization to route and connect to vias that connect up to the first thick metal layer.

The thick metal section is constructed by depositing 3.5 μm of copper embedded in silica and planarized with CMP. Then another 3.5 μm layer of copper is deposited and planarized to form stud interconnect (vias). Figure 14.88 shows a process cross-section that contains one of these 7 μm thick double metal layers; however, this

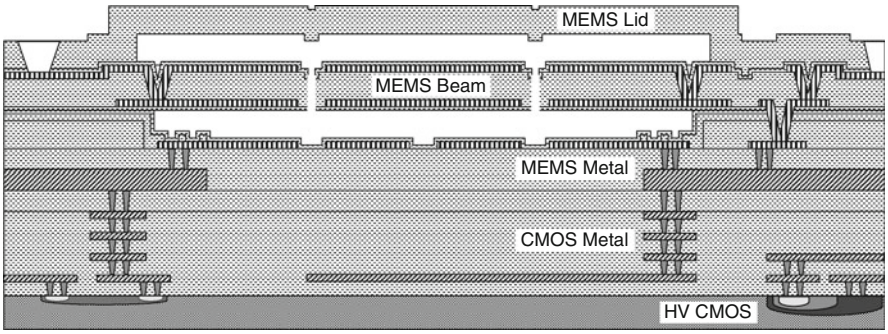


Fig. 14.88 Cross-sectional diagram showing the layers of the WiSpry CMOS first integrated RF MEMS process: CMOS and its interconnect layers (HV CMOS and CMOS Metal), thick metal interconnect layer (MEMS Metal), the gold counterelectrode layer, the gold metallized silicon dioxide structural layer (MEMS Beam), and the wafer-level cap (MEMS Lid) (Reprinted with permission, copyright WiSpry, Inc.)

double deposition can be repeated multiple times. The nominal process uses two of these layers.

The thin metal section forms the surface electrodes, switch contact surfaces, and released MEMS structures. It is composed of three layers of 0.5 μm thick gold, one deposited on the insulating surface of the underlying thick metal section, and one on the upper and lower surface of the released MEMS "beam." The sacrificial layers that allow construction and then release of the silica beam are a 1.5 μm copper layer (below) and a 0.5 μm copper layer (above).

The MEMS structure is encapsulated at the wafer level to protect the MEMS device from contamination, moisture, and the backend processing, such as flip-chip processing, back grinding, dicing, and assembly. Figure 14.89 shows a cross-section of the entire structure. This integrated MEMS+CMOS die is then flip-chip mounted to a substrate to provide a final product solution.

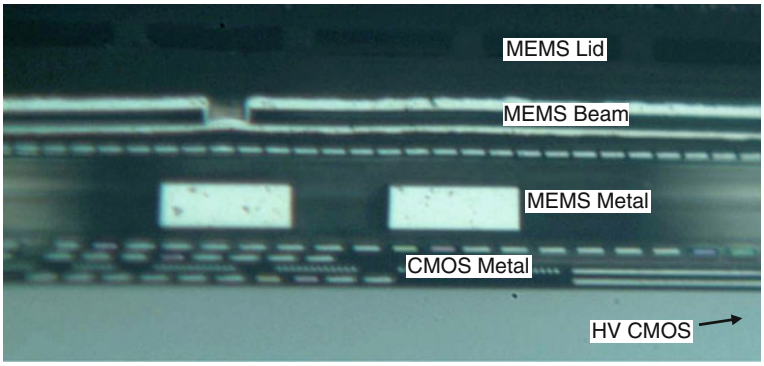


Fig. 14.89 Cross-section showing the CMOS Metal layers, the copper interconnect layer (MEMS Metal), the gold counterelectrodes, the MEMS beam and the wafer-level cap (MEMS Lid) (Reprinted with permission, copyright WiSpry, Inc.)

14.8.3.8 Integrated SiGe MEMS (UCB)

The SiGe process module is intended to solve the problem of merging crystalline semiconductor materials with electronics [94–96]. As a general rule, a CMOS wafer with metallization and transistor device junctions cannot be exposed to temperatures above about 450°C without degradation of the microelectronics, thereby placing severe restrictions on the types of processing steps which can be employed for a "MEMS last" monolithic integration strategy. Typically, crystalline semiconductor materials, such as polycrystalline silicon or polysilicon, are deposited using LPCVD due to its inherently low cost and simple processing, as well as the high quality films that are produced with this technology. However, the deposition temperatures of LPCVD polysilicon are well above 450°C (they are typically in excess of 600°C). Furthermore, it is almost always necessary to anneal LPCVD deposited polysilicon films at temperatures above 900°C to reduce the residual stress and stress gradient for the material to be useful as a structural micromechanical layer for the implementation of MEMS devices.

One approach to avoiding this problem is to fabricate the MEMS first and then proceed to the fabrication of the CMOS. An example of this is the Sandia Integrated MEMS process technology, which is reviewed in the next section [97]. Another strategy is the MEMS last wherein the MEMS are made from a completed CMOS wafer using the silicon substrate and thin-film layers from the CMOS process to implement the MEMS devices. Both of these approaches have their respective advantages and disadvantages [94–97].

Another example of a MEMS last approach was recently reported by UCB [95, 96] and uses LPCVD polycrystalline silicon germanium (SiGe) as the structural micromechanical material layer rather than polycrystalline silicon (polysilicon). The advantage is that SiGe can be deposited at a much lower temperature than polysilicon, thereby allowing CMOS wafers from virtually any foundry to be used in this process to obtain monolithically integrated MEMS–CMOS.

The sequence is essentially a surface micromachining MEMS process (Fig. 14.90). The fully metallized and completed CMOS wafer has photolithography and etching performed to open up vias to the underlying polysilicon lines in order to make electrical connection from the MEMS to the CMOS microelectronics. It is possible to open up vias to the metal, but this risks contaminating the SiGe deposition process tool with a metal and therefore the CMOS polysi is used as the electrical interconnection layer. A LPCVD deposition of $Si_{0.35}Ge_{0.65}$ is performed at 450°C that is approximately 400 nm in thickness. This layer will act as

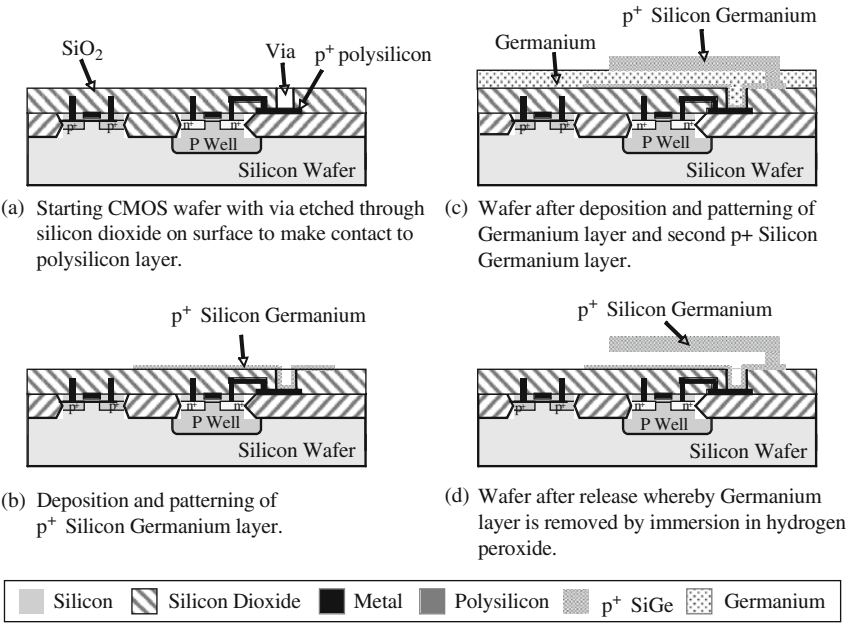


Fig. 14.90 Process sequence for UCB silicon germanium monolithically integrated CMOS–MEMS process technology

a ground plane for the MEMS devices. The layer is defined using photolithography and RIE etching. Next, a pure germanium layer is deposited at 375°C, which is 2 μm in thickness and will act as a sacrificial layer in this surface micromachining process.

A two-step photolithography can now be performed on the sacrificial layer: the first to make shallow dimples to reduce stiction effects and the second to open up anchors and electrical connections from the structural layer to the ground-plane. Given the low selectivity of the germanium RIE etch compared to the underlying $Si_{0.35}Ge_{0.65}$ layer, a very thin layer of LTO is used between these two layers as an etch stop. After the LTO is removed in the anchor regions using short-duration HF immersion, a structural layer of $Si_{0.35}Ge_{0.65}$ is deposited by LPCVD at 450°C to a thickness of 2.5 μm. This structural layer is then defined using photolithography and RIE etching. The MEMS device is then released by immersion of the substrate into a solution of hydrogen peroxide (H_2O_2), which is safe to use with the CMOS devices.

Although this process is very simple compared to many of the other monolithic integration approaches, a major disadvantage is the length of time that the wafers are held at 450°C for the poly SiGe depositions, which is over 3 h. Consequently, this process is appropriate for use with older CMOS technologies wherein the diffusion depths and metal linewidths are not too aggressive. To overcome this limitation, several groups have been working to develop a technology to deposit poly SiGe using PECVD or a combination of PECVD and LPCVD with the purpose of reducing the time the wafers are held at higher temperatures as well as opening the capability of depositing thicker structural layers.

14.8.3.9 Integrated SUMMiT (Sandia)

The Integrated Summit process was developed by Sandia National Labs in the early to mid-1990s and is a sophisticated process technology that monolithically integrates MEMS surface-micromachined components with CMOS microelectronics [97]. This integrated MEMS process technology is termed a so-called "MEMS first" process whereby the MEMS components are fabricated on the wafers first and then the wafers are processed through a standardized CMOS process line to fabricate the microelectronics. The Sandia approach of using MEMS first was to create a deep trench in the surface of the wafer within which the MEMS devices are then fabricated, followed by chemical mechanical polishing to planarize the wafer surfaces so that they can be processed on a CMOS fabrication line.

This approach provides two major processing advantages compared to either an "interleaved MEMS" process technology (such as the Analog Devices' iMEMS process described above) or a MEMS last process technology (such as the CMU ASIMPS process described above). Specifically, the MEMS first approach developed by Sandia eliminates the large topology on the substrate surface because the MEMS are embedded into the substrate, which is then planarized so that it can be processed on a CMOS process equipment set. Secondly, inasmuch as no microelectronics fabrication begins until the MEMS are made, there is a very

high thermal budget available for the MEMS fabrication. Therefore, the materials used in the MEMS fabrication, such as polycrystalline silicon can be deposited at higher temperatures and therefore higher rates, and these materials can be annealed at temperatures sufficient to relieve the residual stress in the as-deposited layers.

Although this process solves some major technical challenges of integration of MEMS with microelectronics, it also presents a potentially major disadvantage as well. This process technology was developed by a government laboratory, which had both very advanced MEMS and CMOS fabrication capability. To be of maximum benefit to the community, the MEMS first processing and the CMOS last processing could be performed at different foundries. This would allow much broader use, market acceptance, and penetration. However, a major question with this process is whether a CMOS foundry would allow preprocessed wafers with MEMS devices embedded into the substrates to be processed on their process line.

The Sandia Integrated MEMS process technology begins with standard silicon wafers (Fig. 14.91). A photolithography step and etching is performed on the substrate surface to create alignment marks that will be used in subsequent processing

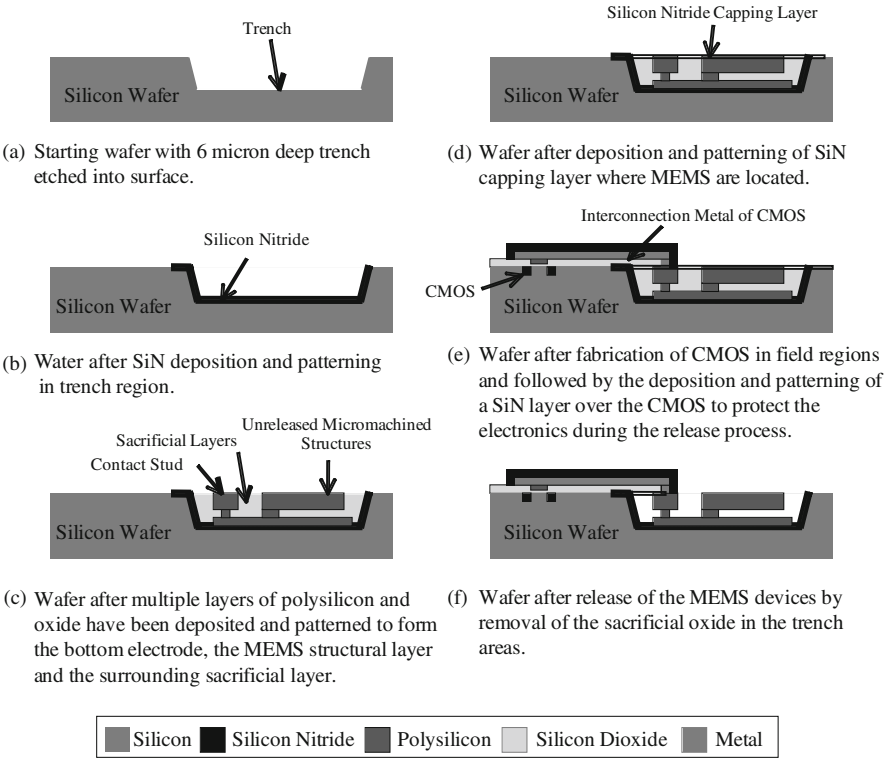


Fig. 14.91 Process sequence for Sandia's Integrated MEMS process

steps. Next, another photolithography is performed, followed by a KOH anisotropic wet chemical etch to form a trench that is approximately 6 μm deep into the top surface of the wafer. The sloping sidewalls of the resultant trenches are used as an advantage in this process sequence. They improve the photolithography processes used to define the MEMS structures, which are made at the base of the trench. That is, depositing photoresist onto the surfaces at the bottom of the trench would be more difficult if the edges of the trenches were vertical. Normally there would be a disadvantage with these sloping trench sidewalls as well, namely the ability to resolve fine features for the MEMS structures in the trenches due to the separation between the mask and the layer to be patterned. However, Sandia claims that by making alignment marks at the bottom of the trenches, the resolution of the MEMS features can be improved to about 1 μm. Nevertheless, this does add an additional photolithographic step to the overall process flow.

A silicon nitride layer is next deposited using LPCVD on the wafer to create a dielectric layer on the bottom of the trenches. This layer is defined using photolithography and a RIE etch. Next, a layer of polycrystalline silicon is deposited using LPCVD and then this layer is defined to make the bottom electrodes for the MEMS devices using photolithography and etching. A silicon dioxide (SiO_2) layer is deposited using LPCVD which will act as the sacrificial layer for the MEMS device processing. This oxide layer is defined using photolithography and etching. Another polycrystalline silicon layer is deposited using LPCVD and this layer is defined to make the structural mechanical layer for the MEMS devices using photolithography and etching. The depth of the trench must be accurately controlled so that the contact stud can be formed to make electrical contact between the microelectronic interconnect metal layer and the MEMS structural layer. Subsequently, the trench is filled with a deposited oxide using a deposition technique that does not result in any voids.

The surface of the MEMS-processed wafer is then planarized using CMP resulting in a surface topology essentially equivalent to that of a prime silicon wafer. The wafer is also annealed at a high temperature to relieve any residual stresses in the micromechanical material layers, specifically the polysilicon structural layer. A layer of silicon nitride is then deposited onto the wafer and defined using photolithography and etching to result in a capping layer of SiN over the areas of the wafer where the MEMS structures are located, and the SiN is removed where the CMOS is to be fabricated.

The wafer is then ready for the CMOS fabrication wherein the microelectronics are fabricated in the substrate field regions (i.e., the substrate surface areas where the MEMS structures are not located) using a standard CMOS process flow. A metal interconnection layer runs from the CMOS to the contact stud previously fabricated in the area of the wafer where the MEMS are located to make electrical connection between the CMOS and MEMS. At the completion of the CMOS process sequence, the capping layer of SiN is removed so that the MEMS structures can be released using a HF immersion to remove the oxide material surrounding the MEMS structural polysilicon layer. The CMOS is protected by a layer of photoresist.

The Sandia Integrated MEMS process technology is highly modular, wherein the MEMS fabrication is distinct from the CMOS fabrication and vice versa, thereby potentially allowing this technology to be implemented with a number of CMOS process technologies available from any number of commercial foundries. However, as mentioned above, many commercial CMOS foundries may be reluctant to use preprocessed wafers with embedded MEMS structures in their CMOS fabrication lines. Other disadvantages of this process technology include: the photolithography of the MEMS structures performed at the bottom of the trenches limits the linewidth resolution of the MEMS structures; this process technology has a large number of processing steps including photolithography processes; it is important that high-quality deposited oxides are used for the sacrificial oxide layers to avoid voids and out-gasing during subsequent processing steps; and the thickness of the MEMS structural layer is limited to only a few microns.

14.9 The Economic Realities of MEMS Process Development

The amount of investment required to develop and manufacture a MEMS device has a huge impact on whether a MEMS business venture will be successful. The amount of time it takes to develop a MEMS device is also extremely important for many new technology-based products due to the limited window of market opportunity. The purpose of this section is to convey some guidance about the cost and time involved in MEMS development and as part of that discussion we demonstrate some of the techniques often used to estimate the cost of MEMS devices before they are in production. Ultimately, business ventures are most concerned about the return on investment (ROI). Ideally, a MEMS business venture would want to be able to estimate these costs and schedules as accurately as possible before any significant funds have been spent on development, so that the ROI can be predicted at the outset.

14.9.1 Cost and Time for MEMS Development

By now the reader will know that MEMS development can be a very challenging endeavor, but the question we now address is how much time and money can be expected to be spent on developing a new MEMS device. For example, unless the MEMS developer is fortunate enough to be able to access an existing (i.e., already fully developed) process technology, he or she will inevitably be required to develop a process sequence. Obviously, this will have a huge impact on the product's ROI. Given the truly enormous range of MEMS devices, applications, and methods used for implementation, it should not be surprising that there is no single formula for making these estimations. Indeed, as with much else related to MEMS technology, these kinds of analyses require access to a significant amount of information and

considerable practical experience to do them well. Nevertheless, we review some basics of how these estimations are performed in order to give the reader some appreciation of the factors and issues involved.

First, it is important to set some ground rules as to what is included in the estimation of development costs for a MEMS device. Specifically, there are many possible items that may be included, such as: setting up a foundry facility, setting up a packaging facility (which may or may not be considered part of the foundry facility), procurement of fabrication equipment capital tooling, procurement of packaging equipment capital tooling, procurement of testing equipment capital tooling, technology licensing fees, and so on. These cost items can vary over a very large range of values depending on many factors including the scale of the operation, the type and automation level of the facility and tools, and whether any development may be required for these resources.

It would be wrong to assume that all the required fabrication equipment, facilities, packaging, and testing equipment for the production of a MEMS device will be readily available from equipment suppliers. For example, many of the companies who entered into the MEMS inertial crash airbag sensor market found that production testing equipment for inertial sensors was not available from any supplier and therefore they were forced to develop this capability themselves at significant expenditure of both time and money. This is a relatively frequent occurrence for many companies who are going into new application areas of MEMS technology. Obviously, such a situation can have a big impact on the development cost and schedule. The determination of whether the needed production equipment resources are available by procurement is best determined by a careful review by experienced MEMS fabricators.

In estimating the total cost to produce a MEMS product it is common practice to break the total cost into two elements: the nonrecurring expenses and the recurring expenses. Nonrecurring expenses are fixed costs and are mostly independent of sales volume. They include the expenses involved in developing a new product design that is manufacturable. Recurring expenses are variable costs and depend on the sales volume. They account for the costs directly attributable to manufacturing the product and typically include material costs, fabrication costs, assembly costs, testing costs, and the like.

The nonrecurring or fixed expenses are examined first. For the fixed expenses, we separate the costs to build the manufacturing capability, including the cost of the capital tooling, from the actual costs of device development, what are commonly termed the nonrecurring engineering (NRE) costs. It should be noted that there is a coupling between the development cost, the existence of (or lack of) accessible foundry infrastructure, and the mode of access to these resources, but for the sake of simplicity, we ignore these effects in this discussion and review foundry costs first.

There are relatively well-developed methods for estimating the costs of establishing integrated circuit foundries based on the size and number of substrates to be produced on an annual basis and the type of process technology that will be employed in production (e.g., 45 nm CMOS, DRAM, etc.). For example, the cost to build and equip a state-of-the-art 300 mm integrated circuit foundry has reached

several billion dollars. The cost of integrated circuit foundries has exponentially increased over the past few decades from around $10 million in the early 1970s to over $3 billion today and this cost escalation is expected to continue in the future. What is surprising, however, is that the per-unit cost of the die produced in these facilities has continued to drop despite the large increase in foundry costs. The major reason for this is the fact that larger foundries can produce more ICs. These foundries have equipment to process larger wafers, which enables more die real estate to the square power.

The smaller linewidths that can be produced in these state-of-the-art foundries allow the die to be made smaller, allowing more die per wafer. These attributes allow the cost to be driven out of the production at a rate faster than the rate at which foundry costs are increasing. It is important to note that the output of modern integrated circuit foundries has reached such high production levels that many companies cannot utilize the entire production capacity that these facilities are capable of manufacturing for their internal needs. This coupled with the requirement of very high capacity utilization levels in order to cover the enormous costs of building and operating these foundries has resulted in the increasingly common practice of many companies to outsource the manufacturing of integrated circuits. As a consequence, the number of companies retaining integrated circuit production core competencies is decreasing every year, with more and more production capability being pooled into very large pure-play foundry operations, such as Taiwan Semiconductor Manufacturing Corporation (TSMC).

The foundry situation for MEMS is quite different. The estimation of the costs of establishing the required foundry facility infrastructure for a MEMS technology can vary over a huge range, with commensurately large variations in the cost of procuring and installing the required fabrication process equipment. Specifically, the cost of building and facilitating a dedicated MEMS foundry (i.e., no integrated circuit manufacturing capability) including capital equipment tools may range from a few $10 s of millions on the low side to a few $100 s of millions or more on the high side. The range is largely determined by the size of the foundry, the size of the substrates being processed, the number of tools required, and the level of automation of these tools. In addition, the time it can take to build a foundry and procure and install the processing equipment is between one to 2 years or more and therefore must be considered in the development schedule (integrated circuit facilities take a similar amount of time to build and equip).

The primary reason that MEMS manufacturing facility costs are far lower than integrated circuit foundries is that most MEMS process technologies do not push the technology envelope of nanometer scale linewidth resolutions (a minimum resolution of a few microns is usually acceptable in a MEMS process technology), larger wafer sizes are not needed or even desired (because the required maximum production volumes are much lower, MEMS foundries are typically at the 150 mm wafer diameter level, whereas IC foundries process 300 mm wafers), and high levels of automation are not required or desired (automation often results in broken MEMS wafers!). Consequently, it is common to see many MEMS foundries reconfigured

from older and out-of-date integrated circuit foundries or equipped with used tools from equipment brokers.

It is also important to consider that MEMS production foundries are typically not able to achieve the same economies of scale due to the specialized nature of each MEMS device, application, and associated process technology. Therefore, much thought must be put into the decision of whether to build and facilitate a dedicated MEMS foundry. Important factors in this decision include the projected manufacturing volume that is required to satisfy the market with the intended device product(s), whether this production volume with the associated revenues and profits can cover the costs of building and operating the facility, the potential ability of selling excess foundry capacity, and, the ability and potential cost advantages gained by going "fabless" and leveraging from an existing MEMS foundry production capability.

Each of these factors should be carefully and objectively examined before making a decision. Although the option of selling excess capacity may sound inviting, in reality it can be very difficult to find customers that can utilize and are willing to purchase the excess production capacity of a foundry due to proprietary concerns and other issues. On the other hand, although it also may sound very inviting to outsource the production to an existing foundry, the problem is that significant investments will often be needed in order to have the correct equipment set for your specific MEMS manufacturing process technology installed at a foundry. This means that either you will pay for such equipment, reducing the financial benefit of outsourcing, or the foundry pays for the equipment and then recoups its costs by raising the per-die costs. Risk that the foundry will have financial problems and go out of business must also be considered. Clearly, selecting a suitable foundry and negotiating an appropriate contract are vital to the financial success of an outsourced MEMS product development.

We now examine the nonrecurring engineering costs of MEMS device development. This task is also neither simple nor easy. First, the process sequence and packaging method that will be employed should be well defined in order to estimate the development costs. Assuming that this is the case, then the question becomes one of defining whether any part of the process sequence can utilize existing and already developed process modules and/or processing steps. If this is the case, then the cost of running these process modules and/or processing steps will be available and can be added together to estimate the "developed" portion of the process sequence. Note that there may be licensing fees associated with the use of another party's intellectual property (IP).

The next step is to figure out how much of the process sequence is "undeveloped" and how much effort and risk is involved in developing these portions of the process sequence. The total of "developed" and "undeveloped" portions can then be integrated into a viable process sequence. Typically, the portions of the process sequence that need to be developed will require processing step development, running partial sequence experiments (short-loop experiments), and process integration. In many cases, transferring process recipes from research-oriented equipment (such as university fabs) to production tools in a manufacturing environment is best considered as "undeveloped" because the differences in tool types and settings can

be quite significant and may require significant time and effort to resolve. Estimating the time and cost of these activities will require experienced MEMS fabricators.

A major reason for the difficulty in estimating these costs is the widely varying difficulty and associated risk involved in developing a new processing step, process module(s), and process sequence. That is, a process sequence that pushes the technology envelope will be inherently more risky and more expensive (and take longer) to develop than one that does not. The determination of a process sequence's risk is something that requires a considerable amount of MEMS fabrication experience. Previous demonstrations of a fabrication method are extremely helpful for reducing process development risk, but it should also be noted that a published paper in an academic journal touting the merits of a process sequence should be viewed with a fair amount of skepticism with respect to statements regarding "high yield" and "manufacturability."

In addition to the risk level, another large determinant of NRE development cost will be whether the MEMS device is based on an integrated process sequence (i.e., MEMS merged with microelectronics on the same substrate). As a general rule, the cost to develop an integrated process sequence will be far more expensive than the development of a nonintegrated process sequence. As an example, the cost to develop the few integrated process technologies in current production was in most cases on the order of $100 M or more.

The last major determinant of NRE development cost will be the number of processing steps in the process sequence and the difficulty in integrating those steps into a viable process sequence. To date, most nonintegrated MEMS process technologies have required on the order of a few $10 Ms or more to develop to production level capability. Moreover, the average length of development time from taking a MEMS device from concept to a manufacturable product has often been over 5 years. It is important to note that both the total time and cost of MEMS development can be significantly reduced by leveraging from existing process technologies. These figures are meant as useful guidance on MEMS development costs, not as exact estimations that are applicable to every scenario or situation. An accurate estimate of NRE cost to develop a fully or partially customized MEMS process sequence requires knowledge of the specifics of the process sequence to be employed, access to costing information (preferably from multiple foundries and sources), experienced MEMS developers, and if possible, software to automate the ability to change important variables such as wafer sizes, tools, and so on. Most of these resources and capabilities are proprietary and are not generally available free of charge to the public. However, there are organizations that have these resources and they can provide these estimates as a service [98, 99].

The development costs of packaging, including assembly and testing, must also be taken into account. As described above, MEMS packaging often requires a unique and highly customized solution and therefore existing packaging approaches may not be suitable. If this is the case, a customized packaging solution will need to be developed. It is difficult to estimate the cost of packaging development inasmuch as it can vary over such a large range. This is particularly true when specialized assembly, packaging, or testing equipment is not available and needs to

be developed. For example, for microfluidic inkjet printheads, the assembly and packaging cost can be several times the chip cost. Therefore, it is advisable to consult with an experienced and knowledgeable MEMS packaging technologist for assistance in developing a plan and estimating these costs.

14.9.2 Production Cost Models

Production costs are a variable cost and as stated above are directly attributable to the manufactured product and are proportional to the volume of product being produced. The development of accurate cost estimates for the production of MEMS devices and products is no easier a task to perform than for development. Although the methods of estimating production costs for the integrated circuit industry are fairly standardized and reasonably well developed, the same is not true for MEMS production. That is, there are standardized cost models for integrated circuits that are commonly used by industry, which typically estimate a cost per unit area (e.g., a few cents per square millimeter) depending on the exact process technology employed (e.g., 45 nm CMOS, etc.) and the volume involved. In contrast, the cost per area for a MEMS device could range from essentially equivalent to that of ICs on the low side to orders of magnitude more expensive on the high side.

Many of the same comments made with regard to estimating the development costs are equally applicable to MEMS production. Specifically, it is very difficult to develop cost models for "generic" MEMS processes that have a hope of being generally applicable, inasmuch as there are no generic MEMS processes or process technologies. That is, the cost to produce a MEMS device wafer is very dependent on specific details of the fabrication process sequence. Equally important is that the cost of production will also depend on the details of the fabrication facility's installed infrastructure, the production yield, the production volume, and the production capacity utilization. For example, yields in IC manufacturing are routinely above 90% once in high-volume production, whereas yields for MEMS production are often considerably lower, even in volume production. Similarly, IC foundry capacity utilization levels routinely run above 85%, whereas MEMS foundries often run at much lower utilization levels. These factors all have a significant impact on the cost of production, but can be very hard to estimate until the device is in a volume production scenario. In addition to the device wafer costs, there are probe, assembly, and test costs that are typically much larger than the wafer cost. In short, given the wide range and diversity of MEMS processes, process technologies, packaging approaches, assembly, and test methods, it is nearly impossible to provide a simple methodology that allows production costs to be accurately estimated. Therefore, our approach is to go through an illustrative example in the next section.

14.9.2.1 MEMS Hybrid Versus Integrated MEMS Production Cost

In this section we develop a cost estimate for the production of a MEMS device that requires microelectronics. We examine the case where the IC die is assembled in the same package as the MEMS (i.e., the hybrid approach) versus the case

where the MEMS is integrated with the microelectronics (i.e., the integrated MEMS approach). This example demonstrates how a cost analysis is performed, wherein the key decision is whether a cost savings is gained by integrating the MEMS device with electronics.

Production cost estimates are usually based on calculating the complete manufacturing cost of a packaged device, including any associated assembly and testing costs. Typically, the starting point is to calculate the usable amount of area available on the wafer, the number of die per wafer (which obviously depends on the size of the die and wafer diameter that the die are made from), and the number of "acceptable" or "usable" die per wafer (i.e., the production yield). Yields can be stated at various points in the production, including after fabrication, after assembly, after testing and packaging, and so on. The collective yield would be the product of each of the yields of all parts of the manufacturing process. Once the number of yielded die has been calculated, then taking the production cost of each wafer and dividing by the number of yielded die allows the cost of each die to be calculated. Other cost components such as mounting, packaging, and testing are then added to derive the cost of a fully assembled, tested, and packaged die.

Table 14.3 shows a calculation of the usable area and die yielded in our example for 150 mm diameter wafers wherein the blue fields are the values entered depending on the process, device type, and wafer size. Table 14.4 is the calculation of the usable area and die yielded for 200 mm diameter wafers. In this analysis and both Tables 14.3 and 14.4, the area of the CMOS die is varied from 0.5 to 4 mm^2 and the MEMS die area is constant at 0.5 mm^2. The other entries in this table are straightforward. The wafer edge exclusion is 3 mm for the CMOS wafers and 10 mm for the MEMS wafers. This refers to the annular-shaped area that lies between where the substrate is yielding acceptable devices and the actual edge of the wafer. The dies are either square or rectangular and the wafer is circular, therefore there will always be some wasted area at the edge of the substrate. This is independent of wafer diameter. Most starting wafers are beveled at the edges to reduce breakage during handling and this also results in some part of the substrate surface being unusable.

The larger amount of edge exclusion for the MEMS wafer as compared to the CMOS wafer is illustrative in MEMS fabrication wherein devices near the substrate edge often do not yield due to process nonuniformities and large topologies. The useful area is calculated by a simple calculation of (wafer radius [millimeters] – wafer exclusion [millimeters])^2 $\times$ 3.14. This assumes that the MEMS chip area is small compared to the wafer area such that the error associated with this "averaging" is negligible. For example, the good MEMS die per 150 mm diameter wafer in the first data column of Table 14.3, is equal to $13267/(0.5 + 0.05) * 90\% = 21,709$. Also note that the MEMS bond pad area in this example is entered as a separate line item (i.e., separate from the MEMS device area) in order to provide some flexibility depending on the packaging approaches that are being considered (i.e., different packaging approaches may require more or less bond pad area). Another reason for considering the MEMS die bond as a separate line item is that this area is not required in an integrated MEMS device.

Table 14.3 Calculation of the usable area for 150 mm diameter wafers[a]

Calculation of number of die							
Wafer diameter [D]	mm	Input D	150	150	150	150	150
CMOS wafer edge exclusion (without chips) [CWE]	mm	Input CWE	3	3	3	3	3
MEMS wafer edge exclusion (without chips) [MWE]	mm	Input MWE	10	10	10	10	10
Useful CMOS wafer area for 150 mm wafer [AreaC150]	mm^2	AreaC150 = pi * (D/2 – CWE)^2	16,278	16,278	16,278	16,278	16,278
Useful MEMS wafer area for 150 mm wafer [AreaM150]	mm^2	AreaM150 = pi * (D/2 – MWE)^2	13,267	13,267	13,267	13,267	13,267
CMOS circuit area incl. outside bond pads [CA]	mm^2	Input CA	0.5	1	2	3	4
MEMS area [MA]	mm^2	Input MA	0.5	0.5	0.5	0.5	0.5
MEMS chip bond pads area [MBA]	mm^2	Input MBA	0.05	0.05	0.05	0.05	0.05
Yield MEMS [YM]	%	Input YM	90.0%	90.0%	90.0%	90.0%	90.0%
Yield packaging and test [YPT]	%	Input YPT	96.0%	96.0%	96.0%	96.0%	96.0%
Yield CMOS (area dependent!) [YCMOS]	%	YCMOS = 1 – (CA * 0.005)	99.8%	99.5%	99.0%	98.5%	98.0%
Yield Integrated MEMS [YieldIM]	%	YieldIM = YM * YCMOS * 0.85	76.3%	76.1%	75.7%	75.4%	75.0%
Good CMOS chips per 150 mm wafer [NumC150]	#	NumC150 = (AreaC150/CA) * YCMOS	32,474	16,196	8057	5345	3988
Good MEMS chips per 150 mm wafer [NumM150]	#	NumM150 = [AreaM150/(MA + MBA)] * YM	21,709	21,709	21,709	21,709	21,709
Good integrated chips per 150 mm wafer [NumIM150]	#	NumIM150 = [AreaM150/(CA + MA)] * YieldIM	10,124	6732	4019	2856	2210

[a]Using a MEMS-only, a CMOS-only, and an integrated MEMS (i.e., MEMS integrated with CMOS on the same substrate) process technology

Table 14.4 Calculation of the usable area for 200 mm diameter wafers[a,b]

Calculation of number of die							
Wafer diameter [D]	mm	Input D	200	200	200	200	200
CMOS wafer edge exclusion (without chips) [CWE]	mm	Input CWE	3	3	3	3	3
MEMS wafer edge exclusion (without chips) [MWE]	mm	Input MWE	10	10	10	10	10
Useful CMOS wafer area for 200 mm wafer [AreaC200]	mm^2	AreaC200 = pi * (D/2 – CWE)^2	29,544	29,544	29,544	29,544	29,544
Useful MEMS wafer area for 200 mm wafer [AreaM200]	mm^2	AreaM200 = pi * (D/2 – MWE)^2	25,434	25,434	25,434	25,434	25,434
CMOS circuit area incl. outside bond pads [CA]	mm^2	Input CA	0.5	1	2	3	4
MEMS area [MA]	mm^2	Input MA	0.5	0.5	0.5	0.5	0.5
MEMS chip bond pads area [MBA]	mm^2	Input MBA	0.05	0.05	0.05	0.05	0.05
Yield MEMS [YM]	%	Input YM	90.0%	90.0%	90.0%	90.0%	90.0%
Yield packaging and test [YPT]	%	Input YPT	96.0%	96.0%	96.0%	96.0%	96.0%
Yield CMOS (area dependent!) [YCMOS]	%	YCMOS = 1 – (CA * 0.005)	99.8%	99.5%	99.0%	98.5%	98.0%
Yield Integrated MEMS [YieldIM]	%	YieldIM = YM * YCMOS * 0.85[1]	76.3%	76.1%	75.7%	75.4%	75.0%
Good CMOS chips per 200 mm wafer [NumC200]	#	NumC200 = (AreaC200/CA) * YCMOS	58,941	29,397	14,624	9700	7238
Good MEMS chips per 200 mm wafer [NumM200]	#	NumM200 = [AreaM200/(MA + MBA)] * YM	41,619	41,619	41,619	41,619	41,619
Good integrated chips per 200 mm wafer [NumIM200]	#	NumIM200 = [AreaM200/(CA + MA)] * YieldIM	19,408	12,906	7705	5476	4237

[a]Using a MEMS-only, a CMOS-only, and an integrated MEMS (i.e., MEMS integrated with CMOS on the same substrate) process technology

[b]We have assumed that when MEMS is integrated with CMOS that the collective yield will be the product of the yields of each of the process technologies and the resultant yield of the integration process, which is taken as 85% in the present example

The one set of entries in Tables 14.3 and 14.4 that are highly process-dependent (and also dependent on the die area) is yield. In general, there are standardized models for estimating yield for integrated circuits based on the number of defects per unit area and the die area [100, 101]. In general, similar statistical techniques can be used for MEMS production. It is important to note that the yield for a process technology always decreases as the die size increases. Having a yield that decreases with increasing die size is typical for semiconductor production because the probability of a random particulate or defect causing a device failure increases as the die gets larger.

In order to estimate the yield, the number of defects per unit area must be known, which will not be the case unless the process technology is already in production. In Tables 14.3 and 14.4 we show the MEMS die yield (i.e., yield for wafers having only MEMS devices without CMOS on the same substrate) as 90% and constant, inasmuch as in this model the MEMS die size is constant. As calculated for the CMOS die, the die size does vary and therefore the yield is dependent on the area of the die, which for the present example is calculated according to the equation Yield CMOS = YCMOS = 1 – (die area $[mm]^2$ * 0.005). (Note that this would translate into a yield of 99.5% for a die that is 1 mm^2.) In addition, there is another yield entry after packaging and testing of 96% that corresponds to the number of devices that meet the acceptance criteria after packaging and testing.

In our example, this is assumed to be independent of whether the packaging is for a hybrid approach or for an integrated MEMS device. The yield of package and testing of CMOS is usually very high, therefore we have assumed it to be 100% in our example. Lastly, the yield of the integrated MEMS, wherein the MEMS and CMOS are fabricated on the same wafer in this example is calculated by taking the product of the MEMS die yield, the CMOS die yield, and a factor for the yield for integrating these two processes on the same substrate, which is assumed to be 85% in this example. In the case of the first data column of Table 14.3, the yield for integrated MEMS, 76.3%, is calculated from 90% * 99.8% * 85%, and the good integrated chips per 150 mm diameter wafer are equal to (13,267/(0.5 + 0.5)) * 76.3%, or 10,124. This represents that increasing the number of photolithographic steps and combining MEMS and microelectronics on the same substrate will typically reduce the yield.

The last three rows of Tables 14.3 and 14.4 calculate the number of good die for the three cases of CMOS-only die, MEMS-only die, and MEMS-integrated with CMOS die for both 150 and 200 mm diameter wafers, respectively. Essentially these calculations take the usable area of the wafer and divide by the die area and then multiply by the yield. For the case of the MEMS-only die, the total die area is the sum of the MEMS area and the MEMS chip bond area. The number of good integrated MEMS die is calculated by summing the area of the CMOS and MEMS die, but neglecting the MEMS chip bond area because no MEMS device-specific bond pads are needed in the case of the MEMS integrated with CMOS.

Now that the number of die has been determined, we can calculate the cost of the die. Tables 14.5 and 14.6 calculate the cost per die for the three process

Table 14.5 Calculation of the cost per die for a MEMS-only, CMOS-only, and integrated MEMS[a]

Cost calculations							
Additional mounting cost for 2 chips [AM Cost]	$	Input AM Cost	0.04	0.04	0.04	0.04	0.04
Packaging and test cost [PT Cost]	$	Input PT Cost	0.12	0.12	0.12	0.12	0.12
CMOS wafer cost 150 mm Asia for 2 chip [CWCost150]	$	Input CWCost150	600	600	600	600	600
CMOS wafer cost 150 mm for integration [ICWCost150]	$	Input ICWCost150	700	700	700	700	700
MEMS wafer cost 150 mm [MWCost150]	$	Input MWCost150	800	800	800	800	800
Discrete CMOS chip cost 150 mm (0.35 μm) [DCCC150]	$	DCCC150 = CWCost150/NumC150	0.018	0.037	0.074	0.112	0.150
Integrated chip cost 150 mm [ICC150]	$	ICC150 = (ICWCost150 + MWCost150)/NumIM150	0.148	0.223	0.373	0.525	0.679
Discrete MEMS chip cost 150 mm [DMCC150]	$	DMCC150 = MWCost150/NumM150	0.037	0.037	0.037	0.037	0.037

[a]MEMS integrated with CMOS on the same substrate) process technology on 150 mm diameter wafers. As in Tables 14.3 and 14.4, the columns represent CMOS controller die areas of 0.5, 1, 2, 3, and 4 mm^2, respectively

Table 14.6 Calculation of the cost per die for a MEMS-only, CMOS-only and integrated MEMS[a]

Cost calculations							
Additional mounting cost for 2 chips [AMCost]	$	Input AM Cost	0.04	0.04	0.04	0.04	0.04
Packaging and test cost [PT Cost]	$	Input PT Cost	0.12	0.12	0.12	0.12	0.12
CMOS wafer cost 200 mm Asia for 2 chip (0.18 μm) [CWCost200]	$	Input CWCost200	800	800	800	800	800
CMOS wafer cost 200 mm for integration (0.18 μm) [ICWCost200]	$	Input ICWCost200	900	900	900	900	900
MEMS wafer cost 200 mm [MWCost200]	$	Input MWCost200	1000	1000	1000	1000	1000
Discrete CMOS chip cost 200 mm (0.18 μm) [DCCC200]	$	DCCC200 = CWCost200/NumC200	0.014	0.027	0.055	0.082	0.111
Integrated chip cost 200 mm [ICC200]	$	ICC200 = (ICWCost200 + MWCost200)/NumIM200	0.098	0.147	0.247	0.347	0.448
Discrete MEMS chip cost 200 mm [DMCC200]	$	DMCC200 = MWCost200/NumM200	0.024	0.024	0.024	0.024	0.024

[a]MEMS integrated with CMOS on the same substrate, process technology on 200 mm diameter wafers. As in Tables 14.3 and 14.4, the columns represent CMOS controller die areas of 0.5, 1, 2, 3, and 4 mm^2, respectively

scenarios for both a 150 mm diameter wafer (Table 14.5) and a 200 mm diameter wafer (Table 14.6). The costs per die are calculated by taking the input values of wafer processing costs for each of the scenarios (these input fields are shaded) and dividing by the number of good die from each process type and wafer diameter from Tables 14.3 and 14.4. Two types of CMOS processes are shown, specifically a 180 nm process technology on 150 mm diameter wafers and a 350 nm process technology on 150 mm diameter wafers. The production cost per wafer for a CMOS process is based on commercial rates, however, the same is not true for the MEMS wafer processing costs, which can vary from one MEMS process technology to another. For simplicity, we have assumed a mature MEMS wafer process technology with a cost of $800 and $1000 per wafer on 150 and 200 mm diameter wafers, respectively, as shown in Tables 14.5 and 14.6. Using the number of good die for a 150 mm diameter wafer in Table 14.3, we calculate the cost per die for a 150 mm diameter wafer as shown in Table 14.5. Likewise, the number of good die for a 200 mm diameter wafer from Table 14.4 can be used to calculate the cost per die for a 200 mm diameter wafer as shown in Table 14.6.

These conceptual cost models are based on the production of a straightforward surface-micromachined MEMS device. In the integrated case, the MEMS process technology is mixed with a circuit process technology such that a single die contains both the MEMS device and microelectronics. In the nonintegrated case, the MEMS device, with no circuitry, is on one chip and the circuitry is fabricated on a standard commercially available CMOS process technology. Both devices are packaged, assembled, and tested using the same methods and equipment. In all other respects, the integrated and nonintegrated MEMS devices are equivalent.

The first and most obvious difference is the cost of the MEMS device wafer. In the integrated process case, the cost represents a very sophisticated, complex, and high mask count process technology. The process complexity requires a large amount of fabrication infrastructure that must be amortized. The yield, although high, is reduced because of this complexity. The nonintegrated MEMS device is a much simpler and lower mask count process technology and the wafer cost is correspondingly lower. On the other hand, the nonintegrated process technology requires an ASIC wafer. However, because it can be produced in a standard commercial CMOS process technology, it can take advantage of the full economies of scale (not to mention the ever-increasing circuit density) of such a process technology.

The backend processes for both cases are very similar. Because of the complexity of the integrated MEMS process technology, 100% testing is almost always appropriate. In the nonintegrated process technology, 100% testing of the MEMS device is also generally recommended due to the large process variations associated with MEMS manufacturing. Testing of a standard commercial CMOS wafer, on the other hand, is often not cost effective. In this case, it is assumed that the ASIC wafer is not tested. Although the testing costs of the integrated and nonintegrated devices are shown as equivalent, it is often the case that the cost of testing the MEMS-only wafer is higher than the integrated wafer, due to the added time and

complexity needed to take measurements on a MEMS device without any on-chip circuitry.

Table 14.7 uses the values in Tables 14.5 and 14.6 to calculate the total cost of a packaged and tested die for three hybrid scenarios that include a two-die configuration wherein the CMOS die from a 150 mm process technology is combined with a die from a 150 mm diameter MEMS wafer, a two-die configuration wherein the CMOS die from a 200 mm process technology is combined with a die from a 200 mm diameter MEMS wafer, and a two-die configuration wherein the CMOS die from a 200 mm process technology is combined with a 150 mm diameter MEMS wafer. Also shown in the last two rows are the cases of an integrated MEMS process technology on both 150 and 200 mm diameter wafers, respectively. Adding the packaging and testing costs ($0.12 for the integrated device and $0.16 for a two-chip device) from Tables 14.5 and 14.6, we calculate the packaged die cost in Table 14.7. For example, in the two-die CMOS and MEMS 150 mm wafer case in the first column, $0.224 is calculated from ($0.018 + $0.037 + $0.16)/96%; in the integrated 150 mm wafer case, $0.279 is equal to ($0.148 + $0.12)/96%.

Figure 14.92 presents the calculated costs for the two-die system wherein both the CMOS and MEMS substrates are produced using 150 mm diameter wafers, compared to an integrated MEMS process technology produced on a 150 mm diameter wafer. The system costs are plotted as a function of the CMOS controller die area along the *x*-axis. As can be seen, no matter the CMOS controller die size, the two-chip system is always less expensive. This may be a surprising result considering that there are both integrated and nonintegrated devices in the marketplace. However, as we discussed in Sections 14.5.6 and 14.6.1, the decision to use an integrated or nonintegrated process requires a full system-level tradeoff analysis and time-to-market business consideration, not simply a cost analysis. Figure 14.93 presents the calculated costs for the two-die system wherein both the CMOS and MEMS substrates are produced using 200 mm diameter wafers, compared to an integrated MEMS process technology produced on a 200 mm diameter wafer. The system costs are plotted as a function of the CMOS controller die area along the *x*-axis. Again, no matter the CMOS controller die size, the two-chip system is always less expensive.

Obviously, the parameters of this model that are most difficult to estimate are the MEMS wafer production costs, the MEMS packaging, assembly, and testing costs, and the yield of the MEMS manufacturing process. (Note: the model portrayed here is only applicable if the MEMS is capped on the wafer level and therefore this cost is included in the MEMS device production cost.) Estimates for each of these parameters are best performed by very experienced fabricators by creating a range for each of these parameters and then calculating the associated costs in order to set reasonable boundaries of the actual costs. Similar to estimation of the development costs, there are organizations that can develop production cost estimates for MEMS devices [98, 99].

Table 14.7 Calculation of the total system cost for various configurations[a]

Total cost for packaged and tested system							
2 chip CMOS and MEMS 150 mm wafer [Cost, 2 Chip 150]	$	Cost, 2 Chip 150 = (DCCC150 + DMCC150 + AM Cost + PT Cost)/YPT	0.215	0.244	0.283	0.322	0.362
2 chip CMOS and MEMS 200 mm wafer [Cost, 2 Chip 200]	$	Cost, 2 Chip 200 = (DCCC200 + DMCC200 + AM Cost + PT Cost)/YPT	0.206	0.220	0.249	0.278	0.307
2 chip 150 mm MEMS wafer with 200 mm CMOS wafer [Cost, 2Chip, M150 + C200]	$	Cost, 2 Chip, M150 + C200 = (DCCC200 + DMCC150 + AM Cost + PT Cost)/YPT	0.219	0.233	0.262	0.291	0.320
Integrated 150 mm wafer [Cost, I150]	$	Cost I150 = (PT Cost + ICC150)/YPT	0.279	0.357	0.514	0.672	0.832
Integrated 200 mm wafer [Cost, I200]	$	Cost I200 = (PT Cost + ICC200)/YPT	0.227	0.278	0.382	0.486	0.592

[a]Including fabrication, packaging, assembly, and testing. As in Tables 14.3 and 14.4, the columns represent CMOS controller die areas of 0.5, 1, 2, 3, and 4 mm^2, respectively

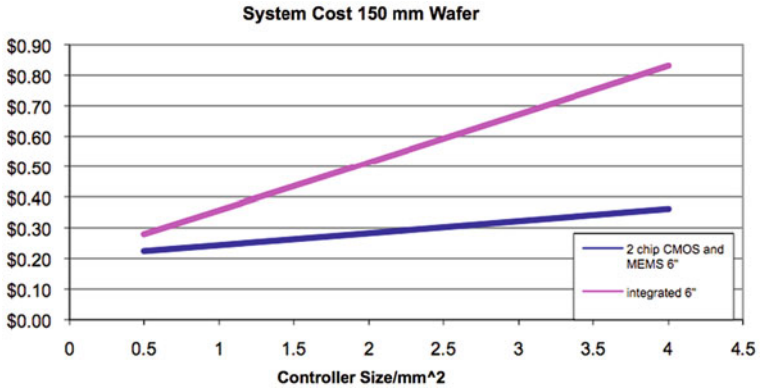


Fig. 14.92 Calculated costs for the two-die system wherein both the CMOS and MEMS substrates are produced using 150 mm diameter wafers, compared to an integrated MEMS process technology produced on a 150 mm diameter wafer. Both system costs are plotted as a function of the CMOS controller die area

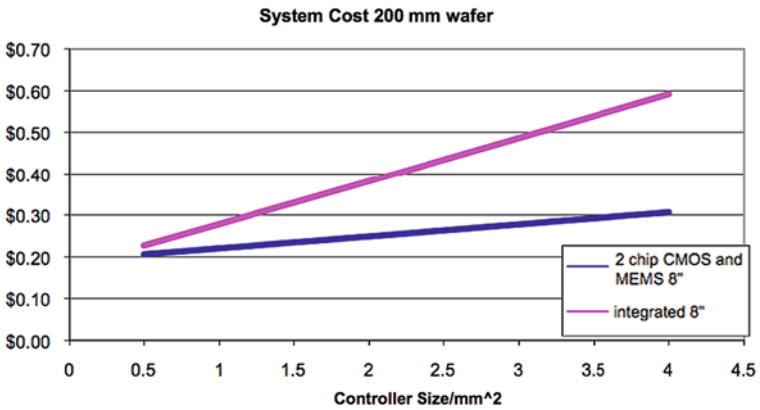


Fig. 14.93 Calculated costs for the two-die system wherein both the CMOS and MEMS substrates are produced using 200 mm diameter wafers, compared to an integrated MEMS process technology produced on a 200 mm diameter wafer. Both system costs are plotted as a function of the CMOS controller die area

14.10 Conclusions

In this chapter we have attempted to provide a concise understanding and appreciation of MEMS process integration. A review of the similarities and differences between MEMS and the related integrated circuit technology was provided, along with some guidance on how MEMS process sequences are successfully developed. We have also reviewed many of the most noteworthy and important MEMS process sequences and technologies that have been developed to date, showing examples

both with and without microelectronics integrated with MEMS. In addition to being a general reference, these wide ranging examples can bolster a designer's experience base for MEMS process integration strategies that were successful. We have provided the general strategy for MEMS cost analysis, and pointed out the complexity of performing such a cost analysis accurately. Unless a MEMS developer has the opportunity to leverage a known, running manufacturing process, there are a very large number of variables that are very difficult to predict, particularly the various yield values. Indeed, it is not uncommon to be off by a factor of two or more in such circumstances. We presented a set of "generic" cases as a cost comparison example. Although the values in this example are meant to be close to "real-world" costs, it is important to understand that these costs are for illustrative purposes only. Calculating MEMS development and manufacturing costs, and hence ROI, is difficult and is often based on less than complete or accurate information. In the end, this analysis is part art, as well as science, and can only be done with the input of MEMS technologists with significant experience.

References

1. S. Bart, M. Chiao, J. Clatterbaugh, M. Collins, J. Custer, J. Harley, L. Lin, J. Lyke, B. Nelson, A. Oliver, J. Tringe, W. Wilson, G. Yang: Packaging for MEMS, T.-R. Hsu (Ed.) (IEE INSPEC, London, 2004)
2. S.F. Bart, H.R. Samuels: Design Techniques for Minimizing Manufacturing Variations in Surface Micromachined Accelerometers, Microelectromechanical Systems, DSC-Vol. 59 ASME WAM, pp. 427–433 (1996)
3. PolyMUMPS Design Handbook, MEMSCap Website
4. R. Ruby: Review and Comparison of Bulk Acoustic Wave FBAR, SMR Technology, Invited Paper, Ultrasonics Symposium (2007)
5. RF Bulk Acoustic Wave Filters for Communications, Ken-ya Hashimoto (Ed.) (Artech House, Norwood, MA, 2009)
6. R. Ruby, R. Parker, D. Feld: Method of Extracting Unloaded Q Applied Across Different Resonator Technologies, Ultrasonics Symposium (2008)
7. Ruby et al.: SBAR Structures and Method of Fabrication of SBAR.FBAR Film Processing Techniques for the Manufacturing of SBAR/BAR Filters, May 9, US Patent #6,060,818 (2000)
8. Larson et al.: Method of Providing Differential Frequency Adjusts in a Thin Film Bulk Acoustic Resonator (FBAR) Filter and Apparatus Embodying the Method, May 20, US Patent #6,566,979 (2003)
9. Sandia web site: http://mems.sandia.gov/ (Accessed in 2010)
10. J.J. Bernstein: A Micromachined Condenser Hydrophone, Solid-State Sensors, Actuators, and Microsystems Workshop, Hilton Head Island, SC, June (2002)
11. S. Calmes, C.H. Cheng, F.L. Degertekin, X.C. Jin, S. Ergun, B.T. Khuri-Yakub: Highly Integrated 2-D Capacitive Micromachined Ultrasonic Transducers, Proceedings of the 1999 IEEE Ultrasonics Symposium, Vol. 2, Oct. 17–20, 1999, pp. 1163–1166 (Tahoe, NV)
12. G.M. Sessler: Silicon microphones, J. Audio Eng. Soc., 44(1/2) (1996).
13. P. Rombach, M. Mullenborn, U. Klein, K. Rasmussen: The First Low Voltage, Low Noise Differential Silicon Microphone, Technology Development and Measurement Results, Technical Digest of the 14th IEEE International Conference on Micro Electro Mechanical Systems, Interlaken, Switzerland, January 21–25, pp. 42–45 (2001)

14. P.V. Loeppert, B.L. Sung: SiSonic – The First Commercialized MEMS Microphone, Solid-State Sensors, Actuators, and Microsystems Workshop, Hilton Head Island, SC, June 4–8, pp. 27–30 (2006)
15. M. Lemkin, T. Juneau, W. Clark, T. Roessig, T. Broshihan: A Low-Noise Digital Accelerometer Using Integrated SOI-MEMS Technology, Technical Digest of the 10th International Conference on Solid-State Sensors and Actuators (Transducers '99), Sendai, pp. 1292–1297 (1999)
16. J.W. Weigold, T.J. Brosnihan, J. Bergeron, X, Zhang: A MEMS Condenser Microphone for Consumer Applications, Technical Digest of the 19th IEEE International Conference on Micro Electro Mechanical Systems, Istanbul, Turkey, Jan. 22–26, pp. 86–89 (2006)
17. R.N. Chandler, W.T. Park, H. Li, G. Yuma, A. Partridge, M. Lutz, T.W. Kenny: Single wafer encapsulation of MEMS devices, IEEE Trans. Adv. Packaging, 26(3), 227 (2003)
18. W.T. Park, R. N. Chandler, H. J. Li, J. Cho, H. Li, T.W. Kenny, A. Partridge, G. Yuma, M. Lutz: Wafer Scale Encapsulation of MEMS Devices, Proceedings of IPACK03, International Electronic Packaging Technical Conference and Exhibition, July 6–11, Maui, Hawaii (2003)
19. SiTime's MEMS First™ Process, SiT-AN20001, Rev. 1.7, 17 February 2009, see http://www.sitime.com/support/documents/AN20001_MEMS_First_Process.pdf (Accessed in 2010)
20. J. Bernstein, S. Cho, A.T. King, A. Kourepenis, P. Maciel, M. Weinberg: A Micromachined Comb-Drive Tuning Fork Rate Gyroscope, Presented at the IEEE Micro Electro Mechanical Systems Conference, Fort Lauderdale, FL, February 7–10, p. 143 (1993)
21. B. Vigna: MEMS Epiphany, MEMS 2009 Conference, Sorrento, Italy, January 26 (2009)
22. Source, iSuppli Corporation, see http://www.isuppli.com (Accessed in 2010)
23. B. De Masi, S. Zerbini, Process builds more sensitive structures, EE Times, November 22 (2004)
24. C.S. Smith, Piezoresistive effect in germanium and silicon, Phys. Rev. 94, 1 (1954)
25. J. Brysek, K. Petersen, J.R. Mallon, L. Christel, F. Pourahmadi: Silicon Sensors and Microstructures (NovaSensor Company Book, Fremont, CA, 1990)
26. S.M. Sze: Semiconductor Sensors (Wiley, New York, NY, 1994)
27. K. Petersen, P. Barth, J. Poydock, J. Brown, J. Mallon, J. Brysek, Silicon Fusion Bonding for Pressure Sensors, IEEE Solid-State Sensor and Actuator Workshop, Hilton Head, South Carolina, June 6–9, p. 144 (1988)
28. L. Spangler, C. Kemp: ISAAC – Integrated Silicon Automotive Accelerometer, The 8th International Conference on Solid-State Sensors and Actuators (Transducers '95), and Eurosensors IX, Sweden, June 25–29, pp. 585–588 (1995)
29. K.A. Shaw, Z. Lisa Zhang, N.C. MacDonald: SCREAM I: a single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures, Sens. Actuators A, 40, 63–70 (1994)
30. F. Ayazi, K. Najafi: High aspect-ratio combined poly and single-crystal silicon (HARPSS) MEMS technology, J. Microelectromech. Syst. 9(3), 288–294 (2000)
31. C. Keller, M. Ferrari: Milli-Scale Polysilicon Structures, Technical Digest, Solid-State Sensor and Actuator Workshop, Hilton Head, SC, June, pp. 133–137 (1994)
32. Miragem Process, http://www.micralyne.com, Micralyne, Edmonton, Alberta, Canadá (Accessed in 2010)
33. aMEMS Process, http://www.mems-exchange.org, MEMS and Nanotechnology Exchange, Reston, VA, USA (Accessed in 2010)
34. SOIMUMPS Process, http://www.memscap.com, MEMSCAP, Research Triangle Park, NC, USA (Accessed in 2010)
35. MEMSOI Process, http://www.tronics.eu, TRONICS Microsystems S.A., France (Accessed in 2010)
36. J.A. Kubby on behalf of the MOEMS Manufacturing Consortium: Hybrid Integration of Light Emitters and Detectors with SOI-Based Micro-opto-electro-mechanical (MOEMS)

Systems, Proc. SPIE 4293, Silicon-Based and Hybrid Optoelectronics III, David J. Robbins, John A. Trezza, Ghassan E. Jabbour, (Eds.), pp. 32–45 (2001)
37. P. Lin, R.M. Boysel, M. Boysel, M. Winters, W. Hawkins, J. Kubby, P. Gulvin, J. Diehl, K. Feinberg, K. German, L. Herko, N. Jia, J. Ma, J. Meyers, P. Nystrom, Y.R. Wang: Multi-user Hybrid Process Platform for MEMS Devices Using Silicon-on-Insulator Wafers, 18th International Conference on Micro Electro Mechanical Systems (MEMS), Miami Beach, FL, USA, pp. 516–519 (2005)
38. S. Hollar, A. Flynn, S. Bergbreiter, K.S.J. Pister: Robot Leg Motion in a Planarized-SOI, 2 Poly Process, Proceedings of the Solid-State Sensor, Actuator & Microsystems Workshop, Hilton Head Island, SC (2002)
39. P. Gulvin, J. Kubby, P. Lin et al.: SOI-Based Optical Add-Drop Multiplexers, Proceedings of the Solid-State Sensor, Actuator & Microsystems Workshop, Hilton Head Island, SC, pp. 356–359 (2004)
40. Silicon-On-Glass Design Handbook, a process module for multi-user service program. Copyright the University of Michigan, March (2007)
41. SOIMUMPS Design Handbook, MEMSCap web site.
42. W.E. Becker, W. Ehrfeld, D. Münchmeyer, H. Belz, A. Heuberger, S. Pongratz, W. Glashauser, J.H. Michel, R. Siemens: Production of separation-nozzle systems for uranium enrichment by a combination of x-ray lithography and galvanoplastics, Naturwissenscahften 69, 520–523 (1982)
43. W.E. Becker, W. Ehrfeld, D. Münchmeyer, P. Hagmann, A. Maner: Fabrication of microstructures with high-aspect ratios and great structural heights by synchrotron radiation lithography, galvanoforming and plastic moulding (LIGA process), Microelectron. Eng. 4, 35–56 (1986)
44. T. Saito, E. Sato, M. Matsuoka, C. Iwakura: Electroless deposition of Ni-B, Co-B and Ni-Co-B alloys using dimethylamineborane as a reducing agent, J. Appl. Electrochem. 28, 559–563 (1998)
45. J. Goettert: The LIGA Process: A Fabrication Process for High-Aspect-Ratio Microstructures in Polymers, Metals, and Ceramics, In S. Soper, W. Wang (Eds.): BioMEMS: Technologies and Applications, pp. 46–94 (CRC Press, Boca Raton, FL, 2006)
46. L. Jian, M.Y. Desta, J. Goettert, Multi-level microstructures and mold inserts fabricated with planar and oblique x-ray lithography of SU-8 negative photoresist, Proc. SPIE, 4557 (2001)
47. R. Turner, Y. Desta, K. Kelly, J. Zhang, E. Geiger, S. Cortez, C. Mancini: Tapered LIGA HARMS, J. Micromech. Microeng. 13, 367–372 (2003)
48. G. Aigeldinger: Implementation of an Ultra Deep X-ray Lithography (UDXRL) System at CAMD, PhD Thesis, Freiburg University (2001)
49. Y. Desta, J. Goettert: X-ray Mask for LIGA Microfabrication, In V. Saile, U. Wallrabe, O. Tabata, J.G. Korvink (Eds.): LIGA and Its Applications, Advanced Micro & Nanosystems, Vol. 7, pp. 11–50 (Wiley-VCH, New York, NY, 2009)
50. M. Kohl, J. Goettert, J. Mohr: Verification of the micromechanical characteristics of electrostatic linear actuators, Proceedings of the 8th International Conference on Solid-State Sensors and Actuators, Stockholm/Sweden, pp. 400–403 (1995)
51. B. Pillans, J. Kleber, C. Goldsmith, M. Eberly: RF Power Handling of Capacitive RF MEMS Devices, IEEE MTT-S, pp. 329–332 (2002)
52. Goldsmith, United States Patent, US #6,608,268
53. MetalMUMPS Design Handbook, MEMSCap web site (Accessed in 2010)
54. J.J. Yao, S. Park, J. DeNatale: High Tuning Ratio MEMS Based Tunable Capacitors for RF Communications Applications, Proceedings of the 1998 Solid State Sensor and Actuator Workshop, Hilton Head, p. 124 (1998)
55. J.J. Yao, S. Park, J. DeNatale: A Low Power Low Voltage Electrostatic Actuator for RF MEMS Applications, Proceedings of the 2000 Solid State Sensor and Actuator Workshop, Hilton Head, p. 246 (2000).

56. R.L. Borwick, P.A. Stupar, J. DeNatale, R. Anderson, C. Tsai, K. Garrett: A High-Q, Large Tuning Range, Tunable Capacitor for RF Applications, IEEE MEMS, p. 669 (2002)
57. R.L. Borwick III, P.A. Stupar, J. DeNatale, R. Anderson, R. Erlandson: Variable MEMS Capacitors Implemented Into RF Filter Systems, IEEE MTT-S Special Issue on RF MEMS, January (2003)
58. C. Tsai, P.A. Stupar, R.L. Borwick III, M. Pai, J. DeNatale, An isolated tunable capacitor with a linear capacitance-voltage behavior, IEEE Transducers, 833 (2003)
59. R.L. Borwick III, P.A. Stupar, J. DeNatale: A hybrid approach to low-voltage MEMS switches, IEEE Transducers 859 (2003)
60. J. DeNatale, R.L. Borwick III, P.A. Stupar, R. Anderson, K. Garrett, W. Morris, J.J. Yao: MEMS High Resolution 4-20 mA Current Sensor for Industrial I/O Applications, IEEE Transducers 1598 (2003)
61. Rockwell Scientific *a*MEMS™ process Design Handbook, MEMS Exchange Website (See http://www.mems-exchange.org/catalog/P3603/)
62. Plastic MEMS (PMEMS) Design Handbook, a process module for multi-user service program. Copyright the University of Michigan, September 2006. (See http://www.mems-exchange.org/catalog/P3714/)
63. D. Sparks, S. Massoud-Ansari, N. Najafi: Chip-level packaging of micromachines using NanoGetters, IEEE Trans. Adv. Packaging 26(3) (2003)
64. D. Sparks, R. Smith, R. Schneider, J. Cripe, S. Massoud-Ansari, A. Chimbayo, N. Najafi: A variable temperature, resonant density sensor made using an improved chip-level package, Sens. Actuators A, 107, 119 (2003)
65. MEMS Exchange process catalog under "Packaging", See https://www.mems-exchange.org/catalog/P3502 (Accessed in 2010)
66. K.H.-L. Chau, S.R. Lewis, Y. Zhao. R.T. Howe, S.F. Bart, R.G. Marcheselli: An integrated force-balanced capacitive accelerometer for low-g applications, Sens. Actuators A, 54, 472–476 (1996)
67. S. Lewis, S. Alie, T. Brosnihan, C. Core, T. Core, R. Howe, J. Geen, D. Hollocher, M. Judy, J. Memishian, K. Nunan, R. Paine, S. Sherman, B. Tsang, B. Wachtmann: iMEMS Inertial Measurement Unit Components, In Technical Digest of the IEEE Electron Devices Meeting, pp. 39.1.1–39.1.4 (Washington DC, 2003).
68. M.R. Douglass: MEMS reliability – coming of age, Proc. SPIE 6884, 688402 (2008)
69. Wicht Technologie Consulting, "MEMS 30" Top 30 MEMS manufacturers in 2006 by revenue, www.wtc-consult.de
70. L.J. Hornbeck: From cathode rays to digital micromirrors: A history of electronic projection display technology, Texas Instrum. Techn. J. 15(3), 7–46 (1998). Also at http://www.dlp.com
71. J. Grimmett, J. Huffman: Advancements in DLP® Technology – the New 10.8 μm Pixel and Beyond, IDW/AD'05, Proceedings of the 12th International Display Workshops (in conjunction with Asia Display 2005), Vol. 2, pp. 1879–1882 (2005)
72. L.J. Hornbeck: Combining Digital Optical MEMS, CMOS, and Algorithms for Unique Display Solutions, IEEE International Electron Devices Meeting Technical Digest, Plenary Session, pp. 17–24 (2007)
73. G. Bitko, A. McNeil, R. Frank: Improving the MEMS pressure sensor, Sens. Mag 17(7) (2000)
74. Information provided by Andrew McNeil of Freescale Semiconductor, August (2009)
75. S.F. Pond: Inkjet Technology and Product Development Strategies (Torrey Pines Research, 2000)
76. W.G. Hawkins, D.J. Drake, M.R. Campanelli: U.S. Patent 4,601,477 (1986), Re.32572 (1988)
77. Hewlett-Packard Journal: 39(5), 51–98 (1988)
78. E. Peeters, S. Vandebroek: Thermal ink jet technology, Circuits Dev. 13(4), 9–23 (1997)
79. W. Hawkins et al: A fully integrated silicon-based 40-V TIJ IC, J. Microelectron. Eng. 9, 165–170 (1992)

80. W. Hawkins, C. Burke, T. Watrobski, T. Tellier, S. Vandebroek, P. Chow: Power MOSFET design for a 40-V 192-element thermal-Ink-Jet IC, J. Trans. Electron Devices, 2674 (1992)
81. E. Peeters: Challenges in commercializing MEMS, IEEE Comput. Sci. Eng. 44–48 (1997)
82. R. Nayve, M. Fujii et al.: High-resolution long-array thermal ink jet printhead fabricated by anisotropic wet etching and deep Si., J. Microelectromech. Syst. 13(5) (2004)
83. M. O'Horo, J. O'Neill, E. Peeters, S. Vandebroek: Micromachining technology for thermal inkjet application, Proc. Sensor Expo 275–279 (1997)
84. R.A. Wood: Monolithic Silicon Microbolometer Arrays, Chapter 3, in Uncooled Infrared Imaging Arrays and Systems, Semiconductors and Semimetals, Vol. 47 (P.W. Kruse, D.S. Skatrud (Eds.) Academic, New York, NY, 1997)
85. P.W. Kruse: Uncooled Thermal Imaging: Arrays, Systems, and Applications, (SPIE Press, 2002)
86. B.E. Cole, R.E. Higashi, R.A. Wood: Monolithic two-dimensional arrays of micromachined microstructures for infrared applications, Invited Paper, Proc. IEEE 86(8), 1679 (1998)
87. Application Specific Integrated MEMS Exchange (ASIM-X) Design Handbook, a process module for multi-user service program, Version 2. Copyright Carnegie Mellon University, April (2006)
88. P.J. Gilgunn, G.K. Fedder: Flip-Chip Integrated SOI-CMOS-MEMS Fabrication Technology, In Technical Digest of the Solid-State Sensor, Actuator and Microsystems Workshop, Hilton Head Island, South Carolina, June 1–5, pp. 10–13 (2008).
89. C. Goldsmith et al.: Characteristics of Micromachined Switches at Microwave Frequencies, 1996 MTT-S Digest, pp. 1141–1144 (1996)
90. A. Dec et al.: Micromachined electro-mechanically tunable capacitors and their applications to RF ICs, IEEE Trans. Microwave Theory Techn. 46(12) (1998)
91. F. Lihui et al.: High Q multiplayer spiral inductor on silicon chip for 5-6 GHz, IEEE Electron Device Lett. 23(8), 470–472 (2002)
92. G.-L. Tan, G. Rebeiz: A DC-contact MEMS shunt switch, IEEE Microwave Wireless Compon. Lett. 12(6), 212–214 (2002)
93. S. Cunningham, A. Morris, D. Dereus, G. Schropfer: High-Performance Integrated RF MEMS: Part 1 – The Process, In Proceedings of the 2003 European Microwave Symposium (EuMW2003) (2003)
94. A. Franke et al.: Polysilicon silicon germanium films for integrated microsystems, J. Microelectromech. Syst. 12(2), 160–171 (2003)
95. R.T. Howe, T.J. King: Poly-SiGe MEMS for Modular Post-CMOS Integrated Microsystems, June 29, 2004. See http://www-bsac.eecs.berkeley.edu/scripts/show_pdf_publication.php?pdfID=1089668703 (Accessed in 2010)
96. B.C.Y. Lin, T.-J. King, R.T. Howe: Optimization of poly-SiGe deposition processes for modular MEMS integration, Micro- and Nanosystems Symposium, December 1–3, Boston, MA, pp. 43–48 (2003)
97. J. Smith et al.: Embedded Micromachined Devices for the Monolithic Integration of MEMS with CMOS, Technical Digest of the IEDM, p. 609 (1995)
98. MEMS and Nanotechnology Exchange, http://www.mems-exchange.org/ (Accessed in 2010)
99. IC Knowledge LLC, http://www.icknowledge.com/ (Accessed in 2010)
100. R.B. Seeds: Yield and Cost Analysis of Bipolar LSI, Proc. IEEE, Int. Electron Devices Meeting, Paper 1.1, October (1967)
101. B.T. Murphy: Cost-size optima of monolithic integrated circuits, Proc. IEEE, 52, 1537–1545 (1964)

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