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Heimo Uhrmann
Robert Kolm
Horst Zimmermann

Analog Filters in Nanometer CMOS

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Heimo Uhrmann • Robert Kolm •
Horst Zimmermann

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Heimo Uhrmann
EMCE
Vienna University of Technology
Vienna, Austria

Horst Zimmermann
EMCE
Vienna University of Technology
Vienna, Austria

Robert Kolm
EMCE
Vienna University of Technology
Vienna, Austria

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Preface

This book describes circuit engineering efforts for modern mobile communication. Electronic circuits for latest mass applications like mobile phones and smart phones are realized as so-called systems on chip (SoC). Such SoCs are realized in nanometer CMOS technology and contain a lot of digital circuits for digital signal processing but they also contain analog circuits which often form the key devices for a good over-all performance. The importance of analog filters nowadays is often underestimated. They are, however, still necessary to obtain high-performance wireless receivers and transmitters.

In fact, progress in CMOS technology and circuit design allows the revolution in modern mobile communication. Every ten years, a new mobile phone generation is introduced. Recently, LTE (Long Term Evolution) was started by telecom companies to form the 4th generation of mobile phones. Up to 100 Mbit/s are possible with LTE for downloads, which is a much higher data rate than with HSPA+.

In the 1990s, GSM allowed mobile phone calls and SMS. Around the year 2000, the mobile phones became capable of using the internet although requiring a lot of patience. Today, mobile internet on the smart phone and via data sticks is part of the daily life. Currently a smart phone boom happens. Mobile broadband access is expected to grow by a factor of more than 20 until 2015. This will involve data rates that cannot be handled by UMTS and HSPA+. The current answer to this challenge is LTE as a standard for mobile communication. In practice, faster transmission of electronic mails with large attachments, fast downloads of music (one song in 2 seconds) and HD videos (in less than 30 minutes), web-video conferences, and online gaming (with response times below 20 ms) will become possible.

To make all this possible for a mass market, analog circuit design in nanometer CMOS technology is a very important key factor. This book concentrates on one sub-topic of analog circuit design, i.e. on analog filters. Starting from the basics of analog filters and the poor transistor characteristics in nanometer CMOS, 10 high-performance analog filters developed by the authors in 120 nm and 65 nm CMOS are described extensively. Among them are g_m-C filters, current-mode filters, and active filters for system-on-chip realization for Bluetooth, WCDMA, UWB, DVB-H, and LTE applications. For the active filters several operational amplifier designs are de-

scribed. The book, furthermore, contains a review of the newest state of research on low-voltage low-power analog filters. To cover the topic of the book comprehensively, linearization issues and measurement methods for the characterization of advanced analog filters are introduced in addition.

This book introduces newest results of development of analog filters in nanometer CMOS and describes methods how to deal successfully with the nanometer hell of physics. Numerous detailed circuit diagrams and plots of measured results allow a fast comprehension.

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Vienna, Austria

Heimo Uhrmann
Robert Kolm
Horst Zimmermann

Contents

Nomenclature

C_L	Load capacitance
C_{OX}	Gate oxide capacitance
CMFB	Common-mode feedback
CMRR	Common-mode rejection ratio
dBc	Decibels relative to the carrier
DR	Dynamic range
DVB-H	Digital video broadcast—handheld
DVB-T	Digital video broadcast—terrestrial
f_c	-3 dB cut-off frequency
f_T	Transit frequency
FOM	Figure of merit
g_{DS}	Output conductance
g_m	Transconductance
GBW	Gain-bandwidth product
HD3	3rd-order harmonic distortions
I_{dsat}	Saturation current
IIP3	Input third-order intercept point
IM3	3rd-order intermodulations
IP3	3rd-order intercept point
L	Gate length
LP	Low-power
N	Filter order
NF	Noise figure
OFDM	Orthogonal frequency division multiplex
OIP3	Output third-order intercept point
opamp	Operational amplifier
P	Power consumption
PM	Phase margin
PSRR	Power supply rejection ratio
Q	Quality factor
rms	Root mean square

SDR	Software defined radio
SF	Scaling factor
SNR	Signal-to-noise ratio
SoC	System on Chip
STI	Shallow trench isolation
t_{OX}	Oxide thickness
THD	Total harmonic distortions
TV	Television
U_{DS}	Drain-source voltage
U_{GD}	Gate-drain voltage
U_{GS}	Gate-source voltage
UMTS	Universal mobile telecommunication system
V_{TH}	Threshold voltage
W	Channel width
WCDMA	Wideband Code Division Multiple Access

Chapter 1
Introduction

Analog circuits are still necessary and have a right to exist in a society that is shaped by the digital revolution. The digital advance is driven by various trends of market and economy [12]. High-performance multimedia systems allow a colorful and high-resolution presentation of digital contents while simultaneously navigating and interacting with this medium. In telecommunication and high-speed communication systems the data volume and speed is rising rapidly while the receiving terminals have to process the incoming data stream in time. Computer systems become faster in terms of higher clock speed and contain a huge amount of data storage in order to provide enough performance, which is necessary to execute the growing number of resource intensive applications in a convenient time.

These few examples give an impression on the progress in digital CMOS design. The development of low-power CMOS technologies is mainly forced by power dissipation, manufacturing costs, and speed performance [38]. During the last decades these requirements are mostly obtained by the technological progress of scaling of the device feature sizes to the nanometer domain. Scaling has a significant impact on the density of digital circuits [33]. A larger number of transistors per chip area increases the functionality and lowers the fabrication costs. Another benefit of shrinking structure sizes is the reduction of the parasitic transistor capacitances. Smaller parasitic capacitances cause thus lower dynamic power dissipation in digital logic. The shortest available channel length ensures the maximum speed [103]. However scaling induces undesirable and challenging effects as well [134]. Short-channel MOSFET transistors suffer from the so-called short-channel effects. These are, among other things, velocity saturation, hot electrons, and impact ionization. The breakdown of the transistors is another issue. The scaling of the minimum feature sizes requires the lowering of the supply voltage due to the rising electric fields inside the transistor. A high electric field, which is inversely proportional to the distance, can destroy the transistor. The lowering of the supply voltage has a power saving effect in digital logic. Power saving in digital applications provokes lower costs for cooling and longer battery life-time for handheld devices. Summarizing, the ongoing downscaling of digital CMOS technology pushes the development stimulus in economy and science.

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Unfortunately, the world where digital systems operate has an analog manner and, thus, interfaces between analog and digital blocks have to be created. An interfacing block may be an analog-digital or a digital-analog converter, an amplifier, an I/O buffer, an analog filter, a mixer, or a radio frequency (rf) front-end for a communication channel. From an economical point of view it is favorable for high-volume applications to integrate all analog and digital system blocks into a mixed-signal system on one chip. Although the analog part is not the essential core of such a mixed-signal system, it has a great impact on the overall system performance. The process of scaling affects the performance of the MOS transistors in analog circuitry severely [36]. Therefore, analog system design in digital CMOS is an important and difficult task. One of the major challenges is the low supply voltage, which is limiting the maximum signal swing. The increasing 1/f noise at small structure sizes increases this challenge. Errors due to device mismatch are inversely proportional to the device sizes as well [9]. Additional gate leakage due to reduced gate oxide thickness has a considerable magnitude [4]. The downscaling of CMOS transistors also has some advantages for analog circuits, of course [47]. For example, the transit frequency of the transistors is rising due to the smaller parasitic capacitances, similar to rising clock frequencies of digital logic.

For the purpose of a power and cost saving device, system on chip solutions are desirable. In this work analog continuous-time filters for radio frequency front-ends are presented as an element in a system on chip. Analog continuous-time filters are sometimes preferable in contrast to switched-capacitor filters or digital filters because of the possibility for high-frequency operation and low power dissipation [120]. Many passive discrete-component filter structures are known, which use the inductor as an important element [121]. Integrated inductors offer only small inductance values and are difficult to realize due to the bad quality factor and large chip area. Inductors can be substituted by the use of active analog continuous-time filters, which use an active element, resistors, and capacitors. Active elements may be operational amplifiers or transconductance amplifiers. Integrated analog filter design in nanometer CMOS faces many technological restrictions, for example the limited dynamic range and matching [11]. The limited signal swing, caused by the low supply voltage and the constant noise level, decreases the dynamic range of analog filters at a constant current consumption. Additionally varying device parameters due to mismatch cause a non-constant frequency response. The use of an active tuning system may correct those errors.

This book considers above mentioned issues and is structured as follows. Chapter 2 classifies filters, describes analog filter types and deals with filter approximations. The nanometer CMOS technologies used for the fabrication of the filters presented in this book are described in Chap. 3. Chapter 4 summarizes operational transconductance amplifiers. Chapter 5 describes g_m-C filters for ultra-wide-band applications and compares the results of the implemented ones with the state-of-the-art in literature. The description of realized current-mode filters for software defined radio applications and the comparison of their results with the state-of-the-art follows in Chap. 6. Chapter 7 presents operational amplifier filters for handheld digital video broadcast and LTE applications.

Chapter 2
Analog Filters

'Filter' is a general term. It is used to separate desired parts from unwanted parts of an original set. In an electrical point of view filters have a variety of duties. Filters are used to cut a particular range of the frequency spectrum of an electrical quantity out of the overall frequency spectrum to retrieve the interesting information out of the plenty of information channels and noise. They can be used as equalizers or matched filters in transmission channels in order to compensate distortions caused by the transmission channel itself. Filters can also be employed for smoothing purposes at the output of digital-to-analog converters [66]. This chapter deals with the characterization of filters, it gives an overview of some analog filters and describes the Butterworth-filter approach in more detail.

2.1 Filter Classification

Due to the diversity of filters many classifications of electronic filters are possible. Some are described in a short overview [24].

2.1.1 Analog and Digital Filters

Electronic filters are distinguished in analog and digital filters. Analog filters have a long tradition in analog circuit design and communication systems and can be grouped in electric and electronic filters, sampled-data filters, and electromechanic filters. Electric and electronic filters are realized by using resistors (R), capacitors (C), inductors (L), and active elements like operational amplifiers or g_m-cells. Analog filters process analog continuous-time input signals in real-time and transform it according to the filter transfer function. Examples for analog electric/electronic continuous-time filters are LCR-filters, g_m-C filters, or operational amplifier-RC filters.

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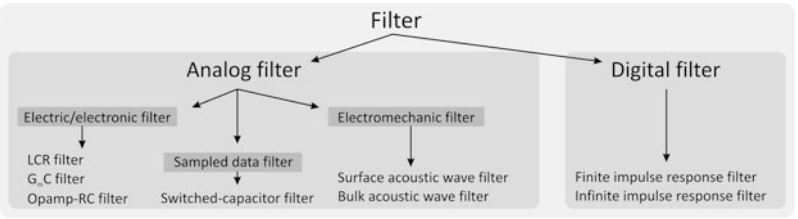


Fig. 2.1 Classification of filters—overview

Sampled-data filters sample the input signal by using a Sample-and-Hold stage on the input before processing the signal. The input signal is quantized at discrete time steps but the signal remains analog. Because of the sampling of the input signal these filters are discontinuous in time. However, sampled data filters belong to the group of analog filters. The switched-capacitor filter is a well known member of the sampled data filters.

Electromechanic filters convert the electrical signal into a mechanical (acoustic) wave which propagates over a ceramic or a crystal and then finally convert it back to the electrical domain. The combination of two electro-acoustic transformers and the signal delay on the crystal perform the filtering operation. Well known representatives of electromechanic filters are surface acoustic wave filters (SAW filter) or bulk acoustic wave filters (BAW filter).

Digital filters emerged since the development of computers and grew rapidly. Digital filters can be realized in hardware or software. They are characterized by sampled, time discrete input- and output signals. Sampled and time-discrete signals represent periodical series of discrete pulses, which represent the signal waveform. The sampled discrete pulses are discrete values due to the finite resolution of the digital number representation. Examples for digital filters are the finite impulse response filter (FIR filter) and infinite impulse response filter (IIR filter). Figure 2.1 shows an overview of the filter classification scheme.

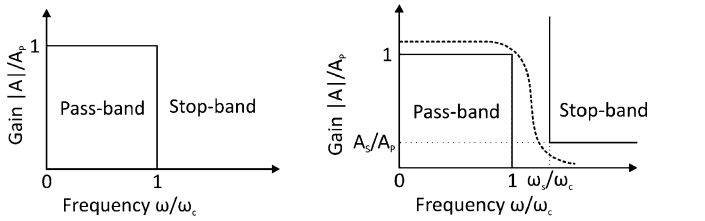
2.1.2 Active and Passive Filters

A passive filter is defined formally in the following way:

> A filter is passive, if the total energy supplied to the filter is nonnegative at any instant of time.

All other filters than passive filters are active filters.

A more common characterization of a passive filter is defined regarding the used elements. A filter is classified as passive, if only passive elements are applied. The basic passive elements are resistors (R), capacitors (C), and inductors (L). If any other active elements are used, such as transistors or amplifiers, a filter is an active filter.



(a) Ideal low-pass filter (b) Specification of a real low-pass filter

Fig. 2.2 Amplitude-frequency response of a low-pass filter

2.1.3 Lumped and Distributed Filters

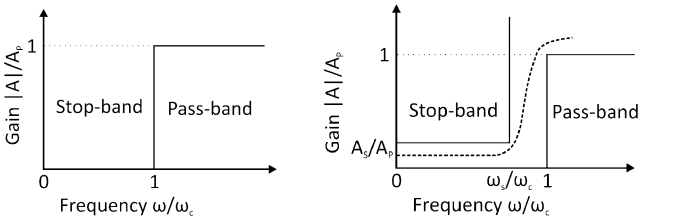
Lumped filters or lumped networks are circuits whose elements (e.g.: R, C, L) are concentrated within their physical devices. The electrical and physical properties of the devices are defined at their terminals and the component connections are small compared to the wavelength of the highest signal frequencies, which are applied to the filter. Distributed filters are networks where the physical dimensions of the elements are in the same range of the signal wavelengths.

2.2 Analog Filter Types

Filters divide the frequency spectrum in different bands and, hence, shape the transfer characteristic of the filter. Stop-bands denominate frequency ranges which block accordant signal fractions from the signal applied at the input. In contrast to this, pass-bands are frequency ranges, which forward the in-band residing input signal frequency fractions to the output. The allocation of the stop-bands and pass-bands specifies the type of the filter. Feasible filter types are the low-pass filter, the high-pass filter, the band-pass filter, the band-stop filter, the all-pass filter and, or the equalization filter [5].

2.2.1 Low-Pass Filter

An ideal low-pass filter exhibits a pass-band from dc, i.e. 0 $\frac{\text{rad}}{\text{s}}$, to the cut-off frequency ω_c whereas the signal is amplified by a gain of A_P. The stop-band starts directly at ω_c and reaches up to infinity with a signal gain of zero. Figure 2.2(a) shows an ideal low-pass filter. In reality filter transfer functions can only approximate the ideal filter transfer characteristics. Figure 2.2(b) shows a general low-pass specification including an example of a filter transfer function (dashed line). The pass-band reaches from dc to the cut-off frequency ω_c with a gain of A_p. In reality filters are not able to switch between pass-band and stop-band abruptly and,



(a) Ideal high-pass filter (b) Specification of a real high-pass filter

Fig. 2.3 Amplitude-frequency response of a high-pass filter

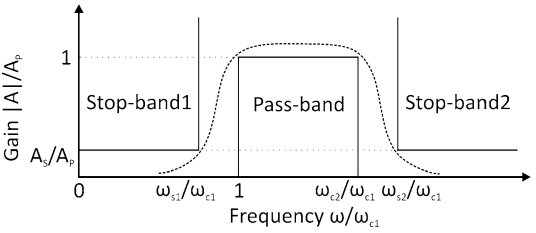


Fig. 2.4 Specification of a band-pass filter

hence, the stop-band starts at $\omega_s > \omega_c$ at a gain of A_s. The span from ω_c to ω_s is called transmission-band. The width of the transmission-band ω_s–ω_c indicates the selectivity of the filter.

2.2.2 High-Pass Filter

An ideal high-pass filter is depicted in Fig. 2.3(a). All signal frequencies in the stop-band are blocked. The stop-band ranges from dc to the cut-off frequency ω_c. All frequencies greater than ω_c pass the filter at a gain of A_p. A specification of a feasible high-pass filter in reality is shown in Fig. 2.3(b). The stop-band extends from zero to ω_s, the pass-band from ω_c to infinity and the transition-band is located between ω_s and ω_c.

2.2.3 Band-Pass Filter

A band-pass filter, as depicted in Fig. 2.4, forwards a specified bundle of wavelengths from ω_{c1} to ω_{c2} having a gain of A_P. The two stop-bands *Stop-band1* and *Stop-band2* cover frequencies from zero to ω_{s1} and ω_{s2} to infinity, respectively. The gain of the two stop-bands is denoted by A_s. An exemplary frequency response is plotted in Fig. 2.4 (dashed line).

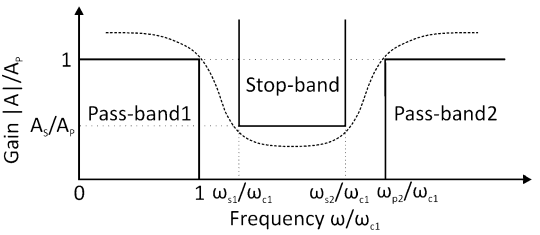


Fig. 2.5 Specification of a band-stop filter

2.2.4 Band-Stop Filter

In contrast to the band-pass filter, a band-stop filter or notch filter eliminates a frequency band from ω_{s1} to ω_{s2}. The rejected band resides between the two pass-bands *Pass-band1* and *Pass-band2*, which are located between zero and ω_{s1} and ω_{s2} and infinity, respectively. Figure 2.5 depicts an example of a band-stop filter specification, A_s and A_p are the corresponding gains for the stop-band and the pass-bands.

2.2.5 All-Pass Filter

All-pass filters forward all wavelengths from zero to infinity equally without any amplitude attenuation. The characteristic filter property concerns the phase response. The propagation delay of the signal depends on the frequency. All-pass filters are mainly used for phase error correction of transmission channels.

2.2.6 Equalization Filter

Equalization filters or equalizers are used for the correction of an uneven frequency response characteristic for smoothing purposes of signals or systems. The transfer function is different from the above considered and is often only usable for one special case of distorted signal.

2.3 Filter Approximation

A physical realization of an ideal filter transfer function is impossible. Hence, a frequency scheme is given, which is dependent on many system parameters and trade-offs. Within this frequency scheme the real filter transfer function has to be located. Important selection criteria are for example a fast transmission from the pass-band to the stop-band or a minimum of filter distortion. The closer the ideal filter transfer function is approximated, the greater is the effort regarding number of

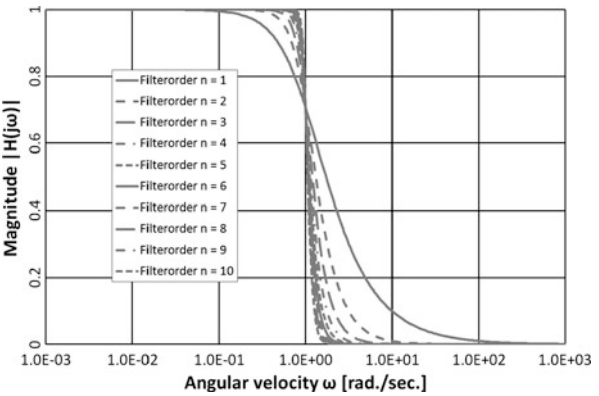


Fig. 2.6 Magnitude functions of normalized Butterworth low-pass filters of first-order to 10th-order

elements, power consumption or costs. Depending on the latitudes various approximations for the ideal filter transfer functions are realizable. Important and popular approximation functions are Butterworth approximations, which are explained in more detail, Chebyshev and inverse Chebyshev approximations, elliptic or Cauer approximations, and Bessel approximations.

2.3.1 Butterworth Filter

The Butterworth filter was first described by Stephen Butterworth and is nowadays popular and often used. The Butterworth filter approximation is demonstrated on the normalized low-pass Butterworth filter. High-pass, band-pass, and band-stop filters can be realized by using the appropriate transformation [66].

The normalized Butterworth function of Nth-order is given by

$$\left|H(j\omega)\right|^2 = \frac{1}{1+\omega^{2N}} \tag{2.1}$$

In (2.1) ω denotes the angular velocity and $N = 1, 2, \ldots$ the filter-order. The magnitude response $|H(j\omega)|$ of a first-order to a 10th-order normalized Butterworth low-pass is visualized in Fig. 2.6. A rising filter order ($N \to \infty$) results in a better approximation to the ideal low-pass filter (see Fig. 2.2(a)). The pass-band and the stop-band coincide longer with the ideal transfer function, simultaneously the transition-band becomes narrower. To comply with the filter specifications an appropriate filter-order N of the Butterworth low-pass filter is necessary.

The Butterworth low-pass filter has some important characteristics:

- The magnitude function of a Butterworth low-pass filter is monotonically decreasing for $\omega > 0$ and the maximum of $|H(j\omega)|$ is at $\omega = 0$.

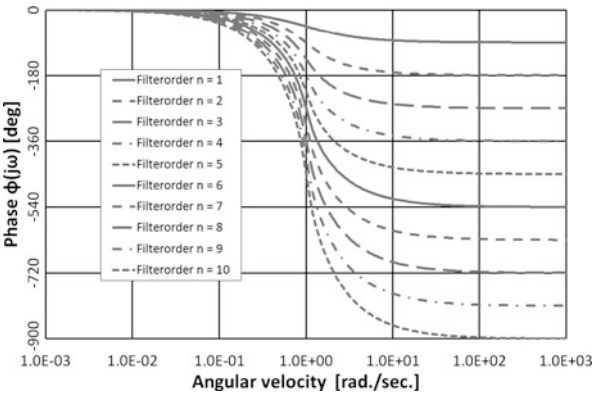


Fig. 2.7 Phase characteristics of normalized Butterworth low-pass filters of first-order to 10th-order

- A Nth-order Butterworth low-pass filter has a maximally flat magnitude function. The maximal flatness of a Butterworth low-pass filter is defined by

$$\frac{d^{(k)}|H(j\omega)|}{d\omega} = 0\Big|_{\omega=0} \quad \forall k = 1 \ldots 2n-1 \tag{2.2}$$

  The first $2n-1$ derivations of $|H(j\omega)|$ of an Nth-order Butterworth filter at $\omega = 0$ are equal to zero.
- A Butterworth filter shows an overshoot in the step response in the time domain, which worsens at rising filter-order N.

The phase characteristics of a Butterworth low-pass filter is given by

$$\Phi(\omega) = \arg\big[H(j\omega)\big] \tag{2.3}$$

Each pole adds $-90°$ phase lag. The phase responses of Butterworth low-pass filters from the order $N = 1$ to 10 is depicted in Fig. 2.7.

The distribution of the poles and zeros in the s-plane are characteristic for filters and can also be used for filter identification. A normalized Butterworth low-pass filter has its poles in the left half plane on the circumference of the unity circle with the center in the point of origin of the s-plane. The poles are spread equidistant over the half circle in the left half s-plane. The location of the poles s_k of $H(s)$ in the left half plane can be calculated by

$$\begin{aligned} s_k &= \sigma_k + j\omega_k = e^{j\frac{(2k+N-1)\pi}{2N}} \\ &= \cos\left(\frac{2k+N-1}{2N}\pi\right) + j\sin\left(\frac{2k+N-1}{2N}\pi\right), \quad k = 1 \ldots N \end{aligned} \tag{2.4}$$

In (2.4) N is the filter order of the Butterworth filter and k is the number of poles. In case of an even filter order no real pole is existent, an odd filter order has exactly one real pole.

2.3.2 Chebyshev or Equiripple Filters

Chebyshev filters offer a frequency response that approximates the ideal low-pass filter more precisely than a Butterworth filter. The transfer function has only poles and lack of any finite zeros. The pass-band of a Chebyshev filter exhibits a pass-band ripple, which ranges between two constant values. The ripple amplitude can be adjusted freely. The ripple amplitude is direct proportional to the filter slope in the transition-band (filter selectivity) and the overshoot of the step response in the time domain. The greater the pass-band ripple, the higher the filter selectivity and the overshoot. The number of ripples depends on the order N of the filter. For frequencies greater than the cut-off frequency the filter has a monotonically decreasing magnitude function similar to Butterworth filters.

2.3.3 Inverse Chebyshev Filter

The inverse Chebyshev filter has complementary properties of the Chebyshev filter concerning the magnitude response. In the pass-band the magnitude function is monotonically decreasing for $\omega > 0$ and the equiripple appears in the stop-band. The filter selectivity is not so high as in Chebyshev filters. The zeros in the filter transfer function bring an additional realization effort.

2.3.4 Elliptic or Cauer Filter

Elliptic filters have an equal ripple in the pass- and in the stop-band. Therefore elliptic filter is also called double Chebyshev filter. The two ripples are individually adjustable. The transition between pass-band and stop-band show a high filter selectivity. The sharp filter edge is realized by a transfer function using a balanced combination of poles and zeros. The magnitude function of an elliptic filter is the best approximation of the ideal low-pass filter compared to Butterworth and Chebyshev filters.

2.3.5 Bessel Filter

In contrast to Butterworth or Chebyshev filters, which approximate the magnitude function of an ideal low-pass filter, the Bessel filter approximates the phase response. Hence, the Bessel filter is also called maximally flat group delay filter. In the pass-band the Bessel filter has a distortion free transmission and keeps the group delay constant. The constant group delay in the pass-band results in a step response,

which shows no overshoot. The filter selectivity is not as good as in Butterworth filter structures. The filter order N is the only parameter to adjust a normalized Bessel filter. The value of N defines the phase and the magnitude response. The higher the filter order, the larger the frequency range with constant group delay and the higher the filter selectivity.

Chapter 3
CMOS Technology

The complementary metal oxide semiconductor technology, where the semiconductor is silicon, is the most rapidly developing high-tech fabrication technique. Products like mobile phones would not be affordable and their volume and weight would not be as small without modern CMOS processes. Modern deep-submicron and nanometer CMOS, however, is somewhat different to CMOS described in many textbooks. Full-custom design of analog circuits, which is essential for high-volume systems on chip as e.g. for mobile phones and smart phones, needs detailed knowledge of the CMOS process, of the devices being available in this process, and of the parasitics. In this chapter, the difficulties of scaling, the 120 nm CMOS, and the 65 nm low-power CMOS process used for the fabrication of the circuits introduced in this book will be described.

3.1 System on Chip (SoC)

Over the last decades electronic devices arose everywhere in our society. These devices combine many standards, applications, and features and are met in low-cost high-volume markets very often. Portability is of particular importance as well. Hence there is the need to develop small-sized, energy saving, and competitive systems in order to improve the sales volume.

System on Chip (SoC) is a strategy which combines all parts that are relevant for the system operation on one chip. Hardly any other parts are necessary for a correct system functionality. A SoC is an overall system with a high level of integration, but it cannot be seen as a simple composition of existing digital, analog, and mixed-signal circuit components. The integration into a SoC implicates innovative approaches in order to find a system design tradeoff, which concerns cost-efficiency, dimensions, and power consumption [95].

A major cost impact is the used process technology [26]. A system on chip design always aims to use the process technology, which results in the cheapest chips. Currently this is deep-sub-micron and nanometer CMOS technology. Moreover the

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digital part of a SoC is the major part, analog circuits have a small but important supporting role. Several interfaces of the SoC have an analog manner, such as input/output ports, analog-to-digital converters, digital-to-analog converters, and radio frequency (rf) front-ends. Although additional process steps for improvements in analog circuit design are available, these process steps are expensive and hence penalize the overall product. In SoC designs standard digital CMOS is commonly used to keep the chip prices low.

3.1.1 Scaling in Digital CMOS Technology—A Retrospection

The CMOS technology underlies a persistent evolution to smaller structure sizes, which is also called scaling. Historically, the common practice of scaling is known as constant field scaling [33]. This strategy keeps the electrical field in the channel of the MOSFET constant while simultaneously reducing the physical dimensions. The channel length L, channel width W, and oxide thickness t_{OX} are reduced by the scaling factor SF. This results in a MOSFET area divided by SF^2 and the parasitic capacitances are divided by SF. The supply voltage and the threshold voltage are graduated by the factor SF to keep the constraint of a constant electrical field. The channel doping is increased by SF. This scaling technique is efficient for improving performance and reducing chip area. Nevertheless technology scaling brings some difficulties.

Scaling Supply and Threshold Voltages The dynamic power consumption in digital circuits is caused by currents during the switching operations and by charging of the load capacitances. Hence, the dynamic power consumption is depending on the supply voltage, since a low supply voltage allows a saving in dynamic power consumption [12]. At constant field scaling the lowering of the supply voltage involves the reduction of the threshold voltage. A low threshold voltage raises the static power consumption, when the transistor is turned off due to leakage currents. The threshold voltage level is adjusted by taking care of the maximal acceptable level of the off-state power consumption.

Gate Oxide Thickness A small gate oxide thickness enhances the transistor performance and in constant field scaling the thickness is also reduced according to SF. However in deep-sub-µm CMOS, the thickness of the gate oxides is only a few atom layers where quantum-mechanical effects have to be considered [41]. The gate leakage currents raise exponentially at decreasing t_{OX} and the tunneling currents can cause a damage of the gate oxide.

Short Channel Transistors Short channels are desirable for fast transistor switching operations, due to the shorter transport time of the charge carriers from source to drain. However, there are some disadvantages:

- High sub-threshold currents occur in off-state transistors. Even at $U_{GS} < V_{TH}$ a current is flowing from source to drain. The currents are generated by punch-through and drain induced barrier lowering (DIBL) [41].
- Surface scattering causes a reduction of the mobility of the electrons [43].
- The velocity saturation lowers the mobility of the carriers of transistors in saturation [89].
- High electric fields in the pinch-off region cause the generation of electron-hole pairs due to impact ionization. The electrons migrate to the drain, the holes move to the substrate in the form of a parasitic substrate current. The body potential is raised and the threshold voltage is lowered due to the body effect again causing a rising of the channel current [138].
- Hot electrons appear at the existence of high electric fields. High energy electrons migrate into the gate oxide and charge the gate oxide and degrade transistor performance and lifetime [85].

Channel Doping The short channel effects can be extenuated by increasing the channel doping, which causes other influences on transistor properties. Important factors are the slower carrier mobility and band-to-band tunneling [41].

3.1.2 Scaling in Digital CMOS Technology—Today

The scaling strategy in deep-submicron and nanometer technologies is different to constant field scaling due to many limitations and parasitic effects. The improvement of the transistor performance relies basically on the gate-length, the gate-oxide thickness, and the source-drain junction scaling [14]. Scaling of these parameters are mainly driven by power optimization, performance maximization, and device reliability.

Power Optimization Reducing the power supply voltage is an effective method to reduce the power dissipation, because subthreshold currents and gate leakage are dependent on the supply voltage [14]. However, there is a limit of scaling the supply voltage, which is the threshold voltage (V_{TH}) of the transistors. A low V_{TH} leads to increasing subthreshold currents and increases the static power dissipation. In order to limit the overall power consumption the threshold voltage is not scaled by SF, it remains larger. For transistor speed issues a sufficient gate overdrive voltage should exist. Therefore the supply voltage is not scaled by SF. For power and performance optimization multi threshold voltage transistors are used. According to the requirements, thin, regular, or thick gate oxide transistors are available, at the drawback of needing additional masks for chip processing. The threshold voltage depends on the operating temperature as well. The power dissipation and the thermal emission are of great interest because of the temperature dependent threshold voltage and the raising number of transistors per chip. Counteractions are cooling, dynamic frequency scaling, voltage-island design technique or adaption of the threshold voltage by the back-gate bias [53].

Performance Maximization The progress in transistor speed has slowed down during the downscaling of CMOS technology. Main reasons are the short-channel effects and some parasitic elements, which do not scale. In digital circuits the performance increases by lowering the capacitance and increasing the transistor saturation currents. At first the saturation current was increased by scaling the oxide thickness and the threshold voltage. As this was not possible anymore due to leakage currents (tunneling effect), the saturation current was increased by strained silicon techniques, channel oriented design, or silicon on insulator. This improves the performance of the MOSFET without scaling the gate oxide thickness [116]. High-k dielectric gates with metal gates may resume the scaling of the gate insulator thickness. Another important factor for transistor speed is the capacitance. Scaling reduces the gate capacitance and the overlap capacitance. However, the gate-to-contact capacitance and the fringing capacitance, which do not scale, will have a major impact on the total capacitance [14].

Device Reliability Scaling, in particular scaling of the gate dielectric, affects the reliability of the transistors. Important reliability stress effects are [72]

- gate insulator time-dependent breakdown, due to insulator trapped charge during high-field stress,
- hot carrier injection, because of high electric fields,
- negative bias temperature instability in PMOS devices, due to interface traps from high gate voltage and high temperature, and
- electromigration, due to defects in conductive materials.

In order to maintain low failure rates at an increasing chip complexity new chip materials have to be evaluated and the design rules have to be adapted [81].

3.1.3 Challenges of Scaling with Respect to Analog Circuits

Besides the major digital part, analog circuits are necessary in SoC applications. The effects of scaling affect analog circuits severely. An outline of challenges and benefits is given.

Transistor Speed and Gain Major effect of scaling in digital circuits is the improvement of speed and packing density. Analog circuits benefit from the increasing speed as well. Parasitic capacitances are reduced and the gate resistance is increased due to the gate length scaling. The transit frequency of the transistors (f_T) and the maximum oscillation frequency increase with ongoing scaling. The transistor speed and the transistor intrinsic gain are in direct competition. High speed transistors lead to a low output resistance and consequently to a low intrinsic gain. Both can be improved by increasing V_{TH} or decreasing U_{GS} to operate in moderate inversion. However, moderate inversion is accompanied with a drop of f_T and oscillation frequency [82].

Supply Voltage and Signal Headroom Digital circuits benefit from a small supply voltage and have a reduced power consumption and increased logic speed. In analog circuits a reduced supply voltage leads to a small signal range and a limited signal headroom and may cause a larger layout area. Newer technologies may induce an increased power consumption [82]. At a constant power consumption the performance deteriorates when newer technologies are used because of their lower supply voltage [4]. Due the low supply voltage of deep-sub-µm and nanometer analog circuits additional circuit blocks (e.g. due to more amplifier stages to achieve the same gain as with conventional circuits in sub-µm technology and/or more replica circuits) the power dissipation increases to keep a constant circuit performance. The increase of power becomes more relevant as the supply voltage is in the range of the threshold voltage V_{TH}. Low V_{TH} devices are sometimes available for analog circuits but cannot be used in the digital domain due to the subthreshold currents. The limited signal range and signal headroom demand accurate analog designs and a good noise performance to maintain the signal-to-noise ratio (SNR) and dynamic range.

Low-Frequency Noise Flicker noise or 1/f noise is generated by the fluctuation of the total number of carriers and the fluctuation of the mobility of the carriers in the transistor channel [70]. It attains increasing observance in analog design due to the shrinking feature sizes in CMOS technology. 1/f noise increases inversely proportional to the gate area and has a considerable amount in deep submicron and nanometer CMOS technology. A common expression of the 1/f-noise density is given in [104]:

$$d\overline{v^2} = \frac{KF_F}{WLC_{OX}^2}\frac{df}{f} \tag{3.1}$$

In (3.1) KF_F is a parameter, nearly independent of the technology. W is the gate width and L represents the gate length. C_{OX} is the specific gate oxide capacitance. It is notable, that almost all technology effects are included in C_{OX}^2.

Matching Matching is an important criterion in analog circuits, especially in differential structures. The matching of V_{TH}, g_m, saturation current (I_{dsat}), and the device matching is mainly dependent on the precision of the manufacturing process. In deep submicron technologies additional factors become significant. Voltage matching, which is usually described by the difference of V_{TH} of two identical transistors, becomes less sensitive to the device dimensions, when technology scales [72]. Matching can be improved by increasing the device dimensions.

Gate Leakage Current The gate leakage current is mainly limited by digital considerations, such as static power consumption. In nanometer CMOS technology gate leakage currents have to be considered in analog circuit design. The gate leakage current depends on the oxide thickness, the gate-source voltage U_{GS}, the gate-drain voltage (U_{GD}), and the gate area [72]. The gate leakage current affects the input bias currents, the gate leakage mismatch and the shot noise due to the gate current. In order to minimize the gate leakage high-k dielectrics for the gate insulator are developed [82].

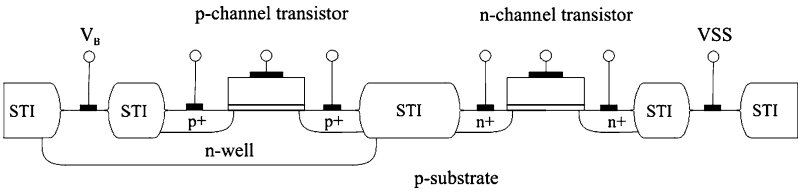


Fig. 3.1 Physical structure of the transistors in 120 nm CMOS

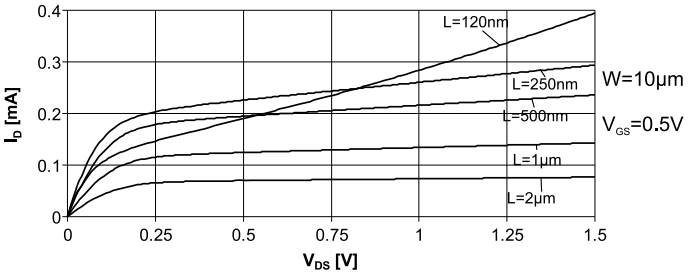
Linearity Distortions in analog circuits in nanometer CMOS technology are mainly caused by the increased influence of the series resistance and velocity saturation. By scaling the CMOS technology, i.e. due to reduced supply voltage, the voltage headroom decreases and in analog bias conditions scaling worsens the linearity [131].

3.2 0.12 µm CMOS Technology

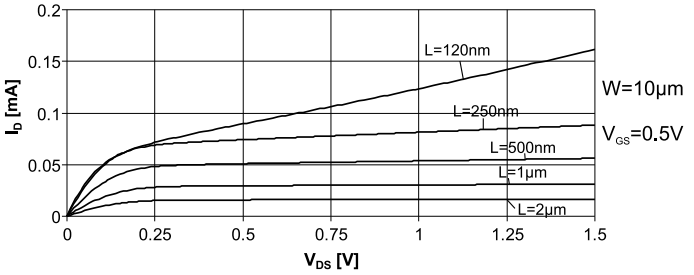
The 120 nm CMOS technology used was developed for SRAM, logic, mixed-signal and mixed-voltage I/O applications. The minimum lithographic structure size is 120 nm. It is a twin well CMOS technology which has a non-epi p-substrate and a n-well. In this technology 4 metal layers (M1–M4) are used for local wiring and 2 more layers (MG, MQ) are used for global wiring. The last metal layer which consists of AlCu (LB) is used for bonding. On the highest level planarized passivation is used. Figure 3.1 shows the physical structure of the transistors in this technology. The isolation between the active devices is done by shallow trench isolation (STI). It should be noticed that transistors close to STI (less than 1.5 µm between gate and STI) have increased threshold voltage, reduced mobility, and thus lower drive current. This is supposed to be due to the mechanical stress from the oxide within the isolation trench. The gate oxide breakdown voltage is about 2 V. The nominal supply voltage is 1.5 V, the maximum supply voltage is 1.6 V. More details are described in [50, 90]. For safe production and handling of the chips, an electrostatic discharge (ESD) protection has to be added on the chip. It usually consists of transistors and diodes which discharge the ESD current. This ESD protection has a large capacitance (typically 1–2 pF) which can have an influence on the remaining circuit.

In Fig. 3.2 the output characteristics for the n-channel transistor and the p-channel transistor for various gate lengths are shown. It shows the typical dependence on the gate length. The Early voltage can be estimated for the NMOS transistor with a length of 120 nm to 0.5 V and for the PMOS transistor to 0.75 V.

In Fig. 3.3 the transconductance in dependence on the gate-source voltages for the n-channel transistor and the p-channel transistor for various gate lengths is shown. The range for velocity saturation starts at a gate-source voltage of about 0.6 V. It shows that for the p-channel transistor the velocity saturation is more distinctive than for the n-channel transistor.



(a) NMOS transistor



(b) PMOS transistor

Fig. 3.2 Output characteristics of the transistors in 0.12 µm CMOS

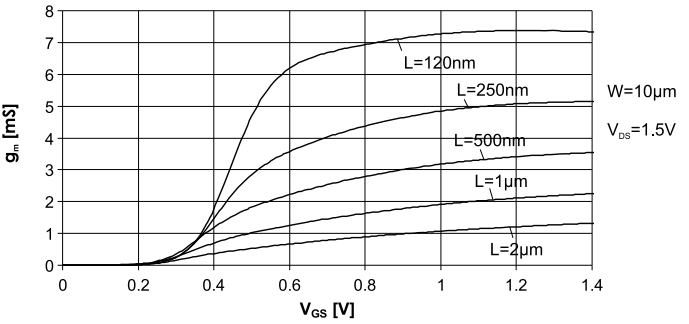
Two different resistors are possible in the 120 nm technology: the N+ diffusion and the P+ polysilicon. The disadvantage of the N+ diffusion resistor is its large capacitance to the substrate. For the P+ polysilicon resistor the block of formation of silicide is done by salicidation which decreases the S/D contact resistance and the gate series resistance.

There are different ways to realize capacitors in the 120 nm technology:

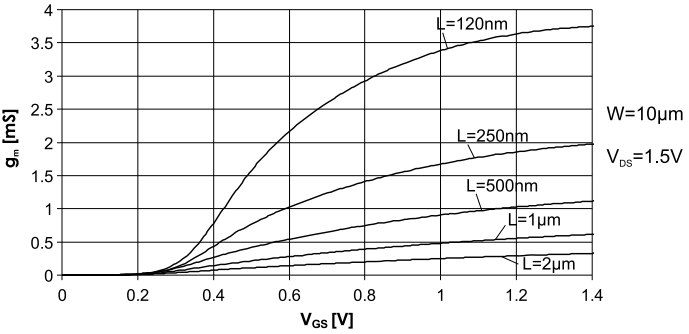
- Metal-metal capacitor
- MOS capacitor
- MIMCAP

The simplest capacitor, the metal-metal capacitor is between different metal layers (see Fig. 3.4). It has no voltage dependency and less parasitics but only small capacitances (typically 0.11 fF/µm^2) can be realized. The realization of a MOS capacitor is shown in Fig. 3.5. Large capacitances can be achieved but it has a high voltage dependency which makes it only appropriate for blocking the supply voltage. To increase the reliability of the capacitor, it can be realized also with a thicker oxide (DG). With this thicker oxide a capacitance film of 4.2 fF/µm^2 is achieved.

The MIMCAP is a *m*etal *i*nsulator *m*etal capacitor (see Fig. 3.6) and is formed by two additional mask layers between the upper copper level and the LB layer. The two plates (QT is the bottom plate and HT is the top plate) of the capacitor are wired to LB through VV (= vias for connecting upper copper level to LB). MIMCAP is allowed for all three possible metal stacks at top of the upmost copper level.



(a) NMOS transistors



(b) PMOS transistors

Fig. 3.3 Transconductances of the transistors in 120 nm CMOS

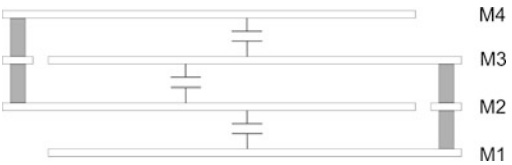


Fig. 3.4 Metal-metal capacitor

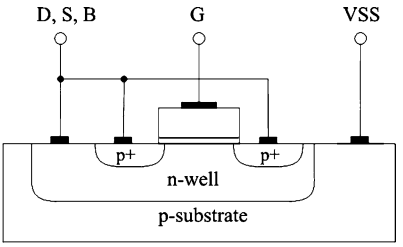


Fig. 3.5 Capacitor realized with a MOS-transistor

3.3 65 nm CMOS Technology

The 65 nm bulk CMOS technology used was developed for logic, SRAM, mixed-signal, and mixed-voltage I/O applications as well as for embedded DRAM appli-

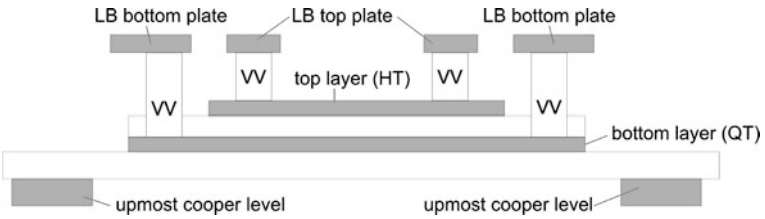
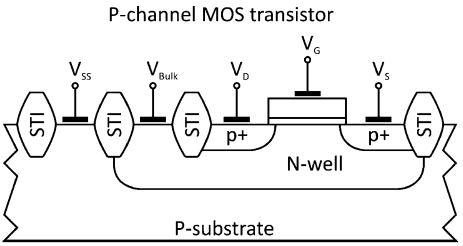
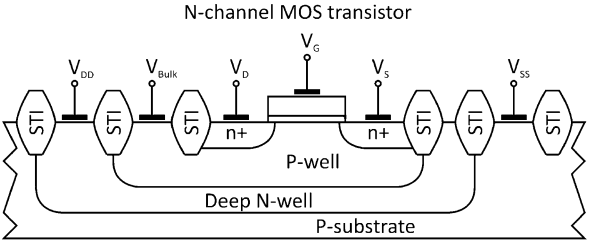


Fig. 3.6 MIMCAP

Fig. 3.7 Cross sections of MOSFET transistors in 65 nm triple-well CMOS



(a) P-channel MOSFET transistor



(b) N-channel MOSFET transistor

cations. Besides the 65 nm CMOS base process, there exists a 65 nm low-power (LP) CMOS process. The 65 nm low-power process has an approximately 100 mV higher threshold voltage than the base process and hence a lower off-state leakage current. Both options have three different oxide thicknesses to support several supply voltages from 1.2 V to 3.3 V [77].

In the following circuits only the 65 nm CMOS low-power technology is used, thus only important characteristics of the low-power CMOS are highlighted. Of course it is more challenging to develop analog circuits in the low-power version than in the base process. The 65 nm CMOS technology used is a triple well process on a p-substrate. The PMOS transistor is located in an isolated N-well and the NMOS transistor is placed in an insulated P-well, which is itself embedded in a deep N-well. Cross-sections of the transistors are depicted in Figs. 3.7(a) and 3.7(b). Active devices are separated by a shallow trench isolation (STI). Stress engineered devices are offered and the stress is caused by the location and the dimension of the STI. Mechanical stress increases the carrier mobility in p-channel MOSFETs and deteriorates the carrier mobility in n-channel MOSFETs [79].

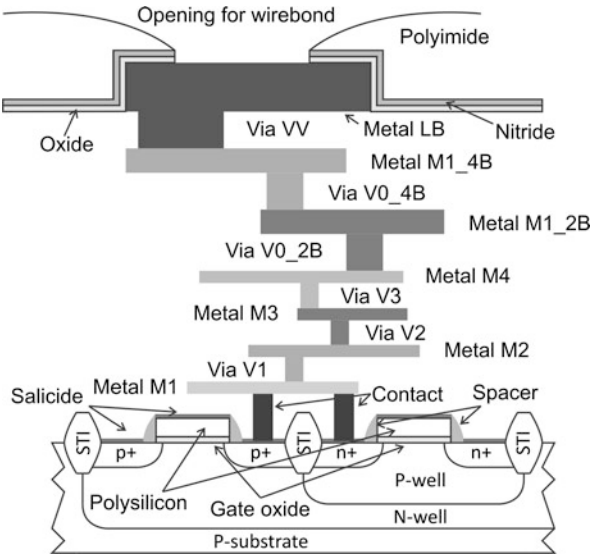


Fig. 3.8 Cross section of the 65 nm low-power CMOS process

The nominal supply voltage in the 65 nm low-power CMOS process is 1.2 V and the maximum supply voltage is 1.32 V. The technology cross section of the 65 nm CMOS process is shown in Fig. 3.8. It should be noted that the aspect ratios are not displayed correctly. The process uses a P-substrate, wherein N-well, P-well, and a deep N-well are embedded. Inside the wells are the appropriate n+ and p+ diffusion regions [115]. The gate oxide isolates the polysilicon gates from the transistor channels. The spacers ensure the isolation between gate and source/drain areas. Self-aligned silicide, also called salicide, forms the interconnect between the semiconductor and metal layers. The contacts connect the salicide to the metal layer 1 (M1). Metal M1 to M4 are 1x thin metal layers, which are connected by the vias V1 to V3. Via V0_2B connects 1x thin metal M4 to thick metal (2x) M1_2B. And finally Via V0_4B contacts the last copper metal layer M1_4B, which is a 4x thick metal layer. In total there exist 6 copper metal layers. The last metal layer LB is used for wiring and wirebonding. Metal LB is an aluminum wire level and is connected to M1_4B by the via VV. For bondpads the oxide and nitride film is opened as well as the polyimide passivation layer [6].

Transistor Characteristics The progress of scaling is noticeable in several transistor parameters and properties. Figure 3.9 shows the output characteristics of an NMOS transistor with varied gate length L in the 65 nm CMOS technology. The transistor width W is 5 µm and the gate source voltage U_{GS} of 600 mV is applied. The Early voltage declines with decreasing gate length L and is in a range of a few volts. At the gate length of 60 nm the Early voltage is only about 0.31 V. At a constant transistor width the drain current should increase at smaller gate lengths. In Fig. 3.9 it is different because of the threshold-voltage roll-off [54]. The threshold-voltage roll-off is caused by the short-channel effect and the fringing-field effect and

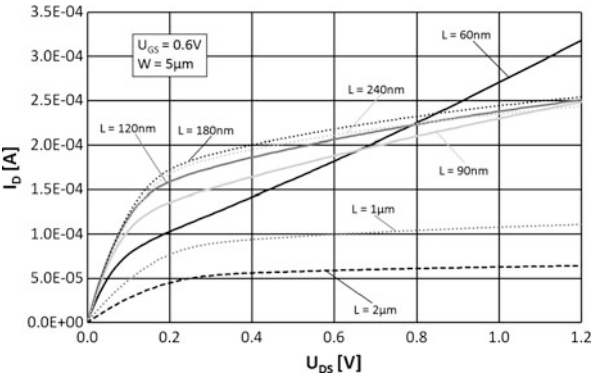


Fig. 3.9 NMOS output characteristics at varied gate length L

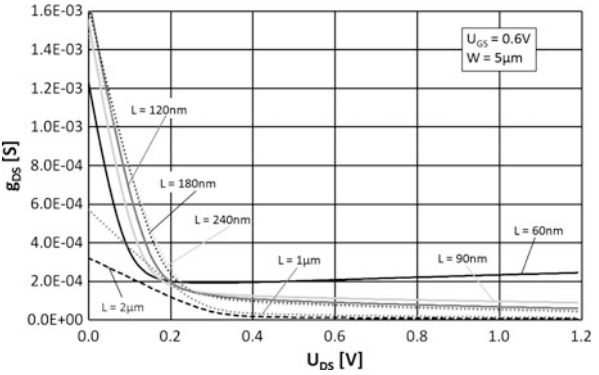


Fig. 3.10 NMOS output conductance g_{DS} at varied gate length L

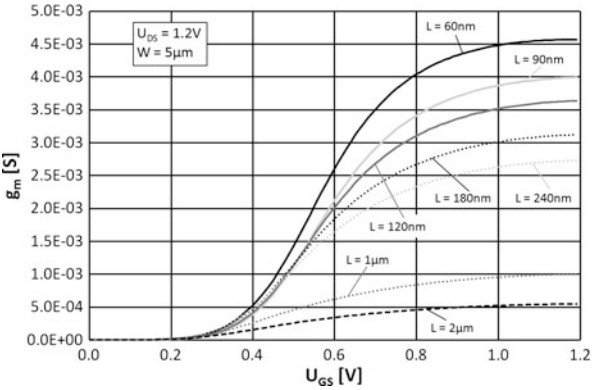


Fig. 3.11 NMOS transconductance g_m at varied gate length L

results in a rising threshold-voltage at decreasing gate lengths. Figure 3.10 depicts the output conductance g_{DS} against the drain source voltage U_{DS} which is decreasing with increasing gate lengths (for $U_{DS} > 0.4$ V).

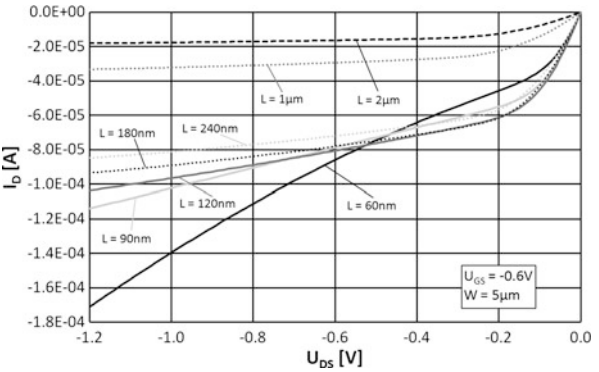


Fig. 3.12 PMOS output characteristics at varied gate length L

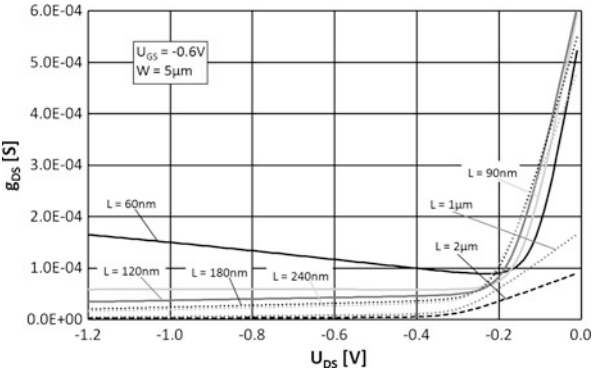


Fig. 3.13 PMOS output conductance g_{DS} at varied gate length L

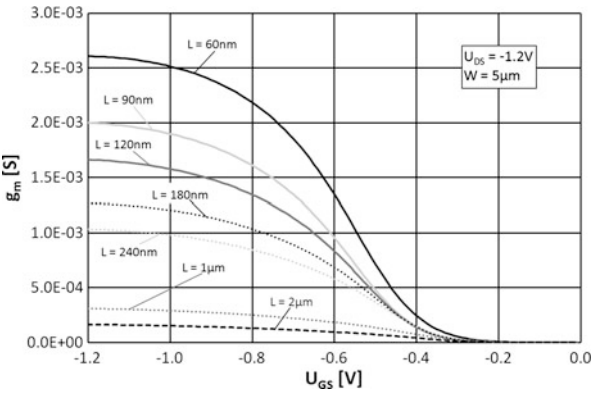


Fig. 3.14 PMOS transconductance g_m at varied gate length L

The transconductance g_m of an NMOS transistor with the gate width of 5 µm is shown in Fig. 3.11. U_{DS} is 1.2 V. g_m is decreasing with larger lengths L as well as g_{DS}.

Figure 3.12 depicts the output characteristics of a PMOS transistor with various gate lengths and 5 µm gate width. The gate-source voltage is fixed at −600 mV. The threshold-voltage roll-off takes effect as well, but is not so obvious. The Early

voltage of a PMOS minimum gate-length transistor is in the same range as of an NMOS transistor. The 60 nm PMOS transistor has an Early voltage of only about 0.26 V. Figure 3.13 shows the output conductance g_{DS}.

Figure 3.14 shows the transconductance of PMOS transistors while gate lengths L are varied. The PMOS transistor has a gate width of 5 µm and is biased with a U_{DS} of 1.2 V. Again a smaller L improves the transconductance g_m.

Chapter 4
Operational Transconductance Amplifiers (OTAs)

An ideal transconductance amplifier is a voltage-controlled current source, with an infinite input and output impedance. Beside in G_m-C filters, OTAs can be used in data converters, variable gain amplifiers and equalizers. In Fig. 4.1 the symbol of a single-ended and a fully-differential transconductor is shown. The factor between the output current and the input voltage is called transconductance.

$$i_{out} = G_m \cdot (v_{inp} - v_{inn}) \tag{4.1}$$

One of the key attractive properties of OTAs is the fast speed in comparison to conventional operational amplifiers. The high-bandwidth capability of the OTA is in part due to the fact that the internal nodes are of low impedance. Usually, a transconductor consists of only one gain stage which means that no compensation capacitance is necessary. Non-ideal parameters of an OTA are the input capacitance C_{in}, the output capacitance C_{out} and the output conductance g_{out}. These non-ideal parameters will limit the AC-performance of the OTA and of filters. The OTA frequency-dependent transconductance and input and output capacitances will affect mainly the high frequency characteristics. The finite output resistance will affect especially the low-frequency response of filters. The transconductance G_m is frequency dependent and can be described by a first-order low-pass

$$G_m(j\omega) = \frac{G_{m0}}{1 + j\omega/\omega_T} = \frac{G_{m0}}{\sqrt{1 + (\frac{\omega}{\omega_T})^2}} e^{-j\Phi(\omega)} \tag{4.2}$$

where G_{m0} is the DC transconductance and ω_T is the transit frequency of the OTA. When an OTA is applied to a G_m-C filter, ω_T is usually much larger than the filter cut-off frequency f_C. So the transconductance at f_C can be described as

$$G_m(j\omega_C) \approx G_{m0} \cdot e^{-j\Phi_E} \tag{4.3}$$

where Φ_E is the phase of the transconductance at the filter cut-off frequency and is called excess phase.

H. Uhrmann et al., *Analog Filters in Nanometer CMOS*,
Springer Series in Advanced Microelectronics 45,
DOI 10.1007/978-3-642-38013-6_4, © Springer-Verlag Berlin Heidelberg 2014

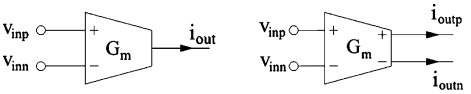


Fig. 4.1 Symbol of a transconductor

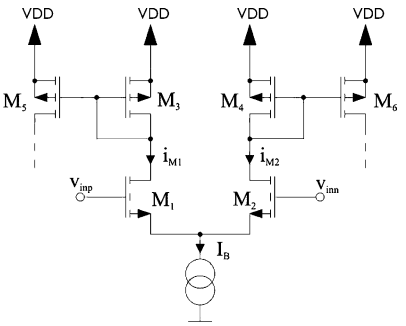


Fig. 4.2 Simplest transconductor

For the design of high-frequency G_m-C filters the parasitic capacitances involve some problems.

- The parasitic capacitances are usually not accurately known. For some high-frequency designs where the parasitics are a large part of the total integrating capacitance, this problem causes an increased uncertainty in the filter capacitance value.
- In general, the parasitics are nonlinear. This induces distortion as well as the frequency response depends on the signal amplitude.
- The presence of parasitics involves some mismatch between two integrators. For best matching, the fraction each type of parasitic contributes to the total integrating capacitance should be kept the same for all integrators.

Another important issue is the input range that will give a constant transconductance. This is very important for determining the level of distortion of the output currents.

4.1 Linearization Techniques for OTAs

The simplest transconductor consists of a standard differential pair (see Fig. 4.2). Under the assumption that the input transistors have an ideal quadratic transfer characteristics, the third harmonic distortion (HD3) and the 3rd-order intermodulation product (IM3) of the currents i_{M1}, i_{M2} can be calculated from [71] as

$$HD3 = \frac{1}{32}\frac{v_{in}^2}{(V_{GS} - V_{TH})^2}, \qquad IM3 = \frac{3}{32}\frac{v_{in}^2}{(V_{GS} - V_{TH})^2} \tag{4.4}$$

Usually the common-mode input voltage is at $V_{DD}/2 = 0.75$ V, which means that the overdrive voltage ($=V_{GS} - V_{TH}$) can be at maximum 0.3 V (V_{TH} is typically

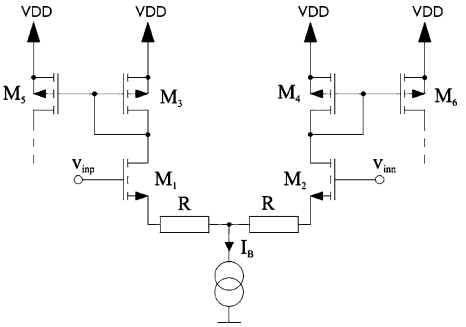


Fig. 4.3 Transconductor with source resistors

0.35 V, the saturation voltage of the current source is at minimum 0.1 V). With this overdrive voltage for an input signal of 200 mV a $HD3 = -37.15$ dB is obtained from (4.4). The linearity of the transconductor can be improved by adding source resistors (see Fig. 4.3). The HD3 can then be calculated from [112]

$$HD3 = \frac{1}{32 \cdot N^2} \frac{v_{in}^2}{(V_{GS} - V_{TH})^2} \tag{4.5}$$

with the degeneration factor N

$$N = 1 + g_m \cdot R \tag{4.6}$$

This expression can be formed with the voltage drop V_R on the resistor to

$$N = 1 + g_m \cdot \frac{V_R}{I_R} = 1 + \frac{2 \cdot V_R}{V_{GS} - V_{TH}} \tag{4.7}$$

An easy estimation gives now that the maximum voltage drop on the resistor can be 0.2 V ($V_{TH} = 0.35$ V, $(V_{GS} - V_{TH}) = 0.1$ V and the saturation voltage on the current source is at minimum 0.1 V) and so the resulting degeneration factor N is 5. With (4.5) the 3rd harmonic distortions are -46.02 dB for an input signal of 200 mV.

In Fig. 4.4 a pseudodifferential self-regulated OTA based on transistors operation in triode region is shown which was introduced by [16]. The transistors M1 and M2 operate in triode region, the transistors M3 and M4 form with the opamps a regulated gain control and they are used to fix the drain voltage of M1 and M2. One of the main sources of the OTA's nonlinearity is the low gain of the opamp at high frequencies. The HD3 of the OTA output current can be expressed from [16] as (neglecting short-channel effects)

$$HD3 = \frac{v_{in}^2}{4} \frac{K_{1,2}^2}{[(A(s) + 1)g_{m1,2} + K_{1,2} \cdot (V_{CM} - V_{D1,2} - V_{TH1,2})]^2} \tag{4.8}$$

where $K_{1,2}$ is the transconductance parameter of the input transistors ($K_{1,2} = \mu_n C_{OX}(W_{1,2}/L_{1,2})$) and $A(s)$ is the gain of the opamp. For filter applications it is assumed that the transconductor's cut-off frequency should be at least 10-times

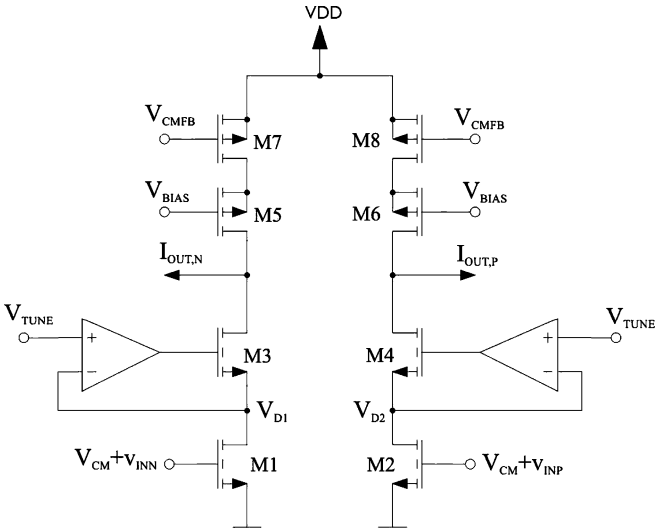


Fig. 4.4 OTA based on transistor operation in triode region

higher than the filter cut-off frequency. This results in a 10-times higher unity-gain frequency than the filter cut-off frequency. So the gain of the opamp in (4.8) is 10. This has the consequence that the second part in the denominator in (4.8) can be neglected and the 3rd harmonics can be calculated from [16]

$$HD3 = \frac{v_{in}^2}{4} \frac{K_{1,2}^2}{[(A(s)+1) \cdot g_{m1,2}]^2} = \frac{v_{in}^2}{4 \cdot (V_{GS} - V_{TH1,2})^2 \cdot (A+1)^2} \tag{4.9}$$

A simple estimation gives for an input voltage of 200 mV and with $V_{GS1,2} - V_{TH1,2} = 300$ mV and $A = 10$ a HD3 of -60.7 dB. But it should be taken into account that the transit frequency of the operational amplifiers should be at least 10 times larger than the filter cut-off frequency which means that the current consumption will increase at higher frequencies.

In [71] another technique to enhance the linearity of an OTA is presented. It is based on the cancellation of two differently biased cross-coupled differential pairs (see Fig. 4.5). The current of the jth transistor is given:

$$i_j = g_{m,j} v_{in} \sqrt{1 - \left(\frac{v_{in}}{2 \cdot (V_{GS} - V_{TH})} \right)^2} \tag{4.10}$$

where v_{in} is the input differential voltage and $g_{m,j}$ is the transconductance of the jth transistor. Expanding (4.10) in a Taylor series and considering only the first two terms, the output current becomes:

$$i_i = g_{m,i} \left[v_{in} - \frac{v_{in}^3}{8 \cdot (V_{GS} - V_{TH})^2} \right] \tag{4.11}$$

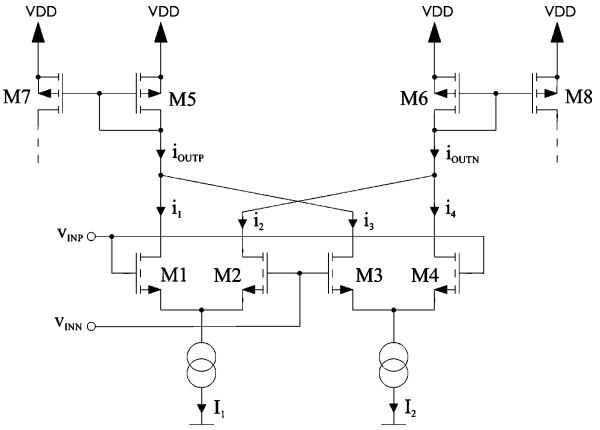


Fig. 4.5 OTA based on cross-coupled differential pairs

The two differential pairs are connected such that the total output currents are $i_{OUTP} = i_1 – i_2$ and $i_{OUTN} = i_3 – i_4$. So the third harmonics can be canceled completely if the following conditions are satisfied

$$\frac{g_{m1}}{(V_{GS1} - V_{TH1})^2} = \frac{g_{m2}}{(V_{GS2} - V_{TH2})^2} \tag{4.12}$$

or

$$\frac{K_1}{V_{GS1} - V_{TH1}} = \frac{K_4}{V_{GS4} - V_{TH4}}, \qquad \frac{K_2}{V_{GS2} - V_{TH2}} = \frac{K_3}{V_{GS3} - V_{TH3}} \tag{4.13}$$

Due to process parameter variations, the bias conditions (I_1 and I_2) where the maximum linearity is achieved can be slightly different. This cancellation technique works only in one certain operation point. Due to the fact that mismatch shifts the operation point, the third harmonics are not canceled completely. If the matching parameters are applied now to (4.10), the amplitude of the 3rd harmonic can be calculated to

$$\begin{aligned} i_{3,out} &= \frac{K_1 + \Delta K_1}{8 \cdot (V_{GS1} - V_{TH1} - \Delta V_{TH1})} v_{in}^3 - \frac{K_2 + \Delta K_2}{8 \cdot (V_{GS2} - V_{TH2} - \Delta V_{TH2})} v_{in}^3 \\ &\approx \frac{K_1}{8 \cdot (V_{GS1} - V_{TH1})} \left(1 + \frac{\Delta K_1}{K_1} + \frac{\Delta V_{TH1}}{V_{GS1} - V_{TH1}}\right) v_{in}^3 \\ &\quad - \frac{K_2}{8 \cdot (V_{GS2} - V_{TH2})} \left(1 + \frac{\Delta K_2}{K_2} + \frac{\Delta V_{TH2}}{V_{GS2} - V_{TH2}}\right) v_{in}^3 \\ &= \frac{K_1}{8 \cdot (V_{GS1} - V_{TH1})} \\ &\quad \cdot \left(\frac{\Delta K_1}{K_1} - \frac{\Delta K_2}{K_2} + \frac{\Delta V_{TH1}}{V_{GS1} - V_{TH1}} - \frac{\Delta V_{TH2}}{V_{GS2} - V_{TH2}}\right) v_{in}^3 \end{aligned} \tag{4.14}$$

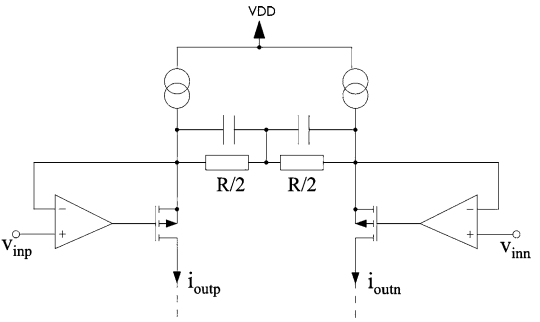


Fig. 4.6 OTA input stage in combination with passive resistors

The 3rd harmonic distortion can be calculated to

$$HD3 = \frac{1}{8}\left(\frac{v_{in}}{V_{GS1} - V_{TH1}}\right)^2 \left(\frac{\Delta K_1}{K_1} + \frac{\Delta K_2}{K_2} + \frac{\Delta V_{TH1}}{V_{GS1} - V_{TH1}} + \frac{\Delta V_{TH2}}{V_{GS2} - V_{TH2}}\right) \tag{4.15}$$

If the transconductor mismatch is estimated to $\Delta K/K = 1\ \%$ and $\Delta V_{TH}/(V_{GS} - V_{TH}) = 1\ \%$ and it is assumed that $V_{GS} - V_{TH} = 200$ mV and $v_{in} = 200$ mV, the standard deviation of the third harmonics is -48.5 dB. This is theoretically the minimum achievable value of the distortions.

In [13] an OTA is described which is realized by means of a G_m input stage in combination with passive resistors (shown in Fig. 4.6). The difference of the input voltages lies across the resistors and due to the use of linear resistors a very linear V–I conversion is obtained without any matching requirements. But it should be noticed that in this design two differential amplifiers with a very good high frequency performance are necessary.

All the here presented linearization techniques are not sufficient to apply these OTAs to a G_m-C filter. At first it should be noticed that the output stage of the OTA produces also some distortions. Secondly, a G_m-C filter consists of several OTAs which means that the distortions increase with the number of OTAs. Under the assumption that the OTAs produce the same distortions, the HD3 of the whole filter can be calculated to

$$HD3_{filter} = HD3_{OTA} \cdot n \tag{4.16}$$

where n is the number of OTAs. When a G_m-C filter consists of 4 OTAs, the HD3 of the filter is 12 dB worse than the HD3 of one OTA. Table 4.1 summarizes the distortions of the presented OTAs and gives an estimation for the distortions, when these OTAs are applied to a G_m-C filter which consists of 4 OTAs.

In [96] another interesting OTA architecture is discussed which is based on a super-source-follower configuration.

Table 4.1 Distortions of the discussed OTAs

OTA topology	$HD3_{OTA}$ [dB]	$HD3_{filter}$ [dB]
Simple OTA	−37.2	−25.2
OTA with source resistors	−46.2	−34.2
OTA with transistors in triode region	−60.7	−48.7
OTA with differential pair	−48.5	−36.5

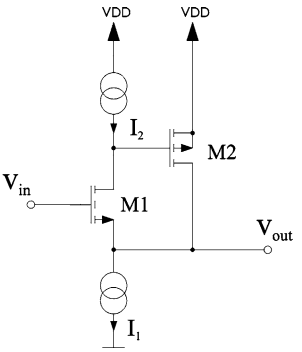


Fig. 4.7 Super-source-follower

4.2 OTA Based on a Super-Source-Follower Configuration

The output resistance of a source follower is approximately $1/g_m$. For some applications, especially for driving low resistors, the output resistance is too high. A possibility to reduce the output resistance is to increase the transconductance which means that the area or dc bias current increases. Another possibility to decrease the output resistance is to use a super-source-follower configuration which is shown in Fig. 4.7. To obtain an operation point the current through the transistor M2 is the difference between I_1 and I_2. Therefor, $I_1 > I_2$ is required for proper operation. Under the assumption that the output resistance of the current sources are much higher than the output resistances of the transistors M1 and M2, the voltage gain is given from [39] by

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} r_{DS1}}{1 + (g_{m1} + g_{mb1}) r_{DS1} + \frac{1}{g_{m2} r_{DS2}}} \tag{4.17}$$

and the output resistance can be expressed by

$$r_{out} = \frac{1}{g_{m1} + g_{mb1}} \cdot \left(\frac{1}{g_{m2} r_{DS1}} \right) \tag{4.18}$$

From (4.17) it is obvious that the voltage gain is near unity if the gain of the loop consisting of the transistors M1 and M2 is high ($g_{m2} r_{01} \gg 1$). The disadvantage of this super-source configuration is that the negative feedback loop through M2 can become instable when a capacitive load is driven. When two super-source-followers

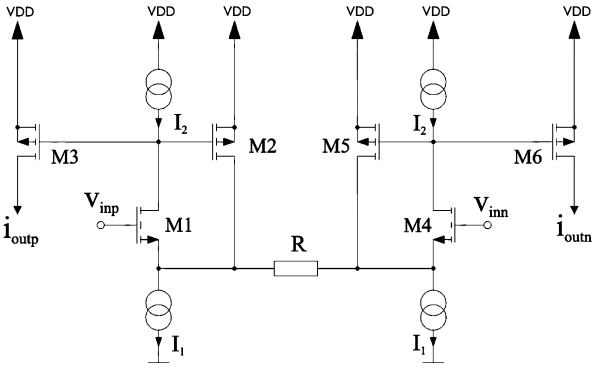


Fig. 4.8 OTA based on a super-source follower configuration

are coupled across a resistor, the voltage on the resistor is the difference of the input voltage (see Fig. 4.8). The current through the resistor can be transferred from M2 to M3 respectively from M5 to M6 because the gate-source voltages are the same. Due to the high closed-loop gain and the use of a linear resistor a very linear voltage to current conversion is obtained. The current through the transistors M2 and M3 can be calculated to

$$i_{M5} = \frac{v_{inp} - v_{inn}}{R + \frac{2}{g_{m1}(1+A_0)}} \cdot \frac{A_0}{1 + A_0} \tag{4.19}$$

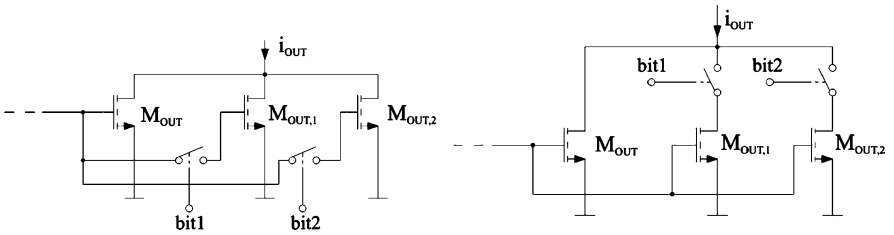
where A_0 is the small-signal open-loop gain of the loop consisting of M1, M2 respectively M4, M5 and is the product of their transconductances times the impedances at the node of the gate of transistor M2, respectively M5, and can be calculated to

$$A_0 = \frac{g_{m1}}{g_{ds,1}} = \frac{g_{m2}}{g_{ds,2}} \tag{4.20}$$

With a high closed-loop gain the term $2/[g_m(1 + A_0)]$ in (4.19) can be neglected which has the consequence that the nonlinearity of g_{m1} does not play a role. So with a higher A_0 the distortions become better.

4.3 Digitally Programmable OTAs

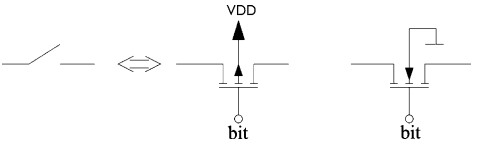
Due to the fact that all devices have manufacturing tolerances, the filter parameters have also some tolerances. To achieve the exact filter parameters, a digitally programmable concept for an OTA is developed. Two different strategies are shown in Fig. 4.9. Several transistors, which are activated by a digital signal, are switched in parallel to the output transistor M_{out}. In the first way (Fig. 4.9(a)), the gates of the transistors M_{out1} and M_{out2} are activated by the digital word. In contrast, in Fig. 4.9(b) the transistors are switched according to their digital word. In addition, this avoids having to insert switches in the high-frequency signal path. Usually the W/L ratio of the switching transistors is smaller than the W/L ratio of the output



(a) Concept 1 for a switchable OTA (b) Concept 2 for a switchable OTA

Fig. 4.9 Concept for a switchable OTA

Fig. 4.10 Switches



transistor M_{out}. This has the consequence that the switching has no influence on the common-mode feedback.

A switch can be realized as a single transistor (see Fig. 4.10). To insure that the bulk-source and bulk-drain pn junctions are reverse biased, the bulk must be connected to V_{DD} for the pMOS transistor. A transistor works in the triode region, when it is used as a switch. The switch resistor R_{ON} can be calculated to

$$R_{ON} = \frac{1}{K' \cdot W/L \cdot (V_{GS} - V_{TH})} \tag{4.21}$$

4.4 Common-Mode Feedback Loop

In a fully differential design a common-mode feedback (CMFB) loop is required to stabilize the common-mode voltage. In principle this stabilization can be done in the discrete time domain or in the continuous-time domain. The main advantage of a sampled CMFB is that the power consumption is quite low. But it should be noticed that it produces also a lot of disturbances like clock feedthrough. So this book focuses only on continuous-time CMFBs. Usually a continuous-time CMFB consists of a differential amplifier which compares in a negative feedback loop the mean value of the output voltages with a reference voltage (see Fig. 4.11). It is necessary that the bandwidth of the amplifier in the CMFB loop is higher than the bandwidth of the OTA in order to ensure stable biasing conditions for all frequencies up to the cut-off frequency.

The realization of a typical common-mode amplifier is shown in Fig. 4.12. The resistors R_1 and R_2 take the mean value of the output voltages, the capacitors C_1 and C_2 make the voltage divider independent of their parasitic capacitances [7]. The resistors R_3 and R_4 decrease the flicker noise, R5 enhances the speed of the

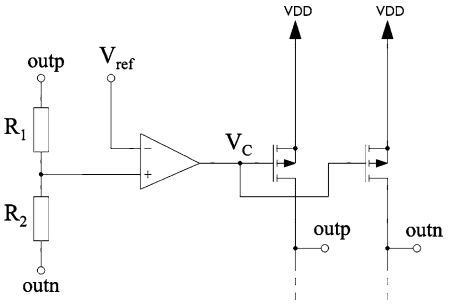


Fig. 4.11 Principle circuit of a CMFB

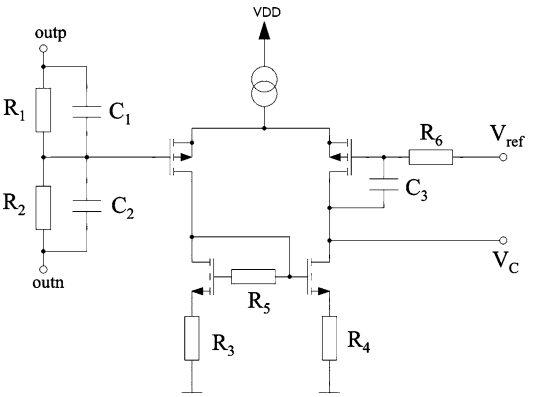


Fig. 4.12 Typical realization of a CMFB

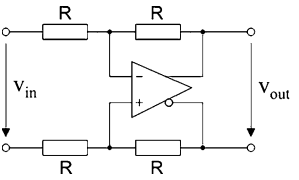


Fig. 4.13 Buffer amplifier

current mirror [135]. The compensation of the amplifier is done with the low-pass consisting of R_6 and C_3.

4.5 Buffer Amplifier

At the output a buffer amplifier is used to drive the pad capacitances. This amplifier consists of a fully differential operational amplifier (detailed description in [106]) which works in a unity-gain configuration (see Fig. 4.13). The amplifier has a transit frequency of 1.5 GHz, a DC gain of 40 dB and can drive the ESD protection and a load capacitance of 3.2 pF. Distortion measurements showed that the 3rd harmonics are −54 dB for an 800 mV peak-to-peak signal.

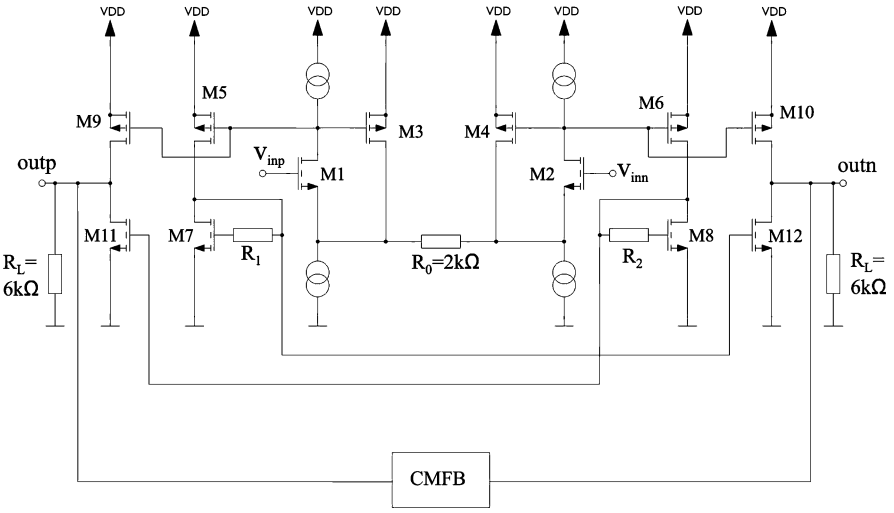
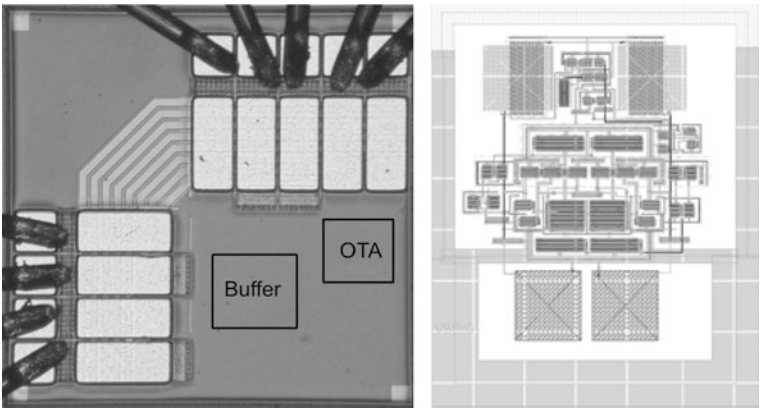


Fig. 4.14 Realization of an OTA with super source followers



(a) Chip photograph of the whole chip (b) Layout plot of the OTA

Fig. 4.15 Realized OTA

4.6 Realization of an OTA

A fully differential OTA based on a super-source-follower configuration (see Fig. 4.14) was realized in 120 nm CMOS [56]. The core of this OTA is described in Sect. 4.2. The currents from the transistors M3 and M4 are transferred to a push-pull stage which minimizes the common-mode gain. The resistors R_1 and R_2 are used to increase the bandwidth of the current mirror [135]. At the output stage the CMFB from Sect. 4.4 is used for the stabilization of the operating point. At the outputs of

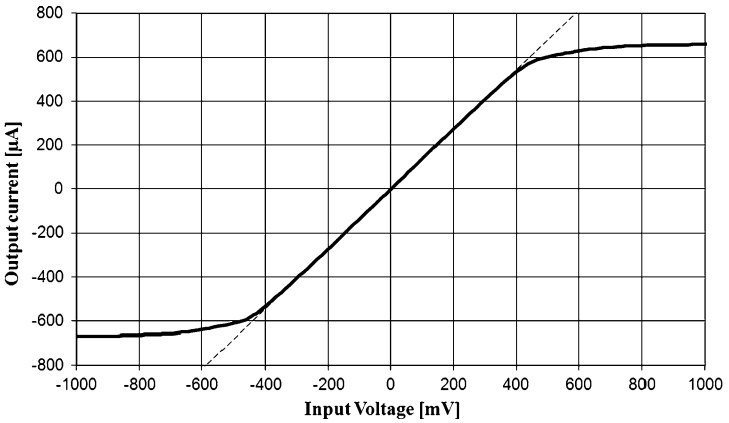


Fig. 4.16 Measured DC transfer characteristics

Table 4.2 Measured harmonics of the output signal

f	HD [dB] $V_{out} = 200\ \mathrm{mV}_{pp}$	HD [dB] $V_{out} = 700\ \mathrm{mV}_{pp}$
$3f_C$	−54.7	−29.0
$5f_C$	−59.5	−37.3

the OTA two resistors $R_L = 6\,\mathrm{k}\Omega$ are connected. This gives with the input resistance of the buffer amplifier (=3 kΩ) a resulting load resistance of 2 kΩ.

In Fig. 4.15 the chip photograph and the layout plot of the realized chip are shown. Due to the passivation layer and the planarization of the metal layers only the upper metal layers (metal layer 5 and 6) can be seen on a chipphoto. The active area of the OTA is $80 \times 60\ \mu\mathrm{m}^2$.

In Table 4.2 the measured differential spectral components of a single-tone measurement with an input frequency of $f_C = 50$ MHz are presented.

At the output of the OTA a buffer amplifier (described in Sect. 4.5) is used to drive the pad capacitances. Figure 4.16 shows the measured DC-transfer characteristics. For a differential output current of ±550 µA the transfer curve is linear.

Chapter 5
G_m-C Filters

Analog filters are required in many mixed-signal systems. They can be used for anti-aliasing purposes, before signals are sampled in an A/D converter or they can be used for reconstructing the signal after a D/A converter. Also at the output of a mixer a filter which suppresses out-of-band interferer signals is necessary. In general, when a filter is designed it is necessary to consider the whole system in which the filter is embedded. Important parameters for filters are in-band and also out-of-band distortions. A high in-band linear dynamic range avoids intermodulation between two in-band signals. Out-of-band distortions are also essential because they describe the immunity against some blockers or disturbances to other channels in a multi-band system. Other important parameters are the noise spectral density or the integrated noise. For some applications the out-of-band spectral noise density should be under a certain level, otherwise the noise would interfere to a neighboring channel. Sometimes, when the same filter is used in the I-path and in the Q-path of a receiver, the mismatch between these two filters should not be too high.

5.1 Filter Topologies

Continuous-time (CT) filters have advantages over and digital filters in terms of high speed and low power dissipation. In fact, switched-capacitor (SC) filters involve some inherent problems especially at higher frequencies. First of all, the clock generation is a complex issue because a non overlapping clock is required, that has accurate clock edges and a low jitter. The clock feed-through leads to an interference with the filtered signal. Secondly, good switching properties of the transistors, which imply a low on-resistance and a high off-resistance, are necessary. A low on-resistance can be achieved by increasing the transistor width that also means an increase of the parasitic capacitance.

In principle, for the realization of integrated CT filters 3 different topologies are possible:

H. Uhrmann et al., *Analog Filters in Nanometer CMOS*,
Springer Series in Advanced Microelectronics 45,
DOI 10.1007/978-3-642-38013-6_5,

- Opamp RC-filter
- G_m-C filter
- Current-mode filter

For the design of CT filters in the frequency range below 50 MHz mostly an active RC-filter based on an opamp is used. The reason is that the opamp works in a feedback loop which allows a large swing with acceptable distortions. To achieve a high linearity, the unity-gain frequency of the opamp must be at least 20 times larger than the filter cut-off frequency. This would cause for a filter with a cut-off frequency of 250 MHz a unity-gain frequency of 5 GHz. The implementation of opamps of such high unity-gain frequencies is a difficult task. The highest achievable transit frequency found in the literature is described in [42] and is 2.6 GHz. So for the realization of CT filters in the hundred-MHz frequency range the G_m-C topology is a better candidate to obtain filters with a high quality factor.

In G_m-C filter design, the key component is the *o*perational *t*ransconductance *a*mplifier (OTA) which is a voltage dependent current source. An OTA usually works in an open-loop configuration which allows higher transit frequencies in comparison to opamps.

For some applications the signal processing is based on current signals. If these signals are applied to a voltage-mode filter, it is necessary to convert at first the current into a voltage and at the filter output the voltage must be converted into a current. With a current-mode filter no power for this conversion is necessary. In principle, current-mode design can be realized with the G_m-C architecture or with current mirrors which are decoupled by capacitors.

5.2 Performance of Filters—Figure of Merit

Typical parameters for analog filters are the cut-off frequency f_C, the power consumption P, the number of poles N and the dynamic range DR which is defined as the ratio of the maximum and minimum signal level which the circuit can handle at the same time. The minimum signal level is determined by the noise of the circuit, the maximum level by distortion. The dynamic range can be expressed as

$$DR = \frac{v_{s,n\ \%\ THD}^2/2}{\overline{v_{noise}^2}} \tag{5.1}$$

where $v_{s,n\ \%\ THD}$ is the magnitude of the signal when its THD reaches n %. Mostly in the literature for the calculation of the dynamic range, a THD of 1 % is assumed.

Generally, in analog circuits the absolute limit of power comes from the need to maintain the energy of the signal much larger than the thermal energy to achieve a required signal-to-noise ratio. This condition can be expressed from [134] as a minimum power per pole $P_{min} = 8 \cdot f_C \cdot k_B \cdot T \cdot SNR$, where f_C is the signal frequency, k_B denotes Boltzmann's constant, T is the absolute temperature and SNR is the signal-to-noise ratio. To compare analog filters, a common figure of merit

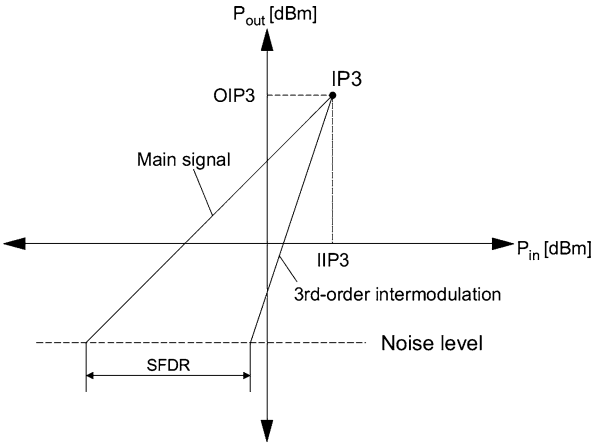


Fig. 5.1 Representation of SFDR and of IP3

(FOM) (introduced by [119]) is the ratio between the power consumption P of the filter and the minimum power P_{min} from [134].

$$FOM_1 = \frac{P}{8k_B T \cdot f_C \cdot N \cdot DR} \tag{5.2}$$

The lower the value for FOM_1 is, the better the filter circuit is. The main disadvantage of FOM_1 is that it is finally independent of the cut-off frequency because the integrated noise and so the DR depend on the cut-off frequency. Another drawback is also that the DR depends on the filter capacitances and so on the chip area which does not play a role in this FOM.

Another FOM, which is an extended version of FOM_1, was introduced by [132] and is given by

$$FOM_2 = \frac{P \cdot A}{N \cdot f_C \cdot SFDR \cdot IIP3} \tag{5.3}$$

where $SFDR$ is the spurious free dynamic range, IIP3 is the 3rd-order input intercept-point and A is the area of the filter. In general, the SFDR represents the maximum relative level that a circuit can tolerate while producing an acceptable signal quality from a small input level. The lower end of this input level is the noise level (see Fig. 5.1).

The IP3 (3rd-order intercept point) is obtained when the 3rd-order intermodulation reaches the main signal. The IIP3 (input intercept point) is the IP3 referred to the input, the OIP3 (output intercept point) is referred to the output. There exists a relationship between SFDR, IIP3 and the input noise level N_{in}

$$SFDR\ [\text{dB}] = \frac{2}{3} \cdot \left(IIP3\ [\text{dBm}] - N_{in}\ [\text{dBm}]\right) \tag{5.4}$$

In [80], a *FOM* is defined by

$$FOM_3 = DR \cdot \left(\frac{2\pi f_C N}{P} \right)^2 \tag{5.5}$$

The advantage of FOM_3 is that it finally depends on f_C but it should be noticed that it decreases with P^2.

Especially for low-passes with a high quality factor or for bandpasses, a *FOM* is defined by[29]

$$FOM_4 = \frac{N \cdot SFDR \cdot f_C \cdot Q}{P} \tag{5.6}$$

where Q is the quality factor of the filter.

5.3 State-of-the-Art

There is a large amount of publications on filters in micrometer and submicrometer CMOS and BiCMOS [21, 22, 31–84, 90]. In [16] a tunable 80–200 MHz 4th-order G_m-C filter in 0.35 µm CMOS is presented. The OTA is realized by transistors operating in triode region. The filter consumes 72 mW at a supply voltage of 2.3 V and has a DR of 52 dB.

In [101] a 4th-order Chebyshev low-pass filter for a multicarrier WCDMA receiver is described. This filter consists of 4 opamps and is realized in a 0.25 µm SiGe BiCMOS process. The cut-off frequency of this filter is 10 MHz, the current consumption is 87 mA, the in-band IIP3 is 2 dBV and the input-referred noise is 35.2 μV_{rms} which lead to an estimated dynamic range of 94 dB.

A 2.5 MHz 3rd-order Chebyshev G_m-C low-pass filter fabricated in a 0.25 µm CMOS process is described in [51]. The filter operates at 2.5 V and consumes 7 mA, the IIP3 is 32 dBm, the output noise is 130 nV/$\sqrt{\text{Hz}}$ which leads to an estimated DR of 75 dB.

A compact 2nd-order G_m-C biquad structure, which was introduced by [17] is shown in Fig. 5.2. Each transistor pair (M1/M2, M3/M4, M5/M6) works here as an OTA (OTA1, OTA2, OTA3) as depicted on the right side in Fig. 5.2. The main advantage of this architecture is its compact structure because only ten transistors and two capacitors are used and its low power consumption of 1.5 mW. The main disadvantage is its small linear range which gives for a 140 mV_{pp} signal a THD of −40 dB. The filter was realized in 0.18 µm CMOS, the pole frequency is tunable between 200 MHz to 600 MHz and the integrated output noise is 88 μV_{rms} which gives a dynamic range of 55 dB.

In [100] a 5th-order G_m-C filter in 0.18 µm CMOS is described. This filter is applied to suppress all higher-order harmonics generated by both a modulator and feedback mixer within a GSM offset-PLL transmitter. The cut-off frequency is tuneable between 48 MHz and 184 MHz and the filter consumes 12.5 mW. In spite

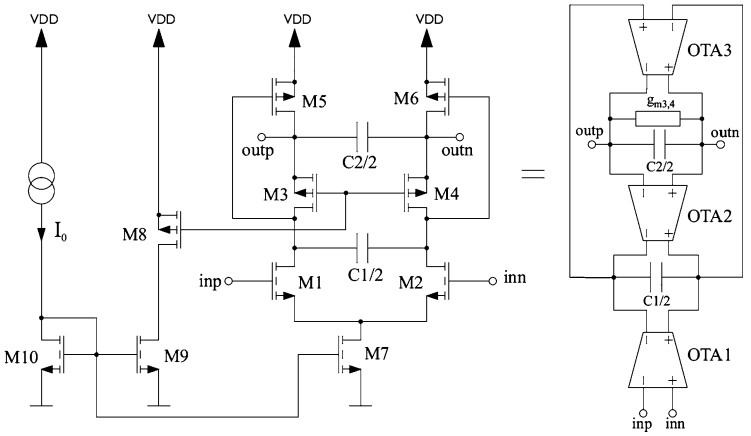


Fig. 5.2 Compact biquad cell

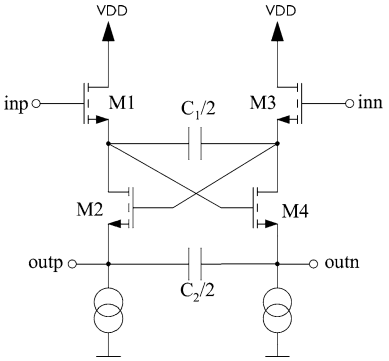


Fig. 5.3 Biquadratic cell based on source-follower configuration

of the supply voltage of 1.8 V the maximum differential output swing is equal to 300 mV.

In [145] a 3rd-order Butterworth low-pass G_m-C filter with a bandwidth of 50 kHz is described. The transconductor linearization technique is done by regulating the drain voltage of triode-biased input transistors through an active-cascode loop. The supply voltage is alterable between 1.2 V, 1.5 V and 1.8 V, the related values of the dynamic range are 67 dB, 75 dB and 76 dB. The filter consumes 167 µW, 240 µW and 292 µW for the supply voltages mentioned.

In [20] a source-follower-based filter cell is presented. The 2nd-order filter, shown in Fig. 5.3, consists of two cross coupled source followers in a positive feedback configuration. In this circuit, low output impedance is achieved and no common-mode feedback (CMFB) is necessary. The filter consisting of two biquad cells was realized in 0.18 µm CMOS and is a 4th-order 10 MHz filter for WLAN application. The IIP3 is 17.5 dBm, −40 dB HD3 for a 600 mV_{pp} is achieved and the integrated noise is 24 μV_{rms} which gives a DR of 79 dB, with a 2.25 mA current consumption.

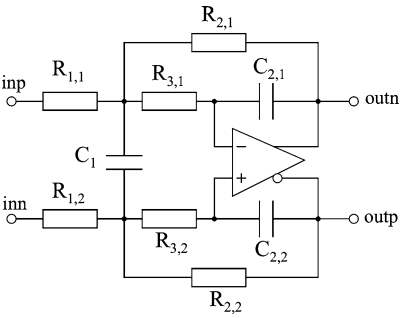


Fig. 5.4 Biquadratic cell based on opamp architecture

In [132] a low-power, 5th-order, active RC-opamp filter in 0.18 µm CMOS is presented. The filter has a bandwidth of 5 MHz and 10 MHz and consumes 4.6 mW at a supply voltage of 1 V. The DR can be estimated to 52 dB by the use of the integrated output noise in the passband of 267 μV_{rms} and the output signal of 0.32 V_{pp} at 1 % THD.

In [35] two 4th-order Bessel low-pass filters that cover various wireless standards are described. The filter is realized by two identical 2nd-order opamp filters as shown in Fig. 5.4. The first filter is designed for WLAN and UMTS applications and has a cut-off frequency of 2.5 MHz and 11 MHz, respectively. The DR is equal to 55 dB in WLAN environment and 58 dB in UMTS. The second filter is constructed for WLAN and Bluetooth tasks, where the bandwidth is switchable between 1 MHz and 11 MHz. The dynamic range in the WLAN mode is 55 dB and in the Bluetooth mode it is 58.2 dB. The filters are fabricated in a 0.13 µm standard CMOS technology and operate at a voltage supply of 1.2 V. The power consumption in WLAN operation is 5.6 mW in both filters and for UMTS and Bluetooth mode it is 3 mW.

Besides these voltage-mode filters no current-mode filters in deep-sub-micron technology can be found in literature. So only current-mode filters in micrometer and submicrometer CMOS can be presented. In [86] a 2nd- and 3rd-order current-mode filter based on the G_m-C architecture in a 0.35 µm standard CMOS technology is presented. A cut-off frequency programmability over the 40–200 MHz range is developed which can be applied to data storage systems. The 2 filters consume 3.7–18.6 mW and 4.8–24 mW per pole at a supply voltage of 2 V. The maximum input signal current at 1 % THD is 120 µA, the DR is 53 dB.

In [114] a 6th-order current-mode filter based on cross-coupled current mirrors in a 2 µm CMOS technology is presented. It consumes 0.7 mW per pole at a supply voltage of 3.3 V, has a cut-off frequency of 10 MHz and a DR of 52 dB.

In [148] a 5th-order current-mode filter in a 1.2 µm CMOS process is described. The cut-off frequency of this low-pass is tunable between 300 kHz and 1 MHz, it consumes 75 µW per pole at a supply voltage of 1.5 V and has a DR of 67 dB.

Table 5.1 summarizes the state-of-the-art.

Table 5.1 State-of-the-art

Citation	Architecture	Power per pole [mW]	Supply voltage [V]	Dynamic range [dB]	Cut-off frequency [MHz]	Order	Distortions	Technology (CMOS)
[16]	G_m-C	18	2.3	52	80–200	4	THD $= -44$ dB $V_{in} = 2\ V_{pp}$	0.35 µm
[101]	opamp	42.5	2.5		10	4	IIP3: 25 dBV	0.25 µm
[51]	G_m-C	1.45	2.5		2.5	3	IIP3: 32 dBm	0.25 µm
[17]	G_m-C	0.75	1.8	55	200–600	2	THD: -40 dB @ $V_{in} = 140\ mV_{pp}$	0.18 µm
[20]	source-follower based	1.02	1.8	79	10	4	IIP3: 17.5 dBm	0.18 µm
[100]	G_m-C	2.52	1.8		48–184	5	IIP3: 7 dBV	0.18 µm
[145]	G_m-C	0.08	1.5	75	0.05	3	THD: -40 dB @ $V_{in} = 260\ mV_{pp}$	0.18 µm
[35]	active-gmC-RC	1.4	1.2	55	11	4	OIP3: 29.3	0.13 µm
[35]	active-gmC-RC	0.75	1.2	58.2	1	4	OIP3: 34	0.13 µm
[132]	opamp	1.22	1.5	73	5	5	IIP3: 20 dBm	0.12 µm
[86]	current-mode G_m-C	4.8	2	53	42–215	3	THD: -40 dB @ $I_{in} = 120$ µA	0.35 µm
[114]	current-mode	0.7	3.3	52	10	6	IM3 $= 40$ dB @ $I_{in} = 55$ µA	2 µm
[148]	current-mode	0.075	1.5	67	0.3–1	5	THD: -40 dB @ $I_{in} = 4$ µA	1.2 µm

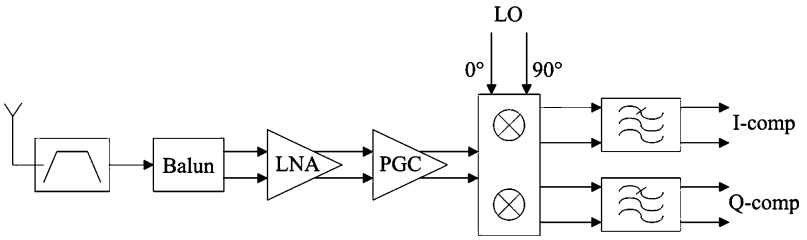


Fig. 5.5 UWB receiver block diagram

5.4 Requirements for the Implemented G_m-C Filters and Applications in Ultra-Wideband

Ultra-wideband (UWB) is a communication technology which can be used for short-range high-bandwidth communications. It allows data rates up to 480 Mb/s in the frequency spectrum of 3 to 10 GHz. It utilizes a large portion of the radio spectrum in a way that it does not interfere with other more traditional narrow band uses. A signal is UWB if its bandwidth is large with respect to the carrier or center frequency of the spectrum (i.e. the fractional bandwidth $(f_h - f_l)/[(f_h + f_l)/2] > 0.2$.

Due to the precision capabilities combined with the low power it is applicable for environments such as hospitals and healthcare. Furthermore UWB can also be used between digital camera, mobile phones, PC or as a general USB-cable replacement, also called wireless USB. An introduction to the UWB standard can be found in [94]. The block diagram of a typical UWB receiver is shown in Fig. 5.5. After the input filter a balun follows which converts the single-ended signal into a fully differential signal. Generally, in a fully differential design, a high power-supply rejection ratio (PSRR) and a high common-mode rejection ratio (CMRR) can be achieved as well as the even-order distortions are eliminated. In mixed-signal or system on chip designs, fully differential structures are important for reducing interference and noise from digital circuits on the same chip. The LNA (low-noise amplifier) is followed by a PGC (programmable-gain control). The Gilbert-type down-conversion mixer generates the quadrature (I and Q) outputs.

For an UWB system a filter with the following parameters is required:

- f_C = 250 MHz
- THD $\leq$ 1 % respectively IM3 better than -40 dB for 200 mV_p output swing
- fully differential design
- mismatch between 2 identical filters: $\leq$0.1 dB in the amplitude and $\leq 1^\circ$ in the phase

5.5 Architectures of G_m-C Filters

The usual way to implement high order filters is the cascade connection of 1st-order and 2nd-order filters due to the modularity of structure and simplicity. The

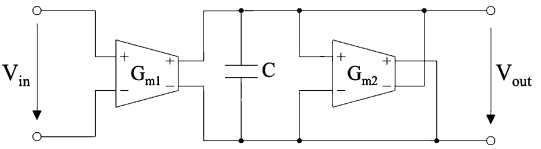


Fig. 5.6 1st-order filter

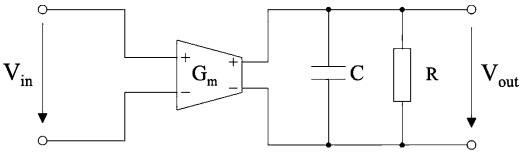


Fig. 5.7 Simple 1st-order filter

realization of a 1st-order G_m-C filter is shown in Fig. 5.6. The transfer function is given by

$$H(s) = \frac{G_{m1}}{G_{m2}} \cdot \frac{1}{1 + sC/G_{m2}} \tag{5.7}$$

The transconductor G_{m2} can be substituted by a resistor (see Fig. 5.7). The transfer function can be calculated to

$$H(s) = \frac{G_m \cdot R}{1 + s \cdot RC} \tag{5.8}$$

In Fig. 5.8 the G_m-C topology of a 2nd-order filter is shown. It consists of an ideal integrator (G_{m1}, C_1) and a lossy integrator (G_{m2}, C_2, R_2). This structure can be generated by an OTA-C simulation of resistor and inductor of a passive RLC resonator.

The transfer function of this 2nd-order filter can be derived by

$$H(s) = \frac{A\omega_0^2}{s^2 + \omega_0/Q \cdot s + \omega_0^2} \tag{5.9}$$

with the filter parameters

$$A = \frac{G_{m0}}{G_{m1}}, \qquad \omega_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}}, \qquad Q = \sqrt{\frac{C_2}{C_1}G_{m1}G_{m2}\ R^2} \tag{5.10}$$

As can be seen from (5.9), the filter gain A can be tuned independently of the quality factor Q, and the resonance frequency ω_0 and the quality factor can be tuned independently of the resonance frequency. An important aspect is now the influence of the nonideal parameters of the OTA to the filter transfer function. In general, a lot of parasitics and finite OTA bandwidth can affect the filter performance. Usually, the parasitic capacitances can be absorbed into the circuit capacitances. This absorption approach determines the real component values by subtracting the parasitic induced increments from the nominal values. This requires that the nominal values should be much larger than the total of the related parasitic capacitances. But at very high frequencies this may not always be possible. Under the assumption that

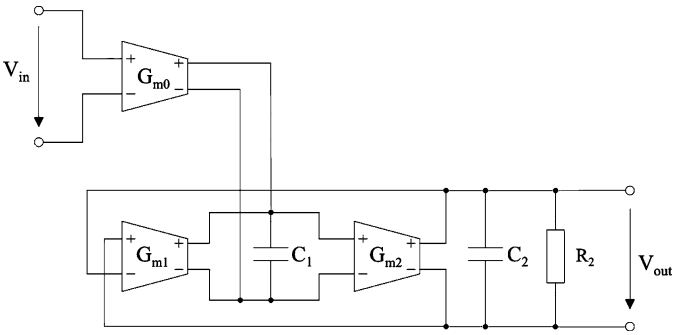


Fig. 5.8 2nd-order filter

all transconductances in the filter circuit in Fig. 5.8 are equal, the changed quality factor Q' can be derived from [102] to

$$Q' = \frac{Q}{1 + 2(1/A_0 - \Phi_E)Q} \tag{5.11}$$

where A_0 denotes the voltage DC-gain of the OTA and Φ_E is the excess phase at the filter cut-off frequency which is defined in (4.3). As can be seen clearly, the excess phase increases the quality factor. Under the assumption that the changed quality factor Q' is maximally increased by 20 % the following condition is necessary

$$(1/A_0 + \Phi_E) \leq 0.125 \tag{5.12}$$

If $A_0 = 30$ is assumed, an excess phase Φ_E of 5.25° at maximum is allowed.

5.6 Implemented Circuits

5.6.1 Realized G_m-C Filter 1

A 3rd-order filter was realized by a cascade connection of a second-order filter and a first-order filter [58]. The filter architecture is shown in Fig. 5.9. The transconductors were realized in the same way as described in Sect. 4.6 (the representation is shown in Fig. 4.14). For the transconductors G_{m0}, G_{m1} only one common-mode feedback together was used. To achieve the exact filter parameters a digitally programmable concept is developed. Figure 5.10 shows the circuit which switches at the output of the OTA (the transistor M_{out} is the n-channel output transistor of the OTA $=$ M_{11} and M_{12} in Fig. 4.14) 2 further stages (it can be extended to several stages) in parallel. The stages are activated when the corresponding data signal is high. The transistors $M_{2,j}$, $M_{3,j}$, $M_{4,j}$ are used to turn off the transistors $M_{1,j}$. The resistor R reduces the influence of the gate-drain capacitance of $M_{1,x}$ on the gate of M_{out}. In the second-order filter the transconductances G_{m0}, G_{m1}, G_{m2} are varied in the same way by 3 bits or 8 different steps. Therefore the cut-off frequency of the filter can

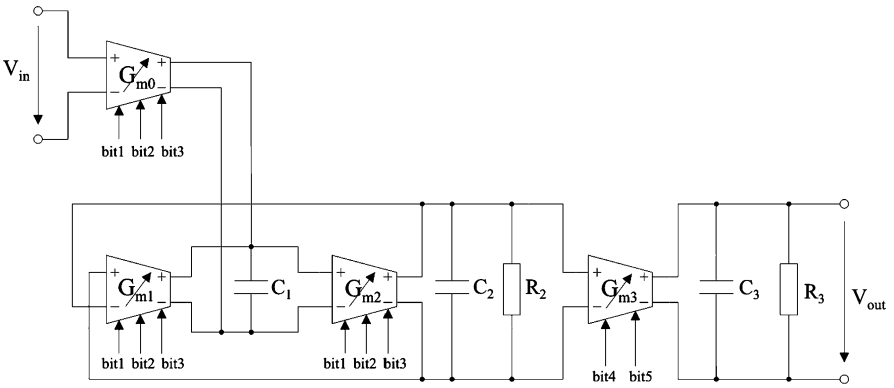


Fig. 5.9 Realized filter

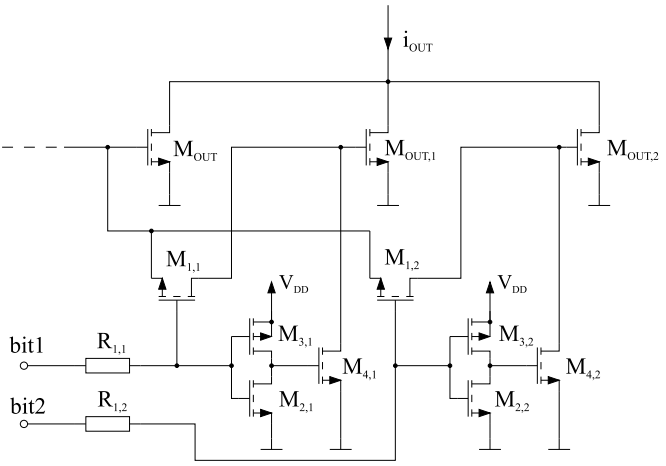


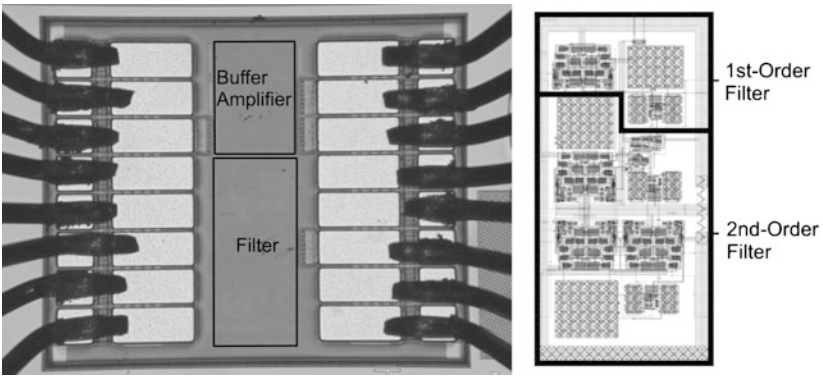
Fig. 5.10 Digitally programmable concept for the gain of the OTA

be varied by 8 steps. The gain of the filter is varied with G_{m3} by 2 bits in 4 different steps.

In Fig. 5.11(a) and 5.11(b) the chip photograph and the layout plot of the realized chip are shown. All capacitors were realized as metal-metal capacitors. The chip area of the whole chip is 650 µm × 540 µm, the chip area of the filter is 270 µm × 140 µm. The measured current consumption is 16.4 mA at a supply voltage of 1.5 V.

Figure 5.12 shows the measured DC transfer characteristics. For a differential input voltage of ±500 mV the curve is linear.

In Fig. 5.13 the amplitude frequency response of the filter, where the gain of the filter is varied and the cut-off frequency is constant, is shown. The gain of the filter is varied by 2 dB in 4 different steps, while the phase response of these four filter characteristics are identical.



(a) Chip photograph of the whole chip

(b) Layout plot of the filter and the buffer amplifier

Fig. 5.11 Realized chip

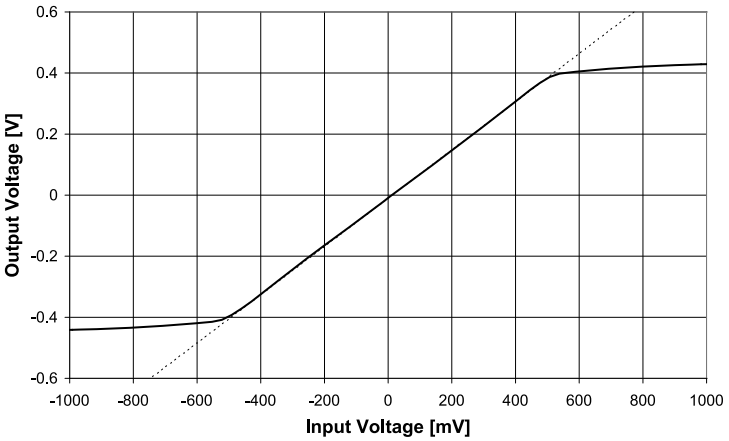


Fig. 5.12 DC-transfer characteristics of the realized filter

In Fig. 5.14(a) the amplitude frequency response and in Fig. 5.14(b) the phase frequency response for the constellation with minimum cut-off frequency (258 MHz) and for maximum frequency (355 MHz) is shown. The amplitude frequency response falls with −60 dB/decade in the cut-off region.

In Table 5.2 the measured differential spectral components of a single-tone measurement with an input frequency of $f_C = 50$ MHz are presented.

In Fig. 5.15 the output spectral components for a two-tone measurement with the frequencies $f_1 = 215$ MHz and $f_2 = 220$ MHz. Both spectral components have an differential output voltage of 200 mV_{pp} (= −10 dBm) is depicted. It shows that IM3 is −40 dB which gives an OIP3 of 10 dBm.

Table 5.3 summarizes the measured results from the realized chip.

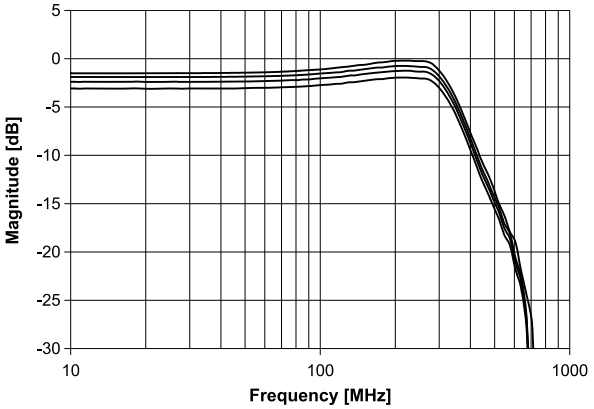
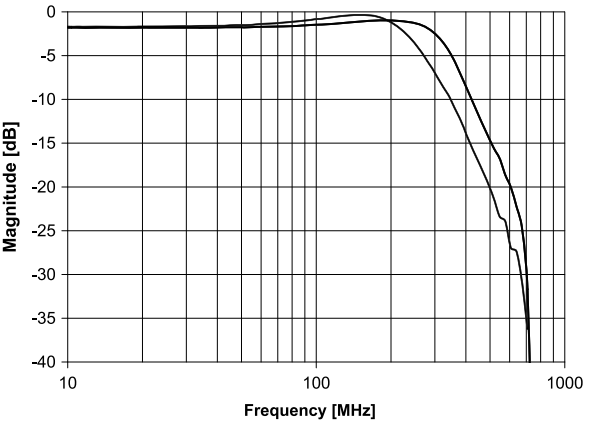
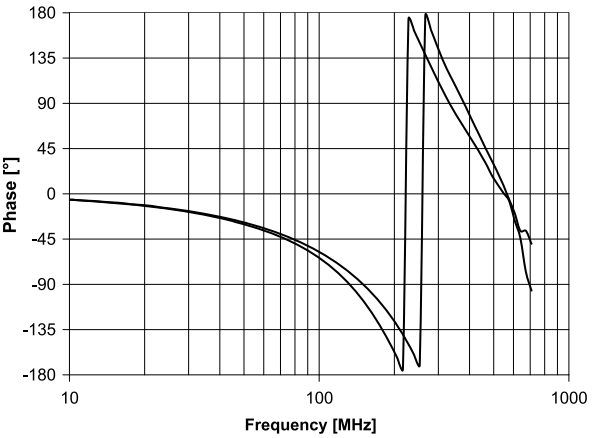


Fig. 5.13 Amplitude frequency response for different gain configurations



(a) Amplitude frequency response of the realized filter



(b) Phase frequency response of the realized filter

Fig. 5.14 Frequency response for the filter with maximum and minimum cut-off frequency

Table 5.2 Measured harmonics of the output signal

f	HD [dB] $V_{out} = 400\ \mathrm{mV}_{pp}$	HD [dB] $V_{out} = 600\ \mathrm{mV}_{pp}$
$2f_C$	−45.2	−42.3
$3f_C$	−44.0	−37.8
$4f_C$	−62.0	−58.4
$5f_C$	−59.0	−56.6

Fig. 5.15 Two-tone measurement

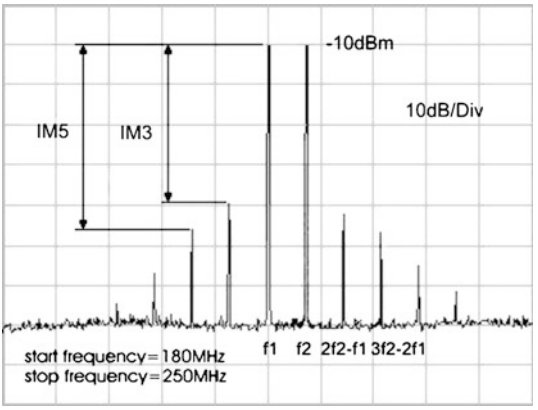


Table 5.3 Properties of the 3rd-order filter

Technology	120 nm CMOS
Voltage supply	1.5 V
Current consumption	16.4 mA
Power consumption per pole	8.20 mW
Cut-off frequency	258–355 MHz
Area of the filter	270 µm × 140 µm
IIP3	12 dBm
1 % THD	405 mV_{pp}
Output spectral noise density	74 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$
Integrated output noise	1.67–1.87 mV_{rms}
Dynamic range	43.7–44.7 dB

5.6.2 Realized G_m-C Filter 2

The OTA from the previous section can be extended by using a regulated cascode in the output stages (see Fig. 5.16). In general, a cascode increases the output impedance by the voltage gain ($= g_m \cdot r_{DS}$) of the transistor. The configuration in Fig. 5.16 is a controlled cascode where no other bias voltages for the cascode transistors are necessary. The transistors M_{casc1}–M_{casc4} are the cascode transistors, the

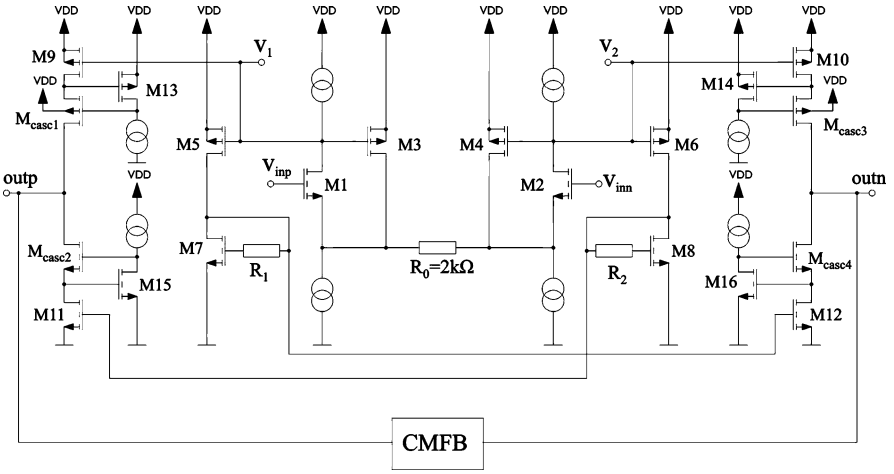


Fig. 5.16 OTA with cascodes at the output

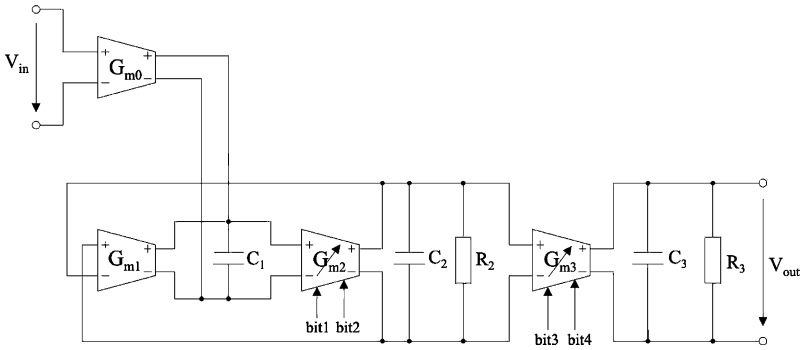
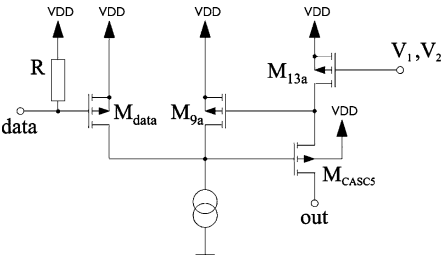


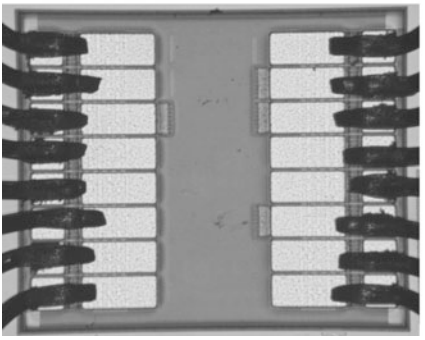
Fig. 5.17 Filter architecture of the realized filter

Fig. 5.18 Digitally programmable concept (see also Fig. 5.16)

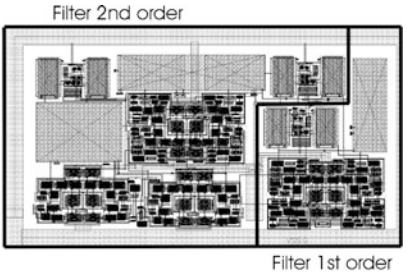


transistors M_{13}–M_{16} with the appended current sources define the operating points for the cascode transistors.

The circuit for the digitally programmable concept is shown in Fig. 5.18. At the output two other output stages with controlled cascodes are in parallel which can be



(a) Chip photograph of the whole chip



(b) Layout plot of the filter and the buffer amplifier

Fig. 5.19 Realized chip

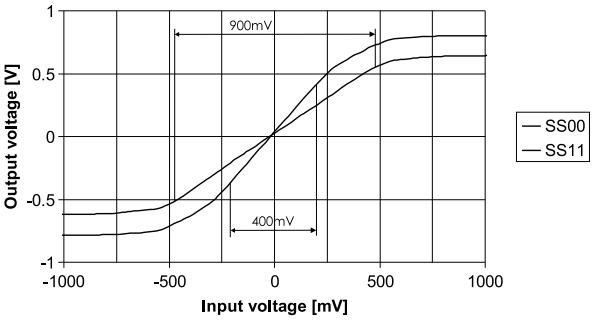


Fig. 5.20 DC-transfer characteristics for the case of maximum gain and minimum gain

activated by a digital signal. If the transistor M_{data} is turned on, the cascode with the transistor M_{casc5} is not activated and so no current flows through it. In addition, this avoids having to insert switches in the high-frequency signal path.

The architecture of the realized filter [57] is shown in Fig. 5.17. For two transconductors (G_{m0}, G_{m2}) a digitally programmable concept was developed. With the transconductor G_{m0} the quality factor and the filter cut-off frequency and with the transconductor G_{m2} the gain of the filter can be tuned in 4 different steps (see (5.10)).

In the Figs. 5.19(a) and 5.19(b) the chip photograph and the layout plot of the realized filter are shown. All capacitors were realized as metal-metal capacitors. The chip area of the whole chip is 850 µm × 550 µm, the chip area of the filter is 270 µm × 140 µm. The measured current consumption of the filter is 13.1 mA at $V_{DD} = 1.5$ V.

Figure 5.20 shows the measured DC transfer characteristics for the case of minimum and maximum gain. The curve is linear for an input voltage range of 900 mV for minimum gain and 400 mV for maximum gain.

In Fig. 5.21 the amplitude frequency response of the filter for the constellation with the same gain and different quality factors is shown. The filter characteristics

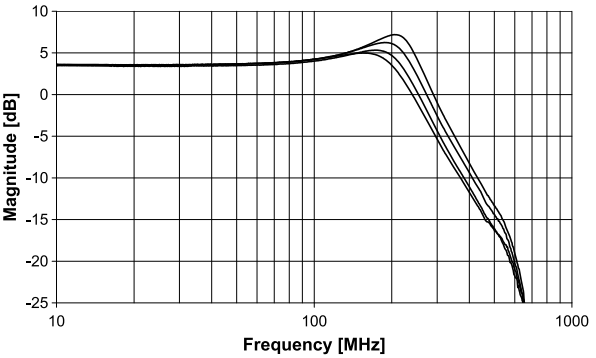


Fig. 5.21 AC-transfer characteristics for different quality factors

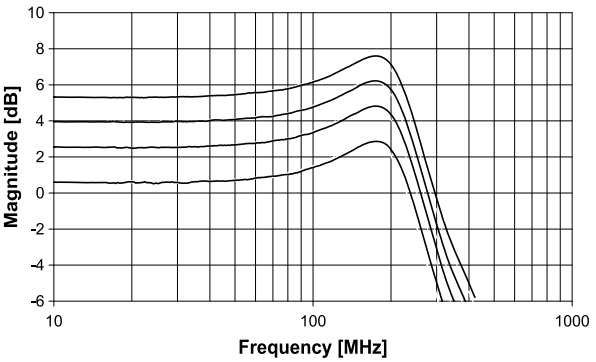


Fig. 5.22 AC-transfer characteristics for different gains

Table 5.4 Measured harmonics for an output voltage of 400 mV_{pp}

f	HD [dB] max. gain	HD [dB] min. gain
$2f_C$	−57.1	−56.2
$3f_C$	−48.1	−43.0
$4f_C$	−66.3	−62.0
$5f_C$	−56.0	−49.7

falls with −60 dB/decade in the cutoff region, the peak has a height of 1.43 dB, 1.71 dB, 2.65 dB, 3.58 dB and the −3 dB cut-off frequency is between 235 MHz and 285 MHz.

The gain of the filter is varied by 5 dB in 4 steps in measurement (see Fig. 5.22), whereby the phase responses of these four filter characteristics are identical.

In Table 5.4 the measured spectral components for a single-tone measurement with an input frequency of $f_C = 50$ MHz and a differential output voltage of 400 mV_{pp} for the constellation with minimum and maximum gain is shown.

For a 2-tone measurement the measured IM3 (input frequencies were 215 MHz and 220 MHz) at an output voltage for both spectral components of 200 mV_{pp} is −46.5 dB for the case with maximum gain and −41 dB for the case with minimum

Table 5.5 Total integrated output noise

f_C [MHz]	$V_{n,rms}$ [mV] min. gain	$V_{n,rms}$ [mV] max. gain
234	1.12	1.58
248	1.15	1.61
268	1.17	1.64
285	1.20	1.68

Table 5.6 Properties of the 3rd-order filter

Technology	120 nm CMOS	
Voltage supply	1.5 V	
Current consumption	13.1 mA	
Power consumption per pole	6.55 mW	
Cut-off frequency	235–285 MHz	
Area of the filter	270 µm × 140 µm	
Configuration	min. gain	max. gain
Gain	0.7 dB	5.2 dB
IIP3	10.5 dBm	13 dBm
Output spectral noise density	63 nV/$\sqrt{\text{Hz}}$	89 nV/$\sqrt{\text{Hz}}$
Integrated output noise	1.12–1.20 mV_{rms}	1.58–1.68 mV_{rms}
Dynamic range	45.4–45.7 dB	44.7–44.9 dB

gain. This gives an OIP3 of 1.41 V_p (= 13 dBm) for the case with minimum gain and 0.75 V_p (= 10.5 dBm) for the case with maximum gain.

The simulated output spectral noise density is 63 nV/$\sqrt{\text{Hz}}$ for the case with minimum gain and 89 nV/$\sqrt{\text{Hz}}$ for the case of maximum gain. In Table 5.5 the total integrated noise for the different filter configurations are presented.

Table 5.6 summarizes the measured results from the realized chip.

5.6.3 Realized G_m-C Filter 3

In this chip [59] no push-pull stage at the output of the OTA was used (see Fig. 5.23). So the current consumption is reduced because one stage less is used. In contrast to the OTAs in the previous filters here the flipped version is used. This has the consequence that the input transistors are PMOS transistors which have a better noise performance than NMOS transistors. In Fig. 5.24 the architecture of the G_m-C filter is shown. For the transconductors G_{m0}, G_{m1}, G_{m2} the same G_m-cells are used and it should be noticed that for G_{m0}, G_{m1} only one CMFB together was used. For common-mode signals the closed loop consisting of G_{m1} and G_{m2} gives a positive feedback. So the closed-loop common-mode gain must be smaller than 1. This can

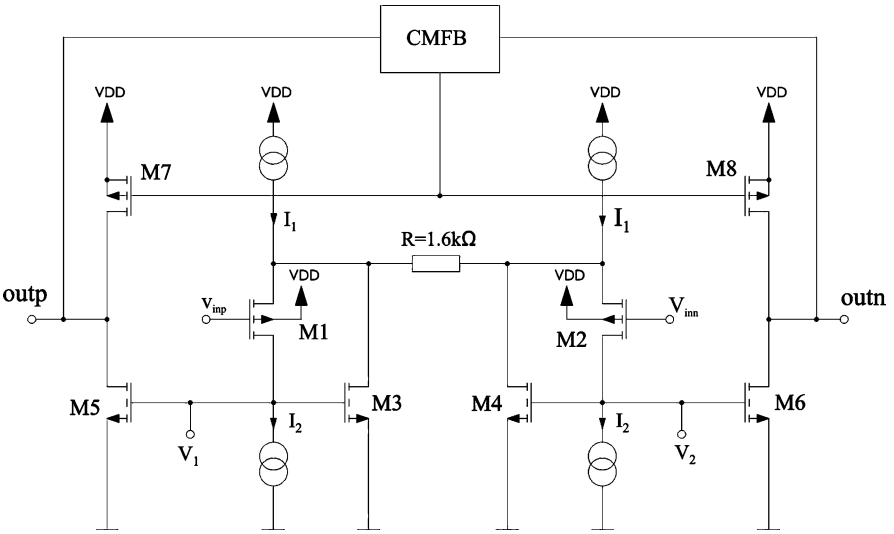


Fig. 5.23 OTA without push-pull stage

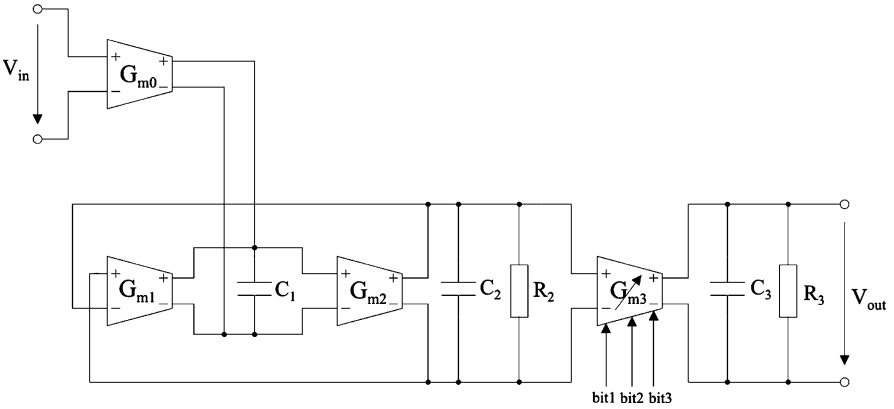


Fig. 5.24 Realized filter

be guaranteed if the output resistances of the transistors M_7–M_8 are quite large. So with large transistor lengths ($L = 480$ nm) the loop is kept stable.

To achieve the exact gain a digitally programmable concept was developed. The transconductor of the first-order filter (G_{m3} is programmable by a digital word in 8 different steps (the output stage is shown in Fig. 5.25. For each output stage a controlled cascode was utilized to increase the output impedance. The W/L ratio of the transistors is half of the W/L ratio of the previous stage, e.g. $(\text{W/L})_{M5,1} = (\text{W/L})_{M5}/2$ which means that the transconductance can be programmed in a dyadic way (the ratio between maximum gain and minimum gain is $1.875 \mathrel{\hat{=}} 5.46$ dB). For verifying the on-chip process variations two identical filters were realized on

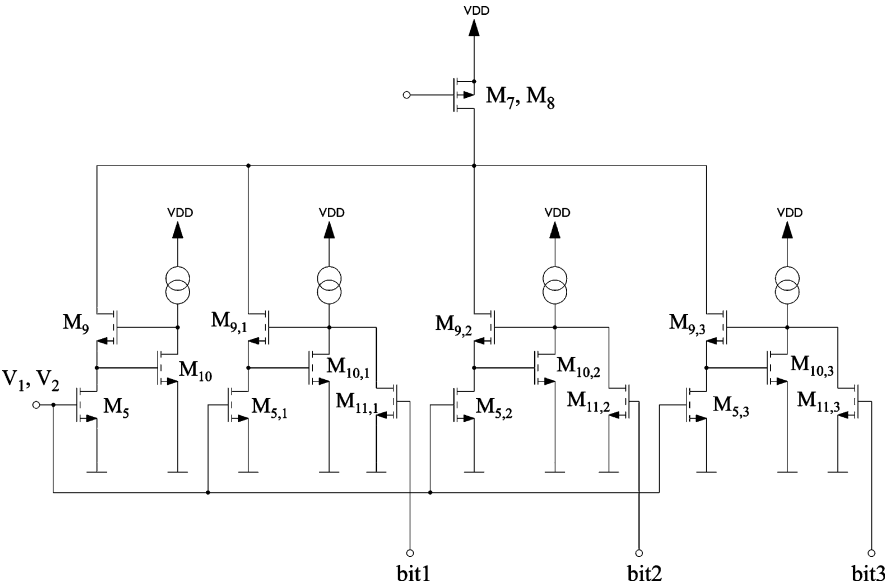
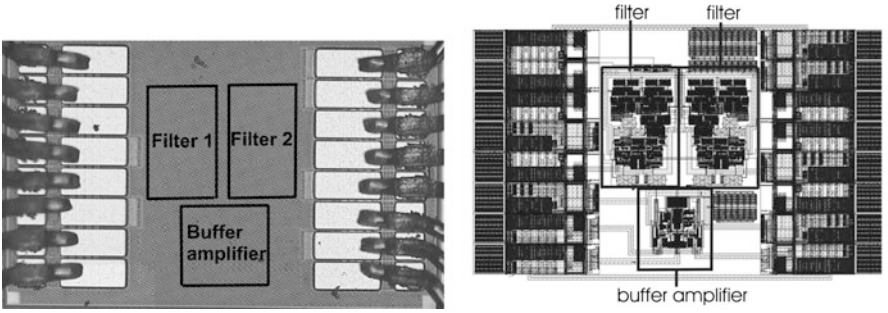


Fig. 5.25 Output stage of the digitally programmable OTA G_{m3}



(a) Chip photomicrograph of the chip (b) Layout plot of the whole chip

Fig. 5.26 Realized chip

one chip. In Fig. 5.26(a) the photomicrograph and in Fig. 5.26(b) the layout of the realized chip is shown. All capacitors were realized as metal-metal capacitors.

Figure 5.27 shows the measured differential DC transfer characteristics for the maximum and minimum gain configuration. The curve is linear for a differential input voltage of ± 350 mV.

Figure 5.28 shows the measured amplitude frequency response of the filter for maximum and minimum gain configuration. The resonance peak is 1 dB, the -3 dB cut-off frequency is 235 MHz. In Fig. 5.29 all different gain configurations are shown. The gain can be varied from 0.4 dB to -5 dB.

In Fig. 5.30 the measured phase frequency response of this filter is shown.

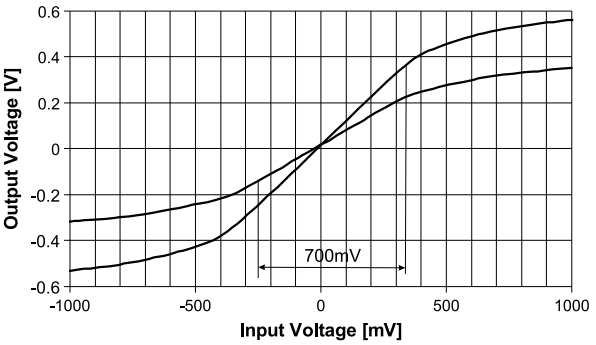


Fig. 5.27 Measured DC-transfer characteristics for maximum gain and minimum gain configuration

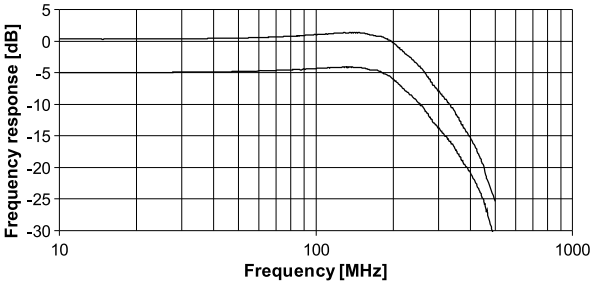


Fig. 5.28 Measured magnitude frequency response for maximum gain and minimum gain configuration

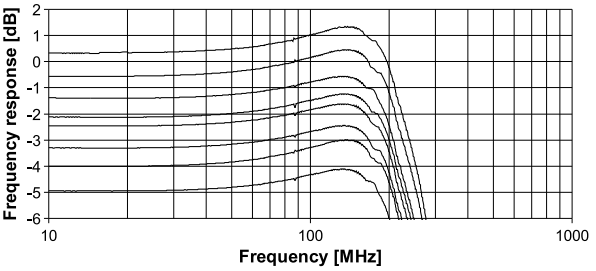


Fig. 5.29 Measured magnitude frequency response (zoomed)

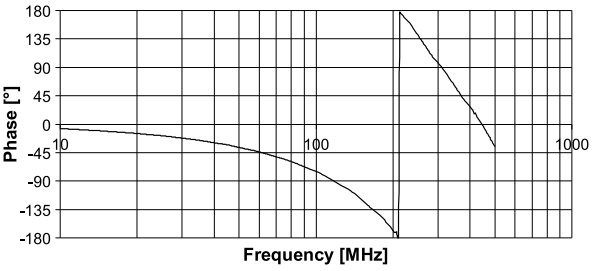


Fig. 5.30 Measured phase frequency response

In Table 5.7 the measured differential spectral components for single-tone measurements with an input frequency of $f_{in} = 50$ MHz and a differential output voltage of 400 mV_{pp} (= 391 mV_{pp} at the input for maximum gain and 711 mV_{pp} for mini-

Table 5.7 Measured harmonics for an output voltage of 400 mV_{pp}

f	HD [dB] max. gain	HD [dB] min. gain
$2f_C$	−61.5	−61
$3f_C$	−49.2	−43.0
$4f_C$	−67.0	−62.0
$5f_C$	−58.0	−49.7

Table 5.8 Properties of the 3rd-order filter

Technology	120 nm CMOS	
Voltage supply	1.5 V	
Current consumption	9.5 mA	
Power consumption per pole	4.75 mW	
Cut-off frequency	235 MHz	
Area of the filter	230 µm × 150 µm	
Configuration	min. gain	max. gain
Gain	−5 dB	0.4 dB
IIP3	21.0 dBm	17.6 dBm
Output spectral noise density	59 nV/$\sqrt{\text{Hz}}$	105 nV/$\sqrt{\text{Hz}}$
Integrated output noise	1.11 mV_{rms}	1.58 mV_{rms}
Dynamic range	48.1 dB	47.5 dB

mum gain) are presented. The IM3 is for a two-tone output signal of 200 mV_{pp} each (at 180 MHz and 190 MHz) −40 dB for the case of minimum gain and −44 dB for the case of maximum gain. This corresponds to an IIP3 of 21.0 Bm and 17.6 dBm.

The simulated noise spectral density at the filter output is 59 nV/$\sqrt{\text{Hz}}$ for the case with minimum gain and 105 nV/$\sqrt{\text{Hz}}$ for the case of maximum gain. This gives a total integrated noise of 1.11 mV_{rms} at the output for the case with minimum gain and 1.85 mV_{rms} for the case with maximum gain.

Table 5.8 summarizes the measured results from the realized chip.

5.7 Considerations about Mismatch

The impact of mismatch becomes more severe with the trend of reducing supply voltage. Characterization of mismatch is crucial for precision analog design. The large sensitivity of all classes of circuits to mismatch makes it necessary to have very precise estimates of mismatch. When the same filter is used in the I-path and Q-path (see Fig. 5.5), the mismatch between the two filters plays also an important role. To quantify the mismatch of two identical filters the relative sensitivity of the transfer function H (defined in [111]) is used. It is calculated to

$$\Delta H/H = \frac{1}{H} \cdot \left(\sum \frac{\partial H}{\partial G_{m,i}} \Delta G_{m,i} + \sum \frac{\partial H}{\partial C_j} \Delta C_j + \sum \frac{\partial H}{\partial R_k} \Delta R_k \right) \tag{5.13}$$

If a 3-rd order filter from the previous sections is assumed with the transfer function (see (5.8), (5.9), (5.10))

$$H(s) = \frac{\frac{G_{m0}G_{m2}}{C_1C_2}}{s^2 + s\frac{C_2}{R} + \frac{G_{m1}G_{m2}}{C_1C_2}} \cdot \frac{G_{m3}R_3}{1 + sR_3C_3} \tag{5.14}$$

and the mismatch of each device is described with the standard deviation, the relative sensitivity is calculated to

$$\begin{aligned}\sigma^2_{|\Delta H/H|} = {} & \sigma^2_{\Delta Gm0/Gm0} + \left|\frac{\omega_0^2}{N}\right|^2 \sigma^2_{\Delta Gm1/Gm1} + \left|1 - \frac{\omega_0^2}{N}\right|^2 \sigma^2_{\Delta Gm2/Gm2} \\ & + \left|\frac{\omega_0^2}{N} - 1\right|^2 \sigma^2_{\Delta C1/C1} + \left|\frac{\omega_0^2}{N}\right|^2 \sigma^2_{\Delta C2/C2} + \left|\frac{s\omega_0/Q}{N}\right|^2 \sigma^2_{\Delta R2/R2} \\ & + \sigma^2_{\Delta Gm3/Gm3} + \left|\frac{1}{1 + sR_3C_3}\right|^2 \sigma^2_{\Delta R3/R3} + \left|\frac{sR_3C_3}{1 + sR_3C_3}\right|^2 \sigma^2_{\Delta C3/C3}\end{aligned} \tag{5.15}$$

with

$$N = s^2 + s\frac{\omega_0}{Q} + \omega_0^2 \tag{5.16}$$

For frequencies much smaller than the cut-off frequency ($|s| \ll \omega_0$) it can be estimated that

$$\frac{\omega_0^2}{N} \approx 1, \qquad \frac{1}{1 + sR_3C_3} \approx 1 \tag{5.17}$$

and so the relatively sensitivity results in

$$\sigma^2_{\Delta H} = \sigma^2_{\Delta Gm0/Gm0} + \sigma^2_{\Delta Gm1/Gm1} + \sigma^2_{\Delta C2/C2} + \sigma^2_{\Delta Gm3/Gm3} + \sigma^2_{\Delta R3/R3} \tag{5.18}$$

For frequencies which are in the range of the cut-off frequency ($|s| \approx \omega_0 \approx 1/(R_3C_3)$) it can be estimated that

$$\frac{\omega_0^2}{N} \approx -jQ, \qquad \frac{1}{1 + sR_3C_3} = \frac{1}{1 + j} = \frac{1}{2} - j\frac{1}{2} \tag{5.19}$$

and so the relative sensitivity is separated into the real part and the imaginary part

$$\begin{aligned}\sigma^2_{\Delta H,real/H} = {} & \sigma^2_{\Delta Gm0/Gm0} + \sigma^2_{\Delta Gm2/Gm2} + \sigma^2_{\Delta C1/C1} + \sigma^2_{\Delta R2/R2} \\ & + \sigma^2_{\Delta Gm3/Gm3} + \frac{1}{4}\sigma^2_{\Delta R3/R3} + \frac{1}{4}\sigma^2_{\Delta C3/C3}\end{aligned} \tag{5.20}$$

$$\begin{aligned}\sigma^2_{\Delta H,imag/H} = {} & Q^2\sigma^2_{\Delta Gm1/Gm1} + Q^2\sigma^2_{\Delta Gm2/Gm2} + Q^2\sigma^2_{\Delta C1/C1} \\ & + Q^2\sigma^2_{\Delta C2/C2} + \frac{1}{4}\sigma^2_{\Delta R3/R3} + \frac{1}{4}\sigma^2_{\Delta C3/C3}\end{aligned} \tag{5.21}$$

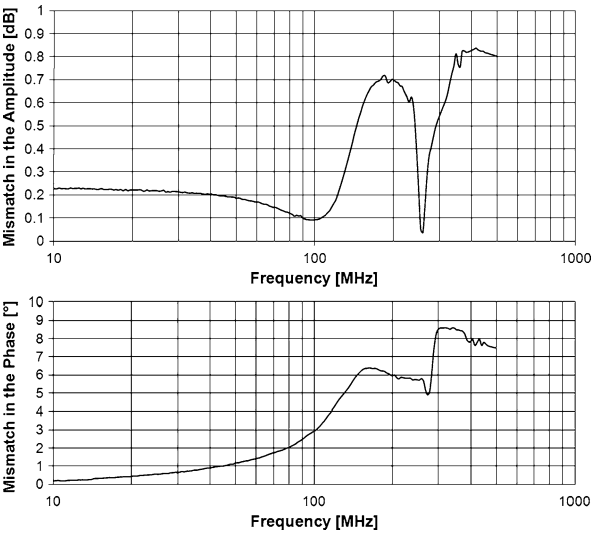


Fig. 5.31 Measured frequency response of the mismatch

To describe now the influence of mismatch in the amplitude it is necessary to add the real and the imaginary part in a quadratic way like

$$\sigma^2_{|\Delta H/H|} = \sqrt{\left(\sigma^2_{\Delta H,real/H}\right)^2 + \left(\sigma^2_{\Delta H,imag/H}\right)^2} \tag{5.22}$$

This is a difficult task because the final probability density function is not a Gaussian function any more. But it is obvious that the mismatch will increase with the quality factor of the filter.

The mismatch of the phase can be calculated as

$$\sigma_{angle(\Delta H/H)} = \arctan\left(\sigma^2_{\Delta H,imag/H}/\sigma^2_{\Delta H,real/H}\right) \tag{5.23}$$

To evaluate this, is a difficult task because the final probability density function is not a Gaussian function any more. But it is obvious that the mismatch will also increase with the quality factor of the filter.

For frequencies above the range of the cut-off frequency ($|s| \gg \omega_0$) it can be estimated that

$$\frac{\omega_0^2}{N} \approx 0, \qquad \frac{1}{1 + sR_3C_3} \approx 0 \tag{5.24}$$

$$\sigma^2_{\Delta H/H} = \sigma^2_{\Delta Gm0/Gm0} + \sigma^2_{\Delta Gm2/Gm2} + \sigma^2_{\Delta C1/C1} + \sigma^2_{\Delta Gm3/Gm3} + \sigma^2_{\Delta C3/C3} \tag{5.25}$$

In the Figs. 5.31(a) and 5.31(b) the measured mismatch between the two realized filters is shown. As discussed in the previous equations, the sensitivity of the filter is highest in the passband at the frequency where the AC frequency response has its maximum. The maximum deviation in the passband is 0.7 dB in the amplitude and 7° in the phase.

Table 5.9 Figure-of-merit comparison

Citation	Technology (CMOS)	V_{DD} [V]	Architecture	FOM_1* [1]	FOM_3** [(Hz/W)^2]	FOM_{own}* [1/Hz]
[16]	0.35 µm	2.3	g_m-C	42864	$1.23 \cdot 10^{26}$	$5.36 \cdot 10^{-4}$
[17]	0.18 µm	1.8	g_m-C	180	$3.55 \cdot 10^{30}$	$4.47 \cdot 10^{-7}$
[20]	0.18 µm	1.8	source-follower based	38	$3.01 \cdot 10^{29}$	$3.88 \cdot 10^{-6}$
[145]	0.18 µm	1.5	g_m-C	1528	$4.88 \cdot 10^{26}$	$3.06 \cdot 10^{-2}$
[35][1]	0.13 µm	1.2	active-g_m-C RC	12152	$7.71 \cdot 10^{26}$	$1.10 \cdot 10^{-3}$
[35][1]	0.13 µm	1.2	active-g_m-C RC	34274	$4.64 \cdot 10^{25}$	$3.43 \cdot 10^{-2}$
[132]	0.12 µm	1.5	opamp	635	$4.46 \cdot 10^{27}$	$1.27 \cdot 10^{-4}$
[114]	2 µm	3.3	current-mode	13335	$1.28 \cdot 10^{27}$	$1.33 \cdot 10^{-3}$
[148]	1.2 µm	1.5	current-mode	1506	$3.16 \cdot 10^{27}$	$5.02 \cdot 10^{-3}$
[86]	0.35 µm	2	current-mode g_m-C	3378	$1.58 \cdot 10^{28}$	$1.57 \cdot 10^{-5}$
Own work						
[58]	0.12 µm	1.5	g_m-C (1)	23631	$2.18 \cdot 10^{27}$	$6.65 \cdot 10^{-5}$
[57]	0.12 µm	1.5	g_m-C (2)	22295	$2.04 \cdot 10^{27}$	$8.91 \cdot 10^{-5}$
[59]	0.12 µm	1.5	g_m-C (3)	9672	$6.09 \cdot 10^{27}$	$4.12 \cdot 10^{-5}$
[62]	0.12 µm	1.5	current-mode and opamp filter	1342	$2.83 \cdot 10^{27}$	$3.23 \cdot 10^{-4}$
[61]	65 nm	1.2	current-mode and opamp filter	92918	$2.29 \cdot 10^{25}$	$2.48 \cdot 10^{-2}$
[60]	65 nm	1.2	current-mode g_m-C	4425	$4.02 \cdot 10^{26}$	$1.09 \cdot 10^{-3}$

*The lower the value for *FOM* is, the better the circuit is

**The higher the value for *FOM* is, the better the circuit is

[1]Two different filters were realized on one chip

5.8 Comparison with the State-of-the-Art

Generally, it is difficult to make a fair comparison considering the different properties of filters like cut-off frequency, dynamic range, output swing, et cetera. As discussed in Sect. 5.2, there exist several *FOM*s for analog filters. To make a fair comparison especially for high-frequency filters, a new *FOM* is introduced which is an extended version of (5.2)

$$FOM_{own} = FOM_1 \cdot \frac{1}{f_C} = \frac{P}{8k_B T \cdot f_C \cdot N \cdot DR} \cdot \frac{1}{f_C} \tag{5.26}$$

This *FOM* has the advantage that f_C plays a more important role. In FOM_1 (5.2), the product of DR ($= v^2_{signal,1\,\%}/v^2_{noise} \propto 1/f_C$) and f_C is frequency independent which means that especially high-frequency filters achieve a worse *FOM* due to their higher power consumption. In contrast to FOM_3 (5.5), this *FOM* depends only

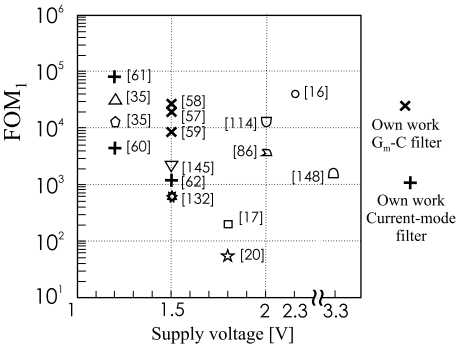


Fig. 5.32 Comparison with FOM_1 to state-of-the-art. The lower the value for FOM is, the better the filter is

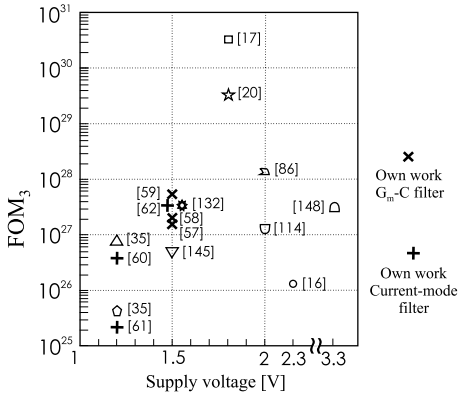


Fig. 5.33 Comparison with FOM_3 to state-of-the-art. The higher the value for FOM is, the better the filter is

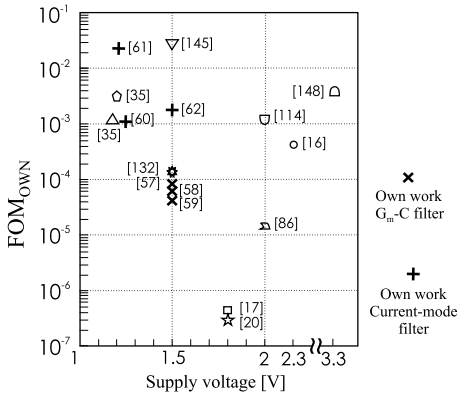


Fig. 5.34 Comparison with FOM_{own} to state-of-the-art. The lower the value for FOM is, the better the filter is

linearly on P. In Table 5.9 the realized filters are compared using different FOMs (FOM_1, FOM_3, FOM_{own}) with state-of-the-art filters. The FOMs versus the supply voltage are plotted in Figs. 5.32, 5.33, 5.34.

It should be noticed that in [4] it is explained that an analog design in 0.12 µm and in 65 nm CMOS leads to an increase in power dissipation at constant performance in comparison to 0.18 µm CMOS. So it is expected that the FOMs in 0.12 µm and

in 65 nm CMOS are worse than the *FOM*s of the published filters [17, 20, 145] in 0.18 µm CMOS. It should be noticed that the filter in [17] describes only simulated results. The drawback of the filter in [20] is that the range between passband and cut-off region is quite large that means that the quality factor of this filter is quite low. This 4th-order filter has at the 5.5-fold cut-off frequency an attenuation of only −30 dB.

For the comparison with published filters in the deep-submicron technology, the realized G_m-C filters have especially for FOM_3 and for FOM_{own} better values than the filters described in [16, 132, 145] and [35]. As seen in Fig. 5.32, especially with FOM_1 the realized G_m-C filters are underperformed due to their high cut-off frequencies. In contrast, FOM_{own} (see Fig. 5.34) delivers for the realized G_m-C filters the best results at a supply voltage of 1.5 V.

No current-mode filters in deep-submicron and ultra-deep-submicron technology can be found in the literature. So the comparison with published current-mode filters [86, 114, 148] can be done only with filters realized in submicrometer and micrometer technologies. But this should be treated with care because the gap is quite large to the deep-submicron and ultra-deep-submicron technology. For comparison with a voltage-mode filter in 0.13 µm CMOS [35], the realized current-mode filter in 65 nm CMOS with the G_m-C approach [60] achieves better *FOM*s. But it should be taken also into account, that in [80] it is explained that G_m-C topology voltage-mode filters have the better performance than current-mode filters. Another issue is also that the realized 65 nm CMOS current-mode filters in [61] and [60] have a virtual ground regulation which needs some power and degrades so the *FOM*s. No virtual ground regulation is used in the current-mode filters in [86, 114] and [148].

Chapter 6
Current-Mode Filters

Voltage-mode filters and especially their linearity and dynamic range suffer from the low supply voltages of deep-sub-micron and nanometer CMOS. This fact served as motivation to investigate current-mode filters with the hope for a better linearity and larger dynamic range. Current-mode filters also may allow saving of current-to-voltage and voltage-to-current converters compared to the case when voltage-mode filters are used in combination with current-mode mixer and current-steering digital-analog converter for instance. A lower power consumption then should be obtainable. This chapter will give on overview on current-mode filters described in literature and will introduce new current-mode filters designed in 120 nm CMOS and 65 nm low-power CMOS. Their properties are described in detail.

6.1 Current-Mode Technique

The application of current-mode signal processing has received remarkable attention and is investigated thoroughly. A strict separation of voltage-mode and current-mode circuits is not possible due to the inherent interrelation of voltage and current. A common classification of voltage-mode circuits is that system relevant signal quantities are represented by voltages. This is in contrast to current-mode circuits, where the important signal quantities are represented by currents [37].

Mixed-signal design in digital low-power nanometer CMOS technology implicates a reduction of the supply voltage and the threshold voltage. In order to keep the static power consumption of digital circuits within limits, the threshold voltage is not scaled by the same factor as the supply voltage (cf. Chap. 3). Concerning these limits there are some challenges in voltage-mode circuits. The low supply voltage makes it difficult to design voltage-mode circuits having high linearity and wide dynamic range [3]. As a consequence of the small supply voltage, voltage-mode circuits suffer increasingly of a small signal headroom and a small effective gate-source voltage ($V_{GS} - V_T$) [147]. It is more difficult to achieve high linearity and wide dynamic range circuits. In addition voltage-mode circuits limit signal bandwidth at the existence of high impedance nodes and have low output impedances.

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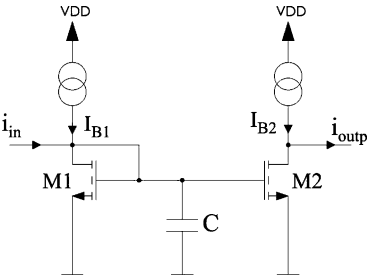


Fig. 6.1 Simplest current-mode filter

Current-mode circuits gain in importance and offer some advantages over voltage-mode counterparts. Signal quantities are represented by currents, which are not limited by the supply voltage. A wide dynamic range and a good linearity are achievable due to the supply voltage independent signal processing. They have potentially a higher bandwidth due to low impedance nodes [118] and stray-inductance effects show less impact on circuit performance. Low input impedances are important for high bandwidth applications. Current-mode circuits have potentially a high slew-rate and are less sensitive to power and ground fluctuations [147].

Signal processing in current-mode circuits is easy as well. Basic mathematical operations, like addition, subtraction, and multiplication by a constant are straightforward realized [98].

The profound investigations in current-mode circuits deliver a huge amount of current-mode applications [146]. Important developments are optical communications, magnetic recording systems, high-speed bus transceivers, analog-to-digital converters, high-frequency filters, and signal processing. These applications use basic building blocks like current conveyors, current feedback operational amplifiers, sampled data current circuits, or dynamic current mirrors.

6.2 Current-Mode Filters Based on Current Mirrors

The simplest single-ended current-mode filter consists of a current mirror and a capacitor (see Fig. 6.1). The transfer function of this filter is given by

$$H(s) = \frac{g_{m2}/g_{m1}}{1 + s \cdot C/g_{m1}} \tag{6.1}$$

Under the assumption that the transistors have a quadratic transfer curve, the 3rd harmonics can be calculated from [114] to

$$HD3 = \frac{1}{32} \cdot \left(\frac{i_{in}}{2I_{B1}}\right)^2 \tag{6.2}$$

A simple estimation gives now for $i_{in} = 250$ µA and $I_{B1} = 400$ µA a $HD3 = -50.3$ dB. This means that at least a DC-current of 400 µA is necessary to fulfill the specifications about distortions.

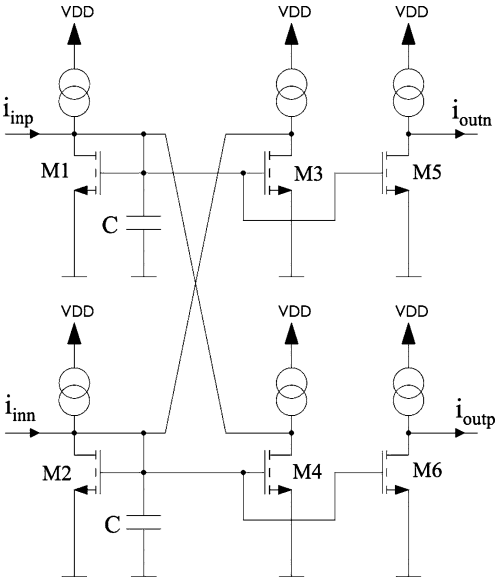


Fig. 6.2 Fully differential current-mode filter

A fully differential current-mode integrator can be realized by two cross-coupled one-to-one current mirrors and an integration capacitor (see Fig. 6.2). This cross interconnection between the current-mirrors provides a naturally high differential gain and a low common-mode gain. The transfer function of this filter is given by

$$H(s) = \frac{i_{outp}}{i_{inp}} = \frac{\frac{\alpha}{1-\alpha} \cdot \beta}{1 + s \cdot \frac{C}{g_{m1}} \cdot \frac{\alpha}{1-\alpha}} \tag{6.3}$$

where $\alpha = g_{m3}/g_{m1}$ and $\beta = g_{m5}/g_{m3}$. An ideal integrator can be realized if $g_{m1} = g_{m3}$ and the resulting transfer function is $g_{m5}/(sC)$.

This structure can now be extended by a resistor R as shown in Fig. 6.3 as an innovation. The transfer function of this filter is given by

$$H(s) = \frac{i_{outp}}{i_{inp}} = \frac{\frac{\alpha}{1-\alpha} \cdot \beta}{1 + s \cdot C \cdot (R + \frac{1}{g_{m1}}) \cdot \frac{1}{1-\alpha}} \tag{6.4}$$

The 3 dB cut-off frequency can be calculated to

$$f_C = \frac{1}{2\pi \cdot (R_1 + \frac{1}{g_{m1}}) \cdot C_1 \cdot \frac{1}{1-\alpha}} \tag{6.5}$$

Equation (6.5) shows that the capacitance C is virtually increased by the capacitance multiplication factor M

$$C_{eff} = \frac{1}{1-\alpha} \cdot C = M \cdot C \tag{6.6}$$

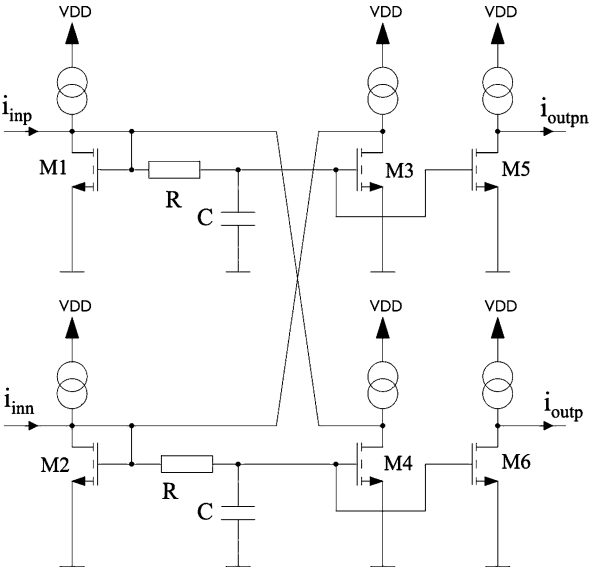


Fig. 6.3 Extended current-mode filter

So, with the resistor R the cut-off frequency of this filter can be decreased which leads to less capacitances and so less chip area. But it should be noticed that the signal current through the transistors M1 respectively M2 is also increased by the factor $\frac{1}{1-\alpha}$. This has also the consequence that the current sources must be scaled also with the same factor.

6.3 Filter Properties

Several parameters exist to evaluate the quality and performance of filters. In the following important and applied indicators are presented.

Power Consumption P The power consumption reflects the consumed energy of the filter.

Filter Order N The filter order is related to the width of the transition band. The higher the filter order, the smaller is the transition band, and the greater the effort in filter design is.

-3 dB Cut-Off Frequency f_c The -3 dB cut-off frequency resides where the signal power at the filter output is the half of the signal power in the pass-band.

Noise The minimum signal level, that a filter can handle, is dependent on the noise of the filter. The integrated in-band noise is denoted by $\overline{v_{\text{noise}}}$ for voltage noise and $\overline{i_{\text{noise}}}$ for current noise.

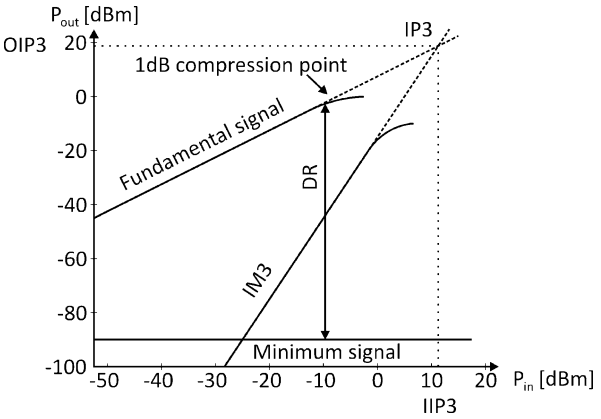


Fig. 6.4 Output power versus input power: IP3 and DR

1 dB Compression Point The 1 dB compression point is the power level, at which the output power level is 1 dB below the ideal output power level (compare Fig. 6.4).

Total Harmonic Distortions (THD) The total harmonic distortions are given at a single frequency excitation as the sum of the powers of the harmonic power components (P_2 to P_k, $k = 2 \ldots \infty$) to the power of the signal at the fundamental frequency (6.7). The harmonics occur at an integer multiple of the fundamental frequency.

$$THD = \frac{\sum_{k=2}^{\infty} P_k}{P_1} \tag{6.7}$$

At a dominant harmonic x the xth-order harmonics are specified and denoted as HD_x. HD_x is defined by the ratio of the power of the xth harmonic to the power of the fundamental frequency [44]. The THD can also be calculated by

$$THD = \sqrt{\sum_{x=2}^{\infty} HD_x^2}. \tag{6.8}$$

Intermodulation Distortion The excitation of a nonlinear system with two signals with the frequencies f_1 and f_2 cause intermodulation products. The frequencies of the modulation products can be derived by

$$Af_1 \pm Bf_2 \tag{6.9}$$

where the sum of A and B is the order of the intermodulation. The 3rd-order intermodulations (IM3) are commonly used and are defined by the output power at the frequencies $2f_1 \pm f_2$ and $2f_2 \pm f_1$.

Third-Order Intercept Point (IP3) The third-order intercept point is a theoretical point, where the signal amplitudes of the fundamental frequencies f_1 and f_2 are equal to the intermodulation products of these signals at the frequencies $2f_1 - f_2$ and

$2f_2 - f_1$. A graphical illustration of the IP3 is given in Fig. 6.4 [99]. The input power at the third-order intercept point is called input third-order intercept point (IIP3), the output power is called output third-order intercept point (OIP3).

Dynamic Range (DR) The dynamic range is defined by the minimum signal level caused by noise and the maximum signal level that introduces a certain amount of THD. Typically the signal amplitude is used which causes a THD of 1 % (equal to −40 dB THD) and is called $\hat{a}_{1\ \%\ THD}$. The dynamic range is defined as

$$DR = \frac{\hat{a}_{1\ \%\ THD}^2}{2 \cdot \overline{noise}^2} \tag{6.10}$$

$\overline{noise}^2$ denotes the integrated in-band noise. A graphical illustration of the DR is also given in Fig. 6.4. The DR is the difference (in logarithmic scale) of the fundamental signal at 1 % THD and the minimum detectable signal of a system.

Figure of Merit (FOM) The minimum power P_{min} per pole, that is needed to achieve a sufficient signal-to-noise ratio S/N, is dependent on the thermal noise power and the bandwidth f of a passive filter and is denoted as

$$P_{min} = 8k_B T \cdot f_c \cdot S/N \tag{6.11}$$

k_B is the Boltzmann's constant and T is the temperature. The figure of merit (FOM_{Filter}) is used as a benchmark for analog filters and is defined by the ratio of the power consumption of the examined filter to the minimum power P_{min}:

$$FOM_{Filter} = \frac{P}{P_{min}} = \frac{P}{8k_B T \cdot f_c \cdot N \cdot DR} \tag{6.12}$$

In (6.12) P is the power consumption of the observed filter, k_B denotes Boltzmann's constant, T is the temperature, f_c is the −3 dB cut-off frequency, N is the number of poles, and DR is the dynamic range [119].

6.4 Motivation and Applications in Bluetooth and Wideband Code Division Multiple Access

Radio communication is an important and fast growing domain in information and communication technologies and electronic industries. Nowadays, an electronic device, such as a mobile phone or a portable computer, combines several wireless communication standards. The idea to concentrate all communication standards on one chip is called Software Defined Radio (SDR). A software defined radio is able to reconfigure the radio interface by downloading any new wireless standard. Another definition is that a SDR is reconfigurable at any level in the radio protocol stack by software [136]. A SDR system is able to change an existing standard or even new

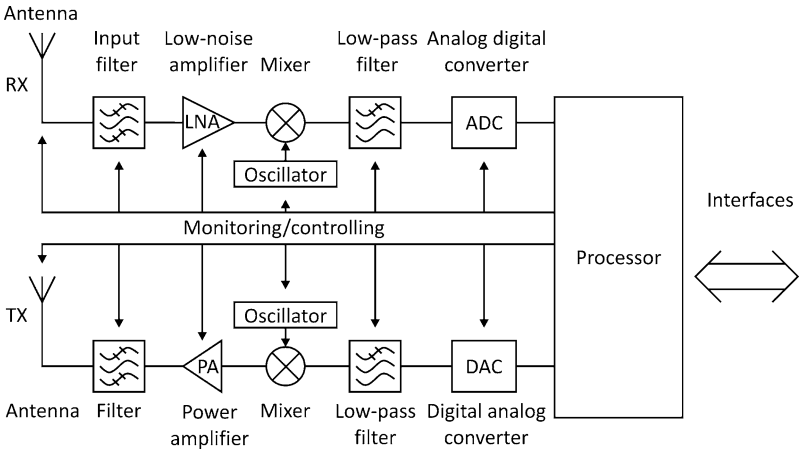


Fig. 6.5 Software defined radio—receive and transmit path

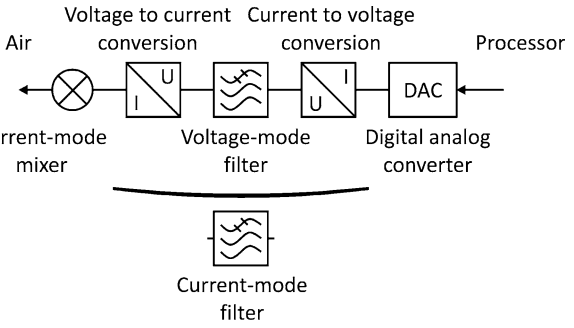


Fig. 6.6 Detailed transmit path of the SDR system

standards can be downloaded. A possible SDR solution is depicted in Fig. 6.5 [137]. The signal is received by an antenna, filtered by an input filter and amplified by a low-noise amplifier. The mixer converts the signal directly into the base-band and the filter selects the desired bandwidth before the analog-digital converter samples the signal and hands it over to the processor.

The transmission of a signal starts at the digital-analog converter, fed with data by the processor. A filter shapes the analog signal from the digital-analog converter (DAC) and the mixer does the up-conversion into the rf-band. A power amplifier drives the antenna, again filtering is necessary. The reconfiguration and adaption to different standards is done by the processor unit via monitoring and controlling networks. Filter bandwidths or corner frequencies, oscillator frequencies and LNA or PA gain are programmable and set by the processor. These monitoring and controlling networks are the core of a SDR system [97].

The proposed current-mode filter is an element of the transmit path of a SDR system. The areas of application in wireless systems are Bluetooth and Wideband Code Division Multiple Access (WCDMA) applications. The details of the transmit path are depicted in Fig. 6.6. The target design uses a current-steering DAC

and a current-mode mixer. The use of a conventional voltage-mode filter necessitates two signal transformations. Before the filter the voltage-mode signal has to be transferred into a current-mode signal and after the filter the voltage-mode signal has to be transferred into the current-mode domain again. The major targets of the current-mode filter design are saving of silicon area and power consumption. This is accomplished by the savings of the two transformation blocks and the low-voltage operation that is applicable for deep sub-micron and nanometer CMOS technology.

The supply voltage of nanometer CMOS technology is low, which results in a limited dynamic range in voltage-mode filters. It will be investigated, to what extent current-mode techniques impact the dynamic range of filters at low supply voltages. The power consumption of the filter impacts the dynamic range as well. Due to the fact that in a current-mode filter the signal quantities are represented by currents, the current consumption is proportional to the signal swings and the necessary bias conditions to avoid distortions. However, a tradeoff between dynamic range and power consumption is required.

6.5 State-of-the-Art

Analog filters are essential blocks in analog circuit design, hence there exist many filter publications. In the following the state-of-the-art is given with the focus on current-mode low-pass filters. The publications are sorted chronologically.

A continuous-time current-mode integrator is described in [68] for high-frequency low-power filters, which are used in video signal processing applications and magnetic disk-drive read channels. The current-mode integrator is designed in 2 µm standard digital CMOS technology and is applied in a fifth-order leapfrog all-pole low-pass filter. The filter cut-off frequency is tunable over a wide range from 25 MHz to 50 MHz by changing the bias currents and thus changing the transconductances of the applied integrators. At a −3 dB cut-off frequency of 30 MHz the filter dissipates 24 mW at a 5 V supply voltage. The total harmonic distortions are given at a cut-off frequency of 30 MHz and an input signal of 1 MHz. A THD of −55 dB is caused by an input signal amplitude of 50 mA_p.

A fifth-order continuous-time current-mode low-pass filter based on current-mode g_m-C integrators, which are suitable for the design of low-voltage high-frequency filters, is presented in [69]. The low-pass filter has a tunable −3 dB cut-off frequency from 24 to 42 MHz. At a −3 dB cut-off frequency of 40 MHz an input signal amplitude of 30 µA causes 1 % total intermodulation distortion. Together with a total integrated rms (root mean square) noise of 7.4 nA_{rms} over 40 MHz a DR of 69 dB is obtained. The filter is designed in 2 µm standard digital CMOS technology and has a power dissipation of 25.5 mW at a supply voltage of 5 V. The active chip area of the low-pass filter is 0.28 mm^2.

A third-order Chebyshev low-pass filter for video signal processing and magnetic disk-drive read-channel systems is described in [149]. In the filter continuous-time current-mode integrators as depicted in Fig. 6.7 are applied. The low-pass filter is

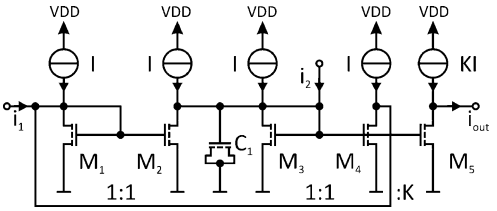


Fig. 6.7 Continuous-time current-mode differential integrator [149]

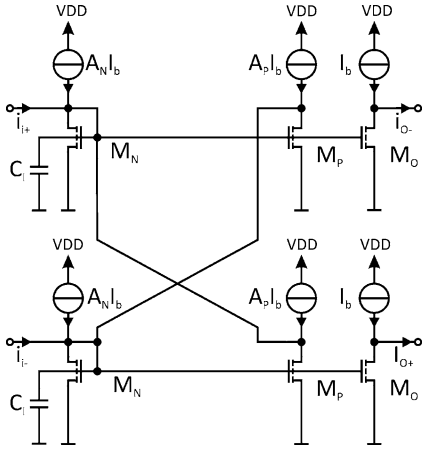


Fig. 6.8 Fully differential current-mode integrator [114]

designed in 1.2 µm CMOS technology and requires 3000 µm^2 active area per pole. It has a supply voltage of 3 V while consuming 6 mW power per pole. The −3 dB cut-off frequency is 125 MHz. The filter produces 1 % THD at an input signal current of 300 µA$_p$ and a total rms input referred noise over a bandwidth of 100 MHz of 182 nA$_{rms}$. This results in an DR of 62 dB.

A sixth-order Bessel low-pass filter in standard 2 µm CMOS technology, which occupies 0.77 mm^2 active area is demonstrated in [114]. The tunable −3 dB cut-off frequency ranges from 7.5 to 13.5 MHz. The filter consumes 4 mW at a supply voltage of 3.3 V. The over 12 MHz integrated output noise results in 714 nA$_{rms}$. 1 % THD is reached at an output signal amplitude of 440 µA$_p$ and the DR calculates to 52 dB. The power supply rejection ratio PSRR at VSS and VDD is 24 dB. The sixth-order Bessel low-pass filter is based on the basic integrator shown in Fig. 6.8.

A fifth-order Chebyshev low-pass filter is introduced in [148]. The filter has a power consumption of 75 µW/pole at a supply voltage of 1.5 V. The −3 dB cut-off frequency is tunable from 300 kHz to 1 MHz. The DR is 67 dB and the total integrated in-band noise is 3.53 nA$_{rms}$ at a −3 dB cut-off frequency of 525 kHz. The PSRR is at minimum 40 dB and the common mode rejection ratio (CMRR) is 70 dB within the pass-band. The Chebyshev filter is designed and fabricated in 1.2 µm n-well CMOS process and requires 0.1 mm^2 chip area per pole.

A low-voltage current-mode integrator using voltage companding is applied in a fourth-order Chebyshev low-pass filter [92]. The integrator is only composed of MOSFET transistors and lacks of any functional capacitors, and hence fits for inte-

gration in digital CMOS technology very well. The cut-off frequency can be tuned from 20 Hz to 20 kHz. The filter consumes 1.16 µW per pole at a −3 dB cut-off frequency of 5 kHz. The dynamic range is 55 dB. Unfortunately the used CMOS process is not mentioned in detail.

A 3 V analog CMOS current-mode continuous-time filter with a negative resistance load is proposed in [49]. The designed third-order Butterworth low-pass filter has a −3 dB cut-off frequency of 50 MHz, a power consumption of 2.4 mW per pole at a 3 V supply voltage. The filter occupies 1 mm^2 in a 1.5 µm n-well standard CMOS technology.

A 5th-order elliptic current-mode low-pass filter with a g_m-C topology is presented in [65]. The filter has a cut-off frequency of 50 MHz and it has a power consumption of 91 mW at a 3.3 V supply voltage. A low distortion level is achieved by scaling for minimum distortion and dynamic biasing for linearization. The current-mode filter is designed in 0.5 µm CMOS and has a core size of 0.56 mm^2. A 15 MHz input current signal of 500 μA_{pp} causes 55 dBc THD and the DR results in 60 dB.

An eighth-order continuous-time current-mode Butterworth low-pass filter is introduced in [25]. The filter is realized with simple current amplifiers and cascade connection of current-mode Sallen-Key biquads. The tuning range covers 237 to 326 MHz with programmable capacitor arrays for frequency tuning, the nominal −3 dB cut-off frequency is 250 MHz. The power consumption of the filter is 24 mW and the supply voltage is 1 V. The THD is −53.5 dB at an input signal of 300 mV_{pp}, however the voltage to current conversion is done by a not specified resistance. The Butterworth filter is designed and simulated in 0.25 µm CMOS technology, the estimated active chip area is 2.46 mm^2.

A low-voltage digitally programmable second-order current-mode low-pass filter which applies a digitally programmable current-mode integrator is presented in [40]. The filter with a −3 dB cut-off frequency of about 80 MHz is integrated in 0.8 µm CMOS technology and needs a supply voltage of 3 V.

A fifth-order Butterworth low-pass filter by applying a current-mode integrator for low-frequency continuous-time filters is demonstrated in [144]. The −3 dB cut-off frequency is tunable from 160 Hz to 5.6 kHz. The filter consumes approximately 20 mW at a supply voltage of 5 V. The filter is designed and fabricated in an AMI 1.2 µm n-well CMOS process and occupies an active area of 0.08 mm^2 per pole.

A current-mode square-root domain filter with a novel current-mode geometric-mean and current squarer circuit is presented in [63]. The filter is used in current controlled oscillators and low-power low-voltage current-mode video frequency filters. The circuit is designed in 0.35 µm AMS CMOS technology, has a supply voltage of 3 V and a −3 dB cut-off frequency range from 1 MHz to 5 MHz. The THD is in the worst case −43 dB for an input amplitude equal to the dc bias current.

A digitally programmable analog current-mode filter for VHF/UHF applications is introduced in [86]. The third-order current-mode Butterworth low-pass filter is tunable from 42 to 215 MHz and has a supply voltage of 2 V at a power consumption of 3.73 mW per pole. A differential input signal of 120 µA causes 1 % THD and the total rms input referred noise is 197 nA_{rms}. A DR of 53 dB is achieved. The filter is designed and fabricated in 0.35 µm n-well CMOS technology and occupies 0.025 mm^2 active area.

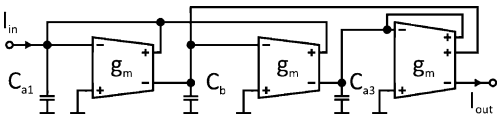


Fig. 6.9 Current-mode third-order single-ended Butterworth low-pass g_m-C filter [48]

A current-mode third-order LC Butterworth low-pass filter using g_m-C techniques is realized in [48]. An outline of the filter structure is depicted in Fig. 6.9. The low-pass filter has a -3 dB cut-off frequency of 200 MHz and dissipates 16.77 mW power at a supply voltage of 1.8 V. A 200 MHz input signal of 0.4 mA causes total harmonic distortions of -46.5 dB. The filter is implemented in the TSMC 0.18 µm 1P6M process and the core area occupies 0.0303 mm^2.

A fifth-order low-pass continuous-time filter for low-voltage applications is introduced in [28]. The filter has a cut-off frequency of 10 MHz and a power consumption of 5 mW at a supply voltage of 3 V. A DR greater than 50 dB is reached at an input signal of 20 µA and the PSRR is slightly larger than 50 dB. The filter is simulated in 1 µm CMOS technology.

A fifth-order low-voltage CMOS current-mode low-pass filter is presented in [67]. The filter is designed in 0.35 µm BiCMOS process and has a power consumption of 21.1 µW at a supply voltage of 1.5 V. The -3 dB cut-off frequency is 482 kHz and the input referred noise at 10 kHz is 4 pA/$\sqrt{\text{Hz}}$. The dynamic range is 40.6 dB.

6.6 Realization of Current-Mode Filters

6.6.1 Current-Input Voltage-Output Filter

Input Filter The realized filter consists of two parts. The first part is a current-mode filter as discussed in Sect. 6.2 and is shown in Fig. 6.10 [62]. The current sources supply a DC-current of about 400 µA and the g_m ratio between the transistors M_3 and M_1 respectively M_4 and M_2 is $\alpha = 1/4$. The resistor $R_{conv} = 2$ kΩ converts now the current into the voltages $v1p$, $v1n$, which are applied to a 2nd-order opamp filter. The cut-off frequencies are controlled by switchable capacitors. The reason to switch capacitors instead of resistors is that the noise level should not change in the passband.

Opamp Filter This 2nd-order filter, which was introduced by [18], is shown in Fig. 6.11. In this topology, the capacitor C_1 and the compensation capacitors from the opamp define the poles. The whole representation of the opamp is shown in Fig. 6.12. In contrast to [18], for each stage a separate common-mode feedback is used. Because one common-mode feedback over two stages will lead to three poles in a loop and cause stability problems. For the input stage the common-mode feedback is done by the two resistors $R_{CMFB} = 100$ kΩ. These resistors should be as high as possible, otherwise they reduce the gain of the opamp. The resistors R_C, which are in series to the compensation capacitors, eliminate the zero in the right-

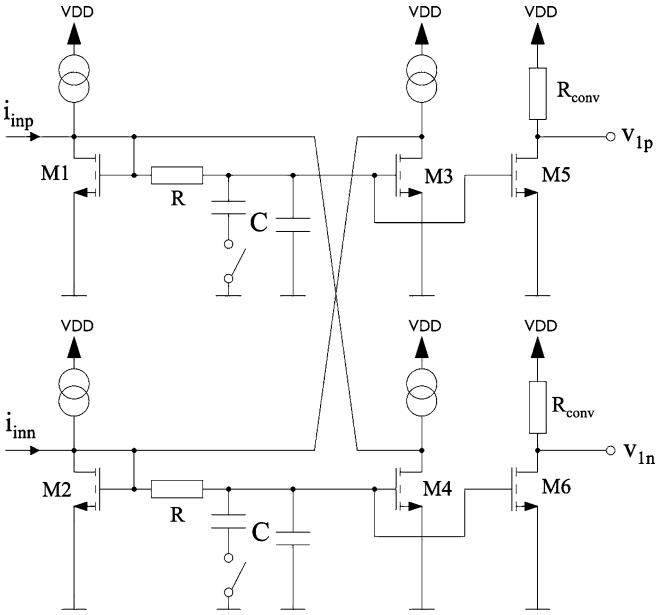
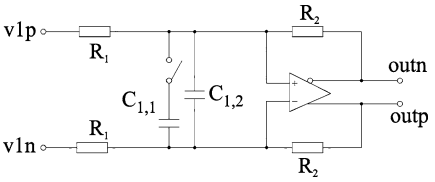


Fig. 6.10 Input filter of the realized filter

Fig. 6.11 Realized filter



half complex plane which is given by the Miller compensation. The transfer function with the filter parameters is given by

$$H(s) = \frac{A\omega_0^2}{s^2 + \omega_0/Q \cdot s + \omega_0^2} \tag{6.13}$$

with

$$A = \frac{R_2}{R1}, \qquad Q = \frac{1}{A+1}\sqrt{\frac{g_{m1}R_2C_1}{C_C}}, \qquad \omega_0 = \sqrt{\frac{g_m 1}{R_2C_1C_C}} \tag{6.14}$$

The bias current of the opamp can be tuned by an external voltage V_{REF} as shown in Fig. 6.13 (V_B in Fig. 6.13 is the same as in Fig. 6.12). Due to the negative feedback and the gain of the differential amplifier the voltage on the resistor R is controlled near to V_{REF}. The current is then mirrored by the transistor M19 to the input stage of the opamp. So the cut-off frequency and the quality factor of the filter can be varied with V_{REF} (see (6.14)).

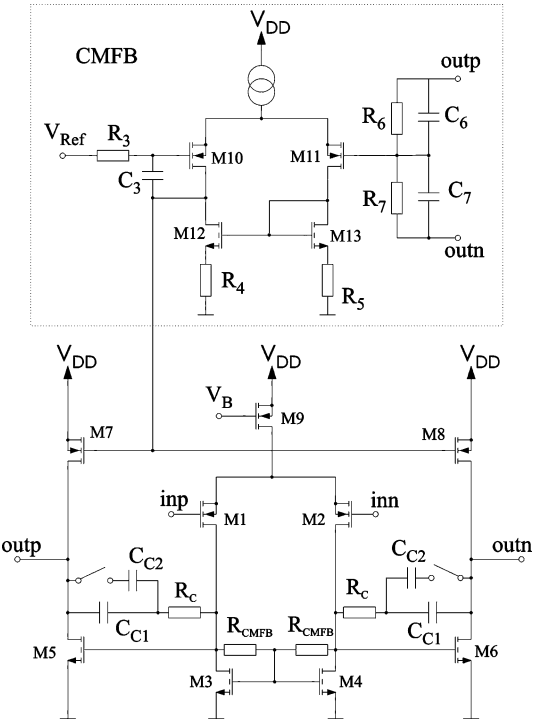


Fig. 6.12 Representation of the complete opamp

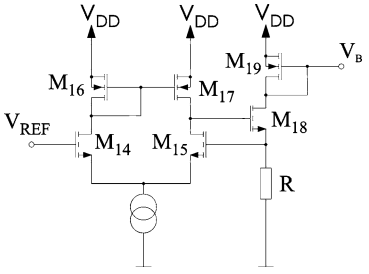
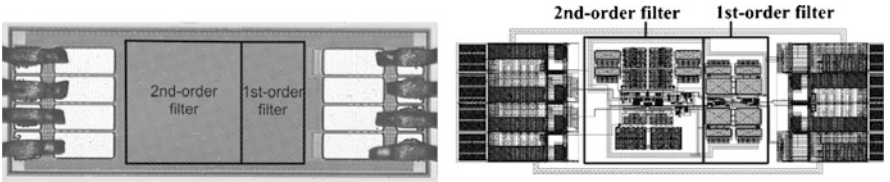


Fig. 6.13 Circuit for the bias current of the opamp

Experimental Results In Fig. 6.14(a) the photomicrograph and in Fig. 6.14(b) the layout plot of the realized chip are shown. The chip area including the pads is 900 µm × 300 µm, the chip area of the filter without the pads is 370 µm × 250 µm. The current consumption of the whole chip is 2.6 mA at $V_{DD} = 1.5$ V, 1.5 mA for the input filter and 1.1 mA for the opamp filter. The filter capacitors were realized with metal-metal capacitors and with MOS-transistors. Figure 6.15 shows the measured DC-transfer characteristics. The linear input range is ±380 µA which is limited by the current sources in the input stage.

In Fig. 6.16 the differential amplitude response and in Fig. 6.17 the differential phase response is shown. By varying V_{REF}, the current through M9 of Fig. 6.12 is changed between 50 µA and 75 µA. The two curves on the left side show the case



(a) Chip photograph of the whole chip (b) Layout plot of the OTA

Fig. 6.14 Realized chip

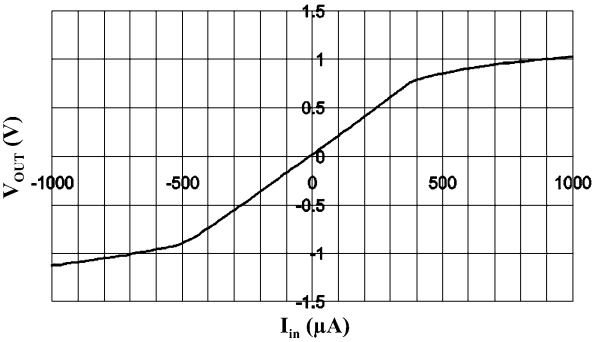


Fig. 6.15 Measured DC-transfer characteristics

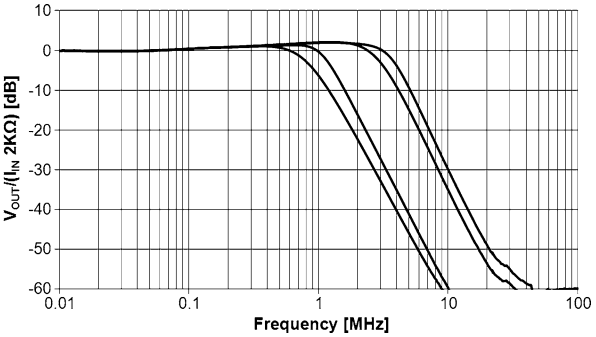


Fig. 6.16 Measured AC-amplitude response

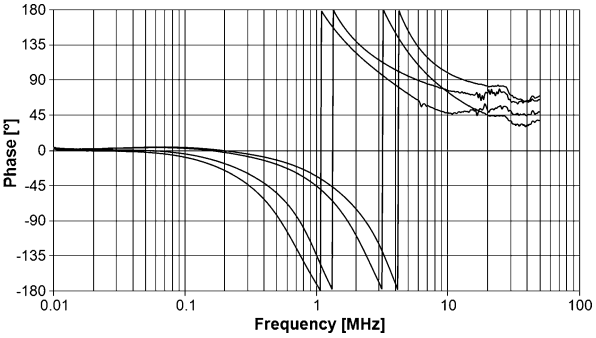


Fig. 6.17 Measured AC-phase response

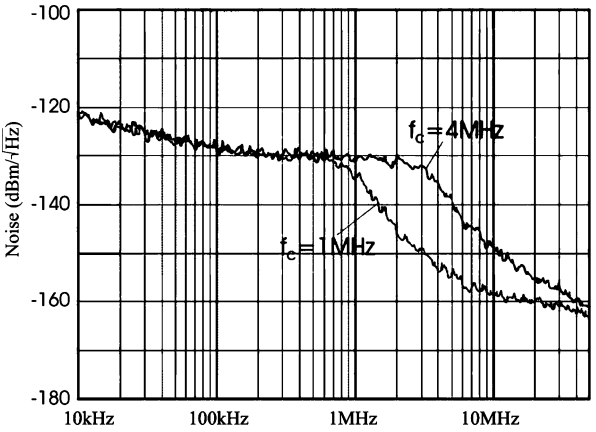


Fig. 6.18 Measured noise spectral density

with f_C of 1 MHz, the two on the right side with f_C of 4 MHz while the reference voltage V_{REF} is varied. The 3 dB cut-off frequency can be tuned from 0.8 MHz to 1.2 MHz for the case with the lower cut-off frequency and from 3.5 MHz to 4 MHz for the case with the higher cut-off frequency. The filter characteristics falls with −60 dB/decade in the cutoff region, the resonance peak has a height between 1 dB and 1.8 dB.

The IM3 of this filter for a two-tone input signal of 125 µA, that corresponds to an output amplitude of 250 mV, is −50 dB. The frequencies for the intermodulation measurements are 700 kHz and 800 kHz for the filter with $f_C = 1$ MHz and 3 MHz and 3.4 MHz for the filter with $f_C = 4$ MHz. This gives an IIP3 of 2.22 mA or an OIP3 of 23 dBm. For an input signal of 315 µA (= 630 mV output signal) the total harmonic distortion is 1 %.

In Fig. 6.18 the measured noise spectral density at the output of the filter is shown. For frequencies smaller than 100 kHz the flicker noise is dominant, in the passband the noise density is 70 nV/$\sqrt{\text{Hz}}$. The measured integrated output noise (includes also the flicker noise) over a bandwidth of 20 MHz is 98.5 µV_{rms} for the case with $f_C = 1$ MHz and 162 µV_{rms} for the case with $f_C = 4$ MHz.

Table 6.1 summarizes the measured results from the realized chip.

6.6.2 Current Input/Output Filter

This filter [61] consists of a 1st-order current-mode filter where a capacitance multiplication technique is applied. The 2nd-order filter consists of an active gm-RC filter where the output voltage is converted into a current.

The input filter (see Fig. 6.19) consists of a current-mode architecture with virtual ground regulation. Virtual ground is achieved with two simple differential amplifiers $A1$, $A2$ with NMOS current-mirror loads which control the input voltage near to V_{REF} which is $V_{DD}/2$. The transfer function of this filter is given by (6.5), the factor $\alpha = 1/2$ which means that the effective capacitance is increased by a factor of 2.

Table 6.1 Summary of the realized chip

Technology	120 nm CMOS	
Voltage supply	1.5 V	
Current consumption	2.6 mA	
Power consumption per pole	1.3 mW	
Input current for 1 % THD	315 µA	
IIP3	2.22 mA	
Output spectral noise density	70 nV/$\sqrt{\text{Hz}}$	
Area of the filter	370 µm × 250 µm	
Cut-off frequency	0.8–1.2 MHz	3.5–4 MHz
Integrated output noise	98.5 µV_{rms}	162 µV_{rms}
Noise density at 12.5 MHz	2.8 nV/$\sqrt{\text{Hz}}$	6.3 nV/$\sqrt{\text{Hz}}$
	162 dBc/$\sqrt{\text{Hz}}$	155 dBc/$\sqrt{\text{Hz}}$
Noise density at 40 MHz	1.8 nV/$\sqrt{\text{Hz}}$	2.2 nV/$\sqrt{\text{Hz}}$
	165 dBc/$\sqrt{\text{Hz}}$	164 dBc/$\sqrt{\text{Hz}}$
Dynamic range	73.1 dB	68.8 dB

The 2nd-order filter (shown in Fig. 6.20) consists of an active gm-RC filter as realized also in Fig. 6.11. The representation of the opamp is shown in Fig. 6.21. In contrast to Fig. 6.12, here in the input stage source degeneration resistors R_S are used which improve the linearity performance. Furthermore, two more transistors (M9, M10) are connected to the output which convert the voltage into the current due to the fact that the gate-source voltage of the transistors M5 and M9 respectively M6 and M10 are equal. The low-pass consisting of R_{out} and C_{out} gives some additional attenuation at higher frequencies.

Experimental Results In Fig. 6.22(a) the photomicrograph and in Fig. 6.22(b) the layout plot of the realized chip is shown. The chip area including the pads is 470 µm × 350 µm, the chip area of the filter without the pads is 300 µm × 180 µm. The current consumption of the whole chip is 5.26 mA at $V_{DD} = 1.2$ V. The filter capacitors were realized with finger capacitors and with MOS-transistors.

In Fig. 6.23 the measured DC-transfer characteristics is shown. The linear input range of the input current is ±350 µA.

In Fig. 6.24 the measured amplitude frequency response is shown. The filter characteristics falls with −60 dB/decade in the cut-off region, the −3 dB cut-off frequency is 0.95 MHz and 3.75 MHz, the DC gain is −1.6 dB.

The harmonic distortion of this filter was measured with an input frequency of 100 kHz for the filter with cut-off frequency of 1 MHz and 400 kHz for the filter with cut-off frequency of 4MHz. In both cases for an input amplitude of 340 µA a THD of 1 % is obtained. In a two-tone measurement an IM3 of −40 dB was measured for a 2-tone input signal of 213 µA (the frequencies are 700 kHz and 800 kHz for the filter with $f_C = 1$ MHz and 3 MHz and 3.4 MHz for the filter with $f_C = 4$ MHz) which corresponds to an IIP3 of 2.13 mA.

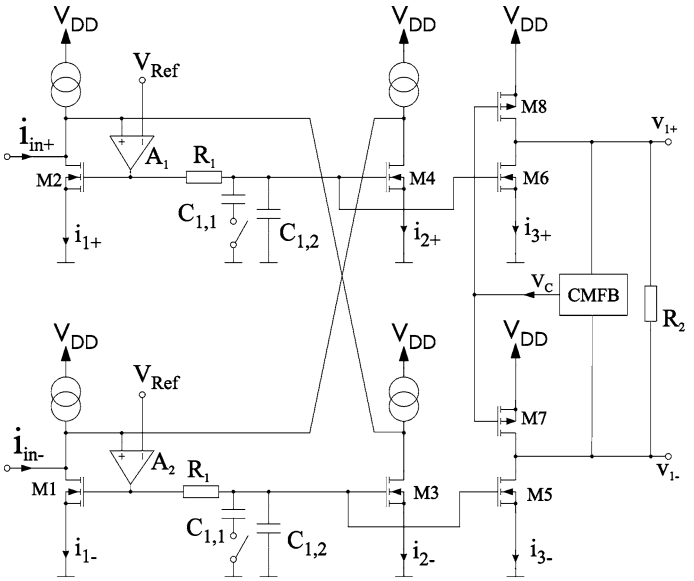
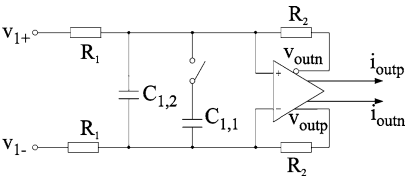


Fig. 6.19 Input filter

Fig. 6.20 2nd-order filter



In Fig. 6.25 the measured output noise spectral density is shown. In the passband the noise is -194 dBA/$\sqrt{\text{Hz}} = 200$ pA/$\sqrt{\text{Hz}}$, the total integrated noise results in 290 nA for the filter with $f_C = 1$ MHz and 470 nA for the filter with $f_C = 4$ MHz.

Table 6.2 summarizes the measured results from the realized chip.

6.6.3 Current-Mode Filters Based on the G_m-C Topology

Introduction Current-mode filters can be realized also with the G_m-C topology. In Fig. 6.26(a) a current-mode integrator and in Fig. 6.26(b) a 1st-order current-mode filter is shown.

The transfer function is given by

$$H_{int} = \frac{G_{m,int}}{sC_{int}}, \qquad H_1 = \frac{1}{1 + sC/G_{m,1}} \tag{6.15}$$

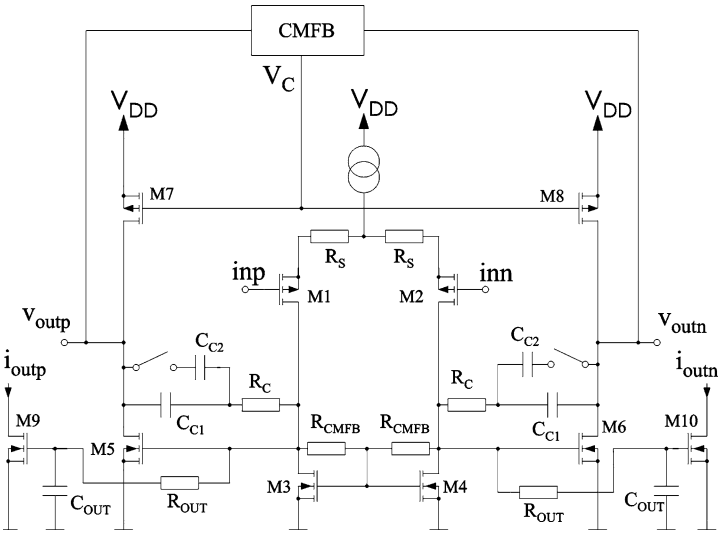
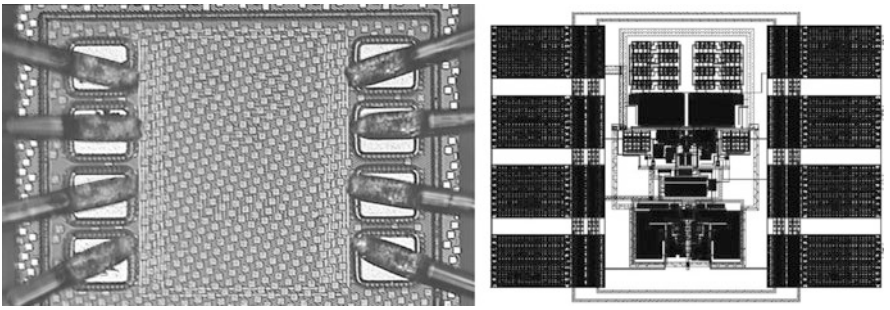


Fig. 6.21 Representation of the opamp



(a) Chip photograph of the realized chip (b) Layout plot of the realized chip

Fig. 6.22 Realized chip

With the topology in Fig. 6.27 a 2nd-order current-mode filter based on the G_m-C topology is shown. The filter parameters of this filter are given by

$$A = \frac{G_{m3}}{G_{m2}}, \qquad Q = \sqrt{\frac{C_2}{C_1} G_{m1} G_{m2} R^2}, \qquad \omega_0 = \sqrt{\frac{G_{m1} G_{m2}}{C_1 C_2}} \tag{6.16}$$

Realized Filter In the realized filter [60] the OTA (Fig. 6.28) based on the super source follower configuration (explained in Sect. 4.2) is used. This OTA is extended by the folded cascodes M_3 and M_4 which increase the closed-loop gain A_0 and so the distortions can be improved. The bulks of the input transistors M_1, M_2 are connected to their respective sources which avoids the backgate effect. The currents

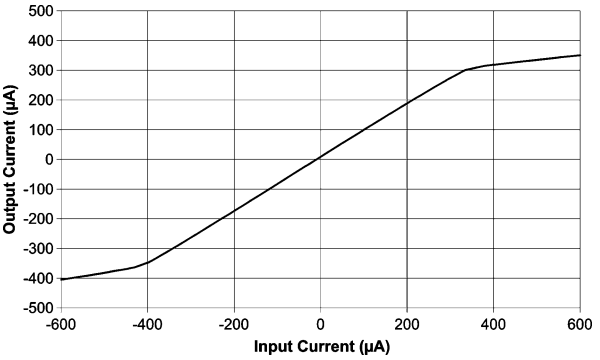


Fig. 6.23 Measured DC-transfer characteristics

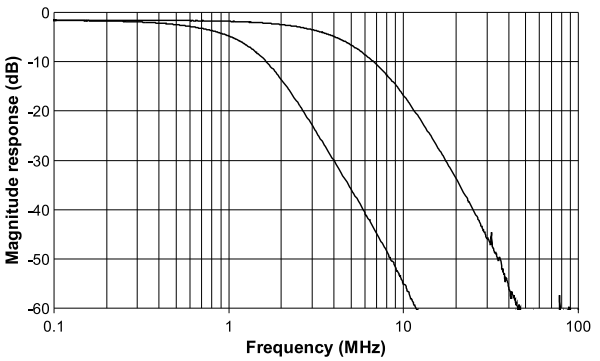


Fig. 6.24 Magnitude frequency response

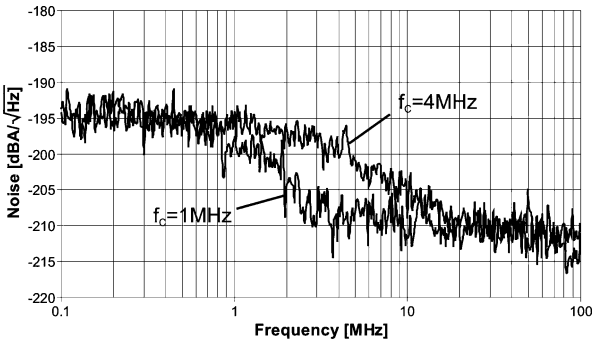


Fig. 6.25 Output noise power spectral density

through the transistors M_5, M_6 are transferred to M_7–M_{10} due to the same gate-source voltages.

In Fig. 6.29 the realized 3rd-order current-mode filter is shown. It consists of an integrator and a 1st-order filter in a negative feedback loop and a 1st-order filter. The low-pass with R_1, C_1 gives the first-order, the OTA G_{m2} forms with C_2 an integrator and the OTA G_{m3} gives with C_3 the third pole. Virtual ground at the input is obtained with two simple differential amplifiers A_1, A_2 which work in a control loop and regulate the input voltage near to a reference voltage V_{REF}.

Table 6.2 Properties of the 3rd-order filter

Technology	65 nm CMOS	
Voltage supply	1.2 V	
Current consumption	5.26 mA	
Power consumption per pole	2.1 mW	
Input current for 1 %THD	340 µA	
IIP3	2.13 mA	
Output spectral noise density	200 pA/$\sqrt{\text{Hz}}$	
Area of the filter	300 µm × 180 µm	
Cut-off frequency	0.95 MHz	3.75 MHz
Integrated output noise	290 nA_{rms}	470 nA_{rms}
Noise density at 12.5 MHz	32 pA/$\sqrt{\text{Hz}}$	39 pA/$\sqrt{\text{Hz}}$
	−135 dBc/$\sqrt{\text{Hz}}$	−133 dBc/$\sqrt{\text{Hz}}$
Noise density at 40 MHz	25 pA/$\sqrt{\text{Hz}}$	25 pA/$\sqrt{\text{Hz}}$
	−138 dBc/$\sqrt{\text{Hz}}$	−138 dBc/$\sqrt{\text{Hz}}$
Dynamic range	56.7 dB	52.6 dB

To control the DC-voltage at the output of the first-order filter (node $V_{1,1}$, $V_{1,2}$) a CMFB (see Fig. 4.12) is used. For the first OTA G_{m2}, the transistors M_{11}, M_{12} work as current sources. For the stabilization of the common-mode voltage at the filter output ($V_{2,1}$, $V_{2,2}$) the control voltage V_C of the CMFB is connected to V_{B2} of the OTA.

$$H(s) = \frac{\omega_0^2}{s^2 + s \cdot \omega_0/Q + \omega_0^2} \cdot \frac{1}{1 + s/\omega_3} \tag{6.17}$$

with the filter parameters

$$\omega_0 = \sqrt{\frac{G_{m2}}{R_1 C_1 C_2}}, \qquad Q = \sqrt{R_1 G_{m2}} \cdot \sqrt{\frac{C_1}{C_2}}, \qquad \omega_3 = \frac{G_{m3}}{C_3} \tag{6.18}$$

Experimental Results In the Figs. 6.30(a) and 6.30(b) the chip photograph and the layout plot of the realized chip are shown. The total chip area is 500 µm × 400 µm, the active area (without pads) is 400 µm × 230 µm. The filter capacitors were realized with finger capacitors and with MOS-transistors.

In Fig. 6.31 the measured DC-transfer characteristics is shown. The curve is linear for an input current of ±280 µA.

In Fig. 6.32 the measured magnitude frequency response is shown. The filter characteristics falls with −60 dB in the cut-off region, the cut-off frequencies are 0.98 MHz and 4.06 MHz and the DC gain is −3.5 dB. In Fig. 6.33 the measured phase frequency response is shown. The phases at the cut-off frequencies are −135° which shows that the filter has a Butterworth behavior. In Table 6.3 the measured 3rd-harmonics for a single-tone measurement are presented. The input frequency was 100 kHz for the filter with $f_C = 1$ MHz and 400 kHz for the filter

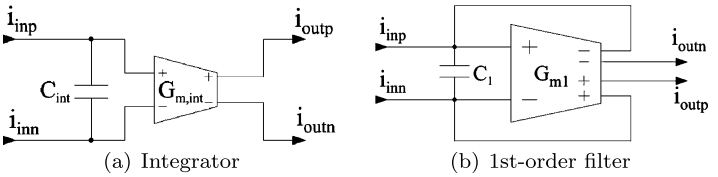


Fig. 6.26 Current-mode filters based on G_m-C architecture

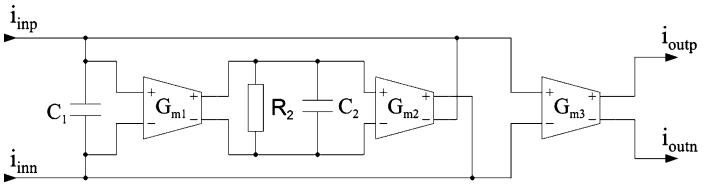


Fig. 6.27 Current-mode filter based on the G_m-C topology

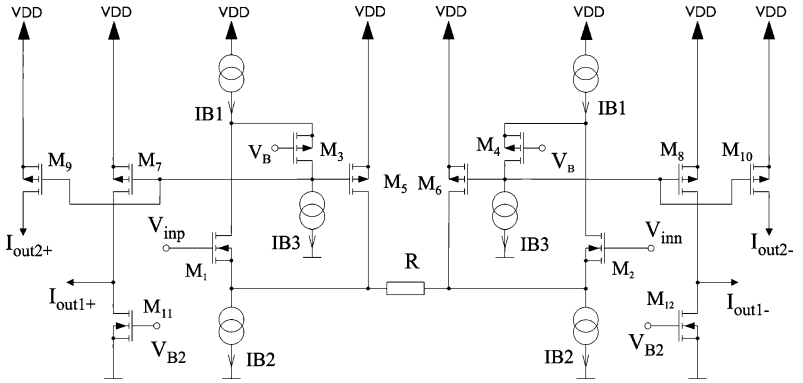


Fig. 6.28 Improved OTA

with $f_C = 4$ MHz. At an amplitude of 240 µA the 3rd-harmonics are −40 dB. The IM3 for a two-tone signal of 140 µA each (the two-tone signals have the frequencies of 600 kHz and 700 kHz for the filter with $f_C = 1$ MHz and 3 MHz and 3.2 MHz for the filter with $f_C = 4$ MHz) is −40 dB. This corresponds to an IIP3 of 1.4 mA. In Fig. 6.34 the measured output noise spectral density is shown. It shows that for frequencies smaller than 700 kHz the flicker noise is dominant. For frequencies larger than 700 kHz the thermal noise in the passband is 25 pA/$\sqrt{\text{Hz}}$. The total integrated noise is 29 nA_{rms} for the filter with $f_C = 1$ MHz and 54 nA_{rms} for the filter with $f_C = 4$ MHz. With this values a DR of 72.5 dB for $f_C = 1$ MHz and 66.5 dB for $f_C = 4$ MHz is obtained.

Table 6.4 summarizes the measured results from the realized chip.

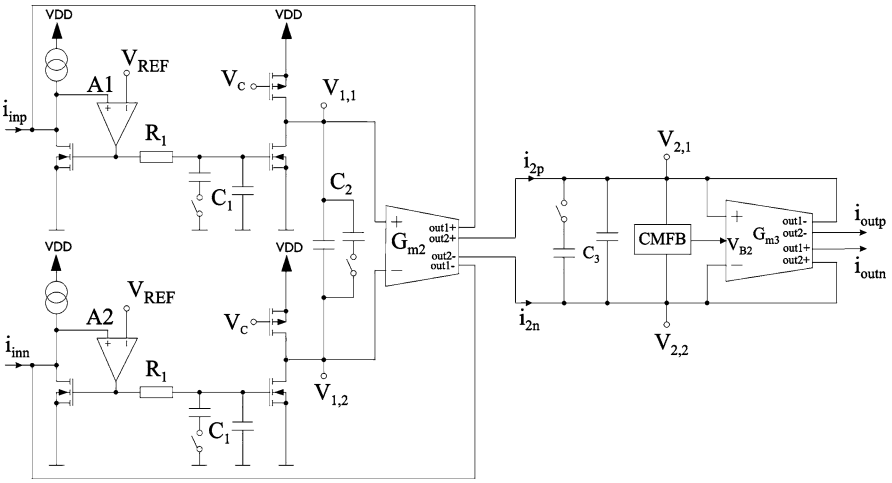
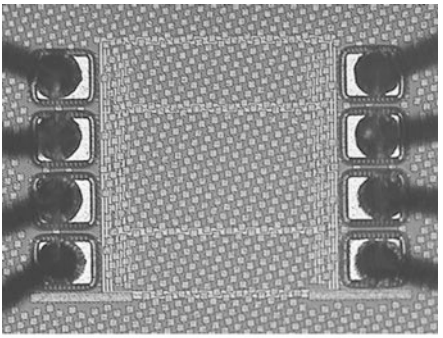
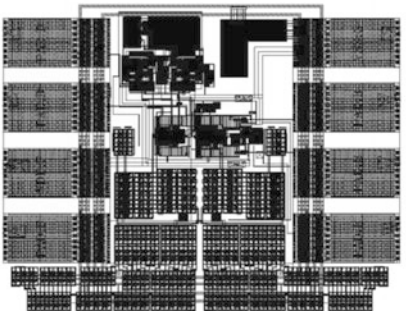


Fig. 6.29 Realized filter

Fig. 6.30 Realized chip



(a) Chip photograph of the realized chip



(b) Layout plot of the realized chip

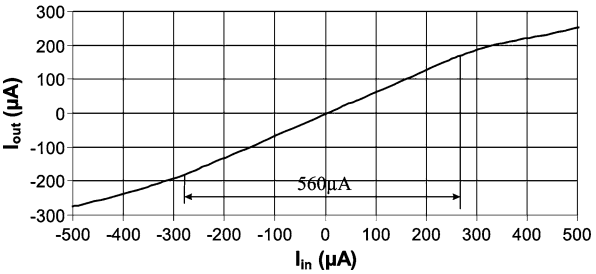


Fig. 6.31 Measured DC transfer characteristics

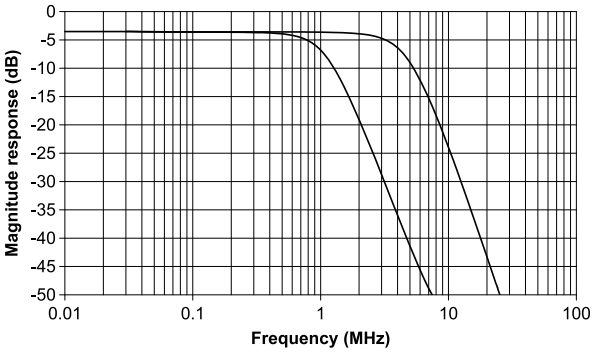


Fig. 6.32 Measured magnitude frequency response

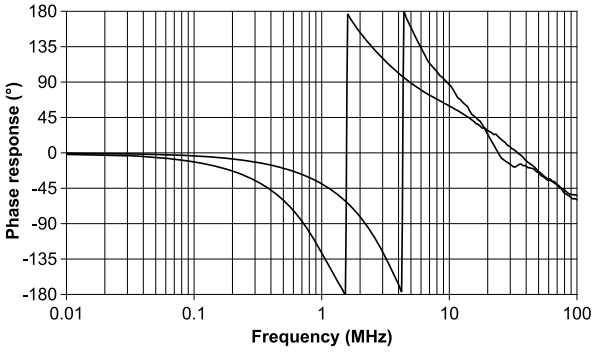


Fig. 6.33 Measured phase frequency response

Table 6.3 Measured harmonics of the output signal

$\hat{I}_{in}$ [µA]	HD3 [dB] $f_C = 1$ MHz	HD3 [dB] $f_C = 4$ MHz
100	−54.0	−56.4
150	−48.6	−51.1
200	−46.1	−46.1
250	−39.4	−39.5
300	−34.7	−36.1

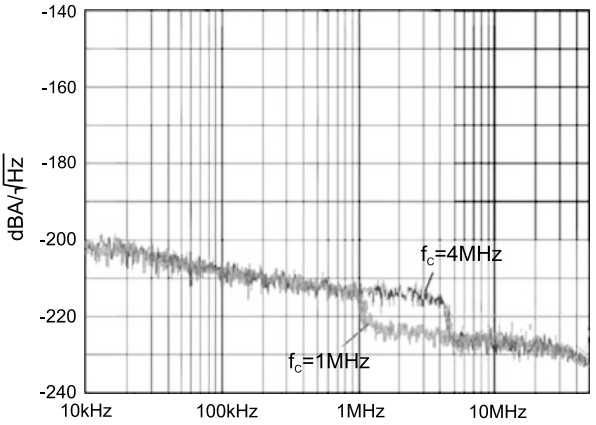


Fig. 6.34 Measured output noise spectral density

6.6.4 A 3rd-Order Current-Mode Continuous-Time Low-Pass Filter Using a Chip Area Saving Strategy

A 3rd-order current-mode continuous-time Butterworth low-pass filter is realized [126]. The aimed −3 dB cut-off frequencies are 1.1 MHz and 4.4 MHz observing the target specifications. Due to the relatively low cut-off frequencies big capacitors for the filter poles are needed. In order to save expensive chip area a capacitor saving strategy is developed. A test chip of the current-mode filter is designed and fabricated in 65 nm CMOS technology and its behavior is characterized.

The block diagram of the low-pass filter is depicted in Fig. 6.35. The filter has a differential topology. It has 3 basic building blocks, whereas the first two blocks, a 1st-order current-mode low-pass filter and a current-mode integrator represent a 2nd-order low-pass filter. The last block is another 1st-order current-mode low-pass filter to obtain an overall 3rd-order current-mode low-pass filter.

Current-Mode Integrator Integrators are essential parts in active filter design and their characteristics contribute to the filter performance and quality directly. In current-mode circuits current-mode integrators are of importance. Figure 6.36 shows the implemented fully differential current-mode integrator, which is an innovative modification of [114]. Figure 6.36(a) represents the detailed schematics of the current-mode integrator, the equivalent circuit is depicted in Fig. 6.36(b).

The integrator is assembled of two cross coupled current mirrors. The cross coupling is done between the transistors M_{1a} and M_{2b} as well as M_{1b} and M_{2a}. The cross coupling effects a high differential gain and a low common-mode gain. The unity-gain frequency is switchable between two frequencies, hence switchable capacitors (C_{1a}, C_{1b}, C_{2a}, C_{2b}) are implemented. The overall filter has relatively low −3 dB cut-off frequencies of 1.1 MHz and 4.4 MHz which need large integrating capacitors. Hence, the capacitors are an important factor of integrated filters and need large chip area. The innovation is the adding of the resistors R_{1a} and R_{1b} to save chip area by keeping the characteristics of the integrator circuit. The transfer function of the modified integrator is derived in the following.

Table 6.4 Summary for the realized current-mode G_m-C filter

Technology	65 nm CMOS	
Voltage supply	1.2 V	
Current consumption	6.8 mA	
Power consumption per pole	2.72 mW	
Input current for 1 % THD	240 µA	
IIP3	1.4 mA	
Output spectral noise density	25 pA/$\sqrt{\text{Hz}}$	
Area of the filter	400 µm × 230 µm	
Cut-off frequency	0.98 MHz	4.06 MHz
Integrated output noise	29 nA_{rms}	54 nA_{rms}
Noise density at 12.5 MHz	4.5 pA/$\sqrt{\text{Hz}}$	4.5 pA/$\sqrt{\text{Hz}}$
	−152 dBc/$\sqrt{\text{Hz}}$	−152 dBc/$\sqrt{\text{Hz}}$
Noise density at 40 MHz	3 pA/$\sqrt{\text{Hz}}$	3 pA/$\sqrt{\text{Hz}}$
	−155.4 dBc/$\sqrt{\text{Hz}}$	−155.4 dBc/$\sqrt{\text{Hz}}$
Dynamic range	72.5 dB	66.6 dB

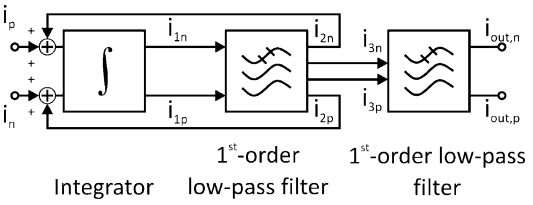


Fig. 6.35 Block diagram of the 3rd-order current-mode Butterworth low-pass filter using a chip area saving strategy

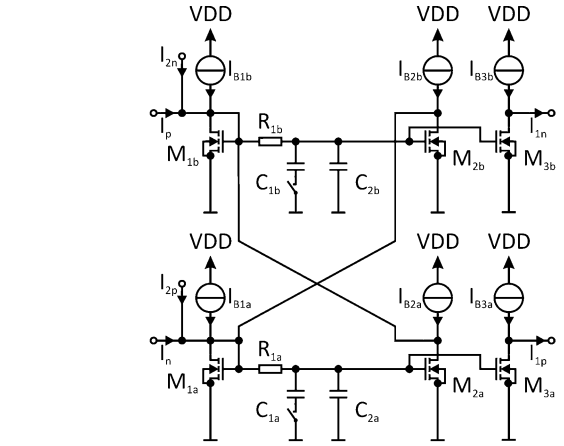
For the formation of the mathematical model Fig. 6.36(b) is used. The connections of I_{2n} and I_{2p} are used for feedback purposes (compare to Fig. 6.35) and are not important for the integrator functionality. Hence, the input currents I_{2n} and I_{2p} are supposed to be 0. For the calculations the switches for the frequency selection are open and only the capacitances C_{2a} and C_{2b} are active. The input currents i_p and i_n are given by

$$i_p = u_{GS1b} g_{m1b} + \frac{u_{GS1a} g_{m2a}}{1 + s R_{1a} C_{2a}} + g_{DS2a} u_{GS1b} + \frac{u_{GS1b}}{R_{1b} + \frac{1}{sC_{2b}}} \tag{6.19}$$

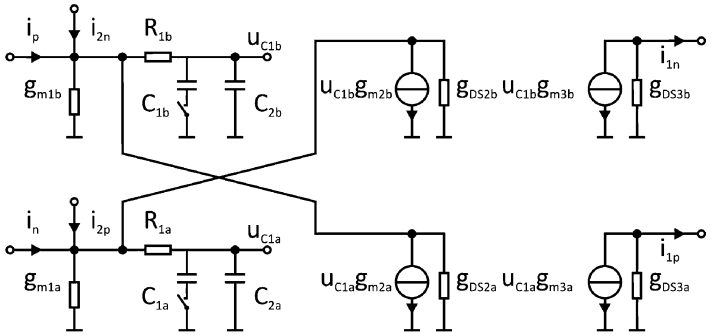
and

$$i_n = u_{GS1a} g_{m1a} + \frac{u_{GS1b} g_{m2b}}{1 + s R_{1b} C_{2b}} + g_{DS2b} u_{GS1a} + \frac{u_{GS1a}}{R_{1a} + \frac{1}{sC_{2a}}} \tag{6.20}$$

An integrator behavior is realizable due to equal circuit elements: $M_{1a} = M_{1b} = M_{2a} = M_{2b}$; $M_{3a} = M_{3b}$; $R_{1a} = R_{1b} = R_1$; $C_{1a} = C_{1b} = C_1$; $C_{2a} = C_{2b} = C_2$. The bias currents I_{B1a}, I_{B1b}, I_{B2a}, and I_{B2b} are equal as well as I_{B3a} and I_{B3b}. By using these element parameters, solutions for u_{GS1a} and u_{GS1b} can be found which are inserted in the equations for the output currents



(a) Current-mode integrator - schematics



(b) Current-mode integrator - equivalent circuit

Fig. 6.36 Current-mode integrator with capacitance saving strategy

$$i_{1n} = -\frac{g_{m3} u_{GS1b}}{1 + R_1 C_2 s} - u_{DS3} g_{DS3} \tag{6.21}$$

and

$$i_{1p} = -\frac{g_{m3} u_{GS1a}}{1 + R_1 C_2 s} - u_{DS3} g_{DS3} \tag{6.22}$$

Finally the transfer function of the current-mode integrator by using (6.22) and (6.21) results in

$$H_I(s) = \frac{i_{1p} - i_{1n}}{i_p - i_n} = \frac{g_{m3}}{g_{DS2} + (R_1(g_{m1} + g_{DS2}) + 1) C_2 s} \tag{6.23}$$

The innovation of the modification is clearly visible in (6.23). In the denominator a supplementary element R_1 appears in addition to C_2 and the transconductance of M_1 and M_3, which manage the unity-gain frequency of the integrator. By increasing the resistor R_1, a huge amount of chip area can be saved. Naturally the

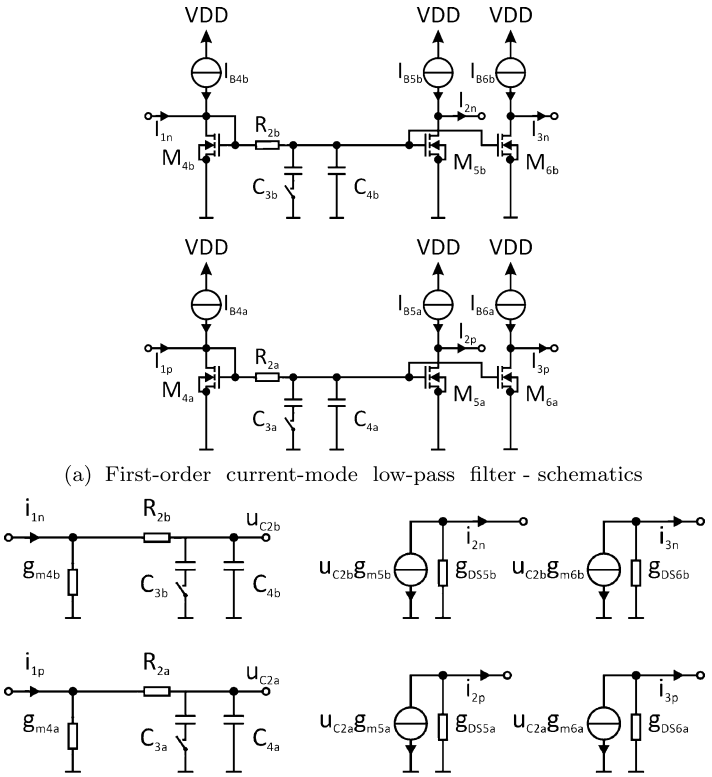


Fig. 6.37 First-order current-mode low-pass filter

resistor increases the noise level of the integrator, hence a trade-off between noise and chip area has to be made. Low unity-gain frequencies can be realized by increasing the transconductance of M_1 as well. A high transconductance is realized by raising the transistor bias current, which deteriorates the power consumption of the integrator. Summarized the resistor R_1 in the current-mode integrator enables to save chip area and power dissipation at the expense of a higher noise level.

First-Order Current-Mode Low-Pass Filter The first-order low-pass filter is shown in Fig. 6.37(a), which consists of two current mirrors due to the differential structure of the overall low-pass filter. The dominant pole is defined by the combination of R_{2a}, C_{3a}, and C_{4a} as well as R_{2b}, C_{3b}, and C_{4b}. The split and switchable capacitors C_{3a}, C_{4a}, C_{3b}, and C_{4b} are implemented to obtain two different -3 dB cut-off frequencies of the 1st-order low-pass filter. A differential design of the entire 3rd-order low-pass filter needs the equality of upper and the lower half: $M_{4a} = M_{4b}$, $M_{5a} = M_{5b}$, $M_{6a} = M_{6b}$, $C_{3a} = C_{3b} = C_3$, $C_{4a} = C_{4b} = C_4$, $R_{2a} = R_{2b} = R_2$,

$I_{B4a} = I_{B4b}$, $I_{B5a} = I_{B5b}$, and $I_{B6a} = I_{B6b}$. The transfer function of the 1st-order current-mode low-pass filter is

$$H_{LP}(s) = \frac{i_{2p} - i_{2n}}{i_{1p} - i_{1n}} = \frac{1}{C_4(R_2 + \frac{1}{g_{m4}}) + 1} \tag{6.24}$$

It is assumed, that only the capacitor C_4 is active.

Two outputs are needed for the connections to the following block and the feedback ($i_{2n/p}$ and $i_{3n/p}$). Since a single current output cannot be used for both purposes due to the Kirchhoff's circuit laws, the output is mirrored twice. Therefore additional bias currents are necessary and increase the overall current consumption.

3rd-Order Current-Mode Butterworth Low-Pass Filter The current-mode integrator and the current-mode 1st-order low-pass filter in negative feedback generates a 2nd-order low-pass filter. The 2nd-order low-pass filter has two outputs (compare to Fig. 6.35): I_{2n} and I_{2p} for feedback purposes and I_{3n} and I_{3p} is connected to the following 1st-order low-pass filter. The transfer function results in

$$H_{LP2} = \frac{1}{\alpha s^2 + \beta s + \gamma} \tag{6.25}$$

The coefficients α, β, and γ are denoted as

$$\alpha = \frac{C_2 C_4}{g_{m3} g_{m4}}(R_2 g_{m4} + 1)\big(R_1(g_{m1} + g_{DS2}) + 1\big) \tag{6.26}$$

$$\beta = \frac{C_2}{g_{m3}}\big(R_1(g_{m1} + g_{DS2}) + 1\big) + \frac{C_4 g_{DS2}}{g_{m3} g_{m4}}(R_2 g_{m4} + 1) \tag{6.27}$$

and

$$\gamma = 1 + \frac{g_{DS2}}{g_{m3}} \tag{6.28}$$

Due to the non-ideal manner of the current-mode integrator and the open-loop gain, is finite (lossy integrator). A limited open-loop gain may deteriorate the entire filter performance severely. To estimate the impact of the non-ideal integrator on the filter performance the quality factors (Q) of the 2nd-order low-pass filter using a lossy integrator is compared to the ideal 2nd-order low-pass filter

$$H_{ideal}(s) = \frac{1}{1 + s\tau + s^2\tau\tau_2} \tag{6.29}$$

τ denotes the time constant of the ideal integrator and τ_2 the time constant of the ideal 1st-order low-pass filter. The transfer function of a 2nd-order low-pass filter is calculated by using the lossy integrator transfer function

$$H_{lossy}(s) = \frac{A_0}{1 + A_0\tau' s} \tag{6.30}$$

τ' is the time constant of the lossy integrator. The transfer function of the 2nd-order low-pass filter by using (6.30) and a 1st-order low-pass filter with the time constant τ_2' results in

$$H(s) = \frac{A_0}{1 + A_0 + s(\tau_2' + A_0\tau') + A_0\tau'\tau_2's^2} \tag{6.31}$$

The quality factor of the ideal 2nd-order low-pass filter in (6.29) results in

$$Q = \sqrt{\frac{\tau_2}{\tau}} \tag{6.32}$$

In the 3rd-order Butterworth low-pass filter the embedded 2nd-order low-pass filter has a Q of 1 and induces

$$\tau = \tau_2 \tag{6.33}$$

The application of the lossy integrator in the 2nd-order low-pass filter (6.31) under the assumption of (6.33) leads to a quality factor Q_{lossy} of

$$Q_{lossy} = \sqrt{\frac{A_0}{1 + A_0}} \tag{6.34}$$

The open-loop gain A_0 of the lossy integrator is

$$A_0 = \frac{g_{m3}}{g_{DS2}} \tag{6.35}$$

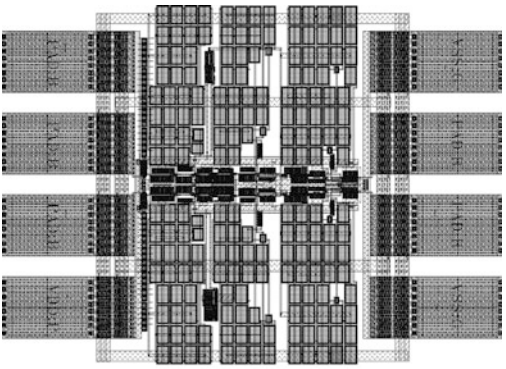
as given in (6.23). Observing (6.35), an open-loop gain of at least 10 is reasonable. The resulting Q is then at least 0.953 instead of 1 which means the relative deviation of Q is at most of -4.7 %. The lossy integrator does not deteriorate the filter performance significantly.

The required 3rd-order low-pass Butterworth filter is realized by connecting another 1st-order low-pass filter as presented in Fig. 6.37. The resulting transfer function is

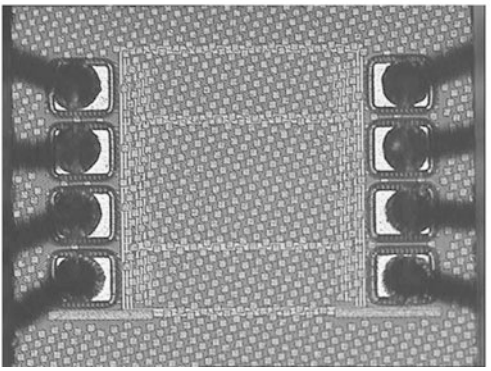
$$H_{Filter}(s) = H_{LP2}(s) \cdot H_{LP}(s) \tag{6.36}$$

by inserting (6.25) and (6.24).

Experimental Results The outlined above 3rd-order Butterworth low-pass filter is designed and fabricated in 65 nm low-power CMOS technology [122, 126] as described in Chap. 3. Figure 6.38(a) shows the layout of the filter and Fig. 6.38(b) depicts the chip photograph, which is not illustrative due to the planarization and passivation layers. The filter has two pins for VSS, one for VDD, two for the differential input, two for the differential output, and one pin is used to switch between the two cut-off frequencies. The filter occupies 350 µm × 220 µm active area and including the pads 500 µm × 360 µm. The filter is powered with 1.2 V supply voltage and consumes 10.3 mA, which refers to 12.36 mW, at either cut-off frequency.



(a) Layout plot



(b) Chip photograph

Fig. 6.38 65 nm CMOS 3rd-order Butterworth low-pass filter [126]

The frequency dominating elements are $C_1 = 7.4$ pF, $C_2 = 20.6$ pF, $R_1 = 13.5$ kΩ, $C_3 = 4$ pF, $C_4 = 11$ pF, $R_2 = 11$ kΩ, $C_5 = 4$ pF, $C_6 = 22$ pF, and $R_3 = 7$ kΩ. For the resulting cut-off frequencies the parasitic gate-source capacitances and the capacitances from the switches have to be considered.

The differential DC measurement is depicted in Fig. 6.39. The low-pass filter shows a good linearity between an input current of −360 μA and +360 μA and an offset of about −20 μA.

The AC characteristics is shown in Fig. 6.40. The amplitude response as shown in Fig. 6.40(a) exhibits the two cut-off frequencies (f_c) of 1.12 MHz and 4.46 MHz. The DC gain is −0.93 dB. The phase response is shown in Fig. 6.40(b).

The distortions are determined by single-tone and two-tone measurements. In the single-tone measurement the amplitude of the input current is varied at a frequency f_{tone} at 100 kHz at a filter bandwidth of 1.12 MHz. The applied frequency f_{tone} is 400 kHz at the filter bandwidth of 4.46 MHz. Table 6.5 shows the 3rd-order harmonic distortions (HD3) in dBc (decibels relative to the carrier) against the input amplitude current.

The total harmonic distortions are measured with a frequency of 100 kHz and 400 kHz at the −3 dB cut-off frequencies of 1.12 MHz and 4.46 MHz, respectively. The results are shown in Table 6.6.

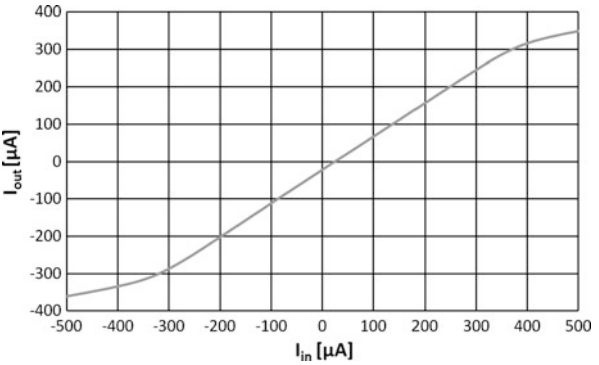
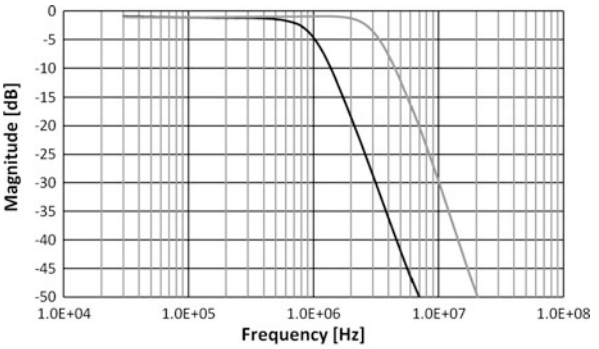
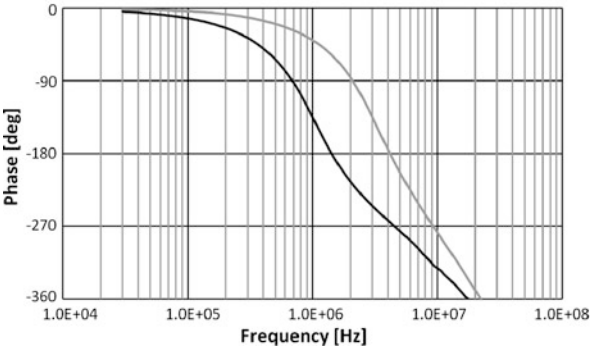


Fig. 6.39 Chip area saving 3rd-order low-pass filter–differential DC characteristics



(a) Amplitude response



(b) Phase response

Fig. 6.40 Chip area saving 3rd-order low-pass filter—frequency response

A two-tone measurement is used for a further distortion and intermodulation characterization. The filter is tested in both cut-off frequency settings. At f_c of 1.12 MHz two sinusoidal signals of 600 kHz and 700 kHz are applied and at f_c of 4.46 MHz two sinusoidal signals of 3.0 MHz and 3.2 MHz. In both -3 dB cut-off frequency configurations an input amplitude of 180 μA_p of one input signal caused an IM3 of -40 dBc. Figure 6.41 depicts the two-tone measurement at a fil-

Table 6.5 Chip area saving 3rd-order low-pass filter—measured HD3

$\hat{I}_{in}$ Signal frequency	$f_c = 1.12$ MHz $f_{tone} = 100$ kHz	$f_c = 4.46$ MHz $f_{tone} = 400$ kHz
150 µA	−55.6 dBc	−61.4 dBc
200 µA	−58.1 dBc	−62.4 dBc
250 µA	−54.2 dBc	−51.1 dBc
300 µA	−44.1 dBc	−42.3 dBc

Table 6.6 Chip area saving 3rd-order low-pass filter—measured THD1 %

f_c	$\hat{I}_{THD1\ \%}$
1.12 MHz	340 μA_p
4.46 MHz	330 μA_p

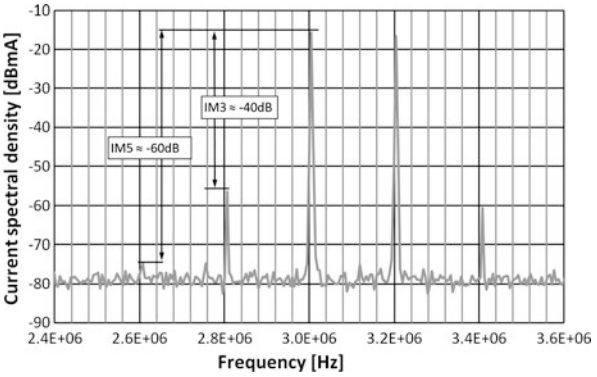


Fig. 6.41 Chip area saving 3rd-order low-pass filter—two-tone measurement at $f_c = 4.46$ MHz

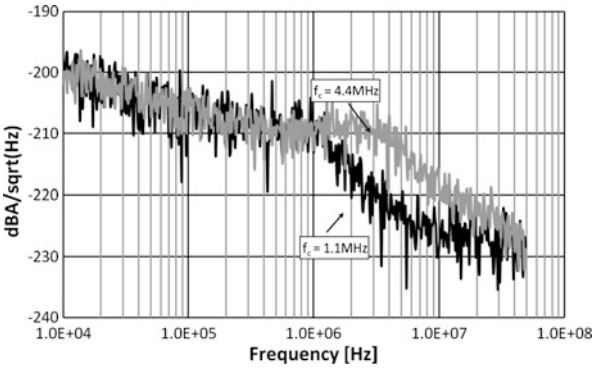


Fig. 6.42 Chip area saving 3rd-order low-pass filter—spectral noise current density

ter −3 dB cut-off frequency of 4.46 MHz. The input current of 180 μA_p at −40 dBc corresponds to a 3rd-order input intercept point (IIP3) of 1.8 mA_p.

The noise measurement is shown in Fig. 6.42 for both −3 dB cut-off frequency settings. The current noise spectral density has a dominant contribution of the 1/f

Table 6.7 Chip area saving 3rd-order low-pass filter—performance summary

Technology	65 nm CMOS	
Chip area	0.077 mm^2	
Supply voltage	1.2 V	
Power consumption	12.36 mW	
DC gain	−0.93 dB	
−3 dB cut-off frequency	1.12 MHz	4.46 MHz
$\hat{I}$ @ THD1 %	340 µA$_p$	330 µA$_p$
IIP3	1.8 mA$_p$	
DR	77.2 dB	70.9 dB
FOM$_{Filter}$	2115	2304

noise, which goes approximately up to 200 kHz. The spectral output-current noise density in the pass-band is about 31.16 pA/$\sqrt{\text{Hz}}$.

The analyses of the rating and performance is done by the criterions in Sect. 6.3. At a −3 dB cut-off frequency of 1.12 MHz the DR is 77.2 dB and the FOM$_{Filter}$ is 2115. At the other bandwidth of 4.46 MHz the DR is 70.9 dB and the FOM$_{Filter}$ is 2304. A summary of the achieved filter performance is given in Table 6.7 [122, 126].

6.6.5 A Chip Area Saving 3rd-Order Current-Mode Continuous-Time Low-Pass Filter with Virtual Ground Regulation

A 3rd-order current-mode continuous-time Butterworth low-pass filter is realized by observing the same specifications as in Sect. 6.6. The aimed −3 dB cut-off frequencies are again 1.1 MHz and 4.4 MHz. The benefit of the chip area saving strategy is exploited and additional cascode transistors of the active load transistors are used [123, 124]. Furthermore a fully differential filter topology is designed and a virtual ground regulation on the filter input is realized. The virtual ground regulation is used for lowering the input impedance. The 3rd-order current-mode low-pass filter is made of three integrator stages, as depicted in the simplified block diagram in Fig. 6.43. The frequency behavior of the 3rd-order low-pass filter is realized by appropriate feedback of the integrators which is shown analytically in the following.

The basic functional block of the filter is the integrator which is defined by the transfer function

$$H_{I1}(s) = \frac{A_o}{s} \tag{6.37}$$

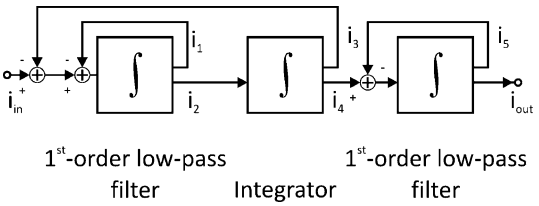


Fig. 6.43 Block diagram of the chip area saving 3rd-order low-pass filter with virtual ground regulation

where A_0 is the gain of the integrator. The integrator in negative feedback results in a first-order low-pass filter:

$$H_{LP1}(s) = \frac{1}{1 + \frac{1}{A_0}s} \tag{6.38}$$

The second-order low-pass is realized by the first-order low-pass filter in series with another integrator and its gain of B_0. Both blocks are again in negative feedback and generate the transfer function

$$H_{LP2}(s) = \frac{1}{\frac{1}{A_0 B_0}s^2 + \frac{1}{B_0}s + 1} \tag{6.39}$$

The 3rd-order low-pass filter is realized by a further integrator in feedback as in (6.38) (gain: C_0) connected to the outputs of the second-order low-pass filter. The transfer function is

$$H_{Filter}(s) = \frac{A_0 B_0 C_0}{(A_0 B_0 + A_0 s + s^2)(C_0 + s)} \tag{6.40}$$

Cascoded Current-Mode Integrator with Virtual Ground Regulation The central component of this filter is the current-mode integrator. Current-mode integrators are presented in [114, 148]. They define the transit frequency of the integrators by the integrating capacitance and the transconductances of the transistors. The proposed cascoded current-mode integrator has an additional parameter to adjust the transit frequency. The schematics and the simplified equivalent circuit is depicted in Figs. 6.44(a) and 6.44(b), respectively [124]. The integrator consists of two cross-coupled cascoded current mirrors, which are made of the transistors M_{1a} to M_{6a} and M_{1b} to M_{6b}. The cascodes are used for a better integrator accuracy. The load transistors are not cascoded, due to the limited signal headroom. For a sufficient output impedance, load transistors with large gate lengths are implemented. The output is mirrored twice, one is used for feedback purposes and the other is fed into the subsequent block. The need of mirroring the output twice is increasing the current consumption of the filter due to the current-mode signal.

The fully differential integrator functionality is realized considering some requirements. M_{1a}, M_{1b}, M_{4a}, and M_{4b} are equal in their dimensions and tagged with M_1. The cascode transistors M_{2a}, M_{2b}, M_{5a}, M_{5b}, M_{8a}, M_{8b}, M_{11a}, and M_{11b} are equal. The load transistors M_{3a}, M_{3b}, M_{6a}, M_{6b}, M_{9a}, M_{9b}, M_{12a}, and M_{12b} are

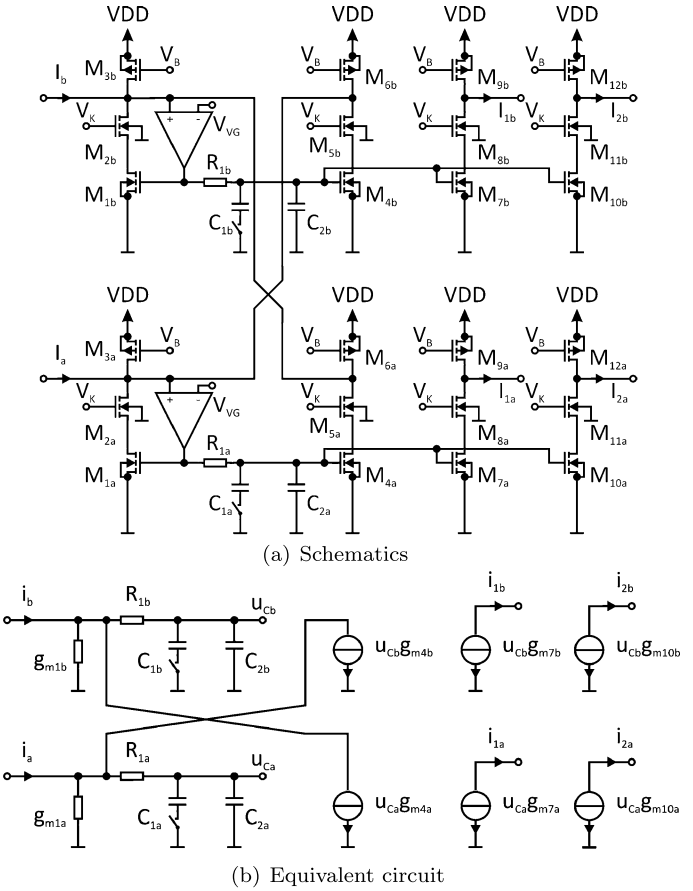


Fig. 6.44 Cascoded chip area saving current-mode integrator with virtual ground

equal as well. The output current mirroring transistors M_{7a} and M_{7b} as well as M_{10a} and M_{10b} are equal. Due to the symmetric integrator structure the resistors R_{1a} and R_{1b} are equal and denoted as R. The capacitors C_{1a} and C_{1b} and accordingly C_{2a} and C_{2b} are equal. For the following calculations they are subsumed as C. The dominant pole of the first integrator in 1st-order low-pass filter configuration is given by $R_1 = 20\ \text{k}\Omega$, $C_1 = 4.4$ pF, and $C_2 = 1.2$ pF. The transit frequency of the second integrator is defined by $R_1 = 20\ \text{k}\Omega$, $C_1 = 4.8$ pF, and $C_2 = 1.3$ pF. The last 1st-order low-pass filter is defined by $R_1 = 20\ \text{k}\Omega$, $C_1 = 4.4$ pF, and $C_2 = 1.2$ pF.

The transfer function of the integrator is calculated with respect to Fig. 6.44(b) and evaluates to

$$H_I(s) = \frac{i_{1a} - i_{1b}}{i_a - i_b} = -\frac{g_{m7}}{(1 + g_{m1}R)Cs} \tag{6.41}$$

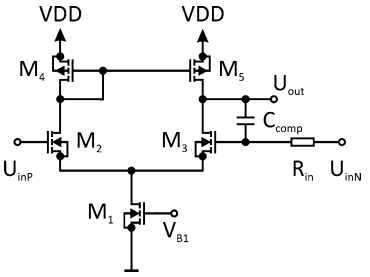


Fig. 6.45 Virtual ground regulator—schematics

Equation (6.37) clarifies the influence of the additional resistor R. Usually the capacitance C and the transconductance g_{m1} are adjusted to set the transit frequency of the integrator. The extra resistor provides an additional parameter for the transit frequency. Low transit frequencies can be accomplished by big capacitors, at the cost of large chip area, or by the increase of the transconductance g_{m1}, which is not power efficient. Increasing the resistor R is an easy way to realize low transit frequencies. Adverse is the noise of the additional resistor, thus a trade-off has to be found to meet the target specifications.

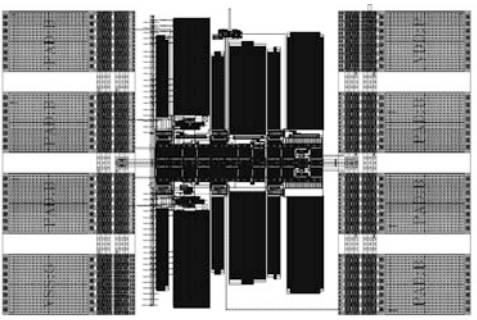
A high output impedance is realized by a large L of the load transistors. The cascode transistors are used for integrator accuracy enhancement. For the system balance the cascode transistors are also inserted in the branches of the current mirrors.

The transit frequency is switchable. Two frequency ranges are achieved by switched capacitors (C_{1a}, C_{1b}, C_{2a}, C_{2b}). The switches are realized as NMOS transistors.

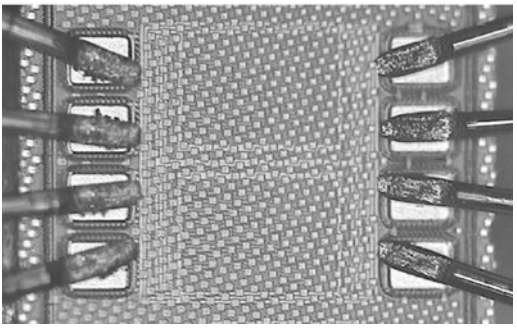
The first integrator of the 3rd-order low-pass filter has a virtual ground regulation. The schematics of the virtual ground regulator is depicted in Fig. 6.45. It contains an NMOS differential pair (M_2 and M_3) with active PMOS (M_4 and M_5) load. Biasing is done by transistor M_1 and the bias voltage V_{B1}. R_{in} decouples the set point of the virtual ground voltage from the regulation and C_{comp} is the compensation capacitor for the differential pair. The virtual ground regulation stabilizes the input voltage and reduces the input resistance. Only the first block at the input is equipped with a virtual ground regulation. The others have the input nodes directly connected to the gates of M_{1a} and M_{1b}. Apart from that the other blocks are identical to the first block.

Experimental Results The 3rd-order Butterworth low-pass filter is designed and fabricated in 65 nm LP CMOS technology. The layout plot and the chip photograph is depicted in Figs. 6.46(a) and 6.46(b), respectively. The active area of the filter is 215 µm × 221 µm and the chip area including the pads is 470 µm × 340 µm. The eight pads are assigned as VSS, VDD, cut-off frequency selection, virtual ground voltage V_{VG}, two differential inputs, and two differential outputs.

The current consumption of the entire filter is 10 mA at a supply voltage of 1.2 V, which corresponds to a power consumption of 12 mW. The virtual ground regulation sets the voltage on the input nodes to 700 mV. The differential DC measurement is



(a) Layout plot



(b) Chip photograph

Fig. 6.46 Cascoded chip area saving 3rd-order current-mode Butterworth low-pass filter with virtual ground regulation [124]

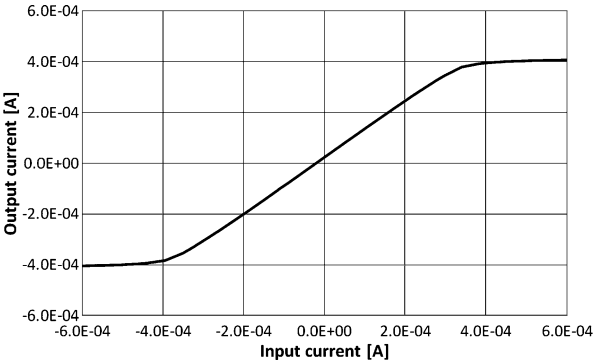
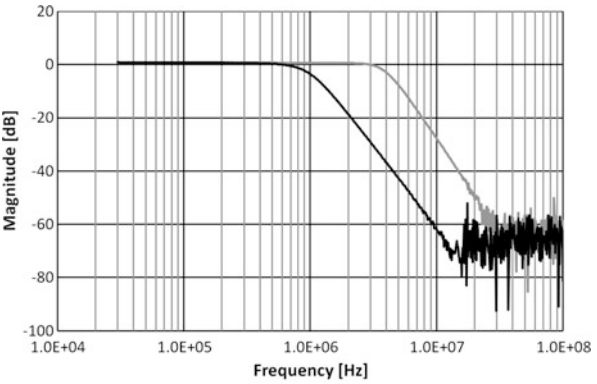


Fig. 6.47 Cascoded chip area saving current-mode 3rd-order low-pass filter with virtual ground regulation—differential DC characteristics

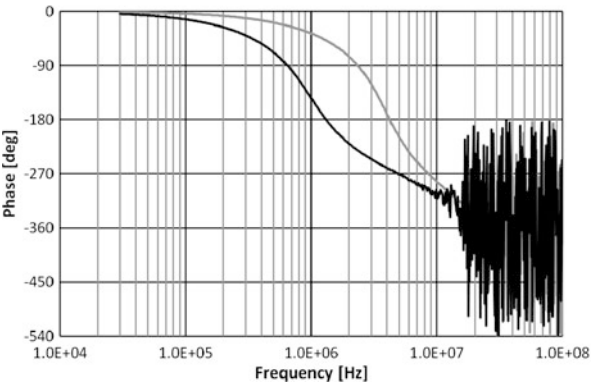
shown in Fig. 6.47 and shows good linearity from −360 µA to 340 µA input current. The filter shows an offset of 20 µA.

The measured frequency response of the cascoded chip area saving 3rd-order current-mode Butterworth low-pass filter is shown in Fig. 6.48. Figure 6.48(a) depicts two −3 dB cut-off frequencies of 1 MHz and 4 MHz, depending on the settings of the switches. The gain in the pass band is about 0.9 dB. The phase response is depicted in Fig. 6.48(b).

Harmonic distortions are measured in a single tone measurement. The input current is varied at a frequency f_{tone} of 100 kHz at a filter bandwidth of 1 MHz and at



(a) Amplitude response



(b) Phase response

Fig. 6.48 Cascoded chip area saving current-mode 3rd-order low-pass filter with virtual ground regulation—frequency response

Table 6.8 Cascoded chip area saving current-mode 3rd-order low-pass filter with virtual ground regulation—measured HD3

$\hat{I}_{in}$ Signal frequency	$f_c = 1$ MHz $f_{tone} = 100$ kHz	$f_c = 4$ MHz $f_{tone} = 400$ kHz
100 µA	−56 dBc	−55 dBc
200 µA	−49.5 dBc	−50 dBc
300 µA	−41.8 dBc	−40.5 dBc
400 µA	−35 dBc	−33.5 dBc

a frequency f_{tone} of 400 kHz at the filter bandwidth of 4 MHz. Measured 3rd-order harmonic distortions (HD3) are presented in Table 6.8.

THD1 % is measured at the same input signal frequencies. Results are given in Table 6.9.

In the two-tone measurement two sinusoidal input signals are applied and the amplitude is increased until an IM3 of −40 dB is reached. At the −3 dB cut-off frequency of 1 MHz the test signals are at 600 kHz and 700 kHz. An input amplitude of 154.5 µA of both input signals causes an IM3 of −40 dB, which corresponds to an IIP3 of 1.54 mA_p. At the −3 dB cut-off frequency of 4 MHz the test signals

Table 6.9 Cascoded chip area saving current-mode 3rd-order low-pass filter with virtual ground regulation—measured THD1 %

f_c	$\hat{I}_{THD1\ \%}$
1 MHz	322 μA_p
4 MHz	322 μA_p

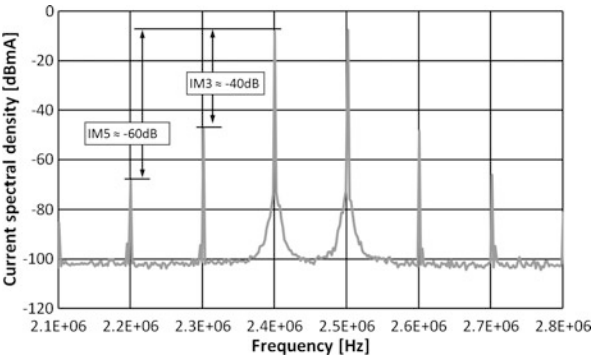


Fig. 6.49 Cascoded chip area saving current-mode 3rd-order low-pass filter with virtual ground regulation—two-tone measurement

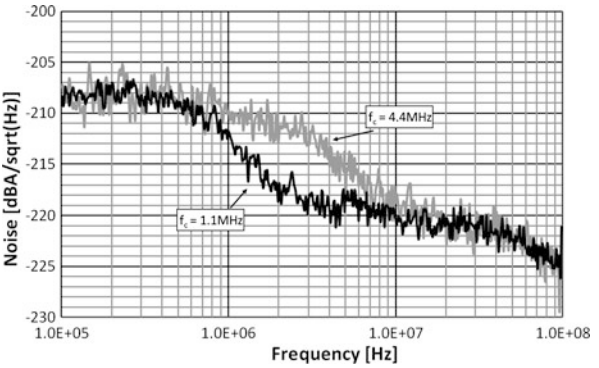


Fig. 6.50 Cascoded chip area saving current-mode 3rd-order low-pass filter with virtual ground regulation—noise measurement

are at 2.4 MHz and 2.5 MHz. An input amplitude of 154.5 µA of both input signals causes an IM3 of −40 dB, which corresponds to an IIP3 of 1.54 mA_p, as well. The two-tone measurement at the 4 MHz −3 dB cut-off frequency setting is given in Fig. 6.49.

The noise measurement is depicted in Fig. 6.50. The spectral output noise density in the pass-band is 31.6 pA/$\sqrt{\text{Hz}}$.

The 3rd-order Butterworth low-pass filter reaches at a −3 dB cut-off frequency of 1 MHz a DR of 77.3 dB and a FOM_{Filter} of 2258.9. At the −3 dB cut-off frequency of 4 MHz the DR is 71.3 dB and the FOM_{Filter} is 2238.3. A summarized overview of the filter performance is given in Table 6.10 [123, 124].

Table 6.10 Cascoded chip area saving current-mode 3rd-order low-pass filter with virtual ground regulation—performance summary

Technology	65 nm CMOS	
Chip area	0.0475 mm^2	
Supply voltage	1.2 V	
Power consumption	12 mW	
DC gain	0.9 dB	
−3 dB cut-off frequency	1 MHz	4 MHz
$\hat{I}$ @ THD1 %	322 µA$_p$	
IIP3	1.54 mA$_p$	
DR	77.3 dB	71.3 dB
FOM$_{Filter}$	2258.9	2238.3

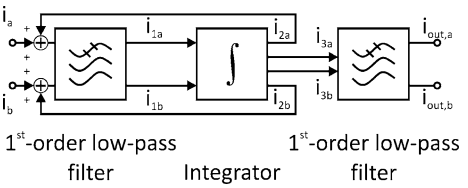


Fig. 6.51 Block diagram of the 3rd-order current-mode low-pass filter using capacitance multiplication

6.6.6 A 3rd-Order Low-Voltage Current-Mode Continuous-Time Low-Pass Filter Using Capacitance Multiplication and Virtual Ground Regulation

A 3rd-order current-mode Butterworth low-pass filter using capacitance multiplication and a virtual ground regulation on the input is realized. The block diagram is depicted in Fig. 6.51. The first block is a first-order current-mode low-pass filter including a virtual ground regulation and using a capacitance multiplication technique. The second block is a cascoded current-mode integrator. The third block is a first-order current-mode low-pass filter using again the capacitance multiplication technique, but without virtual ground regulation.

1st-Order Current-Mode Low-Pass Filter Using Capacitance Multiplication and Virtual Ground Regulation The capacitance multiplication technique is important and effective to save expensive chip area [125]. The schematics and the equivalent circuit is shown in Figs. 6.52(a) and 6.52(b), respectively.

For a 1st-order low-pass filter functionality the transistors have to be designed as following. $M_{1a} = M_{1b}$ and is denoted as M_1. $M_{3a} = M_{3b}$ and is denoted as M_3. $M_{4a} = M_{4b} = M_4$; $M_{6a} = M_{6b} = M_6$; $M_{7a} = M_{7b} = M_7$; $M_{9a} = M_{9b} = M_9$. The cascode transistors M_{2a}, M_{2b}, M_{5a}, M_{5b}, M_{8a}, and M_{8b} are equal. Long gate lengths of the load transistors are inserted due to a larger output resistance. The symmetry requires the equality of $R_{1a} = R_{1b} = R_1$, $C_{1a} = C_{1b} = C_1$, and $C_{2a} = C2b = C_2$. The switches to change the cut-off frequencies are assumed to be open

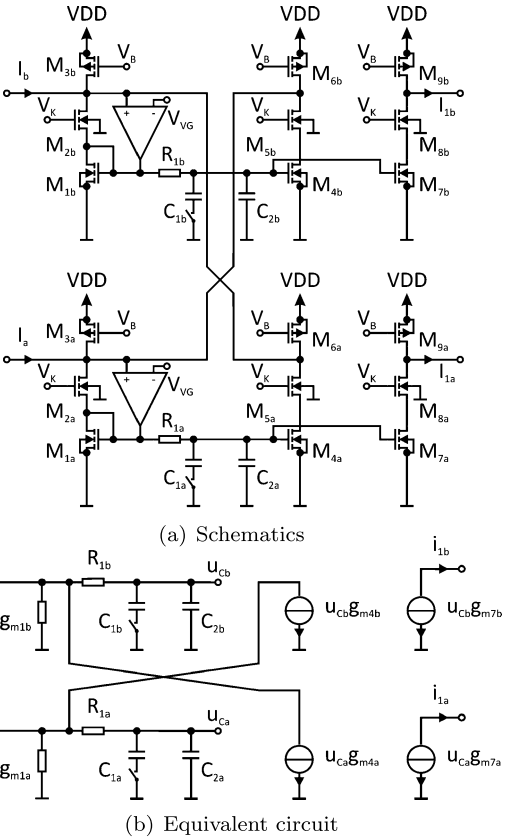


Fig. 6.52 Cascoded current-mode 1st-order low-pass filter using capacitance multiplication

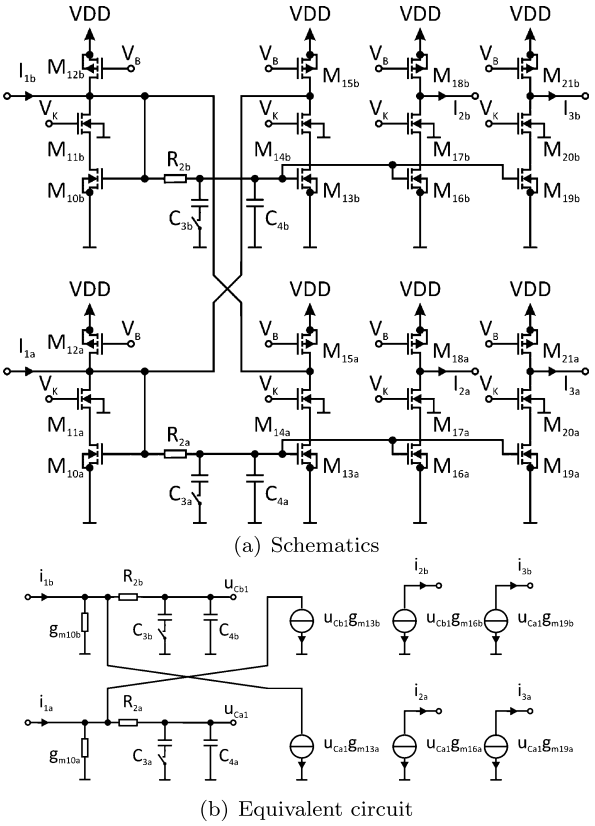
and only C_2 is active. By using this denomination the transfer function of the 1st-order low-pass filter results in

$$H_{LP}(s) = \frac{i_{1b} - i_{1a}}{i_a - i_b} = \frac{\zeta_1 \frac{g_{m7}}{g_{m1}}}{\zeta_1 C_2 (R_1 + \frac{1}{g_{m1}})s + 1} \tag{6.42}$$

In (6.42) the factor ζ_1 is called the capacitance multiplication factor and is defined as

$$\zeta_1 = \frac{g_{m1}}{g_{m1} - g_{m4}} \tag{6.43}$$

A 1st-order low-pass filter behavior needs the condition of the transconductances $g_{m4} < g_{m1}$. Equation (6.42) points out that an increase of the capacitance multiplication factor ζ_1 shifts the cut-off frequency to lower frequencies. The capacitance multiplication factor can be raised by increasing the transconductance g_{m4}. The proposed 1st-order low-pass filter has a ζ_1 of 3. The new development results in an enlargement of the effective capacitance of 30 %. However, the saving of chip area is at the cost of the dynamic range. Due to the current-transmission ratio the current



(a) Schematics

(b) Equivalent circuit

Fig. 6.53 Cascoded current-mode integrator without virtual ground regulation

in M_4, M_5, and M_6 is smaller than in M_1, M_2, and M_3. The gain of the 1st-order low-pass filter can be adjusted by the transconductance g_{m7}. The multiplication factor ζ_1 can be increased by approaching g_{m4} to g_{m1}. However, process tolerances have to be considered and $g_{m4} < g_{m1}$ has to be assured. Therefore a ζ_1 of 3 is used.

Cascoded Current-Mode Integrator The second block of the 3rd-order current-mode low-pass filter, the integrator, is shown in Fig. 6.53. The transfer function is given by

$$H_I(s) = \frac{i_{2b} - i_{2a}}{i_{1a} - i_{1b}} = \frac{i_{3b} - i_{3a}}{i_{1a} - i_{1b}} = \frac{g_{m10}}{(1 + g_{m10}R_2)C_4 s} \tag{6.44}$$

under the following assumptions: The transistors $M_{10a} = M_{10b} = M_{13a} = M_{13b} = M_{16a} = M_{16b} = M_{19a} = M_{19b}$ are equal and denoted as M_{10}. The load transistors are equal: $M_{12a} = M_{12b} = M_{15a} = M_{15b} = M_{18a} = M_{18b} = M_{21a} = M_{21b}$. The cascode transistors are equal: $M_{11a} = M_{11b} = M_{14a} = M_{14b} = M_{17a} = M_{17b} = M_{20a} = M_{20b}$. The cascodes provide a better integrator accuracy. The resistors R_{2a} and R_{2b} are equal and denoted as R_2, the capacitors C_{3a} and C_{3b} are equal and denoted as C_3. The capacitors C_{4a} and C_{4b} are equal and denoted as C_4. The switch

is assumed to be open and the effective capacitance is C_4. The output is mirrored twice because of the current-mode signal which increases the current consumption of the filter.

By combining (6.42) and (6.44) the 2nd-order low-pass filter results in

$$H_{LP2} = \frac{g_{m7} g_{m10} \zeta_1}{Ds^2 + Es + F} \tag{6.45}$$

The coefficients D, E, and F represent:

$$D = C_2 C_4 \zeta_1 (R_1 g_{m1} + 1)(1 + g_{m10} R_2) \tag{6.46}$$

$$E = (1 + g_{m10} R_2) C_2 g_{m1}, \quad \text{and} \tag{6.47}$$

$$F = \zeta_1 g_{m7} g_{m10} \tag{6.48}$$

The final 3rd-order current-mode Butterworth low-pass filter is realized with another 1st-order current-mode low-pass filter using capacitance multiplication as introduced in Fig. 6.52. The only difference is the omitted virtual ground regulation. With a consecutive numbering of the circuit devices the 3rd-order Butterworth low-pass filter results in

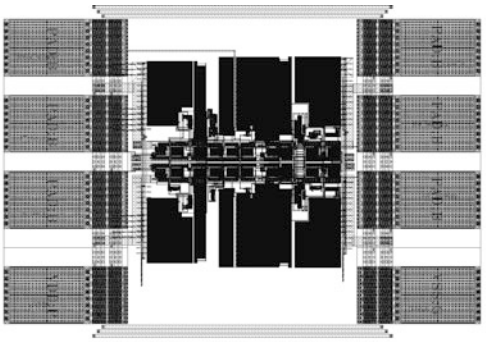
$$H_{Filter}(s) = \frac{g_{m7} g_{m10} \zeta_1}{Ds^2 + Es + F} \cdot \frac{\zeta_2 \frac{g_{m28}}{g_{m22}}}{\zeta_2 C_6 (R_3 + \frac{1}{g_{m22}}) s + 1} \tag{6.49}$$

Measurement Results The 3rd-order Butterworth low-pass filter is designed and fabricated in 65 nm LP CMOS technology. The active area of the filter is 215 µm × 215 µm and the chip size including the pads is 510 µm × 360 µm. The layout plot is shown in Fig. 6.54(a) and the chip photograph is depicted in Fig. 6.54(b). The chip pins are VSS, VDD, cut-off frequency select, virtual ground voltage V_{VG}, two differential inputs, and two differential outputs.

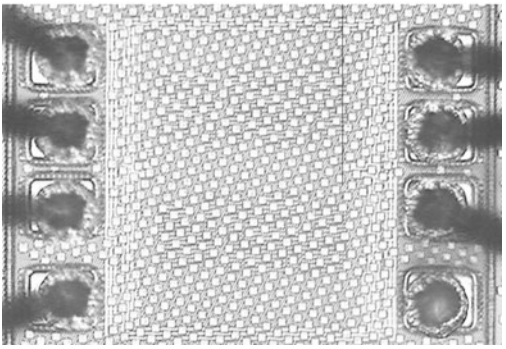
The supply voltage of the 3rd-order current-mode Butterworth low-pass filter is only 1 V for power saving reasons at a current consumption of 9.6 mA. This results in a power consumption of 9.6 mW. The differential DC characteristics at a virtual ground voltage of 500 mV is shown in Fig. 6.55. The input-output current relation is linear at an input range from −480 µA to 480 µA. The offset at the output is about −50 µA at 0 V input voltage.

The frequency response in Fig. 6.56 shows the Butterworth low-pass filter characteristics at a virtual ground voltage of 500 mV. The −3 dB cut-off frequencies of 1 MHz and 4 MHz are digitally switchable. The −3 dB cut-off frequencies are determined at the input voltages of 400 mV, 500 mV, and 600 mV. In both frequency settings the deviation of the −3 dB cut-off frequencies was lower than 1 %. The filter has a gain of 4 dB at all three virtual ground voltages at the input node.

Single-tone measurements were performed to show the in-band distortions. The results are given in Table 6.12 for the two −3 dB cut-off frequencies of 1 MHz and 4 MHz and for the input node voltages of 400 mV, 500 mV, and 600 mV.



(a) Layout plot



(b) Chip photograph

Fig. 6.54 Low-voltage 3rd-order current-mode Butterworth low-pass filter using capacitance multiplication [125]

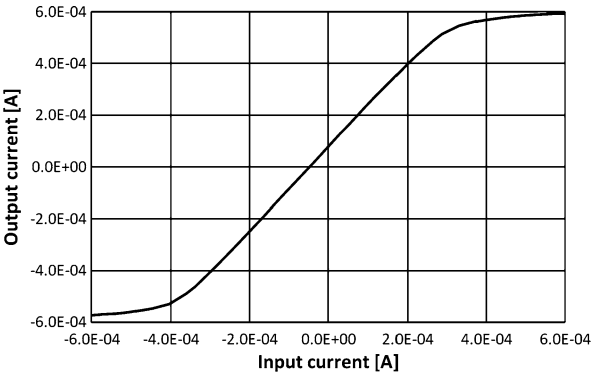
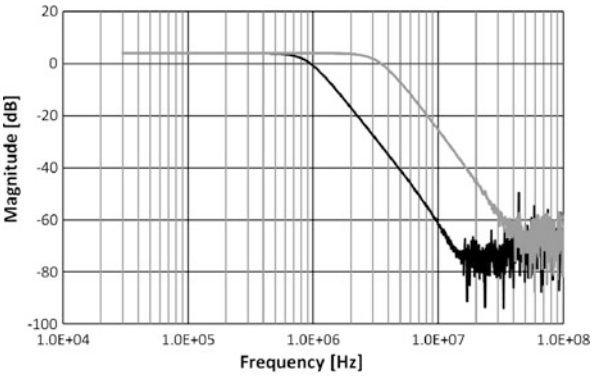


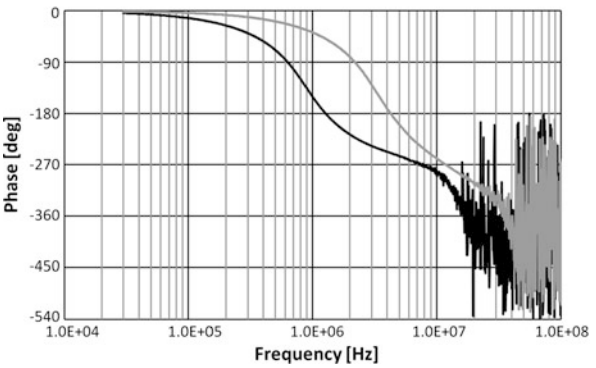
Fig. 6.55 Current-mode 3rd-order low-pass filter using capacitance multiplication—differential DC characteristics

The THD1 % is measured at all three virtual ground voltages. The test signal frequency at the −3 dB cut-off frequency of 1 MHz and 4 MHz was 100 kHz and 400 kHz, respectively. The input amplitudes which lead to 1 % THD are listed in Table 6.11.

Two-tone measurements were performed in order to identify the 3rd-order intermodulations. The frequencies of the two sinusoidal input signals at 1 MHz −3 dB cut-off frequency were 500 kHz and 600 kHz. The amplitude of both input signals



(a) Amplitude response



(b) Phase response

Fig. 6.56 Current-mode 3rd-order low-pass filter using capacitance multiplication—frequency response

are raised until a IM3 of −40 dB is reached. The resulting amplitudes of both input signals at different virtual ground voltages and the corresponding IIP3 are denoted in Table 6.13. The frequencies of the input signals at $f_c = 4$ MHz were 2.4 MHz and 2.5 MHz. The results are given in Table 6.13 as well.

The spectral output noise current density at a virtual ground voltage of $V_{VG} =$ 500 mV is depicted in Fig. 6.57. The average spectral output noise density in the pass-band is 40 $\text{pA}/\sqrt{\text{Hz}}$ which corresponds to an input referred average noise density of 25 $\text{pA}/\sqrt{\text{Hz}}$.

The presented low-voltage current-mode 3rd-order Butterworth low-pass filter using capacitance multiplication has a DR of 73.8 dB and a FOM_{Filter} of 3873 at the −3 dB cut-off frequency of $f_c = 1$ MHz. At $f_c = 4$ MHz the DR is 67.8 dB and the FOM_{Filter} results in 4034. A performance summary of the filter is printed in Table 6.14 [125].

6.7 Comparison to the State-of-the-Art

For the comparison to the state-of-the-art Table 6.15 lists the most important key data of various current-mode filters which are mentioned in the state-of-the-art

Table 6.11 Current-mode 3rd-order low-pass filter using capacitance multiplication—measured THD1 %

f_c	$\hat{I}_{THD1\ \%}@V_{VG} = 0.4$ V	$\hat{I}_{THD1\ \%}@V_{VG} = 0.5$ V	$\hat{I}_{THD1\ \%}@V_{VG} = 0.6$ V
1 MHz	272 μA_p	277 μA_p	277 μA_p
4 MHz	272 μA_p	277 μA_p	268 μA_p

Table 6.12 Current-mode 3rd-order low-pass filter using capacitance multiplication—measured HD3 for different virtual ground voltages

$\hat{I}_{in}$ Signal frequency	$f_c = 1$ MHz $f_{tone} = 100$ kHz	$f_c = 4$ MHz $f_{tone} = 400$ kHz
V_{VG}	400 mV	
100 µA	−55.8 dBc	−57.5 dBc
150 µA	−54 dBc	−50.8 dBc
200 µA	−50 dBc	−48.1 dBc
250 µA	−44.8 dBc	−42.6 dBc
300 µA	−39 dBc	−36.8 dBc
V_{VG}	500 mV	
100 µA	−52.5 dBc	−52.4 dBc
150 µA	−54.5 dBc	−51.6 dBc
200 µA	−49.2 dBc	−49.2 dBc
250 µA	−45.5 dBc	−43.7 dBc
300 µA	−38.5 dBc	−37.8 dBc
V_{VG}	600 mV	
100 µA	−58 dBc	−52.6 dBc
150 µA	−54 dBc	−53.8 dBc
200 µA	−48.9 dBc	−50.9 dBc
250 µA	−45.4 dBc	−43.5 dBc
300 µA	−39.8 dBc	−38.8 dBc

(Sect. 6.5). Unfortunately only a small number of publications of current-mode filters in deep-sub-micron and nanometer CMOS are available, hence older micrometer and sub-micrometer technologies are involved in the comparison as well. Voltage-mode counterparts are omitted in the comparison due to their inherently different structure and performance. For example, current-mode circuits need sufficient bias currents to guarantee a good distortion behavior. In general, circuits in deep-sub-micron and nanometer CMOS technologies have a higher power consumption at the same performance compared to circuits in micron and submicron technologies as explained in Chap. 3. The effect of 1/f noise in deep-sub-micron and nanometer CMOS technology is considerable; especially in filters with low cut-off frequencies the noise has a significant impact on the filter performance. The figure of merit tries to combine significant filter characteristics to show the filter perfor-

Table 6.13 Current-mode 3rd-order low-pass filter using capacitance multiplication—intermodulation measurements

Signal frequencies	$f_c = 1$ MHz $f_{tone1} = 500$ kHz $f_{tone2} = 600$ kHz	$f_c = 4$ MHz $f_{tone1} = 2.4$ MHz $f_{tone2} = 2.5$ MHz
V_{VG}	400 mV	
$\hat{I}_{in}$	164 μA_p	154 μA_p
IIP3	1.6 mA_p	1.5 mA_p
V_{VG}	500 mV	
$\hat{I}_{in}$	168 μA_p	159 μA_p
IIP3	1.7 mA_p	1.6 mA_p
V_{VG}	600 mV	
$\hat{I}_{in}$	168 μA_p	145 μA_p
IIP3	1.7 mA_p	1.5 mA_p

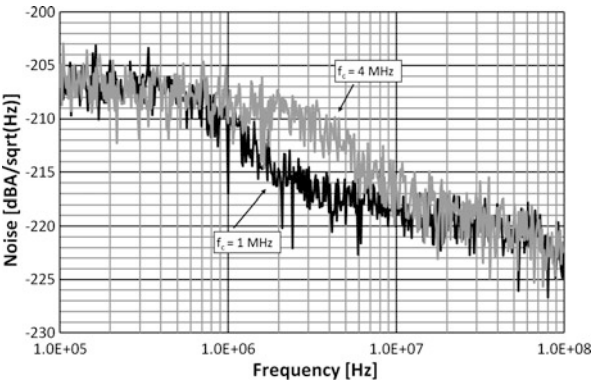


Fig. 6.57 Current-mode 3rd-order low-pass filter using capacitance multiplication—noise measurement

Table 6.14 Current-mode 3rd-order low-pass filter using capacitance multiplication—performance summary

Technology	65 nm CMOS	
Chip area	0.0462 mm^2	
Supply voltage	1.0 V	
Power consumption	9.6 mW	
DC gain	4 dB	
−3 dB cut-off frequency	1.0 MHz	4.0 MHz
$\hat{I}$ @ THD1 %	377 μA_p	
IIP3	1.7 mA_p	1.6 mA_p
DR	73.8 dB	67.8 dB
FOM_{Filter}	3873	4034

Table 6.15 Comparison to the state-of-the-art

Citation	Technology	Supply voltage	Power consumption	Filter order	−3 dB frequency cut-off	Active area	DR	FOM_{Filter}
State-of-the-art								
[68]	2 µm CMOS	5 V	24 mW@30 MHz	5	25–50 MHz	n.a.†	n.a.†	n.a.†
[69]‡	2 µm CMOS	5 V	25.5 mW@40 MHz	5	24–42 MHz	0.28 mm^2	69 dB	484
[149]‡	1.2 µm CMOS	3 V	18 mW	3	125 MHz	0.009 mm^2	62 dB	914
[114]‡	2 µm CMOS	3.3 V	4 mW	6	7.5–13.5 MHz	0.774 mm^2	52 dB	12694
[148]‡	1.2 µm CMOS	1.5 V	375 µW	5	300 kHz–1 MHz	0.5 mm^2	67 dB	860
[92]‡	digital CMOS†	1.2 V	1.16 µW@5 kHz	4	20 Hz–20 kHz	n.a.†	55 dB	5535
[49]	1.5 µm CMOS	3 V	7.2 mW	3	50 MHz	n.a.†	n.a.†	n.a.†
[65]‡	0.5 µm CMOS	3.3 V	91 mW	5	50 MHz	0.56 mm^2	60 dB	10985
[25]	0.25 µm CMOS	1 V	24 mW	8	277–326 MHz	n.a.†	n.a.†	n.a.†
[40]	0.8 µm CMOS	3 V	n.a.†	2	80 MHz	n.a.†	n.a.†	n.a.†
[144]	1.2 µm CMOS	5 V	20 mW	5	160 Hz–5.6 kHz	0.4 mm^2	n.a.†	n.a.†
[63]	0.35 µm CMOS	3 V	n.a.†	2	1–5 MHz	n.a.†	n.a.†	n.a.†
[86]‡	0.35 µm CMOS	2 V	11.1–55.8 mW	3	42–215 MHz	0.075 mm^2	53 dB	13324
[48]	0.18 µm CMOS	1.8 V	16.77 mW	3	200 MHz	0.303 mm^2	n.a.†	n.a.†
[28]‡	1 µm CMOS	3 V	5 mW	5	10 MHz	n.a.†	50 dB	30179
[67]‡	0.35 µm BiCMOS	1.5 V	21.1 µW	5	482 kHz	n.a.†	40.6 dB	23013
Own publications								
[62]‡	120 nm CMOS	1.5 V	3.9 mW	3	0.8–1.2 MHz	0.0925 mm^2	73.1 dB	1922
[62]‡	120 nm CMOS	1.5 V	3.9 mW	3	3.5–4 MHz	0.0925 mm^2	68.8 dB	1293

Table 6.15 (Continued)

Citation	Technology	Supply voltage	Power consumption	Filter order	−3 dB frequency cut-off	Active area	DR	FOM_{Filter}
[61]‡	65 nm CMOS	1.2 V	6.3 mW	3	0.95 MHz	0.054 mm^2	56.7 dB	142625
[61]‡	65 nm CMOS	1.2 V	6.3 mW	3	3.75 MHz	0.054 mm^2	52.6 dB	92873
[60]‡	65 nm CMOS	1.2 V	8.16 mW	3	0.98 MHz	0.092 mm^2	72.5 dB	4710
[60]‡	65 nm CMOS	1.2 V	8.16 mW	3	4.06 MHz	0.092 mm^2	66.6 dB	4432
[126]‡	65 nm CMOS	1.2 V	12.36 mW	3	1.12 MHz	0.077 mm^2	77.2 dB	2115
[126]‡	65 nm CMOS	1.2 V	12.36 mW	3	4.46 MHz	0.077 mm^2	70.9 dB	2304
[123]‡	65 nm CMOS	1.2 V	12 mW	3	1 MHz	0.0475 mm^2	77.3 dB	2259
[123]‡	65 nm CMOS	1.2 V	12 mW	3	4 MHz	0.0475 mm^2	71.3 dB	2238
[125]‡	65 nm CMOS	1 V	9.6 mW	3	1 MHz	0.0462 mm^2	73.8 dB	3873
[125]‡	65 nm CMOS	1 V	9.6 mW	3	4 MHz	0.0462 mm^2	67.8 dB	4034

†... not available

‡... plotted in Fig. 6.58

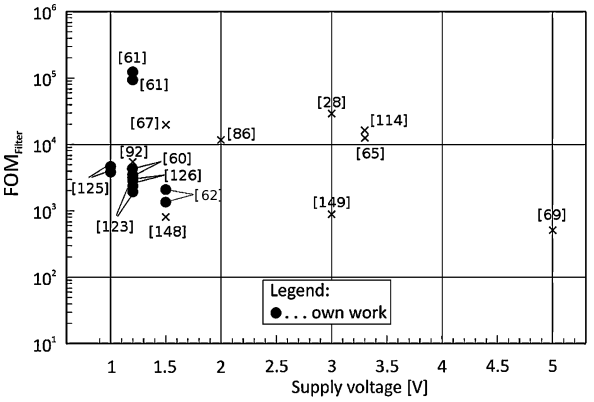


Fig. 6.58 Figure of merit of current-mode filters—state-of-the-art

mance. Generally, a fair and comprehensive comparison by just one figure of merit is difficult. The figure of merit, as given in (6.12), is printed against the supply voltage in Fig. 6.58, if calculable. It should be kept in mind, lower values of FOM_{Filter} are better.

Simulation results of a 5th-order leapfrog all-pole low-pass filter are presented in [68]. The filter is designed in 2 µm CMOS and has a 5 V supply voltage. Not any numbers of noise or dynamic range are given, hence a FOM_{Filter} cannot be calculated. A good FOM_{Filter} is reached in [69] (2 µm CMOS) and [149] (1.2 µm CMOS) due to the extensive use of cascoding in the current amplifier of the filter at a high supply voltage (5 V and 3 V). A moderate FOM_{Filter} and DR is reached in [114] even in 2 µm CMOS at a 3.3 V supply voltage and a power consumption of 4 mW. An ultra low-power current-mode filter is presented in [148], which reaches a good FOM_{Filter}. The supply voltage is 1.5 V and the power consumption is 375 µW at a −3 dB cut-off frequency of 525 kHz. Only simulations are presented in [92] and reach a good FOM_{Filter}, although the used technology is not mentioned. The 4th-order Chebyshev low-pass filter consumes only 1.16 µW at a bandwidth of 5 kHz. Simulation results for a 3rd-order Butterworth filter at 3 V supply voltage and 7.2 mW power dissipation are presented in [49]. No FOM_{Filter} is available due to missing noise, distortion, and DR figures. The power consumption in [65] is extremely high at a supply voltage of 3.3 V because of the high bias currents. These are needed for a low distortion filter design. However, the high power consumption (18.8 mW per pole) leads to a moderate FOM_{Filter} in 0.5 µm CMOS. Results in [25] and [40] are achieved only by simulations in 0.25 µm CMOS and 0.8 µm CMOS, respectively. Distortions and noise performance are missing, hence a FOM_{Filter} cannot be calculated. Measurement results of a 5th-order Butterworth filter in 1.2 µm CMOS at 5 V supply voltage are presented in [144]. Anyhow no FOM_{Filter} is available due to missing THD1 % and noise figures. A current-mode square-root domain filter in 0.35 µm CMOS is presented in [63]. Not even the power consumption is reported, hence no FOM_{Filter} is available. A more recent technology is used in [86]. At a supply voltage of 2 V and power consumption of 3.73 mW per pole only a decent DR of 53 dB and a moderate FOM_{Filter} is reached. A filter in 0.18 µm tech-

nology is presented in [48]. The filter consumes 16.77 mW at 1.8 V supply voltage. Unfortunately THD1 % or the DR is missing, a FOM_{Filter} is not available. A 5th-order low-pass filter is presented in [28]. Simulations in 1 µm CMOS with a power consumption of 5 mW show a moderate FOM_{Filter} and DR with a high supply voltage. [67] is the only representative of a current-mode filter in a 0.35 µm BiCMOS technology at a supply voltage of 1.5 V. It is an ultra low-power design (21.1 µW) with a low −3 dB cut-off frequency at the cost of a high DR, hence the FOM_{Filter} is moderate.

[123, 125, 126] are own designs in low-power 65 nm CMOS technology and all presented results are measurements. The nanometer CMOS technology issues are solved and these designs reach good DR and FOM_{Filter} figures. Using capacitance saving techniques and capacitance multiplication for current-mode integrators up to 30 % capacitor area could be saved. Despite the system specified low cut-off frequencies the 1/f noise does not deteriorate the integrated noise too much. [123, 125] are realized with virtual ground regulations. This is at the cost of chip area and current consumption, which affects the FOM_{Filter} negatively as well.

Chapter 7
Operational Amplifier RC Low-Pass Filter

Several applications pose challenges for wireless receivers due to close blockers in the frequency spectrum. This requires amplifiers and filters with a high linearity. Due to the challenges of the nanometer hell of physics concerning design of operational amplifiers, new circuit architectures will be investigated. In fact, it will turn out that the low supply voltage of nanometer CMOS circuits is the most limiting factor to achieve a good linearity and a large dynamic range. A high-voltage operational amplifier finally will show the best performance in a filter-mixer combination. In addition, 1/f noise will turn out to reduce the choice of usable mixer topologies considerably.

7.1 Motivation and Application in DVB-H and LTE

Handheld terminals, such as mobile phones, mobile computers, or personal digital assistants (PDA) increase their functionalities for marketing reasons. In order to boost the sales figures the scope of operation ranges from various sensors, like GPS and several interfaces, like Bluetooth and WLAN, to entertainment, like internet or gaming. Television (TV) is an important fraction in entertainment industries, hence television is offered for handheld mobile terminals. Nearly every device, like a mobile phone, a music player, or even a camera has a suitable display and can be used for the information transport. Entertainment and news are a constant companion all-around and at any time for a huge mass of customers.

Watching television on mobile phones, mobile television, is already available via the universal mobile telecommunication system (UMTS). UMTS was designed to join existing digital cellular systems together with future terrestrial and satellite communication services. UMTS covers voice services, messaging, fax, data communication, video streaming, local area networks, teleshopping, and information distribution. UMTS increases the density of mobile devices and allows a large amount of UMTS terminals in parallel use. For video streaming applications UMTS has some inherent structural weaknesses. These are poor data rates and its unicast

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oriented data transmission. Unicast data transmission is defined as a point-to-point connection with an exclusive information transfer between one transmitter and one receiver. However, unicast communication is pretty inefficient and expensive, if many receiving terminals demand the identical data stream like in television. Every video stream is transferred separately and stresses the service environment [93].

A broadcast network is more efficient for serving information to numerous customers compared to an unicast network. An existent and widely spread TV broadcast service is digital video broadcasting—terrestrial (DVB-T). The physical radio transmission of DVB-T is performed by orthogonal frequency division multiplex (OFDM) multi carrier modulation. It allows high-speed point-to-multipoint connections with the possibility to receive the broadcast service with portable devices. TV is available at a speed range that reaches from pedestrians to fast moving cars. DVB-T is used in many countries and hence, it has a huge geographical coverage.

The existent standard of DVB-T together with its suitability for fast moving television receivers caused the development of the standard for digital video broadcast—handheld (DVB-H). DVB-H is compatible to DVB-T to a large extent. Hence there is no need to establish a new and expensive broadcast network, the existing can be employed. DVB-H is optimized for mobile multimedia devices which results in some challenges:

- They have no external power supply and are battery supplied, are light weighted and pocket sized. The limited power consumption is important for long operating time.
- The broadcast service provides audio and video streaming in adequate quality. Sufficient data rates are necessary.
- Mobility is a fundamental factor for handheld devices. Television reception should be possible indoor and outdoor at a speed from walking to driving. The antenna of the mobile system has limited dimensions and cannot be adjusted to the sender while moving. Multiple antennas are impossible due to space restrictions. Occurring transmission errors have to be corrected and a time slicing technique for the transmission is used. Positive side effects of the time slicing are battery power saving and a soft handover between two adjacent transmission cells.
- Due to the re-use of the existing DVB-T broadcast network the DVB-H transmission should not interfere with DVB-T channels noticeable [64].

The successor of DVB-H is Long Term Evolution (LTE). LTE is a new and simplified data centric (all IP) core network featuring collapsed architecture and improved redundancy [83]. Important points of an LTE system are:

- high data rates up to 100 Mbps downlink and 50 Mbps uplink,
- scalable bandwidth from 1.25 MHz to 20 MHz,
- good throughput and spectrum efficiency,
- short package latency,
- operating at mobile speed up to 350 km/h in special cases,
- reduced costs, and
- interworking and handover with existing systems [8].

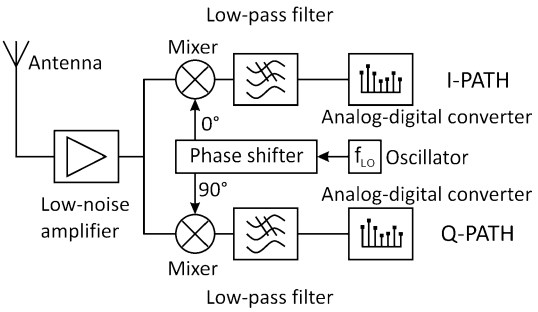


Fig. 7.1 Direct conversion receiver—architectural overview

The ambition of the work was the implementation of a first-order low-pass filter in the receiver chain of a DVB-H receiver. The overall receiver structure is a direct conversion receiver. The architectural overview is depicted in Fig. 7.1. An antenna receives the rf-signal and the low-noise amplifier boosts the signal before it is split into an in-phase (I) and a quadrature (Q) component. The mixers convert the signals directly into the base-band. The base-band signals are filtered by low-pass filters and the analog-to-digital converters convert the selected channel into the digital domain. Direct conversion receiver architectures are preferable to superheterodyne receiver architectures, especially for highly integrated and low-power systems [1].

The industry partner wished to see the improvement of a new operational amplifier in the DVB-H receiver in comparison to their prior work. Target is the implementation of the low-pass filter as a first-order operational amplifier RC low-pass filter, which converts the current-mode output signal of the passive mixer into a voltage-mode signal. Furthermore the filter amplifies the signal with 40 dB and selects the channel bandwidth of 4 MHz. For the signal conversion and amplification a first-order operational amplifier RC low-pass filter is chosen. The use of a 2nd-order low-pass filter should be avoided because it would result in a lower in-band signal-to-noise ratio. Operational amplifiers are investigated that fulfill gain bandwidth product, open-loop gain, noise, and linearity specifications for a robust and cheap receiver, that do not deteriorate the in-band phase and group delay in the DVB-H or LTE receiver.

7.2 Operational Amplifiers—An Overview

The idea of the concept of operational amplifiers (opamps) was firstly mentioned by Tellegen and called “ideal amplifier” in 1954. In 1964, Widlar created the first integrated operational amplifier. They were often used in analog calculations for mathematical operations like addition or integration. Until today operational amplifiers are very important in analog circuits and often used in various applications [52].

Ideal operational amplifiers can be seen as voltage controlled voltage sources. The basic operational amplifier offers three pins: two differential inputs v_{in}^{+} and v_{in}^{-} and one single-ended output v_{out}. The input impedance is infinite, thus no input

current is flowing into the input nodes v_{in}^{+} and v_{in}^{-}. The output impedance is zero and the output voltage v_{out} is defined by the differential input voltage $(v_{in}^{+} - v_{in}^{-})$ and the open-loop gain A_0:

$$v_{out} = \left(v_{in}^{+} - v_{in}^{-}\right) A_0 \tag{7.1}$$

The differential open-loop gain is infinite over a frequency range from DC to infinity. The common-mode rejection is infinite, i.e. the common-mode gain is zero. The use of operational amplifiers in open-loop configurations is not reasonable. Due to the high open-loop gain the output of the opamp would always be in saturation. A feedback circuit enables a well defined circuit behavior. The output is mainly defined by the feedback. The ideal operational amplifier is often used for circuit analysis. The result is a good approximation for the practical operational amplifier, however, practical operational amplifiers have non idealities [117].

Real operational amplifiers do not exhibit an ideal behavior. Important non-idealities are summarized shortly [39]. Input bias currents flow into bipolar operational amplifier inputs and cause voltage drops in the feedback network. At MOS input stages the input bias currents are in general very small. In nanometer CMOS technologies tunneling currents result in increasing input bias currents. The input offset current is the difference between the input bias currents and is caused due to mismatch. The input offset voltage is the differential input voltage, which drives the output to zero and is also caused by mismatch. The common-mode input range is the range of the input DC voltage level at which all transistors in the input stage are in their active region. The common-mode rejection ratio describes the effect of a common-mode input signal to the output. The influence of variations in the power supply at the operational amplifier output is described by the power supply rejection ratio.

The input resistance can usually be neglected in feedback configuration due to the high voltage gain of the operational amplifier. In MOS input stages the input resistance is near infinity. Transistor properties of nanometer CMOS like tunneling currents, however, reduce the input resistance. The output resistance is caused by the output stage of the operational amplifier. The output resistance has a negligible influence on the closed-loop performance, provided that the output resistance in combinations with the load keeps the operational amplifier stable.

The frequency response of a real operational amplifier declines towards high frequency due to the internal parasitic nodes. To ensure closed-loop stability compensation capacitances are implemented. A large gain is an elementary property of operational amplifiers, which is demanding in nanometer CMOS technologies. An intrinsic gain of a transistor close to 10 and an Early voltage of about 0.3 V lead to limitations of the operational amplifier gain.

7.3 Characterization of Operational Amplifiers

The used performance and quality parameters of operational amplifiers additional to Sect. 6.3 are shortly described.

Load Capacitance The load capacitance (C_L) is an important factor in operational amplifier circuits. C_L affects the power consumption and the bandwidth of an operational amplifier.

Gain-Bandwidth Product The gain-bandwidth product (GBW) is the product of the low-frequency gain and the bandwidth. The GBW is a very important criterion in amplifier design. In operational amplifier design the GBW is determined as the frequency at which the gain of the opamp is unity.

DC Gain The DC gain or low-frequency gain is the open-loop gain of the operational amplifier. It should be high in order to sustain the approximation with an ideal opamp.

Phase Margin A operational amplifier is usually operated in negative feedback. A phase lag of 180° turns the negative feedback into positive feedback and oscillations are the possible consequence. Oscillations occur at a positive feedback if the gain of the opamp is greater than 1. The phase margin (PM) is the difference of the phase lag at unity gain (GBW) and the critical 180°. A PM greater than 90° guarantees no peaking, a PM converging to 0° causes peaking, and a negative PM results in oscillation.

Power Supply Rejection Ratio The power supply rejection ratio (PSRR) describes the influence of a power supply ripple on the output of the operational amplifier. The PSRR is defined as ratio of the noise in the supply rails to the resulting signal at the output. PSRR_{VDD} is the power supply rejection ratio for the positive power supply and PSRR_{VSS} is the power supply rejection ratio for the negative power supply:

$$PSRR_{VDD} = \frac{A_{dm}}{A_{VDD}} \quad \text{and} \quad PSRR_{VSS} = \frac{A_{dm}}{A_{VSS}} \tag{7.2}$$

A_{dm} denotes the differential gain, A_{VDD} is the small-signal gain from the positive power supply to the output and A_{VSS} is the small-signal gain from the negative supply to the output.

Common-Mode Rejection Ratio The common-mode rejection ratio (CMRR) determines the influence of a common-mode input signal on the output. The CMRR is defined by the ratio of the differential gain to the common-mode gain:

$$CMRR = \frac{A_{dm}}{A_{cm}} \tag{7.3}$$

A_{dm} is the differential gain and A_{cm} is the common-mode gain.

Figure of Merit A simple but often used figure of merit of operational amplifiers is defined as

$$FOM_{Opamp} = \frac{GBW\ [\mathrm{MHz}] \cdot C_L\ [\mathrm{pF}]}{I\ [\mathrm{mA}]} \tag{7.4}$$

The GBW is inserted in MHz, the load capacitance C_L in pF and I is the current consumption of the operational amplifier in mA [104].

7.4 Challenges for Operational Amplifier Design in Nanometer CMOS

Operational amplifier design in nanometer CMOS technology has notable constraints. The most important ones are shortly discussed.

Two-stage operational amplifiers are very common in micrometer and submicrometer technologies. In nanometer CMOS technologies it is difficult to achieve sufficient gain with a common two-stage design. The small channel length entails a low gain per transistor. Hence, the gain per stage is limited and more gain stages are needed to provide sufficient gain. An often used gain enhancement technique is the use of cascode transistors. Cascoding needs sufficient supply voltage for a good performance. At a low supply voltage cascodes reduce the output swing and deteriorate the operational amplifier performance. Beside cascoding other gain enlargement techniques such as gain boosting or bootstrapping do not work properly at low supply voltages [105].

Cascading is a technique that lines up the gain stages in series. The comparison of a cascoded and a cascaded amplifier results in equal gain under the assumption that the amount of cascode transistors and cascaded transistors are equal [104]. However, the current consumption in the cascade is higher due to additional bias currents. A great advantage of cascaded amplifiers is the possibility of rail-to-rail output.

The GBW of a cascoded stage, which is a single-stage amplifier, is dependent on the driven load capacitance on the output. A cascaded stage is a two-stage amplifier and an additional capacitor for compensation is needed. The compensation capacitance is an additional load to C_L, hence more current is needed to drive the entire output capacitance and the overall power consumption is increased [104].

7.5 State-of-the-Art of Operational Amplifiers

The publications of the state-of-the-art of operational amplifiers are sorted chronologically.

A low-voltage class AB operational amplifier for a sample and hold circuit is presented in [133]. The opamp is supplied with 1.5 V and needs 4.5 µA which corresponds to a power consumption of 6.75 µW. The opamp has a gain of 106 dB, a GBW of 1 MHz, and a phase margin of 47° at a load of 5 pF. The power supply rejection ratio over VDD at DC PSRR_{VDD} is 105 dB and the PSRR_{VSS} is 115 dB. The operational amplifier is designed in AMS 0.8 µm CMOS technology and has an input referred noise spectral density of 95 nA/$\sqrt{\text{Hz}}$ at $f = 1$ kHz.

A fully differential operational amplifier in 0.13 µm CMOS is introduced in [78]. The current consumption is 3.1 mA at a supply voltage of 1.5 V. A GBW of 3.2 GHz at a PM of 44° and a gain of 50 dB is achieved. The CMRR is 118 dB.

A high-speed two-stage feed-forward operational amplifier for an opamp RC filter is published in [42]. The GBW is 2.6 GHz at a moderate phase margin of 35° and a load capacitance of 300 fF. The operational amplifier has a gain of 50 dB at a supply voltage of 1.8 V and a current consumption of 4 mA. The opamp is designed in 0.18 µm CMOS technology.

A three-stage fully differential operational amplifier in 0.12 µm digital CMOS is described in [107]. The supply voltage ranges from ±0.3 V to ±0.6 V. The opamp has a gain of 86 dB at a supply voltage of ±0.6 V and a current consumption of 1.8 mA. The GBW is 46 MHz and the PM is 66° at a capacitive load of 10 pF. The fabricated chip has an active area of $155 \times 50\ \mu m^2$.

A medium-speed operational amplifier with a gain of 86 dB, a GBW of 392 MHz, and a phase margin of 73° at a C_L of 2 pF is presented in [109]. The operational amplifier consumes 12 mW at 1.8 V single power supply. The opamp is designed in a TSMC P-well 0.18 µm standard digital CMOS technology.

A high-speed fully differential operational amplifier with a two-signal-path topology is published in [106]. The opamp has a GBW at 1.5 GHz and a phase margin of 45° at a load of 3.2 pF twice. The gain is 40.4 dB and the slew-rate is 5000 V/µs. The opamp needs $100 \times 120\ \mu m^2$ active area in a 120 nm digital CMOS technology. It consumes 9.16 mA at 1.2 V supply voltage.

A fully differential six-stage opamp containing three signal paths in 0.12 µm digital CMOS technology is described in [108]. A differential gain of 120 dB at a supply voltage of 1.2 V and a power consumption of 27.5 mW is realized. At a C_L of 3.5 pF twice the opamp has a GBW of 866 MHz and a PM of 36°. The slew-rate is 890 V/µs and an active area of $0.0236\ mm^2$ is used.

A low-cost fully differential operational amplifier using a self-biased cascode output stage and a cross-coupled input stage is presented in [15]. The opamp is fabricated in 0.35 µm CMOS technology using 84 µm × 67 µm silicon area. The opamp has 60 dB DC gain and at a load of 100 pF a slew-rate of 3 V/µs, a GBW of 7.8 MHz, and a PM of 67°. The opamp pulls 0.666 mA at a supply voltage of 3.3 V.

A low-noise operational amplifier with current driving bulk technology in 0.25 µm CMOS technology with an active area of $0.01053\ mm^2$ is introduced in [73]. The opamp needs 0.94 mA at a 2.5 V supply and has a DC gain of 76 dB. Driving a 5 pF load capacitance the opamp has a GBW of 280.5 MHz and a PM of 48°.

Single-, two-, and three-stage operational amplifiers in 0.18 µm CMOS technology at a supply voltage of 1.8 V are compared in [45]. The single-stage opamp needs 35 mA to drive a 8.6 pF load capacitance twice at a GBW of 2.4 GHz and has a DC gain of 66 dB. The two-stage design has a DC gain of 27.1 dB and pulls 40 mA to drive a load of twice 7.4 pF at a GBW of 4.8 GHz. The three-stage opamp has a DC gain of 111 dB and a GBW of 1.27 GHz at a current consumption of 45 mA.

Two low-voltage class-AB operational amplifiers based on dynamic threshold voltage MOS transistors are published in [2]. Both are designed in 0.18 µm CMOS, have a supply voltage of 1 V and are loaded with a 5 pF capacitor. The first operational amplifier has a DC gain of 50.1 dB, a GBW of 26.2 MHz, and a CMRR of 78 dB at a power consumption of 550 µW. The second opamp is designed for

biomedical applications with a power dissipation of 40 µW. It has a DC gain of 53 dB and a GBW of 1.3 MHz.

A CMOS Miller operational amplifier with a 1/f noise reduction technique is presented in [55]. It is implemented in 0.13 µm CMOS technology and occupies 0.09 mm^2 active area. The chip draws 1.2 mA at a 1.5 V supply and has a GBW of 10 MHz and a DC gain of 63.2 dB.

A fully differential three-stage operational amplifier with rail-to-rail input common-mode range in 120 nm CMOS is proposed in [140]. The open-loop gain is 73 dB and the GBW is 4.4 MHz at a 5 pF load capacitance. The PM is 70° and the power consumption is 1.8 mW at 1.5 V supply. The PSRR$_{VDD}$ is 51.1 dB and the PSRR$_{VSS}$ is 54.8 dB and the CMRR is 57.3 dB. The chip area is 0.01 mm^2.

A 0.35 µm CMOS operational amplifier, which is suitable for low-voltage environments is introduced in [10]. It has rail-to-rail input and output voltage ranges. Driving a 17 pF capacitive load the opamp has a GBW of 8.1 MHz and a gain of 76.2 dB. The power dissipation is 385 µW, the CMRR is 70.5 dB at DC, the PSRR$_{VDD}$ is 45 dB, and the PSRR$_{VSS}$ is 40.5 dB. The active area is 0.0532 mm^2.

A cascoded operational amplifier with high gain in 0.35 µm CMOS technology is presented in [75]. An open-loop gain of 93 dB at a supply voltage of 3 V is achieved and the current consumption is 16.2 mA. The opamp has a phase margin of 61° at a GBW of 135 MHz and drives a load capacitor of 7 pF. The power supply rejection ratio for VSS is 58 dB and for VDD it is 68 dB. The CMRR is 40 dB.

A fully differential opamp with constant large- and small-signal behavior rail-to-rail input stage is introduced in [141]. The operational amplifier has a GBW of 135 MHz at a 15 pF load capacitance and 51° PM. The open-loop gain is 76.3 dB and the slew-rate for the rising and the falling edge is about 105 V/µs. The chip has a power consumption of 17.25 mW at a voltage supply of ±0.75 V and needs a chip area of 0.0097 mm^2 in 0.12 µm CMOS technology.

A fully differential folded cascode opamp and a fully telescopic opamp for a 40 MS/s 12-bit pipelined ADC are compared in [27]. Both are designed in 0.35 µm CMOS technology and are supplied with 3.3 V. The telescopic opamp has a DC gain of 86.4 dB and a slew-rate of 832 V/µs at a current consumption of 4.8 mA. A GBW of 570 MHz and a PM of 85.6° at a C_L of 1.4 pF are reached. The folded cascode opamp has a gain of 85.9 dB, a slew-rate of 472 V/µs and needs 4.8 mA. It is loaded with $C_L = 1.4$ pF and has a GBW of 350 MHz and a PM of 56°.

A low-voltage operational amplifier using a four-stage frequency compensation scheme is developed in [143]. The opamp has a voltage supply of 1 V and has a power dissipation of 1.4 mW. The open-loop gain is 108 dB and the GBW is 40.2 MHz at a PM of 62° driving a 500 pF load. The active area in 0.12 µm CMOS is 0.017 mm^2.

A fully differential rail-to-rail input/output with a current-mode common-mode feedback circuit for small-signal behavior control is presented in [142]. The operational amplifier is designed in 65 nm CMOS technology and needs 0.014 mm^2. The open-loop gain is 100 dB, the GBW is 40 MHz, and the phase margin is 64° at a load of 15 pF. The supply voltage is ±0.5 V and the power consumption is 0.72 mW. The operational amplifier has a PSRR at 10 Hz of 65 dB and a CMRR at 10 Hz of 74 dB. The input noise at 100 kHz is 186 nV/$\sqrt{\text{Hz}}$.

A rail-to-rail constant-g_m CMOS operational amplifier in 0.6 µm CMOS is described in [139]. An open-loop gain of 113.6 dB, a GBW of 11.9 MHz, and a PM of 53° is achieved at a supply voltage of 3 V.

A two-stage Miller operational amplifier is compared to a folded cascode opamp in 90 nm CMOS in [23]. The two-stage Miller opamp has a DC gain of 52.4 dB, a GBW of 1014 MHz, a PM of 47.4°, and a slew-rate of 697.5 V/µs. The folded cascode opamp has a DC gain of 65.7 dB and a GBW of 539.4 MHz at a PM of 7.721°. The DC gain amounts to 103.2 dB.

A low-power, high-gain, fully differential ultra-wide bandwidth operational amplifier is presented in [34]. It is supplied with 1.8 V and has a current consumption of 13.9 mA to obtain a DC gain of 65 dB. The GBW is 2.3 GHz at a phase margin of 58° and 2 pF load. The CMRR, the PSRR_{VDD}, and the PSRR_{VSS} are 96 dB, 62 dB, and 62.5 dB, respectively. The slew-rate is larger than 450 V/µs. The opamp is implemented in 0.18 µm CMOS technology and has an active area of 200 µm × 200 µm.

A pseudo differential two-stage operational transconductance amplifier in 0.18 µm CMOS technology is published in [110]. The amplifier has a DC gain of 72.8 dB and pulls a current of 0.154 mA at a supply voltage of 0.7 V. A GBW of 0.97 MHz at a PM of 70° is achieved.

7.6 State-of-the-Art of Voltage-Mode Filters

The publications of the state-of-the-art of voltage-mode filters are sorted chronologically.

A 350 MHz opamp RC filter using the operational amplifier as presented in Sect. 7.5 is implemented in [42]. The 5th-order elliptic filter has a tuning range of the −3 dB cut-off frequency from 40 MHz to 350 MHz and a gain of 0 dB. The filter has a power dissipation of 25.2 mW at a supply voltage of 1.8 V. The third-order in-band intercept point is $-13\ \text{dBV}_{rms}$ and the average noise in the pass-band is $24\ \text{nV}/\sqrt{\text{Hz}}$.

A 3rd-order Butterworth low-pass g_m-C filter is published in [145]. It is part of a transceiver designed for wireless sensor networks. The filter can handle a supply voltage range from 1.2 V to 1.8 V. The nominal −3 dB cut-off frequency is 50 kHz, however the tuning range of the cut-off frequency is between 13 kHz and 80 kHz, depending on the supply voltage. At the nominal bandwidth of 50 kHz at the supply voltage of 1.5 V the dynamic range at THD1 % is 75 dB and the power consumption is 240 µW. The PSRR_{VDD} is 30 dB and the CMRR is 47 dB. The filter is realized in 0.18 µm TSMC CMOS technology and has an active area of $0.113\ \text{mm}^2$.

A complete base-band chain for WLAN using optimized g_m stages for linearity and low-voltage operation is presented in [30]. The 6th-order elliptic low-pass g_m-C filter is supplied with 1.4 V and has a power consumption of 13.5 mW. The variable gain amplifiers provide a gain range between 13.5 and 67.5 dB. The −3 dB cut-off frequency is switchable between 1, 10, and 100 MHz. The minimum input referred noise density is $19\ \text{nV}/\sqrt{\text{Hz}}$. The filter is designed in 90 nm CMOS technology and has $0.55\ \text{mm}^2$ active area.

A 4th-order continuous-time reconfigurable Bessel low-pass filter structure for UMTS/WLAN is introduced in [19]. The filter is implemented in 0.13 µm CMOS technology and occupies 0.9 mm^2. In the UMTS mode the filter has a cut-off frequency of 2.11 MHz and a DC gain of 4 dB. The input-referred integrated noise of 36 μV_{rms} results in a DR of 81 dB. The filter has a supply voltage of 1.2 V and a power consumption of 3.4 mW. In the WLAN mode the filter has a −3 dB cut-off frequency of 11 MHz and a DC gain of 4 dB. The DR at −40 dB THD is 81 dB and the input referred noise is 36 μV_{rms}. The filter in WLAN mode needs 11.8 mA at a supply voltage of 1.2 V.

Two baseband blocks consisting of a digital-to-analog converter and a low-pass filter for WLAN/UMTS and WLAN/Bluetooth are presented in [35]. Both are realized in 0.13 µm CMOS and have a supply voltage of 1.2 V. All filters are 4th-order Bessel low-pass filters. The WLAN mode filter of the first device has a −3 dB cut-off frequency of 11 MHz, a power consumption of 5.6 mW, and a DR of 55 dB. The UMTS mode of the first device has a bandwidth of 2.5 MHz, a power consumption of 3 mW, and a DR of 58 dB. The core area of the first device combining DAC and filter is 0.8 mm^2. The WLAN mode of the second device has a similar performance as the WLAN mode of the first device. The Bluetooth mode of the second device has a −3 dB cut-off frequency of 1 MHz, a power consumption of 3 mW, and a DR of 58.2 dB. The second device has a core area of 0.7 mm^2.

A 10 MHz 4th-order Bessel low-pass filter using composite source-followers is published in [20]. The use of positive feedback enables complex poles with a single branch for a single-branch biquadratic cell. The filter consumes 2.28 mA at a supply voltage of 1.8 V. The DC gain is −3.5 dB and the DR is 79 dB at a HD3 of −40 dB. The filter is implemented in 0.18 µm CMOS technology and has an active area of 0.26 mm^2.

A 4th-order active g_m-RC Butterworth filter for a WLAN receiver with high-linearity performance, operating at very low supply voltage, is presented in [21]. The filter has a gain of 0 dB and a −3 dB cut-off frequency of 11.3 MHz. It has a supply voltage of 550 mV and a power dissipation of 3.5 mW. The in-band IIP3 is 8 dBm and the DR is 60 dB at a THD of −40 dB. The filter is implemented in 0.13 µm CMOS technology and the core area is 0.45 mm^2.

A 4th-order wideband low-power band-pass filter for wireless receivers is published in [22]. It is a cascade of two active opamp RC cells. The pass-band of the filter ranges from 300 kHz to 8 MHz and the gain is 30.6 dB. The filter is supplied with 1.2 V and has a power dissipation of 1.3 mW. The IIP3 is −10 dBm and the DR is 52 dB. The filter is designed in 65 nm CMOS technology.

A wide tuning-range 3rd-order g_m-C Butterworth filter for Bluetooth, cdma2000, Wideband CDMA, and WLAN is introduced in [76]. The filter has a tuning range from 500 kHz to 20 MHz to cover all specified cut-off frequencies. Depending on the tuned bandwidth the filter consumes 4.1 mW to 11.1 mW at a supply voltage of 1.2 V. The filter is implemented in TSMC 0.18 µm and occupies less than 0.23 mm^2.

A second-order Butterworth low-pass g_m-C filter for baseband communication in mobile radio receivers is introduced in [32]. The filter is designed in 0.18 µm CMOS technology and has a supply voltage of 1.8 V. The power consumption is 384 µW. The filter has a gain of 38 dB and a cut-off frequency of 24 MHz.

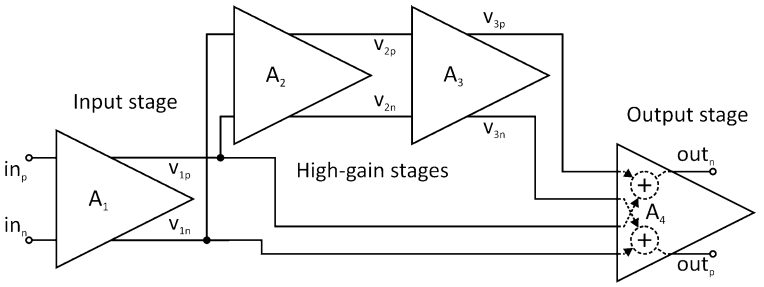


Fig. 7.2 Four-stage feed-forward operational amplifier—block diagram

7.7 Realization of Operational Amplifiers and Operational Amplifier Filters

7.7.1 A Four-Stage Feed-Forward Operational Amplifier

A four-stage operational amplifier is realized and characterized [129]. Due to low intrinsic transistor gain and the limited supply voltage, four stages are necessary to obtain sufficient gain. For high-speed purposes a feed-forward path fastens the operational amplifier. A block diagram is depicted in Fig. 7.2 for a further clarification of the internal opamp structure.

The fully differential operational amplifier is organized in an input stage A_1, a high-gain stage branch, consisting of the stages A_2 and A_3, and a summing and class AB output stage A_4. The feed-forward branch is realized from the input stage directly to the output stage. A detailed circuit schematic is depicted in Fig. 7.3. The biasing networks are omitted due to simplicity.

The input stage A_1 contains an NMOS differential pair biased by M_{3a}. For high-speed reasons the input transistors M_{1a} and M_{2a} have minimal gate length and thus cause a high level of 1/f noise. To reduce the noise contribution large W input transistors are used. The load of the differential pair are the PMOS transistors M_{4a}, M_{5a}, M_{6a}, and M_{7a}. These load transistors are split to ease a fast common mode regulation. 80 % of the load (M_{6a} and M_{7a}) is biased constantly by V_{B2a}. The remaining part (M_{4a} and M_{5a}) is used for the common-mode regulation. The effect is a reduced gain in the common-mode feedback loop but the speed is increased due to the smaller parasitic load capacitance. The operational amplifier is realized with a separate common-mode feedback (CMFB) regulation for each gain stage. The common-mode level is detected by the resistors R_{1a} and R_{2a}. The common-mode regulator is another differential pair. The resistor R_{3a} is used for ac decoupling. The FET-diode M_{13a} keeps a fundamental current through M_{10a} if the load transistors shut off and bring a faster regulation. The capacitor C_{3a} adds a dominant pole to the regulation and is used for high-frequency compensation of the common-mode feedback loop. For high frequencies the CMFB level is set by the capacitors C_{1a} and C_{2a}.

The two cascaded differential amplifiers A_2 and A_3 form the high-gain amplifiers. A_2 contains an NMOS differential pair with similar structure to the input am-

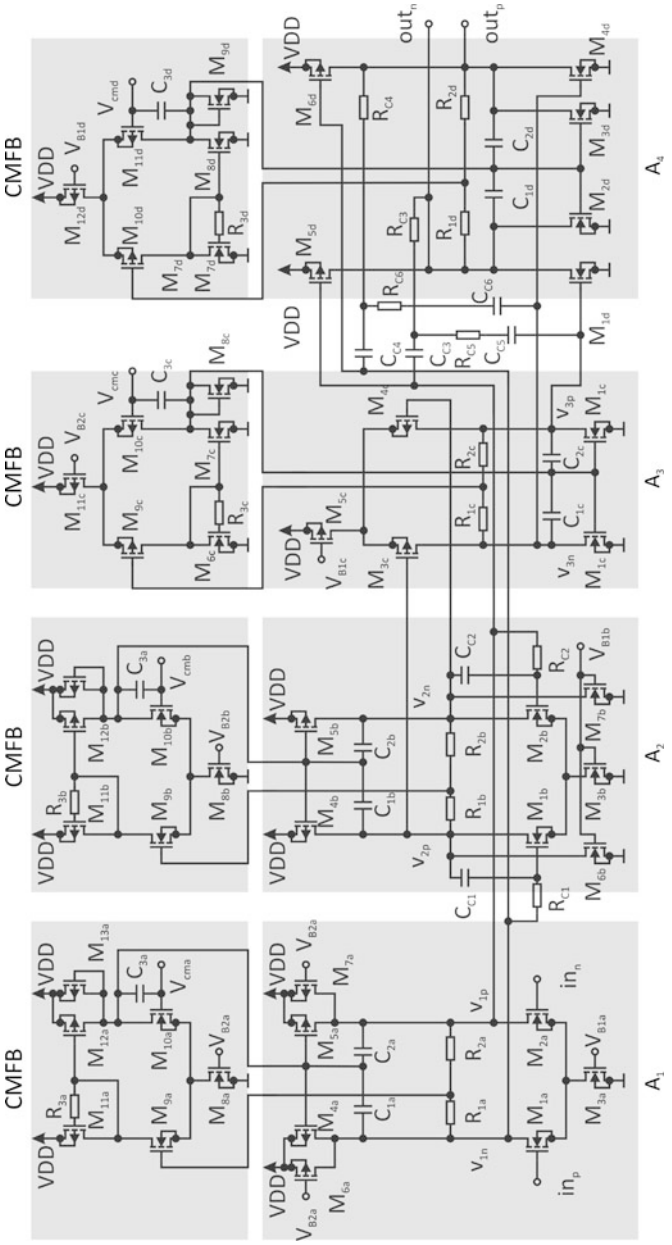


Fig. 7.3 Four-stage feed-forward operational amplifier—schematic

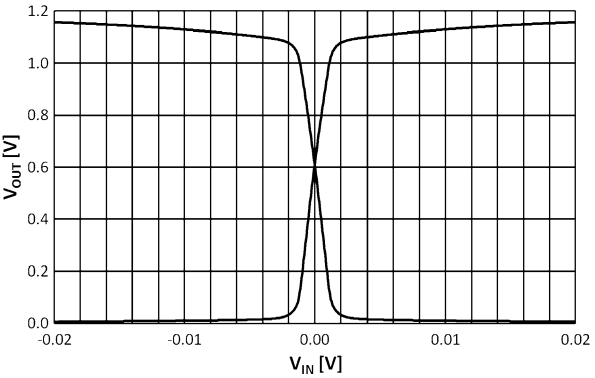


Fig. 7.4 Four-stage feed-forward operational amplifier—DC characteristics

plifier. M_{6b} and M_{7b} ensure a fundamental current even if the input transistors M_{1b} and M_{2b} shut off. In this way the delay at turn on of the load transistors M_{4b} and M_{5b} is reduced and ringing of the CFMB is minimized. The currents drawn from M_{6b} and M_{7b} are of the extent of approximately one tenth of the bias current through M_{3b}. A_3 contains a PMOS differential pair and a PMOS differential pair for the CMFB. The PMOS stage provides an output voltage range of v_{3p} and v_{3n} that is optimal for the output stage.

The output stage is a class-AB amplifier with weak AB behavior. The common-mode output voltages of A_1 and A_3 are set to ensure the AB characteristics. Besides the amplification, the output stage merges the feed-forward signal directly from A_1 and the high-gain signal directly from A_3. The CMFB uses a PMOS differential pair and the output common-mode voltage is controlled by the transistors M_{2d} and M_{3d}.

The compensation is done by a modified nested Miller compensation. The Miller network consists of the resistors R_{C3} to R_{C6} and the capacitors C_{C3} to C_{C6} [87]. The modification is the separate compensation of the high-gain branch by the elements R_{C1}, R_{C2}, C_{C1}, and C_{C2}.

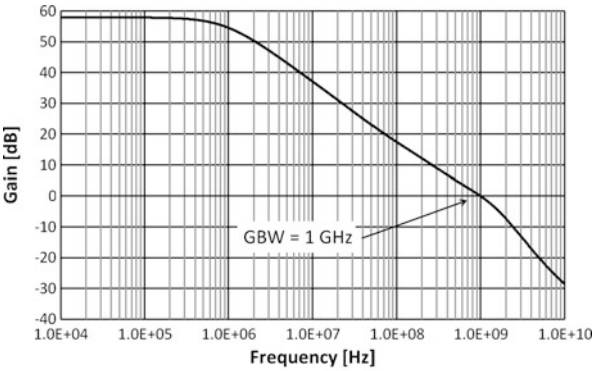
Simulation Results The operational amplifier is designed in 65 nm CMOS technology and consumes 11.4 mW power at a supply voltage of 1.2 V. The driven load is 5 pF in parallel to 10 kΩ at each output.

The DC characteristics of the opamp is depicted in Fig. 7.4. The output common-mode level is set to 600 mV. A good linearity in an input voltage range of ±1 mV is reached.

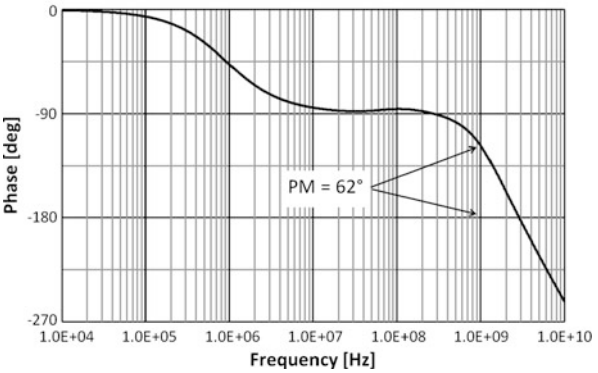
The frequency response is shown in Fig. 7.5. Figure 7.5(a) exhibits a GBW of 1 GHz and a gain of 58 dB. The phase response in Fig. 7.5(b) shows a phase margin of 62° at a load of 5 pF in parallel to 10 kΩ at each output pin.

The input referred spectral noise density is depicted in Fig. 7.6. The very dominant 1/f noise goes up to about 100 kHz. The input referred spectral noise density at 10 kHz is about 15.4 nV/$\sqrt{\text{Hz}}$ and 5.7 nV/$\sqrt{\text{Hz}}$ at 1 MHz.

The four-stage feed-forward operational amplifier reaches a FOM_{Opamp} of 1052 $\frac{\text{MHz·pF}}{\text{mA}}$. A performance summary is given in Table 7.1 [129].



(a) Amplitude response



(b) Phase response

Fig. 7.5 Four-stage feed-forward operational amplifier—frequency response

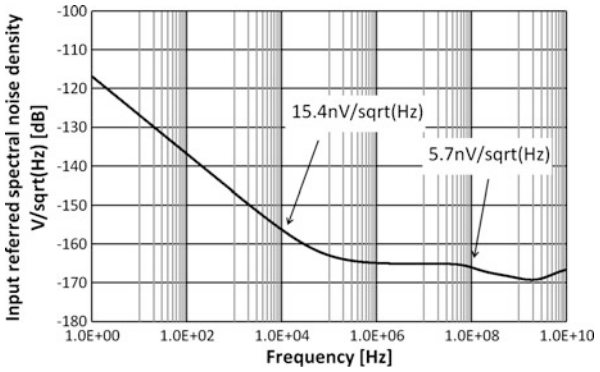


Fig. 7.6 Four-stage feed-forward operational amplifier—spectral input referred noise density

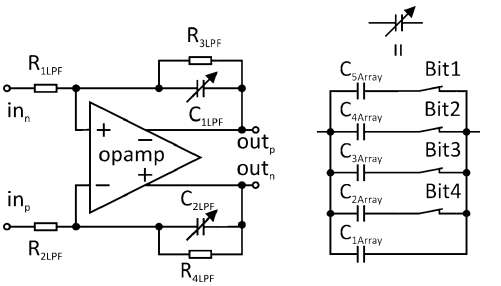
7.7.2 A First-Order Operational Amplifier RC Low-Pass Filter Using a Four-Stage Feed-Forward Operational Amplifier

The introduced four-stage feed-forward operational amplifier was not fabricated separately but is used in a first-order opamp RC low-pass filter as depicted in

Table 7.1 Four-stage feed-forward operational amplifier—performance summary

Technology	65 nm CMOS
Supply voltage	1.2 V
Power consumption	11.4 mW
DC gain	58 dB
GBW	1 GHz
Load	2×5 pF $\parallel$ 10 kΩ
PM	62°
FOM	1052 $\frac{\text{MHz·pF}}{\text{mA}}$

Fig. 7.7 First-order opamp RC filter—schematics



(a) Filter design (b) Capacitor array

Fig. 7.7. The gain of the filter is set by

$$-\frac{R_{3LPF}}{R_{1LPF}} \quad \text{and} \quad -\frac{R_{4LPF}}{R_{2LPF}} \tag{7.5}$$

The −3 dB cut-off frequency is given by

$$f_{-3\text{ dB}} = \frac{1}{2\pi C_{1LPF} R_{3LPF}} \tag{7.6}$$

or similar for C_{1LPF} and R_{3LPF}. The capacitors C_{1LPF} and C_{2LPF} are tunable in order to compensate for process variations. The capacitance tuning network is depicted in Fig. 7.7(b). The tuning network is a 4-bit controlled capacitor array, hence the cut-off frequency can be varied in $2^4 = 16$ steps. The capacitor values are 1.3 fF, 1.3 fF, 700 fF, 400 fF, and 200 fF for C_{1Array}, C_{2Array}, C_{3Array}, C_{4Array}, C_{5Array}, respectively. R_{1LPF} and R_{2LPF} are 100 Ω, which represents the equivalent mixer output resistance. R_{3LPF} and R_{4LPF} are 10 kΩ.

Measurement Results The first-order operational amplifier RC filter is designed and fabricated in 65 nm CMOS technology. A chip photo is shown in Fig. 7.8. The circuit structures are hidden by the planarization and passivation layers as well as metal fill. The chip is supplied with 1.2 V via the pins VDD and VSS, the inputs and outputs are in_p, in_n and out_p, out_n, respectively. The pins Bit1 to Bit4 are used for tuning of the −3 dB cut-off frequency. The chip occupies 0.104 mm^2 active area and 0.254 mm^2 including the pads.

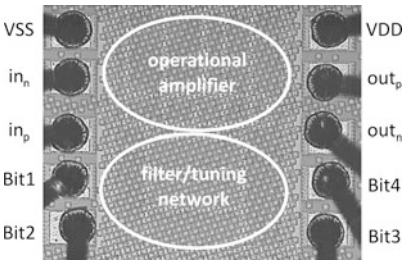


Fig. 7.8 First-order opamp RC filter—chip photo

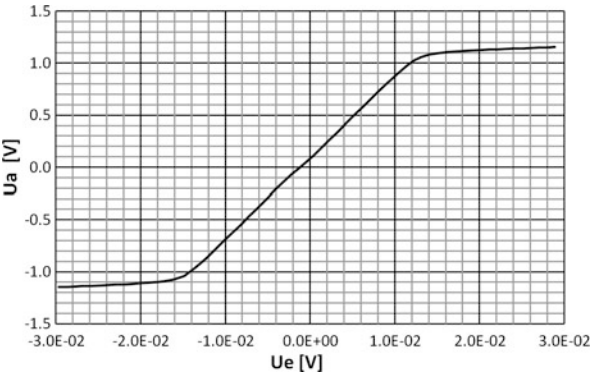


Fig. 7.9 First-order opamp RC filter—DC characteristics

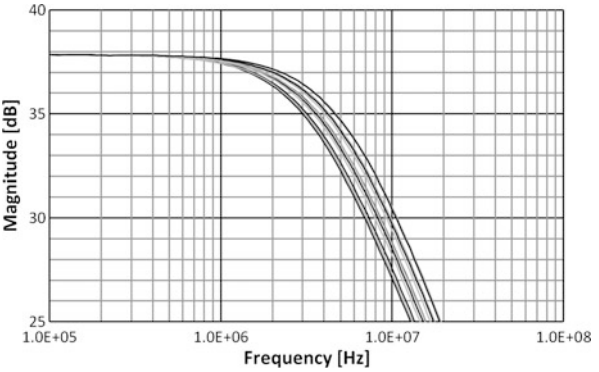


Fig. 7.10 First-order opamp RC filter—AC characteristics, tuning range

The DC filter characteristics are shown in Fig. 7.9. The low-pass filter has an almost linear output range of ±1.1 V and a 10 mV offset. The filter is loaded with approximately 1.5 pF including the pads in parallel to 4.7 kΩ on each output pin. The load represents the expected load of the following ADC.

The AC characteristics are presented in Fig. 7.10. The filter gain is 38 dB which deviates from the adjusted 40 dB due to parasitic elements in the switches and the non-ideal operational amplifier. The tuning range spans from 3.5 MHz to 4.5 MHz.

For the distortion measurements the −3 dB cut-off frequency is set to 4 MHz. For single tone distortion measurements the input signal frequency is 100 kHz, hence

Table 7.2 First-order opamp RC filter—3rd-order harmonic distortions

Output amplitude V_{pp}	HD3
2.0 V_{pp}	−45.0 dBc
2.1 V_{pp}	−48.9 dBc
2.2 V_{pp}	−41.8 dBc

Table 7.3 First-order opamp RC low-pass filter—performance summary

Technology	65 nm CMOS
Supply voltage	1.2 V
Current consumption	8.34 mA
DC gain	38 dB
3 dB cut-off frequency	3.5–4.5 MHz
Load	2×1.5 pF ‖ 4.7 kΩ
DR	57.2 dB
FOM_{Filter}	143945

HD3 and HD5 are in-band. The 3rd-order harmonic distortions at given input signals are given in Table 7.2.

The total harmonic distortions are estimated by using HD3 and HD5 (compare to (6.8)). An output signal swing of 2.15 V causes THD1 %.

The 3rd-order intermodulation products are measured in-band as well. The applied frequency of the input signals are 1 MHz and 1.1 MHz. The input amplitude of 15.5 mV of both input signals causes an IM3 of −40 dB.

The performance of the first-order opamp RC filter is rated with the dynamic range and the figure of merit. Using the simulated integrated noise from 0 to 4 MHz, a DR of 57.2 dB and a FOM_{Filter} of 143945 is reached. A summary of the filter performance is given in Table 7.3 [128].

7.7.3 A Four-Stage Multiple Feed-Forward Operational Amplifier

A fully differential four-stage operational amplifier with multiple feed-forward is designed in 65 nm CMOS [127]. Four stages are used to realize sufficient gain and two feed-forward branches enlarge the GBW of the operational amplifier. A block diagram is depicted in Fig. 7.11.

The four stages and two feed-forward branches are organized as following. After the input stage A_1 the amplified signal is split to all three remaining stages A_2, A_3, and A_4. The high-gain stages A_2 and A_3 are used for high DC gain, the feed-forward is used to keep the phase lag small. The output stage A_4 is a class AB amplifier and superposes the feed-forward signal from the input stage and the signal from the high-gain stage.

Figure 7.12 depicts a detailed schematic of the operational amplifier. The biasing networks are not shown. The input stage contains an NMOS differential pair. The in-

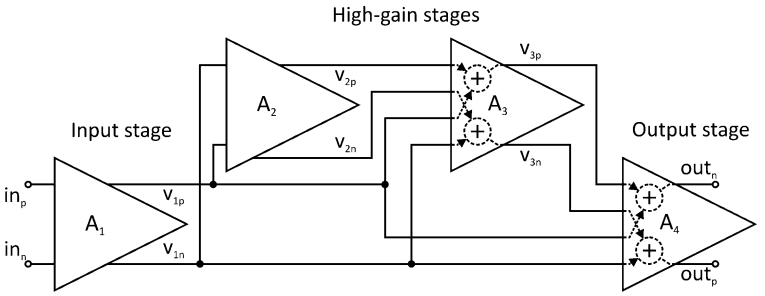


Fig. 7.11 Four-stage multiple feed-forward operational amplifier—block diagram

put transistors M_{1a}, M_{2a}, M_{3a}, and M_{4a} are common centroid to improve matching in the input stage. The current source of the differential pair is split into two parts. The first, M_{5a} is constantly biased, the latter, M_{6a}, is used for the common-mode regulation. The loads of the input stage are the resistors R_{3a} and R_{4a}. The input referred noise is significantly reduced compared to active PMOS loads, however the gain of the input stage is reduced. The common-mode regulator contains a PMOS differential pair. The common-mode level is detected by the resistors R_{1a} and R_{2a}, the target common-mode level is set by V_{cma}. The loop-control is closed via M_{6a}, which is a part of the current-source, hence the common-mode control loop is faster.

The high-gain stages are two cascaded differential amplifiers (A_2 and A_3). The first high-gain stage A_2 uses an NMOS input pair (M_{1b} and M_{2b}) for signal amplification. The amplifier is constantly biased by the current source M_{3b}. The load transistors are split. M_{4b} and M_{7b} are constantly biased. M_{5b} and M_{6b} are for the common-mode regulation. The amplifier in the common-mode regulation contains an NMOS differential pair, the common-mode level is derived by R_{1b} and R_{2b}. The reference input is V_{cmb}. A_3, the second high-gain stage contains an NMOS differential pair as well and has two inputs. M_{1c} and M_{2c} are connected at the output of the input stage, hence they act as a feed-forward in the high-gain stages and has some speed benefits. M_{5c} and M_{6c} are driven by the output of the first high-gain stage A_2. The use of M_{5c} and M_{6c} brings an additional signal amplification in the high-gain branch. M_{3c} is the fixed part of the bias of A_3 and M_{4c} is used for the common-mode regulation.

The output stage A_4 is a class AB amplifier, realized by proper common-mode voltage setting of the previous stages A_1 and A_3. The output stage amplifies and adds up the feed-forward signal of A_1 and the high-gain signal of A_3. The common-mode regulation is done over the two stages A_3 and A_4. The common-mode level is tapped between R_{1d} and R_{2d} and is controlled by the part of the current source M_{4c} in A_3.

The overall operational amplifier is compensated with a nested Miller compensation [87]. The compensation network includes R_{C1} to R_{C4} and C_{C1} to C_{C4}. The high-gain stages are compensated by their own by R_{C5}, R_{C6}, C_{C5}, and C_{C6}.

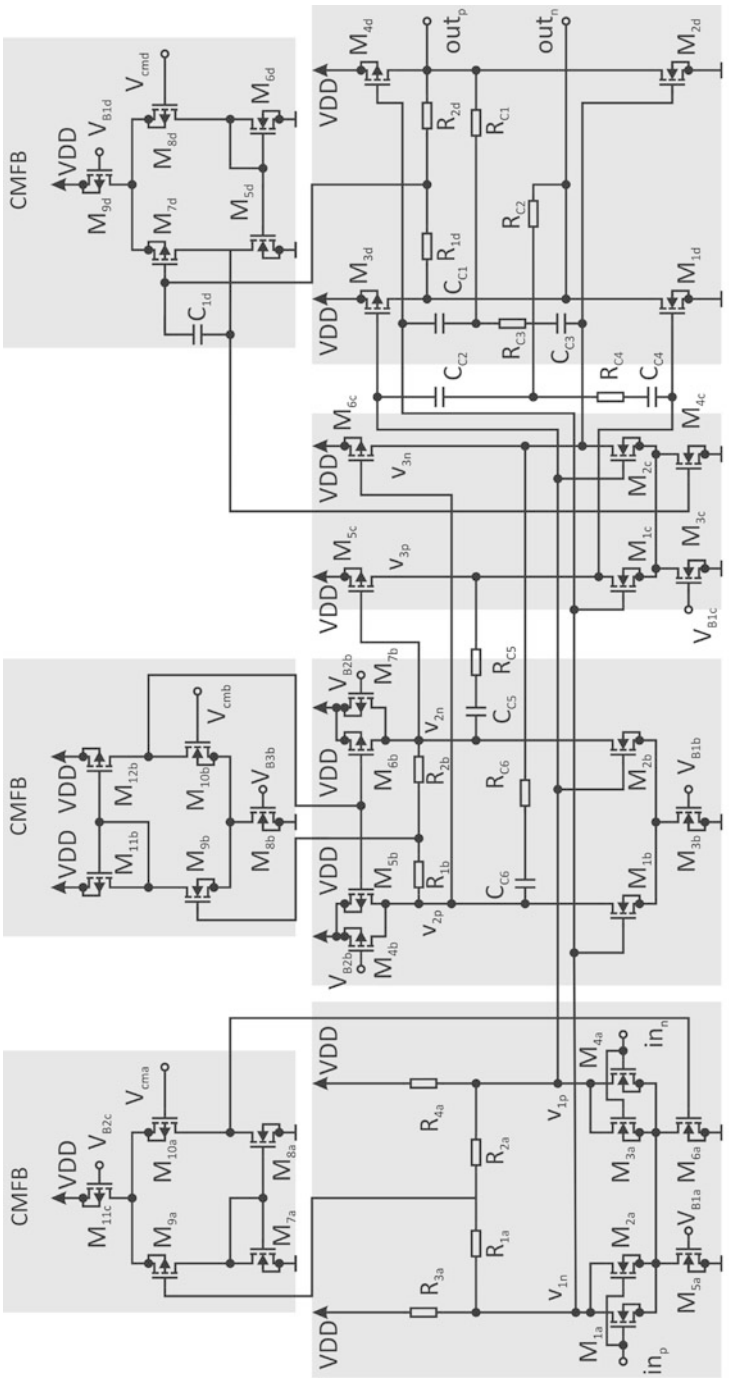


Fig. 7.12 Four-stage multiple feed-forward operational amplifier—schematic

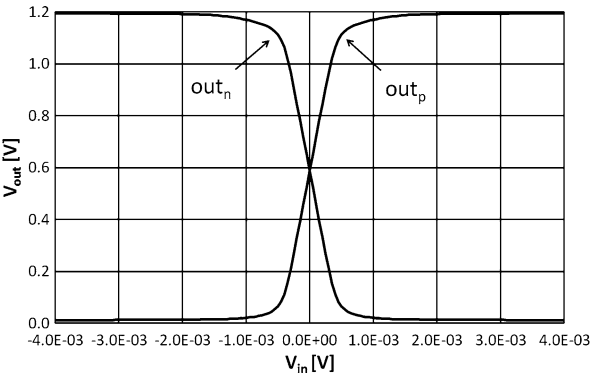


Fig. 7.13 Four-stage multiple feed-forward operational amplifier—DC characteristics

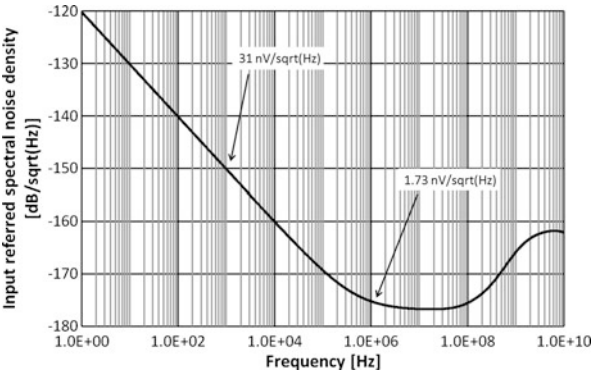


Fig. 7.14 Four-stage multiple feed-forward operational amplifier—spectral input referred noise density

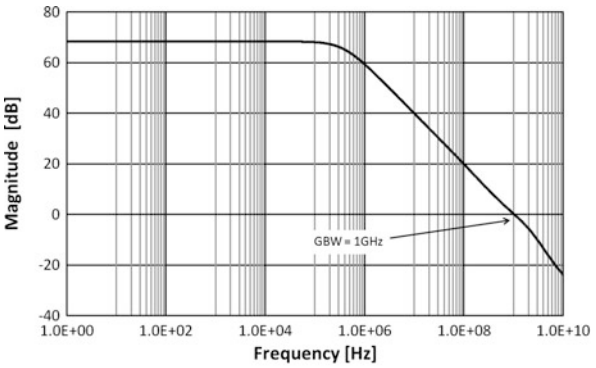
Simulation Results The operational amplifier is designed in 65 nm low-power CMOS technology and uses a supply voltage of 1.2 V. The current consumption is 9.6 mA and a capacitive load of 4 pF in parallel to 10 kΩ on each of the differential outputs is driven.

The open-loop DC characteristics are depicted in Fig. 7.13. The common-mode level at the output is 600 mV and a good linearity is achieved at an input range of ±0.5 mV.

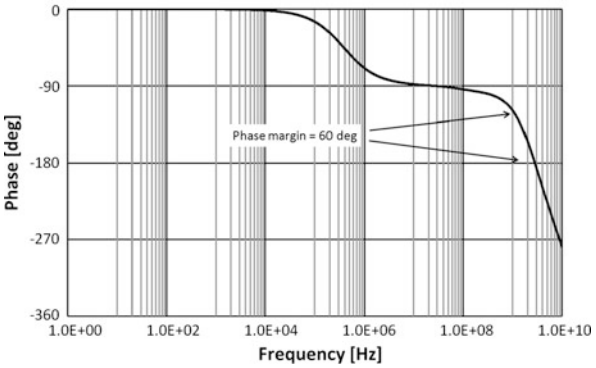
The input referred spectral noise density is shown in Fig. 7.14. At 1 kHz the input-referred spectral noise density is 31 nV/$\sqrt{\text{Hz}}$ and at 1 MHz 1.73 nV/$\sqrt{\text{Hz}}$.

The frequency response is depicted in Fig. 7.15. The amplitude response in Fig. 7.15(a) exhibits a DC gain of 68 dB and a gain bandwidth product of 1 GHz. The phase response in Fig. 7.15(b) shows a phase margin of 60°, which is equivalent to a phase lag of 120°.

The power supply rejection ratio at DC is $\text{PSRR}_{VSS} = 77.4$ dB and $\text{PSRR}_{VDD} = 77.7$ dB at VSS and VDD, respectively. The operational amplifier has a figure of merit of 833 $\frac{\text{MHz·pF}}{\text{mA}}$. A performance summary is given in Table 7.4 [127].



(a) Amplitude response



(b) Phase response

Fig. 7.15 Four-stage multiple feed-forward operational amplifier—frequency response

Table 7.4 Four-stage multiple feed-forward operational amplifier—performance summary

Technology	65 nm CMOS
Supply voltage	1.2 V
Current consumption	9.6 mA
DC gain	68 dB
GBW	1 GHz
Load	2×4 pF $\parallel$ 10 kΩ
PM	60°
FOM_{Opamp}	833 $\frac{\text{MHz·pF}}{\text{mA}}$

7.7.4 A First-Order Operational Amplifier RC Low-Pass Filter Using a Four-Stage Multiple Feed-Forward Operational Amplifier

The four-stage multiple feed-forward operational amplifier is used in an first-order opamp RC filter as depicted in Fig. 7.16. The gain and the −3 dB cut-off frequency is set like in (7.5) and (7.6). R_{1LPF} and R_{2LPF} correspond to the equivalent mixer

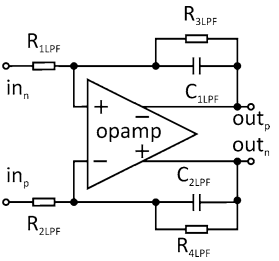


Fig. 7.16 First-order opamp RC filter using the four-stage multiple feed-forward opamp—schematics

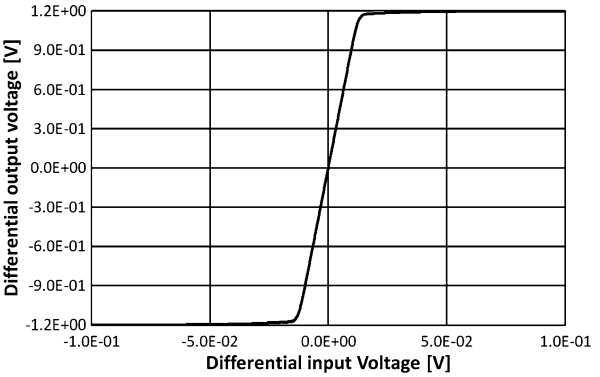


Fig. 7.17 First-order opamp RC filter using four-stage multiple feed-forward operational amplifier—differential DC characteristics

output resistances and are 100 Ω. R_{3LPF} and R_{4LPF} define the gain of the filter and are 5 kΩ. The filter capacitances C_{1LPF} and C_{2LPF} are 8 pF.

Simulation Results The filter was not fabricated because of a lack of chip area. The first-order opamp RC filter is supplied with 1.2 V and has a power consumption of 11.5 mW. The load of the filter is 4 pF in parallel to 10 kΩ. The differential DC characteristics are shown in Fig. 7.17. The common-mode level is 600 mV and the graph is linear in an input voltage range of ±11 mV.

The input referred spectral noise density is shown in Fig. 7.18. The input referred spectral noise density at 10 kHz is 10 nV/$\sqrt{\text{Hz}}$ and at 1 MHz 2.5 nV/$\sqrt{\text{Hz}}$. The average integrated noise density from 500 Hz to 4 MHz is 2.94 nV/$\sqrt{\text{Hz}}$.

The AC characteristics are shown in Fig. 7.19. The amplitude response in Fig. 7.19(a) shows a filter DC gain of 40 dB and a −3 dB cut-off frequency of 4 MHz. The phase response is depicted in Fig. 7.19(b). The distortion measurement is performed with a sinusoidal input signal of 100 kHz. The THD of −40 dB of the output signal occurs at a differential input signal amplitude of 11.48 mV_p. The in-band intermodulations are determined by using two-tones at 1 MHz and 1.2 MHz. A differential input signal amplitude of 7.2 mV_p causes IM3 of −40 dB. The filter has a DR of 62.7 dB and a FOM_{Filter} of 54744. A performance summary is given in Table 7.5.

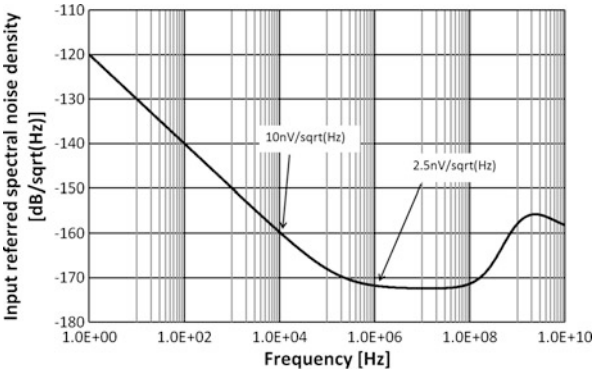
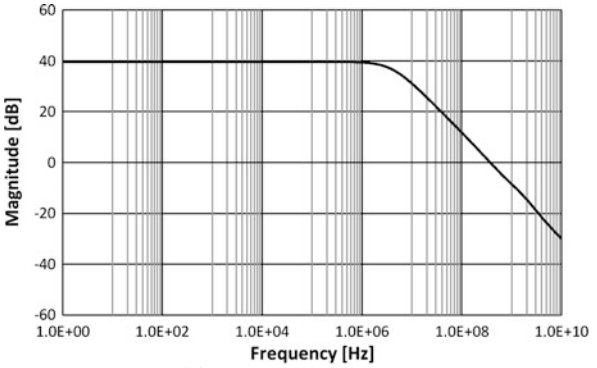
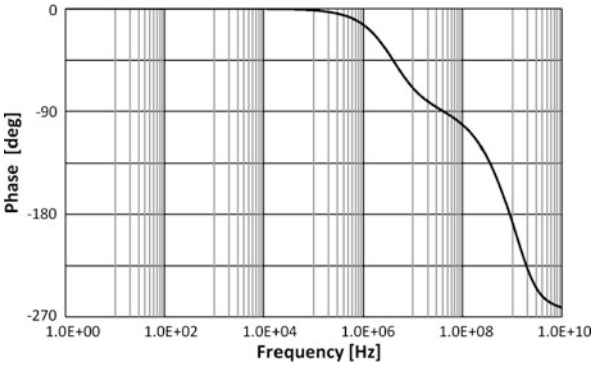


Fig. 7.18 First-order opamp RC filter using four-stage multiple feed-forward operational amplifier—spectral input referred noise density



(a) Amplitude response



(b) Phase response

Fig. 7.19 Four-stage multiple feed-forward operational amplifier—differential frequency response

7.7.5 Three-Stage High-Voltage Operational Amplifier in 65 nm CMOS at 2.5 V Supply Voltage

An operational amplifier is implemented in 65 nm CMOS technology, which is appropriate for a 2.5 V supply voltage, although the nominal supply voltage of the

Table 7.5 First-order opamp RC low-pass filter using the 4-stage multiple feed-forward opamp—performance summary

Technology	65 nm CMOS
Supply voltage	1.2 V
Power consumption	11.5 mW
DC gain	40 dB
3 dB cut-off frequency	4 MHz
Load	2×1.5 pF $\parallel$ 5 kΩ
DR	62.7 dB
FOM_{Filter}	54744

digital CMOS process is only 1.2 V. The higher supply voltage enables a higher output voltage swing and, hence, avoids clipping at large input signals. Furthermore higher drain-source voltages of the transistors can be provided due to the high supply voltage. Thus lower distortions and intermodulation products occur [44]. Applying a supply voltage outside specification is a challenging issue. Nanometer CMOS transistors with their thin gate oxide are vulnerable to high electrical fields. Hence, V_{GS} and V_{DS} must remain within the specified limits. Exceeding these limits leads to reliability problems up to immediate electrical damage. To avoid those breakdowns, additional transistors are inserted between the supply rails. They ensure a proper voltage dividing and additionally they operate as cascodes which enhance speed and gain [91, 113].

The schematic of the operational amplifier is shown in Fig. 7.20. The opamp is organized in three stages, the input stage, the high-gain stage, and the output stage. A feed-forward from the input-stage to the output stage is implemented as well. The input stage is realized with two differential pairs. The load of the NMOS differential pair is substituted by the PMOS differential pair. The NMOS current source is split into two parts, M_{1a} having a fixed bias, and M_{2a}, which is used for the common-mode feedback. The current source is cascoded with M_{3a}. M_{9a} and M_{8a} are used for proper voltage division. The common-mode regulation is realized with a cascoded PMOS differential pair. The actual value of the common-mode voltage is determined by R_{1a} and R_{2a}, and C_{1a} and C_{2a}. The set point is V_{cma}. The common-mode regulation is closed by M_{2a}.

The high-gain stage uses a PMOS differential pair (M_{3b} and M_{4b}). The current source is again split into a fixed part (M_{6b}) and a variable part (M_{7b}) for a fast common-mode regulation. The current source is cascoded by M_{5b} and the load transistors M_{1b} and M_{2b} are constantly biased.

The output stage is simultaneously the summing stage for the high-gain branch and the feed-forward branch. The feed-forward signal is amplified and added to the output signal by the transistors M_{5c} and M_{6c}. The high-gain signal is amplified and added to the output signal by M_{1c} and M_{2c}. M_{3c} and M_{4c} are cascode transistors and M_{7c} and M_{8c} are current sources. The common-mode feedback is realized with an NMOS differential pair. The regulation is closed by the current source transistor M_{7b} of the high-gain stage.

The compensation is done by nested Miller compensation [87]. The compensation network is R_{C1}, R_{C2}, and C_{C1} to C_{C4}.

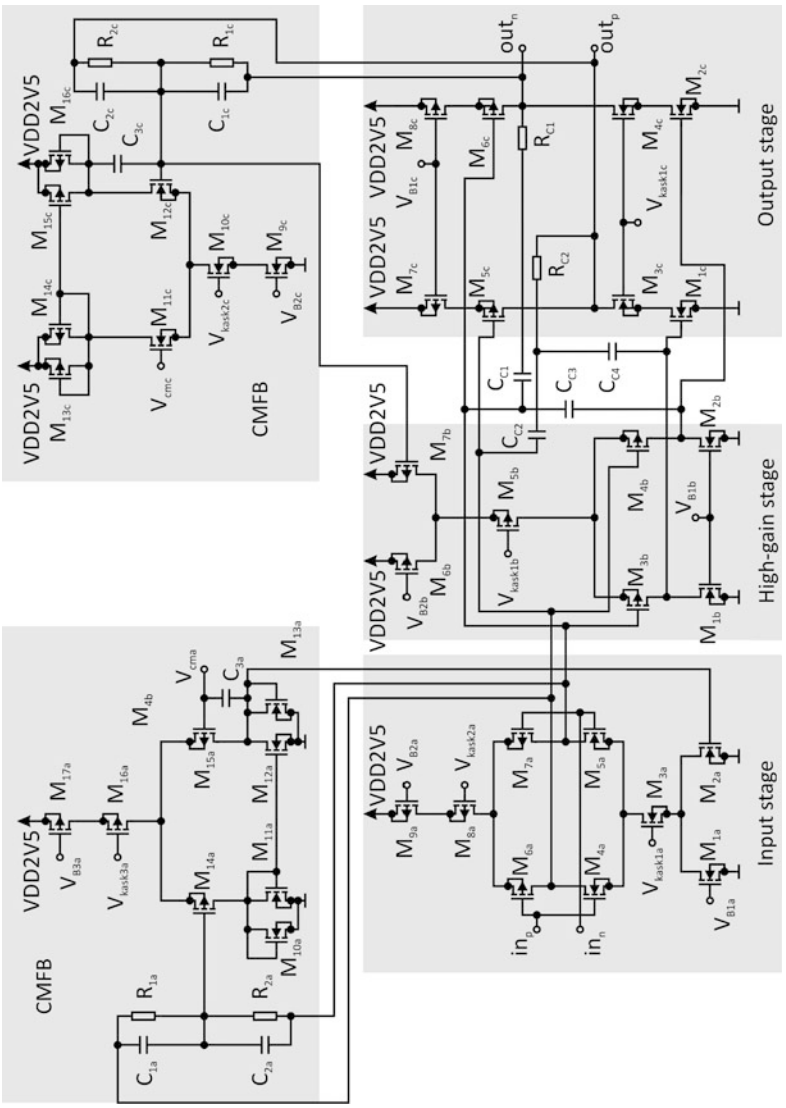


Fig. 7.20 Three-stage high-voltage operational amplifier—schematics

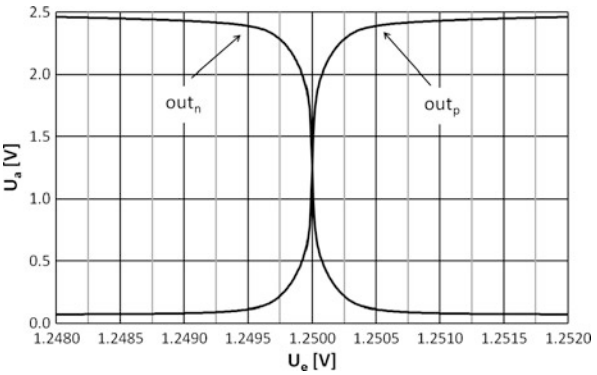


Fig. 7.21 Three-stage high-voltage operational amplifier—DC characteristics

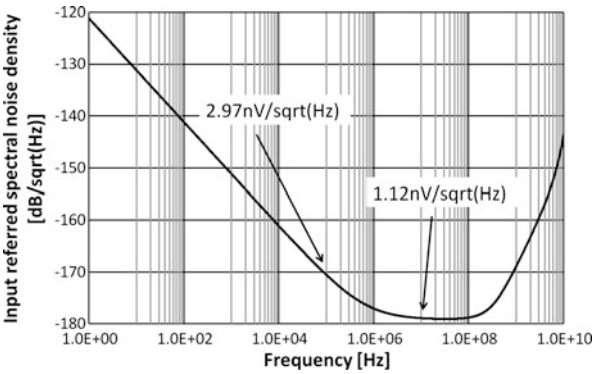
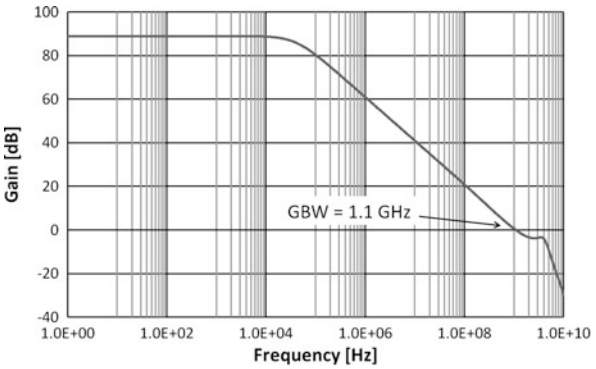


Fig. 7.22 Three-stage high-voltage operational amplifier—input referred spectral noise density

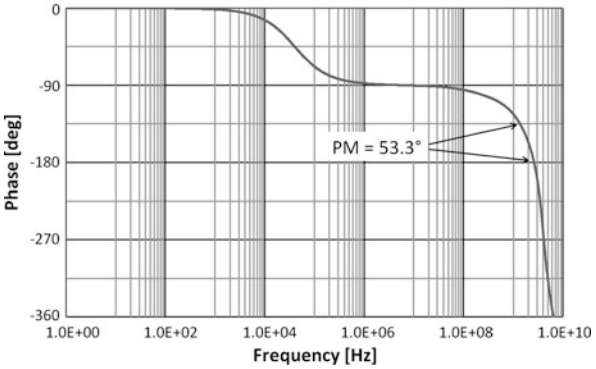
Simulation Results The operational amplifier has a supply voltage of 2.5 V and a current consumption of 5.85 mA. The opamp drives a load of 1 pF at each output pin. The DC characteristics are depicted in Fig. 7.21. The output range is between 0.1 V and 2.4 V. The common-mode output voltage is 1.25 V.

The input referred spectral noise density is depicted in Fig. 7.22. At 100 kHz the input referred noise density is 1.97 nV/$\sqrt{\text{Hz}}$ and at 10 MHz 2.12 nV/$\sqrt{\text{Hz}}$. The average input referred integrated noise density is 1.71 nV/$\sqrt{\text{Hz}}$ between the integration limits of 500 Hz and 4 MHz.

The AC characteristics are given in Fig. 7.23. The amplitude response in Fig. 7.23(a) shows a DC gain of 89 dB and a gain-bandwidth product of 1.1 GHz. The phase response in Fig. 7.23(b) has a PM of 53.3°. The PSRR_{VSS} is 107 dB and PSRR_{VDD} is 108 dB. The operational amplifier has a FOM_{Opamp} of 376 $\frac{\text{MHz·pF}}{\text{mA}}$. The performance summary is given in Table 7.6.



(a) Amplitude response



(b) Phase response

Fig. 7.23 Three-stage high-voltage operational amplifier—frequency response

Table 7.6 Three-stage high-voltage operational amplifier—performance summary

Technology	65 nm CMOS
Supply voltage	2.5 V
Current consumption	5.85 mA
DC gain	89 dB
GBW	1.1 GHz
Load	2×1 pF
PM	53.3°
FOM_{Opamp}	376 $\frac{\text{MHz·pF}}{\text{mA}}$

7.7.6 Mixer and Filter Combination Using a Three-Stage High-Voltage Operational Amplifier

The high-voltage operational amplifier is inserted in a mixer-filter combination of a direct conversion receiver architecture [130]. The mixer and the filter is depicted in Fig. 7.24. The mixer is a four transistor switching network including a g_m-cell for signal amplification, working in the 2.5 V domain as well. The passive mixer is used because of the lower 1/f noise especially in narrow band channels. Passive

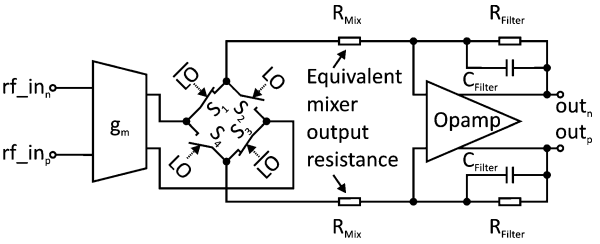


Fig. 7.24 Mixer filter combination

mixers have no inherent 1/f noise [46] and additional bias networks are not necessary. A better power efficiency can be achieved. The g_m-cell and the passive mixer was provided by Infineon. The mixer operation principle is described in [88]. The mixer-filter operates in the UHF (ultra high frequency) band in the frequency range from 470 MHz to 862 MHz, which is divided in 48 channels.

Simulation Results The first-order low-pass filter is realized by using the equivalent output resistance R_{Mix} of the passive mixer. The filter transfer function is

$$H_{Filter} = \frac{R_{Filter}}{R_{Mix}} \frac{1}{1 + s R_{Filter} C_{Filter}} \tag{7.7}$$

C_{Filter} denotes the filter capacitance and is 23 pF. R_{Filter} is the filter resistor with a value of 2 kΩ. The mixer output resistance is 100 Ω. C_{Filter} and R_{Filter} are set for a mixer-filter gain of 24 dB and a −3 dB cut-off frequency of 4 MHz. The clock frequency f_{LO} is set to 666 MHz. 666 MHz is the carrier frequency of the 45th DVB-T channel which is in the middle of the UHF band. The average integrated input referred noise density, integrated from 500 Hz to 4 MHz, results in 2.96 nV/$\sqrt{\text{Hz}}$. The noise figure NF is 16.1 dB. The mixer-filter combination consumes 12.7 mA at a supply voltage of 2.5 V.

The out-of-band IIP3 is determined by applying two sinusoidal signals of 658 MHz and 663 MHz, hence the IM3 is at 2 MHz in the pass-band. The 1 dB compression point is determined by a input signal of 668 MHz, 2 MHz in the pass-band as well and results in 0 dBm. The 3rd-order input intercept point of +10 dBm is achieved. A performance summary of the mixer-filter combination is given in Table 7.7 [130].

Comparison of the Mixer-Filter Combination The comparison to similar mixer filter combinations is difficult, because only complete analog front-ends are mostly published. A mixer-filter architecture in 0.13 µm CMOS for a ultra-wide band receiver is presented in [74]. The front-end has an in-phase and a quadrature-phase branch, which consists of one g_m-cell, two mixers, and two transimpedance amplifiers. The −3 dB cut-off frequency is 250 MHz at a clock frequency range from 3.1 to 4.7 GHz. The minimum noise figure is 3.3 dB and the IIP3 is −14 dBm. A direct comparison is difficult, due to different specifications in bandwidth and rf frequency range.

Table 7.7 Performance summary

Technology	65 nm CMOS
Supply voltage	2.5 V
Frequency	666 MHz
Bandwidth (base-band)	4 MHz
Gain	24 dB
NF	16.1 dB
Average integrated noise density	2.96 nV/$\sqrt{\text{Hz}}$
IIP3	+10 dBm
Current consumption	12.7 mA

7.8 Comparison to State-of-the-Art of Operational Amplifiers

A comparison to the state-of-the-art of operational amplifiers is given in Table 7.8. The publications are sorted chronologically. It needs to be kept in mind, that regarding (7.4) higher values of FOM_{Opamp} are better.

The operational amplifier in [133] is simulated in 0.8 µm CMOS and has a gain of 106 dB. A good FOM_{Opamp} of 1111 $\frac{\text{MHz·pF}}{\text{mA}}$ is reached due to the ultra low-power design (6.75 µW). The opamp has only a moderate GBW of 1 MHz at a PM of 47° and 5 pF load capacitance. An operational amplifier in 0.13 µm CMOS with 50 dB gain and 3.2 MHz GBW is realized in [78]. Simulation results without any C_L are given, hence no FOM_{Opamp} is available. A high-speed opamp (0.18 µm CMOS) with a GBW of 2.6 GHz is presented in [42]. Only a moderate FOM_{Opamp} of 367 $\frac{\text{MHz·pF}}{\text{mA}}$ is achieved due to the small load capacitance and 4 mA current consumption at 1.8 V supply.

The opamp in [107] can drive a large C_L of 10 pF at 1.2 V supply voltage and 1.8 mA power consumption. The GBW of 46 MHz (PM = 66°) allows only a moderate FOM_{Opamp} of 256 $\frac{\text{MHz·pF}}{\text{mA}}$. A medium-speed opamp in 0.18 µm CMOS is realized in [109]. Despite the use of cascodes a power of 12 mW is needed to drive a 2 pF load (post layout simulations). The PM (73°) is high, however only a moderate FOM_{Opamp} (118 $\frac{\text{MHz·pF}}{\text{mA}}$) is achieved. A high-speed opamp with a GBW of 1.5 GHz is published in [106] in 120 nm CMOS technology. The gain is only 40 dB but the FOM_{Opamp} of 1048 $\frac{\text{MHz·pF}}{\text{mA}}$ is good, 9.16 mA at 1.2 V supply is needed to drive a load of 3.2 pF twice. The high-gain opamp (120 dB) in 120 nm CMOS technology, presented in [108], consumes much power (27.5 mW). The GBW is high (886 MHz) at a load of 3.5 pF twice and a PM of 36° but the FOM_{Opamp} of 265 $\frac{\text{MHz·pF}}{\text{mA}}$ is only moderate.

A 0.35 µm CMOS technology is used in [15]. Cascoding, which is only possible with sufficient supply voltage allows a low power consumption and a huge load capacitance of 100 pF. A current consumption of 0.666 mA at 3.3 V supply voltage and a low GBW of 7.8 MHz (PM = 67°) results in a good FOM_{Opamp} (1171 $\frac{\text{MHz·pF}}{\text{mA}}$). An excellent FOM_{Opamp} of 1492 $\frac{\text{MHz·pF}}{\text{mA}}$ is achieved in [73], although the GBW (280.5 MHz) is only mid-range (PM = 48°). The current consumption is low (0.94 mA) due to a folded cascode structure at 2.5 V supply voltage

Table 7.8 Comparison to the state-of-the-art of operational amplifiers

Citation	CMOS technology	Supply voltage	Power consumption	Gain	GBW	PM	Load	FOM_{Opamp}
State-of-the-art								
[133]	0.8 µm	1.5 V	6.75 µW	106 dB	1 MHz	47°	5 pF	1111 $\frac{\text{MHz·pF}}{\text{mA}}$
[78]	0.13 µm	1.5 V	4.65 mW	50 dB	3.2 MHz	44°	n.a.†	n.a.†
[42]	0.18 µm	1.8 V	7.2 mW	50 dB	2.6 GHz	35°	2×0.3 pF ‖ 1 kΩ	367 $\frac{\text{MHz·pF}}{\text{mA}}$
[107]	0.12 µm	1.2 V	2.16 mW	86 dB	46 MHz	66°	10 pF ‖ 750 kΩ	256 $\frac{\text{MHz·pF}}{\text{mA}}$
[109]	0.18 µm	1.8 V	12 mW	86 dB	392 MHz	73°	2 pF	118 $\frac{\text{MHz·pF}}{\text{mA}}$
[106]	0.12 µm	1.2 V	10.99 mW	40.4 dB	1.5 GHz	45°	2×3.2 pF	1048 $\frac{\text{MHz·pF}}{\text{mA}}$
[108]	0.12 µm	1.2 V	27.5 mW	120 dB	866 MHz	36°	2×3.5 pF	265 $\frac{\text{MHz·pF}}{\text{mA}}$
[15]	0.35 µm	3.3 V	2.2 mW	60 dB	7.8 MHz	67°	100 pF	1171 $\frac{\text{MHz·pF}}{\text{mA}}$
[73]	0.25 µm	2.5 V	2.35 mW	76 dB	280.5 MHz	48°	5 pF	1492 $\frac{\text{MHz·pF}}{\text{mA}}$
[45]	0.18 µm	1.8 V	19.4 mW	66 dB	2.4 GHz	n.a.†	8.6 pF	560 $\frac{\text{MHz·pF}}{\text{mA}}$
[45]	0.18 µm	1.8 V	72 mW	27.1 dB	4.8 GHz	n.a.†	2×7.4 pF	1776 $\frac{\text{MHz·pF}}{\text{mA}}$
[45]	0.18 µm	1.8 V	81 mW	111 dB	1.27 GHz	n.a.†	n.a.†	n.a.†
[2]	0.18 µm	1 V	550 µW	50.1 dB	26.2 MHz	n.a.†	5 pF ‖ 10 kΩ	238 $\frac{\text{MHz·pF}}{\text{mA}}$
[2]	0.18 µm	1 V	40 µW	53 dB	1.3 MHz	n.a.†	5 pF ‖ 10 kΩ	162 $\frac{\text{MHz·pF}}{\text{mA}}$
[55]	0.13 µm	1.5 V	1.8 mW	63.16 dB	10 MHz	n.a.†	n.a.†	n.a.†
[140]	0.12 µm	1.5 V	1.8 mW	73 dB	4.4 MHz	70°	5 pF	18.3 $\frac{\text{MHz·pF}}{\text{mA}}$
[10]	0.35 µm	1 V	385 µW	76.2 dB	8.1 MHz	>60°	17 pF ‖ 1 MΩ	385 $\frac{\text{MHz·pF}}{\text{mA}}$
[75]	0.35 µm	3 V	48.6 mW	93 dB	135 MHz	61°	7 pF	58 $\frac{\text{MHz·pF}}{\text{mA}}$
[141]	0.12 µm	1.5 V	17.5 mW	76.3 dB	135 MHz	51°	15 pF	176 $\frac{\text{MHz·pF}}{\text{mA}}$

Table 7.8 (Continued)

Citation	CMOS technology	Supply voltage	Power consumption	Gain	GBW	PM	Load	FOM_{Opamp}
[27]	0.35 µm	3.3 V	15.84 mW	86.4 dB	570 MHz	85.6°	1.4 pF	166 $\frac{\text{MHz·pF}}{\text{mA}}$
[27]	0.35 µm	3.3 V	15.84 mW	85.9 dB	350 MHz	56°	1.4 pF	102 $\frac{\text{MHz·pF}}{\text{mA}}$
[143]	0.12 µm	1 V	1.4 mW	108 dB	40.2 MHz	62°	500 pF	14357 $\frac{\text{MHz·pF}}{\text{mA}}$
[142]	65 nm	1 V	0.72 mW	100 dB	40 MHz	64°	15 pF	833 $\frac{\text{MHz·pF}}{\text{mA}}$
[139]	0.6 µm	3 V	n.a.†	113.57 dB	11.9 MHz	56°	n.a.†	n.a.†
[23]	90 nm	n.a.†	n.a.†	52.37 dB	1.014 GHz	47.4°	n.a.†	n.a.†
[23]	90 nm	n.a.†	n.a.†	65.66 dB	539.4 MHz	7.7°	n.a.†	n.a.†
[34]	0.18 µm	1.8 V	25 mW	65 dB	2.3 GHz	58°	2 pF	331 $\frac{\text{MHz·pF}}{\text{mA}}$
[110]	0.18 µm	0.7 V	107 µW	72.8 dB	0.97 MHz	70°	n.a.†	n.a.†
Own publications								
[129]	65 nm	1.2 V	11.4 mW	58 dB	1 GHz	62°	2×5 pF $\parallel$ 10 kΩ	1052 $\frac{\text{MHz·pF}}{\text{mA}}$
[127]	65 nm	1.2 V	11.52 mW	68 dB	1 GHz	60°	2×4 pF $\parallel$ 10 kΩ	833 $\frac{\text{MHz·pF}}{\text{mA}}$
[130]	65 nm	2.5 V	14.63 mW	89 dB	1.1 GHz	53.3°	2×1 pF	376 $\frac{\text{MHz·pF}}{\text{mA}}$

† . . . not available

($C_L = 5$ pF). Three operational amplifiers in 0.18 CMOS technology (supply voltage 1.8 V) are compared in [45]. The first one has a GBW of 2.4 GHz ($C_L = 8.6$ pF), a gain of 66 dB, a current consumption of 35 mA, and a medium FOM_{Opamp} of 560 $\frac{\text{MHz·pF}}{\text{mA}}$. The second opamp has a GBW of 4.8 GHz ($C_L = 2 \times 7.4$ pF), a DC gain of only 27.1 dB, and needs 40 mA. Despite of the enormous power consumption a good FOM_{Opamp} (1776 $\frac{\text{MHz·pF}}{\text{mA}}$) is reached. The remaining high-gain opamp with 111 dB DC gain and a current consumption of 45 mA (GBW = 1.27 GHz) has no given load capacitance, hence no FOM_{Opamp} is available. Two ultra low-power opamps at only 1 V supply voltage (0.18 µm CMOS) are presented in [2]. Both reach only moderate FOM_{Opamp} of 238 $\frac{\text{MHz·pF}}{\text{mA}}$ ($C_L = 5$ pF, GBW = 26.2 MHz, 0.55 mA current consumption) and 162 $\frac{\text{MHz·pF}}{\text{mA}}$ ($C_L = 5$ pF, GBW = 1.3 MHz, 0.04 mA current consumption). No C_L is given in the low-power opamp design (1.8 mW, 0.13 µm CMOS, GBW = 10 MHz) in [55], hence no FOM_{Opamp} is calculable. A three-stage operational amplifier in 120 nm CMOS is proposed in [140] with 73 dB DC gain, 4.4 MHz GBW, and 1.2 mA current consumption at 1.5 V. A C_L of 5 pF leads to a poor FOM_{Opamp} of 18.3 $\frac{\text{MHz·pF}}{\text{mA}}$. A low-power 0.35 µm CMOS opamp at only 1 V supply voltage is presented in [10]. A GBW of 8.1 MHz and a power dissipation of 385 µW together with the load capacitance of 17 pF results in a medium FOM_{Opamp} of 385 $\frac{\text{MHz·pF}}{\text{mA}}$. An opamp in 0.35 µm CMOS technology at 3 V is presented in [75]. Despite of the cascoded circuitry the power consumption is high (48 mW), the GBW is 135 MHz, and the FOM_{Opamp} of 58 $\frac{\text{MHz·pF}}{\text{mA}}$ is poor.

A 135 MHz GBW opamp at C_L of 15 pF in 0.12 µm CMOS is introduced in [141]. A DC gain of 76.3 dB, a current consumption of 11.5 mA at 1.5 V supply lead to a medium FOM_{Opamp} of 176 $\frac{\text{MHz·pF}}{\text{mA}}$. Two opamps in 0.35 µm CMOS with a high GBW (570 MHz and 350 MHz) are published in [27]. The high power consumption (both: 15.84 mW) and the low load capacitance (both: 1.4 pF) disallow a good FOM_{Opamp} (166 $\frac{\text{MHz·pF}}{\text{mA}}$ and 102 $\frac{\text{MHz·pF}}{\text{mA}}$). A low voltage (1 V) operational amplifier in 0.12 µm CMOS with a power dissipation of 1.4 mW is presented in [143]. A GBW of 40.2 MHz (PM = 62°), a C_L of 500 pF, and a DC gain of 108 dB allow an excellent FOM_{Opamp} of 14357 $\frac{\text{MHz·pF}}{\text{mA}}$. An operational amplifier in 65 nm CMOS is presented in [142] with an open-loop gain of 100 dB, a GBW of 40 MHz (PM = 64°) and a load of 15 pF. A power consumption of 0.72 mW at 1 V supply voltage results in a good FOM_{Opamp} of 833 $\frac{\text{MHz·pF}}{\text{mA}}$. A high-gain opamp is introduced in [139] in 0.6 µm technology. A GBW of 11.9 MHz and a PM of 53° are achieved. No C_L and no power consumption are reported. Two operational amplifiers in 90 nm CMOS with a high GBW (1.014 GHz and 539.4 MHz) are realized in [23]. The PM (7.7°) of the second opamp is extremely small. No further information is provided. A high GBW operational amplifier (2.3 GHz) in 0.18 µm CMOS is introduced in [34] and reaches a moderate FOM_{Opamp} of 331 $\frac{\text{MHz·pF}}{\text{mA}}$ due to the small load capacitance (2 pF) and the high power consumption (13.9 mA at 1.8 V supply voltage). A low-power (107 µW) and low supply voltage (0.7 V) opamp with a GBW of 0.97 MHz is presented in [110], but [110] does not provide the C_L for a FOM_{Opamp} calculation. Unfortunately only a few operational amplifier designs in nanometer CMOS technology were available at this time.

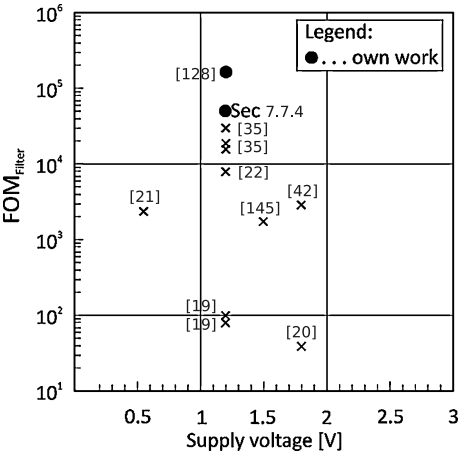


Fig. 7.25 Comparison to the state-of-the-art—voltage–mode filters

The operational amplifiers presented in the work at hand [127, 129, 130] are implemented in 65 nm CMOS technology. A low supply voltage (1.2 V) and high threshold voltages of the transistors disallow the application of cascodes. There is the tendency of high power consumption at high operational amplifier gain and high GBW at the same time. A high GBW of 1 GHz and a high load capacitance enable a good FOM_{Opamp} (1052 $\frac{\text{MHz·pF}}{\text{mA}}$ and 833 $\frac{\text{MHz·pF}}{\text{mA}}$). The opamp at 2.5 V is optimized for a large output signal swing and uses extensive cascoding. A high gain of 89 dB is realized. The output stage of the opamp is optimized for an on-chip design, hence only small load capacitances are taken into account. A small C_L and the high power consumption result in a moderate FOM_{Opamp} of 367 $\frac{\text{MHz·pF}}{\text{mA}}$.

7.9 Comparison to State-of-the-Art of Voltage-Mode Filters

A comparison to the state-of-the-art of voltage-mode filters is given in Table 7.9. The publications are sorted chronologically. It needs to keep in mind, that regarding (6.12) lower values of FOM_{Filter} are better. A plot of the FOM_{Filter}s against the supply voltage is depicted in Fig. 7.25.

The presented opamp in [42] is used in a 40 MHz to 350 MHz opamp RC filter. The 5th-order elliptic low-pass filter has a power dissipation of 25.2 mW at 1.8 V supply voltage. At the −3 dB cut-off frequency of 350 MHz the DR is moderate (52 dB) and the FOM_{Filter} is medium (2742). A low-power Butterworth filter at 1.5 V in 0.18 µm TSMC CMOS is introduced in [145]. The −3 dB cut-off frequency is tunable from 13 to 80 kHz. At 50 kHz a good DR of 75 dB is reached, but the low −3 dB cut-off frequency results in a medium FOM_{Filter} of 1527. A 90 nm CMOS elliptic low-pass filter design is published in [30], which has a cut-off frequency of 1, 10, and 100 MHz. The gain is variable from 13.5 to 67.5 dB. No distortion and noise performance are reported, hence no DR and FOM_{Filter} is available. A filter for UMTS and WLAN with −3 dB cut-off frequencies of 2.11 MHz and 11 MHz is

Table 7.9 Comparison to the state-of-the-art of voltage-mode filters

Citation	CMOS technology	Supply voltage	Power consumption	Gain	Filter order	−3 dB cut-off frequency	Active area	DR	FOM_{Filter}
State-of-the-art									
[42]‡	0.18 µm	1.8 V	25.2 mW	0 dB	5	40–350 MHz	0.5 mm^2	52 dB	2742
[145]‡	0.18 µm	1.5 V	240 µW	n.a.†	3	13–80 kHz	0.113 mm^2	75 dB	1527
[30]	90 nm	1.4 V	13.5 mW	13.5–67.5 dB	6	1–100 MHz	0.55 mm^2	n.a.†	n.a.†
[19]‡	0.13 µm	1.2 V	3.4 mW	4 dB	4	2.11 MHz	0.9 mm^2	81 dB	97
[19]‡	0.13 µm	1.2 V	14.2 mW	4 dB	4	11 MHz	0.9 mm^2	81 dB	77
[35]‡	0.13 µm	1.2 V	5.6 mW	8 dB	4	11 MHz	0.7 mm^2	55 dB	12146
[35]‡	0.13 µm	1.2 V	3 mW	8 dB	4	2.5 MHz	0.8 mm^2	58 dB	14349
[35]‡	0.13 µm	1.2 V	3 mW	8 dB	4	1 MHz	0.7 mm^2	58 dB	34258
[20]‡	0.18 µm	1.8 V	4.1 mW	−3.5 dB	4	10 MHz	0.26 mm^2	79 dB	39
[21]‡	0.13 µm	0.55 V	3.4 mW	0 dB	4	11.3 MHz	0.45 mm^2	60 dB	2270
[22]‡	65 nm	1.2 V	1.3 mW	32 dB	4	7.8 MHz	n.a.†	52 dB	7934
[76]	0.18 µm	1.2 V	4.1–11.1 mW	0 dB	3	0.5–20 MHz	0.23 mm^2	n.a.†	n.a.†
[32]‡	0.18 µm	1.8 V	384.44 µW	38 dB	2	24 MHz	n.a.†	n.a.†	n.a.†
Own publications									
[128]‡	65 nm	1.2 V	10 mW	38 dB	1	3.5–4.5 MHz	0.104 mm^2	57 dB	143945
Sect. 7.7.4‡	65 nm	1.2 V	11.5 mW	40 dB	1	4 MHz	n.a.†	62 dB	54744

†... not available

‡... plotted in Fig. 7.25

realized in [19]. Both filters in 0.13 µm CMOS at 1.2 V have a good DR of 81 dB and a good FOM_{Filter} of 97 and 77, respectively. Three filters for the application in WLAN, UMTS, and Bluetooth in 0.13 µm CMOS are presented in [35]. Hence the −3 dB cut-off frequencies are 11 MHz, 2.5 MHz, and 1 MHz, respectively. The filters at 1.2 V supply voltage achieve a medium DR from 55 dB to 58.2 dB. The FOM_{Filter}s are moderate from 12146 to 34258. The given active area is big, but includes the area for the DAC. A 4th-order Bessel filter is realized in [20]. In 0.18 µm CMOS at 1.8 V the filter consumes 2.28 mA and has a bandwidth of 10 MHz. A very good DR of 79 dB and a very good FOM_{Filter} of only 39 is achieved. A low-voltage active g_m-RC Butterworth filter in 0.13 µm CMOS is realized in [21]. At a supply voltage of 550 mV and a −3 dB cut-off frequency of 11.3 MHz a medium DR of 60 dB and a medium FOM_{Filter} of 2270 are achieved. A cascade of two opamp RC cells in 65 nm CMOS forms a 4th-order wideband filter in [22]. The filter has a gain of 32 dB, a moderate DR of 52 dB, and a moderate FOM_{Filter} of 7934 at a −3 dB cut-off frequency of 7.8 MHz. The multiple standard 3rd-order Butterworth filter in [76] has a tuning range from 500 kHz to 20 MHz. The power consumption depends on the filter bandwidth and the supply voltage is only 1.2 V in 0.18 µm CMOS technology. The distortions are missing in [76], hence no DR and FOM_{Filter} are available. A 2nd-order Butterworth filter with low power consumption of only 384.44 µW is introduced in [32]. The filter gain is 38 dB and the −3 dB cut-off frequency is 24 MHz. The noise as well as the distortions are not reported. DR and FOM_{Filter} cannot be determined.

The 65 nm CMOS filters designed in this work ([128] and Sect. 7.7.4) have only a moderate FOM_{Filter} despite of the medium DR of 57.2 dB and 62 dB. A main reason is the system inherent filter-order and the filter gain in combination with distortions. The receiver front-end is designed to have a passive mixer and a following 1st-order Butterworth operational amplifier RC low-pass filter. The opamp RC filter does the output signal conversion from the passive mixer, the first signal amplification, and the bandwidth selection of the DVB-H channel. A 1st-order Butterworth low-pass filter is used instead of a higher-order filter in order to save power dissipation in the overall direct conversion receiver. The high filter gain in conjunction with the filter order is reason why the filter design comes off badly. The target −3 dB cut-off frequency of the filter is 4 MHz and the gain is 38 dB or 40 dB. Any modulation products appear in the 4 MHz channel bandwidth and disturb the desired in-band signal. Low distortions and intermodulations are achievable by a large GBW and a sufficient gain of the opamp. These constraints lead to a complex and power consuming opamp that deteriorates the FOM_{Filter} of the 1st-order Butterworth operational amplifier RC low-pass filter.

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