

Raghu Murali *Editor*

Graphene Nanoelectronics

From Materials to Circuits

 Springer

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Foreword by Jeff Welser

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ISBN 978-1-4614-0547-4 e-ISBN 978-1-4614-0548-1

DOI 10.1007/978-1-4614-0548-1

Springer New York Dordrecht Heidelberg London

Library of Congress Control Number: 2011946064

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Foreword

For almost a half century, the semiconductor industry has managed to double the number of transistors on an integrated circuit chip every 18–24 months with such consistency that it has been dubbed Moore’s Law, after Gordon Moore who first noted the trend in 1965. [1] For the past 30 years, the primary technology for the industry has been the silicon complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET), and it has been the ability to shrink this device according to Robert Dennard’s scaling theory [2] that has largely enabled Moore’s Law to continue for so long. The result has been exponentially increasing performance per dollar in both integrated circuits (ICs) and all of the electronic and information technology (IT) systems they enable. Not only has scaling resulted in growing worldwide semiconductor industry revenues from \$20B in 1980 to almost \$300B in 2010, but it has also played a major role in driving the overall economy: in the United States, it has been estimated that from 1995 to 2005, while IT industries only made up 3% of Gross Domestic Product (GDP), they accounted for 25% of overall economic growth. Taken as a whole, “these industries contribute more to economy-wide productivity growth than all other industries combined.” [3]

However in the early 2000s, as the gate length for the Si FET crossed into the sub-100 nm range and the traditional gate insulator approached 10 nm thicknesses, the industry’s ability to continue to follow Dennard’s rules for decreasing dimensions and supply voltage faltered. Subsequent technology generations have seen exponentially increasing active switching and passive leakage powers, limiting the ability to take full advantage from scaling devices and doubling transistor counts. The result has been an increased focus on new materials and/or devices that could continue the historical scaling trends.

Since its re-discovery through the ingenious use of scotch tape by Novoselov, Geim and co-workers [4] in 2004, graphene has emerged as an exciting new material, with potential to impact many areas of technology. The number of publications on graphene has exploded over the past 5 years, with new theoretical claims and experimental breakthroughs seeming to happen almost monthly. However, it is a long journey from those eureka moments to finding real

applications for graphene in new devices and technology. This book attempts to take a comprehensive look at graphene in the context of nanoelectronic applications, with an eye towards highlighting the key physics, material properties, and fabrication challenges that would most interest a researcher looking to apply it to new transistors and IC technologies. It is hoped this overview will be useful for both introducing the field to new investigators, as well as offering an organized reference to those already immersed in the field.

To set the stage for understanding the challenges ahead for any new nanoelectronics technology, it is useful to step back and consider critically the status of the current technology. In the first chapter, “CMOS Performance Scaling,” the physics of scaling a Si FET down to its current gate length of just tens of nanometers and beyond are examined, highlighting the challenges of maintaining performance while managing both active and passive power. The prospect of continuing to add new innovations, such as strain and new materials for both the gate and channel regions of the device, are also discussed to understand the potential paths for extending FET scaling to its limits.

In the next two chapters, the prospects for graphene in helping to address some of these challenges in future FETs are considered. “Electronic Transport in Graphene” gives a thorough overview of the basic graphene material properties and physics, with a specific eye on how these properties can be exploited for electronic transport devices. Building on this base, “Graphene Transistors” considers how to apply the material specifically to transistors, both for digital and analog applications. This chapter thoroughly covers all of the considerations that go into making a good transistor, and while the high carrier velocity in graphene makes it attractive for many applications, the lack of a natural bandgap in the unpatterned material adds new challenges, particularly for digital switches.

Going beyond simply improving existing device structures, the “Alternative State Variables for Graphene Transistors” chapter considers entirely new ways of exploiting graphene’s unique physics. Rather than simply building transistors that modulate current flow to manipulate data, this chapter looks at the possibility of representing information with other state variables, such as spin, pseudospin, or even mechanical motion. In each case, graphene offers new ways to manipulate these novel states that may open the door to a whole new class of devices. However, to build these devices into circuits may require an even bigger change in the “wiring” between them. “Transport of Novel State Variables” considers the physics of moving various state variables—from electronic charge to carrier spin to plasmons—between devices in graphene, and compares the potential performance and energy dissipation of these interconnects with state-of-the-art CMOS. Indeed, transport may end up being the critical factor in choosing future state variables and devices.

While graphene offers many exciting new technology opportunities, they all depend on the ability not only to successfully produce high-quality graphene films, with single or few atomic layer thicknesses, but also to pattern these films and integrate them with other materials to create full device structures. The last portion of this book considers several aspects of these challenges, starting with three

chapters on graphene film growth: “Formation of Epitaxial Graphene,” “Graphene Growth by CVD Methods,” and “Chemical Approaches to Produce Graphene Oxide and Related Materials.” While all of these approaches offer significant advantage over the initial “scotch tape method” of graphene film formation, all face clear challenges in producing uniform, low-defect layers, particularly over the large areas necessary for making a manufacturable technology. Finally, given the importance of gate structures in almost all devices, the last chapter “Atomic Layer Deposition of Dielectrics on Graphene” looks at methods for depositing insulators with high-quality interfaces on the thin graphene films.

The early days of research into any new material are often filled with a mix of hype and pessimism: while some are quick to exclaim the revolutionary potential for creating whole new technology paradigms, others are equally eager to point out the impossibility of ever supplanting the existing infrastructure. Hopefully this book can contribute by offering a balanced view of both the opportunities and challenges presented by graphene, and encourage continued, methodical work on how best to utilize this exciting material in future nanoelectronic systems.

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References

1. G. E. Moore, “Cramming more components onto integrated circuits,” *Electronics*, vol. 38, no. 8, pp. 114–117, 1965.
2. R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design for ion-implanted MOSFET’s with very small physical dimensions,” *IEEE J. Solid-State Circuits*, vol. SC-9, no. 5, pp. 256–268, Oct. 1974.
3. D. Jorgenson, “Moore’s law and the emergence of the new economy,” Semiconductor Industry Association, Washington, DC, 2005 Annual Report, 2005.
4. K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva, and A.A. Firsov, “Electric field effect in atomically thin carbon films,” *Science*, vol. 306, pp. 666–669, 2004.

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Chapter 1

CMOS Performance Scaling

Ali Khakifirooz and Dimitri A. Antoniadis

CMOS transistor density has been scaled exponentially in the past two decades and the intrinsic device performance has followed a commensurate scaling trend. Prior to the 90-nm node, mere shrinking of the device dimensions, following Dennard's scaling theory, was sufficient to guarantee increased device performance; beyond the 90-nm node, new innovations were necessary to continue the historical performance scaling trend. Strain engineering and high-k/metal gate technologies were the two major innovations that made the commensurate performance scaling in the past decade possible. However, it appears that new device structures and performance boosters will continue to be the need of the future. This chapter provides a basic overview of MOSFET scaling trend, followed by a discussion of MOSFET operation in deca-nanometer scale based on the so-called virtual source injection model. A simple analytical model for transistor I - V characteristics and intrinsic transistor delay is provided and used to quantify the historical trends of MOSFET performance scaling. Carrier velocity is shown to be the main driver for the continued MOSFET performance increase. Finally, the prospect of velocity increase is reviewed for strained Si, Ge, and compound semiconductors.

1.1 Introduction

The integrated circuit industry has witnessed a tremendous growth in the past four decades. This has been enabled by continuous scaling of transistors as described by Moore's law, which states that the number of the transistor per chip doubles every

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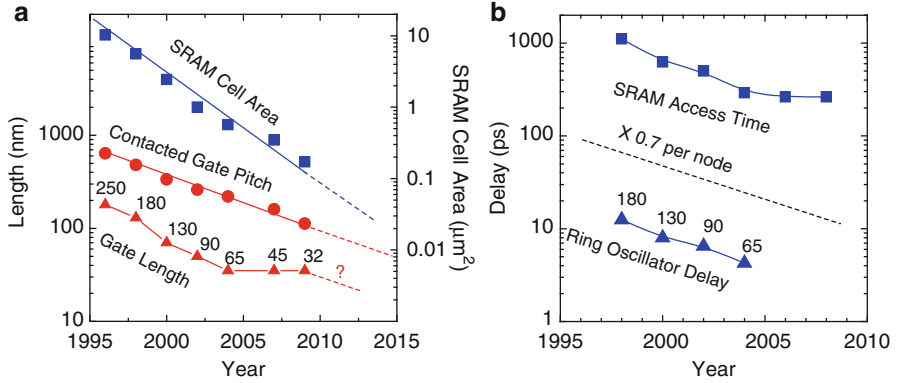


Fig. 1.1 Scaling trend of MOSFET geometry over the past 15 years (a) and the associated decrease in delay (b). MOSFET pitch is scaled by a factor of 0.7 per technology node to accommodate for doubling of transistor count. Up to the 65-nm node, circuit delay has followed the same pace of scaling by a factor of 0.7 per node (Data from Intel)

2 years. As a result, the chip area and thus the cost of delivering a given functionality has dropped exponentially during this period. What happened in practice, however, was that chip area remained almost constant and the chip functionality increased.

The key enabler for the exponential scaling of the CMOS technology is the scaling of the MOSFET pitch, which has been historically scaled by a factor of 0.7 per technology generation as illustrated in Fig. 1.1. Other transistor dimensions have been scaled with almost the same pace, according to Dennard's scaling theory [1]. Note that technology scaling does not necessarily require proportional scaling of the MOSFET gate length as long as it fits the pitch. In fact, Fig. 1.1 shows that starting from 180-nm technology, the gate length was shrunk faster than the pitch, perhaps to achieve higher speed. However, gate length scaling has virtually stopped since the 65-nm node. Of course, this trend cannot continue forever, and at some point, most likely at the 22-nm node, the gate length needs to be scaled down. Up to the 65-nm node, transistor delay followed the pace of 30% reduction per node. This was achieved by mere dimensional scaling down to the 130-nm node and then through various strain engineering techniques since the 90-nm node. However, it appears that delay scaling has slowed down since the 45-nm node. This is due to the fact that parasitic components associated with a MOSFET do not follow the scaling trend and their relative importance increases as transistors shrink.

Figure 1.2 shows the main parasitic components associated with a state-of-the-art MOSFET. The effective fringing capacitor, C_f^* , which consists of the inner fringe, C_{if} , outer fringe, C_{of} , and overlap capacitance, C_{ov} , is approximately 0.5 fF/ μm and does not scale with gate length [3]. In fact, due to the proximity of source/drain contacts to the gate electrode, future technology nodes will suffer from a larger parasitic capacitance [4]. On the other hand, the source/drain series resistance, which consists of the silicide/semiconductor contact resistance and the resistance associated with the heavily doped S/D regions and the extensions, is about

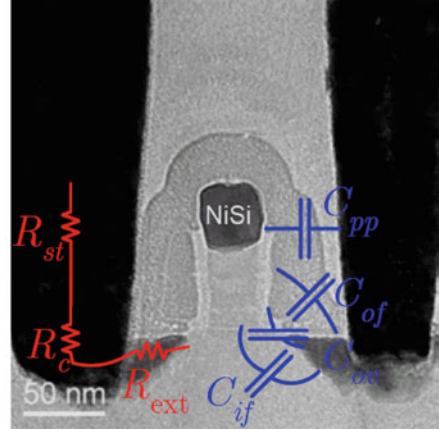
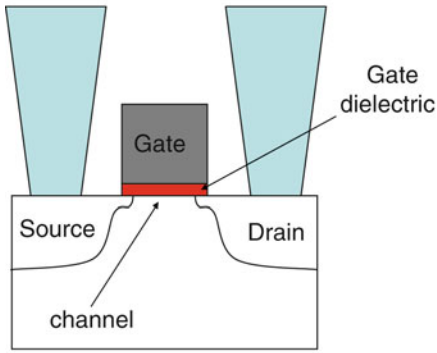


Fig. 1.2 MOSFET structure and its main parasitic components: the effective fringing capacitance, C_f^* , which consists of the inner fringe, C_{if} , outer fringe, C_{of} , and overlap capacitance, C_{ov} , is approximately 0.5 fF/ μm and does not scale with the gate length. In fact, due to the proximity of the gate electrode and S/D contacts, another term, C_{pp} , is added as the device pitch is further scaled down. The source/drain series resistance consists of the silicide/semiconductor contact resistance, R_c , and the series resistance associated with the heavily doped S/D regions and extensions, R_{ext} , and does not scale down very well. As these devices are further shrunk, an additional series resistance due to finite conductivity of the contact studs, R_{st} , is added to the total series resistance (TEM image is reprinted with permission from [2] © 2005 IEEE)

80 $\Omega \mu\text{m}$ per side for modern NFETs and does not scale very well. Furthermore, as the devices are scaled, the resistance associated with finite conductivity of the metal contacts is becoming more significant and remedies, such as Cu contacts, were introduced to minimize this additional component.

An equally important issue for state-of-the-art CMOS is the scaling of the supply voltage (V_{DD}) to keep the power consumption under control as well as to maintain the device reliability. While the supply and threshold voltage (V_T) followed a similar trend in the earlier technology nodes, threshold voltage scaling was eventually slowed down to control the exponentially growing standby power. This means that less gate over drive ($V_{DD} - V_T$) is available as the devices are scaled. In conjunction with the increased importance of the parasitic components, this has already decelerated delay scaling.

A possible solution to compensate for the performance drop imposed by the loss of gate overdrive and the increase in the parasitic components is to improve transport properties of the channel by employing new materials. In fact, over the past decade, strain engineering has been extensively used to alter the transport properties of the Si channel and thereby continue the historical trend of the performance scaling. However, it appears that strained silicon is approaching its limit while the effectiveness of some of the strain engineering methods diminishes as device pitch is scaled below 100 nm. New channel materials are being studied to enable continued transistor performance scaling in the future.

1.2 Basics of MOSFET Operation

As shown in Fig. 1.2, the MOSFET is a three-terminal device, where the gate controls the conductivity of the channel region and thus flow of current between source and drain. The source and drain are doped with a high density of impurity atoms and with a polarity opposite to that in the channel region. For example, in a silicon n-MOSFET the source and drain are doped with arsenic or phosphorus with a density above $1 \times 10^{20} \text{ cm}^{-3}$, while the channel region is doped with boron or indium with a density less than $1 \times 10^{19} \text{ cm}^{-3}$. The gate is separated from the channel by a dielectric with a thickness of about 1 nm. At low gate voltages, there is no electron conduction between the source and drain. When the gate voltage is increased above a threshold voltage,¹ a thin layer of electrons called inversion layer is formed in the channel region, next to the gate dielectric, and makes the flow of electrons from source to the drain possible. In that sense a MOSFET can be considered as a switch; when the gate voltage is smaller than a threshold voltage, there is limited current flow and the transistor is “off”, and when the gate voltage is above the threshold voltage the transistor is “on”.

Of course, the MOSFET is not an ideal switch. When the transistor is “off”, the source-drain current flow is not zero, instead it depends exponentially on the gate voltage as seen in Fig. 1.4. The voltage spent to drop the current by one order of magnitude is called subthreshold swing; ideally 60 mV/dec at room temperature, but typically 80–100 mV/dec for state-of-the-art transistors. Furthermore, unlike an ideal switch, the threshold voltage depends on the voltage across the switch, i.e., the drain to source voltage. This phenomenon is known as drain-induced barrier lowering (DIBL) as will be discussed further in the next section. Ideally, DIBL should be zero but it is typically 50–200 mV/V in state-of-the-art MOSFETs.

To minimize the subthreshold swing and DIBL, the gate needs to have a stronger coupling to the channel than the drain. This is achieved by aggressive scaling of the gate dielectric thickness and by making the source/drain extensions shallow. Also, it will help to confine the carriers closer to the gate dielectric by either placing a heavily doped well or halo (p-type for an NFET) as done in bulk MOSFETs or by making the substrate only a few nanometers thick as done in fully-depleted silicon-on-insulator (FDSOI) devices.

¹ Note that the definition of the threshold voltage is somewhat arbitrary as the transition from off-state to on-state, also known as strong inversion, is gradual. The transition region is often called weak inversion. Several definitions for the threshold voltage are given in the literature. The two most common definitions that are based on the I – V characteristics of the transistor are (1) constant current threshold voltage, where V_T is defined as the gate voltage at which the drain current is equal to an empirically-defined current, usually around 10^{-7} A/WL , with W and L being the gate width and length in micrometer, respectively, and (2) extrapolated threshold voltage, obtained by drawing the tangent to the I – V curve at the point where the transconductance is maximum and finding the intercept with the x -axis.

Obviously, as a switch, it is desired that a MOSFET delivers a high $I_{\text{on}}/I_{\text{off}}$ ratio. In a typical CMOS logic circuit most of the transistors are in the off state at any given time. Reducing the off-current thus minimizes the static power that is wasted even when the circuit is in the idle mode:

$$P_{\text{Static}} = \sum I_{\text{off}} V_{DD}$$

On the other hand, since the transistors in the logic circuit mostly drive capacitive loads, higher on-current enables faster switching:

$$\text{delay} \sim C_{\text{eff}} V_{DD} / I_{\text{on}}$$

A more accurate delay metric is introduced in Sect. 1.5.

1.3 Physics of MOSFET Operation in Deca-Nanometer Scale

The essential physics of state-of-the-art MOSFET operation can be captured by the channel potential barrier model. Note that this is a descriptive model and the actual shape of the barrier depends on the details of the device structure, bias conditions, semiconductor band structure, and carrier transport.

A potential barrier in the channel controls the flow of carriers from source to drain. In the subthreshold regime, i.e., gate voltage smaller than threshold voltage, there is a large barrier to the flow of carriers from source to drain, Fig. 1.3a. The barrier height is linearly controlled by the gate voltage but the thermionic emission of carriers over the barrier is exponentially proportional to the barrier height and hence the current is exponentially proportional to the gate voltage and the temperature. Of course, if the channel is short enough, the barrier will be so narrow that some carriers can directly tunnel from the source to the drain, but this is not the case for a well-designed MOSFET. Increasing the drain voltage in the subthreshold regime slightly decreases the barrier height and makes the barrier slightly narrower, Fig. 1.3b. This is called DIBL and is usually modeled as a reduction in the threshold voltage proportional to the drain voltage. However, it should be noted that the barrier height reduction is not a linear function of the drain voltage and is usually stronger at smaller drain voltages.

When V_G is above the threshold voltage, the barrier is lowered enough so that many carriers can flow over the barrier and towards the drain. The “inversion” charge density in the channel is determined by a Fermi distribution that depends on the difference between the Fermi level and the local potential. In the near equilibrium case shown in Fig. 1.3c, the barrier is extended over almost the entire channel. Therefore, carrier transport depends on the scattering rate over the entire channel. In this case, the transistor current depends linearly on the drain voltage and hence the name linear regime. When the drain voltage is high enough, as in Fig. 1.3d, the

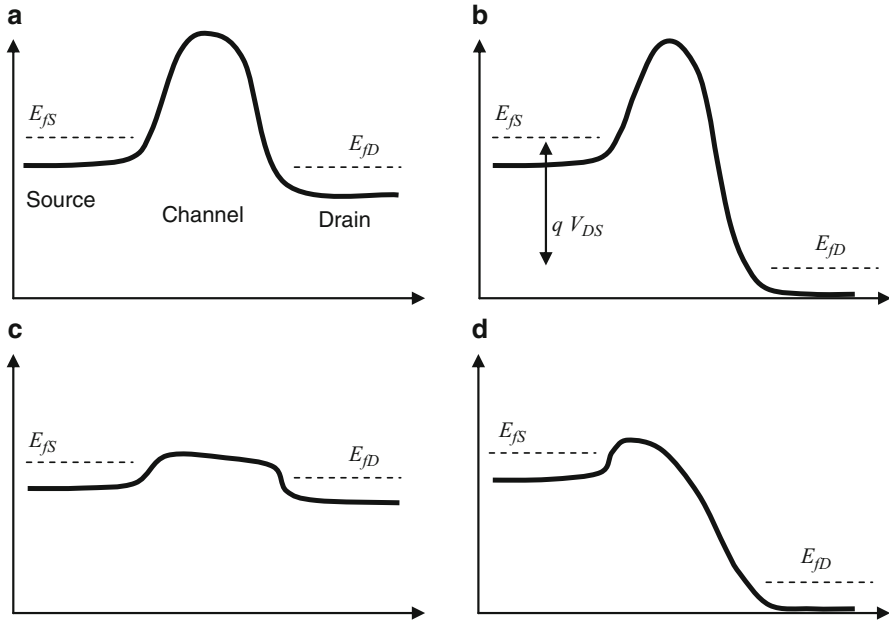


Fig. 1.3 Channel potential barrier at different bias conditions (a) in the subthreshold regime, i.e. $V_G < V_T$, there is a large barrier impeding the flow of carriers from the source to drain. (b) The barrier is lowered and slightly narrowed as the drain voltage is increased. The effect is commonly known as the drain-induced barrier lowering (DIBL) and is modeled as a reduction in the threshold voltage proportional to the drain voltage. With V_G above the threshold voltage, the barrier is low enough that many carriers can go over the barrier and flow to the drain. (c) With a small drain voltage, such a small barrier extends over the entire channel, so the current depends on the scattering mechanism over the entire channel. This is the so-called linear regime, where the current depends linearly on the drain voltage. (d) If the drain voltage is high enough, the barrier extends only over a small region near the source. Carrier transport is effectively controlled by the rate they overcome the barrier at the top of the barrier, the so-called virtual source

barrier extends only over a small region near the source. Carrier transport depends on the rate that they overcome the barrier at its peak, the so-called virtual source. Once a carrier goes past this point, it is unlikely that future scattering events cause the carrier to go back to the source. Although, in its simplest form it is assumed that the transistor current only depends on the scattering rates at the vicinity of the virtual source, it should be noted that the exact shape of the barrier depends on carrier density, which in turn depends on carrier distribution along the channel according to Fermi statistics. To satisfy charge continuity along the channel, the charge density in turn depends on the average carrier velocity, which depends on scattering rates over the entire channel. It is also assumed that in this case the transistor current is almost independent of the drain voltage, except for the reduction of threshold voltage due to DIBL. In other words, the transistor current saturates as drain voltage increases and hence the name saturation regime.

1.4 Simple MOSFET Model

In this section, a simple I – V model is presented for a MOSFET that operates in the saturation regime. The reader is referred to [5] for a complete model that is applicable to both linear and saturation regimes and the transition between the two. The drain current normalized to the width, I_D/W , of a MOSFET can be described by the product of the local charge areal density times the local carrier velocity anywhere in the channel. According to the “virtual source” MOSFET model, for a well-tempered MOSFET, the inversion charge density at the virtual source is independent of the drain voltage except for the DIBL. Also, by direct comparison to measured data, it turns out that the average carrier velocity at the virtual source is weakly dependent on either V_{GS} or V_{DS} , provided that the transistor is biased in saturation. Hence,

$$I_D/W = Q_{ix0} v_{x0} \quad (1.1)$$

where, Q_{ix0} is the inversion charge density and v_{x0} is the average carrier velocity at the virtual source. To model the virtual-source inversion charge density, the following empirical expression allows for a continuous model from weak to strong inversion:

$$Q_{ix0} = C_{\text{inv}} n \phi_t \ln \left(1 + \exp \frac{V'_{GS} - (V_T - \alpha \phi_t F_f)}{n \phi_t} \right) \quad (1.2)$$

where C_{inv} is the effective gate-to-channel capacitance per unit area in strong inversion, ϕ_t is the thermal voltage ($k_B T/q$), $V'_{GS} = V_{GS} - I_D R_S$ is the internal gate–source voltage, i.e., corrected for the voltage drop on the source resistance R_S , n is the subthreshold coefficient, which is related to the so-called “subthreshold swing” by $S = n \phi_t \ln 10$, and $V_T = V_{T0} - \delta V'_{DS}$, where V_{T0} is the strong-inversion threshold voltage at $V_{DS} = 0$, and $V'_{DS} = V_{DS} - I_D (R_S + R_D)$ is the internal source–drain voltage corrected for the drop across the source and drain resistances, with δ being the DIBL coefficient with units of volt per volt. The term $\alpha \phi_t F_f$ allows for the requirement of different values of the threshold voltage in strong and weak inversion or in other words the so-called “constant-current” and “extrapolated” threshold voltages. A Fermi transition function F_f is used to allow for smooth transition between the two values [5].

In the strong inversion the above model can be reduced to

$$I_D/W = C_{\text{inv}} (V_{GS} - V_T) v, \quad (1.3)$$

where

$$v = \frac{v_{x0}}{1 + C_{\text{inv}} R_S W (1 + 2\delta) v_{x0}} \quad (1.4)$$

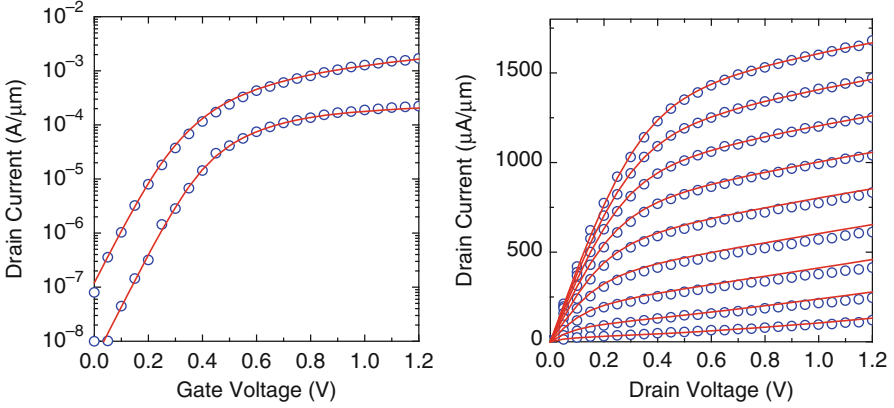


Fig. 1.4 Comparison of the analytical transistor model (*lines*) with data (*circles*) for a 65-nm node uniaxially strained NFET

is the effective velocity. Note that the notion of the “effective velocity” is just to simplify the mathematics. In the presence of S/D series resistance the internal gate-source voltage is less than the V_{GS} measured at the terminals and hence the actual inversion charge is less than $C_{inv}(V_{GS} - V_T)$. The effective velocity is defined as the apparent velocity for (1.3) to hold as if the inversion charge is given by $C_{inv}(V_{GS} - V_T)$.

1.5 MOSFET Performance Metric

Historically a CV/I metric has been used as a measure of the intrinsic MOSFET performance, where C is usually the inversion capacitance, i.e. $C_{inv} L_G$, sometimes corrected for some parasitic capacitances, V is the operating voltage V_{DD} , and I is the on-current, i.e., the current at $V_{GS} = V_{DS} = V_{DD}$. This simple metric worked fine for earlier technology nodes despite the fact that the switching charge $C_{inv} L_G V_{DD}$ does not include the parasitic capacitances inherent to the transistor and that the drain voltage never reaches I_{on} during switching. This is because of the fact that this metric also overestimates the inversion charge. However, as stated in Sect. 1.1, the relative importance of parasitic capacitances increases as transistor dimensions shrink.

To refine the delay metric, an “effective current”, defined as the average of several points on the I - V loci of the transistor during the transition between logic states, was shown to better predict transistor delay. The most common definition is [6]:

$$I_{eff} = (I_D(V_{GS} = V_{DD}, V_{DS} = V_{DD}/2) + I_D(V_{GS} = V_{DD}/2, V_{DS} = V_{DD}))/2 \quad (1.5)$$

A significant observation is that usually the ratio $I_{\text{eff}}/I_{D\text{sat}}$ decreases as transistors are scaled down, mainly due to increased DIBL, which decreases the output resistance of the transistor. Future device designs should thus be aimed at increasing the effective current by controlling the short channel effects, while maintaining an acceptable on-current.

The intrinsic transistor delay is defined as $\tau = \Delta Q_G/I_{\text{eff}}$ [3], where I_{eff} is given by (1.5) and ΔQ_G is the charge difference between the two logic states, that includes both channel and fringing field charges. It follows that:

$$\tau = \frac{(1 - \delta)V_{DD} - V_T + (C_f^*V_{DD}/C_{\text{inv}}L_G) \frac{L_G}{v}}{(3 - \delta)V_{DD}/4 - V_T} \quad (1.6)$$

The above delay formulation should be compared to the conventional CV/I :

$$\tau = \frac{V_{DD}}{V_{DD} - V_T} \frac{L_G}{v} \quad (1.7)$$

that shows no dependence on DIBL and parasitic capacitances.

Some comments are in order here: First, the delay formulation of (1.6) uses the concept of effective current, which is only valid for $V_{DD} > 2V_T$ [6]. Also, strictly speaking, the delay formulation should use PMOS parameters in the numerator for charge estimation and NMOS parameters in the denominator for effective current calculation, and vice versa. However, in a given technology, NMOS and PMOS transistors usually have similar threshold voltages, DIBL, gate lengths, and inversion and fringing capacitances, and hence it is reasonable to use the intrinsic transistor delay given by (1.6) based on one transistor type only. The strength of (1.6) lies in the fact that it provides an analytical expression for the transistor delay based on the parameters that can be easily extracted for a given technology and have physical meaning. Therefore, it provides an easy method to explore design space, device structures, and material systems.

1.6 Historical Trend of MOSFET Performance Scaling

Figure 1.5 shows the historical trend of the intrinsic delay for some benchmark technologies, calculated using (1.6). It is interesting to note that across many technology generations with different flavors of the device architecture, the intrinsic transistor delay has scaled almost linearly in proportion to the gate length. Of course, in recent years various strain engineering methods have been incorporated to enhance carrier transport in the channel to continue the historical scaling trend. As reflected in Fig. 1.5, strain engineering is in fact essential for continued performance increase, otherwise there would be saturation in the delay versus gate length behavior.

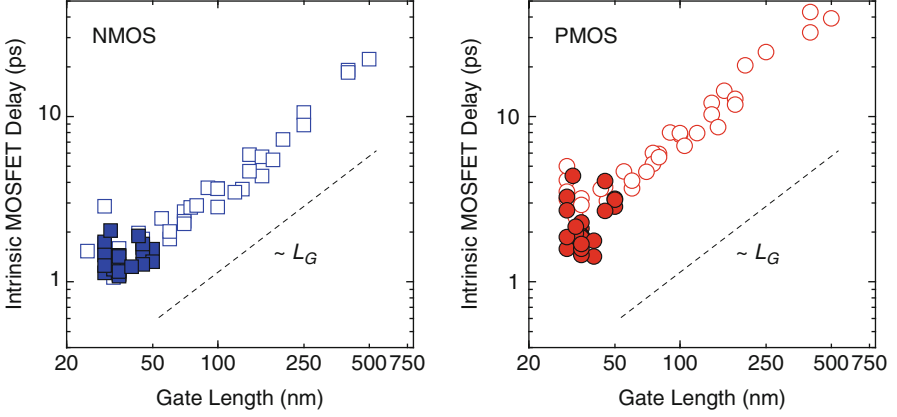


Fig. 1.5 Historical trend of the intrinsic transistor delay for some benchmark technologies. *Filled symbols* represent strain-engineered devices. Across many technology generations with different device designs, the intrinsic transistor delay has scaled almost linearly in proportion to the gate length. However, saturation of performance scaling is seen in the most recent technology nodes, especially if strain engineering is not used

1.7 Velocity Evolution in Silicon-Based MOSFETs

Even though the relative importance of the parasitic components, mainly parasitic capacitance through the increase in the $C_f^*/C_{inv}L_G$ term in (1.6), grows as the transistors are scaled, Fig. 1.5 shows that over the past two decades the intrinsic MOSFET delay has decreased in proportion to the gate length. In fact, to compensate for the increase in the first term of (1.6) and maintain commensurate scaling of the delay with gate length, the effective velocity had to increase. To analyze the evolution of velocity with dimensional scaling, it is more instructive to perform the study in terms of the virtual source velocity, v_{x0} . The virtual source velocity is in turn related to the ballistic velocity, v_θ , through the ballistic efficiency, B ,

$$v_{x0} = Bv_\theta = \frac{\lambda}{2l + \lambda} v_\theta \quad (1.8)$$

where λ is the backscattering mean free path of carriers in the vicinity of the virtual source and l is the critical length for backscattering to the source [7], which is shown through Monte Carlo simulations to be proportional to the distance over which the potential drops by $k_B T/q$.

Figure 1.6 shows the extracted virtual source velocity for the benchmark technologies as a function of gate length. As l decreases in proportion to the channel length, the virtual source velocity increases. However, for gate lengths below 100 nm there is a saturation in the velocity, most likely due to increased Coulomb

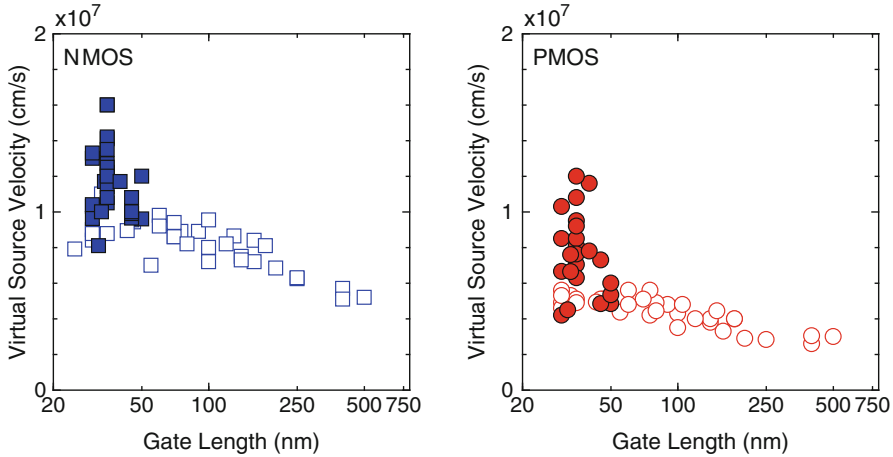


Fig. 1.6 Extracted virtual source velocity, v_{x0} , as a function of gate length for benchmark technologies. *Filled symbols* represent strain-engineered devices. Saturation of virtual source velocity is seen for unstrained devices below a gate length of about 100 nm

scattering that results from increased doping necessary to maintain electrostatic integrity. In recent years, innovations in strain-engineering have restored the velocity increase by improving mobility and ballistic velocity.

1.8 Limits of Velocity Increase in Strained Silicon

So far, electron velocity enhancement has been limited by the magnitude of uniaxial strain exerted on the transistor channel. While with most local strain-engineering methods, channel strain is limited to about 0.5%, it is possible to achieve uniaxial strain with a magnitude well beyond 1% by preferential relaxation of biaxial strain [8–10]. Early short-channel devices show promising results [10], but devices with more competitive S/D resistances are yet to be fabricated to assess whether higher strain levels translate to significant enhanced carrier velocity. Nevertheless, the fact that mobility enhancement of about 100% is maintained at low temperatures [8] suggests that the enhancement is most likely due to a decrease in effective mass and hence should yield significant velocity increase [3].

On the contrary, experimental data on short-channel PFETs demonstrate that although hole mobility as high as $4\times$ with uniaxially strained (100) Si [11], and $8\times$ with strained (110) wafers [12] compared to relaxed (100) Si, has been observed, the enhancement in virtual source velocity is limited to about a factor of 2, as shown in Fig. 1.7a. In fact, band structure calculations suggest that the enhancement in ballistic hole velocity saturates to about a factor of 2, as shown in Fig. 1.7b. This is due to the fact that the band structure near the top of the valence

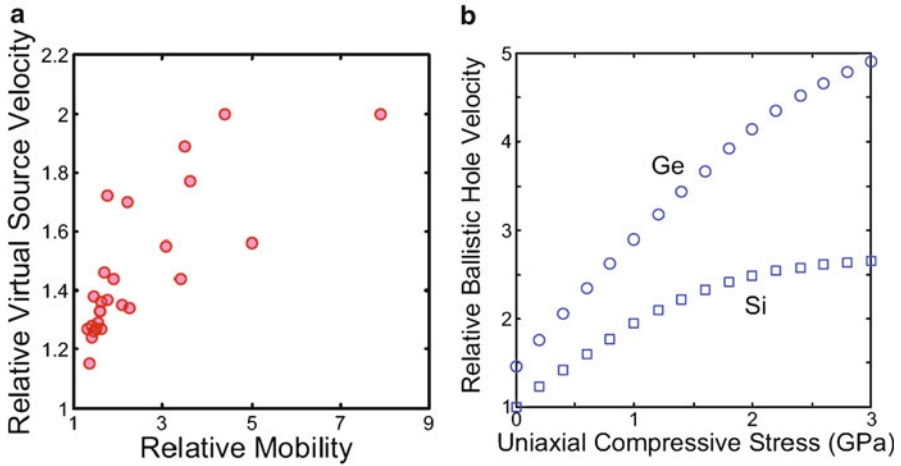


Fig. 1.7 (a) Relative virtual source velocity as a function of relative mobility, extracted from short channel strain-engineered PFETs. Data are referenced to control devices built on (100) Si with [110] channel direction. (b) Calculated ballistic hole velocity in uniaxially strained Si and Ge with (100) and [110] surface and channel orientation, respectively, and normalized to the velocity in relaxed Si. Calculations are performed with non-self-consistent $k \cdot p$ method and demonstrate that in strained Si ballistic hole velocity does not increase with compressive stress above roughly 2 GPa. Relaxed Ge does not offer significant benefits over Si, in agreement with experimental data. However, considerably higher velocities are expected with uniaxially strained Ge (Reprinted with permission from [4]. © 2005 IEEE)

band does not change further once a stress level of about 2 GPa is reached. The band structure at higher energies, which are still within reach of optical phonon energy, continues to change and thus offers higher hole mobility due to reduction in interband scattering.

1.9 Prospects of Velocity Increase in Ge and III-V Semiconductors

Figure 1.8a compares the estimated virtual-source velocity from short-channel Ge PFETs with corresponding numbers in state-of-the-art relaxed and strained Si transistors. Only a small enhancement is expected from either relaxed or biaxially strained Ge and SiGe, despite the fact that mobility enhancement in excess of a factor of 2 compared to relaxed Si has been reported in these devices. On the contrary, with uniaxially strained Ge significantly higher hole velocities are expected as shown in Fig. 1.7b. In fact, early uniaxially strained SiGe-channel MOSFETs show promising results and further advancement is anticipated in the future as embedded SiGe stressor loses its effectiveness in sub-100-nm transistor pitch and is not straightforward to be integrated with FDSOI device structures that are anticipated in 20-nm node and beyond.

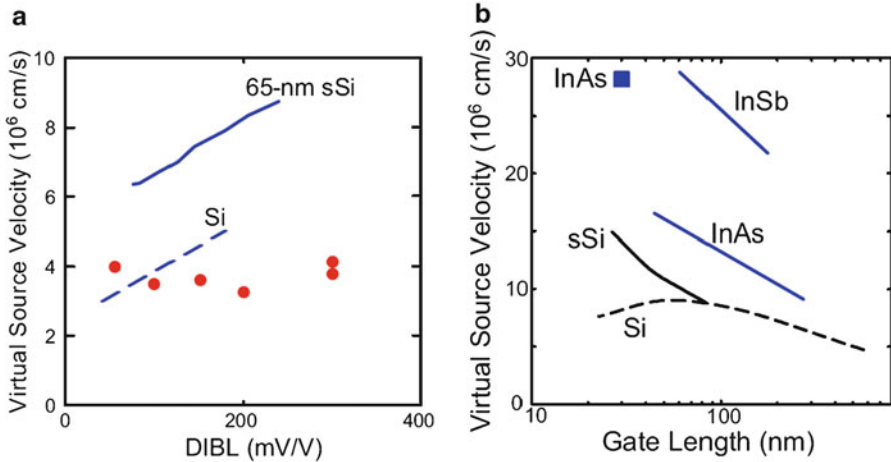


Fig. 1.8 (a) Hole virtual source velocity extracted from short-channel Ge PFETs from literature (*symbols*) compared with historical data for relaxed and uniaxially strained Si. Experimental data for both relaxed and biaxially strained Ge are included, demonstrating that without uniaxial strain, Ge does not offer any benefit over relaxed Si. (b) Comparison of virtual source velocity in deeply scaled III–V HEMTs and historical Si data (Reprinted with permission from [4]. © 2005 IEEE)

For electrons, III–V channel transistors [13–15] offer significantly higher velocity over state-of-the-art strained Si as shown in Fig. 1.8b. However, this is accompanied by small band-gap and effective mass, which lead to high band-to-band tunneling that limits the supply voltage [16]. Special device design combining the reduced-drain-electric-field benefits of HEMT architecture with reduced resistance of source/drain self-alignment will be essential to realize the intrinsic electron transport benefits. An additional challenge is that due to small quantization mass, the inversion capacitance with these materials is relatively small compared to Si MOSFETs with equivalent dielectric thickness and this can limit the anticipated drive current increase and device performance [17]. Note that since the switching charge is dominated by parasitic capacitances, the conventional CV/I metric, which suggests that reduction of the inversion capacitance is beneficial, is not a good choice for performance benchmarking particularly in this case [3]. Thus, it is anticipated that III–V channel materials can only have significant NFET performance benefit if T_{inv} (thickness of inversion layer) and R_S values are similar to competing Si devices. The same requirements also hold for PFETs with Ge or GeSi compounds, which do hold promise of higher hole velocity than Si.

1.10 Summary and Conclusions

This chapter provided an overview of the historical MOSFET performance scaling and studied basic dependencies of the performance on device parameters. Basics of MOSFET operation in deca-nanometer regime were reviewed and a simple

analytical model was presented that describes the I - V characteristics of the MOSFET based on a set of parameters that are physically meaningful and are usually reported in the literature. An analytical expression for intrinsic MOSFET delay was then provided and used to study the historical trends of MOSFET performance scaling. Virtual source velocity of carriers was shown to be the main driver for increased performance over the past two decades. Limits of strain-engineered velocity increase in Si-channel MOSFETs were discussed and it was concluded that it is unlikely that strained-Si provides velocity increase higher than what is achieved in today's state-of-the-art MOSFETs. Finally, prospects of velocity increase in Ge and III-V channel devices were discussed. It was shown that without uniaxial compressive strain, Ge or GeSi-channel MOSFETs do not provide any benefit over strained-Si. Higher velocities are expected in uniaxially strained Ge, but solid experimental data is still missing. In contrast, electron velocity values significantly higher than achieved in strained-Si have been already demonstrated in III-V devices. However, the performance of these devices is mainly limited because of the small quantization and density-of-states effective mass in these materials, which results in smaller C_{inv} compared to Si MOSFET.

The material presented in this chapter provides the basis for benchmarking devices with novel channel materials. In particular, (1.2)–(1.4) provide a methodology for extracting virtual source velocity from I - V and C - V measurements. As long as the measured transistors are well-behaved, i.e., have reasonable DIBL, and have a gate length less than about 100 nm, the extracted velocity can be used to predict the performance of a hypothetical device with more aggressive gate length and with aggressively scaled gate dielectric and reduced series resistance. Equation (1.6) then gives an estimate of the intrinsic delay of such a hypothetical transistor provided that realistic assumptions are made about the parasitic capacitances. This approach yields more realistic benchmarking results than using popular metrics such as long channel mobility, on-current, or delay and energy calculations that are based on the CV/I metric.

References

1. R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. Leo Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, pp. 256–268, 1974.
2. F. Boeuf, *et al.*, "0.248 μm^2 and 0.334 μm^2 conventional bulk 6 T-SRAM bit-cells for 45 nm node low cost - general purpose applications," in *Symp. VLSI Tech.*, pp. 130–131, 2005.
3. A. Khakifirooz and D. A. Antoniadis, "MOSFET performance scaling – Part I: Historical trends," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1391–1400, 2008.
4. A. Khakifirooz and D. A. Antoniadis, "MOSFET Performance scaling – Part II: Future directions," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1401–1408, 2008.
5. A. Khakifirooz, O.M. Nayfeh, and D.A. Antoniadis, "A simple semiempirical short-channel MOSFET current-voltage model continuous across all regions of operation and employing only physical parameters," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1674–1680, 2008.
6. M. H. Na, E. J. Nowak, W. Haensch, and J. Cai, "The effective drive current in CMOS inverters," in *IEDM Tech. Dig.*, Dec. 2002, pp. 121–124.

7. M. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electron Device Lett.*, vol. 22, no. 6, pp. 293–295, 2001.
8. T. Irisawa, T. Numata, T. Tezuka, N. Sugiyama, and S. Takagi, "Electron transport properties of ultrathin-body and tri-gate SOI nMOSFETs with biaxial and uniaxial strain," in *IEDM Tech. Dig.*, 2006, pp. 457–460.
9. P. Hashemi, L. Gomez, M. Canonico, and J.L. Hoyt, "Electron transport in gate-all-around uniaxial tensile strained-Si nanowire n-MOSFETs," in *IEDM Tech. Dig.*, 2008, pp. 865–868.
10. K. Maitra, A. Khakifirooz, P. Kulkarni, *et al.*, "Aggressively scaled strained-silicon-on-insulator undoped-body high-k/metal-gate nFinFETs for high-performance logic applications," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 713–715, 2011.
11. S. Narasimha, *et al.*, "High performance 45 nm SOI technology with enhanced strain, porous low-k BEOL, and immersion lithography," in *IEDM Tech. Dig.*, 2006, p. 689.
12. B. Yang, *et al.*, "Stress dependence and poly-pitch scaling characteristics of (110) PMOS drive current," in *Symp. VLSI Tech.*, 2007, pp. 126–127.
13. D.-H. Kim and J. A. del Alamo, "Logic Performance of 40 nm InAs HEMTs," in *IEDM Tech. Dig.*, 2007, p. 629.
14. D.-H. Kim and J. del Alamo, "30 nm E-mode InAs PHEMTs for THz and future logic applications," in *IEDM Tech. Dig.*, 2008, p. 30.1.1.
15. G. G. Dewey, M. K. Hudait, K. Lee, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, and R. Chau, "Carrier transport in high-mobility III–V quantum-well transistors and performance impact for high-speed low-power logic applications," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1094–1097, 2008.
16. D. Kim, T. Krishnamohan, H.S.P. Wong, and K.C. Saraswat, "Band to band tunneling study in high mobility materials : III-V, Si, Ge and strained SiGe," in *Device Research Conf.*, 2007, p. 57.
17. K. D. Cantley, Y. Liu, H. S. Pal, T. Low, S. S. Ahmed, and M. S. Lundstrom, "Performance analysis of III-V materials in a double-gate nano-MOSFET," in *IEDM Tech. Dig.*, 2007, p. 113.

Further Reading

- Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 2nd Ed., 2009.
- D.K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley and Sons, 3rd Ed., 2006.
- M. Lundstrom, *Fundamentals of Carrier Transport*, Cambridge University Press, 2000.
- S. Datta, *Electronic Transport in Mesoscopic Systems*, Cambridge University Press, 1997.

Chapter 2

Electronic Transport in Graphene

Jun Zhu

This chapter provides an experimental overview of the electrical transport properties of graphene and graphene nanoribbons, focusing on phenomena related to electronics applications. Section 2.1 gives a brief description of the band structure. Section 2.2 discusses the effect of various scattering mechanisms in 2D sheets and nanoribbons and compares the characteristics of exfoliated and synthesized graphene. The physics of high-bias transport in graphene field effect transistors is described in Sect. 2.3. Section 2.4 gives a brief summary and outlook.

2.1 Electronic Band Structure of Graphene

2.1.1 Tight-Binding Calculations

Figure 2.1 shows the hexagonal lattice of graphene, where each unit cell contains two carbon atoms, A and B. The lattice vectors $a_1 = a/2(\sqrt{3}, 1)$ and $a_2 = a/2(\sqrt{3}, -1)$, where $a = \sqrt{3}a_{c-c} = 2.46 \text{ \AA}$ is the lattice constant. In the reciprocal lattice space, the first Brillouin zone spanned by the wave vector $k = (k_x, k_y)$ is also hexagonal. Of particular importance are the two inequivalent points K and K' at the six corners of the Brillouin zone. Their positions are given by $\pm 2\pi/\sqrt{3}a(1, 1/\sqrt{3})$, $\pm 2\pi/\sqrt{3}a(0, 2/\sqrt{3})$, and $\pm 2\pi/\sqrt{3}a(-1, 1/\sqrt{3})$. The low-energy electronic band structure of graphene can be well described by a simple tight-binding Hamiltonian

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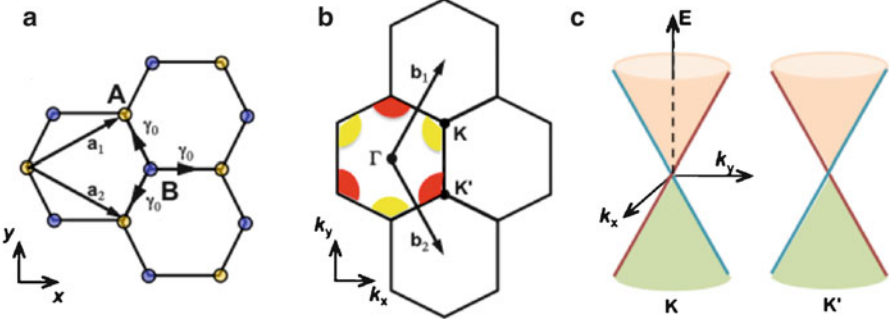


Fig. 2.1 The band structure of graphene. (a) The hexagonal lattice of graphene. (b) The reciprocal lattice in momentum space. (c) The Dirac cones near the K and K' points of the Brillouin zone. Carriers in the same cone with opposite momenta have opposite pseudo-spins. Carriers in different cones with opposite momenta have the same pseudo-spin

considering only nearest-neighbor hopping and one π orbital per carbon atom. This simple model allows for an analytical solution of the energy bands [1]:

$$E^\pm(k_x, k_y) = \pm\gamma_0 \sqrt{1 + 4 \cos(\sqrt{3}k_x a) \cos(k_y a) + 4 \cos^2(k_y a/2)} \quad (2.1)$$

where $\gamma_0 \sim 2.7$ eV is the nearest-neighbor hopping integral shown in Fig. 2.1a.

In pristine undoped graphene, the conduction and valence bands touch at the K and K' points. Expanding equ. (2.1) near K (K') yields a linear dispersion:

$$E^\pm(\boldsymbol{\kappa}) = \pm\hbar v_F |\boldsymbol{\kappa}| \quad (2.2)$$

where $\boldsymbol{\kappa} = \mathbf{k} - \mathbf{K}$ ($\mathbf{K}'$) is the wave vector measured from $\mathbf{K}$ ($\mathbf{K}'$) and v_F is the electronic group velocity given by:

$$v_F = \sqrt{3}\gamma_0 a / 2\hbar \quad (2.3)$$

Equation (2.2) produces touching conic bands at the K and K' points of the Brillouin zone as shown in Fig. 2.1c. Electrons in graphene are referred to as Dirac fermions because of this linear, photon-like dispersion and the touching points in momentum space are called Dirac points. The Fermi level E_F resides precisely at the Dirac point in undoped graphene. E_F increases (decreases) upon electron (hole) doping. Equation (2.2) is a good approximation as long as the energy does not deviate too far from E_F , or conversely that the momentum does not deviate too far from the K (K') point. This condition is satisfied in most current graphene devices.

Angle resolved photoemission spectroscopy (ARPES) shows that electron-phonon coupling produces small deviations from the linear bands as E_F rises [2] above 200 meV. Graphene also possesses an additional quantum number called pseudo-spin, which originates from its two equivalent A and B sublattices. The pseudo-spin of an electron rotates along the Dirac cone, locked to the momentum wave vector $\mathbf{k}$.

Hence carriers with opposite $\mathbf{k}$ have also opposite pseudo-spin; their wave functions are orthogonal and have no overlap. Consequently, 180° backscattering is forbidden in graphene. Defects that break this A-B sublattice symmetry will also break the pseudo-spin conservation. Examples are atomic defects, ripples and dislocations.

Because of its linear bands, the effective mass of electrons and holes in graphene is defined as

$$m^* = \hbar^2 k / (dE(k)/dk)|_{E=E_F}$$

instead of

$$m^* = \hbar^2 / (d^2 E(k)/dk^2)|_{E=E_F}$$

used in conventional parabolic band semiconductors. An analogy to photons gives $E_F = m^* v_F^2$. The two expressions yield identical results: $m^* = \hbar \sqrt{\pi n / v_F}$. In this simple model, the effective mass is isotropic, electron–hole symmetric and is proportional to $\sqrt{n}$, where n is the carrier density. This $\sqrt{n}$ dependence has been confirmed experimentally and the Fermi velocity v_F is measured to be approximately $1.0\text{--}1.1 \times 10^6$ m/s in graphene [3]. This is somewhat larger than the v_F given by first-principles calculations of γ_0 and may already contain substantial corrections from electron–electron interactions beyond the tight-binding model [4, 5]. Using the so-defined effective mass m^* , the density of states in graphene can be written just like a conventional two-dimensional electron gas (2DEG):

$$\rho(E) = \frac{2E}{\pi \hbar^2 v_F^2} = \frac{2\sqrt{\pi n}}{\pi \hbar v_F} = \frac{2m^*}{\pi \hbar^2} \quad (2.4)$$

where a fourfold degeneracy (two due to spin and two due to the K/K' valley) has been taken into account. The density of states increases linearly with E and is proportional to $\sqrt{n}$, vanishing at the Dirac point. The linear dispersion and the absence of a band gap gave rise to many unusual electronic properties in graphene such as the half-integer quantum Hall effect, Klein tunneling, minimum conductivity and weak anti-localization. For detailed reviews, see [3, 6].

2.1.2 Graphene Nanoribbons

As the size of a graphene sheet shrinks in one direction, its electronic properties change accordingly. Two important considerations emerge in graphene nanoribbons (GNRs), namely, quantum confinement and the effect of edge states. Figure 2.2a and b show schematics of two GNRs with identical width W but two different kinds of edge terminations: armchair in (a) and zigzag in (b). In both cases, electronic states are confined in the x direction, similar to a particle confined in a one-dimensional quantum well. This quantum confinement leads to quantized momentum $k_x = n\pi/W$ ($n = 0, 1, 2, \dots$). It slices the Brillouin zone into discrete energy bands as shown in Fig. 2.2c.

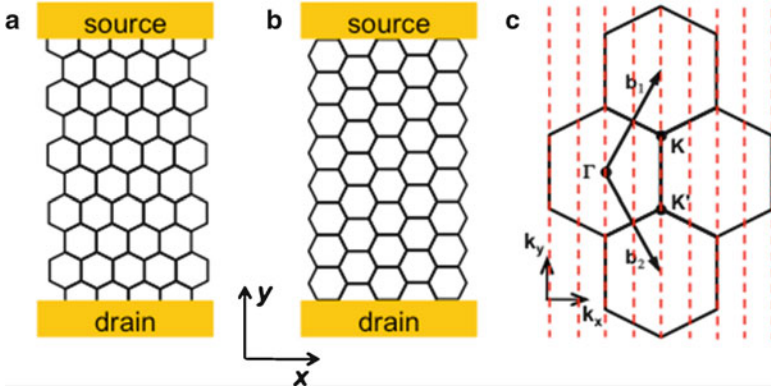


Fig. 2.2 The edge configurations of nanoribbons. (a) An armchair ribbon. (b) A zigzag ribbon. (c) Confinement in the x direction quantizes k_x , as illustrated by the dashed lines. This quantization slices the band structure of 2D graphene into 1D discrete bands

The spacing between adjacent bands is on the order of $\Delta E \approx \hbar v_F \pi / W$ or $2 \text{ eV} / W (\text{nm})$. The finite gap in its band structure makes the GNR potentially useful in digital nanoelectronics, an arena of applications closed to 2D single-layer graphene because of the lack of a band gap. In practice, this is a technically challenging route since a sizable bandgap of $\sim 1 \text{ eV}$ requires a small W , on the order of a few nm. This will be further explained in Sect. 2.2.3 when experiments on GNRs are discussed.

The quick estimate above neglected the effect of edge termination. GNRs may be metallic or semiconducting depending on their edge termination. This sensitivity shouldn't be surprising since GNRs are really just unrolled carbon nanotubes. In Fig. 2.3, the electronic dispersion of a zigzag (a) and two armchair GNRs (b, c) are shown [7, 8]. These results are obtained by solving the Dirac equation with appropriate boundary conditions.

Figure 2.3a shows that zigzag GNRs possess a dispersionless state at the Fermi energy, which is localized in real space near the ribbon's edge and decays exponentially into the ribbon's interior. These edge states can also be spin polarized when a transverse electric field is applied across the width of the ribbon, leading to so-called "half metallicity" [9]. An armchair GNR does not have such an edge state; it can be either semiconducting or metallic depending on the width of the ribbon W . (Interestingly, a zig-zag carbon nanotube "unfolds" into an armchair GNR, hence the following counting rule.) An armchair GNR with $W = (3n + 1)a$, where n is an integer and $a = 2.46 \text{ \AA}$ is the lattice constant of graphene, is metallic with conic bands at the Γ point of the Brillouin zone (Fig. 2.3c). In other cases, a gap opens and the ribbon is semiconducting (Fig. 2.3b). In realistic devices, the edge often contains a mixture of zigzag and armchair regions. Calculations show that the zigzag edge states can survive to some degree in a wider ribbon ($W > \text{a few nm}$) so long as there aren't too many armchair sites [8]. Beyond the simple picture presented above, first-principles calculations show that the size of the band gap not only depends on the width of the ribbon but also on the edge functionalization and

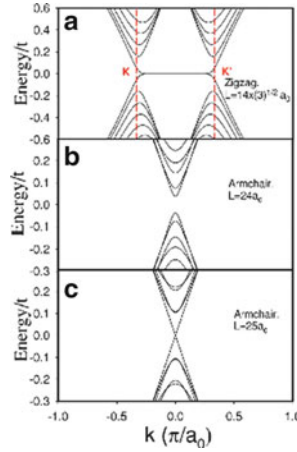


Fig. 2.3 The band structure of nanoribbons showing the dispersionless, localized edge states in a zigzag GNR in (a). The bands of gapped and gapless armchair GNRs are shown in (b) and (c) respectively (Reproduced with permission from [7]. © 2006 American Physical Society)

crystallographic details of the edge [10]. Both are experimental factors that are not well understood or controlled at the moment. Experimental results on the transport characteristics of GNR devices are presented in Sect. 2.2.3.

2.2 Electronic Transport

2.2.1 Electron-Phonon Scattering

Since its discovery, graphene has been hailed as a promising transistor material. Its carrier mobility μ reaches $10,000 \text{ cm}^2/\text{Vs}$ at room temperature, in comparison to less than $1,000 \text{ cm}^2/\text{Vs}$ in silicon MOSFETs. What is the secret behind this superb performance? Due to pseudo-spin conservation, complete backscattering (180°) is forbidden. However this suppression only contributes to an approximate twofold increase in μ since large angle scattering is still allowed. The key reason of graphene's high mobility at room temperature has to do with its phonons, *i.e.*, lattice vibrations. In conventional semiconductor materials such as silicon and GaAs, optical phonon scattering dominates at room temperature, causing a sharp decrease of the electron mobility with increasing temperature [11]. In graphene, the energies of optical phonons are too high ($\hbar\Omega > 150 \text{ meV}$) to participate at room temperature [12, 13]. However, electrons do interact with longitudinal acoustic (LA) phonon modes of graphene and the emission and absorption of LA phonons lead to

momentum loss and the generation of resistance. The contribution to the resistivity from LA phonons is temperature-dependent and can be described by [14]:

$$\rho_{ph}(T, n) = \frac{h}{e^2} \frac{\pi^2 D^2 k_B T}{2h^2 \rho_m v_{ph}^2 v_F^2} \quad (2.5)$$

where D is the acoustic deformation potential, $v_{ph} = 2.1 \times 10^4$ m/s is the sound velocity of LA phonons in graphene and $\rho_m = 6.5 \times 10^{-7}$ kg/m² the areal mass density of graphene. Equation (2.5) applies to the high-temperature regime $T > T_{BG}$, where $T_{BG} = 2\hbar k_F v_{ph}/k_B$ is the Bloch-Grüneisen temperature. As T drops below T_{BG} , the phonon wave vector drops below $2k_F$ and forward scattering becomes increasingly dominant. Forward scattering produces a small momentum change and consequently the phonon resistance vanishes more rapidly with temperature, following a T^4 power law [15].

The linear- T dependence described in (2.5) has been observed experimentally and the acoustic deformation potential D is found to be approximately [16, 17] 18 eV. The LA phonon resistivity amounts to roughly 0.1 Ω/K , a very small number thanks to high sound velocity in graphene. It is independent of carrier density, which leads to $\mu_{LA} \sim 1/n$. At room temperature and $n = 1 \times 10^{12}/\text{cm}^2$, μ_{LA} is approximately 2×10^5 cm²/Vs. This intrinsic mobility value is still 2 orders of magnitude higher than the measured mobility of most current graphene devices, but it will be the ultimate mobility limit of graphene devices. Figure 2.4a shows the measurements of Chen et al. The linear- T regime extends down to 30 K, which is around $T_{BG} \sim 50\sqrt{n}$, where T_{BG} is in kelvin, and n is in 10^{12} cm^{-2} . The Bloch-Grüneisen regime at lower temperature is difficult to probe in these samples, but has been measured in electrolyte-gated graphene, where a high carrier density in the range of $10^{14}/\text{cm}^2$ increases T_{BG} by an order of magnitude and measurements there indeed reveal a T^4 dependence, in good agreement with theory [14, 15].

The readers might also notice that in Fig. 2.4a the linear- T dependence is superseded by a more rapid rise above $T \sim 100\text{--}150$ K. But it was already said that the optical phonons in graphene are irrelevant. Where then does this additional T -dependence come from? This is because, in most devices, the graphene sheet is supported by a substrate, typically SiO₂, and is not suspended in space. This situation is similar to silicon MOSFETs, where carriers in the silicon inversion layer are scattered by the electric field generated by polar optical phonon modes in the adjacent gate oxide [18]. This process is called remote oxide phonon (ROP) scattering and can also occur in graphene on SiO₂, giving rise to additional resistance and temperature dependence. The experimental evidence of ROP scattering in such devices is convincing, with the observations quantitatively reproduced in multiple samples and in different laboratories under different measurement conditions [16, 17]. This effect is also well-understood and modeled theoretically [18, 19] and a good agreement between theory and experiment exists. At room temperature, two optical modes of the SiO₂ substrate, $\hbar\Omega_1 \approx 60$ meV and $\hbar\Omega_2 \approx 150$ meV contribute to ROP scattering and together impose an extrinsic mobility limit of roughly 4×10^4 cm²/Vs [16].

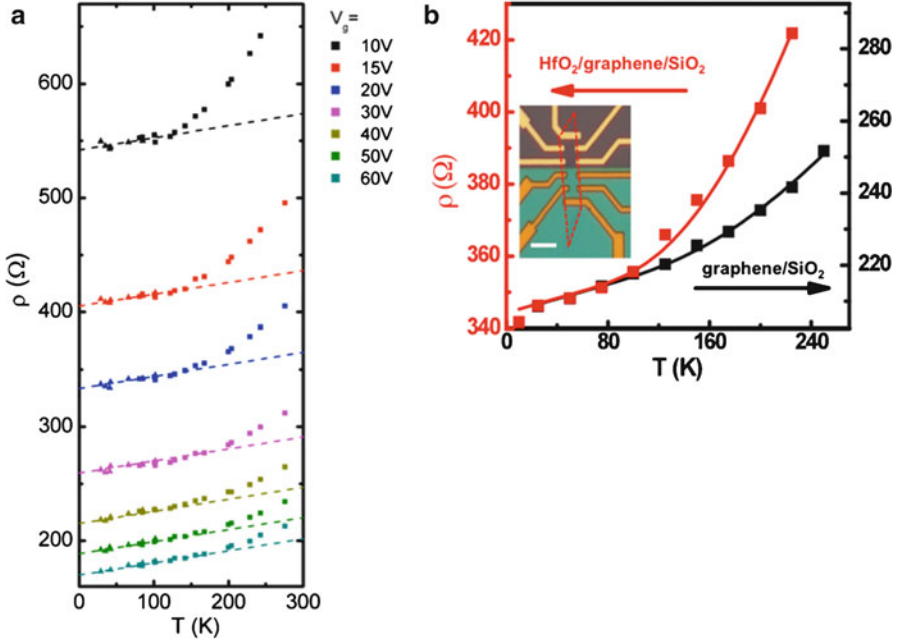


Fig. 2.4 The temperature-dependent resistivity of graphene. (a) Resistivity of a graphene on SiO_2 sample as a function of temperature and at different backgate voltages (Adapted from [16]). (b) Resistivity of a graphene on SiO_2 sample covered by a thin film of HfO_2 in the bottom half of the device. $n = 3 \times 10^{12}/\text{cm}^2$. The scale bar is 5 μm . Resistivity in the HfO_2 -covered portion exhibits a sharper rise with temperature due to the additional contribution of ROP scattering from the HfO_2 overlayer (Adapted from Ref. [17])

Unlike a silicon inversion layer, a graphene sheet has two surfaces. Device applications often require a local top gate, adding another gate oxide layer into the picture. As one might expect, this introduces more ROP scattering. The situation of a half-covered $\text{HfO}_2/\text{graphene}/\text{SiO}_2$ sandwich structure was studied by Zou et al. [17] and shown in Fig. 2.4b, where the two oxide layers contribute distinct remote phonon modes but also screen each other. Overall, the soft modes in the HfO_2 overlayer dominate and impose another extrinsic mobility limit of approximately $2 \times 10^4 \text{ cm}^2/\text{Vs}$. These studies show that although the intrinsic mobility of graphene due to LA phonon scattering is high, an actual device is subject to additional extrinsic scattering sources, some of which cannot be completely eliminated if gating is required. Efforts can be made, however, to balance functionality and performance. The choice of the gate oxide will be an important consideration. Low- κ dielectrics, in general, have stiffer phonon modes and cause less ROP scattering. SiC, which is the substrate of epitaxially grown graphene, should have much less ROP scattering than SiO_2 . As the development of graphene transistors progresses, these issues will need to be examined carefully and factored into the design of future devices.

2.2.2 Disorder Scattering

All phonon scattering, whether intrinsic or remote, vanishes at the limit of $T = 0$. The mobility of current graphene devices, however, does not go to infinity but remains finite. In graphene exfoliated on SiO_2 substrates, μ is at best $20,000 \text{ cm}^2/\text{Vs}$. Suspension improves this number by an order of magnitude. Graphene grown on SiC or by CVD method typically has μ in the range of several thousands. Here, the focus is on the mechanisms of scattering in mechanically exfoliated graphene; a discussion of scattering in SiC and CVD grown graphene is presented in Sect. 2.2.4.

What extrinsic scattering mechanism(s) are responsible? This question has been a central concern of graphene researchers and one on which a consensus has yet to be reached. To address this issue, it is helpful to take a look at other well-known 2D systems, e.g., silicon inversion layers and modulation-doped GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ structures. In Si/ SiO_2 devices, both interface roughness and charges in the oxide layer or close to the Si- SiO_2 interface limit the low-temperature electron mobility to below $50,000 \text{ cm}^2/\text{Vs}$ [11, 20]. It is difficult to increase μ further because of the inherent structural discontinuity at the Si- SiO_2 interface and the resulting defect states and interface charges. This problem does not exist in GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ heterostructures, since the lattices of GaAs and AlGaAs match each other perfectly. There, μ is limited by ionized donors sitting quite a distance away ($\sim 100 \text{ \AA}$) from the 2D channel and consequently μ up to $3 \times 10^7 \text{ cm}^2/\text{Vs}$ has been achieved. In order to accomplish this feat, the sources used for the molecular beam epitaxy (MBE) growth have to be very pure so that scattering by impurities is minimized. From this analogy, several possible sources of scattering can be identified: Coulomb charges, interfacial roughness and lattice defects (impurities, vacancies).

The most commonly used substrate for graphene devices is a 300 nm SiO_2 supported by a layer of heavily doped Si, also acting as a back-gate. Since charges are brought into graphene via the field effect, the counter-ions situated 300 nm away from the graphene produce little scattering. That leaves the graphene- SiO_2 interface; it was seen before that the Si- SiO_2 interface is extremely important for silicon inversion layers. There are two aspects to the interface: roughness, since graphene conforms very well to the undulations of SiO_2 , and interfacial charges. Although graphene doesn't form chemical bonds with the SiO_2 surface, it is nonetheless subject to charge transfer and Coulomb scattering from the resulting ionized donors. In ambient conditions, the hydrated surface of silica is covered with silanol (Si-OH) and siloxane (Si-O-Si) groups and possibly multi-layers of water [21]. Molecular dynamics calculations have shown that the surface states of SiO_2 can transfer electrons to graphene, resulting in electron doping. This n-doping was revealed in measurements only after prolonged pumping in vacuum and at high temperatures [22] since it is often masked by additional p-doping from H_2O and O_2 molecules physically adsorbed on the graphene sheet. The surface of SiO_2 also supports complex chemical reactions. Similar to carbon nanotubes, graphene devices supported on SiO_2 show pronounced hysteresis, pointing to charge traps involving surface-bound water molecules [23, 24]. Although the details of these

scenarios remain to be fully understood, it seems very likely that interfacial charges are present in graphene on SiO₂ devices and constitute a main source of scattering.

Quantitatively, the process of Coulomb impurity scattering in graphene and other 2DEGs is well understood within the framework of a self-consistent Boltzmann kinetic theory for diffusive transport [25–28]. In graphene, the 2D sheet conductance $\sigma = 2e^2/h (k_F l)$ and the mean free path $l = v_F \tau_t$. τ_t is the transport scattering time, given by:

$$\frac{1}{\tau_t} = n_{\text{imp}} \int_0^\pi Q(\theta, k_F) (1 + \cos \theta) (1 - \cos \theta) d\theta \quad (2.6)$$

where $\theta = \theta_{\mathbf{k}\mathbf{k}'}$ is the angle between the initial and final wave vector $\mathbf{k}$ and $\mathbf{k}'$, n_{imp} is the Coulomb impurity density and $Q(\theta, k_F)$ is the matrix element of the screened Coulomb scattering potential between an electron and a charged impurity. The factor $(1 + \cos \theta)$ is unique to graphene, resulting from pseudo-spin conservation: it suppresses 180° backscattering. The factor $(1 - \cos \theta)$ reduces the impact of small-angle scattering. Equation (2.6) shows that τ_t is inversely proportional to n_{imp} , but also depends on the carrier density. Detailed calculations show that τ_t scales with $\sqrt{n}$ and leads to a conductivity that is linearly proportional to the carrier density at densities sufficiently away from the Dirac point [25]:

$$\sigma = 20e^2/h(n/n_{\text{imp}}) \quad (2.7)$$

A mobility of 10,000 cm²/Vs thus corresponds to an impurity density of $\sim 5 \times 10^{11}/\text{cm}^2$ close to the interface. For impurities farther from the graphene plane, the spatial variation of their scattering potential is smaller; this corresponds to a small Fourier component in momentum space and predominantly small-angle scattering, which results in an enhanced τ_t . Thus, the measurement of τ_t alone cannot distinguish a higher impurity density sitting far away from a lower impurity density sitting nearby; another probe must be used. The single-particle momentum relaxation time, or quantum scattering time τ_q , is such a probe. Unlike τ_t , which represents the time it takes an electron to be backscattered, τ_q represents the time interval between two successive collisions, independent of the scattering angle. Taking the weight factor $(1 - \cos \theta)$ out of τ_t , an expression for τ_q is obtained:

$$\frac{1}{\tau_q} = n_{\text{imp}} \int_0^\pi Q(\theta, k_F) (1 + \cos \theta) d\theta \quad (2.8)$$

The ratio τ_t/τ_q of the two scattering times carries information about the scattering angle. A large ratio indicates the dominance of small-angle scattering and consequently Coulomb charges far from the 2D channel. A small ratio suggests that charged impurities are nearby and/or the scattering is dominated by short-ranged

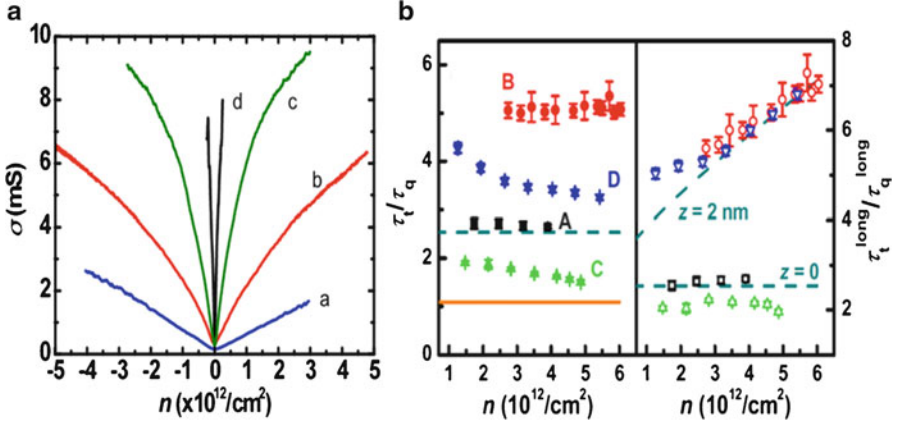


Fig. 2.5 The density-dependent conductivity of graphene and the ratio of the two scattering times. (a) The conductivity vs carrier density (electrons are positive) of graphene on SiO_2 (traces a and b) and on h-BN (trace c) and suspended (trace d). The field effect mobility is 4,400, 14,500, 60,000 and 230,000 cm^2/Vs in samples a–d respectively. Traces a and b are adapted from Ref. [29]. Trace c: courtesy of Cory Dean. Trace d: courtesy of Kirill Bolotin. (b) The ratio of τ_i/τ_q (left panel) and the long-ranged component of τ_i/τ_q (right panel) as a function of the carrier density (Reproduced with permission from [29]. © 2009 American Physical Society)

(i.e. δ -function-like) sources. The use of τ_i/τ_q is a well-known method in 2DEGs to probe the nature and location of scattering sources. For example, in modulation-doped $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ heterostructures, τ_i/τ_q routinely reaches several tens, since the ionized donors are far away. This ratio is close to 1 in silicon inversion layers, since both interfacial charges and surface roughness contribute roughly equally to τ_i and τ_q .

The above description of Coulomb impurity scattering compares favorably to experimental observations in graphene. A linear $\sigma(n)$ dependence is commonly observed, as shown in Fig. 2.5a. The relationship between carrier mobility and charged impurity density in (2.7) was verified in Ref. [30] by deliberately introducing doping and Coulomb scattering via the adsorption of K atoms onto the surface of graphene in ultra-high vacuum.

One aspect of experimental observations not captured by (2.7) is the sublinear behavior many devices exhibit at high carrier densities (Fig. 2.5a). It was shown that short-ranged scatterers that weakly interact with graphene, such as neutral adsorbates, give rise to a constant resistance ρ_s [31]. This constant ρ_s becomes increasingly important at high carrier densities and leads to the observed bending in the σ vs. n curve at large n . Combining the long and short-ranged sources, the total conductance of a graphene sheet can be described by:

$$\sigma_{\text{tot}}^{-1} = \sigma_{\text{long}}^{-1} + \rho_s; \quad \sigma_{\text{long}} = ne\mu_{\text{FE}} + \sigma_0 \quad (2.9)$$

Here, σ_0 is a small residue conductivity on the order of 10^{-4} S that is typically required to fit data. ρ_s is several tens to hundreds of Ω and the field effect mobility $\mu_{FE} = \frac{1}{e} \frac{d\sigma}{dn}$ ranges from several thousands up to 20,000 cm^2/Vs . The corresponding τ_t is typically tens to hundreds of fs and the mean free path l can be as long as several hundred nm.

Microscopically, what is the origin of the weakly interacting short-range scatterers and where are the charged impurities coming from? At the moment there is no clear answer to the first question. Progress has been made to address the second question by simultaneously measuring τ_t and τ_q and computing their ratio [29, 32]. Figure 2.5b plots the results of Hong et al. [29], where the authors separated the contributions of long and short-ranged scattering to τ_t and τ_q , and found that the Coulomb impurities responsible for τ_t^{long} and τ_q^{long} are within $z = 2$ nm of the graphene/SiO₂ interface. A subset of the data, together with the data of [32], points to the presence of charged impurities right at the graphene-SiO₂ interface ($z \approx 0$). These results are consistent with the surface states and surface chemistry of SiO₂ discussed earlier, but cannot directly reveal their microscopic origin. More surface studies are required to understand this important issue.

To increase the mobility further requires either a chemically inert substrate or the suspension of graphene. Both experiments have been reported. By using a crystalline BN substrate, Dean et al. reported μ_{FE} up to 60,000 cm^2/Vs [33]. Bolotin et al. and Du et al. achieved μ_{FE} of $2.3 \times 10^5 \text{ cm}^2/\text{Vs}$ in suspended devices [34, 35]. Both results are shown in Fig. 2.5a. These experiments unambiguously identify the substrate as the most important factor in limiting the carrier mobility in graphene.

The model of Coulomb impurities plus short-range scatterers has been successful in describing the majority of the conductivity measurements. A random distribution of Coulomb impurities can also naturally account for the appearance of spatial charge density inhomogeneity near the Dirac point—electron-hole puddles—revealed in STM measurements [36, 37]. The observed density variations have a characteristic length scale of 10–20 nm and a typical magnitude of Δn of a few $10^{11}/\text{cm}^2$. Both characteristics are consistent with arising from the Coulomb impurity density of 10^{11} – $10^{12}/\text{cm}^2$ given by carrier mobility in current devices. The coexistence of electrons and holes renders the intrinsic Dirac point physics, such as the presence of a minimum conductivity [3], inaccessible in these devices.

Lattice defects can also scatter carriers in graphene. This effect should be more pronounced in synthesized graphene (*i.e.* CVD-grown or SiC-derived). On graphene sheets exfoliated from high-quality graphite crystals, STM studies have revealed nearly perfect lattices with an estimated defect density of less than [38] $1 \times 10^8/\text{cm}^2$. Vacancies and chemisorbed adatoms/molecular groups produce a particular type of atomic defects called midgap states or resonant scatterers. These couple strongly to the electronic states of graphene and scatter electrons more efficiently than Coulomb charges [39, 40]. Although they are very short-ranged, their contribution to resistivity cannot be described by a constant ρ_s as was the case for weakly interacting short-ranged scatterers, but is given by: [39]

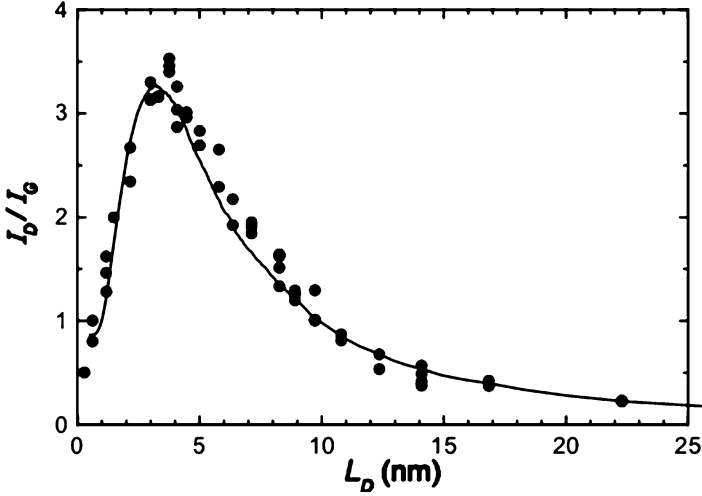


Fig. 2.6 The normalized intensity of the Raman D band vs. the defect density. L_D is the average distance between defects (Adapted from [44])

$$\sigma_d = ne\mu_d = \frac{2e^2}{\pi h} \frac{n}{n_d} \ln^2(k_F R_0) \quad (2.10)$$

where n_d is the midgap state density and R_0 the radius of the interaction potential, typically a few Å. Equation (2.10) produces a roughly linear $\sigma(n)$ relation with sublinear bending at high densities due to the $\ln^2(k_F R_0)$ term. The shape of the curve resembles the combined contributions of Coulomb impurities and weak short-ranged scatterers that is shown in Fig. 2.5a.

Several groups have studied the effect of midgap scattering on mobility by creating vacancies through ion irradiation [41] or by adding chemisorbed hydrogen [42] or fluorine atoms [43]. Chen et al. [41] demonstrates the mobility degradation from midgap state scattering using sequential increments of ion dosage. Luccese et al. [44] showed that the Raman intensity of the D band (normalized to the G band) is proportional to the defect density in the low-defect-density range. The relationship between n_d and I_D/I_G was calibrated by comparing STM and Raman data. As shown in Fig. 2.6, $I_D/I_G \sim 1$ corresponds to a vacancy density of $n_d \sim 1 \times 10^{12}/\text{cm}^2$. I_D/I_G becomes highly nonlinear and non-monotonic for I_D/I_G greater than 2 as defects start to coalesce [44]. Chen et al. [41] and Ni et al. [42] studied the evolution of $1/\mu$ vs ion dosage [41] or I_D/I_G [42] as defects were deliberately added to graphene. Both find a linear relationship between $1/\mu$ and n_d , in agreement with (2.10). The slope of $1/\mu$ vs n_d varies from 1.2 to 6.7×10^{-15} Vs in Ref [42], converting I_D/I_G to n_d using Ref. [44]. In Ref. [41], this slope is found to be 7.9 and 9.3×10^{-16} Vs. Although small differences may come from the different type of defects studied, the reason behind this large spread is unclear.

Interestingly, graphene sheets exfoliated from graphite crystals without any intentional defect addition show a small I_D/I_G ratio of about 0.01. The origin of this small D band is not known at the moment. As discussed earlier, the natural defect density of exfoliated graphene is a factor of 100 too small to account for this D band. Exposure to radiation and lithographic processes could potentially increase the defect density, although studies have not been done to verify this hypothesis. If the D band in untreated devices also comes from atomic defects, this would imply $n_d \sim 1 \times 10^{10}/\text{cm}^2$ and the slope of $1/\mu$ vs n_d can be used to estimate its effect on mobility. The estimated μ_d would vary from 15,000 to 130,000 cm^2/Vs according to the slopes obtained in Ref. [41] and Ref. [42]. Thus, the contribution of midgap state scattering towards the mobility ceiling $\mu_{\text{total}} \sim 20,000 \text{ cm}^2/\text{Vs}$ observed in all devices remains ambiguous. It is clear, however, atomic defects *alone* cannot account for the existing experimental observations. For example, midgap scattering produces a τ_i/τ_q ratio of less [32] than 2, which is inconsistent with data from several devices shown in Fig. 2.5b [29]. It is also difficult to see how atomic defects of density close to $1 \times 10^{10}/\text{cm}^2$ can produce the characteristics of electron–hole puddles observed in STM experiments [36, 37]. Midgap state scattering is more likely to play a significant role in synthesized graphene, where the lattice defect density is higher. Equation (2.10) provides a useful estimate of its magnitude.

The remarkable mobility increase obtained on BN substrates: $\mu_{\text{total}} = 60,000 \text{ cm}^2/\text{Vs}$ [33] clearly highlights the critical role of the substrate. What is the key to the success of the BN substrate? Chemical inertness? The absence of surface dangling bonds and functional groups certainly represents a huge improvement over the graphene-SiO₂ interface. Or perhaps it is the atomic flatness? The role of surface roughness—ripples—in the graphene sheet is briefly discussed next. This is a developing story as both theory and experiments [45–47] continue to make progress.

Free-standing graphene shows ripple height on the order of 1 nm in transmission electron microscope (TEM) measurements [48]. Although an interesting problem of its own, this situation is not discussed here but rather the focus is on substrate-supported—especially SiO₂-supported—graphene, which is more relevant for nanoelectronics applications. A graphene sheet conforms to the morphology of a rough surface to maximize surface adhesion. To what degree the features of a SiO₂ surface are faithfully followed is a trade off between the adhesion energy and the cost of elastic energy due to the curvature of the rippled sheet. Conforming to a sharp feature on the surface produces a large curvature and raises the elastic energy cost; in this case a detachment may be more energetically favorable. It was shown recently [47] that although a little smoother, the surface roughness of graphene highly correlates with that of the SiO₂ surface underneath, following features with radii of curvature up to $\sim 1 \text{ nm}^{-1}$ (99.9% of the SiO₂ surface roughness satisfies this condition). On mica substrates, graphene sheets are atomically flat with a roughness of less than 25 pm [49]. Thus the substrate appears to leave little room for the graphene sheet to ripple freely on its own, although this possibility cannot be completely ruled out.

The topographic correlation between graphene and the substrate underneath provides interesting opportunities to manipulate the mechanical properties of the

graphene sheet, some of which are already being exploited for applications [50]. But how does the curvature of graphene impact its transport properties? Conceptually, curvature changes the carbon-carbon bond lengths locally and leads to a variation of the neighboring hopping integrals, which is equivalent to a fictitious, random magnetic field that deflects electrons and produces scattering [45]. Its carrier density dependence is predicted to follow $\sigma_r \propto n^{2H-1}$, for $2H > 1$ and $\ln^2(k_F a)$ for $2H = 1$, where $a = 2.46 \text{ \AA}$. $2H$ is the exponent of the surface height-distance correlation function [45] $\langle [h(r) - h(0)]^2 \rangle \propto r^{2H}$. A condition of $2H = 2$ can potentially give a linear $\sigma(n)$ behavior observed experimentally. Measurements of the exponent $2H$ are inconclusive at the moment and in any case, a quantitative evaluation of the magnitude of the ripple scattering will be difficult because of the qualitative nature of the theory and the experimental challenges of controlling the surface roughness of a graphene sheet and other scattering mechanisms separately. Much work remains to be done before the question of “how much does ripple scattering contribute to the resistivity?” can be answered.

This section ends with a brief discussion of chemical doping. Graphene has a large surface-to-volume ratio and its surface is easily accessible. This exposure offers an effective pathway to develop chemical and biological sensors for toxic gases and biomolecules; high-sensitivity detection of NO_2 has been demonstrated [51]. Adsorbates also provide a means alternative to gating for modifying the carrier density and profile to control graphene’s transport properties [52]. On the other hand, to understand and eliminate unintentional chemical doping is important to the performance and stability of many graphene devices. Here the focus is on dopants physically adsorbed on the graphene surface; since graphene is chemically inert, this is true for most dopants. Doping graphene through lattice substitutions [53] is discussed in Chap. 3. The main mechanism for detecting a variety of physical adsorbates on graphene has been through a shift of the Fermi level (or equivalently the change of the Hall coefficient) in a gated device. This “doping” effect, however, appears to have multiple origins. Experiments have shown that alkaline and transition metals dope graphene through direct charge transfer. As a result, carriers in graphene are scattered by the ionized donors and the carrier mobility decreases with increasing doping, following approximately the Coulomb impurity model [30, 54]. With molecular adsorbates, the situation is more complicated. H_2O is widely believed to be responsible for the ubiquitous p-doping observed in graphene devices stored in ambient conditions. This doping can be removed after vacuum pumping and/or thermal annealing. NO_2 molecules also provide p-doping while NH_3 molecules produce n-doping. Whether these molecules transfer charge directly to graphene is not clear. Density functional theory (DFT) calculations have suggested this explanation for open-shelled molecules such as NO_2 [55, 56]; this mechanism is unlikely to apply to close-shelled molecules such as H_2O and NH_3 , where the HOMO and LUMO levels of the molecule are far away from the Fermi level of graphene. Indirect charge transfer from other sources, such as the SiO_2 surface states, due to the graphene work function change induced by the dipolar adsorbate layer, was also proposed [40]. However, charge transfer from a *nearby* source faces

a general difficulty of accounting for an important experimental observation, *i.e.* all three dipolar adsorbates (H_2O , NO_2 , NH_3) appear to be able to dope graphene to at least a few $10^{12}/\text{cm}^2$ with very little effect on mobility [51, 52]. These results differ from the doping effect of elemental metals and are at odds with Coulomb scattering resulting from ionized donors nearby; ionized donors of a density of $2 \times 10^{12}/\text{cm}^2$ would give rise to a mobility of $2,500 \text{ cm}^2/\text{Vs}$ if they are on the graphene surface; even if they are separated from the graphene sheet by a 2 nm layer of PMMA residue (which is common in lithographically processed devices) they should still give rise to a mobility of $6,000 \text{ cm}^2/\text{Vs}$ (see Ref. [29] for how these values are calculated), large enough to be observed in Refs. [51, 52]. But this is not the case experimentally. One possible explanation is that perhaps molecules deposited at room temperature form clusters, where Coulomb scattering is reduced. Indeed, evidence of clustering and reduced scattering has been reported in Ref. [54] using transition metals. However, even in the most weakly scattered case there, doping of $2 \times 10^{12}/\text{cm}^2$ still leads to a mobility of $5,000 \text{ cm}^2/\text{Vs}$. Can clustering explain the lack of mobility degradation and to what degree do molecules have to cluster to cause a negligible change in device characteristics? These questions remain unanswered. The above discussions suggest that although chemical doping by molecules is widely observed, the doping mechanisms are not entirely understood.

In addition to metals and gas molecules, many organics such as F4-TCNQ [57] and 4-amino-TEMPO [58] and inorganic molecules such as HNO_3 [59] are found to dope graphene as well. This route is particularly compatible with thin-film processing techniques and could be very useful for integrating graphene into organic photovoltaics and flexible electronics [59–61].

2.2.3 Transport in Nanoribbons

This section gives a brief overview of transport in graphene nanoribbons. GNRs are a potential solution for using graphene in digital electronics since they can have a band gap. The production and study of GNRs have been very active areas of graphene research since the birth of the field. As discussed in Sect. 2.1.2, the mechanism of band gap opening in GNRs is quantum confinement. The size of the gap E_g is inversely proportional to the width W and is estimated to be $\sim 2 \text{ eV}/W$ (nm). To open a sizeable gap, sub-10 nm GNRs are required. This is a challenge technically. In recent years, many approaches have been used to produce GNRs; each has its pros and cons and a technically viable solution has yet to emerge. State-of-the-art electron-beam lithography has produced GNRs with widths below 20 nm [62]. This process is compatible with large-scale patterning but faces challenges from edge roughness. CVD growth can produce bulk quantities of crystalline GNRs with varying width [63]. Chemical exfoliation of graphite has demonstrated sub-10 nm GNRs with smooth edges but the distribution of the width is difficult to control [64]. Unzipping carbon nanotubes using an oxidative process [65] or plasma etching [66] provides another route to generate sub-10 nm ribbons.

A bottom-up assembly process has demonstrated the synthesis of a-few-hexagon-wide GNRs with well-defined edges [67]. Presently, chemistry-assisted processes have an advantage in producing narrow GNRs but need to address the issues of width uniformity, device integration and scaling for practical device applications.

Despite these challenges, much progress has been made in understanding electronic transport in GNRs. Although metallic GNRs exist theoretically, all GNR devices so far are found to be semiconducting. This is because the edge state of the zigzag GNR and the metallic state of certain armchair GNRs do not survive even small edge disorder, which is always present in current GNRs. In this section, the focus is on a few aspects of semiconducting GNRs that are most relevant for nanoelectronics—the size of its band gap and its characteristics in transistors and interconnects.

1. The size of the band gap

To address this issue properly, the meaning of “gap” needs to be defined. Semiconducting GNRs possess a spectrum gap E_g but this is not necessarily what’s measured in transport experiments. Backgated GNR devices behave like bipolar transistors; the differential conductance dI/dV_{sd} at small source-drain bias V_{sd} becomes nearly zero (the “off” state) for a range of V_g near the charge neutrality point; this range ΔV_g is referred to as the “transport gap,” beyond which the conductivity of the device rises rapidly (the “on” state). For a $W = 30$ nm GNR on 300 nm SiO_2 , ΔV_g is roughly a few tens of volts and translates into a Fermi level span Δ_m of a few hundred meV [68–70]. This energy scale can be empirically fit to $\alpha/(W - W_0)$, where W_0 represents an inactive width, partly attributed to the discrepancy between the widths of the etching mask and the actual ribbon and partly attributed to edge disorder induced localization/inactivation [71, 72]. Han et al. [71] found $\alpha \sim 5$ eVnm and $W_0 = 12$ nm. The transport gap does not depend on the length of the ribbon. Experiments also measure a “source-drain gap” ΔV_b by increasing the source drain bias V_{sd} and detecting a sharp rise of I_{sd} inside the transport gap (see Fig. 2.7a, b). ΔV_b can be a few tens of mV and increases with increasing ribbon length L . It also tends to be smaller in wider ribbons. In addition to Δ_m and ΔV_b , there are two more energy scales, namely an activation energy E_a which describes the temperature dependence of dI/dV_{sd} in the transport gap as $dI/dV_{sd} \propto \exp(-E_a/2k_B T)$, and a $k_B T^*$ where dI/dV_{sd} changes from the activated behavior to variable-range hopping in 1D, i.e. $\exp[-(T_0/T)^{1/2}]$ for $T < T^*$. E_a is up to a few tens meV and $k_B T^*$ is an order of magnitude smaller than E_a (see Fig. 2.7c) [68].

In an ideal semiconductor, it is expected that $E_g = \Delta_m = \Delta V_b = E_a$ and T^* is non-existent. Why is the story so complicated in GNRs? The complication arises from disorder. There are two types of disorder in GNRs. Similar to planar sheets, GNRs prepared on SiO_2 substrates suffer from charged impurity scattering and the resulting Coulomb potential fluctuation Φ_d . The variance $\Delta\Phi_d$ ranges from 15 meV to 77 meV in scanned probe measurements [36, 37, 73]. The typical lateral size of the resulting electron-hole puddles is about 10–20 nm. Together with the quantum confinement gap of the GNR, these puddles become isolated quantum dots. For a GNR to conduct sufficiently, a majority of the puddles have to be filled or emptied by sweeping the gate potential; the range of V_g required to do that may be

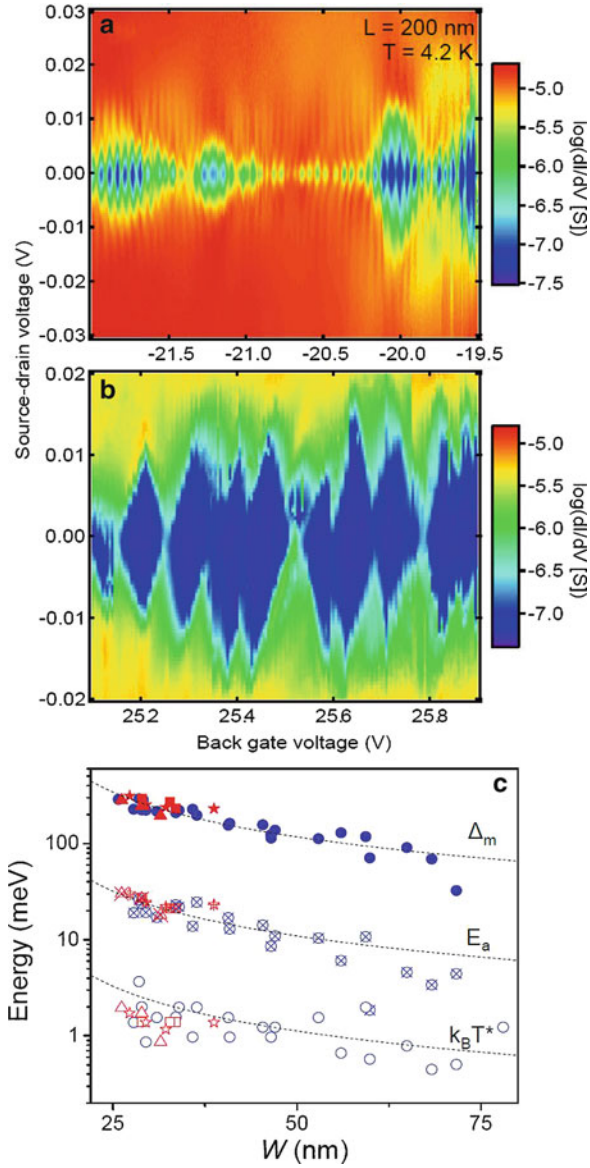


Fig. 2.7 Transport characteristics of graphene nanoribbons (a) and (b) false color plot of differential conductance as a function of the backgate voltage and the source-drain voltage. The ribbon is 30 nm wide and 200 nm long. Coulomb blockade and oscillations are apparent (Reproduced with permission from [69]). (c) Various energy scales of long GNRs as a function of the ribbon width (Reproduced with permission from [68]. © 2010 American Physical Society)

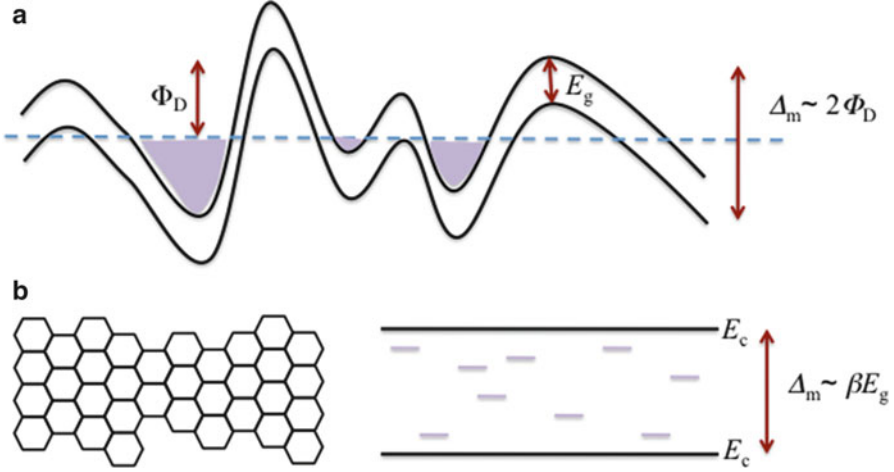


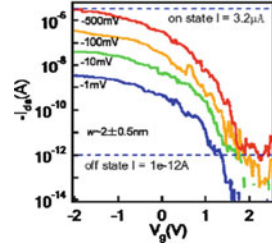
Fig. 2.8 Disorders in graphene nanoribbons. (a) Quantum dots produced by Coulomb potential fluctuations. (b) Anderson localized states produced by edge disorder

interpreted as the transport gap. ΔV_g is therefore dominated by the amplitude of the disorder potential $\sim 2\Phi_d$. This situation is illustrated in Fig. 2.8a. Sometimes severe line-edge roughness could also lead to local constrictions that form quantum dots [74].

In addition, even slight edge disorder (width variation, missing atoms, functionalization) can produce localized states near the edge (hereafter referred to as Anderson states to differentiate from quantum dots produced by variations in the Coulomb potential), which penetrate into the interior of the ribbon to block conduction. These Anderson states appear inside and beyond the pristine band gap E_g and effectively create quasi-mobility edges E_c as illustrated in Fig. 2.8b. Conduction inside the band of Anderson states is low enough to be considered inside a transport gap. In this scenario, ΔV_g is related to the edge disorder. Several calculations have found the energy range of the Anderson states mimics the experimental width dependence of the transport gap, i.e., $\Delta_m = \alpha/(W - W_0)$ with α being a few eVnm [72, 75, 76].

Examine the various energy scales involved for a $W = 30$ nm GNR: the pristine band gap E_g is about 60 meV; the Coulomb disorder amplitude $2\Phi_d$ can range from 30 to 160 meV; and the energy range of the Anderson states is on the order of 100 meV. These forms of disorder are all unavoidable in practical devices and their energy scales are close enough that most likely they all contribute to the conduction of GNRs. In short GNRs, quantum dots tend to be the most prominent type of localized states and consequently Coulomb blockade and Coulomb oscillations are observed [69, 70]. Coulomb impurities are subject to rearrangement via annealing, the effect of which has been experimentally shown [69]. In longer ribbons, the behavior of the Anderson states manifests in the width dependence of the transport gap [68]. In both scenarios, because the transport gap is much larger than the $k_B T$

Fig. 2.9 The on/off ratio in GNR transistors. The source-drain current as a function of the gate voltage in a 2 nm wide GNR showing high on/off ratio of 106. (Reproduced with permission from [83]. © 2008 American Physical Society)



range of the experiments, the measured temperature dependence of the conductance in [68] does not probe the transport gap but instead probes the energy cost to hop between neighboring localized states, whether they be quantum dots or Anderson states. The observed E_a is consistent with the hopping energy between Anderson states [77] but is also compatible with that between neighboring quantum dots [78], and may include contributions of Coulomb charging energy [77] as well. The transition from nearest neighbor hopping of the form $\exp(-E_a/2k_B T)$ to variable-range hopping of the form $\exp[-(T_0/T)^{1/2}]$ at lower temperature, as demonstrated experimentally [68], follows from the general behavior of a percolation network. Another manifestation of this localization physics is seen in gapped bilayer graphene, where the combination of a gate-induced band gap and Coulomb disorder give rise to similar experimental observations [79–81].

2. Transistor characteristics

Despite the complications of disorder, GNRs can function as bipolar transistors. As the gate voltage V_g sweeps beyond the transport gapped region, the conduction turns on. Near room temperature, the current on/off ratio is less than 10 in lithographically produced GNRs ($W > 20$ nm) [71, 82] but can reach 10^6 in chemically exfoliated ultra-narrow ribbons ($W = 2$ nm) with a subthreshold slope of 210 mV/decade [83] Fig. 2.9. The low on/off ratio in etched GNRs is not surprising since the conduction inside the transport gap is given by nearest neighbor hopping $\exp(-E_a/2k_B T)$, where E_a is only a few tens of meV. The high on/off ratio observed in Ref. [83] may result from a combination of smaller width, smoother edges and shorter channel length of the ribbon. These high-performing GNR devices demonstrate the potential of GNR transistors once disorder is under control.

It was shown that the etching process used to produce GNRs reduces the carrier mobility [62] in ribbons narrower than 60 nm. At $W = 20$ nm, the carrier mobility drops to several hundreds of cm^2/Vs . Line edge roughness, which produces band-edge fluctuations and consequently carrier scattering, is primarily responsible for this degradation. The impact of line edge roughness (a few nm in lithographically produced ribbons) increases in narrower ribbons, where the conduction becomes more one-dimensional [84, 85]. Empirically, the mobility limited by line-edge roughness μ_{LER} scales with the ribbon width W as $W^{4.3}$, producing a sharp drop of mobility with decreasing width [62]. This is further discussed in Chap. 3.

Both carbon nanotubes and 2D graphene sheets support breakdown current densities exceeding $1 \times 10^8 \text{ A/cm}^2$. This excellent property is preserved in GNRs. Current GNRs devices show a breakdown current density of up to $1 \times 10^9 \text{ A/cm}^2$, about a factor of 1,000 higher than copper [83, 86]. The superb current-carry capability makes GNRs a promising candidate for interconnect applications.

To summarize, at the current stage, disorder dominates the transport properties of GNRs; the various gaps experimentally measured have little to do with the true band gap arising from quantum confinement. As a transistor or interconnect, an ideal GNR has many desirable key characteristics, including high current on/off ratio, high carrier mobility and high current carrying capacity. But this anticipated high performance is currently heavily degraded by disorder. Obtaining GNRs with atomically smooth edges will be a crucial step in improving its electronic properties and fulfilling its promise in digital electronics.

2.2.4 Transport in SiC-Grown and CVD-Grown Graphene

So far the example of graphene mechanically exfoliated onto a substrate, in particular SiO_2 , has been used to discuss transport properties. Many device applications demand a high-throughput, scalable approach. Large-area synthesis of graphene has been an active area of the field. Presently, graphene can be epitaxially grown on SiC substrates [87] and on transition metals through chemical vapor deposition (CVD) [88, 89]. These subjects will be discussed in Chaps. 6 and 7 in detail. In this section, some unique aspects of these synthesized materials are discussed in the context of the scattering mechanisms. Synthesis of epitaxial graphene (EG) on SiC substrates uses high temperatures ($1,200\text{--}1,800^\circ\text{C}$) to sublimate Si atoms from the surface. The growth can be initiated on either the Si face, termed (0001), or the C face, termed (000 $\bar{1}$). It is comparatively easier to control the number of graphene layers grown on the Si face and obtain single-layer graphene growing continuously over long strips of atomically flat terraces of SiC several microns in width [90]. The step edges likely do not have a significant impact on transport [91]. Experiments show that graphene grown on the Si face exhibits the characteristic Dirac cone dispersion [2] and the resulting half-integer quantum Hall sequence in magneto-transport [91, 92]. Growth on the C face tends to yield multi-layer sheets with each layer rotated from its neighbors by roughly 0° or 30° degrees. The rotation effectively decouples the layers so that the system can be viewed for many purposes as independent graphene sheets in parallel, instead of graphite. These growth characteristics have important consequences on the transport properties.

Regardless of which surface of the SiC substrate EG is grown on, the work function difference between SiC and graphene induces a dipole field at the interface and consequently graphene is electron-doped to $10^{12}\text{--}10^{13}/\text{cm}^2$. The ionized donors, because of their vicinity to the graphene sheet, are an important source of charged impurity scattering. The reader may recall that a random distribution of

charged impurities of a density $5 \times 10^{11}/\text{cm}^2$ adjacent to the graphene sheet limits the carrier mobility to approximately $10,000 \text{ cm}^2/\text{Vs}$. Single-layer graphene grown on the Si face of SiC exhibits μ up to a few thousands cm^2/Vs [91, 92]. Charged impurity scattering plays a central role here. Recently, Reidl et al. showed that a layer of hydrogen atoms intercalated between the Si surface and the buffer layer can saturate the dangling bonds of the Si surface, yielding quasi-free standing graphene [93]. This passivation also removes the electron doping effect of the substrate and can potentially yield higher quality devices with a larger density tuning range.

In multi-layer graphene grown on the C face of the SiC substrate, an electrical current goes through all layers but is dominated by the bottom layer, which is heavily electron doped by the substrate. The carrier density quickly decreases in the layers above, due to screening. As a result of this density gradient, the topmost layer only has a low carrier density in the range of $10^9/\text{cm}^2$ [94, 95]. Screened by the layers underneath, the topmost layer exhibits the electronic signatures of a high-quality single-layer graphene. Both STM and infrared absorption studies have shown the quantum scattering time τ_q of this layer reaches several hundred fs [94, 95], which corresponds to a quantum mobility $\mu_q = e\tau_q/m^*$ of above $200,000 \text{ cm}^2/\text{Vs}$ at such low carrier densities. This value is comparable to that of suspended graphene discussed earlier. Recently, single-layer growth on the C face has also been achieved [96].

Raman spectra of EG grown on the Si face show variable D band intensity I_D/I_G from [90, 97] <0.05 to 0.2 . The D band can originate from lattice defects or grain boundaries. As discussed in Sect. 2.2.2, lattice defects scatter electrons in graphene according to (2.10). An I_D/I_G on the order of 0.1 due to isolated atomic defects may give rise to mobility in the range of $1,000$ – $10,000 \text{ cm}^2/\text{Vs}$, which is non-negligible. Grain boundaries connect crystalline domains of different lattice orientations. In the simplest case of straight, periodic grain boundaries, electrons incident upon a grain boundary may be fully transmitted or reflected depending on the indices of the two domains, similar to the formation of gaps in carbon nanotubes [98]. Detailed studies of grain boundaries on EG are scant [94] but recent studies on CVD-grown graphene reveal irregular, aperiodic grain boundaries [99]. Understanding transport through such complex boundaries requires more modeling. This topic will be revisited when discussing CVD-grown graphene.

In Sect. 2.2.1, the contribution to the temperature-dependent resistivity from LA phonon scattering and remote oxide phonon (ROP) scattering (due to the adjacent substrates and top-gate oxides) was discussed. The intrinsic LA phonon scattering should remain the same for EG. The amplitude of the ROP scattering in a graphene/6H-SiC interface can be calculated using silicon carbide's static and optical dielectric constants of $\epsilon_0 = 6.5$, $\epsilon_\infty = 9.7$ and its surface optical phonon frequency of $\hbar\omega_{SO} = 116 \text{ meV}$ [100], following methods outlined in Ref. [17]. These estimates show that ROP scattering from the SiC interface leads to a room temperature mobility of $360,000 \text{ cm}^2/\text{Vs}$. This is a negligible contribution compared to other scattering sources and makes SiC a better substrate than SiO_2 from the viewpoint of phonon resistance. However, a top gate is necessary to control carrier densities in EG grown on SiC and large arrays of transistors with Al_2O_3 or HfO_2 top-gate oxide

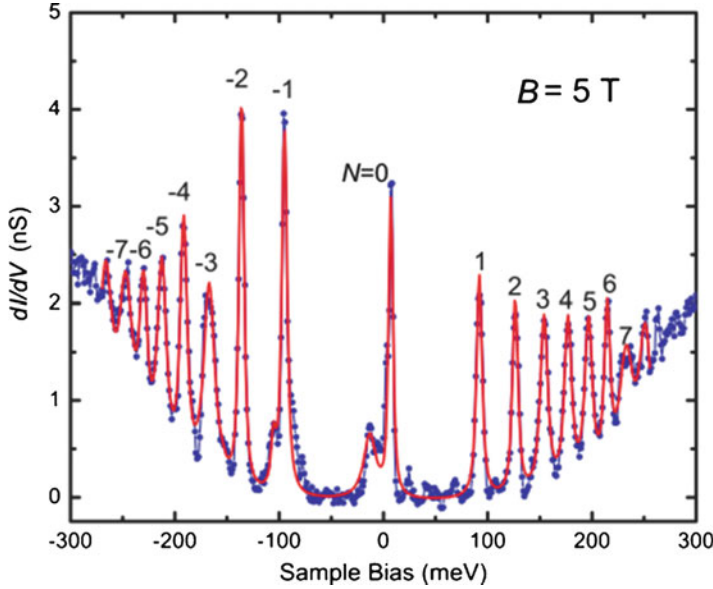


Fig. 2.10 Probing the Landau level quantization of EG grown on the C face of 4H-SiC with STM. Tunneling differential conductance as a function of the sample bias. The indices mark the Landau levels corresponding to a Dirac fermion dispersion (Adapted from [94])

have indeed been fabricated (see Chap. 9 for more details). The ROP scattering will be dominated by the top-gate oxide and it is important to establish the phonon-related performance limits of these devices.

Next, the electrical transport properties of CVD-grown graphene are briefly discussed. This method of synthesis began only a few years ago [88, 89] but has shown great promise in yielding very large-area and high-quality graphene sheets. Chapter 7 gives a more detailed account of this subject. The discussion here is focused on graphene synthesized on copper substrates, which is predominantly single-layer with a small fraction of multi-layer islands [89]. Devices are made by transferring grown graphene sheets to a $\text{SiO}_2/\text{doped Si}$ substrate. The best devices have a quality comparable to that of exfoliated graphene (carrier mobility up to $9,000 \text{ cm}^2/\text{Vs}$) and show well-developed half-integer quantum Hall effect but μ of the majority of the CVD grown graphene samples is on the order of $1,000 \text{ cm}^2/\text{Vs}$, lower than that of exfoliated graphene [59, 89, 99, 101]. Since devices are tested on the same type of substrate ($\text{SiO}_2/\text{doped Si}$), the difference must come from the growth and transfer processes. By varying growth conditions, Hwang et al. [101] demonstrated a strong correlation between the carrier mobility and the intensity of the Raman D band: an increase in D band intensity correlates to a degradation of mobility. As the Raman D band signal can arise from lattice defects or grain boundaries, this study shows that a high defect and/or grain boundary density can cause mobility loss. The same study

also shows that even with a small I_D/I_G of less than 0.05, which is fairly common for CVD grown graphene, the carrier mobility is still less than $1,500 \text{ cm}^2/\text{Vs}$, pointing to the existence of other major scattering sources.

The experiments of Huang et al. [99], provided critical information on the growth morphology and transport characteristics of CVD-grown graphene. Combining atomically resolved scanning transmission electron microscopy and diffraction techniques, the authors mapped out the grains and grain boundaries of grown specimens and demonstrated that the grain size (ranging from a few hundred nm to more than a μm) depends on the purity of the copper substrate on which the graphene sheet is grown and also the method of growth. However, scanned electrostatic force microscopy also shows that grain boundary scattering does not play an important role in carrier transport, at least not at the level of μ of a few thousand cm^2/Vs . Independently, Li et al. [102], demonstrated a low-pressure growth procedure which can yield graphene grains up to 0.5 mm in size, but μ remains several thousand cm^2/Vs . The insensitivity of μ to the grain size appears puzzling first, but is actually easy to understand since the mean free path of the carriers, for *e.g.* at $n = 2 \times 10^{12}/\text{cm}^2$ and $\mu = 5,000 \text{ cm}^2/\text{Vs}$, is only 80 nm, which is much less than the grain size. As the mobility improves, crystal misorientations, defects and adsorbates associated with grain boundaries will eventually become limiting factors.

If not grain boundaries, what is responsible for the low carrier mobility in CVD-grown graphene? The answer probably lies in the contaminants acquired during growth and transfer. In [99], graphene grown on ultrapure copper (99.999%) exhibits a factor of 7 increase in mobility compared to graphene grown on lower purity copper (99.8%) (Fig. 2.11). This suggests that impurities in copper, which may have surfaced during the pre-growth annealing process, are likely to play a role. The process of transferring graphene onto a substrate involves solution etching (commonly FeCl_3) and usually solution removal of the PMMA stamp. Both processes leave residue on graphene. Cleaner growth and transfer may hold the key to yet higher quality CVD graphene production. The large size and freedom to work with any substrates give this synthesis route a unique advantage in pursuing a variety of applications.

2.3 High-Field Transport in Graphene Field Effect Transistors

In this section, the underlying physics of electrical transport in graphene field effect transistors (FETs) operated at high source-drain bias (transverse electric field) is discussed. Figure 2.12 plots the drain current I_d vs the source-drain bias V_{sd} at different top and back gate biases V_{tg} and V_{bg} in a dual-gated graphene FET [103]. At low bias V_{sd} , the drain current I_d is linearly proportional to V_{sd} . In this linear regime, the slopes of the I_d (V_{sd}) (I - V) curves represent the conductance of the device, which is proportional to the carrier density n and the mobility μ . At high bias, the I - V becomes highly non-linear and tends toward saturation. A high saturation velocity/current, together with a flat plateau (low output conductance) in the current saturated regime, makes graphene FETs promising for high-frequency linear

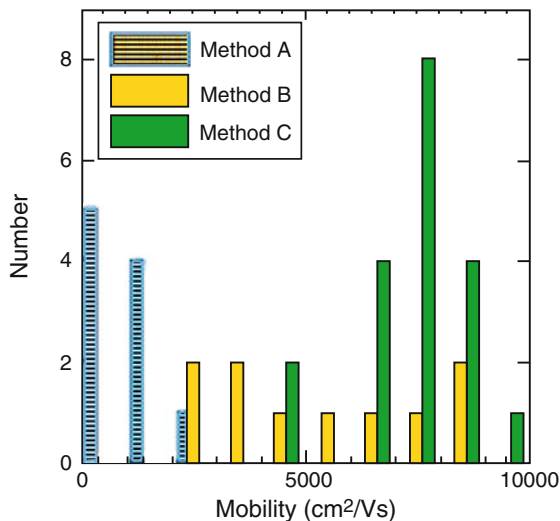


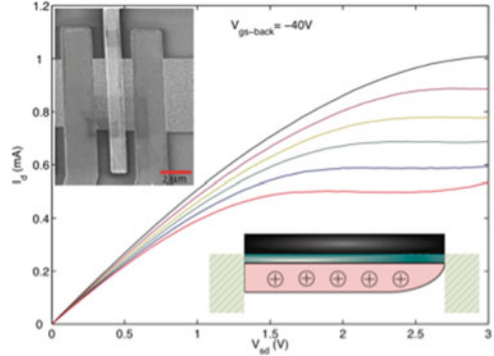
Fig. 2.11 Correlation between carrier mobility and growth method. *Method A*: growth condition similar to [89] on 99.8% pure copper foil. *Method B*: growth done in a rapid thermal tube furnace on 99.8% copper foil. *Method C*: the same growth condition as A but on 99.999% ultrapure copper foil (Adapted from [99])

amplifiers. A clear understanding of these aspects plays a crucial role in designing, modeling and optimizing the performance.

In the Drude model, an electron accelerates in an electric field E for a time τ_t , the transport scattering time, and achieves a momentum $m\mathbf{v} = eE\tau_t$, or equivalently a drift velocity $v = Ee\tau_t/m = \mu E$. The linear relationship between v and E translates into a linear I - V in the low-bias regime. At large electron drift velocity, inelastic collisions with phonons become increasingly important, causing the electron to lose momentum and energy. In addition, the Joule heat pumped into the device raises the electron temperature T_e and broadens the Fermi distribution. The Coulomb interaction among electrons and holes produce a drag, *i.e.* carriers of opposite sign flow in the same direction, leading to a small net current [104, 105]. These two effects together can eventually cause the electron drift velocity to reach a saturation value v_{sat} .

For single and dual-gated graphene FETs, several phonon channels participate in inelastic scattering. These include the LA and optical phonons of graphene (the LO mode at the Γ point with energy $\hbar\Omega = 196$ meV and the TO mode at the K point with energy $\hbar\Omega = 149$ meV [13]). Inelastic scattering by phonons dissipates heat from the electronic system to the graphene lattice, raising the lattice temperature T_L . The hot lattice is then cooled by the substrate and the metal contacts. Knowing the coupling strength to the various phonon modes allows the rate of momentum and energy loss and hence the electron drift velocity and temperature to be calculated

Fig. 2.12 I - V characteristics of a dual-gated graphene field effect transistor. *Upper inset:* SEM micrograph of such a device. Scale bar: 2 μm . *Lower inset:* schematics of the pinch-off condition (Adapted from [103])



and compared to experiments [104–108]. Calculations of the contributions from graphene phonons alone yield saturation velocities too low compared to experiments [106–108]; on the other hand, by including also the surface optical phonons of the adjacent substrate and top-gate oxide, DaSilva [107] et al. demonstrate excellent agreement between experiment and theory with no adjustable parameters (Fig. 2.13a). In addition, it was shown in [107, 109] that the direct emission of substrate optical phonons is the primary channel through which hot electrons in graphene transistors operating at high source-drain bias lose momentum and energy. This direct cooling mechanism lowers T_e and allows v_{sat} to reach higher values than it would otherwise. The saturated current density is in the range of a few $\text{mA}/\mu\text{m}$, and is approximately linear in n at high carrier densities (Fig. 2.13b). Calculations also show that both the density of Coulomb impurities (Fig. 2.13b) and the choice of substrate (Fig. 2.13c) have little effect on v_{sat} , although the velocity saturation occurs at lower bias in cleaner samples [107, 108].

It is instructive to compare the high-bias transport of graphene and metallic carbon nanotube FETs. The latter is well described by a simple model $I = \frac{V}{R_0 + V/I_{\text{sat}}}$ where R_0 is the small-bias resistance of the sample and I_{sat} the saturation current. At high bias, the current approaches $I_{\text{sat}} \sim 25 \mu\text{A}$ in not-so-short carbon nanotubes [110–112]. Expressed in terms of electron drift velocity, the above equation reads $v = \frac{\mu E}{1 + \mu E/v_{\text{sat}}}$. This model accurately describes the current saturation process if the emission of the relevant optical phonon can be viewed as instantaneous, i.e. the electron-phonon backscattering length l_{ph} is much shorter than the length required for the electron to accelerate in the electric field to reach the energy threshold of emitting this phonon, $l_{\Omega} = \hbar\Omega/eE$. In carbon nanotubes, l_{Ω} is a few hundred nm while l_{ph} is of order 10 nm. Therefore $l_{\text{ph}} \ll l_{\Omega}$ is satisfied [110, 112]. It follows from the Landauer formula that $I_{\text{sat}} = (4e/h)\hbar\Omega = 25\mu\text{A}$ with $\hbar\Omega = 160 \text{ meV}$ [110]. In graphene, a similar derivation would lead to $v_{\text{sat}}/v_F = \hbar\Omega/E_F$ [103], where $v_{\text{sat}} \propto 1/\sqrt{n}$. However, studies show that l_{ph} is not so short in graphene due to weaker electron-phonon coupling [106, 107] and therefore the instantaneous emission model does not apply and a full microscopic theory must be employed. A comparison to data in Fig. 2.13a shows that the instantaneous emission model

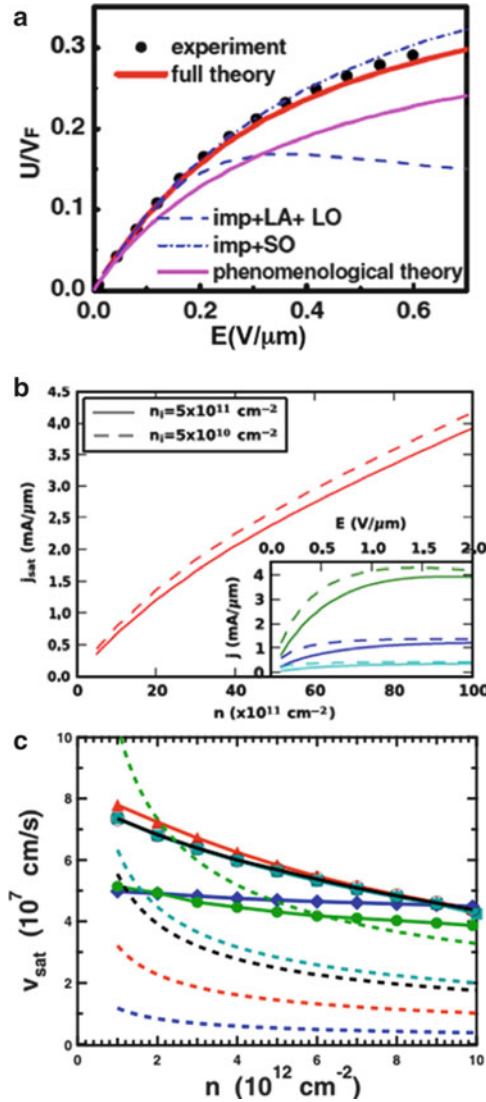


Fig. 2.13 The mechanism of current saturation in graphene transistors operated at high bias. (a) Measured and calculated drift velocity as a function of the source-drain electric field in a backgated graphene on SiO_2 device. The carrier density is $n = 2.1 \times 10^{12}/\text{cm}^2$. Data can only be explained by including the surface optical phonon of the SiO_2 substrate. (b) The saturation current density vs. the carrier density for two Coulomb impurity densities. The inset shows calculated I-V for three carrier densities (from top to bottom) $n = 1 \times 10^{13}/\text{cm}^2$, $2.0 \times 10^{12}/\text{cm}^2$ and $5 \times 10^{11}/\text{cm}^2$ respectively. The I-V curves saturate at lower electric field in cleaner samples (Reproduced with permission from [107]). (c) The saturation velocity as a function of carrier density for graphene on different substrates at room temperature: circles—intrinsic, black open circles—on BN, squares—on SiC, triangles—on SiO_2 , and diamonds—on HfO_2 . The dashed curves are predictions using the instantaneous emission model (Reproduced with permission from [108]. © 2010 American Physical Society)

underestimates the experimental current. In practice, an empirical and useful expression

$$v = \frac{\mu E}{\left[1 + (\mu E/v_{sat})^\beta\right]^{1/\beta}}$$

captures the I - V characteristics of silicon transistors very well, from which the saturation velocity can be obtained [113]. This approach has been used to analyze high-bias transport in graphene as well [114].

A saturation current density of a few mA/ μ m in a single graphene layer translates into a bulk current density exceeding 10^8 A/cm², which is extraordinary and advantageous in amplifier applications. It also highlights the critical role of power management in the design of such devices. In the high-bias regime of a graphene transistor, the Joule heat pumped into a (μ m)² graphene sheet is on the order of 1 mW and the temperature at the center of the sheet can rise above 1,000 K [109]. The majority of the heat is directly or indirectly dissipated through the graphene/substrate interface and the oxide layers (a small portion is carried away by the metal contacts). Studies show that the thermal conductance of the graphene/SiO₂ interface is in the range of 2,000–10,000 WK⁻¹cm⁻² and varies from device to device, likely sensitive to details of the individual interfaces [109, 115]. The thermal conductance of a 300 nm SiO₂ oxide layer is roughly 300 WK⁻¹cm⁻², using a bulk thermal conductivity of 1 WK⁻¹m⁻¹. Reducing the thickness of the oxide and improving the thermal contact of the interface can enhance heat flow through the substrate and further lower the electron temperature, allowing the saturation current to reach even higher values [108].

Finally, it is instructive to point out the difference between the I - V curves in Figs. 2.12 and 2.13. The I - V curves in Fig. 2.12 reach saturation; one of them shows an upturn at very high V_{sd} . In Fig. 2.13a, the experimental I - V curve does not saturate below $E = 1$ V/ μ m, in agreement with calculations. The origin of the saturation observed in the devices used in Fig. 2.12 arises from a spatially varying carrier density profile across the channel, produced by the difference between the top-gate voltage and the varying potential across the channel at high V_{sd} [103]. As shown in the lower inset of Fig. 2.12, a portion of the channel is “pinched off”. This effect is most pronounced in transistors using thin top-gate oxides; it can be modeled and exploited to achieve complete saturation (zero output conductance) in graphene amplifiers.

2.4 Summary and Outlook

Six years after the isolation of a single-layer sheet from the bulk, the young and booming field of graphene has seen rapid progresses in both understanding its fundamental properties as a novel two-dimensional electron system and developing

its potential for nanoelectronics, photonics and energy applications. The focus of the chapter has been to describe the current understanding of electrical transport in 2D graphene, graphene nanoribbons and field effect devices. Various mobility limiting mechanisms including charged impurities, atomic defects, surface corrugations, intrinsic graphene phonons and extrinsic remote oxide phonons are discussed. Presently, charged impurities are the dominant source of scattering in graphene devices, whose elimination requires suspension or chemically inert substrates such as BN. Transport at high source-drain bias is distinctly different from the low-bias regime; the emission of surface optical phonons of the substrate is crucial to current saturation and heat dissipation. The conduction in ribbons is quite complex, due to the presence of Coulomb potential fluctuations and edge disorder. Compared to exfoliated graphene, epitaxial graphene and CVD-grown graphene have clear potential advantages in creating large-scale devices, but require better growth techniques. Substrates play a crucial role in many aspects of graphene electronics. To achieve a high on/off ratio and subthreshold slope in graphene transistors, disorder-induced hopping conduction must be eliminated. There will be abundant challenges and opportunities to use cleaner substrates for graphene growth and transfer to further improve the carrier mobility and to integrate graphene with functional oxides such as magnetic [116] and ferroelectric films [117, 118] to obtain new functionalities. Hybrid device designs incorporating graphene into biological sensors [119] and organic photovoltaics [61] are emerging and much more development is expected on these interdisciplinary fronts to fully utilize graphene's excellent electronic and optical properties.

Acknowledgements The author acknowledges helpful discussions with Bill Cullen, Michael Fuhrer, Philip Kim, Elena Polyakova and Arend Van Der Zande. The assistance of my student Ke Zou in preparing the figures is much appreciated and I thank Vincent Crespi for a careful reading of the manuscript. This work is supported by NSF Grants No. NIRT ECS-0609243 and No. CAREER DMR-0748604.

References

1. Wallace, P. The Band Theory of Graphite. *Physical Review* **71**, 622–634 (1947).
2. Bostwick, A., Ohta, T., Seyller, T., Horn, K. & Rotenberg, E. Quasiparticle dynamics in graphene. *Nature Physics* **3**, 36–40 (2006).
3. Castro Neto, A., Guinea, F., Peres, N., Novoselov, K. & Geim, A. The electronic properties of graphene. *Reviews of Modern Physics* **81**, 109–162 (2009).
4. Park, C., Giustino, F., Spataru, C., Cohen, M. & Louie, S. Angle-resolved photoemission spectra of graphene from first-principles calculations. *Nano letters* **9**, 4234–4239 (2009).
5. Borghi, G., Polini, M., Asgari, R. & MacDonald, A. Fermi velocity enhancement in mono-layer and bilayer graphene. *Solid State Communications* **149**, 1117–1122 (2009).
6. Peres, N. Colloquium: The transport properties of graphene: An introduction. *Reviews of Modern Physics* **82**, 2673 (2010).
7. Brey, L. & Fertig, H. Electronic states of graphene nanoribbons studied with the Dirac equation. *Physical Review B* **73**, 235411 (2006).

8. Nakada, K., Fujita, M., Dresselhaus, G. & Dresselhaus, M.S. Edge state in graphene ribbons: Nanometer size effect and edge shape dependence. *Physical Review B* **54**, 17954–17961 (1996).
9. Son, Y., Cohen, M. & Louie, S. Half-metallic graphene nanoribbons. *Nature* **444**, 347–349 (2006).
10. Barone, V., Hod, O. & Scuseria, G. Electronic structure and stability of semiconducting graphene nanoribbons. *Nano Lett* **6**, 2748–2754 (2006).
11. Ando, T., Fowler, A. & Stern, F. Electronic properties of two-dimensional systems. *Rev. Mod. Phys.* **54**, 437–672 (1982).
12. Piscanec, S., Lazzeri, M., Mauri, F. & Ferrari, A. Optical phonons of graphene and nanotubes. *The European Physical Journal-Special Topics* **148**, 159–170 (2007).
13. Charlier, J.C., Eklund, P., Zhu, J. & Ferrari, A. Electron and phonon properties of graphene: Their relationship with carbon nanotubes. *Carbon Nanotubes*, 673–709 (2008).
14. Hwang, E. & Das Sarma, S. Acoustic phonon scattering limited carrier mobility in two-dimensional extrinsic graphene. *Physical Review B* **77**, 115449 (2008).
15. Efetov, D.K. & Kim, P. Controlling Electron-Phonon Interactions in Graphene at Ultrahigh Carrier Densities. *Physical Review Letters* **105**, 256805 (2010).
16. Chen, J., Jang, C., Xiao, S., Ishigami, M. & Fuhrer, M. Intrinsic and extrinsic performance limits of graphene devices on SiO₂. *Nature Nanotechnology* **3**, 206–209 (2008).
17. Zou, K., Hong, X., Keefer, D. & Zhu, J. Deposition of high-quality HfO₂ on graphene and the effect of remote oxide phonon scattering. *Physical Review Letters* **105**, 126601 (2010).
18. Fischetti, M., Neumayer, D. & Cartier, E. Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-kappa insulator: The role of remote phonon scattering. *Journal of Applied Physics* **90**, 4587–4608 (2001).
19. Fratini, S. & Guinea, F. Substrate-limited electron dynamics in graphene. *Physical Review B* **77**, 195415 (2008).
20. Deal, B. The current understanding of charges in the thermally oxidized silicon structure. *Journal of the Electrochemical Society* **121**, 198C (1974).
21. Zhuravlev, L. The surface chemistry of amorphous silica. Zhuravlev model. *Colloids and Surfaces A: Physicochemical and Engineering Aspects* **173**, 1–38 (2000).
22. Romero, H.E. et al. n-Type behavior of graphene supported on Si/SiO(2) substrates. *ACS NANO* **2**, 2037–44 (2008).
23. Kim, W. et al. Hysteresis caused by water molecules in carbon nanotube field-effect transistors. *Nano Lett* **3**, 193–198 (2003).
24. Aguirre, C. et al. The Role of the Oxygen/Water Redox Couple in Suppressing Electron Conduction in Field-Effect Transistors. *Adv. Mater.* **21**, 3087–3091 (2009).
25. Adam, S., Hwang, E., Galitski, V. & Das Sarma, S. A self-consistent theory for graphene transport. *Proceedings of the National Academy of Sciences* **104**, 18392 (2007).
26. Hwang, E., Adam, S. & Das Sarma, S. Carrier transport in two-dimensional graphene layers. *Physical Review Letters* **98**, 186806 (2007).
27. Ando, T. Screening effect and impurity scattering in monolayer graphene. *Journal of the Physical Society of Japan* **75**, 074716 (2006).
28. Nomura, K. & MacDonald, A. Quantum transport of massless dirac fermions. *Physical Review Letters* **98**, 076602 (2007).
29. Hong, X., Zou, K. & Zhu, J. Quantum scattering time and its implications on scattering sources in graphene. *Physical Review B* **80**, 241415 (2009).
30. Chen, J. et al. Charged-impurity scattering in graphene. *Nature Physics* **4**, 377–381 (2008).
31. Shon, N.H. & Ando, T. Quantum transport in two-dimensional graphite system. *Journal of the Physical Society of Japan* **67**, 2421–2429 (1998).
32. Monteverde, M. et al. Transport and Elastic Scattering Times as Probes of the Nature of Impurity Scattering in Single-Layer and Bilayer Graphene. *Physical Review Letters* **104**, 126801 (2010).

33. Dean, C. et al. Boron nitride substrates for high-quality graphene electronics. *Nature Nanotechnology* **5**, 722–726 (2010).
34. Bolotin, K. et al. Ultrahigh electron mobility in suspended graphene. *Solid State Communications* **146**, 351–355 (2008).
35. Du, X., Skachko, I., Barker, A. & Andrei, E.Y. Approaching ballistic transport in suspended graphene. *Nature Nanotechnology* **3**, 491–495 (2008).
36. Zhang, Y., Brar, V., Girit, C., Zettl, A. & Crommie, M. Origin of spatial charge inhomogeneity in graphene. *Nature Physics* **5**, 722–726 (2009).
37. Deshpande, A., Bao, W., Miao, F., Lau, C. & LeRoy, B. Spatially resolved spectroscopy of monolayer graphene on SiO₂. *Physical Review B* **79**, 205411 (2009).
38. Stolyarova, E. et al. High-resolution scanning tunneling microscopy imaging of mesoscopic graphene sheets on an insulating surface. *Proceedings of the National Academy of Sciences* **104**, 9209 (2007).
39. Stauber, T., Peres, N. & Guinea, F. Electronic transport in graphene: A semiclassical approach including midgap states. *Phys. Rev. B* **76**, 205423 (2007).
40. Wehling, T.O., Katsnelson, M.I. & Lichtenstein, A.I. Adsorbates on graphene: Impurity states and electron scattering. *Chem Phys Lett* **476**, 125–134 (2009).
41. Chen, J.-H., Cullen, W., Jang, C., Fuhrer, M. & Williams, E. Defect Scattering in Graphene. *Phys. Rev. Lett.* **102**, 236805 (2009).
42. Ni, Z. et al. On resonant scatterers as a factor limiting carrier mobility in graphene. *Nano letters* **10**, 3868–3872 (2010).
43. Hong, X., Cheng, S.-H., Herding, C. & Zhu, J. Colossal negative magnetoresistance in dilute fluorinated graphene. *Phys. Rev. B* **83**, 085410 (2011).
44. Lucchese, M. et al. Quantifying ion-induced defects and Raman relaxation length in graphene. *Carbon* **48**, 1592–1597 (2010).
45. Katsnelson, M. & Geim, A. Electron scattering on microscopic corrugations in graphene. *Philosophical Transactions A* **366**, 195 (2008).
46. Geringer, V. et al. Intrinsic and extrinsic corrugation of monolayer graphene deposited on SiO₂. *Physical Review Letters* **102**, 076102 (2009).
47. Cullen, W.G. et al. High-Fidelity Conformation of Graphene to SiO₂ Topographic Features. *Phys Rev Lett* **105**, 215504 (2010).
48. Meyer, J.C. et al. The structure of suspended graphene sheets. *Nature* **446**, 60–63 (2007).
49. Lui, C., Liu, L., Mak, K., Flynn, G. & Heinz, T. Ultraflat graphene. *Nature* **462**, 339 (2009).
50. Bao, W. et al. Controlled ripple texturing of suspended graphene and ultrathin graphite membranes. *Nature nanotechnology* **4**, 562–566 (2009).
51. Schedin, F. et al. Detection of individual gas molecules adsorbed on graphene. *Nature Materials* **6**, 652–655 (2007).
52. Lohmann, T., Von Klitzing, K. & Smet, J. Four-Terminal Magneto-Transport in Graphene pn Junctions Created by Spatially Selective Doping. *Nano letters* **9**, 1973–1979 (2009).
53. Wei, D. et al. Synthesis of N-doped graphene by chemical vapor deposition and its electrical properties. *Nano letters* **9**, 1752–1758 (2009).
54. Pi, K. et al. Electronic doping and scattering by transition metals on graphene. *Physical Review B* **80**, 075406 (2009).
55. Wehling, T. et al. Molecular doping of graphene. *Nano Lett* **8**, 173–177 (2008).
56. Leenaerts, O., Partoens, B. & Peeters, F. Adsorption of H₂O, NH₃, CO, NO₂, and NO on graphene: A first-principles study. *Physical Review B* **77**, 125416 (2008).
57. Chen, W., Chen, S., Qi, D.C., Gao, X.Y. & Wee, A.T.S. Surface transfer p-type doping of epitaxial graphene. *Journal of the American Chemical Society* **129**, 10418–10422 (2007).
58. Choi, J., Lee, H., Kim, K., Kim, B. & Kim, S. Chemical Doping of Epitaxial Graphene by Organic Free Radicals. *The Journal of Physical Chemistry Letters* **1**, 505–509 (2009).
59. Bae, S. et al. Roll-to-roll production of 30-inch graphene films for transparent electrodes. *Nature nanotechnology* **5**, 574 (2010).

60. Park, H., Rowehl, J.A., Kim, K.K., Bulovic, V. & Kong, J. Doped graphene electrodes for organic solar cells. *Nanotechnology* **21**, 505204 (2010).
61. Gomez De Arco, L. et al. Continuous, highly flexible, and transparent graphene films by chemical vapor deposition for organic photovoltaics. *ACS nano* **4**, 2865–2873 (2010).
62. Yang, Y. & Murali, R. Impact of size effect on graphene nanoribbon transport. *Electron Device Letters, IEEE* **31**, 237–239 (2010).
63. Campos-Delgado, J. et al. Bulk production of a new form of sp^2 carbon: Crystalline graphene nanoribbons. *Nano Letters* **8**, 2773–2778 (2008).
64. Li, X., Wang, X., Zhang, L., Lee, S. & Dai, H. Chemically derived, ultrasmooth graphene nanoribbon semiconductors. *Science* **319**, 1229 (2008).
65. Kosynkin, D. et al. Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons. *Nature* **458**, 872–876 (2009).
66. Jiao, L., Zhang, L., Wang, X., Diankov, G. & Dai, H. Narrow graphene nanoribbons from carbon nanotubes. *Nature* **458**, 877–880 (2009).
67. Cai, J. et al. Atomically precise bottom-up fabrication of graphene nanoribbons. *Nature* **466**, 470–473 (2011).
68. Han, M., Brant, J. & Kim, P. Electron transport in disordered graphene nanoribbons. *Physical review letters* **104**, 056801 (2010).
69. Gallagher, P., Todd, K. & Goldhaber-Gordon, D. Disorder-induced gap behavior in graphene nanoribbons. *Physical Review B* **81**, 115409 (2010).
70. Stampfer, C. et al. Energy gaps in etched graphene nanoribbons. *Phys Rev Lett* **102**, 056403 (2009).
71. Han, M.Y., Özyilmaz, B., Zhang, Y. & Kim, P. Energy band-gap engineering of graphene nanoribbons. *Physical Review Letters* **98**, 206805 (2007).
72. Evaldsson, M., Zozoulenko, I.V., Xu, H. & Heinzl, T. Edge-disorder-induced Anderson localization and conduction gap in graphene nanoribbons. *Physical Review B* **78**, 161407 (2008).
73. Martin, J. et al. Observation of electron–hole puddles in graphene using a scanning single-electron transistor. *Nature physics* **4**, 144–148 (2008).
74. Sols, F., Guinea, F. & Neto, A.H.C. Coulomb blockade in graphene nanoribbons. *Physical Review Letters* **99**, 166803 (2007).
75. Mucciolo, E.R., Castro Neto, A. & Lewenkopf, C.H. Conductance quantization and transport gaps in disordered graphene nanoribbons. *Physical Review B* **79**, 075407 (2009).
76. Querlioz, D. et al. Suppression of the orientation effects on bandgap in graphene nanoribbons in the presence of edge disorder. *Applied Physics Letters* **92**, 042108 (2008).
77. Martin, I. & Blanter, Y.M. Transport in disordered graphene nanoribbons. *Physical Review B* **79**, 235132 (2009).
78. Adam, S., Cho, S., Fuhrer, M. & Das Sarma, S. Density inhomogeneity driven percolation metal-insulator transition and dimensional crossover in graphene nanoribbons. *Physical Review Letters* **101**, 046404 (2008).
79. Zou, K. & Zhu, J. Transport in gapped bilayer graphene: the role of potential fluctuations. *Physical Review B* **82**, 081407 (2010).
80. Taychatanapat, T. & Jarillo-Herrero, P. Electronic Transport in Dual-Gated Bilayer Graphene at Large Displacement Fields. *Physical Review Letters* **105**, 166601 (2010).
81. Yan, J. & Fuhrer, M.S. Charge Transport in Dual Gated Bilayer Graphene with Corbino Geometry. *Nano Letters* **10**, 4521–4525 (2010).
82. Chen, Z., Lin, Y.-M., Rooks, M.J. & Avouris, P. Graphene nano-ribbon electronics. *Physica E* **40**, 228–232 (2007).
83. Wang, X. et al. Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors. *Physical review letters* **100**, 206803 (2008).
84. Basu, D., Gilbert, M., Register, L., Banerjee, S. & MacDonald, A. Effect of edge roughness on electronic transport in graphene nanoribbon channel metal-oxide-semiconductor field-effect transistors. *Applied Physics Letters* **92**, 042114 (2008).

85. Fang, T., Konar, A., Xing, H. & Jena, D. Mobility in semiconducting graphene nanoribbons: Phonon, impurity, and edge roughness scattering. *Physical Review B* **78**, 205403 (2008).
86. Murali, R., Yang, Y., Brenner, K., Beck, T. & Meindl, J.D. Breakdown current density of graphene nanoribbons. *Applied Physics Letters* **94**, 243114 (2009).
87. First, P. et al. Epitaxial Graphenes on Silicon Carbide. *MRS Bulletin* **35**, 296 (2010).
88. Reina, A. et al. Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition. *Nano letters* **9**, 30–35 (2008).
89. Li, X. et al. Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils. *Science* **324**, 1312–1314 (2009).
90. Emtsev, K.V. et al. Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide. *Nature Materials* **8**, 203–207 (2009).
91. Jobst, J. et al. Quantum oscillations and quantum Hall effect in epitaxial graphene. *Physical Review B* **81**, 195434 (2010).
92. Shen, T. et al. Observation of quantum-Hall effect in gated epitaxial graphene grown on SiC (0001). *Applied Physics Letters* **95**, 172105 (2009).
93. Riedl, C., Coletti, C., Iwasaki, T., Zakharov, A. & Starke, U. Quasi-free-standing epitaxial graphene on SiC obtained by hydrogen intercalation. *Physical Review Letters* **103**, 246804 (2009).
94. Miller, D.L. et al. Observing the Quantization of Zero Mass Carriers in Graphene. *Science* **324**, 924–927 (2009).
95. Orlita, M. et al. Approaching the Dirac point in high-mobility multilayer epitaxial graphene. *Physical Review Letters* **101**, 267601 (2008).
96. Wu, X. et al. Half integer quantum Hall effect in high mobility single layer epitaxial graphene. *Applied Physics Letters* **95**, 223108 (2009).
97. Lee, D.S. et al. Raman spectra of epitaxial graphene on SiC and of epitaxial graphene transferred to SiO₂. *Nano letters* **8**, 4320–4325 (2008).
98. Yazyev, O.V. & Louie, S.G. Electronic transport in polycrystalline graphene. *Nature Materials* **9**, 806–809 (2010).
99. Huang, P.Y. et al. Grains and grain boundaries in single-layer graphene atomic patchwork quilts. *Nature* **469**, 389–92 (2011).
100. Nienhaus, H., Kampen, T. & Mönch, W. Phonons in 3 C-, 4 H-, and 6 H-SiC. *Surface science* **324**, L328–L332 (1995).
101. Hwang, J., Kuo, C., Chen, L. & Chen, K. Correlating defect density with carrier mobility in large-scaled graphene films: Raman spectral signatures for the estimation of defect density. *Nanotechnology* **21**, 465705 (2010).
102. Li, X. et al. Large-Area Graphene Single Crystals Grown by Low-Pressure Chemical Vapor Deposition of Methane on Copper. *Journal of the American Chemical Society* **133**, 2816–2819 (2011).
103. Meric, I. et al. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nature Nanotechnology* **3**, 654–659 (2008).
104. Tse, W. & Das Sarma, S. Energy relaxation of hot Dirac fermions in graphene. *Phys. Rev. B* **79**, 235406 (2009).
105. Bistritzer, R. & MacDonald, A. Hydrodynamic theory of transport in doped graphene. *Physical Review B* **80**, 085109 (2009).
106. Barreiro, A., Lazzeri, M., Moser, J., Mauri, F. & Bachtold, A. Transport properties of graphene in the high-current limit. *Physical Review Letters* **103**, 076601 (2009).
107. DaSilva, A., Zou, K., Jain, J. & Zhu, J. Mechanism for current saturation and energy dissipation in graphene transistors. *Physical Review Letters* **104**, 236601 (2010).
108. Perebeinos, V. & Avouris, P. Inelastic scattering and current saturation in graphene. *Phys. Rev. B* **81**, 195442 (2010).
109. Freitag, M. et al. Energy dissipation in graphene field-effect transistors. *Nano letters* **9**, 1883–1888 (2009).

110. Yao, Z., Kane, C. & Dekker, C. High-field electrical transport in single-wall carbon nanotubes. *Physical Review Letters* **84**, 2941–4 (2000).
111. Javey, A., Guo, J., Wang, Q., Lundstrom, M. & Dai, H. Ballistic carbon nanotube field-effect transistors. *Nature* **424**, 654–657 (2003).
112. Park, J.Y. et al. Electron-phonon scattering in metallic single-walled carbon nanotubes. *Nano Letters* **4**, 517–520 (2004).
113. Canali, C., Majni, G., Minder, R. & Ottaviani, G. Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature. *Electron Devices, IEEE Transactions on* **22**, 1045–1047 (1975).
114. Meric, I. et al. Channel Length Scaling in Graphene Field-Effect Transistors Studied with Pulsed Current–Voltage Measurements. *Nano Letters* **11**, 1093 (2011).
115. Mak, K.F., Lui, C.H. & Heinz, T.F. Measurement of the thermal conductance of the graphene/SiO₂ interface. *Applied Physics Letters* **97**, 221904 (2010).
116. Haugen, H., Huertas-Hernando, D. & Brataas, A. Spin transport in proximity-induced ferromagnetic graphene. *Physical Review B* **77**, 115406 (2008).
117. Hong, X., Posadas, A., Zou, K., Ahn, C.H. & Zhu, J. High-Mobility Few-Layer Graphene Field Effect Transistors Fabricated on Epitaxial Ferroelectric Gate Oxides. *Physical Review Letters* **102**, 136808 (2009).
118. Zheng, Y. et al. Gate-controlled nonvolatile graphene-ferroelectric memory. *Applied Physics Letters* **94**, 163505 (2009).
119. Ohno, Y., Maehashi, K., Yamashiro, Y. & Matsumoto, K. Electrolyte-gated graphene field-effect transistors for detecting pH and protein adsorption. *Nano Lett* **9**, 3318–3322 (2009).

Further Reading

- N. W. Ashcroft, and N. D. Mermin, *Solid State Physics* (Brooks Cole, 1976).
- C. Weisbuch, and B. Vinter, *Quantum Semiconductor Structures: Fundamentals and Applications* (Academic Press, 1991).
- Carbon Nanotubes: Advanced Topics in the Synthesis, Structure, Properties and Applications*, edited by Ado Jorio, Gene Dresselhaus and Milred S. Dresselhaus, (Springer, 2008).
- B. I. Shklovskii, and A. L. Efros, *Electronic Properties of Doped Semiconductors* (Springer, 1984).
- Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures*, edited by H. Grabert, and M. H. Devoret, (Plenum Press, New York, 1992).

Chapter 3

Graphene Transistors

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Analog and digital transistors have unique requirements because of their differing applications. Fundamental requirements for analog (RF) applications are low access resistance, low parasitics, and high mobility; digital FETs require a bandgap and complementary operation (normally-on and normally-off devices). In this chapter, Graphene transistors are discussed in light of these requirements and are compared to silicon and III-V transistors. Increasing device density on-chip requires continued geometrical scaling; width and length scaling of graphene FETs are discussed with an emphasis on edge-scattering and methods to compensate for it. Circuit implementations of graphene FETs are looked into including mixers, frequency multipliers, and inverters. A few non-FET graphene transistors are introduced including the Klein tunneling transistor.

3.1 Introduction

Semiconductor technology can be broadly classified into digital and analog electronics. Digital electronics mostly use silicon-based complementary MOSFETs as the unit of switching, are highly integrated (with billions of transistors per chip), and are made in fabs that cost at least USD 1B to build. In addition, the tremendous resources invested in the last four decades have given Si CMOS technology a huge performance advantage. Thus, any new technology that wants to compete with Si technology in digital electronics faces high barriers to entry—from investments required to replace existing fabs to technology development needed to outperform Si CMOS. Analog electronic circuits, on the other hand, are not as highly integrated, and thus are more open to new technologies. Analog circuits are mostly used in the baseband and RF areas for telecom applications and can be implemented in CMOS as well as

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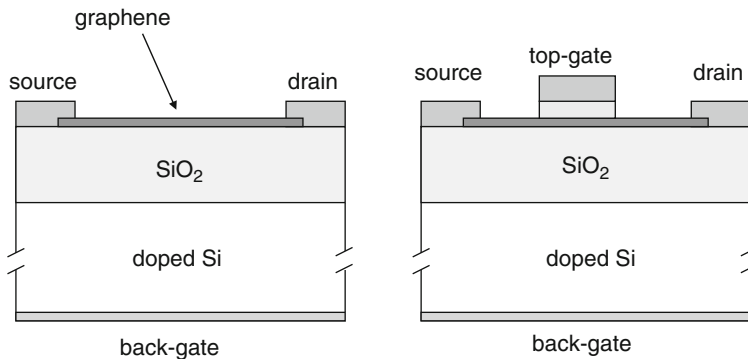


Fig. 3.1 Back-gated and top-gated Graphene FETs are shown in (a) and (b) respectively. Exfoliated and CVD graphene are usually on 300 nm or 90 nm SiO_2 substrate on doped Si. The doped Si allows for backgating

non-silicon materials including SiGe, InP, and GaAs. Thus, graphene has the immediate potential to be applied in analog circuits. This chapter will look at both digital and analog applications of graphene transistors.

While Si MOSFETs are usually top-gated, early graphene FETs (GFETs) were bottom gated. In fact, the optical visibility of single layer graphene (SLG) flakes on 300 nm of SiO_2 was one of the main reasons for back-gating graphene FETs [1]. The scotch-tape technique, first proposed by Geim and Novoselov [2], had wide appeal thanks to the simple tools needed to obtain SLG—repeated peeling of graphite yielded SLG that could then be transferred onto oxidized Si substrates and identified by optical microscopy. E-beam lithography was usually used to align to micron-sized flakes, and metallic contacts were patterned on the flake. One lithography step was thus sufficient to obtain a back-gated (BG) FET. To pattern nanoribbons, additional lithography and etch steps are required. Top-gated FETs (TG FETs) would require additional lithography and etch/deposition steps depending on the type of FET desired. A cross-section of BG and TG GFETs is shown in Fig. 3.1. Epitaxial graphene [3] typically uses TG FETs to study device properties. FETs with a combination of back- and top-gating have been used to study various device phenomena such as bandgap opening in bilayer graphene [4].

In this chapter, the term “GFET” could mean either large-area graphene FETs or graphene nanoribbon (GNR) FETs; GNRs can be formed either from large-area graphene (by lithography and etch) or chemically (from graphite or CNTs, see Chap. 9). In a GFET, varying the gate potential changes the channel Fermi level; this in turn makes the graphene channel either n-type or p-type, and leads to a unique current–voltage curve. When $E_F \sim 0$, the conductivity is minimum; the intrinsic carrier density of graphene is predicted to be $n_i \sim 10^{11} \text{ cm}^{-2}$ [5]. When $E_F > 0$ (i.e. $V_G < 0$), electrons are induced in the channel, leading to mostly electronic conduction. Similarly, when $E_F < 0$, the channel is in majority-hole conduction. The gate voltage at which conductivity a minimum (V_{gmin}) is zero

for ideal graphene but for as-fabricated samples dependent on a number of parameters including impurity type and density, doping from various overlayers, and the work function difference between graphene and the substrate.

Using simple gate electrostatics, the on-off ratio of 2D graphene FETs can be estimated. For large-area BG GFETs on 300 nm SiO₂ with $V_G \sim 50$ V, the induced carrier density is $\sim 3 \times 10^{12} \text{ cm}^{-2}$; since $\sigma = en\mu$, the modulation of conductivity would be ~ 30 ($=n_e/n_i$), where n_e is the induced carrier density, assuming that mobility (μ) is constant as carrier density increases in the channel. In single layer graphene, Coulomb-impurity limited mobility is found to be independent of carrier density (n) while the mobility limited by short-range scattering has a $\mu \propto 1/n$ dependence [6]; assuming negligible short-range scattering, the maximum on-off ratio will be 30, for V_G in the range ± 50 V. Due to impurity-induced effects, the carrier density at $V_G = V_{gmin}$ is higher than n_i and the on-off ratios measured have been smaller than 30 for SLG. Also, the constant μ makes the σ - V_g relationship to be linear—however, μ could be different between the electron and hole regimes because of various asymmetries in the FET.

3.2 Digital FETs

Traditionally, Si MOSFETs have been limited by short-channel effects (SCE) that usually result in a reduced on-off ratio. With each generation of scaling, Dennard's scaling theory [7] requires the depletion depth to be scaled by the same factor as the lateral dimensions; this is to maintain good gate control of the channel but requires higher channel doping; the higher doping reduces channel mobility. Control of SCE should be easier in GNR FETs since the channel is atomically thin.

A bottleneck to continued scaling of Si CMOS [8] is power dissipation and the resulting drain on battery life or need for advanced heat removal techniques. Power dissipation in Si CMOS has two main components: dynamic power ($\frac{1}{2} CV_{dd}^2 f_{clk}$) where C is the capacitance being charged, V_{dd} is the power supply voltage, and f_{clk} is the switching frequency; static power ($I_{off}V_{dd}$) where I_{off} is the off current. There is a third component of power, called short-circuit or switching power, that makes a small contribution to the overall power. The power dissipation can be decreased by one of these methods:

1. Decrease C : C is the sum of device capacitance (C_{DEV}) and wire capacitance (C_W). In recent CMOS generations, C_W has become a major component of C , since wire scaling does not change C_W by much—see Chap. 5 for more discussion; thus merely scaling device footprint is not sufficient to reduce C . Even if graphene transistors were to offer zero C_{DEV} , the power savings resulting from this would be negligible if the circuit architecture did not change. A number of short-wire architectures have been proposed in the past [9]; these reduce the average wire length, and thereby result in a lower average C_W .

2. Reduce V_{dd} : this has a number of challenges including
 - (a) Power supply noise.
 - (b) IR drop in the power supply distribution network.
 - (c) Lower on-current I_{on} (since gate overdrive, $V_G - V_T$, is lower) resulting in a higher delay.
3. Threshold voltage, V_T : V_T can be reduced to allow for a reduction in V_{dd} while maintaining gate overdrive; however, a low V_T causes a high I_{off} , which in turn increases the static power. A high V_T would reduce gate overdrive, and result in a higher circuit delay ($\sim CV_{dd}/I_{on}$)
4. Oxide thickness (t_{ox}) scaling: this allows for better gate control of the channel and a smaller V_{dd} ; however, since the oxide is already down to a few monolayers, there is little room for significant scaling of t_{ox} .
5. Reduce f_{clk} : slower circuits can be used in parallel to overcome circuit delay issues—however, this requires a tradeoff with circuit area and latency. Recent trends in the progression of general purpose microprocessors from single-core to multi-core designs reflects the use of parallelism and lower frequencies to reduce power dissipation [10].

The off-current is made of various components—subthreshold leakage (I_{sub}) and gate leakage (I_{gate}) being the main ones. I_{sub} can be reduced by improving subthreshold swing (S), for e.g. by better control of channel as in a Fin FET [11]. Non-traditional FETs have been proposed that can achieve a low S —these include the tunnel FET [12], impact ionization FET [13] and ferroelectric-dielectric FET [14]. However, each of these designs has a tradeoff with the on-current or with some other transistor metric.

There is significant ongoing effort to find a new transistor that can overcome the power dissipation issues of Si CMOS. Using graphene in FET channels offers many potential advantages including (1) higher mobility, in turn resulting in faster switching, (2) atomically thin channel, resulting in better gate control of the channel, and (3) stacking multiple layers of graphene can enable monolithic 3D integration. In addition, graphene interconnects have been shown to have many advantages compared to copper (which is used as Si CMOS interconnects) including a higher current carrying capacity [15], lower resistivity [16], and smaller mutual capacitance; an all-graphene system can be envisioned that will result in both a better device as well as interconnect performance compared to Si CMOS.

3.3 Bandgap

Complementary operation of FETs (with n- and p-FETs) is commonly used in Si technology; this enables reduced static power when not switching. The off-state is achieved by the creation of a potential barrier between the source and drain—the off current between the source and drain (I_{sub}) is proportional to $\exp(-E_g/kT)$, where

E_g is the bandgap. In the absence of a bandgap, carriers would see a gapless junction from source to drain and the I_{sub} would be unacceptably large.

A simple way of obtaining gapped graphene is by quantum confinement which can be induced by patterning graphene into nanoribbons [17]. Graphene nanoribbons show a bandgap behavior with a relationship $E_g = \alpha/W$ where α has been predicted to be 2 eV, and W is the nanoribbon width (in nm). The reciprocal relationship between E_g and W is one of the prime motivators to use narrow-width GNRs; $W \sim 5$ nm would yield significant bandgap to minimize subthreshold leakage.

Producing GNRs using top-down lithography has been known to produce rough edges—this leads to significant edge-scattering, leading to a reduced mobility in GNRs when width is scaled below 30 nm; this will be discussed in detail in a later section. Other methods of opening a bandgap in graphene include (1) asymmetric field in bilayer graphene [4], (2) substrate-induced gap opening by breaking the crystal symmetry [18], (3) using vertical facets of SiC [19], and (4) nanomesh etched into graphene [20]. Each of these methods has its corresponding issues—(1) a significant field is needed to open the bilayer bandgap (3 MV/cm back-gating for $I_{\text{on}}/I_{\text{off}}$ of 100) and electrostatic doping has been used to provide this field; the bandgap obtained is small compared to that possible from narrow-width GNRs, (2) there are significant arguments that the measurements used for this demonstration are being interpreted wrongly [21], (3) the method does not seem scalable to sub-100 nm GNRs, and (4) mobility suffers as a result of etched patterns in nanomesh graphene. In most of these methods, the inability to vary the bandgap leaves no viable methods of producing novel quantum heterostructure devices.

Transistor operation does not need a bandgap if a non-FET mode of switching is used. Klein tunneling is one approach to make a gapless switch using graphene. In addition, small bandgaps, like those obtained using bilayer graphene, can still be used in devices such as tunnel FETs. Both these concepts will be discussed later in the chapter.

3.4 RF FETs

In RF applications, transistors are operated in the on-state and RF signals to be amplified are superimposed onto the dc gate voltage. The cutoff frequency, f_T , is the frequency at which the magnitude of the small-signal current gain becomes unity, and is indicative of the highest frequency at which the RF can be useful in RF applications. The equation for f_T can be simplified as $f_T = g_m/(2\pi C)$; f_T can be maximized by maximizing g_m and making g_{ds} (the output conductance) as well as all the capacitances and resistances in the equivalent circuit as small as possible. Since most of these parameters vary with both V_{gs} and V_{ds} , f_T usually peaks deep in the saturation region where g_m is near its peak and g_{ds} has decreased significantly [22]. However, in the linear region, f_T is low since g_m is low and g_{ds} is high. Thus, saturation of drain current is necessary to reach a high f_T , Fig. 3.2. The $I_{ds} - V_{ds}$

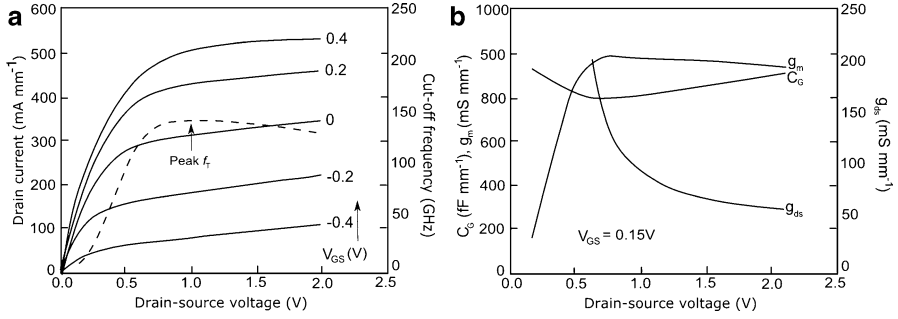


Fig. 3.2 (a) Drain current (*solid lines*) and f_T (*dashed line*) versus drain voltage; and (b) transconductance (g_m), gate capacitance (C_G), and drain conductance (g_{ds}) for a RF GaAs high electron mobility transistor. (Adapted from [22])

characteristics of many graphene FETs show either a linear behavior with no/weak saturation; this reduces g_m and limits device switching speed. Some GFETs show an unusual saturation behavior that includes a second linear region.

In the measurement of f_T for discrete FETs, the effect of parasitics is removed by measuring special “open” and “short” structures and extracting the intrinsic device performance from these measurements. Graphene FETs with GHz capabilities have been reported using both exfoliated and epitaxial graphene. Epitaxial graphene FETs with a f_T of 4.4 GHz and $L \sim 2 \mu\text{m}$ were reported in [23]. This $f_T \cdot L_g$ product is very similar to that of Si nFETs. In [24], a $f_T = 100$ GHz transistor with 240 nm gate was reported; a 10 nm HfO_2 dielectric was used (along with an interfacial polymer layer about 10 nm thick) and the FET showed weak saturation. In spite of such weak saturation characteristics, the graphene FETs outperform silicon MOSFETs. Figure 3.3 shows a comparison of f_T for various FETs. For conventional RF FETs with $L > 0.2 \mu\text{m}$, f_T shows a L^{-1} dependence. f_T also increases with mobility, but at small L , mobility becomes less important than parasitic resistance and short channel effects. The peak f_T of graphene FETs shows a $1/L^2$ dependence [25]; such a behavior was thought to result from operation in the triode (linear) regime.

Two main limiters of RF FET performance are:

1. *Top-gate dielectrics*—deposition of high-K dielectrics reduce channel mobility, and optimal techniques are needed that maintain channel mobility.
2. *Access resistance*—this is the resistance between the source/drain contacts and the gated graphene region; as gate length shrinks, the access resistance becomes a larger part of the overall resistance; methods to reduce this resistance include back-gate electrostatic doping and self-aligned gate formation methods.

Both these limiters are discussed in further detail in later sections and chapters.

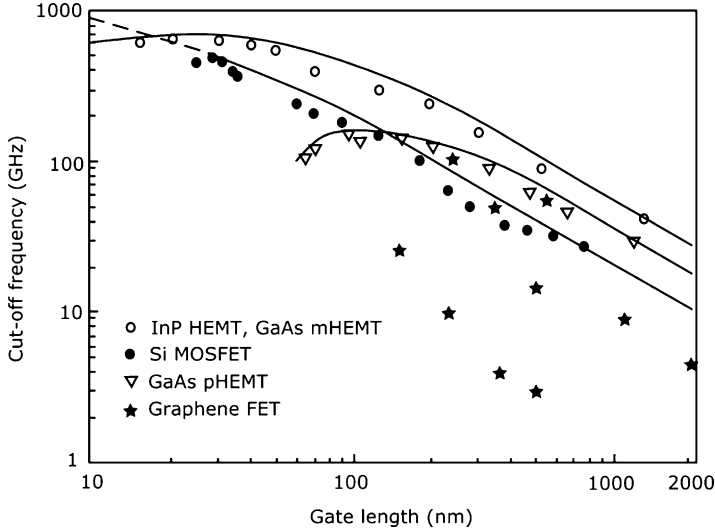


Fig. 3.3 Cutoff frequency comparison for various types of RF FETs including graphene and nanotube FETs. The symbols are experimental data points and the lines are a guide to the eye. (Adapted from [22])

3.5 Width Scaling

As the width of an armchair-GNR is reduced, the bandgap increases but the effective mass increases as well, Fig. 3.4; this reduces the carrier velocity which in turn reduces carrier mobility. This scenario assumes perfect edges; in reality, top-down lithography introduces edge disorder which will introduce additional width-dependent size-effects of carrier transport. Such a size-dependence will reduce carrier-mobility-related advantages that graphene has to offer such as ballistic transport and long coherence length. In many other materials too electrical resistivity becomes size-dependent at nanometer dimensions, e.g. copper [8] and InAs nanowires [27]. In Cu, grain boundary scattering and edge scattering result in a $3\times$ increase in resistivity (compared to the bulk value) when a Cu wire is scaled down to 20 nm width.

Numerous theoretical studies have shown the significant impact of edge scattering on GNR transport. Edge defects break the perfect, repeating hexagonal lattice that defines a specific orientation [28]. Metallic armchair and zigzag GNRs with edge roughness of just a few atoms exhibit significant on-current variation [28]. Interestingly, the results indicate a transport gap that is inversely proportional to ribbon width. Charge suppression mechanisms such as lateral confinement (i.e. quantum dot structures that require carrier tunneling for carrier propagation) work towards opening up this transport gap [29]. As edge disorder increases, the transport gap increases due to increased lateral confinement or “bottlenecks”. In fact, even for

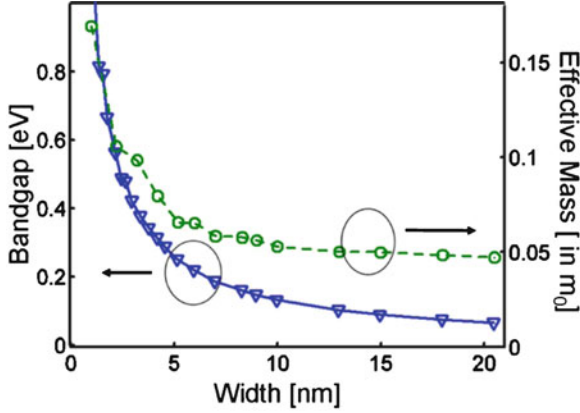


Fig. 3.4 Dependence of bandgap and effective mass on the width of GNRs; m_0 is the free electron mass (Reproduced with permission from [26]. © 2007 IEEE)

metallic zigzag ribbons a transport gap arises for small widths [29]. This observation reveals an important device challenge: transport gaps result in devices with a low mobility and no chirality dependence whereas for best device performance, a true bandgap is desired.

In [28], simulations were used to investigate the impact of disorder on GNRs. A metric for disorder was defined to be zero for maximum disorder and one for an ideal edge. It was found that for a moderately disordered ($r \sim 0.5$) armchair-GNR FET of width 4.18 nm, device on-off ratio is degraded by 10X from the ideal case of a perfect edge. More surprisingly, even for an almost near perfect armchair GNR ($r = 0.99$) a nearly $3\times$ on-off ratio degradation is observed. In another numerical study [30], various scattering mechanisms and their respective limits on carrier transport were considered. Based on a disorder amplitude of 0.5 nm, it has been predicted that edge disorder becomes the dominant scattering mechanism at room temperature (over acoustic phonon scattering) as GNR width scales below 5 nm [30]. Thus a tradeoff currently exists between the need for a band-gap versus the desire for a sufficiently wide ribbon so as to minimize the effects of edge disorder.

In [31], width-dependent mobility of GNRs is extracted using flaked graphene. Figure 3.5(inset) shows a representative device studied in this work. The main metric used in [31] to compare across dimensions was mobility, which changes with carrier concentration; thus it is important to measure mobility at the same carrier density across different GNRs to ensure a fair comparison. This is done by making $V_g - V_{gmin}$ the same across GNRs; the back-gate capacitance is 11.5 nF/cm^2 for 2D graphene, and higher for GNRs (due to fringe fields); for a carrier density of $n = 5 \times 10^{12} \text{ cm}^{-2}$, this translates to $V_g - V_{gmin} \sim 70 \text{ V}$. Mobility is extracted using the electron density relation: $\mu = l/(npe)$ where $n = 5 \times 10^{12} \text{ cm}^{-2}$, ρ is the resistivity, and e is electronic charge. Mobility extraction using the transconductance method yielded similar

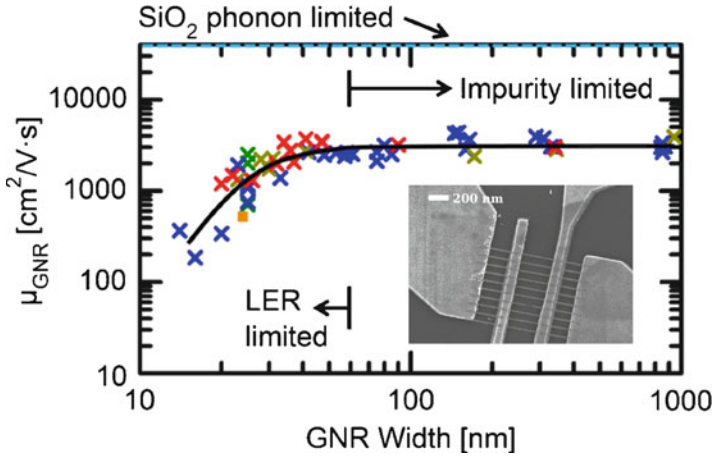


Fig. 3.5 GNR mobility versus GNR width; For $W < 60$ nm, the size effect is seen to degrade GNR mobility. For $W > 60$ nm, mobility is limited by impurity scattering. The inset shows an SEM image of a set of 10 GNRs between each electrode pair (Reproduced with permission from [31]. © 2010 IEEE)

trends but the mobility value extracted using the method is 30–50% lower than that using the carrier density method. The experimentally extracted GNR mobility is shown in Fig. 3.5. Graphene on SiO_2 has various scattering mechanisms limiting its conductivity (1) intrinsic scattering, which limits mobility to $\sim 2 \times 10^5 \text{ cm}^2/\text{V-s}$ (at $T = 300 \text{ K}$)—a mobility of $200,000 \text{ cm}^2/\text{V-s}$ has been measured in suspended graphene [32], (2) extrinsic scattering due to SiO_2 phonons [33], which imposes a carrier mobility limit of $40,000 \text{ cm}^2/\text{V-s}$ at $n = 1 \times 10^{12} \text{ cm}^{-2}$ and $T = 300 \text{ K}$, (3) impurity scattering [34], and (4) line-edge roughness (LER) scattering. It is possible to estimate the contribution of impurity scattering in GNRs using scattering theory [34]. The impurity density is estimated to be $n_i = 2\text{--}19 \times 10^{11} \text{ cm}^{-2}$ for the set of devices used in [31]. LER-limited mobility can be extracted by comparing the mobility of devices before and after the oxygen plasma etch. E-beam lithography was used in [31], and the resulting LER was about 2 nm. A reciprocal relationship is seen between LER-mobility and line-width; the data fit is of the type $\mu_{\text{LER}} = A.W^B$ where A is a constant and $B \sim -4.1$. This value of B compares well with previous work [5] which predicted $B \sim -4$. However, LER-induced mobility degradation sets in at much wider widths than the sub-5 nm dimensions predicted earlier. For $W > 60$ nm, the primary scattering contribution is from impurity scattering whereas for $W < 30$ nm, LER scattering is dominant. While wider ribbons show a mobility of more than $10,000 \text{ cm}^2/\text{V-s}$ for a low impurity density, $\mu < 1,000 \text{ cm}^2/\text{V-s}$ for GNRs with $W < 20$ nm; this is because of the $W^{-4.1}$ dependence of LER-limited mobility.

The size effect also extends to thermal conductivity in graphene. Graphene, in its 2D form, has been shown to have a high thermal conductivity of around $5,000 \text{ W/m-K}$ [35] pointing to its potential use as an on-chip heat spreader. However, recent measurements show that sub 20 nm ribbons have a thermal

conductivity of 1,100 W/m-K—this is due to the increased phonon scattering at the edges. Thus, finding ways to reduce edge scattering can improve nanoribbon thermal conductivity as well.

3.6 Mitigation of Edge Scattering

A traditional method to reduce edge scattering is to optimize the lithography process to lower LER. However, there are limits to how low an LER can be achieved by top-down lithography, and the plasma process that follows lithography will likely introduce additional roughness. Thus, a number of novel methods are being pursued to mitigate edge scattering. These include chemically derived GNRs, hydrogenation, fluorination, passivation of edges, waveguiding structures, gas-based etching, and metal catalyst etching.

Chemically derived GNRs have been produced by many methods (1) starting from graphite, and taken through a chemical exfoliation, the graphite breaks up into fine GNRs; widths down to a few nm have been obtained using this method [36]; (2) GNRs obtained from unzipping CNTs; depending on the starting CNTs, the resulting GNRs could be anywhere from a few nm to a few hundreds of nm wide [37, 38]; (3) self-assembly has been used to make GNRs a few nm wide [39]. Unlike GNRs derived from graphene sheets by top-down lithography, chemically derived graphene (CDG) suffers from placement issues when building circuits. Most experiments utilizing CDG spin coat a solution (containing graphene) onto an oxidized substrate. Following this, various methods (Raman, AFM) are used to identify the position of suitable GNRs, and electrodes are patterned onto these GNRs. Figure 3.6 shows mobility versus linewidth for CDG; also shown is the

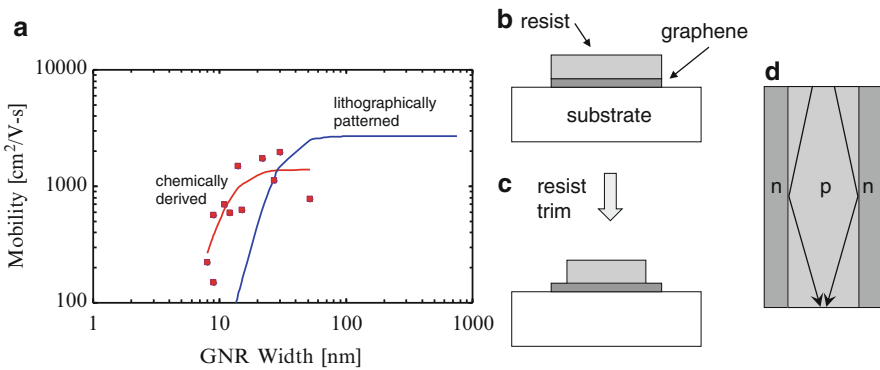


Fig. 3.6 (a) Mobility comparison between lithographically patterned [31] versus chemically derived [36] GNRs; (b–d) Self-aligned formation of carrier waveguides in graphene—(b) the resist pattern is transferred to graphene, to form GNRs, (c) the resist is trimmed by a few nm on each side. The open regions on the GNR can be doped the opposite type as the basal plane; (d) top-view of a GNR with npn junction. Electrons incident on the junction at glancing angles are reflected back into the central region

behavior for flaked graphene. While CDG has a slightly better μ , there is still a large deterioration in transport properties with reducing width. It is not clear if this degradation is due to rough edges or other scattering mechanisms.

Hydrogenation and fluorination can be used to modify the edge structure of GNRs. During etching of GNRs after lithography, a number of dangling bonds and rough edges are created that introduce extra scattering sites. This can be avoided if the edges are converted from sp^2 to sp^3 type of bonding. A variety of techniques could be used for this step—remote plasma, direct plasma with shielding, high temperature furnace processing, etc. Simulations show that partial hydrogenation of wide GNRs can produce narrow GNRs with similar properties as similarly-sized GNRs representing their graphene parts; in addition, it was found that GNRs with unsmooth edges will likely have a better performance after partial hydrogenation [40]. Hydrogenation of graphene converts it to an insulating state, termed [41] “graphane.” Top-down lithography can be used to pattern insulating and conducting regions in graphene [42], thereby creating GNRs without etching away any material. This method has the advantage of avoiding the creation of defects and dangling bonds; thus, carriers in GNRs created this way would face lesser scattering.

Waveguiding structures could be used to limit the interaction of electrons with edges. By defining channels of pnp or npn, it is possible to confine electrons to a central channel, similar to total internal reflection of light in an optical fiber. The physical mechanism responsible for confining electrons in the central region is pseudospin conservation, to be discussed later in this chapter. Two possible confinement methods can be used [43]—‘optical’ guiding where the ‘cladding’ has a lower carrier density than the core, and ‘p-n’ guiding where the core and cladding have opposite carrier types. Confinement is dependent on a number of factors including launch angle of carriers, doping concentration, doping abruptness, contact material, and stray doping from ambient/substrate/contacts. A self-aligned technique can be used to form such waveguide structures. Starting with a resist material that can also act as a dopant, GNRs of a particular width are formed by etching away the exposed graphene. The resist is then trimmed to reveal GNR edges—the edge can then be doped with a different material to form ‘p-n’ guides or left undoped to form ‘optical’ guides, Fig. 3.6.

Gas-phase etching has been used in a CVD chamber to achieve highly controlled etching of GNRs [44]. Lithographically patterned GNRs were narrowed down at the rate of a few nm/min to a few nm in width. The etch was performed by a high temperature oxidation of graphene in a slightly reducing environment in the presence of ammonia. GNRs of 20–30 nm width were patterned lithographically and were etched down to <10 nm. On-off ratios in excess of 10^4 were achieved at room temperature; however, mobility was less than $50 \text{ cm}^2/\text{V-s}$ for these GNRs and thus there was no advantage in carrier mobility compared to lithographically defined GNRs.

Thermally activated metal nanoparticles have been used to define crystallographic edges in graphene. In [45], activated nickel nanoparticles were used to obtain sub-10-nm nanoribbons with edges aligned along a single crystallographic direction, Fig. 3.7. Etched cuts did not intersect, resulting in continuously connected

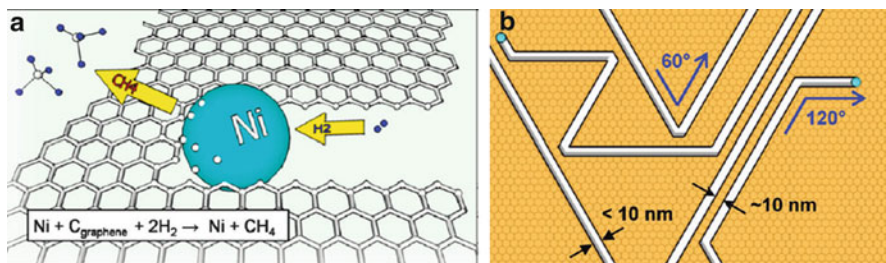


Fig. 3.7 (a) A Ni particle etching a graphene sheet. Ni particles are thought to absorb C from graphene edges and the C reacts with H_2 to make methane. (b) Chirality-preserving angles are seen in SLG etching; nanoribbons of 10 nm width were formed by this method (Reproduced with permission from [45]. © 2009 American Chemical Society)

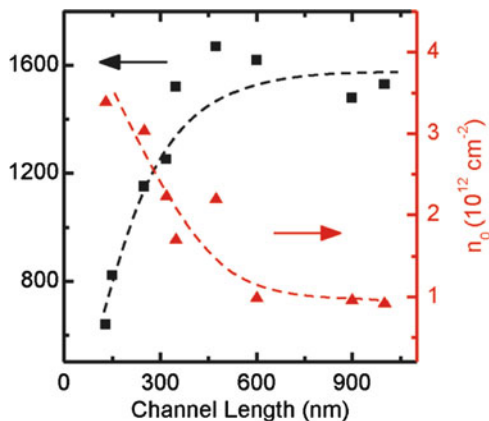
geometries. In addition, Raman spectroscopy showed that the quality of the graphene did not degrade after the etch. In [46], Fe nanoparticles are used to etch graphene and produce long crystallographic edges. Flaked graphene is uniformly spin-coated with a 15 mL solution of 50 mg/L $Fe(NO_3)_3 \cdot 9H_2O$ in isopropyl alcohol. The samples are then transferred to a furnace and heated in hydrogen and argon gas flow (320 sccm/600 sccm, respectively) at $900^\circ C$ for 45 min. At these temperatures, the Fe accumulates to form nanoparticles which can diffuse along the surface of the oxide and graphene. The high temperature provides enough energy for the metal particles to move in specific directions, cutting graphene as they move. The challenge in this approach is to achieve controlled cutting of graphene.

3.7 Length Scaling

Length scaling is important for both device density and to achieve faster switching. An early work on length scaling in graphene [47] indicated that mobility remained constant down to $L \sim 2 \mu m$ and decreased linearly for $L < 2 \mu m$. The behavior was thought to be because of a combination of (1) a non-scaling series resistance, and (2) crossover from diffusive to ballistic regime of transport. The mean free path was extracted to be 300 ± 100 nm.

In [48], pulsed measurements were used to study channel length (L) scaling; L was varied between 130 nm and $2.5 \mu m$; pulsed measurements are usually used to avoid the effect of charge traps, which manifest as hysteresis in the IV curves. The devices were characterized in the p-doped regime since the contacts were p-doping graphene underneath the metal. It was found that when pulsed IV measurements were used (pulsed input for both top-gate and drain, with back-gate grounded), the devices exhibited significant improvement in g_m and output conductance in saturation, when compared to DC measurements. In addition,

Fig. 3.8 Field-effect mobility and impurity density versus channel length
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saturation characteristics were consistently observed in the IV response. The intrinsic g_m of a 130 nm device was more than 0.45 mS/ μm ; g_m was almost independent of channel length—this indicated that velocity saturation is the main cause of current saturation. It was found that the low field mobility decreased with L for $L < 500$ nm—from 1500 cm^2/Vs to 640 cm^2/Vs at $L \sim 130$ nm, Fig. 3.8. The cause of this is thought to be from graphene damage during metal-contact fabrication rather than because of a crossover from diffusive to quasi-ballistic transport. This assertion was supported by the fact that (a) mean free path was only 28 nm in these devices, and (b) high-field transport is unaffected by the length scaling, indicating that the transport in these devices is determined by phonon emission and not by impurity scattering.

3.8 Impact of Number of layers on FET Performance

Using simulations, it was shown in [49] that with thin gate oxide and reduced interlayer coupling, multi-layer graphene (MLG) FETs can achieve a high on-current. For a $W \sim 2.7$ nm armchair GNR, it was found that the bandgap reduces from 516 to 197 meV as the number of layers ($n_\#$) increases from 1 to 10. In addition, E_g decreases monotonically with increasing coupling strength—this decrease is more significant for GNRs with a larger $n_\#$ and can increase band to band tunneling, resulting in a higher I_{off} . For thin dielectrics, the quantum capacitance (C_Q) is comparable to the oxide capacitance (C_{ox}); as $n_\#$ increases from 1 to 10, the gate capacitance (C_G) increases by 3.9X because of a proportional increase in C_Q (which is a function of carrier density); the average carrier velocity decreases slightly (by 15%) and the on-current improves by 3.2X.

Experimental investigation of MLG FETs was presented in [50] where flaked graphene on 90 nm oxide was used; it was found that for wide-area FETs, I_{on} (I_{off})

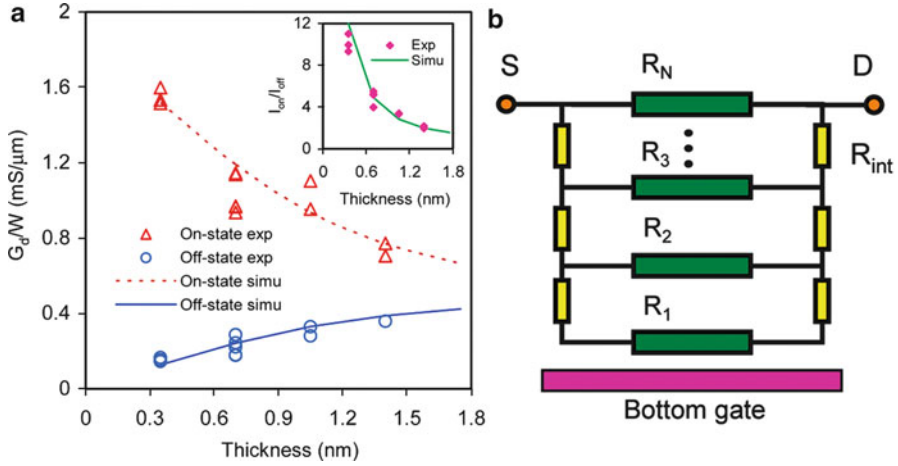


Fig. 3.9 (a) Normalized conductance versus channel thickness for GFETs. The inset shows on-off ratio versus thickness. (b) Resistor network model for BG FET (Reproduced with permission from [50]. © 2009 American Chemical Society)

decreases (increases) with increasing number of layers, Fig. 3.9. The I_{on}/I_{off} ratio scales as $1/n_{\#}$. A resistor network model was used to explain this behavior. An interlayer resistance (R_{int}) of 105Ω was derived from a HOPG block. A screening potential was introduced that describes how fast the gate-induced charge decays from the bottom layer to the top layer (for a bottom gated FET). A Thomas-Fermi screening theory was applied to model the intralayer conductance; the gate induced charge Q_{gate} is distributed among the various layers, with each layer having a charge Q_i :

$$Q_i \propto \frac{1}{t_{ox} + r_i} \exp\left(-\frac{t_{ox} + r_i}{\lambda}\right)$$

$$\sum_{i=1}^{n_{\#}} Q_i = Q_{gate}$$

where λ is the screening length, and r_i is the distance from the bottom of the graphene stack to the i th layer. Assuming that only the top layers are contacted, three different cases were considered: (1) $R_{int} = 0$ and $\lambda = 0$ resulted in a flat I_{on}/I_{off} curve (with increasing $n_{\#}$) (2) $R_{int} = 0.05R_{off}$ and $\lambda = 0$ resulted in increasing I_{on} (with increasing $n_{\#}$) rather than the other way. (3) $R_{int} = 0.05R_{off}$ and $\lambda = 0.6$ nm resulted in a dependence of I_{on} and I_{off} (versus $n_{\#}$) that accurately matched experimental behavior.

Since λ is just over 1 layer thick, the influence of oxide charge can be suppressed in $n_{\#} > 2$ layers. For $n_{\#} = 3$, the current through the bottom layer is only 20% of the current compared to a $n_{\#} = 1$ FET under similar conditions; this was argued to result

in a lower noise in MLG FETs. The resistor network approach was used to model top-gated epitaxial graphene (EG) FETs, and it was found that the decrease in on/off ratio with increasing $n_{\#}$ was less severe than in the back-gated case—this is because of (1) smaller interlayer coupling in EG because of rotational stacking [51], and (2) top-gating combined with top-contacts makes the conduction occur mostly in the layers where the gate has control. In addition, since the bottom layers contribute little to conduction, they serve to decouple substrate-induced charge inhomogeneities [52].

3.9 Doping

Doping offers a way to control the conductivity of graphene, and can also allow control of carrier type. Doping also allows for tuning the carrier injection from the contact to the semiconducting material—band alignment between the electrode and semiconductor is critical for efficient carrier injection. Traditional doping in semiconductors such as Si has been substitutional—an atom of the dopant replaces a host atom and donates a hole or electron. A doping density of 1 per 100,000 host atoms can improve Si conductivity by orders of magnitude compared to intrinsic Si [53]. Carrier mobility in Si falls with increasing doping due to increased scattering from the dopant atoms. For e.g. when doping density increases from 10^{15} cm^{-3} to 10^{18} cm^{-3} , mobility reduces from more than $1000 \text{ cm}^2/\text{V} \cdot \text{s}$ to $300 \text{ cm}^2/\text{V} \cdot \text{s}$. Complementary doping in Si is the cornerstone of CMOS circuits; n-type and p-type transistors are coupled together such that there is no current path from source to ground when the circuit is not switching. Switching from bipolar and NMOS technologies to CMOS resulted in a dramatic reduction in the energy dissipation of solid state circuits.

A number of materials have been used to dope graphene. Unlike substitutional doping in solid state semiconductors, graphene doping is mostly surface charge transfer (SCT) based. It was observed early on that most flaked graphene devices were slightly p-doped even though intrinsic graphene is supposed to be undoped. This p-doping was thought to come from oxygen or water vapor in the ambient. In a controlled experiment, it was found that NH_2 and CO dope graphene n-type whereas H_2O and NO_2 dope it p-type, for gas concentration in the ppm range [54]. The high surface area to volume ratio of graphene makes it a very good sensing platform; on the other hand, because of the unavailability of bonding sites on ideal graphene, most sensing is performed by surface charge transfer doping rather than covalent bonding. Graphene transistors have been used as a probe for getting insight into electrochemical reactions at interfaces, especially atmospheric doping of graphene; the water/oxygen redox couple was identified as the underlying mechanism [55].

It was also noticed that the enhanced sensitivity of graphene to various gases was more due to process residues adhered to its surface rather than the intrinsic response of graphene [56]. These process-induced residues on graphene can be cleaned by current anneals or furnace anneals. Furnace anneals typically involve placing the sample in H_2/Ar flow at elevated temperatures ($>400^\circ\text{C}$) for 1 h. Compared to as fabricated (contaminated) devices, cleaned devices had roughly one-third the

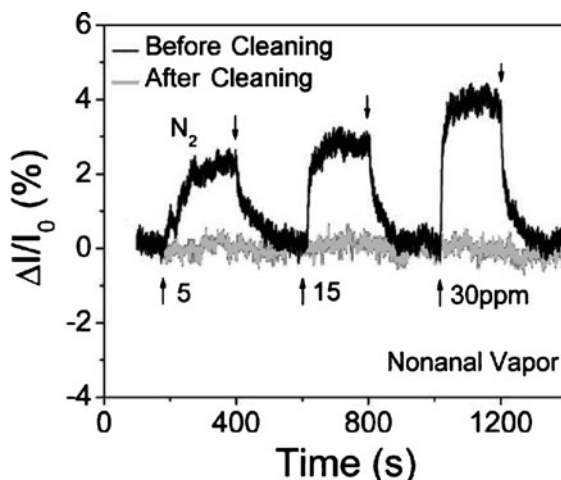


Fig. 3.10 Measured sensor responses, before and after device cleaning. Exposure to nonanal vapor results in a 3% change in current (for 5 ppm exposure) before sample cleaning; but the response drops by 1–2 orders of magnitude after sample cleaning (Reproduced with permission from [56]. © 2009 American Chemical Society)

concentration of doped carriers, four-times higher carrier mobility, and much weaker electrical response (1–2 orders of magnitude lower) on exposure to chemical vapors, Fig. 3.10. AFM measurements revealed that cleaned graphene had a much reduced thickness; in addition, hysteresis in electrical measurements was also reduced significantly. It is likely that resist residue acts as an adsorbent layer that concentrates molecules from the vapors, and thus amplifies the sensitivity of graphene. Polymer films are used as analyte concentrators in some types of vapor sensors, and polymer on graphene could be performing a similar function.

The roughness of the substrate has been found to carry over to graphene [57], and this introduces additional scattering. Also, surface impurities on the SiO₂ substrate introduce electron hole puddles in graphene [52], causing impurity scattering. In addition, the ambient doping of graphene is thought to occur in large part because of the interaction of atmosphere with the SiO₂ substrate. Thus, there is a quest for alternatives for SiO₂ substrates, and various substrates have been tried including mica, SiN, hexagonal boron nitride (h-BN), ferroelectric substrate, and various types of surface functionalization. It has been noticed that ambient doping of graphene can be reversed; the intrinsic doping level drops when graphene is placed in vacuum for an extended period; this can be accelerated by heating the sample above 140°C. This behavior seems to suggest that loosely bound species, like water attached to the silanol groups of the surface, are the main culprits for ambient doping. The initial state of doping is returned when graphene is exposed to air for a short time (~1 min). This reversibility suggests that adsorbate-induced doping is dependent on substrate-specific properties. Substrate quality depends on the morphology and defects of the

SiO₂ surface (for flaked graphene); it is thought that when adsorbates such as hydroxyl groups attach to dangling bonds on the surface, there is a buildup of silanol (SiOH) layer which is hydrophilic. Dipolar molecules can attach to the silanol layer and cause adsorbate-induced doping of graphene. This was a motivation behind chemical hydrophobization of the substrate [58]; the process involves leaving the SiO₂ substrate in a HMDS solution for more than 15 h; the HMDS molecules seem to form an ordered self-assembled layer on the substrate. Electrical measurement reveal that mobilities as high as 12,000 cm²/V^s can be obtained and gate hysteresis is suppressed even in ambient conditions. The HMDS screens the influence of substrate charges, and leads to a more reproducible behavior between different graphene flakes. In a separate work, phenyl-alkyl terminated self assembled monolayers were used to functionalize the oxide surface before transfer of CVD graphene to SiO₂. This was found to result in an improved carrier mobility [59].

H-BN has been found to have an atomically smooth surface and a low density of dangling bonds and charge traps. In addition, its lattice constant is similar to that of graphite and it has a large electrical bandgap. Single- and bilayer graphene on h-BN have been found to have carrier mobilities an order of magnitude higher than graphene on SiO₂; the devices on h-BN also show reduced chemical reactivity and display intrinsic doping [60].

Charge screening has been used to limit disorder induced by the substrate. In [61], ferroelectric PZT substrates were used as a support for graphene flakes; these substrates had a large spontaneous polarization pointing into the surface. This polarization is thought to be almost fully screened by a high-density layer of surface adsorbates prior to exfoliation since the scattering from interfacial adsorbates was found to be much weaker than on SiO₂; carrier mobility in excess of 70,000 cm²/V-s at $n = 2.4 \times 10^{12} \text{ cm}^{-2}$ and $T = 300 \text{ K}$ was measured. In [62] screening was studied by immersing graphene in various organic solvents, with dielectric constants up to 189 (N-methylformamide). The transport characteristics change systematically with dielectric constant; carrier mobility up to 70,000 cm²/V-s have been measured in graphene devices in a high-K solution (with a dielectric constant κ_2). Beyond a certain κ_2 , transport properties do not improve further, indicating that the intrinsic limit of room temperature mobility has been reached (for graphene on SiO₂), Fig. 3.11. The ratio of electron to hole mobility was found to decrease sharply from more than 3 to almost 1 when κ_2 approaches 80. The asymmetric scattering in graphene has been attributed to the differing scattering cross sections by charged impurities for holes and electrons. As the charged impurity scattering is screened, this asymmetry disappears. It was also found that short range scattering is unaltered by the high-K solvents. Ionic solutions of NaF have also been used to investigate screening [63]; it was noticed that as the ionic concentration is increased from 0.005 M to 1 M, carrier mobility increases by more than 5X; the position, and the width of the minimum conductivity point changes significantly, indicating a much weaker intrinsic doping of graphene with increasing ionic concentration.

There have been a few reports of substitutional doping of graphene. In [64], n-doped graphene is obtained by irradiating graphene with 30 keV N⁺-ions

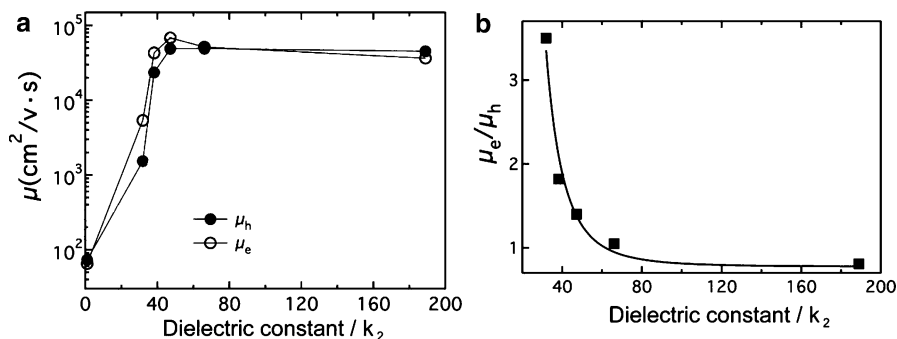


Fig. 3.11 (a) Carrier mobility versus dielectric constant of solution (k_2). Both electron and hole mobility improve as k_2 increases. (b) Ratio of electron to hole mobility versus k_2 (Reproduced with permission from [62]. © 2009 American Chemical Society)

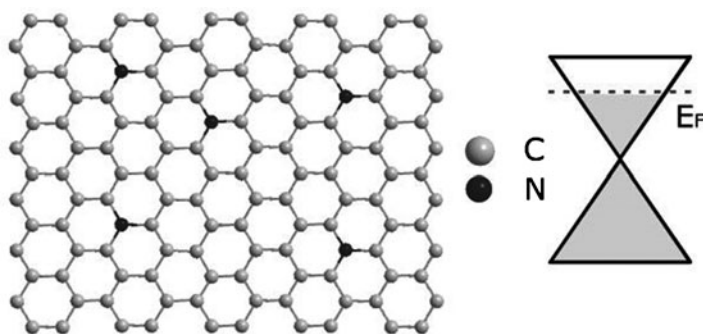


Fig. 3.12 The atomic structure of graphene annealed in NH_3 after irradiation. Graphene is doped by substituting C atoms with N atoms (Reproduced with permission from [64]. © 2010 American Chemical Society)

followed by an anneal in NH_3 , Fig. 3.12. Raman spectroscopy was used to confirm that defects created by N^+ irradiation were restored after the NH_3 anneal. Annealing in NH_3 was compared to that in N_2 ; when annealing in N_2 was followed by Auger electron spectroscopy (AES), there was no N-signal; however, an anneal in NH_3 revealed an N signal. Backgated transport measurements reveal that V_{gmin} is negative after the NH_3 anneal but positive after an N_2 anneal; the positive V_{gmin} after N_2 anneal was thought to be from atmospheric doping of defect sites. Carrier mobility was measured to be a few 1,000 after the NH_3 anneal.

In [65], diazonium salts and poly(ethylene imine) were used to dope graphene to be p-type and n-type, respectively. Graphene devices were exposed to a solution of 4-bromobenzenediazonium tetrafluoroborate at 300 K in atmosphere. The resulting IV curve was found to have shifted to the right, indicating p-type doping. In addition, electron mobility was found to be reduced when compared to the as-fabricated device; the hole mobility and minimum conductivity were found to be unchanged.

This lack of conductance suppression suggested that there was no significant sp^3 hybridization; Raman imaging suggested that the attachment of diazonium salts was more than simple van der Waal's adsorption.

PEI has been known to be an n-type dopant for CNTs. Graphene devices were soaked in a 20% PEI solution for 3 h at 300 K. Post-soak testing revealed a strong n-type doping along with a conduction asymmetry, this time for holes. Nonequilibrium Greens function (NEGF) modeling was used to explain this phenomenon; it was postulated that the asymmetry is caused by a combination of the Fermi level misalignment at the electrode/channel interface and the nonconstant DOS of the graphene electrodes. It was also predicted that when graphene is doped by metal, conductance asymmetry occurs even if the channel is intrinsic.

In [66], stacks of CVD graphene were p-doped with nitric acid. The doping decreases sheet resistance by 3X, down to 90 Ω/sq for eight layers. HNO_3 doping is thought to occur when electrons are transferred from graphene to nitric acid during the formation of a charge-transfer complex:



Two types of doping were demonstrated—"interlayer doped" where doping was performed after each layer was stacked, and "last layer doped" where doping was performed after all layers were stacked, Fig. 3.13. Simulations have revealed that the graphene surface acts as a catalytic reducing/oxidizing agent; this drives the chemical disproportionation of adsorbed dopant layers into charge transfer complexes; these complexes then inject carriers into the 2D graphene lattice.

It was shown that CVD graphene can be made p-doped by AuCl_3 [67]. CVD graphene on PMMA was dipped in a 5 mM aqueous solution of AuCl_3 ; AuCl_3 is reduced to Au particles by charge transfer from graphene; the surface potential change was studied by Kelvin probe microscopy, and it was found that the potential shift was as much as 0.5 eV within 20s; after 20s, the potential saturates, and then slightly decreases beyond 40s. Au particles were found to aggregate on wrinkles and thicker layers of graphene for less than a 20s exposure; but for doping time longer than 20s, the coverage was more uniform across the graphene surface. In a study of layer by layer doping using AuCl_3 [68], it was found that a four-layer stack of CVD graphene can be doped so that the sheet resistance was 54 Ω/sq . In addition, the optical transmittance of the stack was measured to be 85% at 550 nm wavelength, making it a contender for applications that need a high electrical conductance along with a good optical transmittance.

As-grown epitaxial graphene on SiC, because of the work function difference with the SiC substrate, is n-doped; the Dirac point is 300 meV below the Fermi level. Doping of epitaxial graphene was demonstrated using F4-TCNQ [69], an electron acceptor. ARPES measurements were used to study doping behavior, and it was found that a 0.8 nm thick layer of the dopant was sufficient to compensate for the intrinsic doping induced by the workfunction difference with the substrate. The dopant could be applied via wet chemistry and was fairly stable to temperature and light. In [70] photoemission spectroscopy revealed that electron transfer from

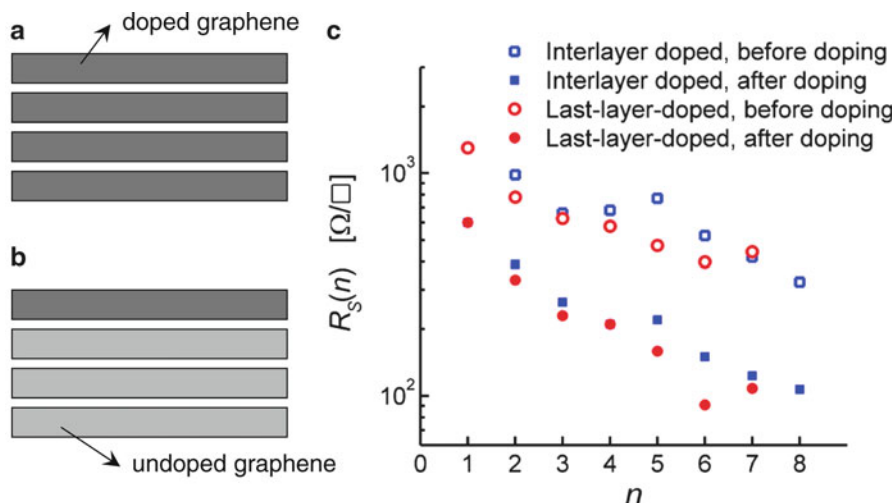


Fig. 3.13 Schematic of (a) interlayer doped and (b) last-layer doped graphene stacks. (c) Sheet resistance versus number of layers for both interlayer and last-layer doped cases (Reproduced with permission from [66]. © 2010 American Chemical Society)

graphene to F4-TCNQ was responsible for p-doping of graphene. F4-TCNQ has an electron affinity of 5.2 eV; another acceptor, C_{60} , was also tried out as a dopant; because of the weaker electron affinity of C_{60} (3.7 eV), only a weak doping of graphene occurs. Gold, bismuth and antimony were also demonstrated to dope epitaxial graphene [71]; the doping was verified by ARPES measurements; it was shown that while bismuth and antimony shifted the Fermi level in the direction of the Dirac point, gold was able to p-dope the graphene, with the Dirac point about 100 meV above the Fermi level.

Chemically derived GNRs were n-doped by ammonia [72] when the GNRs were electrically annealed in a NH_3/Ar mixture at 1 torr. The source-drain bias was swept from zero to a few volt, resulting in a temperature rise of the GNRs due to Joule heating; Raman thermometry revealed that the temperature of these GNRs rose to about 300°C. XPS and nano SIMS confirmed the presence of nitrogen in the GNRs; it was postulated that most of the doping occurred at the edges and defect sites since these regions have a much higher chemical reactivity. In addition, similar mobilities before and after NH_3 doping revealed that carrier transport is not degraded by this method.

Hydrogen silsesquioxane (HSQ) has been investigated as a dopant for graphene; an early report speculated that hydrogen released from HSQ resulted in basal plane hydrogenation [73]. HSQ, a well known spin-on dielectric [74], also came to be known for its use as a high resolution e-beam resist. Thus a doping technique using HSQ can enable high resolution patterning *and* doping [75]. In the context of its use as a spin-on dielectric, HSQ crosslinking has been found to be a complex transition from a hydrogen-rich cage-like structure to a hydrogen-depleted network-like structure [76]. This transition enables HSQ to function as both a p-type and n-type dopant. Flaked graphene was deposited on 300 nm SiO_2 followed by

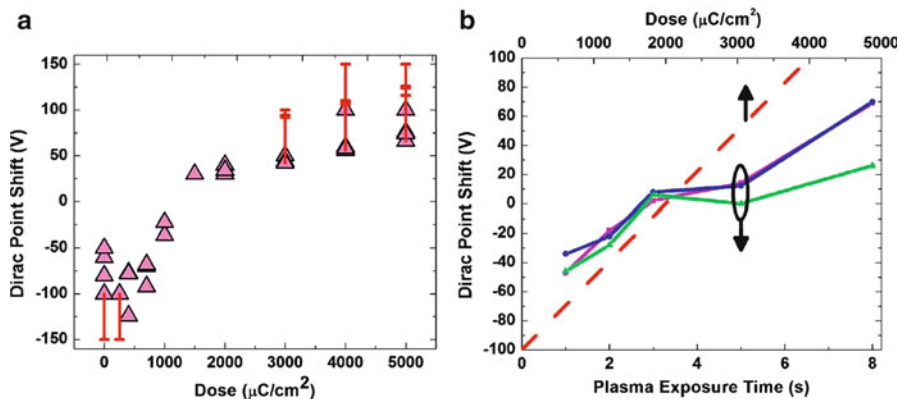


Fig. 3.14 (a) Incident e-beam dose versus V_{gmin} shift for a number of flaked graphene devices coated with 30 nm HSQ. For small incident dose, the graphene is n-doped while for large doses the graphene is p-doped. (b) Doping by plasma-induced cross-linking of HSQ. Electrical measurements were performed after 1 s plasma exposures, for three devices. Also shown for reference is the dependence of V_{gmin} shift on incident e-beam dose (Reproduced with permission from [75]. © 2010 American Institute of Physics)

patterning of contacts. The devices were tested for their electrical response; following this, a 30 nm HSQ layer was spin coated onto the graphene, followed by a 180°C bake for 3 min. One set of samples were washed in TMAH, which is normally used as a developer for HSQ. Electrical testing of these samples revealed a strong n-type doping, indicated by a shift of V_{gmin} to large negative voltages. A second set of samples coated with HSQ was exposed to e-beam radiation; a 100 kV beam was used, and the incident dose (D) ranged from 250 to $5,000 \mu\text{C}/\text{cm}^2$. Since as-fabricated devices can have a slight initial doping, the V_{gmin} shift (rather than the absolute V_{gmin}), ΔV_{gmin} , is used as a metric to gauge HSQ doping. For $250 < D < 1,000 \mu\text{C}/\text{cm}^2$, ΔV_{gmin} increases from less than -100 V to 0 V . For D between $1,000$ to $5,000 \mu\text{C}/\text{cm}^2$, ΔV_{gmin} increases from 0 V to more than 100 V ; a saturation is seen in the amount of shift induced, Fig. 3.14. This saturation is likely because the cross-linking process is almost complete as D reaches $2,000 \mu\text{C}/\text{cm}^2$.

In addition to using e-beam irradiation, plasma and thermal treatment were also investigated for doping large-areas of graphene with HSQ. Thermal annealing of HSQ at 500°C is known to induce a structural change; a plasma of energetic ions is better for processes with a tight thermal budget. A set of devices with a HSQ layer dosed with e-beam irradiation at $600 \mu\text{C}/\text{cm}^2$ was used to study plasma-induced doping from HSQ. A dose $D \sim 600 \mu\text{C}/\text{cm}^2$ was chosen so that the pre-plasma V_{gmin} was close to 0 V . The devices were taken through an exposure to low power Ar plasma. Short, 1 s flash exposures to the plasma were performed followed by electrical testing. ΔV_{gmin} is initially negative and slowly becomes positive compared to the as-fabricated device, Fig 3.14; carrier mobility shows improvement at early stages of cross-linking followed by a saturation at longer exposure times—this indicates that there is little surface damage of graphene as a result of the doping, and there is possibly some compensation of charged impurities, thus actually improving carrier mobility.

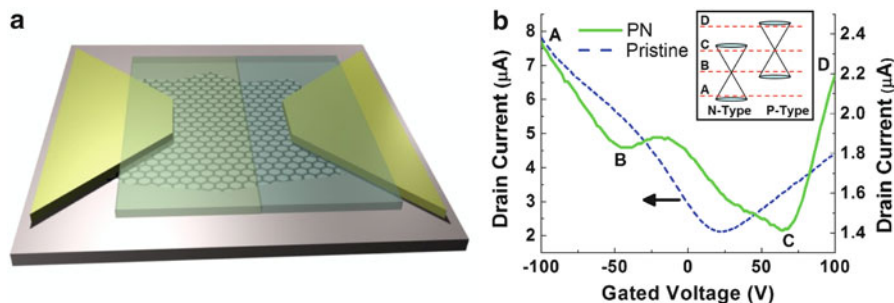


Fig. 3.15 (a) Schematic of a graphene p-n junction—one half of the graphene surface is doped p-type and the other half is doped n-type by HSQ. (b) Electrical testing reveals a double dip for the p-n junction; the Fermi level separation is found to be more than 340 meV (Reproduced with permission from [75]. © 2010 American Institute of Physics)

The ability of HSQ to dope graphene either p-type or n-type results from a mismatch of bond strengths between Si-H and Si-O bonds in the HSQ, as well as outgassing of H at higher degrees of crosslinking. Si-H and Si-O in HSQ have bond strengths of 4.08 eV and 8.95 eV, respectively; at low temperatures (100–200°C) or small incident dose ($<300 \mu\text{C}/\text{cm}^2$ at 100 kV), Si-H bonds are readily broken, providing hydrogen to bond with the graphene basal plane. Due to the offset in electronegativity, hydrogen acts as an n-type dopant for graphene. Higher degrees of cross-linking in the HSQ film leads to p-doping by two primary mechanisms—Si-O bonds being to break at larger incident energies, and this provides O for adsorption at the graphene surface. In addition, hydrogen is removed from the HSQ film by outgassing. Advanced stages of cross linking leads to HSQ decomposing into SiH_4 and H_2 components. These components escape from the HSQ film, as evident through decreased Si-H to Si-O bond ratio as well as the porous nature of the film. The complementary doping property of HSQ has been used to demonstrate p-n junctions; an as-fabricated graphene flake was covered with a film of HSQ followed by high dose e-beam incidence on one half of the flake—this part of the flake becomes p-doped. The other half was left unexposed, and is thus doped n-type. Back-gated IV measurements revealed a double-dip curve indicating a superposition of two V-curves; one V_{gmin} was at +70 V and the other at -50 V, Fig. 3.15; the separation between the energy levels on the p- and n-sides was in excess of 340 meV.

3.10 Performance Projections for Digital FETs

A number of theoretical studies have shown the potential of GFETs. GFETs were simulated in [26]—a top-of-the barrier MOSFET model was used to derive IV curves assuming ballistic transport. As the armchair-GNR width is reduced, the bandgap

increases but the effective mass increases as well, Fig. 3.4; this reduces the carrier velocity. An oxide thickness of 1.1 nm was assumed. Compared to ideal Si MOSFETs at the 90 nm node ($I_{on} \sim 680 \mu\text{A}/\mu\text{m}$), ballistic GFETs were found to have a 2X higher on-current: at widths of 2.2 nm–4.2 nm (armchair GNR FETs) the on-current was 1,300–1,440 $\mu\text{A}/\mu\text{m}$, respectively. Current is the product of average velocity and the carrier density at the top of the barrier. The higher current from GFETs is as a result of the higher average velocity of carriers in the channel—for devices studied in this work, the velocity was 2–4X higher than that in Si. The higher average velocity stems from the lower effective mass of carriers in GFETs—0.15 m_0 and 0.11 m_0 for $W \sim 2.2$ nm and 4.2 nm respectively compared to 0.19 m_0 for Si. But the Si MOSFET has a higher carrier density because of its larger quantum capacitance—however, this is not sufficient to compensate for the much higher velocities in GFETs.

Based on experiments that revealed a small bandgap from substrate-induced effects in epitaxial graphene, the performance of EG FETs were studied in [77]. Subthreshold swing, S , can be derived for these FETs as:

$$S = \left(1 + \frac{C_{sub} + C_Q}{C_G} \right) \frac{kT}{q} \ln(10)$$

FET operation was studied by varying V_{ds} , donor molar fraction at the contacts (α_D), and oxide thickness t_{ox} . Increasing V_{ds} from 0.1 V to 0.25 V results in a S increase from 84 to 202 mV/dec—this is because the increased V_{ds} causes hole accumulation and increases C_Q . Increasing the contact doping increases both the on and off current because of the improved capacity for carrier injection from the source. A smaller doping level is found to be better to achieve a low I_{off} . Increasing the t_{ox} leads to a worse S because of the weaker capacitive coupling between gate and channel. For lower V_{ds} (0.1 V), the effect of increasing t_{ox} is weaker— S is almost constant at 75 mV/dec for t_{ox} varying from 1 nm to 4 nm. It was shown that even with optimized device parameters, an on-off ratio of only 50 can be obtained with $V_{dd} \sim 0.25$ V, with $S \sim 140$ mV/dec.

In [78], a virtual-source based IV model was discussed. This model aimed to describe ambipolar transport in short-channel GFETs; transistor operation is broken down into three regions (I) at high V_g , quasi-Fermi level is above E_{dirac} , and conduction is mostly by electrons, (II) transition region where the channel conduction is by both electrons and holes, and (III) low V_g conduction is by holes. In region II, electrons are injected from the source and holes injected from the drain—these meet and recombine in pairs at some point in the channel, Fig. 3.16. Modulation of the contact resistance by backgate was also included in the model. Virtual-source carrier velocity (v) was extracted for GFETs (with CVD-grown graphene) and compared to Si MOSFETs as well as III-V heterostructure FETs, Fig. 3.17. GFETs show a v of more than 2.5×10^7 cm/s—higher than either Si or III-V HFETs.

In [79], a three-dimensional quantum simulation study was used to study GFET behavior. A multiple-gate geometry was found to improve short-channel effects but

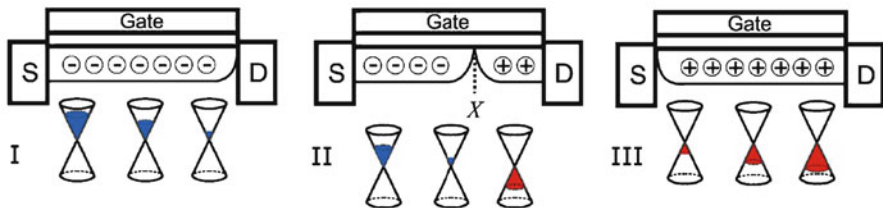


Fig. 3.16 Three operating regimes of the GFET are shown. (I) n-Type carriers in the channel (II) ambipolar transport. Point X is the recombination point. (III) p-Type carriers in the channel. Also shown is the bandstructure along with the location of the Fermi level at different points in the channel (Reproduced with permission from [78]. © 2011 IEEE)

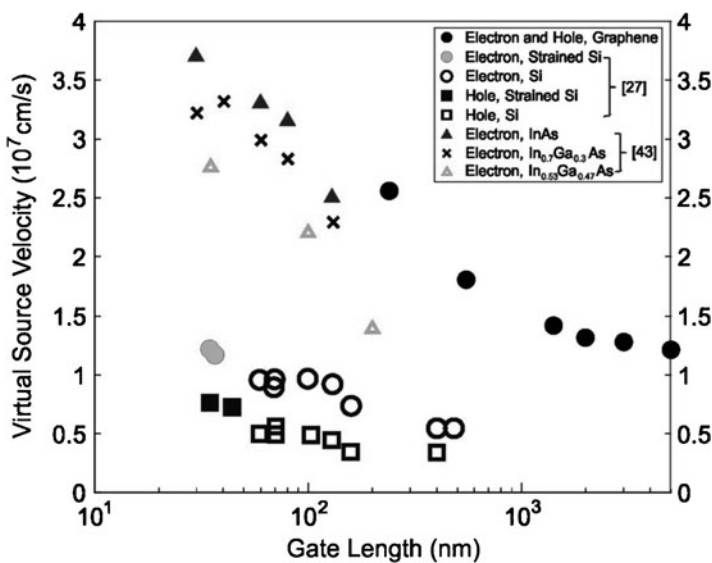


Fig. 3.17 Virtual source injection velocity versus gate length for various transistors (Reproduced with permission from [78]. © 2011 IEEE)

the improvement was not as significant as that for equivalent Si MOSFETs (in terms of I_{on} and g_m). Reducing t_{ox} was found to be more important than using high- κ dielectrics for improved transistor performance. For $L < 10$ nm, I_{off} was found to increase significantly because of source-drain tunneling. Here the GFET operated close to the quantum capacitance limit (because of the low density of states); thus adding multiple gates has little impact on the gate capacitance which is dominated by the quantum capacitance. As a result, gate geometry (single, double or gate-all around configurations) did not significantly affect S and DIBL as compared to a Si MOSFET, for $L \sim 20$ nm. The GFET parameters were $W \sim 1.3$ nm, $V_{dd} \sim 0.5$ V,

$t_{\text{ox}} = 2 \text{ nm}$, and $\kappa = 4$. For $L \sim 20 \text{ nm}$ and 10 nm , the on-off ratio is 1800 and 240, respectively. For $L \sim 5 \text{ nm}$, the transistor behaves more like a conductor, and there is little modulation of drain current because of direct tunneling from source to drain. Because of the larger carrier velocity in graphene, the intrinsic delay can be 3.5X better than an equivalent Si MOSFET with $L \sim 10 \text{ nm}$.

3.11 Contact Resistance

Usually metal–semiconductor junctions form a Schottky barrier while metal–metal contacts have no potential barrier and the vacuum level changes abruptly at the metal/metal interface [80]. The screening length is given by

$$\chi^{-1} = \sqrt{4\pi N(E_f)}$$

where $N(E_f)$ is the DOS at E_f , the Fermi level; χ is very short in metals (fraction of a nm). The graphene metal contact is similar to the metal–metal contact; however because of the low DOS for graphene, even a small charge transfer results in a large shift of the Fermi level and also a large χ , Fig. 3.18. This charge transfer forms a dipole layer at the interface; the graphene–metal contact can be quantified by two quantities— δV (the dipole potential) and ϕ_{MG} (the work function difference between graphene and metal). The long charge transfer region causes a p–n junction to form near the metal/graphene contact.

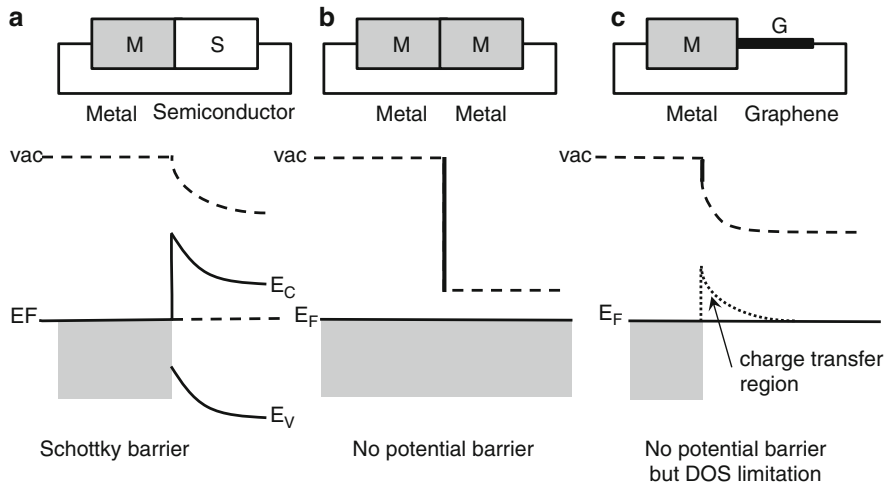


Fig. 3.18 Energy band diagram for (a) metal–semiconductor (b) metal–metal and (c) metal–graphene contacts (Adapted from [80])

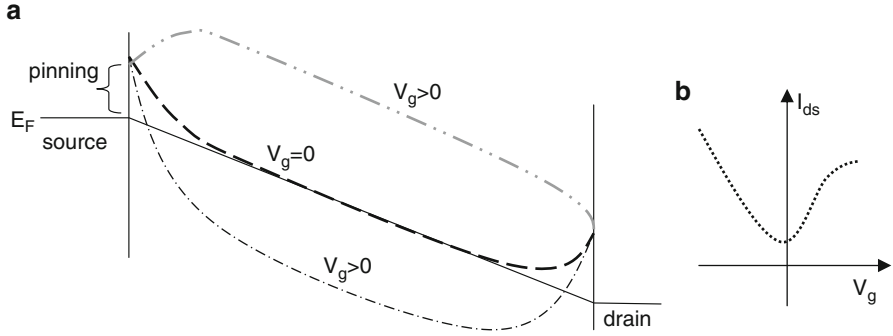


Fig. 3.19 (a) Band-diagram showing source-channel-drain regions for various gate biases. The metal contact is assumed to induce electron doping in graphene. For $V_g > 0$, a pn junction is formed both at the source and drain, and introduces additional resistance, thereby causing asymmetry in the IV response (b)

The formation of a p–n junction can be dependent on the back-gate bias. For a electron-doping metal contact, a negative V_g results in the usual linear σ - V_g curve; but a positive V_g results in a additional resistance from the p-n-p junction. This introduces asymmetry in the IV response, Fig. 3.19. Contact doping of graphene has been studied both theoretically and experimentally. It was shown that external electrodes behave differently from invasive electrodes on graphene [81].

A scaling analysis of the two-probe device resistance can be used to extract contact resistance. Devices with different contact separation are tested for their two-terminal resistance, R_{2p} ($=2R_c + R_{GR}$), where R_{GR} is the graphene channel resistance, and R_c is the contact resistance; note that both R_{GR} and R_c can be dependent on the back-gate voltage for structures that are backgated. R_c is extracted by plotting R_{2p} versus L , and extrapolating R_{2p} to $L = 0$ (for a given width). The transfer length measurement (TLM) works when the channel length is much larger than the carrier mean free path in the channel (i.e. the channel is diffusive). Another popular method is to use four-probe measurements and compare them to two-probe measurements.

In [82], a Ti/Au bilayer was used to contact graphene of three different thicknesses—single (SLG), bi (BLG) and trilayer (TLG) graphene. The contact resistance was found to be quantitatively the same for different layer thicknesses, gate voltages and temperatures $\sim 800 \pm 200 \Omega\text{-}\mu\text{m}$. Since the electronic properties of SLG, BLG and TLG are very different, the similarity in R_c for varying n suggests that a charge transfer from metal to graphene shifts the Fermi level far from the Dirac point. This could also be the reason why R_c is independent of the backgate voltage—the density of charges induced by the backgate is much smaller than the charge transfer from metal. In [83], TLM structures were used to extract the contact resistance of backgated graphene FETs with 60 nm Ni contacts. Contact resistivity was found to be independent of the backgate voltage as well as the number of layers. The contact resistivity was found to be $10^{-5} \Omega\text{-cm}^2$.

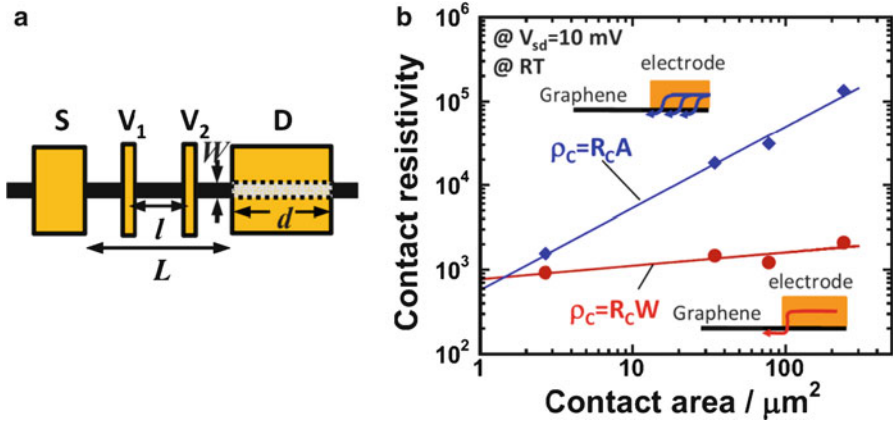


Fig. 3.20 (a) Device schematic showing source and drain contacts, as well as voltage probes V_1 and V_2 . W is the ribbon width, D is the contact length, L is the distance between source and drain, and l is the distance between the two inner voltage probes. (b) ρ_{CW} and ρ_{CA} are extracted by a four-probe measurement; the former assumes areal conduction and the latter assumes edge conduction (Reproduced with permission from [84]. © 2010 American Institute of Physics)

In [84], multiprobe devices were used and current-flow path at the metal-graphene junction was discussed. Contact resistance is extracted by using the relation $R_c = 1/2(R_{\text{total}} - R_{\text{ch}} * L/l)$ —the terms are explained in Fig. 3.20. Contact resistivity was extracted by using different contact areas—while the source and drain contact areas were made different, the voltage probes were all similar to avoid any uncertainty from the probes themselves. Two definitions of contact resistivity (ρ_C) were used— $\rho_{cA} = R_c A$ and $\rho_{cW} = R_c W$. While ρ_{cW} is constant with increasing contact area, ρ_{cA} shows a monotonically increasing behavior, Fig. 3.20. This indicates that ρ_C is characterized by contact length rather than contact area; this is possibly because of current crowding at the edge of the contact metal. It was also confirmed that the crowding depends on the contact metal—Cr/Au, Ti/Au and Ni were found to have contact resistivity ranges of 5×10^3 – 10^5 , 10^4 – 10^5 , and 400–2000 $\Omega \cdot \mu\text{m}$, respectively. Also, it was found that ρ_{cW} was independent of layer thickness for all these three types of contact metals. A transmission line model was used to understand the edge conduction—in the model, ρ_C (contact resistivity) was defined in units of $\Omega \cdot \text{cm}^2$. The other two resistances in the model are the sheet resistance of metal (R_{ms}) and sheet resistance of graphene (R_{gs}); while R_{ms} is low, R_{gs} is not—this is because the high mobility of graphene is not sufficient to compensate for its low carrier density compared to that of metal. A transfer length γ was defined as $\gamma = \sqrt{(\rho_C/R_{\text{gs}})}$; γ takes into account the fact that current does not flow only across the edge but diffuses a certain distance into graphene. A cross bridge Kelvin (CBK) structure was used to extract ρ_C and was found to be $5 \times 10^{-6} \Omega \cdot \text{cm}^2$ at $n \sim 5 \times 10^{12} \text{ cm}^{-2}$ for a Ni contact. γ was extracted to be 1 μm even though the contact length (d) was 4 μm . Figure 3.21 shows calculated ρ_C for various d and L . For $d < \gamma$, contact resistance is determined by areal conduction whereas for $d > \gamma$, the

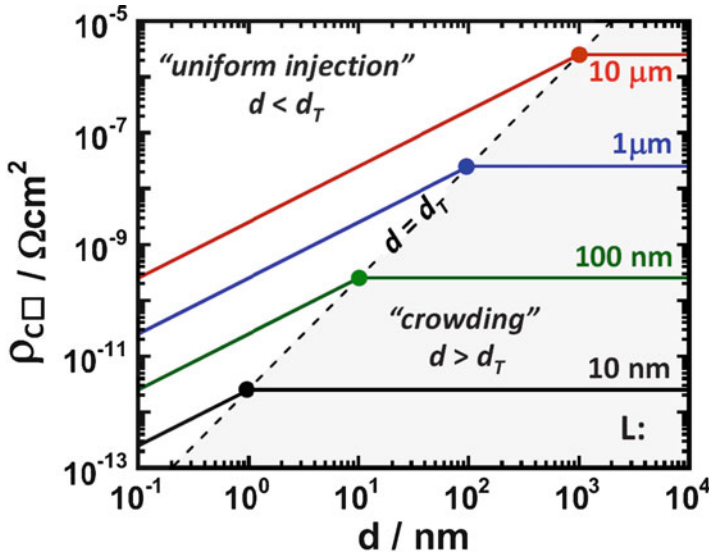


Fig. 3.21 Contact resistivity (ρ_C) versus d (contact length) for various L (source–drain distance). For $L \sim 10$ nm, the required ρ_C is orders of magnitude lower than experimentally reported results (Reproduced with permission from [84]. © 2010 American Institute of Physics)

conduction transitions to mostly edge conduction (“crowding”), and thus there is a saturation of ρ_C . The required value of ρ_C for $L \sim 10$ nm is seen to be less than $10^{-10} \Omega \text{ cm}^2$ under the assumption that contact resistance contributes to less than 10% of the overall channel resistance. Since the sheet resistance of graphene is lower than Si, the requirement for ρ_C is more stringent for graphene. The large work function difference between Ni and graphene causes a charge transfer to graphene, and thus reduces ρ_C . It was also argued that the gate-independence of R_C in [83] was because of the assumption that all metal-graphene contacts in that work were equivalent. In reality, this assumption was found to induce a large estimation error in R_C , and the CBK method is more reliable since a single graphene/metal contact is measured. A V_g dependence of ρ_C was found; this is consistent with previous findings of V_g dependence, for e.g. in [85], where ρ_C was 300–500 $\Omega \mu\text{m}$ for Ti contacts at $n \sim 3 \times 10^{12} \text{ cm}^{-2}$. The behavior is caused by the V_g dependence of DOS of graphene under the metal contact. Independently, it was found in [86] that the contact resistivity is 150–200 $\Omega\text{-}\mu\text{m}^2$ and the transfer length is 0.2–0.5 μm , for a Cr(0.5 nm)/Pd contact to graphene.

End-contact formation to epitaxial graphene was discussed in [87]. XPS of EG revealed the existence of C-O and C=O bonds on the graphene surface post metallization; this was attributed to resist residue. A low-power O_2 plasma treatment was used to improve contact resistance, Fig. 3.22. Even though graphene is found to degrade with increased plasma exposure, the contact resistance actually improves. For a 90s exposure, ρ_C decreases to $4 \times 10^{-7} \Omega \text{ cm}^2$. Beyond $t \sim 120$ s, ρ_C starts increasing, and Raman imaging shows a degradation of the 2D peak

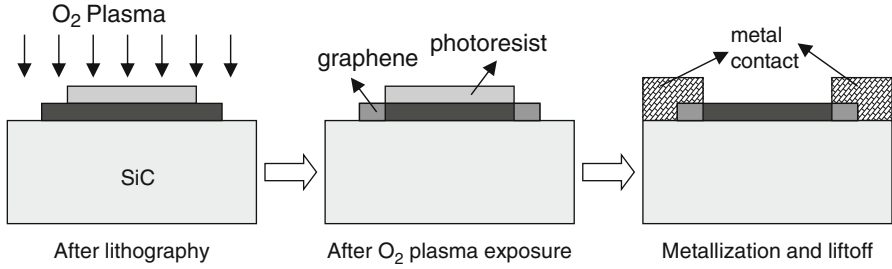


Fig. 3.22 A photoresist mask is patterned before electrode metallization; a low power O_2 plasma is used to “roughen” the exposed graphene. This is followed by a metallization and liftoff process.

intensity—this suggests that the majority of the sp^2 bonding has been destroyed. Note that the treated graphene is only that exposed to metal contacts, and not the channel region itself, which is covered by resist throughout the plasma exposure process. Further heat treatments at $450\text{--}475^\circ\text{C}$ for 15 min. reduce ρ_C further by 1.3–4X. A wide range of metals were used for the study—Al, Ti, Cu, Pd, Ni and Pt—but there was little difference in ρ_C for the different metals. This could be because the plasma treatment altered the pristine nature of graphene. It was also found that using Al and >15 nm of Pd or Pt as a contact metal results in severe delamination and using Cu results in nonuniform coverage. It has also been found that e-beam evaporated metallization results in a lower contact resistance than sputtered metallization. The sputter process was thought to create defects, and resulted in a 5X higher R_C than for the e-beam process. Increasing sputter power increased R_C . Multi-layer graphene showed an insensitive behavior to the type of metallization used; it was argued that the sputter process leaves the lower graphene layers intact in MLG and thus preserves the behavior of MLG.

In [88], Pd/Au contacts (25/25 nm) were found to result in a R_C of $230\text{--}900\ \Omega\text{-}\mu\text{m}$ for $V_g - V_{gmin}$ between -33 V and 0 V, for flaked graphene on 90 nm SiO_2 . In addition to a backgate dependence of R_C , a clear asymmetry between electron and hole conduction was observed, with R_C being higher in the n-branch. It was also observed that R_C reduces to from 185 to $120\ \Omega\text{-}\mu\text{m}$ ($V_g - V_{gmin} = -30$ V) when T decreases from 300 K to 6 K. Analysis of the experimental data combined with theoretical results revealed that carrier transport in graphene under Pd is almost ballistic, and the transmission efficiency is $\sim 75\%$ at 6 K. At room temperature, the transport is more diffusive, leading to a larger R_C . The ideal metal-graphene resistance was estimated to be $40\ \Omega\text{-}\mu\text{m}$ while the actual resistance is higher because the number of conduction modes in graphene underneath the metal is restricted by the metal-induced doping and broadening. In [48], for a 1 nm Cr/ 80 nm Au contact, R_C is found to be between 190 to $224\ \Omega\text{-}\mu\text{m}$, and scaled with width rather than contact area.

Electrical transport measurements average out any local variations and thus a complementary method is needed to study contact doping. In addition, because graphene transistors have been back gated in most experiments, the graphene under metal contacts goes through a transition in carrier type as the back gate potential is

varied; this creates additional complexity in extracting the true performance of graphene transistors. In [89], scanning photocurrent microscopy (SCPM) measurements were used to study the impact of electrical contacts. These measurements revealed the presence of potential steps that could act as potential barriers at the metal contacts. In [90], a high resolution photo current imaging was performed on backgated graphene devices by using a near-field scanning optical microscopy (NSOM) technique. The metal electrodes pin the Fermi level in graphene and create a potential step within the graphene sheet; Pd was found to introduce a p-doping of the graphene underneath. For $V_g < V_{gmin}$, conduction is mostly by holes, and a p-p junction forms near the graphene-electrode interface; for $V_g > V_{gmin}$, a p-n junction forms near this interface since the contact region still stays p-type. By using a diffusive transport model, it can be shown that a graphene p-n junction has a larger resistance than a p-p junction. Thus, contact doping contributes to an asymmetry between the electron- and hole-conduction regimes. It was also found that the charge-transfer doping from the electrodes extends hundreds of nanometers into adjacent regions of the graphene channel.

Ultimate monolithic integration in graphene will avoid the use of metal-graphene junctions, and use graphene for all parts of a circuit: all the way from transistors, to vias, contacts, and interconnects. This will avoid many of the issues faced by metal-graphene contacts but there are considerable challenges to implementing a monolithic graphene chip. Use of vertical graphene structures and CNTs for vias will likely be pursued for monolithic integration.

3.12 From Transistors to Circuits

While most graphene transistors have been demonstrated as discrete devices, there have been a few reports circuit demonstrations, including frequency multipliers, inverters and mixers.

Frequency Multipliers: Conventional frequency multipliers are either diode or FET based—the former offers good conversion efficiency (30%) but no gain while the latter offers gain but a lower efficiency (~15%). Ambipolar transport properties of graphene have been used to demonstrate full-wave signal rectification as well as frequency doubling [91]. By using a common source configuration, a sinusoidal voltage applied to the backgate was rectified at the drain electrode; a 10 kHz signal was demonstrated to double to 20 kHz with good spectral purity—this frequency is much less than the 1THz multipliers possible using Si diodes but points to the possibility of using graphene for this application.

Inverters: An early demonstration of a graphene inverter [92] required large gate voltages because of backgating with a thick oxide, and the voltage gain was <0.05 . In [93], top-gate stacks were prepared by a simple process but also afforded low-voltage operation. The inverters were operated at 2 V and showed a 4–7X gain, Fig. 3.23. A 30 nm Al top-gate was evaporated on top of graphene, without a

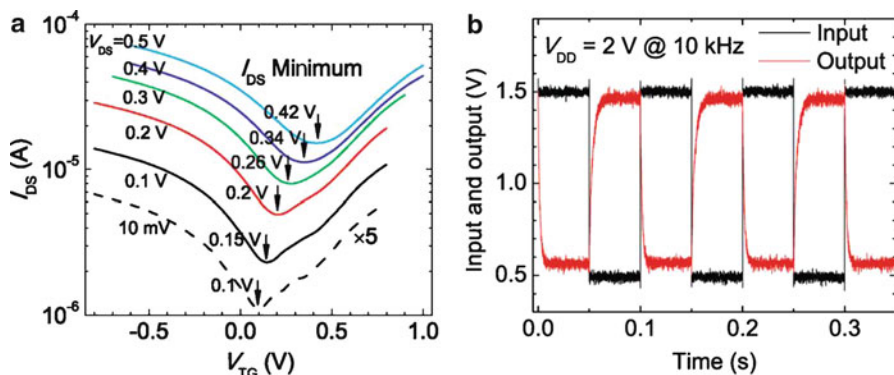


Fig. 3.23 (a) Shift of V_{gmin} with V_{ds} —this property is used to obtain n- and p-type GFETs; (b) dynamic response of SLG inverters (Reproduced with permission from [93]. © 2010 American Chemical Society)

dielectric in between. The device was exposed to air for many hours and a 4–8 nm passivation layer formed both on top of Al as well as at the graphene-metal interface—this was attributed to the diffusion of atmospheric oxygen. The leakage current from the top gate to graphene was found to be less than 0.2 nA, with a breakdown voltage of ~ 2.4 V. Complementary n- and p-type transistors were obtained by making use of the drain-voltage dependence of V_{gmin} ; it was observed that as V_{ds} increased from 0.1 V to 0.5 V, V_{gmin} shifts from 0.15 to 0.42 V. This was explained to be caused by the influence of V_{ds} on the channel—as V_{ds} increases, the channel potential increases and the effective gate-channel voltage decreases; thus V_g has to increase to introduce the same charge as before. The shift of the pull-up FET is always larger than that of the pull-down FET because of the upstream location of the pull-up FET. The static power dissipation was on the order of μ A because of the absence of a bandgap. In a related work [94] bilayer graphene was used to make inverters; the BLG FETs had an on-off ratio of 70 and 400 at 300 K and 77 K, respectively. A subthreshold slope of 140 mV/dec at 77 K was obtained (compared to more than 600 mV/dec for SLG). The BLG inverter showed a superior output voltage swing because of a better capacitive coupling and the presence of a bandgap. Inverter operation was demonstrated by setting $V_{bg} = -6$ V, and $V_{dd} \sim 1$ V. Frequencies up to 10 KHz were inverted with little degradation of the signal.

Mixers: Mixers are important components in RF communication systems, and are typically used for frequency conversion. The output component of interest is $f_{IF} = f_{RF} - f_{LO}$, where f_{RF} is the input RF frequency and f_{LO} is the input local oscillator frequency. CVD graphene was used to demonstrate a mixer up to 10 MHz [95]. An ideal GFET shows symmetric transfer characteristics that is infinitely differentiable; then the drain current can be described as:

$$I_d = a_0 + a_2(V_g - V_{gmin})^2 + a_4(V_g - V_{gmin})^4 + \dots$$

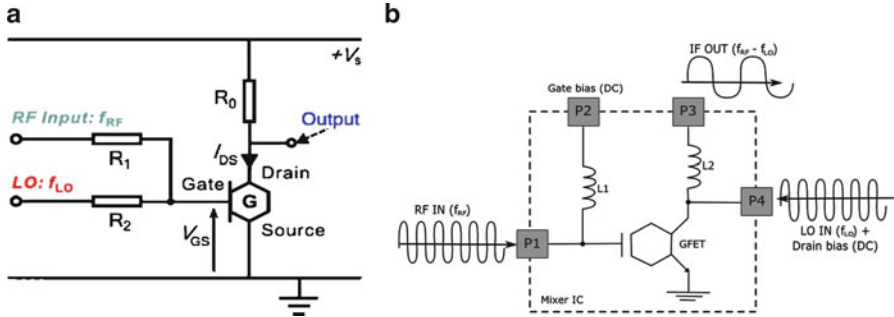


Fig. 3.24 Circuit implementation for GFET RF mixer (a) discrete CVD-grown GFET showed operation up to 10 MHz (Reproduced with permission from [95]. © 2010 IEEE). (b) Integrated epitaxial-graphene mixer operated at frequencies up to 10 GHz (Adapted from [96])

where a_0, a_2, a_4 are constants. From this model, ideal GFETs biased at V_{gmin} should show only the difference and sum frequencies and other even-order terms; thus, odd-order intermodulations can be significantly reduced compared to conventional unipolar mixers. Conventional mixers need more complicated circuits to achieve good performance while GFETs need to display symmetric characteristics but can use much simpler circuits. The implemented circuit using a GFET is shown in Fig. 3.24a. When two RF signals at 10 MHz and 10.5 MHz are applied to the gate, the GFET mixes them to generate $(f_{RF} + f_{LO})$ and $(f_{RF} - f_{LO})$ at the output. The power at these frequencies is more than 10 dB higher than the power at the input/fundamental frequencies. In addition, the power at the odd-order frequencies like $2f_{LO} - f_{RF}$ and $2f_{RF} - f_{LO}$ are significantly suppressed. The frequency limit can be calculated from $f_T = g_m / (2\pi C)$. In the studied devices, there was significant asymmetry in the transfer curves, perhaps because of contact doping or adsorbates. Since the device operation was within ± 1 V of V_{gmin} , the asymmetry in IV did not cause a noticeable degradation of the mixing operation.

The mixer used for the above demonstration was limited in frequency more by parasitics rather than GFET performance. An integrated mixer was demonstrated in [96] that could operate up to 10 GHz. The circuit was fabricated using graphene grown on SiC, and the footprint, including contact pads, was less than 1 mm^2 . The circuit implementation is shown in Fig. 3.24b. The GFET is modulated both by f_{RF} and f_{LO} , and the drain current contains the sum and difference frequencies. The inductors complement the GFET— L_1 resonates out the parasitic capacitances from the input RF pads and the gate of the GFET while L_2 provides an input match to the LO signal and also acts as a low-pass filter between the drain and output port P3. The graphene was 2–3 layers thick, and the Si-face of SiC was used. The $I_d - V_{gs}$ curve was linear and did not show a V_{gmin} —perhaps because of the strong n-type doping from the substrate. The output characteristics showed a linear $I_d - V_{ds}$ for V_{ds} upto 1.6 V. This resulted in a g_m that increased with rising V_{ds} . At $V_{ds} \sim 1.6$ V, a current density of $2 \text{ mA}/\mu\text{m}$ and g_m of $80 \mu\text{S}/\mu\text{m}$ was achieved. R_c was measured to be $600 \Omega\text{-}\mu\text{m}$. With the measured g_m and C_G , f_T is calculated to be 9 GHz for $L \sim 550 \text{ nm}$

and $V_{ds} = 1.6$ V. The drain current can be described as $I_d \sim A(B + g_m V_g) V_{ds}$ where A and B are constants. Since the output signal is proportional to I_d , the power of f_{IF} is proportional to the product of g_m and g_d . Current saturation was not achieved, and most devices showed a triode-like behavior. It was found that g_m slightly decreases with V_g ; this was also evident in the conversion loss of the mixer as a function of V_g . This strong correlation showed that the graphene mixer performance was determined by the GFET rather than by parasitics. The conversion loss of the graphene mixer showed good thermal stability when the temperature was increased from 300 K to 400 K. This was attributed to the degenerate doping level in the GFETs and a temperature-independent scattering mechanism associated with optical phonons at high biases. Conventional semiconductor mixers need additional feedback circuitry to minimize thermal sensitivity.

3.13 Non-classical Charge-Based Transistors

The unique bandstructure of graphene provides opportunities to construct charge-based switches with the potential of outperforming Si CMOS FETs. In this section, transistors based on three different physical phenomena will be discussed: Klein tunneling, Veselago lensing, and Zener tunneling.

Klein Tunneling: The transmission of relativistic particles through high and wide potential barriers is termed “Klein paradox.” Because of the chiral nature of the carriers in graphene, massless Dirac fermions allow for a possibility of realizing Klein tunneling in single layer graphene [97]. Massive chiral fermions in bilayer graphene offers a complementary system as will be discussed below. In Klein tunneling, an incoming electron starts penetrating through a potential barrier if the barrier height V_o is more than the electron’s rest energy mc^2 . Here T , the transmission probability, depends only weakly on V_o , and approaches 1 for very high barriers. In conventional tunneling, T exponentially decays with V_o . The physical mechanism responsible for this effect is the existence of positron states inside the barrier, which align in energy with the electron continuum outside, provided there is a sufficiently strong potential. Matching between the electron and positron wavefunctions across the barrier leads to a high T described by the Klein paradox. The required potential drop is mc^2 over the Compton length (h/mc) —this yields enormous electric fields ($>10^{16}$ V/cm).

Normally electron and hole physics are described by separate Schrodinger equations that are not in any way connected. But in graphene, electron and hole states are interconnected. Graphene’s quasiparticles have to be described by two-component wavefunctions to define relative contributions of sublattices A and B (a pseudospin index η connects the two components). The conical spectrum of graphene originates from the intersection of the energy bands from sublattices A and B; thus an electron with energy E propagating in the positive direction originates from the same branch of the electronic spectrum as a hole with energy $-E$

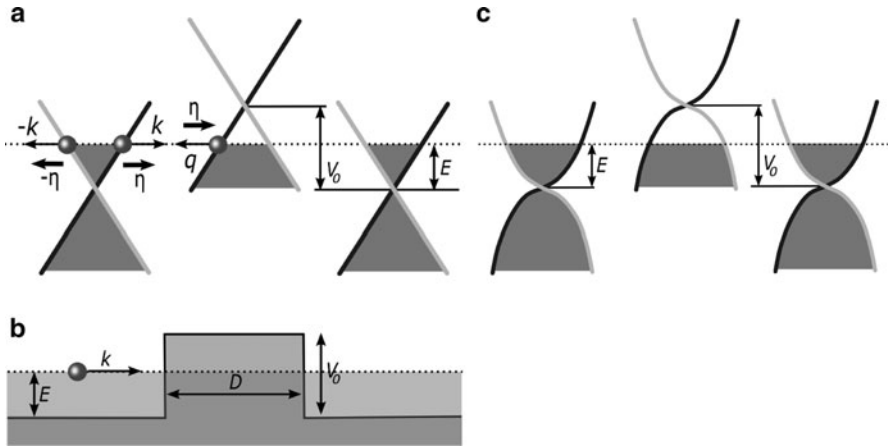


Fig. 3.25 The energy–momentum relationship can be assumed to be linear in graphene at low energies (<1 eV). The dark and light curves emphasize the origin of the spectrum—they denote the crossing of the energy bands associated with crystal sublattices A and B. (a) Band diagram for single-layer graphene—the pseudospin denoted by vector $\mathbf{n}$ is parallel (antiparallel) to the direction of motion of electrons (holes). (b) Potential barrier of width D , and height V_0 . The Fermi level is indicated as a dotted line. (c) Band spectrum of carriers in bilayer graphene (Adapted from [97])

propagating in the opposite direction. Thus, electrons and holes belonging to the same branch have a pseudospin pointing in the same direction—the direction of the pseudospin is parallel to the momentum for electrons and antiparallel to holes. Chirality is the projection of pseudospin on the direction of motion, and is positive for electrons and negative for holes, Fig. 3.25.

To model carrier transmission into the barrier, infinitely sharp edges are assumed for the barrier; such a barrier could be created by field-effect through a thin insulator. Since Dirac fermions in graphene are massless, there is no theoretical requirement on the electric field required to form positron-like states under the barrier. Conservation of pseudospin can be used to understand Klein tunneling in graphene, Fig. 3.25. Pseudo-spin flipping processes are rare since they require a short-range potential that would act differently on the A and B sites of the graphene lattice. Thus, an electron moving to the right can be scattered only to a right-moving electron or a left-moving hole state. This requirement for matching of pseudospin for quasiparticles inside and outside the barrier results in perfect tunneling. The angle-dependent scattering for SLG and BLG is shown in Fig. 3.26. Charge carriers in BLG have a parabolic energy spectrum, which means that they are massive quasiparticles with a finite DOS at zero energy. But these quasiparticles are also chiral but $T \sim 0$ at normal incidence in BLG; this seems to be because charge conjugation requires a propagating electron with wavevector $\mathbf{k}$ to transform into a hole with wavevector $i\mathbf{k}$ (rather than $-\mathbf{k}$) which is an evanescent wave inside a barrier. This small transmission can be exploited to create BLG Klein tunneling FETs. The angle of incidence of

Fig. 3.26 Transmission probability as a function of the incident angle for (a) single-layer and (b) bilayer graphene. Inside the barrier the electron concentration is $5 \times 10^{11} \text{ cm}^{-2}$, while the hole concentration is 10^{12} cm^{-2} . The barrier width is 100 nm while the height is (a) 200 meV, and (b) 50 meV. Adapted from [97]

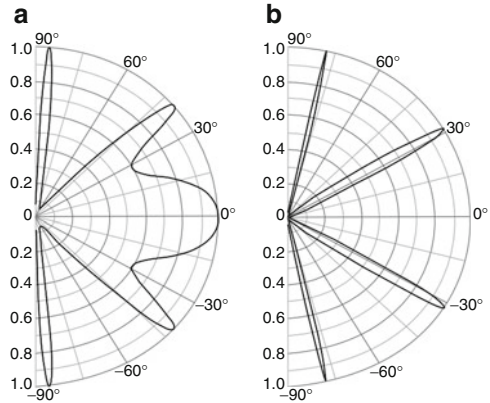
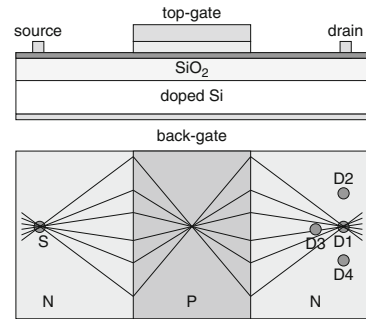


Fig. 3.27 Electron veselago lens. The central p-region is modulated by a top-gate while the entire graphene layer can be modulated by the back-gate. The top-gate voltage can be used to control the focusing of carriers from the pair of leads SD1 to either SD2, SD3 or SD4. Adapted from [98]



carriers will have a significant impact on the transmission and hence the on/off ratio. Methods to inject collimated carriers include the use of point-contact junctions and super-lattice structures.

Veselago Lens: Focusing of carriers by a single p-n junction in graphene has been predicted [98]. Fine-tuning the carrier density on the n- and p-side allows precise focusing. This concept can be used to turn a n-p-n junction into a Veselago lens for electrons. The density of carriers in the p-region is controlled by a top-gate. When the densities in p- and n-regions are equal, charge carriers injected into graphene would meet again in the focus at a distance $2w$ from the source. Varying V_g over the p-region enables the transformation of the focus into a cusp displaced by about $2(\ln l - 1)w$ along the x-axis and thus to shift the strong coupling from the pair of leads SD1, to SD2, SD3 or SD4, Fig. 3.27. The concept can be used to also create beam splitters. A reconfigurable logic device based on the Veselago lens was proposed in [99]. Electrostatic doping is used to define coplanar split-gates beneath a graphene sheet. By applying opposite biases to the split gates, pn junctions are formed. The transmission probability across the pn interface is given as

$$T(\theta) = \cos^2(\theta) \cdot \exp(-\pi k_F d \cdot \sin^2(\theta))$$

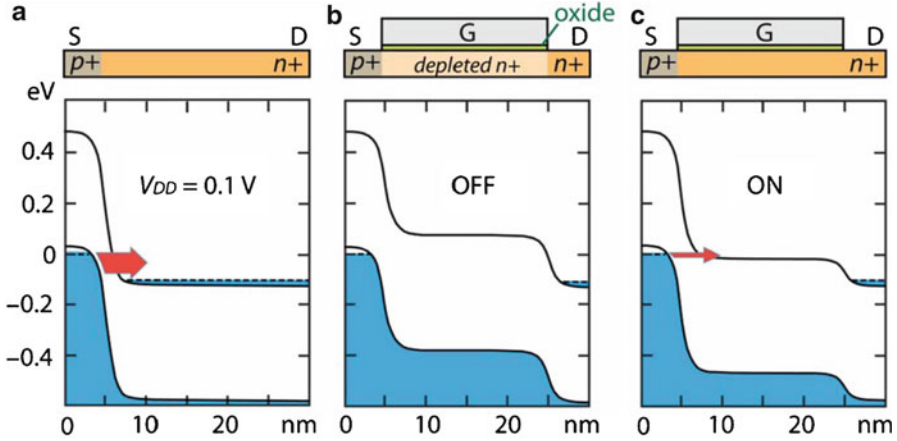


Fig. 3.28 Energy band diagram for a TFET consisting of an p + source (S), and n + drain (D). In (a) the Zener tunneling channel is shown under 0.1-V bias (*without a gate*). In (b), the gate fully depletes the channel at zero gate potential creating a normally off state. In (c), a positive gate voltage turns the channel on with current set by the overlap of valence band electrons with unfilled conduction band states (Reproduced with permission from [100]. © 2010 IEEE)

where k_F is the Fermi wave vector, θ is the incident angle between the electron wave vector and interface, and d is the gap of the p-n interface. Given reasonable values for d and k_F , the critical angle for T_{IR} is 45° , yielding an on/off ratio of 10^3 – 10^5 . Thus, the device can be tuned from the on to off state by switching the n-n interface to the angle-dependent p-n interface.

Tunnel FET: The operation of a TFET is explained in Fig. 3.28. A GNR with a significant bandgap is assumed for the operation. Abrupt p⁺n⁺ junctions are assumed along with a small drain bias. Zener tunneling from valence band to conduction band contributes to the channel current. To achieve enhancement mode operation, the gate workfunction needs to be tuned to the p⁺n⁺ junction; in addition the gate needs to fully deplete the channel. A positive V_g triggers Zener tunneling; the gate bias lowers the vertical field normal to the gate; this might contribute to a better channel mobility. Simulations show [100] that GNR TFETs could achieve on-current of more than $200 \mu\text{A}/\mu\text{m}$ with a V_{dd} of 0.1 V and an off-current of $0.1 \mu\text{A}/\mu\text{m}$. The 1D Zener tunneling current is calculated by integrating the product of charge flux and tunneling probability from the Fermi energy level at the p + side to the n + side. Simulations show that with a reverse bias of 0.1 V, GNR tunnel junctions can achieve a current density of $1 \text{ mA}/\mu\text{m}$. Narrower bandgap materials with smaller effective mass can achieve higher tunneling current; thus, GNRs are predicted to show four orders of magnitude higher current than Si. Use of bilayer graphene permits the implementation of TFETs without the need for lithography because of the bandgap achievable with asymmetric fields; simulations show that on-off ratios of more than 1,000 are possible, with a supply voltage of only 0.1 V.

3.14 Summary

Graphene transistors based on traditional FET structures are attractive because of the high carrier mobility. Considering progress to date, GFETs are more suitable for RF applications since they do not require a bandgap. For digital applications, it remains to be seen if GFETs with bandgaps can outperform Si FETs. A number of device-related challenges need to be addressed before GFETs can be integrated into mainstream circuits; these include contact resistance, doping, and scattering from edge, dielectrics, and substrate.

References

1. K. S. Novoselov, *et al.*, “Two-dimensional gas of massless Dirac fermions in graphene,” *Nature*, vol. 438, pp. 197–200 (2005).
2. K. S. Novoselov, *et al.*, “Electric field effect in atomically thin carbon films,” *Science*, vol. 306, pp. 666–669 (2004).
3. C. Berger, *et al.*, “Electronic confinement and coherence in patterned epitaxial graphene,” *Science*, vol. 312, pp. 1191–1196 (2006).
4. F. N. Xia, D. B. Farmer, Y. M. Lin, and P. Avouris, “Graphene Field-Effect Transistors with High On/Off Current Ratio and Large Transport Band Gap at Room Temperature,” *Nano Letters*, vol. 10, pp. 715–718 (2010).
5. T. Fang, A. Konar, H. L. Xing, and D. Jena, “Carrier statistics and quantum capacitance of graphene sheets and ribbons,” *Applied Physics Letters*, vol. 91, 092109 (2007).
6. W. Zhu, V. Perebeinos, M. Freitag, and P. Avouris, “Carrier scattering, mobilities, and electrostatic potential in monolayer, bilayer, and trilayer graphene,” *Physical Review B*, vol. 80, 235402 (2009).
7. G. Baccarani, M. R. Wordeman, and R. H. Dennard, “Generalized Scaling Theory and Its Application to a 1/4 Micrometer Mosfet Design,” *IEEE Transactions on Electron Devices*, vol. 31, pp. 452–462 (1984).
8. S. I. Association, “International Technology Roadmap for Semiconductors,” (2007).
9. S. W. Keckler, *et al.*, “A wire-delay scalable microprocessor architecture for high performance systems,” *2003 IEEE International Solid-State Circuits Conference*, vol. 46, pp. 168–169 (2003).
10. D. Geer, “Chip makers turn to multicore processors,” *Computer*, vol. 38, pp. 11–13 (2005).
11. D. Hisamoto, *et al.*, “FinFET - A self-aligned double-gate MOSFET scalable to 20 nm,” *IEEE Transactions on Electron Devices*, vol. 47, pp. 2320–2325 (2000).
12. K. Boucart and A. M. Ionescu, “Double-gate tunnel FET with high-K gate dielectric,” *IEEE Transactions on Electron Devices*, vol. 54, pp. 1725–1733 (2007).
13. K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, “Impact ionization MOS (I-MOS) - Part I: Device and circuit simulations,” *IEEE Transactions on Electron Devices*, vol. 52, pp. 69–76 (2005).
14. S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices,” *Nano Letters*, vol. 8, pp. 405–410 (2007).
15. R. Murali, *et al.*, “Breakdown current density of graphene nanoribbons,” *Applied Physics Letters*, vol. 94, (2009).
16. R. Murali, *et al.*, “Resistivity of Graphene Nanoribbon Interconnects,” *IEEE Electron Device Letters*, vol. 30, pp. 611–613 (2009).

17. M. Y. Han, B. Ozyilmaz, Y. B. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Physical Review Letters*, vol. 98, 206805 (2007).
18. S. Y. Zhou, *et al.*, "Substrate-induced bandgap opening in epitaxial graphene," *Nature Materials*, vol. 6, pp. 770–775 (2007).
19. M. Sprinkle, *et al.*, "Scalable templated growth of graphene nanoribbons on SiC," *Nature Nanotechnology*, vol. 5, pp. 727–731 (2010).
20. J. W. Bai, *et al.*, "Graphene nanomesh," *Nature Nanotechnology*, vol. 5, pp. 190–194 (2010).
21. E. Rotenberg, *et al.*, "Origin of the energy bandgap in epitaxial graphene," *Nature Materials*, vol. 7, pp. 258–259 (2008).
22. F. Schwierz, "Graphene transistors," *Nature Nanotechnology*, vol. 5, pp. 487–496 (2010).
23. J. S. Moon, *et al.*, "Top-Gated Epitaxial Graphene FETs on Si-Face SiC Wafers With a Peak Transconductance of 600 mS/mm," *IEEE Electron Device Letters*, vol. 31, pp. 260–262 (2010).
24. Y.-M. Lin, *et al.*, "100-GHz Transistors from Wafer-Scale Epitaxial Graphene," *Science*, vol. 327, 662 (2010).
25. K. A. Jenkins, *et al.*, "Graphene RF Transistor Performance," *ECS Transactions*, vol. 28, pp. 3–13 (2010).
26. G. C. Liang, N. Neophytou, D. E. Nikonov, and M. S. Lundstrom, "Performance projections for ballistic graphene nanoribbon field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 54, pp. 677–682 (2007).
27. A. C. Ford, *et al.*, "Diameter-Dependent Electron Mobility of InAs Nanowires," *Nano Letters*, vol. 9, pp. 360–365 (2009).
28. D. A. Areshkin, D. Gunlycke, and C. T. White, "Ballistic transport in graphene nanostrips in the presence of disorder: Importance of edge effects," *Nano Letters*, vol. 7, pp. 204–210 (2007).
29. D. Gunlycke, D. A. Areshkin, and C. T. White, "Semiconducting graphene nanostrips with edge disorder," *Applied Physics Letters*, vol. 90, 142104 (2007).
30. T. Fang, A. Konar, H. Xing, and D. Jena, "Mobility in semiconducting graphene nanoribbons: Phonon, impurity, and edge roughness scattering," *Physical Review B*, vol. 78, 205403 (2008).
31. Y. X. Yang and R. Murali, "Impact of Size Effect on Graphene Nanoribbon Transport," *IEEE Electron Device Letters*, vol. 31, pp. 237–239 (2010).
32. K. I. Bolotin, *et al.*, "Ultrahigh electron mobility in suspended graphene," *Solid State Communications*, vol. 146, pp. 351–355 (2008).
33. J. H. Chen, *et al.*, "Intrinsic and extrinsic performance limits of graphene devices on SiO₂," *Nature Nanotechnology*, vol. 3, pp. 206–209 (2008).
34. Y. W. Tan, *et al.*, "Measurement of scattering rate and minimum conductivity in graphene," *Physical Review Letters*, vol. 99, 246803 (2007).
35. A. A. Balandin, *et al.*, "Superior thermal conductivity of single-layer graphene," *Nano Letters*, vol. 8, pp. 902–907 (2008).
36. X. R. Wang, *et al.*, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Physical Review Letters*, vol. 100, 206803 (2008).
37. D. V. Kosynkin, *et al.*, "Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons," *Nature*, vol. 458, pp. 872–876 (2009).
38. L. Jiao, *et al.*, "Narrow graphene nanoribbons from carbon nanotubes," *Nature*, vol. 458, pp. 877–880 (2009).
39. J. Cai, *et al.*, "Atomically precise bottom-up fabrication of graphene nanoribbons," *Nature*, vol. 466, pp. 470–473 (2010).
40. H. Xiang, *et al.*, "'Narrow' Graphene Nanoribbons Made Easier by Partial Hydrogenation," *Nano Letters*, vol. 9, pp. 4025–4030 (2009).
41. D. C. Elias, *et al.*, "Control of Graphene's Properties by Reversible Hydrogenation: Evidence for Graphane," *Science*, vol. 323, pp. 610–613 (2009).

42. R. Balog, *et al.*, “Bandgap opening in graphene induced by patterned hydrogen adsorption,” *Nature Materials*, vol. 9, pp. 315–319 (2010).
43. J. R. Williams, T. Low, M. S. Lundstrom, and C. M. Marcus, “Gate-controlled guiding of electrons in graphene,” *Nature Nanotechnology*, vol. 6, pp. 222–225 (2011).
44. X. Wang and H. Dai, “Etching and narrowing of graphene from the edges,” *Nature Chemistry*, vol. 2, pp. 661–665 (2010).
45. L. C. Campos, *et al.*, “Anisotropic Etching and Nanoribbon Formation in Single-Layer Graphene,” *Nano Letters*, vol. 9, pp. 2600–2604 (2009).
46. S. S. Datta, D. R. Strachan, S. M. Khamis, and A. T. C. Johnson, “Crystallographic Etching of Few-Layer Graphene,” *Nano Letters*, vol. 8, pp. 1912–1915 (2008).
47. Z. Chen and J. Appenzeller, “Mobility Extraction and Quantum Capacitance Impact in High Performance Graphene Field-effect Transistor Devices,” *IEEE International Electron Devices Meeting*, pp. 509–512 (2008).
48. I. Meric, *et al.*, “Channel Length Scaling in Graphene Field-Effect Transistors Studied with Pulsed Current–voltage Measurements,” *Nano Letters*, vol. 11, pp. 1093–1097 (2011).
49. Y. Ouyang, H. Dai, and J. Guo, “Projected performance advantage of multilayer graphene nanoribbons as a transistor channel material,” *Nano Research*, vol. 3, pp. 8–15 (2010).
50. Y. Sui and J. Appenzeller, “Screening and Interlayer Coupling in Multilayer Graphene Field-Effect Transistors,” *Nano Letters*, vol. 9, pp. 2973–2977 (2009).
51. J. Hass, *et al.*, “Why multilayer graphene on 4 H-SiC(000(1)over-bar) behaves like a single sheet of graphene,” *Physical Review Letters*, vol. 100, 125504 (2008).
52. J. Martin, *et al.*, “Observation of electron–hole puddles in graphene using a scanning single-electron transistor,” *Nature Physics*, vol. 4, pp. 144–148 (2008).
53. S. M. Sze, *Physics of Semiconductor Devices*: Wiley-Interscience, 1981.
54. F. Schedin, *et al.*, “Detection of individual gas molecules adsorbed on graphene,” *Nature Materials*, vol. 6, pp. 652–655 (2007).
55. P. L. Levesque, *et al.*, “Probing Charge Transfer at Surfaces Using Graphene Transistors,” *Nano Letters*, vol. 11, pp. 132–137 (2010).
56. Y. Dan, *et al.*, “Intrinsic Response of Graphene Vapor Sensors,” *Nano Letters*, vol. 9, pp. 1472–1475 (2009).
57. M. Ishigami, *et al.*, “Atomic structure of graphene on SiO₂,” *Nano Letters*, vol. 7, pp. 1643–1648 (2007).
58. M. Laffkioti, *et al.*, “Graphene on a Hydrophobic Substrate: Doping Reduction and Hysteresis Suppression under Ambient Conditions,” *Nano Letters*, vol. 10, pp. 1149–1153 (2010).
59. Z. Liu, A. A. Bol, and W. Haensch, “Large-Scale Graphene Transistors with Enhanced Performance and Reliability Based on Interface Engineering by Phenylsilane Self-Assembled Monolayers,” *Nano Letters*, vol. 11, pp. 523–528 (2010).
60. C. R. Dean, *et al.*, “Boron nitride substrates for high-quality graphene electronics,” *Nature Nanotechnology*, vol. 5, pp. 722–726 (2010).
61. X. Hong, *et al.*, “High-Mobility Few-Layer Graphene Field Effect Transistors Fabricated on Epitaxial Ferroelectric Gate Oxides,” *Physical Review Letters*, vol. 102, 136808 (2009).
62. F. Chen, J. L. Xia, and N. J. Tao, “Ionic Screening of Charged-Impurity Scattering in Graphene,” *Nano Letters*, vol. 9, pp. 1621–1625 (2009).
63. F. Chen, J. Xia, and N. Tao, “Ionic Screening of Charged-Impurity Scattering in Graphene,” *Nano Letters*, vol. 9, pp. 1621–1625 (2009).
64. B. Guo, *et al.*, “Controllable N-Doping of Graphene,” *Nano Letters*, vol. 10, pp. 4975–4980 (2010).
65. D. B. Farmer, *et al.*, “Chemical Doping and Electron–hole Conduction Asymmetry in Graphene Devices,” *Nano Letters*, vol. 9, pp. 388–392 (2009).
66. A. Kasry, *et al.*, “Chemical Doping of Large-Area Stacked Graphene Films for Use as Transparent, Conducting Electrodes,” *ACS Nano*, vol. 4, pp. 3839–3844 (2010).
67. Y. Shi, *et al.*, “Work Function Engineering of Graphene Electrode via Chemical Doping,” *ACS Nano*, vol. 4, pp. 2689–2694 (2010).

68. F. Gunes, *et al.*, "Layer-by-Layer Doping of Few-Layer Graphene Film," *ACS Nano*, vol. 4, pp. 4595–4600 (2010).
69. C. Coletti, *et al.*, "Charge neutrality and band-gap tuning of epitaxial graphene on SiC by molecular doping," *Physical Review B*, vol. 81, 235401 (2010).
70. W. Chen, *et al.*, "Surface Transfer p-Type Doping of Epitaxial Graphene," *Journal of the American Chemical Society*, vol. 129, pp. 10418–10422 (2007).
71. I. Gierz, *et al.*, "Atomic Hole Doping of Graphene," *Nano Letters*, vol. 8, pp. 4603–4607 (2008).
72. X. R. Wang, *et al.*, "N-Doping of Graphene Through Electrothermal Reactions with Ammonia," *Science*, vol. 324, pp. 768–771 (2009).
73. S. Ryu, *et al.*, "Reversible Basal Plane Hydrogenation of Graphene," *Nano Letters*, vol. 8, pp. 4597–4602 (2008).
74. M. J. Loboda, C. M. Grove, and R. F. Schneider, "Properties of a-SiO_x : H thin films deposited from hydrogen silsesquioxane resins," *Journal of the Electrochemical Society*, vol. 145, pp. 2861–2866 (1998).
75. K. Brenner and R. Murali, "Single step, complementary doping of graphene," *Applied Physics Letters*, vol. 96, 063104 (2010).
76. H. J. Lee, *et al.*, "Structural comparison of hydrogen silsesquioxane based porous low-k thin films prepared with varying process conditions," *Chemistry of Materials*, vol. 14, pp. 1845–1852 (2002).
77. M. Cheli, P. Michetti, and G. Iannaccone, "Model and Performance Evaluation of Field-Effect Transistors Based on Epitaxial Graphene on SiC," *IEEE Transactions on Electron Devices*, vol. 57, pp. 1936–1941 (2010).
78. H. Wang, *et al.*, "Compact Virtual-Source Current–voltage Model for Top- and Back-Gated Graphene Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 58, pp. 1523–1533 (2011).
79. Y. Ouyang, Y. Yoon, and J. Guo, "Scaling behaviors of graphene nanoribbon FETs: A three-dimensional quantum simulation study," *IEEE Transactions on Electron Devices*, vol. 54, pp. 2223–2231 (2007).
80. K. Nagashio and A. Toriumi, "DOS-limited contact resistance in graphene FETs," *arxiv*, 1104.1818 (2011).
81. B. Huard, N. Stander, J. A. Sulpizio, and D. Goldhaber-Gordon, "Evidence of the role of contacts on the observed electron–hole asymmetry in graphene," *Physical Review B*, vol. 78, 121402 (2008).
82. S. Russo, *et al.*, "Contact resistance in graphene-based devices," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 42, pp. 677–679 (2010).
83. A. Venugopal, L. Colombo, and E. M. Vogel, "Contact resistance in few and multilayer graphene devices," *Applied Physics Letters*, vol. 96, pp. 013512–3 (2010).
84. K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact," *Applied Physics Letters*, vol. 97, pp. - (2010).
85. P. Blake, *et al.*, "Influence of metal contacts and charge inhomogeneity on transport properties of graphene near the neutrality point," *Solid State Communications*, vol. 149, pp. 1068–1071 (2009).
86. K. L. Grosse, *et al.*, "Nanoscale Joule heating, Peltier cooling and current crowding at graphene-metal contacts," *Nature Nanotechnology*, vol. 6, pp. 287–290 (2011).
87. J. A. Robinson, *et al.*, "Contacting graphene," *Applied Physics Letters*, vol. 98, pp. 053103–3 (2011).
88. F. Xia, *et al.*, "The origins and limits of metal-graphene junction resistance," *Nature Nanotechnology*, vol. 6, pp. 179–184 (2011).
89. E. J. H. Lee, *et al.*, "Contact and edge effects in graphene devices," *Nature Nanotechnology*, vol. 3, pp. 486–490 (2008).
90. F. N. Xia, *et al.*, "Photocurrent Imaging and Efficient Photon Detection in a Graphene Transistor," *Nano Letters*, vol. 9, pp. 1039–1044 (2009).

91. H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene Frequency Multipliers," *IEEE Electron Device Letters*, vol. 30, pp. 547–549 (2009).
92. F. Traversi, V. Russo, and R. Sordan, "Integrated complementary graphene inverter," *Applied Physics Letters*, vol. 94, 223312 (2009).
93. S. L. Li, *et al.*, "Low Operating Bias and Matched Input–output Characteristics in Graphene Logic Inverters," *Nano Letters*, vol. 10, pp. 2357–2362 (2010).
94. S. L. Li, *et al.*, "Enhanced Logic Performance with Semiconducting Bilayer Graphene Channels," *ACS Nano*, vol. 5, pp. 500–506 (2011).
95. H. Wang, *et al.*, "Graphene-Based Ambipolar RF Mixers," *IEEE Electron Device Letters*, vol. 31, pp. 906–908 (2010).
96. Y. M. Lin, *et al.*, "Wafer-Scale Graphene Integrated Circuit," *Science*, vol. 332, pp. 1294–1297 (2011).
97. M. I. Katsnelson, K. S. Novoselov, and A. K. Geim, "Chiral tunnelling and the Klein paradox in graphene," *Nature Physics*, vol. 2, pp. 620–625 (2006).
98. V. V. Cheianov, V. Fal'ko, and B. L. Altshuler, "The Focusing of Electron Flow and a Veselago Lens in Graphene p-n Junctions," *Science*, vol. 315, pp. 1252–1255 (2007).
99. S. Tanachutiwat, J. U. Lee, W. Wang, and C. Y. Sung, "Reconfigurable multi-function logic based on graphene P-N junctions," presented at the Proceedings of the 47th Design Automation Conference, Anaheim, California, 2010.
100. A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol. 98, pp. 2095–2110 (2010).

Chapter 4

Alternative State Variables for Graphene Transistors

Kosmas Galatsis, Alexander Shailos, Ajey P. Jacob, and Kang L. Wang

4.1 Introduction

October 2004 marked the discovery of single layer graphene as well as its first use as an FET channel material [1]. This epic discovery of a new class of two-dimensional material garnered so much scientific excitement and subsequent advancement, that it ultimately led to Novoselov and Geim being awarded the 2010 Noble Prize in Physics. Graphene's potential stems from its ability to not only accommodate electron charge based devices, but also an impressive array of other realized and proposed devices based on spin, phonons, photons, pseudospin as well as some more exotic devices based on alternate state variables. This chapter will introduce the reader to graphene devices based on these alternative state variables.

Irrespective of the material employed or device conceived, fundamentally, the operation, manipulation and processing of information (as represented by a state variable) is ultimately required to undertake any form of information processing. In the crudest sense, binary information can be thought of being represented by two distinguishable states; read, write and erase operations enable initialization and switching from one state to the other. The term “state variables” is used to denote the enabling physical representations of these states [2]. In addition, information is also required to be transmitted from one physical location to another. The performance of any information processing system is governed by limits set by fundamental physics (i.e. physical constants such as the speed of light and various quantum mechanical principles), material limits (such as thermal conductivity, defects, mobility, dielectric constant and saturation velocity), device design

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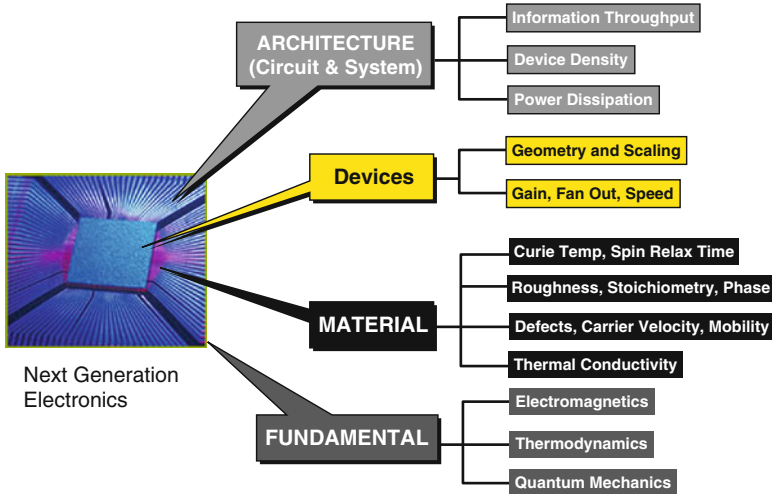


Fig. 4.1 A view of the various limits that bind the performance of any information processing system

(such as gain, fan-out and parasitic effects) and manufacturing advancements (such as yield, critical dimensions and line edge roughness). This hierarchy was best described by Meindl’s work in the 1990s [3] and shown in Fig. 4.1.

Alternative state variables beyond electronic charge are already widely used. Examples include (a) magnetism (magnetic spin domains) used in magnetic data storage and computer disk drives, (b) chalcogenide phase-change-based memory technology that makes up CD and DVD technology and (c) photons that are ubiquitous in high throughput optical communication systems. It should be noted that in all cases, information processing still takes place in the charge-based domain. This clearly shows that although alternate state variables have found applications in memory and high speed data transfer, information processing through logic functionality is still dominated by “electronics.” With the projected scaling saturation of CMOS at about 10 nm [4], a number of alternative logic devices are being pursued that have the potential to go beyond the CMOS scaling limit [5]. Since the discovery of its superior electronic and physical properties, graphene has been a “playground” for scientists to explore alternative state-variable-enabled devices. As such, this chapter will explore some of the following interesting examples:

- Graphene FET devices based on electronic charge
- Graphene atomic switches using molecular charge
- Spin FETs based on spin domains
- Pseudospin state variable enabled via the Bilayer Pseudospin Field-Effect Transistor (BiSFET)
- Phonon state variable enabled via graphene based Thermal Logic

4.2 Electronic Charge in Graphene

The drive to realizing graphene in 2004 was motivated by the promise of obtaining superior electronic properties beyond conventional silicon technology [1]. The most cited electronic property of graphene is its mobility. Upper mobility limits of $10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ of suspended graphene have been reported [6]. When implementing FETs, graphene nanoribbons (GNR) with a finite bandgap are usually employed to enable charge modulation via field effect electrostatics. A bandgap in graphene is usually obtained by patterning it into nanoribbons, where energy gaps of up to 0.3 eV for 10 nm widths have been measured [7]. However, canonical fabrication processes used to make graphene nanoribbons compromise carrier mobility. For example, 1–10 nm width nanoribbons have shown to exhibit a mobility less than $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [8]. As the nanoribbon width is reduced, edge states dominate electron transport, resulting in a reduced mobility. In addition, electron energy levels increase, which increases gate leakage current [9]. Another challenge facing digital graphene FET devices is a large contact resistance between graphene and metal contacts (at about 1,000 Ω). This is many times higher than that of silicon MOSFETs [10]. Because of these shortfalls, graphene may not be the ideal candidate for “digital” charge-based electronics; but graphene is still suitable for use in radio frequency (RF) FET transistors because RF transistors don’t necessarily need to be turned completely off. The fastest graphene transistor currently has a 140-nm gate length and a cut-off frequency of $f_T = 300 \text{ GHz}$ [11].

Fundamentally however, both graphene and conventional silicon FET device implementations are ultimately limited by the nature of switching using electronic charge, which in the simplest form can be approximated by a capacitor. The energy dissipated in charging and discharging (one full cycle) a capacitor, C , is given by $E_{\text{dissipated}} = CV^2 = NqV_{DD}$, where V_{DD} is the supply voltage. In the ideal case, only one electron would need to be switched, $N = 1$, which would reduce the energy dissipation to only qV_{DD} , which in this case is directly a function of V_{DD} . It has been shown that the fundamental minimum switching energy dissipated for a single electron in equilibrium with the thermal bath is $kT \ln 2 = 0.017 \text{ eV}$, presented by Landauer’s bistable potential well method [12–14], Shannon’s Channel Capacity Theorem [15], the ideal MOSFET Model [3, 16, 17] and thermodynamic derivations [17–19]. This is valid given the condition that the switching time, $\tau_{\text{switch}} \gg T_I$, where T_I is the electron energy relaxation time. Taking into account the energy relaxation, the minimum energy is $\alpha T_I/2 + kT \ln 2$, where $\alpha = qV_{DD}/\tau_{\text{switch}}$ [2]. This formula is derived by analyzing the evolution of a generic two-level quantum [20–22]. According to ITRS [23], a single MOS transistor will be capable of operating at a frequency of 12.5 THz, corresponding to 0.08 ps switching time, which is faster than the 1 ps electron relaxation time in Si. One should note however, that the energy stored in the gate capacitances in conventional CMOS integrated circuits is mostly dissipated in the resistance of the clock and drive metal interconnects, where relaxation times are as fast as 10 fs. With regards to the material medium of graphene, where ballistic transport takes

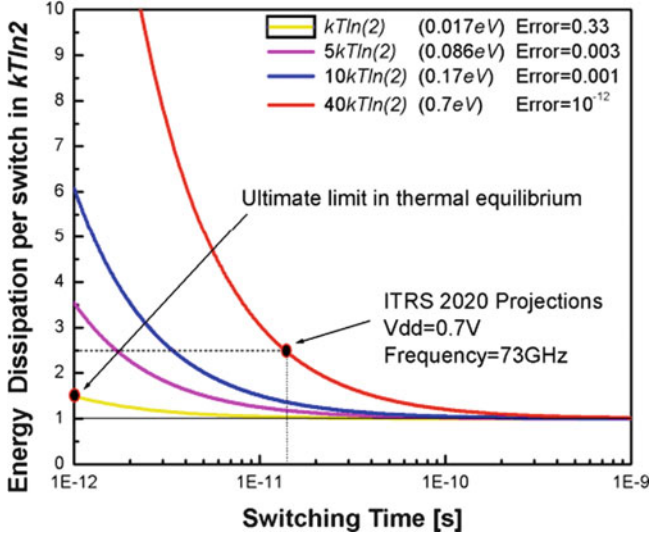


Fig. 4.2 Energy dissipation versus switching time for different energy separation (different error rates). The energy dissipation exponentially increases and the dynamic term dominates beyond 32 GHz (Reproduced with permission from [2]. © 2009 IEEE)

place, heat dissipation still occurs at the contact points. The most significant performance parameter of a logic gate is the average power that it dissipates in order to operate at the maximum clock rate. Figure 4.2 illustrates the substantial increase in energy dissipation as a result of faster switching and the trade-off that relates V_{DD} , switching speed, and energy dissipation.

With respect to an ultimately scaled charge-based graphene transistor for digital operation, the minimum nanoribbon size will mostly depend on the required bandgap. To estimate the ultimate density of charge-based transistors in graphene, an electron-in-a-well model can be used. For the quantum well in one and two dimensions, there is always a bound state. However, for a quantum well in three dimensions with a finite energy barrier, the existence of the bound state is governed by the relation between the well width a and energy barrier height $E_{barrier}$; the minimum size of the well for the given barrier height is given by:

$$a = \frac{\pi\hbar}{2\sqrt{2E_{barrier}m_{eff}}}$$

This is an ultimate limit; for reliable device operation at a finite temperature, one would require the quantum well width to be larger. For the typical energy scale in a graphene nanoribbon on the order of 0.3 eV and effective electron mass of about $m_{eff} = 0.01m_e$ [24] where m_e is a free electron mass, one can approximate the minimal possible well size to be less than 1 nm. Other estimates invoking Heisenberg uncertainty relations provide a gate (barrier) length of several nm

(electron in a well model) [18] while others consider the ultimate limit to be restricted by the fundamental building blocks of matter such the size of a carbon atom [25]. Assuming the latter (single atom and ignoring interconnection area requirements), and also assuming Boolean information to be represented by the altering charge population within a physical system consisting of two bound carbon atoms, such a scenario will occupy an area less than 1×1 nm.

4.3 Atomic Switches Using Graphene

Molecular-based switching offer unique advantages beyond electronic charge because of the much larger mass that is involved in the switching event; this translates into longer retention times. This and their two-terminal nature are some reasons why molecular-based devices are more suitable for memory device applications [26] and are incorporated into alternative architecture designs such as hybrid CMOS-nanowire and neural network implementations [27, 28]. Other benefits include molecular design and synthesis that allows preferential molecular self-assembly onto metals and semiconductors for interconnection [29], and the promise of achieving atom-scale densities [30]. Some examples using molecular based state variables include molecular and atomic switches demonstrated using synthetic rotaxane functional molecules [31], metallocarborane molecules [32] and CNTs [33]. Atomic scale devices have also been proposed and demonstrated using graphene; for e.g. [34] a nanomechanical switch using a suspended graphene ribbon that deformed the graphene when a voltage bias was applied; capacitive coupling causes the suspended graphene to come to close proximity with the bottom electrode; upon bias removal, elastic forces return the graphene to the “open” position. An atomic-scale graphene switch was also demonstrated by Bockrath et al. [35, 36]. These switches are fabricated by creating nanoscale gaps using electrical breakdown of graphene sheets. Atomic switching was shown to occur at a current density of 1.6 mA/ μ m, which is equivalent to about 1 μ A/atom switching at about 5 V. It was also reported that the physical breakdown dimension is less than 10 nm. To restore conductance, a bias of about 4 V is applied; this is thought to form a linear chain of carbon material that shorts the graphene break junction. The $I_{\text{on}}/I_{\text{off}}$ ratio is about 100. Given the lack of amplification, this switch would make a useful non-volatile two-terminal memory element. A schematic of this device is shown in Fig. 4.3 and a typical voltage versus time switching characteristic is shown in Fig. 4.4.

From a more fundamental analysis, such an atomic switch can be constructed by linear C=C bonds with atomic length scales, and based upon the bonding and formation energies, a calculation of minimal energy dissipation for carbon–carbon atomic switching could be derived. Iijima et al. [37] investigated carbon formation energies, migration, and breakage behaviors of carbon chains that were attached to graphene; methods used included transmission electron microscopy (TEM), Fig. 4.5, and density functional theory (DFT) calculations. Their studies found that

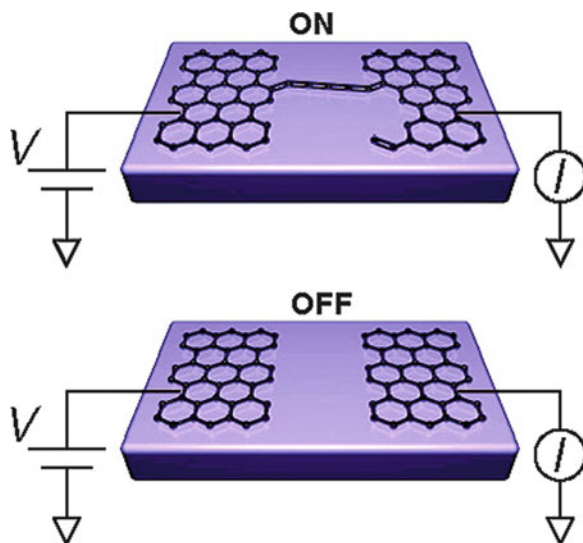


Fig. 4.3 Atomic-scale switch based on graphene (Reproduced with permission from [35]. © 2008 American Chemical Society)

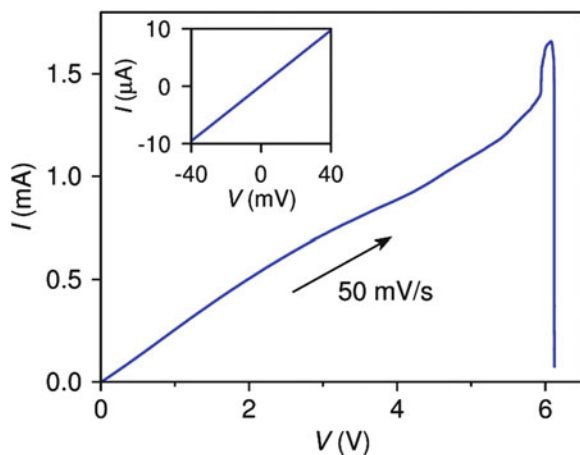


Fig. 4.4 Current vs. voltage during the breakdown process. Inset: Low bias current–voltage characteristic prior to breakdown (Reproduced with permission from [35]. © 2008 American Chemical Society)

the formation energy of a carbon atomic chain from a narrow zigzag edge GNR is about 1.09 eV/Å. Therefore, for a width of 10 nm, a formation energy of 109 eV (1.75×10^{-17} J) would be required to form a linear atomic carbon bridge. To cause breakdown, energy greater than the bond energy must be applied. For this example,

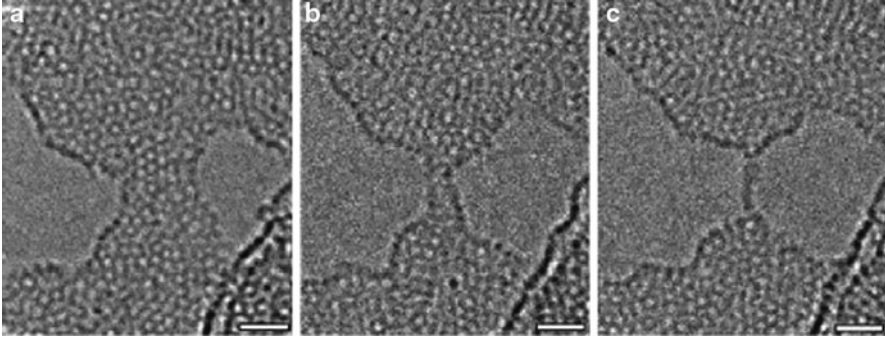


Fig. 4.5 Consecutive HR-TEM images showing the dynamics for the formation and breakage of freestanding carbon atomic chains through continuous electron beam irradiation. (a) A GNR with a width of about 1.7 nm was formed between two holes in graphene. (b) The GNR was thinned row-by-row under continuous irradiation. (c) A carbon chain consisting of double strands was formed, and there was a knot that remained on the left chain. Scale bar = 1 nm (Reproduced with permission from [37]. © 2009 American Physical Society)

assume that a carbon link is made up of bonding of cumulene ($=C=C=C=C$), where the bond energy is 614 kJ/mol. To minimize quantum tunneling effects, assume a 10 nm long atomic carbon chain requires to be broken, which contains about 75 cumulene covalent bonds. Therefore, $E_{Breakdown} = 75 \times 10^{-18} \text{ J}$ (468 eV). The energy for each switching event cycle would be $E_{dissipated} = E_{formation} + E_{Breakdown}$, so then $E_{dissipated} \sim 9.25 \times 10^{-17} \text{ J}$ (577 eV).

Using molecules as a state variable is considerably different from an electron due to their characteristic weight and size, in that they are substantially physically larger and heavier. This difference is particularly advantageous for memory applications where storage time can be estimated from the Wentzel–Kramers–Brillouin (WKB) theory as

$$\tau_{store} \sim \frac{1}{P_{tun}} = \exp\left(\frac{2\sqrt{2m}}{\hbar}(a\sqrt{E_b})\right)$$

where P_{tun} is the probability of tunneling, m is the molecular mass, E_b is the barrier height and a is a constant. For logic device implementations, molecular-memory-based devices are expected to be slower than electron or spin implementations due to the larger m for molecules, (although the maximum vibration frequency of the rotational mode is less than 1 ps), since

$$t_{sw} = \frac{L}{v} = L\sqrt{\frac{m}{2E_b}}$$

where L is the feature size. Indeed, molecular devices hold the promise of scaling to extremely high density levels approaching the number of active molecular elements

close to Avogadro's number; however to achieve extreme scaling, practical challenges such as addressing the complex interconnection scheme, eliminating undesirable coupling effects, and achieving reliable readout are required to be solved at an architectural level. In terms of speed, the vibrational energy relaxation ($\sim 2,700 \text{ cm}^{-1}$) [38] would be the fastest physical molecular dynamic movement possible, and hence would not switch faster than about 1 ns—similar to some of the fastest atomic switch experiments thus far undertaken [39–41].

4.4 Spin in Graphene

Spin-enabled devices and concepts are receiving a great deal of attention not just in graphene but for various types of material systems. The promise of spin is that it can be used to represent, compute and transmit information in a more robust fashion than electron charge. This is because variability in a spin-based device is limited only by thermal fluctuations and not by quantum fluctuations as in electronic devices [42]. In addition, spintronics offers the possibility of building low-power, high-performance non-volatile electronic devices by decoupling the energy intensive electron-charge transfer from its electron-spin degree of freedom.

Spin is the fundamental building block of magnetism, and as such, invoking on-demand electron spin orientation requires a magnetic field, B , to be generated and manipulated. Another way to accomplish this is via spin–orbit (SO) coupling. An applied magnetic field produces Zeeman splitting of magnitude $\Delta E = g\mu B$, where g is the electron g -factor and μ is the Bohr magneton. The energy levels split symmetrically with a separation of ΔE and relax after T_1 , having energies $\pm \Delta E/2$. This situation is very similar to electron charge where distinguishability must exceed the thermal noise minimum of $kT \ln 2$. Other than coupling differences, the spin scenario mimics power considerations for electron charge as previously presented, where the total energy dissipation of a single electron is $E_{\text{dissipation}} = 1/2\alpha T_1 + kT \ln 2$.

Spin-based devices such as spinFETs and STTRAM devices require the following critical parameters to be satisfied; (1) effective modulation of spin degree of freedom requiring a spin modulation mechanism (2) a very high spin transit time or decoherence length; a means for spin polarized electrons to travel larger distances without losing encoded information (3) effective injection and detection of spin current from a ferromagnetic system into a non-magnetic system; a means of reaping low write and read currents. Of most interest are materials with large spin coherence length and large spin coupling, but unfortunately this combination is seldom found in material systems. Nevertheless, it is anticipated that at least one of these characteristics will be satisfied at room temperature for fabricating a useful spin device. Carbon-based materials such as graphene are attractive for spin based electronics because of their large spin coherence length and weak spin orbit coupling. Graphene (C) has a low atomic number, leading to weak spin orbit coupling and zero nuclear spin; the latter leads to low hyperfine coupling interactions which in turn reduces spin scattering. Spin coherence lengths in graphene have been

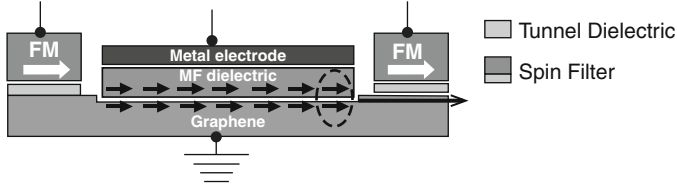


Fig. 4.6 A graphene FET cross-sectional view with ferromagnet (FM) source/drain, spin filters and multiferroic gate dielectric for inducing exchange coupling through gate modulation

measured to be on the order of $2\ \mu\text{m}$ at room temperature, much higher than most semiconductors [43]. Another report shows that a spin diffusion length of $1.5\ \mu\text{m}$ and a corresponding spin lifetime of $84\ \text{ps}$ is obtained through Hanle experiments [44]. These properties are not only attractive for transporting spin-encoded information over a larger distance but also make it interesting for fabricating trans-conductance devices such as those based on the Sugahara–Tanaka model [45]. However, the small spin-orbit interaction of graphene is a limitation for the design of conventional devices such as the Datta–Das spin FET [46]. As a result of graphene’s weak spin orbit interaction, modulation of spin information is difficult. To enable spin modulation, the spin-splitting of bands and gate modulation in graphene have been proposed via (1) doping with transition metals, to create dilute magnetic graphene (similar to dilute magnetic semiconductors) for carrier-mediated transport [47], (2) the exchange proximity interaction (EPI) through ferromagnetic oxide/graphene sandwich structures. In exchange proximity interaction [48], graphene is in close proximity to a ferromagnetic oxide or a multiferroic oxide and experiences an exchange interaction that provides a Zeeman field for electrons in graphene; this induces a spin precession around the magnetization axis of the ferromagnetic oxides, Fig. 4.6. Effective Zeeman splitting acts on the spin of graphene carriers, thereby inducing a precession around the magnetization axis of the ferromagnetic oxide. In addition, unlike other semiconductor materials, graphene has been shown to make better spin tunnel junction contacts devoid of large Schottky contact resistance, offering a pathway to high spin polarization injection [49].

The dynamic behavior of single spin switching is different from charge-based switching since the switching process does not depend on moving carriers. It is limited by the spin’s (electron or hole) relaxation time (the time it takes for spin orientation to relax to its equilibrium state). Similar to the electron relaxation time in the momentum space, the spin relaxation time is dependent on the spin–orbit coupling properties of the material. The shortest spin relaxation time is estimated to be about $1\ \text{ps}$ associated with holes that have a stronger spin–orbit coupling, while electrons can reach up to several hundred nanoseconds to microseconds when the coupling is weaker [50]. To gain the benefits of spin based systems via minimizing scattering events, electron motion is typically required to be at a minimum. The smallest spin element/device could conceptually be a single atom, and hence potentially be capable of device densities $>10^{14}/\text{cm}^2$. If operated at minimum

power dissipation ($2 \times 1.5kT\ln 2$) and 1 ps, it would dissipate power in the range of MW/cm². Such a dense array could be implemented with graphene nano-islands (<10 nm on a side) made from graphene [51].

4.5 Pseudospin in Graphene

An interesting alternate state variable that is possible to realize in graphene is pseudospin [52]. Using the unique material properties of graphene, a Bilayer Pseudospin enabled Field-Effect Transistor (BiSFET) has been proposed [53]. The operation of this device is based on phase-coherent many-body excitonic tunneling effect in graphene bilayers; modulation is by gate control and fine-tuning of charge carriers in each layer. The term “pseudospin” is used to suggest the similarity to the “up” and “down” spin states of a ferromagnet. For pseudospin, each layer (together with either its associated holes or electrons) can be considered a degree of freedom. Through gate control of fermionic charge carrier densities, electrons in one layer can pair with holes in the opposite layer resulting in bosonic electron–hole-pairs/excitons which then can condense. Consequently, the condensation alters the quantum wavefunctions in the bilayer qualitatively, converting states that were isolated in one of the two layers into states that are a coherent linear combination of top and bottom layer components [53]. This qualitative change enhances conductance through the two layers, reducing the tunnel resistance from a large value to one limited by contacts only. Similar coherence transport has been observed in GaAs/AlGaAs bilayer systems [54]. Room temperature operation is possible if the carrier densities in the two layers are equal but have opposite polarity—electrons in one layer, holes in the other. It has been shown theoretically [55] that such a condensate could occur in an *n*-type and *p*-type graphene layer pair with large and nearly equal carrier densities ($n = p$), separated by a thin dielectric tunnel barrier. Figure 4.7a shows a simple BiSFET device schematic of the two graphene layers with associated contacts, Fig. 4.7b shows the equivalent circuits and Fig. 4.7c shows the modeled electrical characteristics. The tunneling conductance between the *p* and *n* graphene layers is large at small interlayer bias, and becomes small at high interlayer bias. The maximum voltage and current that the device can reach also depends on the charge densities in the two layers. For a device with equal charge densities (balanced), every electron in the *n*-layer is paired with a hole in the *p*-layer, so the tunneling rate between the two layers is the highest and most desirable. For unequal charge densities, both I_{max} and V_{max} are smaller than in the balanced case.

Circuit simulations of a 20 nm gate width shows that the average energy consumed per clock cycle per BiSFET is 0.008 aJ at 100 GHz [53]. As a comparison, a CMOS MOSFET at 100 GHz would consume about 5 aJ per switch; from a device perspective, the BiSFET seems attractive. To enable condensation, a key transition temperature needs to be met, known as the Kosterlitz–Thouless (KT) temperature. Simulations show that this transition temperature approaches 300 K when E_F is larger than 0.3 eV, and carrier concentration, n is larger than 10^{13} cm², and d , the

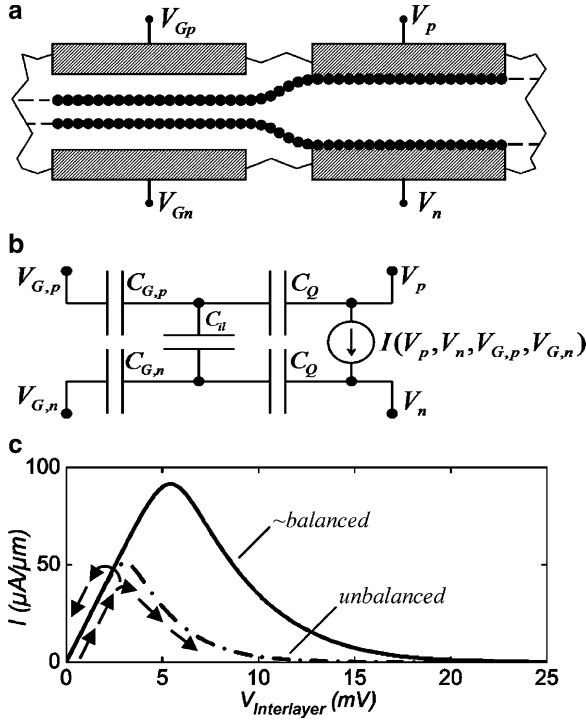


Fig. 4.7 (a) Schematic representation of a BiSFET, (b) circuit model, and (c) interlayer current-voltage (I - V) characteristics for the BiSFET used for SPICE simulations in this letter, with approximately balanced and unbalanced charged densities, the latter due to a -25 mV effective gate voltage (Reproduced with permission from [53]. © 2009 IEEE)

distance between graphene layers is less than 2 nm [56]. Studies on time-dependant dynamics of condensation in a bilayer graphene arrangement has not been explicitly investigated. To develop an understanding of BiSFET and pseudospinronic ultimate speed limitation, various approaches can be taken. This includes (a) modeling the bilayer graphene structure as a capacitor and simply taking the RC time constant [57]; circuit simulations show switching at 100 GHz; (b) using a superfluidity approach and considering the Landau criterion; the velocity of the superfluid cannot exceed sound velocity (1.5×10^4 m/s)—taking a device size of 10 nm, gives a time in the $\sim$ ps regime [58]; (c) simply taking the electron hole recombination time in graphene at densities of about 10^{12} cm^{-2} —this has been calculated to be about 1 ps [59]. For the purposes of a benchmark approach, a minimum switching speed of 1 ps is assumed along with a minimum device dimension of $20 \text{ nm} \times 20 \text{ nm}$ given the gate width dimension of SPICE simulations chosen in [53] and recent studies also showing graphene widths of less than 20 nm width will have a appreciable drop of the maximum current [60].

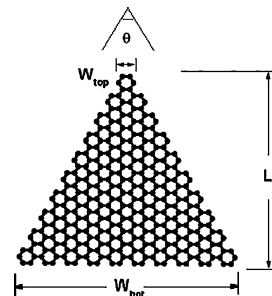
4.6 Phonons in Graphene

The use of phonons as a state variable has also been proposed to be implemented within graphene. Traditionally, phonons are regarded as heat carriers, but, just like electrons, spins, and photons, they are able to physically represent information, and hence are considered a state variable. Given graphene's high thermal conductivity ($>5,000$ W/mK) [61], various proposals employing phonons as a state variable in graphene have been conceived [62–65]. Thermal rectification occurs when there is a larger thermal conductivity along one dimension than the opposite and such a thermal gradient can be obtained in a nonlinear lattice. It has also been observed that in nonlinear carbon lattice systems, negative differential thermal resistance (NDTR) can be obtained and this has in the potential to enable thermal logic and memory [64, 66].

Graphene offers the advantage that it is a geometric 2D material that can be easily patterned. This is important for rectification purposes as the geometric outline of the device dictates information pathways of phonon-based circuits. Phonon based devices such as thermal rectifiers [67], thermal transistors [66], thermal logic gates [66] and thermal memory [64] have been conceptualized and proposed. At the core of these proposals are some fundamental molecular dynamic phenomena; in carbon nanotubes, both mass gradient and the gradient along the radius of the nanotube helps in rectification; in graphene, it is the width gradient that provides maximum rectification [65, 68, 69]. Figure 4.8 shows an example of a graded 2D graphene nanoribbon thermal rectifier. This arrangement act as a thermal diode, where good thermal conduction occurs under a positive “thermal bias” and a “poor” thermal conduction under negative “thermal bias”. This emphasizes that phonon transport occurs along the gradient where the width decreases, otherwise known as thermal rectification.

Figure 4.9 shows an example of a proposed thermal transistor. The device has non-linear source (S) and drain (D) components controlled by a gate (G).

Fig. 4.8 An example of a graded graphene 2-D structure that provides maximum thermal rectification. W_{top} and W_{bot} correspond to the first layer with one hexagonal atomic pattern and bottom with N layers respectively. Each segment is graded in an $L/2$ fashion (Reproduced with permission from [65]. © 2009 American Institute of Physics)



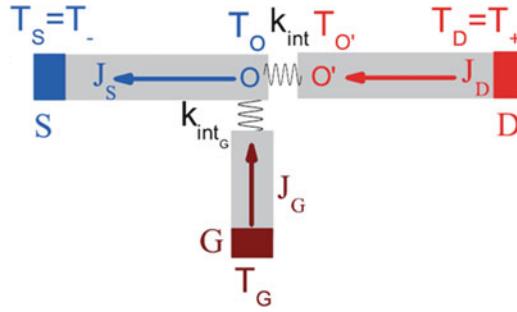


Fig. 4.9 Schematic of a simple thermal transistor. T_+ and T_- are discrete temperatures where $T_+ > T_-$. The gate (G) is also set at a discrete temperature T_G . Each segment is modeled by a one-dimensional Frenkel–Kontorova (*FK*) lattice. The *FK* model describes a chain of harmonic oscillators subject to an external sinusoidal potential. The spring constants k_{int} and k_{intG} are the most important thermal transistor parameters that control the magnitude and position of the NDTR (Reproduced with permission from [66]. © 2008 American Physical Society)

A temperature gradient in each of these components generates a harmonic oscillation. These thermally generated harmonic oscillations can be modeled as if they reverberate on attached springs with spring constants k_{int} and k_{intG} that are correlated to the temperature gradient associated with S-D and S-G. Studies on graphene systems show that the above configurations clearly demonstrate NDTR characteristics. The NDTR can be understood from studying the vibrational spectra at points O and O' . NDTR provides the key for thermal logic gates, e.g., super-response and negative response, which are necessary for the thermal signal repeater and the NOT gate. Figure 4.10 shows a simulation of a thermal NOT gate.

Fundamentally, phonons define the very nature of temperature. Absolute zero is the temperature at which atoms have minimal motion. In a material, the unit of vibrational energy that arises from oscillating atoms is known as a phonon. In order for a phonon to represent information, it must possess energy beyond the natural occurring vibrational modes at a certain temperature, T . One can also imagine this situation as sending a “heat” packet that represents a binary “1”. Therefore, the energy required to project a phonon “packet” of information must be greater than $kT \log 2$. In addition, a phonon travels at a certain velocity known as the phonon group velocity. Phonon group velocities of longitudinal (L) and transverse (T) modes in graphene have been measured to be $v(L) = 21.3$ km/s and $v(T) = 13.6$ km/s [70]. To put this in perspective, it will take at least 5 ns for a phonon to travel a distance of 1 nm in graphene. Ultimately, the minimum requirements to enable the existence of a phonon would be between two carbon atoms. This example is analogous to ion traps, where quantum information is transferred from one ion trap to another by phonon coupling [71]. With respect to using graphene and propagating a packet of information in the form of a phonon, one could imagine a single carbon ($=C=C=C=C=$) chain or a single honeycomb graphene chain with defined edge states. In the case of a honeycomb, we can estimate the ultimate

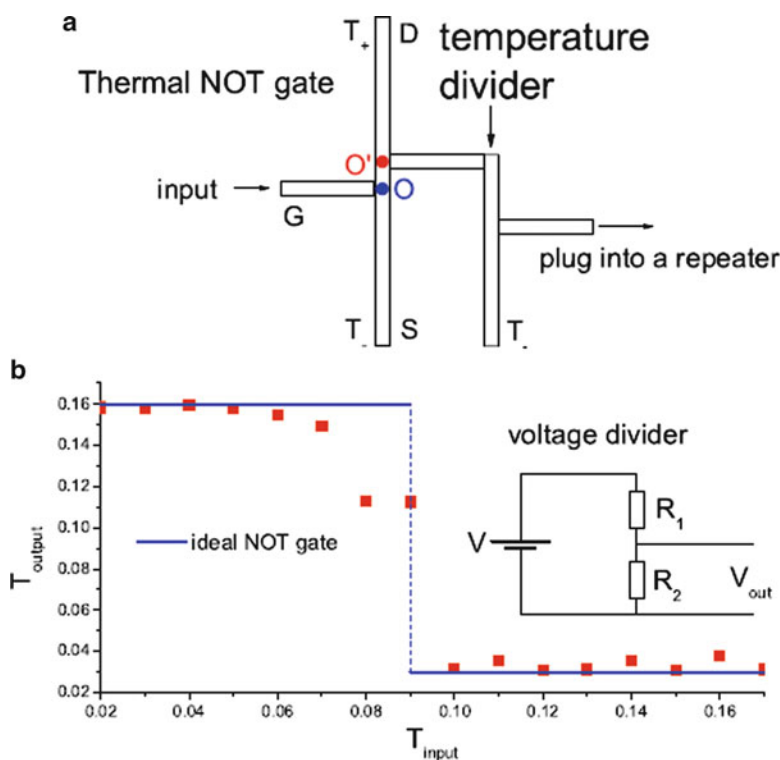


Fig. 4.10 (a) Structure of the thermal NOT gate. Through the G segment, the signal is transferred to the O point of the transistor. The output of the transistor (from the OO point) is transferred to the temperature divider. Plug the output of the temperature divider into a repeater; the final output is shown in (b). (b) Function of the thermal NOT gate. It is very close to an ideal NOT gate. Inset: Structure of a two-resistor voltage divider, the counterpart of a temperature divider, which supplies a voltage lower than that of the battery (Reproduced with permission from [66]. © 2008 American Physical Society)

scaling of these devices to measure at least two carbon-to-carbon bonds where the device would effectively be an integer multiple of the C–C bond length (0.142 nm). For Table 4.11 calculations, it is assumed that a graphene width of 1 nm is possible.

4.7 Outlook

Figure 4.11 summarizes some of the key performance attributes of alternative state variables. Many practical challenges such as fabrication, device–device interconnection, circuits and manufacturing issues have been deliberately avoided. Rather, the focus is on the elemental state variable operation relevant to natural physical limits.

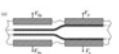
State Variable	Electron	Spin	Pseudo Spin	Phonon	Molecular Motion
Device Implementation					
Fastest Switching Speed	~1ps energy relaxation time	~1ps precession frequency	~1ps recombination time, RC time constant	~5ns phonon group velocity	1ns vibrational speed
Energy	0.05eV $3kT/\ln 2$ (1 electron)	0.05eV $3kT/\ln 2$ (1 spin)	0.05eV $3kT/\ln 2$	0.02eV $kT/\ln 2$	577 eV
Smallest Device Footprint	1nm x 1nm (2 carbon atoms)	0.5nm x 0.5nm (1 carbon atom)	20nm x 20nm	1nm x 1nm (2 carbon atoms)	0.2nm x 75(0.2nm) chain of 75 carbon atoms
Modulation Method -on/off	field effect modulation	magnetic field, spin orbit coupling	carrier densities n and p via electric field control	temperature or voltage via thermoelectrics	capacitive and elastic forces
Advantages	electron based devices well understood	mono -atom operation	low power consumption	Ideal for phonon directional control	extremely good "off" properties (not leaky)
Challenges	bandgap control, static power, edge state control	isolation and single spin addressing	transistional temperature sensitivities T_c	phonons travel relatively slowly	high energy to break C=C covalent bonds

Fig. 4.11 Summary of graphene based state variable performance estimates. “Fastest switching speed” refers to the fastest possible speed the physical state variable can alternate between bistable states. “Minimum switching energy” refers to the smallest amount of energy dissipated by the process required to switch the device. This disregards any external power required to achieve this process, such as power to generate a magnetic field. Smallest device footprint assumes the minimum area required that would support the state variable. Modulation method refers to an external stimulus that enables or catalyzes a switching event. The last two rows highlight the advantages and challenges of each state variable

From the outset, it can be seen that the “alternative” state variables do not profoundly outperform electron charge. The current challenge in microprocessor technology development is in minimizing energy dissipation, which fundamentally requires the state variable to compete with the thermal noise bath (less than kT in the most idealized case). If energy dissipation is to be less than this limit, distinguishability will be compromised and elaborate fault tolerant and redundancy mechanisms would need to be implemented which in turn would compromise fabrication cost, planar area, design simplicity, and chip yield.

With respect to speed, it can be seen that to no surprise, mechanical switches that rely on the movement of carbon atoms do not support fast operation. Similarly, electrons, spins, magnons and phonons all exhibit similar energies required for a switching event to occur.

The challenge still remains to derive a physical state variable that surpasses electron charge via graphene based device concepts. Although graphene has enabled a great deal of such exotic state variables and physics, the jury is still out as to whether these state variables will be translated into useful devices, circuits, and systems.

Acknowledgments The authors would like to acknowledge the support of the Nanoelectronics Research Institute, Western Institute of Nanoelectronics (WIN) together with the Focus Center Research Program (FCRP), the Center on Functional Engineered NanoArchitectonics (FENA). We also thank Dr. Alex Khitun (UCLA), Dr. Ian Young (Intel Corporation), Prof. Matthew Gilbert (UIUC), Dr. Brian Doyle (Intel Corporation) and Dr. Dmitri Nikonov (Intel Corporation) for various fruitful discussions. Special thanks goes to Dr. Kerry Bernstein (IBM) and Dr. Steve Kramer (MICRON) for manuscript review inputs.

References

1. K. Novoselov, A. Geim, S. Morozov, D. Jiang, Y. Zhang, S. Dubonos, I. Grigorieva, and A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, p. 666, 2004.
2. K. Galatsis, A. Khitun, R. Ostroumov, K. Wang, W. Dichtel, E. Plummer, J. Stoddart, J. Zink, J. Lee, and Y. Xie, "Alternate State Variables for Emerging Nanoelectronic Devices," *Nanotechnology, IEEE Transactions on*, vol. 8, pp. 66–75, 2009.
3. J. D. Meindl, "Low power microelectronics: retrospect and prospect," *Proceedings of the IEEE*, vol. 83, pp. 619–635, 1995.
4. Y. Taur, "CMOS design near the limit of scaling," *IBM Journal of Research and Development*, vol. 46, pp. 213–222, 2002.
5. J. Hutchby, G. Bourianoff, V. Zhirnov, and J. Brewer, "Extending the road beyond CMOS," *Circuits and Devices Magazine, IEEE*, vol. 18, pp. 28–41, 2002.
6. J. Meyer, A. Geim, M. Katsnelson, K. Novoselov, T. Booth, and S. Roth, "The structure of suspended graphene sheets," *Nature*, vol. 446, pp. 60–63, 2007.
7. M. Han, B. Özyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Physical review letters*, vol. 98, p. 206805, 2007.
8. X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Physical review letters*, vol. 100, p. 206803, 2008.
9. L. Mao, "Finite size effects on the gate leakage current in graphene nanoribbon field-effect transistors," *Nanotechnology*, vol. 20, p. 275203, 2009.
10. S. Russo, M. Craciun, M. Yamamoto, A. Morpurgo, and S. Tarucha, "Contact resistance in graphene-based devices," *Physica E: Low-dimensional Systems and Nanostructures*, 2009.
11. L. Liao, Y. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, pp. 305–308, 2010.
12. R. W. Keyes and R. Landauer, "Minimal energy dissipation in logic," *IBM Journal of Research & Development*, vol. 14, pp. 152–7, 1970.
13. R. Landauer, "Irreversibility and heat generation in the computing process," *IBM Journal of Research & Development*, vol. 5, p. 183, 1961.
14. R. Landauer, "Computation: a fundamental physical view," *Physica Scripta*, vol. 35, pp. 88–95, 1987.
15. C. Shannon, "The mathematical theory of communication," *Bell Systems Technical Journal*, vol. 27, pp. 379–423, Mar 1948 1948.
16. J. D. Meindl, "A history of low power electronics: how it began and where it's headed," in *Proceedings 1997 International Symposium on Low Power Electronics and Design (IEEE Cat. No. 97TH8332)*. ACM, 1997, pp. 149–51. New York, NY, USA.
17. J. D. Meindl and J. A. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1515–16, 2000.
18. V. V. Zhirnov, R. K. Cavin, III, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling - a gedanken model," *Proceedings of the IEEE*, vol. 91, pp. 1934–9, 2003.

19. R. W. Keyes, "Fundamental limits in digital information processing," *Proceedings of the IEEE*, vol. 69, pp. 267–78, 1981.
20. K. L. Wang, K. Galatsis, R. Ostroumov, M. Ozkan, K. Likharev, and Y. Botros, "Nanoarchitectonics: Advances in Nanoelectronics," in *Handbook of Nanoscience, Engineering and Technology*, 2nd ed, W. A. Goddard, III, W. D. Brenner, S. E. Lyshevski, and J. G. Iafrate, Eds. Boca Raton: CRC Press, 2007.
21. R. Ostroumov and K. L. Wang, "On Power Dissipation in Information Processing," in *American Physical Society*, Los Angeles, 2005.
22. R. Ostroumov and K. L. Wang, "Fundamental power dissipation in scaled CMOS and beyond," in *Proceedings of the SRC Techcon Conference*, Portland, 2005.
23. ITRS, "International Technology Roadmap for Semiconductors, 2005," *Semiconductor Industry Association (SIA)* <http://public.itrs.net/Reports.htm>.
24. K. Majumdar, K. V. R. M. Murali, N. Bhat, and Y.-M. Lin, "External Bias Dependent Direct To Indirect Band Gap Transition in Graphene Nanoribbon," *Nano Letters*, vol. 10, pp. 2857–2862, 2010.
25. R. Singh, J. O. Poole, K. F. Poole, and S. D. Vaidya, "Fundamental device design considerations in the development of disruptive nanoelectronics," *Journal of Nanoscience and Nanotechnology*, vol. 2, pp. 363–8, 2002.
26. J. R. Heath, "Molecular Electronics," *Annual Review of Materials Research*, vol. 39, pp. 1–23, 2009.
27. M. Butts, A. DeHon, and S. C. Goldstein, "Molecular electronics: devices, systems and tools for gigagate, gigabit chips," in *IEEE/ACM International Conference on Computer Aided Design. IEEE/ACM Digest of Technical Papers (Cat. No.02CH37391)*. IEEE. 2002, pp. 433–40. Piscataway, NJ, USA.
28. K. K. Likharev and D. B. Strukov, "CMOL: devices, circuits, and architectures," *Introducing Molecular Electronics*. Springer-Verlag. 2005, pp. 447–77.
29. J. E. Green, J. Wook Choi, A. Boukai, Y. Bunimovich, E. Johnston-Halperin, E. DeIonno, Y. Luo, B. A. Sherif, K. Xu, Y. Shik Shin, H.-R. Tseng, J. F. Stoddart, and J. R. Heath, "A 160-kilobit molecular electronic memory patterned at 1011 bits per square centimetre," *Nature*, vol. 445, pp. 414–417, 2007/01/25/print 2007.
30. D. Eigler, C. Lutz, and W. Rudge, "An atomic switch realized with the scanning tunnelling microscope," 1991.
31. W. Dichtel, J. Heath, and J. Fraser Stoddart, "Designing bistable [2] rotaxanes for molecular electronic devices," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 365, p. 1607, 2007.
32. S. Kabehie, A. Stieg, M. Xue, M. Liong, K. Wang, and J. Zink, "Surface Immobilized Heteroleptic Copper Compounds as State Variables that Show Negative Differential Resistance," *The Journal of Physical Chemistry Letters*, vol. 1, pp. 589–593, 2010.
33. T. Rueckes, K. Kim, E. Joselevich, G. Y. Tseng, C.-L. Cheung, and C. M. Lieber, "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing," *Science*, vol. 289, pp. 94–97, July 7, 2000 2000.
34. K. Milaninia, M. Baldo, A. Reina, and J. Kong, "All graphene electromechanical switch fabricated by chemical vapor deposition," *Applied Physics Letters*, vol. 95, p. 183105, 2009.
35. B. Standley, W. Bao, H. Zhang, J. Bruck, C. Lau, and M. Bockrath, "Graphene-based atomic-scale switches," *Nano Lett*, vol. 8, pp. 3345–3349, 2008.
36. M. Bockrath, J. Bruck, and N.-C. Yeh, "Graphene Atomic Switches for Ultra-Compact Logic Devices & Non-Volatile Memories," in *NRI Annual Review* Gaithersburg, 2009.
37. C. Jin, H. Lan, L. Peng, K. Suenaga, and S. Iijima, "Deriving carbon atomic chains from graphene," *Physical review letters*, vol. 102, p. 205501, 2009.
38. A. Ferrari, J. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. Novoselov, and S. Roth, "Raman spectrum of graphene and graphene layers," *Physical review letters*, vol. 97, p. 187401, 2006.

39. J. Beebe and J. Kushmerick, "Nanoscale switch elements from self-assembled monolayers on silver," *Applied Physics Letters*, vol. 90, p. 083117, 2007.
40. T. Tamura, T. Hasegawa, K. Terabe, T. Nakayama, T. Sakamoto, H. Sunamura, H. Kawaura, S. Hosaka, and M. Aono, "Material dependence of switching speed of atomic switches made from silver sulfide and from copper sulfide," 2007, p. 1157.
41. K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, "Quantized conductance atomic switch," *Nature*, vol. 433, pp. 47–50, 2005.
42. I. Ovchinnikov and K. Wang, "Variability of electronics and spintronics nanoscale devices," *Applied Physics Letters*, vol. 92, p. 093503, 2008.
43. N. Tombros, C. Jozsa, M. Popinciuc, H. Jonkman, and B. Van Wees, "Electronic spin transport and spin precession in single graphene layers at room temperature," *Nature*, vol. 448, pp. 571–574, 2007.
44. W. Han, K. Pi, W. Bao, K. McCreary, Y. Li, W. Wang, C. Lau, and R. Kawakami, "Electrical detection of spin precession in single layer graphene spin valves with transparent contacts," *Applied Physics Letters*, vol. 94, p. 222109, 2009.
45. S. Sugahara and M. Tanaka, "Spin MOSFETs as a basis for spintronics," *ACM Transactions on Storage (TOS)*, vol. 2, pp. 197–219, 2006.
46. S. Datta and B. Das, "Electronic analog of the electro optic modulator," *Applied Physics Letters*, vol. 56, pp. 665–667, 2009.
47. T. Jayasekera, B. D. Kong, K. W. Kim, and M. Buongiorno Nardelli, "Band Engineering and Magnetic Doping of Epitaxial Graphene on SiC (0001)," *Physical review letters*, vol. 104, p. 146801, 2010.
48. Y. Semenov, K. Kim, and J. Zavada, "Spin field effect transistor with a graphene channel," *Applied Physics Letters*, vol. 91, p. 153105, 2007.
49. V. Karpan, G. Giovannetti, P. Khomyakov, M. Talanana, A. Starikov, M. Zwierzycki, J. van den Brink, G. Brocks, and P. Kelly, "Graphite and graphene as perfect spin filters," *Physical review letters*, vol. 99, p. 176602, 2007.
50. C. Tahan and R. Joynt, "Rashba spin-orbit coupling and spin relaxation in silicon quantum wells," *Physical Review B*, vol. 71, Feb 2005.
51. J. Bai, X. Zhong, S. Jiang, Y. Huang, and X. Duan, "Graphene nanomesh," *Nat Nano*, vol. 5, pp. 190–194, 2010.
52. M. Polini, R. Asgari, Y. Barlas, T. Pereg-Barnea, and A. MacDonald, "Graphene: A pseudochiral Fermi liquid," *Solid State Communications*, vol. 143, pp. 58–62, 2007.
53. S. Banerjee, L. Register, E. Tutuc, D. Reddy, and A. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): a proposed new logic device," *Electron Device Letters, IEEE*, vol. 30, pp. 158–160, 2009.
54. I. Spielman, J. Eisenstein, L. Pfeiffer, and K. West, "Resonantly enhanced tunneling in a double layer quantum Hall ferromagnet," *Physical review letters*, vol. 84, pp. 5808–5811, 2000.
55. H. Min, R. Bistritzer, J. Su, and A. MacDonald, "Room-temperature superfluidity in graphene bilayers," *Physical Review B*, vol. 78, p. 121401, 2008.
56. H. Min, R. Bistritzer, J.-J. Su, and A. H. MacDonald, "Room-temperature superfluidity in graphene bilayers," *Physical Review B*, vol. 78, p. 121401, 2008.
57. D. Reddy, L. Register, E. Tutuc, and S. Banerjee, "Bilayer Pseudospin Field-Effect Transistor: Applications to Boolean Logic," *Electron Devices, IEEE Transactions on*, vol. 57, pp. 755–764, 2010.
58. S. Ianeselli, C. Menotti, and A. Smerzi, "Beyond the Landau criterion for superfluidity," *Journal of Physics B: Atomic, Molecular and Optical Physics*, vol. 39, p. S135, 2006.
59. F. Rana, "Electron-hole generation and recombination rates for Coulomb scattering in graphene," *Physical Review B*, vol. 76, p. 155431, 2007.
60. M. Gilbert, "Performance Characteristics of Scaled Bilayer Graphene Pseudospin Devices," *Electron Devices, IEEE Transactions on*, pp. 1–9.
61. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Letters*, vol. 8, pp. 902–907, 2008.

62. L. A. Jauregui, Y. Yue, A. N. Sidorov, J. Hu, Q. Yu, G. Lopez, R. Jalilian, D. K. Benjamin, D. A. Delkd, W. Wu, Z. Liu, X. Wang, Z. Jiang, X. Ruan, J. Bao, S. S. Pei, and Y. P. Chen, "Thermal Transport in Graphene Nanostructures: Experiments and Simulations," *ECS Transactions*, vol. 28, pp. 73–83, 2010.
63. J. Hu, X. Ruan, and Y. Chen, "Thermal conductivity and thermal rectification in graphene nanoribbons: a molecular dynamics study," *Nano Letters*, vol. 9, pp. 2730–2735, 2009.
64. L. Wang and B. Li, "Thermal memory: a storage of phononic information," *Physical review letters*, vol. 101, p. 267203, 2008.
65. N. Yang, G. Zhang, and B. Li, "Thermal rectification in asymmetric graphene ribbons," *Applied Physics Letters*, vol. 95, p. 033107, 2009.
66. L. Wang and B. Li, "Thermal logic gates: computation with phonons," *Physical review letters*, vol. 99, p. 177208, 2007.
67. B. Li, L. Wang, and G. Casati, "Thermal diode: Rectification of heat flux," *Physical review letters*, vol. 93, p. 184301, 2004.
68. G. Wu and B. Li, "Thermal rectifiers from deformed carbon nanohorns," *Journal of Physics: Condensed Matter*, vol. 20, p. 175211, 2008.
69. N. Yang, N. Li, L. Wang, and B. Li, "Thermal rectification and negative differential thermal resistance in lattices with mass gradient," *Physical Review B*, vol. 76, p. 20301, 2007.
70. D. L. Nika, E. P. Pokatilov, A. S. Askerov, and A. A. Balandin, "Phonon thermal conduction in graphene: Role of Umklapp and edge roughness scattering," *Physical Review B*, vol. 79, p. 155413, 2009.
71. J. I. Cirac and P. Zoller, "Quantum Computations with Cold Trapped Ions," *Physical review letters*, vol. 74, p. 4091, 1995.

Chapter 5

Transport of Novel State Variables

Shaloo Rakheja and Azad Naeemi

5.1 Introduction

In this chapter, a framework is developed for comparison of different post-CMOS interconnect technologies using physical models of transport mechanisms for these novel interconnects. In the first part of the chapter, an overview of CMOS interconnects is provided with an emphasis on the impact of scaling on the performance and energy dissipation of local (<100 gate pitches) interconnects. The second part of the chapter deals with the delay modeling of novel interconnects. The upper bound on the performance of novel interconnects is benchmarked against their conventional CMOS counterparts. A set of guidelines is derived at the device and circuit level for post-CMOS technologies.

The revolutionary growth of the semiconductor industry has been in large part because of the increase in binary information throughput of devices. Binary information throughput is a measure of the computation capability at the device level and is given as the number of instructions executed per second per unit area of the chip. Miniaturization of circuits has helped pack more functionality on the chip at a reduced cost per function. Scaling silicon field effect transistors (FETs) may be severely limited beyond the 2020 technology roadmap as there may be significant challenges in the thermal management of ICs [1–3]. Increase in quantum mechanical tunneling of electrons through the gate dielectric and the increase in sub-threshold leakage current are the two most important factors that would inhibit the scaling of silicon based electronics, which is essentially a charge based technology [2, 3]. At the heart of the current FET structure is the metal-oxide-semiconductor (MOS) capacitor that consumes energy proportional to its capacitance value in every switching cycle. There is a critical need to have an alternative switching paradigm

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Table 5.1 Mapping of transport mechanism and the corresponding state variable for which the transport mechanism can potentially be used to establish communication between on-chip receiver and driver

Transport mode	Information token/state variable
Diffusion	Spin, pseudo-spin (graphene), temperature (Phonons), direct excitons, indirect excitons
Drift	Indirect excitons, spin, pseudo-spin
Ballistic	Spin, pseudo-spin, temperature (phonons)
Spin waves	Spin
Electromagnetic waves	Photons, plasmons

that can overcome the energy limitations of charge based FETs. In addition, the capacitance of on-chip interconnects presents an extra load and increases power dissipation in a microprocessor.

Possible alternatives to electronic charge that can be utilized as a state variable include electron spin, pseudo-spin in graphene, direct/indirect excitons, temperature, plasmons, magnetic domain walls, and photons [4]. Graphene is a promising material for dealing with this new set of state variables thanks to its long spin coherence length [5], suitability for generation and manipulation of direct and indirect excitons [6], long electron phase coherence length [7] and pseudo-spin [8].

The three requirements generic to any information processing system are (a) ability to have distinguishable states, (b) ability to switch between digital states aided by external controls, and (c) as the ability to transmit information from one physical location on the chip to another, which is essentially “communication.” Any logic technology must be complemented with an interconnect technology that can help transport information between different devices on a chip. To avoid area and power overhead, these devices must avoid signal conversion at least at the local level. Moreover, in current microprocessors it has been shown that interconnects consume more than 50% of the dynamic power [9]. Dimensional scaling of interconnects increases the delay of interconnects thereby increasing their latency [10]. Therefore, it becomes important to quantify the interconnect aspects in non-charge based logic technology.

Communication between devices can be established by physically transporting the carrier of information between devices or by wave propagation between devices. Thus, transport mechanisms can be broadly categorized into *particle transport* and *wave-based communication*. Particle-based transport mechanisms include: *diffusion, drift and ballistic transport*. Wave-based communication includes *electromagnetic waves, plasmonic waves and spin waves*. Table 5.1 lists various transport mechanisms and the state variables that they can communicate.

5.2 The CMOS Interconnect

The quintessential purpose of an interconnect is to communicate information between different physical locations of a chip with minimum latency [11]. Physically, interconnects are patterned metal layers atop a dielectric or within a dielectric.

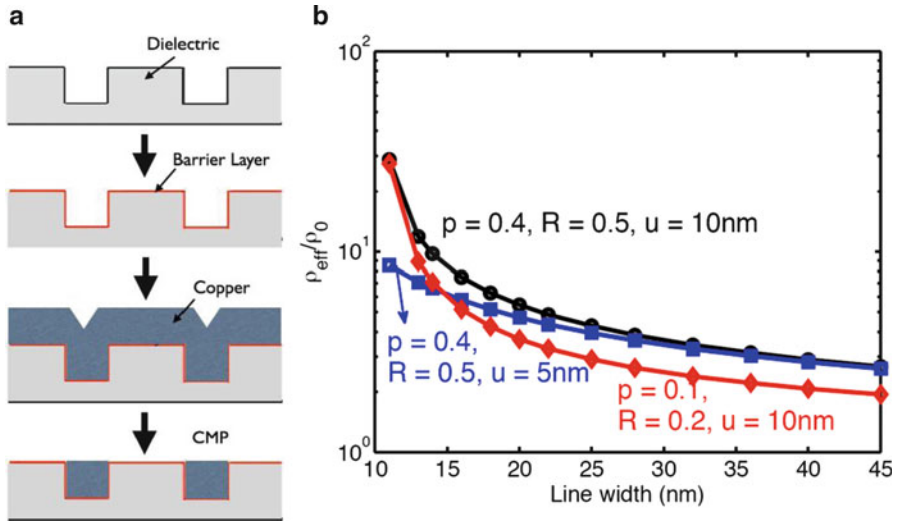


Fig. 5.1 (a) Cu damascene process, adapted from [14]. (b) Compact resistivity models to project Cu resistivity versus line-width [15]

In the current CMOS technology, interconnects are implemented in copper with an intra/interlayer dielectric having a low effective dielectric constant ($\kappa_{\text{eff}} \leq 3$). The use of copper interconnects was introduced at the 220 nm technology node in microprocessors [12]. The damascene process to pattern copper interconnects has played a pivotal role in the success of copper interconnect technology [12, 13]. Copper damascene process is essentially a four-step process that begins with patterning the dielectric using photomasks and lithography techniques. The second step consists of the deposition of a barrier layer such as Ta or TiN over the patterned dielectric in order to prevent interaction between the metal and dielectric. This is especially important because diffusion of copper into the dielectric creates a deep impurity level that degrades device performance. The third step consists in filling the pattern with metal using electrochemical deposition. In the last step, chemical mechanical polishing is performed to remove excess copper and to planarize the metal surface. The process steps in a typical Cu damascene process are illustrated in Fig. 5.1. The drive towards lowering the effective dielectric constant (to minimize the wire capacitance) increases manufacturing complexity, and this affects cost and reliability. A hybrid of porous low- κ dielectrics with air gap technology may be incorporated in future process flows to sustain the drive towards lower dielectric constants [10].

While miniaturization of transistors increases their performance, the native interconnect delay increases with miniaturizing interconnects [16]. Challenges associated with scaling of interconnects include resistivity degradation, material integration issues, planarity control and reliability problems due to electrical, thermal, and mechanical stresses in a multi-layer wire stack. The impact of process variations on the electrical variability of circuits becomes significant as the critical dimensions of

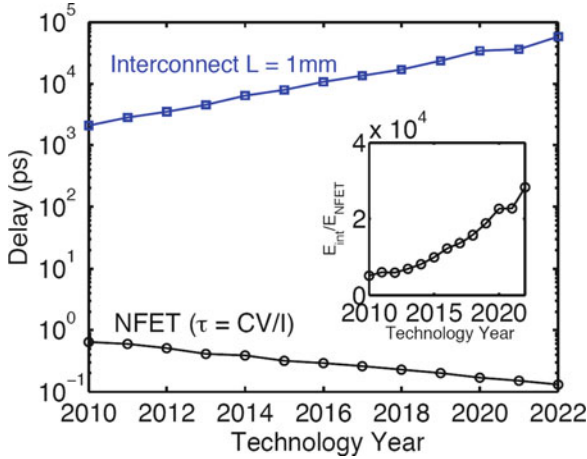


Fig. 5.2 Delay of interconnect of length 1 mm versus the technology year. Also plotted is the delay of a minimum sized NFET versus the technology year. The inset shows the energy dissipation of a 1 mm interconnect without repeaters normalized to the energy dissipation of a minimum sized NFET for different technology years. Data is from ITRS [10]

integrated circuits shrink. As the interconnect dimensions approach the mean free path of electrons in copper ($\lambda_{Cu} \sim 40$ nm), the interaction of electrons with the interconnect sidewalls and grain boundaries tends to increase the effective resistivity of the wire. To model the interconnect resistivity, the following should be taken into account: electron grain boundary reflectivity, sidewall specularity, and line edge roughness [15, 17, 18]. Performance metrics of interconnects for future technology nodes have been projected by the ITRS [10]. Figure 5.1 shows the effective resistivity of Cu normalized to its bulk resistivity as a function of the line-width of the metal for different values of sidewall specularity, grain boundary reflectivity, and line edge roughness. The cumulative impact of size effects is to increase the effective resistivity of the interconnect, thereby deteriorating its performance.

Figure 5.2 shows interconnect and FET delays versus the technology year, based on ITRS projections [10]. This figure serves to highlight the growing disparity in the performance of interconnects and transistors as a result of dimensional scaling. The inset of this plot shows the energy dissipation of interconnects normalized to the energy dissipation of a minimum size n-type FET. Although there has been little or no variation in the interconnect capacitance over the different technology generations, there has been a steady decrease in transistor capacitance. This enhances the energy dissipation of interconnects relative to that of transistors.

The circuit model that is used to analyze CMOS interconnects is shown in the inset of Fig. 5.3. The circuit consists of a CMOS inverter that drives the interconnect and the load. The load consists of an identically sized CMOS inverter. The circuit may be represented as a network of resistances and capacitances characteristic of the driver, the interconnect, and the load. A distributed rc network model is used to represent the interconnect. At the local interconnect level, the inductance of the interconnect

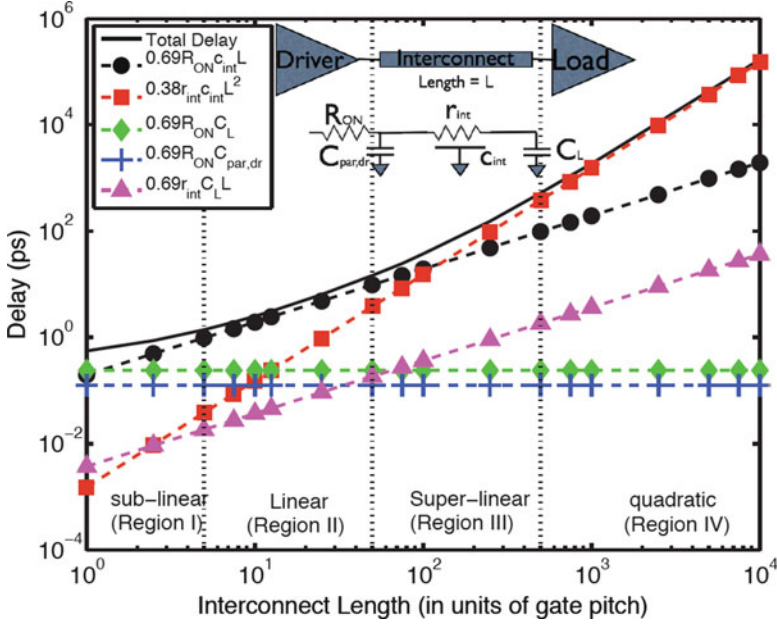


Fig. 5.3 Delay associated with the various delay components, as modeled in (5.1), when the CMOS interconnect is driven by a driver which is $5\times$ the min. driver size at the 2020 technology node. Inset shows the electrical circuit used to model the performance of CMOS interconnects (Reproduced with permission from [19]. © 2010 IEEE)

does not play any role; therefore, inductance is not included in the model. Using the Elmore delay formula, the delay of the CMOS circuit may be written as,

$$t_{CMOS} = 0.69R_{ON}(C_{par,dr} + C_L) + 0.69(R_{ON}c_{int} + r_{int}C_L)L + 0.38r_{int}c_{int}L^2 \quad (5.1)$$

For the ITRS 2020 technology node (minimum feature size = 14 nm), the on-resistance (R_{ON}) of a minimum size n-FET is extracted as 24 k Ω , and the parasitic capacitance of a minimum-sized driver is 7.56 aF. C_L is the load capacitance of the fan-out gate and is ~ 15 aF for a minimum size inverter load. The interconnect resistance per-unit length, r_{int} , and capacitance, c_{int} , values are $2 \times 10^6 \Omega/\text{cm}$ and 1.65 pF/cm, respectively [10].

Figure 5.3 plots the delay contribution from the various components in (5.1); the interconnect is assumed to be driven by a driver which has $5\times$ the strength of a minimum size driver. For interconnects of very short length (up to 5 gate pitches), the effect of $R_{ON}(C_{par,dr} + C_L)$ is comparable to the effect of $R_{ON}c_{int}L$ on the total delay. This is identified as the sub-linear region (Region I) in Fig. 5.3. In Region II (linear region), the total delay follows very closely the term $R_{ON}c_{int}L$ and the effect of other terms on the total delay can be ignored. The linear region spans interconnects of length 5–50 gate pitches. However, for interconnects longer

than 50 gate pitches, the effect of the term $r_{int}c_{int}L^2$ becomes non-negligible in comparison to the term $R_{ON}c_{int}L$ on the total delay. This is identified as the super linear region (Region III), which extends from length 50 gate pitches to 500 gate pitches. For interconnects longer than 500 gate pitches, the total delay is dominated by the interconnect delay and this is identified as the quadratic region (Region IV).

It is worthwhile to note that currently there are no manufacturable solutions to achieve many of the ITRS projections at the 14 nm technology. However, ITRS projections represent the consensus among semiconductor experts on the best current estimate of the industry's needs for a given node [10]. Research and development efforts will potentially allow for reaching these goals.

5.3 Novel Interconnects

A map is provided in Table 5.1 that relates a state variable to the physical transport mechanism that may be used to communicate information. As of now, there is no clear front-runner technology that may replace or even augment the CMOS technology. Therefore, the map provides a generic platform to compare many novel technology options. Also, using transport equations based on physical transport modes enables the exploration of fundamental limits of novel technologies at the material, device, circuit, and architecture levels.

This section is divided into two parts (1) particle transport interconnects, and (2) wave-based interconnects.

5.3.1 Particle Transport Interconnects

Particle transport based interconnects include diffusion, drift, and ballistic interconnects. These interconnects rely on the actual physical movement of information bearing entities (called “carriers” hereafter) between different physical locations on the chip.

5.3.1.1 Diffusion Interconnects

Diffusion is a kinetic process that is driven by the carrier density gradient in the system. Diffusion as a transport mode may be used for a variety of different state variables including those that do not have a net electric charge associated with them. The state variables that may be transported by diffusion include spin, pseudo-spin in graphene, phonons and excitons (both direct and indirect) [5, 8, 20, 21]. Information can be encoded in the polarization of spin, which has two stable states in the

presence of a magnetic field: the spin up and the spin down. Thus, the two states of spin can be used to represent the binary logic states “0” and “1” or vice versa. Spintronics (short for spin electronics) is based on manipulating the information encoded in the spin states of the electron. Spintronics may have the potential advantages of increased data storage, higher reliability, and lower power dissipation. However, these advantages may be materialized only if electron spin is used both as an input and output. If spin is used solely to control electric current the technique will face the same scaling limits as charge based technology.

There have been some noteworthy proposals for logic based on electron spin manipulation and detection. Some devices have electric inputs and outputs and a spin degree of freedom to control their operation; other devices are defined completely by spin inputs and outputs. Devices belonging to the latter category include magnetic cellular automata, magnetic domain wall logic, domain wall majority logic, spin wave bus devices, and spin gain transistors [22]. In the proposal for an all-spin logic [23], information is stored in the orientation of nanomagnets and information is written via the spin transfer torque effect. Although electric currents are used to inject spin polarized currents in the device channel, it is possible to isolate the electric current path completely from the spin current path. Research efforts directed towards analyzing the delay, energy dissipation, scalability, reliability, and manufacturability of spin torque device logic are underway, both at the theoretical and experimental levels. Notwithstanding the early nature of research in spintronic logic, the delay models obtained later in this section may be extended to describe the channel and the interconnect delay in the all spin logic device.

In graphene, an additional degree of freedom is provided by the pseudo-spin. The unit cell in graphene consists of two carbon atoms. The phase shift between wavefunctions of electrons on the two atoms is analogous to spin. Thus it can be used to represent logic states “0” and “1”. In bilayer graphene, the two layers provide an additional degree of freedom of pseudo-spin and can be used to represent binary logic states [8].

An exciton is a quantum of electronic excitation energy traveling in the periodic structure of the crystal. It can be visualized as a Coulomb-correlated electron hole pair. Binary logic can be represented by presence or absence of excitons, or by utilizing the spin degree of freedom of excitons. A direct exciton is electrically neutral and hence its movement gives rise to the transportation of energy but not electric charge. An indirect exciton, on the other hand, consists of spatially separated electron and hole pairs as in bilayer graphene [6]. Unlike direct excitons, which cannot be manipulated by external electric field, indirect excitons can be transported with an external electric field.

The diffusion equation in 1D is given as

$$\frac{\partial n}{\partial t} = D \frac{\partial^2 n}{\partial x^2} - \frac{n}{\tau_n} \quad (5.2)$$

Here n denotes the carrier concentration in $1/\text{cm}$, D is the diffusion coefficient in cm^2/s and τ_n is the carrier relaxation time in s . In this analysis it is assumed that the

decay in carrier density is negligible in the time it takes for the carriers to diffuse from the driver to the receiver ($\tau_n \gg \tau_D = L^2/D$). This assumption is made in order to obtain an upper bound on the performance of diffusion interconnects. Diffusion time is proportional to L^2/D and the constant of proportionality (denoted as γ in this analysis), depends on the boundary conditions. The boundary conditions used for solving (5.2) are given as

$$n(x, 0 < t < t_1) = 0 \quad (5.3a)$$

$$n(x = 0, t) = u(t - t_1) \quad (5.3b)$$

$$\frac{\partial n}{\partial x}(x = L, t) = 0 \quad (5.3c)$$

where t_1 is an arbitrary time at which the concentration at the transmitter changes from zero to unity corresponding to logical “0” to logical “1” bit transition at the input. In the condition of negligible carrier relaxation, the diffusion equation for novel interconnects is analogous to the voltage diffusion equation for electrical interconnects [24]. The boundary conditions (5.3a–c) are used to obtain an upper bound on the performance of diffusion interconnects. In essence, the boundary conditions assume that the receiver is ideal and has a negligible impact on the interconnect. This is similar to the boundary condition for the voltage diffusion equation in CMOS circuits when a small load is connected to the electrical interconnect.

The numerical solution of (5.2) obtained using the PDE solver of MATLAB [25] is plotted in Fig. 5.4. Delay as a function of interconnect length L is given as

$$t_{DIFF} = \gamma \frac{L^2}{D} \quad (5.4)$$

The time taken to reach 50% of the steady state concentration at the receiver is $0.38 L^2/D$, assuming that the rise time of signal at the input is infinitesimally small. Hence, the normalized diffusion time $\gamma = t_{DIFF}/(L^2/D) = 0.38$. The value of 50% delay gradually increases as the input signal rise time increases, as depicted in the inset of Fig. 5.4. In this analysis γ is set to 0.38 to obtain an upper bound on the performance of diffusion interconnects.

Logic gates based on temperature as the state variable have also been suggested [26]. Known as thermal logic gates, they use phonons as the information carrier. Phonons can be transported by diffusion between an on-chip driver and receiver in a thermal computation system. The diffusion equation for phonons is better known as the heat equation [27]. For isothermal systems, the heat equation is given as

$$\frac{\partial T}{\partial t} = k_{th} \frac{\partial^2 T}{\partial x^2} \quad (5.5)$$

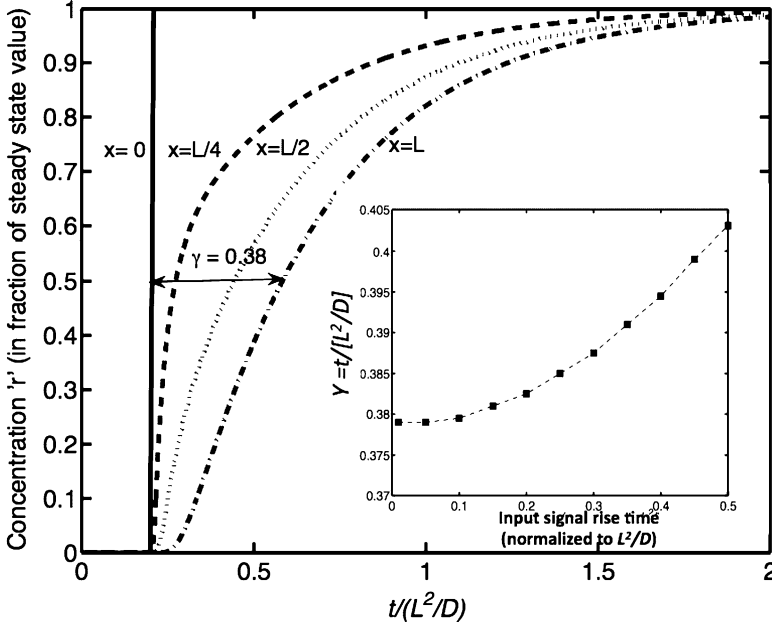


Fig. 5.4 Fractional concentration (r) at different points in the interconnect versus normalized diffusion time $t_{DIFF}/(L^2/D)$. The time taken to reach 50% of the steady state concentration at the receiver end (denoted as $x = L$) is $0.38 L^2/D$. The inset shows that the time taken to reach 50% of concentration at output increases as the input signal slope increases (Reproduced with permission from [19]. © 2010 IEEE)

where T is the temperature in Kelvin and k_{th} is the thermal diffusivity, and is the ratio of thermal conductivity and the volumetric heat capacity.

$$k_{th} = \frac{K}{C \cdot \rho} \quad (5.6)$$

where K is the thermal conductivity in W/m.K and C is the specific heat capacity in J/Kg.K and ρ is the material density in Kg/m³. Recently, a graphene thermal transistor has been discussed by Wang and Baowen [26]. It is a 3-terminal device exhibiting negative differential thermal resistance. To build a transistor that uses temperature as the state variable, Graphene and CNTs may serve as the material system. Also, interconnects in this system can be fabricated from the same material, thereby providing a homogenous integration and can overcome the problems associated with hybrid integration of different technologies [26, 28]. Phonons may be transported via diffusion and the interconnect delay of phonon diffusion interconnects is given as

$$t_{THERMAL,DIFF} = \gamma_{th} \frac{L^2}{k_{th}} \quad (5.7)$$

Table 5.2 Material parameters used to evaluate performance of particle transport based interconnects

Material parameter	Value
Spin diffusion coefficient D (cm ² /s)	200 [5]
Mobility of electrons μ (cm ² /Vs)	10,000 [5]
Thermal conductivity K (W/m K)	3,000 [30]
Specific heat capacity C (J/Kg K)	1,000 [31]
Material density ρ (Kg/m ³)	1,300
Mean free path λ (μ m)	1 [32]
Speed of sound in graphene (Km/s)	20 [29]

Thermal conductivity (κ) and Specific heat capacity (C) values are quoted at 300 K for graphene. Thermal properties of graphene are strong functions of temperature and also depend on size quantization. These values are only representative values used for comparing graphene interconnects with other interconnects. κ and C in carbon nanotube based interconnects are also quite similar

In principle, k_{th} decreases as temperature increases because K decreases with increase in temperature and C increases with temperature. At lower temperatures, the thermal conductivity of graphene increases rapidly with increasing temperature. However, beyond 80 K, the thermal conductivity begins to decrease with temperature, which is due to the growing strength of the three-phonon Umklapp scattering process in graphene [29]. In (5.7), k_{th} is assumed to be temperature independent in order to obtain an upper bound on the performance of phonon diffusion interconnects. Like the constant of proportionality γ in (5.4) for the diffusion delay, γ_{th} depends on boundary conditions. For similar boundary conditions as in (3), $\gamma_{th} = 0.38$. Values of material parameters to evaluate the interconnect delay in spin diffusion and thermal diffusion system in graphene are given in Table 5.2.

5.3.1.2 Drift Interconnects

Drift interconnects use an external electric field to manipulate carriers that have a net charge associated with them. Hence, drift interconnects can be used for electron spin and indirect excitons as in bilayer graphene [6, 21]. Drift is a possible transport option for an all-spin transistor since spin is a quantum mechanical property of an electron. Since electron by virtue of its charge moves with drift velocity on application of an external electric field, spin may be transported by drift as well. Drift can also be used for transporting indirect excitons. An indirect exciton consists of spatially separated electron and hole pairs as in bilayer graphene [6, 21]. Drift interconnects can have lower delay compared to diffusion interconnects. The delay associated with drift interconnects is

$$t_{DRIFT} = \frac{L}{v_d} \quad (5.8)$$

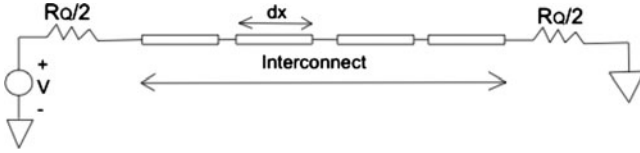


Fig. 5.5 Equivalent circuit diagram of a nanowire under low bias conditions. R_Q is the quantum resistance and its value is $12.9 \text{ k}\Omega$ per conduction channel. The differential element dx has resistance $(R_Q/l_0) dx$. The mean free path l_0 is taken to be $1 \text{ }\mu\text{m}$ for this analysis [33] (Reproduced with permission from [19]. © 2010 IEEE)

where v_d is the drift velocity of electrons. The drift velocity of electrons in the interconnect can be obtained by first calculating the actual electric field across the interconnect length. When the interconnect length is comparable to the mean free path of electrons, the effect of quantum resistance cannot be ignored. There is a minimum resistance (also known as the quantum resistance) of $h/2e^2 \approx 12.9 \text{ k}\Omega$ associated with an ideal quantum wire. This quantum resistance, R_Q , is only a contact resistance and is not a function of length [33]. The equivalent circuit diagram of a nanowire with an external bias across it is shown in Fig. 5.5. The model does not include capacitance or inductance of the nanowire, since a steady state model is being considered to obtain an upper bound on the speed of drift interconnects. At low electric fields, the resistance per unit length of the interconnect is only dependent on the low field mean free path of carriers in the nanowire.

The drift velocity v_d of electrons in the interconnect is equal to $\mu_0 E_{net}$, where E_{net} is the net electric field across the interconnect length L and μ_0 is the electron mobility in a long interconnect.

$$E_{net} = \frac{V_{DD} - IR_Q}{L} \quad (5.9)$$

$$I = \frac{V_{DD}}{R_Q + R_Q \frac{L}{l_0}} \quad (5.10)$$

where V_{DD} is the voltage applied across the interconnect, I is the current through the interconnect, R_Q is the quantum resistance, and l_0 is the mean free path of electrons in the interconnect at low electric field. Using (5.9) and (5.10), drift velocity v_d can be expressed as

$$v_d = \frac{\mu_0}{1 + \frac{l_0}{L}} \left(\frac{V_{DD}}{L} \right) \quad (5.11)$$

Using v_d from (5.11), the delay due to drift can be expressed as

$$t_{DRIFT} = \frac{L^2}{V_{DD} \mu_0} \left(1 + \frac{l_0}{L} \right) \quad (5.12)$$

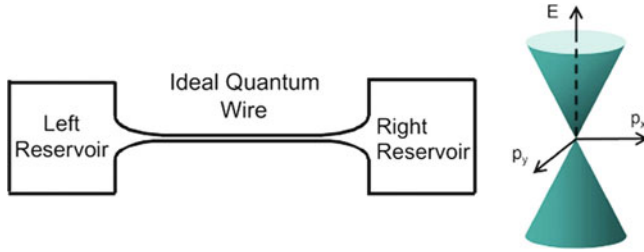


Fig. 5.6 An ideal quantum wire is shown on the *left*. The energy dispersion relation of graphene is shown on the *right*. Electron charge current is zero if the number of left-mover and right-mover electrons is same. However, the net spin current can be non-zero if the spin polarization in the left reservoir is changed (Reproduced with permission from [34]. © 2010 IEEE)

The drift based interconnect for particle transport is significantly different from the CMOS interconnect, which is an RC based interconnect. In an RC interconnect, information is transmitted through a voltage wave which diffuses from the driver to the receiver [24]. Although the nature of the voltage diffusion equation is similar to the particle diffusion equation, the speed at which information can travel in an RC interconnect can be much higher than the speed at which particles can be physically transported through the interconnect. In other words, in an RC interconnect signal can arrive sooner than the electrons at the receiver. For spin-based interconnects, electrons carrying spin information have to physically move from the driver to the receiver.

5.3.1.3 Ballistic Interconnects

Ballistic transport refers to the movement of carriers without scattering events in a medium. Ballistic transport is typically observed in low-dimensional conductors because of the small phase space for scattering of carriers. Ballistic spin transport can occur without any net-charge transport, thereby yielding pure-spin current and zero electric current. If the number of right mover electrons is equal to the number of left mover electrons in the ballistic channel between the driver and the receiver, then the net electric current in the channel is zero. However, if the spin polarization of electrons in the left reservoir (driver) is different than the spin polarization of electrons in the right reservoir (receiver), then a pure spin current can flow from the driver to the receiver (Fig. 5.6). In graphene, the E-k relationship near the Dirac point can be modeled by a linear approximation [35]; this makes the velocity of carriers independent of energy, and is equal to the Fermi velocity $v_f \approx 8 \times 10^5$ m/s. Hence, spin in graphene can be transported at Fermi velocity. The ballistic nature of the conductor prevents the left-mover and right-mover electrons to collide and mix-up.

The delay associated with a graphene ballistic interconnect is

$$t_{BALL} = \frac{L}{v_f} \quad (5.13)$$

If the interconnect is longer the carrier mean free path, then ballistic transport will tend towards a diffusive transport, and a unified model of ballistic-diffusive transport is necessitated. However, since the aim is to compare the best-case performance of various novel interconnects, a model corresponding to pure ballistic transport is sufficient for this analysis.

In addition to electron spin, phonons can also undergo ballistic transport in graphene; this could be the basis of a ballistic thermal switch. The delay for ballistic thermal interconnect is given as in (5.13) with the Fermi velocity replaced by phonon speed (v_{ph}). In graphene, the speed of acoustic phonons is ≈ 20 Km/s [29].

$$t_{THERMAL,BALL} = \frac{L}{v_{ph}} \quad (5.14)$$

5.3.2 Wave-Based Interconnects

In wave-based interconnects, communication of information is supported in a wave-based fashion without actual movement of particles. The wave-based interconnects discussed in the following sub-sections include spin wave bus interconnects and plasmonic interconnects.

5.3.2.1 Spin Wave Bus

Spin wave is a collection of precession of electron magnetic moment about a magnetic field. Spin waveguides can be made of magnetic films, a wire or a combination of wires made of ferromagnetic films, anti-ferromagnetic materials or ferrite materials [36–40]. Spin information is encoded in the phase of the spin wave, and superposition of spin waves is used to achieve useful logic functionality [37, 40]. The final logic state is detected by the inductive voltage measurement by the receiving microstrip. Information exchange via spin waves takes place without net electric charge current. The signal propagation speed of spin wave depends on factors such as the waveguide material and structure, spin-wave frequency and the magnitude and direction of external magnetic film. The delay associated with spin waves is:

$$t_{SWB} = \frac{L}{v_p(\omega)} \quad (5.15)$$

where $v_p(\omega)$ is the propagation velocity as a function of frequency of operation. The numerically simulated propagation velocity of NiFe spin wave bus in [37] is found to be 10^4 m/s. To benchmark against other transport mechanisms, two spin wave propagation velocities in NiFe are considered (1) 10^5 m/s (optimistic),

Table 5.3 Data from [45] of group velocity of cylindrical Ag plasmonic interconnect in SiO₂ dielectric. c_0 is the speed of light in vacuum

Diameter (nm)	Free space wavelength (nm)	Group velocity
10	500	$0.02c_0$
10	1000	$0.1c_0$
50	500	$0.12c_0$
50	1000	$0.38c_0$

and (2) 10^4 m/s (realistic). Somewhat higher spin wave velocities of 1.3×10^5 m/s are possible for other magnetic materials [41], but only NiFe spin wave bus has been considered here.

5.3.2.2 Plasmonic Interconnects

Optical interconnects have been widely studied as alternative solutions to chip–chip and chip–board interconnects where bandwidth is a critical metric [42]; in addition, their potential for intra-chip communication has been analyzed [42, 43]. However due to an order of size mismatch between nanoelectronic components and the wavelength of light, the use of optical interconnects will likely be restricted to the global interconnect level.

Plasmonics is a new technology of manipulating and routing light at the sub-micron length scales in metallic nanostructures embedded in dielectric. The conduit of propagation of plasmon waves is termed as the plasmon waveguide. Surface plasmons are light waves that propagate along the surface of a conductor, usually a metal. It can be viewed as a coupled electron and light oscillation, also known as “langmuir waves”. The most attractive feature of plasmons over conventional dielectric devices is their ability to confine light to structures with dimensions below the diffraction limit and to realize high field intensities in relatively small volumes. This could help to miniaturize photonic circuits that have typically been much larger than their electronic counterparts [44]. Plasmonic waveguides can also be used to propagate light and serve as the interconnect for plasmonic circuits. However, to utilize plasmonics for local interconnects on-chip, plasmonic switches need to be made. Otherwise the overhead associated with signal conversion (energy and circuit area overhead) will be prohibitive.

Plasmonic interconnects implemented with metallic nano-particles (such as Au, Ag, Cu, Al) in a dielectric may be used as a medium for propagation of plasmonic waves. The speed at which information can be transmitted in plasmonic interconnects depends on factors such as the material of the plasmonic waveguide, structure of the waveguide, and the plasmon frequency. The speed of propagation of surface plasmons is comparable to the speed of light in the dielectric material. Simulations have been used to obtain the group velocity of an isolated surface plasmonic waveguide made with an Ag cylinder embedded in a dielectric matrix of SiO₂ [45]. The group velocities are given in Table 5.3 for different combinations of diameter and the free space wavelength.

A propagating surface plasmon mode on a metal surface will eventually attenuate owing to losses associated with absorption in the metal. This absorption depends on the dielectric constant of the metal at the oscillating frequency. In the visible spectrum of light, silver is the metal with lowest absorption losses and hence provides a propagation length of 10–100 μm . The propagation length can be as high as 1 mm at the 1,550 nm telecom wavelength [46]. The range of propagation length in silver matches with the typical length of local and intermediate interconnects in electronic circuits. Propagation length is defined as the length at which the energy of the surface plasmon decays by a factor of $1/e$ ($e = 2.718$). Surface plasmons suffer from evanescent field coupling between neighboring wires wherein energy is lost from one signal wire carrying energy to another not carrying any energy initially. This is referred to as “crosstalk”, that is, leakage of signal energy from an interconnect to its neighbors. Crosstalk coupling length in plasmons degrades at lower operating frequencies and/or larger diameter of the waveguides [45]. The requirements of lower crosstalk in plasmonic interconnects are counter to those for higher signal propagation length. Hence, a careful optimization of the size of the plasmonic waveguide and the free-space wavelength can be performed to maximize the propagation length for a specified crosstalk level.

The implementation of plasmonic interconnects at the local level requires plasmonic switches in order to avoid energy and area overhead associated with signal conversion between the electrical and plasmonic domains.

5.4 Comparison of Novel Interconnects

The performance of novel interconnects is benchmarked against their conventional CMOS counterparts as a function of interconnect length. The limitations imposed by the interconnect delay are identified. Possible approaches towards improving the performance of novel circuits are highlighted. In order for novel circuits to be competitive against conventional CMOS circuits, it is shown that interconnect lengths need to be shorter than CMOS interconnects. The concept of “area scaling” is developed in the following sub-sections.

5.4.1 Particle Transport Interconnects Versus CMOS Interconnects

The delay associated with particle transport interconnects is plotted in Fig. 5.7. For post-CMOS interconnects, the delay associated with the drivers and receivers is neglected in the analysis; this is because the goal of this benchmarking is to establish an upper bound on the performance of novel interconnects. The figure also shows the delay associated with a CMOS system for two driver sizes (1) channel

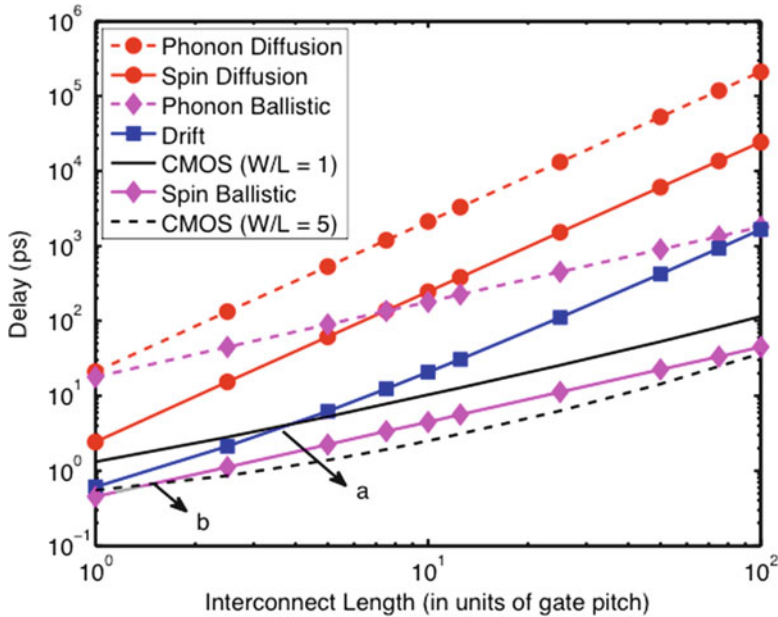


Fig. 5.7 Interconnect delay versus interconnect length for different particle transport mechanisms. CMOS delay is obtained for the 2020 technology node. W/L denotes the width to length ratio of the CMOS driver. For novel interconnects, the switch delay is ignored but for CMOS interconnects switch delay is taken into account. Material parameter values to obtain the plot are provided in Table 5.2. An external voltage of 0.8 V is assumed for drift interconnects. The novel interconnects are all slow compared to CMOS interconnects, except for the ballistic interconnect. At point “b”, ballistic interconnect becomes only slightly slower than CMOS interconnect with W/L = 5 driver size. Drift interconnect is faster than CMOS interconnect at W/L = 1 driver size, but only up to few gate pitches (denoted by “a”) (Reproduced with permission from [19]. © 2010 IEEE)

width-to-length ratio $W/L = 1$ and (2) channel width-to-length ratio $W/L = 5$ (also termed “5×”). In high performance logic, minimum sized drivers are rarely used due to their limited drive capability.

Most of the novel interconnects are relatively slow compared with the CMOS interconnect. This means that even if new circuits were to employ perfect switches with negligible delays, the delay of novel interconnects will be significantly more than that of CMOS interconnects. Diffusion interconnects with diffusion coefficient $D = 200 \text{ cm}^2/\text{s}$ are slower compared to CMOS interconnects. To make diffusion interconnects equally fast as CMOS interconnects with minimum sized CMOS drivers, for an interconnect length of 10 gate pitches, a diffusion coefficient of approximately $4,700 \text{ cm}^2/\text{s}$ is required (point “a” in Fig. 5.8). Compared to 5× minimum CMOS driver size, the diffusion coefficient needed is approximately $2 \times 10^4 \text{ cm}^2/\text{s}$ (point “b” in Fig. 5.8). This value of diffusion coefficient is more than an order of magnitude larger than the reported value of diffusion coefficient in high mobility graphene [5]. Owing to extremely small thermal diffusivity for phonons, diffusion interconnects for

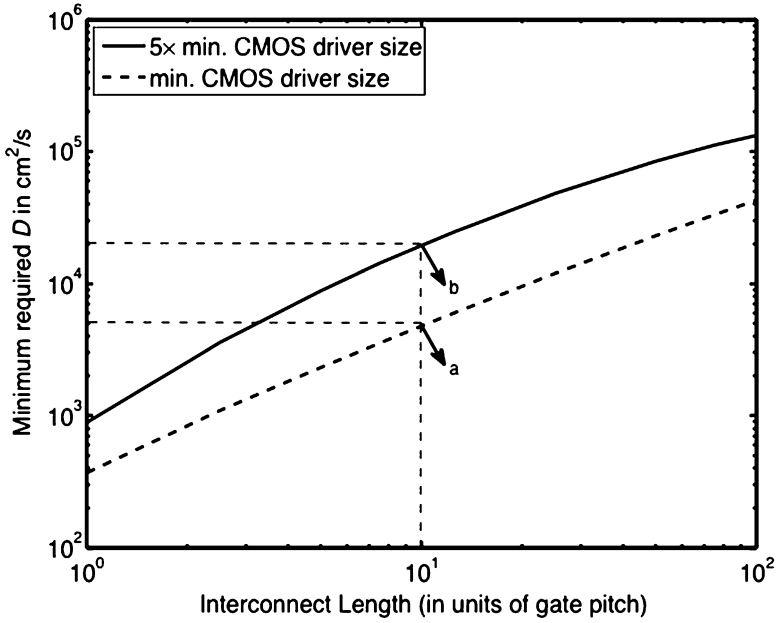


Fig. 5.8 Minimum required diffusion coefficient, D , in diffusion interconnects to achieve an equal performance as a CMOS system at the 2020 technology node. The value of diffusion coefficient required at 10 gate pitches for diffusion interconnects to be able to match in performance with CMOS interconnects is 4,700 cm²/s (point “a”) and 20,000 cm²/s (point “b”) for CMOS interconnect driven by minimum size driver and 5× minimum size driver, respectively

phonons have the maximum delay, which is approximately an order of magnitude larger than the delay of CMOS interconnects driven by minimum size driver at an interconnect length of 1 gate pitch. Also, phonon ballistic interconnects are slower than CMOS interconnects since the speed of phonons in graphene is around 20 Km/s. Spin drift interconnects with $\mu_0 = 10^4$ cm²/Vs and $l_0 = 1$ μm, offer higher speed than CMOS interconnects but only up to an interconnect length of 4 gate pitches (point “a” in Fig. 5.7).

Ballistic interconnects are faster than CMOS interconnects driven by minimum size CMOS driver. However, spin ballistic interconnects are only slightly slower than CMOS interconnects if the interconnect is longer than 0.5 gate pitches (point “b” in Fig. 5.7); this is assuming that CMOS interconnects are driven by a driver that is 5× the minimum driver size. This means that bigger devices may be tolerated in a ballistic transport system.

In order to be competitive with CMOS circuits, logic circuits with new devices will have to be scaled down in area so that the interconnect lengths are shorter. It is possible to derive the area scaling factor needed in the new logic to achieve similar performance as CMOS logic. This is obtained by equating the delay through novel interconnects and the delay through the CMOS system. Area scaling of new logic obtained thus does not account for intrinsic device delays in the new logic, and

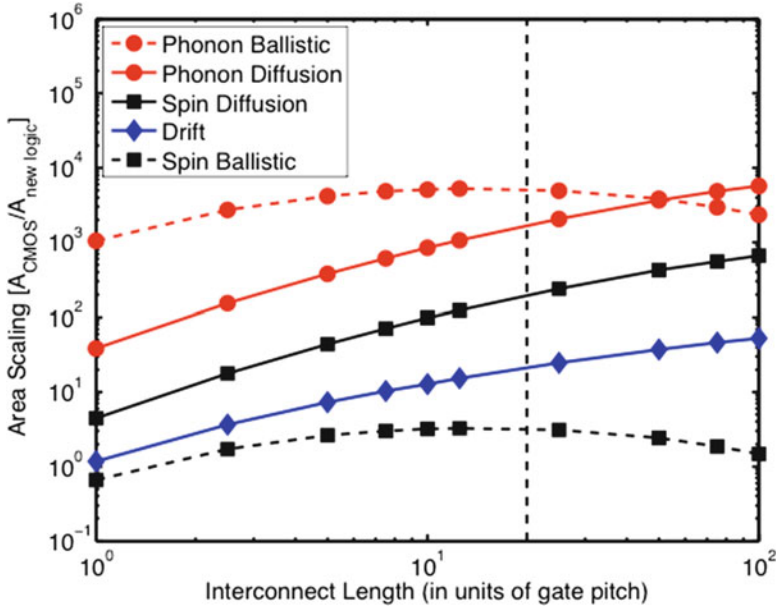


Fig. 5.9 Area scaling of new logic versus interconnect length, to obtain an equal performance as the CMOS logic (at $5\times$ minimum sized CMOS driver) (Reproduced with permission from [19]. © 2010 IEEE)

hence provides an optimistic value of area scaling. The required area scaling will be more severe if intrinsic device delays are taken into account.

Assuming that the logic gate pitch in the new logic is scaled by a factor of $L_{p,CMOS}/L_{p,new\ logic}$ (where L_p is the gate pitch) and the number of gates needed to implement a logic function is scaled $N_{CMOS}/N_{new\ logic}$, one can obtain the area scaling factor of the new logic as:

$$\frac{A_{CMOS}}{A_{new\ logic}} = \left(\frac{L_{p,CMOS}}{L_{p,new\ logic}} \right)^2 \times \frac{N_{CMOS}}{N_{new\ logic}}$$

As shown in Fig. 5.9, the required area scaling factors for diffusion and drift interconnects increase with the interconnect length for local interconnects up to 100 gate pitches. This is because the interconnect delay for diffusion and drift based transport mechanisms increases more rapidly with length as compared to CMOS interconnects. The area scaling factors for spin ballistic interconnects is less than unity at the minimum sized CMOS driver, while it is only slightly more than unity at $5\times$ the minimum sized CMOS driver. Further, the required area scaling factors for ballistic—both spin and thermal—interconnects exhibit a maximum. Beyond the maximum point, the delay of the CMOS interconnect increases more rapidly compared to the delay of the ballistic interconnects. This aids in lowering the requirement on the area scaling factors for ballistic interconnects.

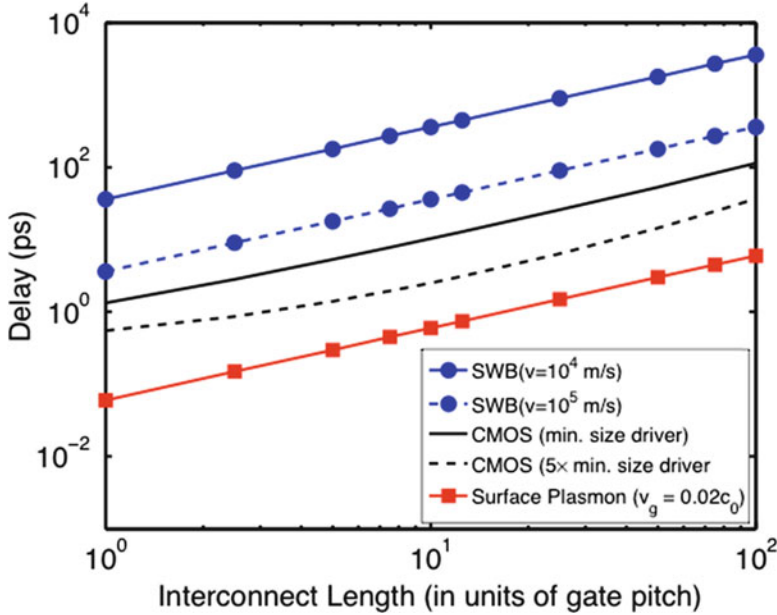


Fig. 5.10 Delay versus interconnect length for wave based interconnects. Also plotted is the delay through CMOS interconnects for reference. Delay of CMOS interconnects is plotted for min. driver size and $5\times$ the min. driver size. For spin wave bus, two propagation velocities have been considered. For surface plasmons, velocity of propagation is considered to be $0.02c_0$ [45] corresponding to an Ag cylinder of diameter 10 nm embedded in SiO_2 dielectric at free space wavelength of 500 nm; c_0 is the speed of light in vacuum. (Reproduced with permission from [19]. © 2010 IEEE)

5.4.2 Wave-Based Interconnects Versus CMOS Interconnects

The delay associated with spin-wave bus and plasmonic interconnects is plotted as a function of the interconnect length in Fig. 5.10. Delay associated with switches in the new technology is neglected in order to establish an upper bound on the performance of interconnects. Plasmonic interconnects are orders of magnitude faster compared to CMOS interconnects as well as other interconnects discussed in this chapter. This is because the propagation speed of plasmons can be comparable to the speed of light in the dielectric medium of the plasmon waveguide.

The delay through spin wave bus is plotted for propagation speeds of 10^4 m/s (realistic value) and 10^5 m/s (optimistic value). Spin wave bus is always slower than CMOS interconnects. To match the performance of CMOS interconnects, circuits utilizing spin wave bus must be made smaller in area. The required area scaling factor for spin-wave bus interconnects is plotted in Fig. 5.11. When compared with CMOS interconnects driven by minimum size drivers, an area scaling factor of $\approx 10\times$ is required for spin wave buses having a propagation speed of 10^5 m/s while an area scaling factor of approximately $1,000\times$ is required for spin wave buses

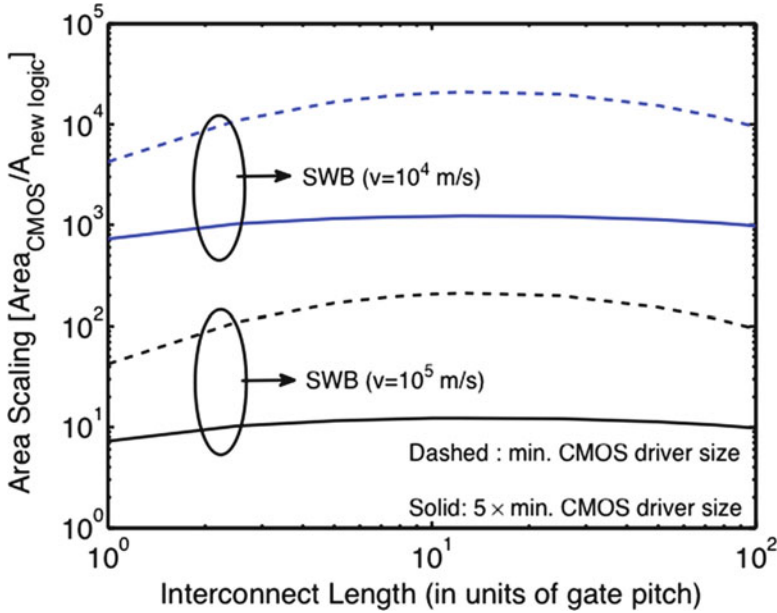


Fig. 5.11 Area scaling required of SWB to obtain equal performance as the CMOS interconnect. Area scaling for interconnects when compared with CMOS interconnects driven by a bigger driver is considerably more (Reproduced with permission from [19]. © 2010 IEEE)

having a propagation velocity of 10^4 m/s. The required area scaling factor shoots up by $10\times$ when a spin wave bus is compared with a CMOS interconnect driven by a driver whose strength is $5\times$ the strength of a minimum size CMOS driver. Such large area scaling factors may not be achievable at all in spin wave bus circuits. The scalability of spin wave bus below the spin wavelength poses a significant challenge [47]. While the width and the thickness of the spin wave bus can be scaled down to several nanometers, the wavelength must be reduced to make the length shorter. A representative value of spin wavelength based on defect tolerance is estimated to be 100 nm [47]. Hence, the concept of scaling the footprint of the device may not be easily viable in spin wave bus circuits.

Table 5.4 gives the area scaling factors for different interconnects to match in performance when compared with CMOS system for both a minimum size driver and a $5\times$ minimum size CMOS driver. Area scaling at an interconnect length of 10 gate pitches is tabulated. The CMOS driver size has a significant impact on the area scaling required of new logic to match the performance of a CMOS system. Such large area scaling factors may be very demanding for the new logic technology. This may mean that new circuits may operate at a lower speed. But their speed penalty has to be justified by significant energy improvements. Attractive approaches towards smart logic architectures may be extremely favorable to the new technologies. Parallel processing could be used for new technologies to overcome interconnect delay.

Table 5.4 Area scaling factor for different interconnects to match in performance with CMOS interconnects

Interconnect type	W/L = 1	W/L = 5
Diffusion (spin)	24	97.5
Ballistic (spin)	0.19	3.2
Drift (spin)	2.2	13
Ballistic (phonon)	304	5126
Diffusion (phonon)	199	845
Spin wave bus ($v_p = 10^4$ m/s)	1.2×10^3	2.05×10^4
Spin wave bus ($v_p = 10^5$ m/s)	12.2	205

W/L denotes the width to length ratio of the CMOS driver. The values in the table are obtained for an interconnect length of 10 gate pitches

5.5 Outlook and Future Directions

Interconnects impose major limitations in charge based technology by consuming more than 50% of dynamic power in microprocessors. In addition they also add delay to critical path and add noise and jitter to signals. Future technology options could exploit alternate state variables to overcome the constraints inherent to CMOS technology. Future devices that are aimed towards using alternate state variables for information processing must be able to communicate their corresponding state variable in a fast and energy efficient way, at least locally. Otherwise the energy and circuit overhead needed for signal conversion will be prohibitive.

Various transport mechanisms may be used for communicating information encoded in the novel state variables. Diffusion of information carriers may be used for charged as well as neutral state variables such as phonons, electron spins, and excitons. Ballistic transport may be used when the system size is smaller than the mean free path of the carriers. Like diffusion, ballistic transport may also be used for phonons, spin, and excitons. Drift as a means of transport works only when the information bearing particle has a net charge associated with it such as in electron spin, indirect excitons, and pseudo-spin in graphene. Information may also be communicated in a wave-based fashion without any actual movement of carriers in the system. In case of spin wave bus interconnects, information may be encoded in the phase of the spin wave. Spin waves superposition is used to achieve useful logic functionality. Plasmonic waveguides may be used as the conduit of information encoded in plasmons that are coupled electron photon oscillations existing at the interface between a metal and dielectric.

Even with perfect post-CMOS switches, the delay of most novel interconnects, with the exception of ballistic and plasmonic interconnects, is significantly higher than that of CMOS interconnects. In this sense, post-CMOS interconnects impose greater limitations on technology, the slowest transport mechanism being phonon diffusion. Spin diffusion is moderately faster than phonon diffusion due to higher

spin diffusivity as compared to phonon diffusivity. Propagation velocity of spin waves is limited to 10^5 m/s and hence the delay through these interconnects is larger than that of CMOS interconnects.

With the exception of plasmonic and ballistic interconnects, circuits utilizing alternate state variables can be competitive in terms of speed only if the interconnect lengths in them are shorter compared to those in CMOS circuits. Shorter lengths can be obtained (1) if the gate pitch of the new switches is scaled with respect to CMOS switches, and/or (2) fewer switches are needed in the new logic to do the same task. Area scaling of new logic is defined as the ratio of the area of CMOS circuit and the new circuit (both of which implement the same function). It is found that new switches must be comparatively smaller in area. However, the area scaling factors are quite large and may be very demanding for most of the alternative technology options.

Alternate state variable devices are likely to use a hybrid of new interconnects and electrical interconnects. While local interconnects can use novel transport mechanisms for information transfer, global interconnects are likely to be electrical. Even though novel interconnects may not offer a performance advantage over CMOS interconnects, their use can potentially be justified by improvement in circuit area and/or major energy benefits.

References

1. G. I. Bourianoff, "The future of nanocomputing," IEEE Computer Society, 2003.
2. V. V. Zhirnov, R. K. Cavin-III, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling—a gedanken model," *Proceedings of the IEEE*, vol. 91, no. 11, 2003.
3. R. K. Cavin, V. V. Zhirnov, D. J. C. Herr, A. Alba, and J. A. Hutchby, "Research directions and challenges in nanoelectronics," *Journal of Nanoparticle Research*, vol. 8, no. 6, 2006.
4. K. Galatsis, A. Khitun, R. Ostroumov, K. L. Wang, W. R. Dichtel, E. Plummer, J. F. Stoddart, J. I. Zink, J. Y. Lee, Y. H. Xie, and K. W. Kim, "Alternate state variables for emerging nanoelectronic devices," *IEEE Transactions on Nanotechnology*, vol. 8, no. 1, 2009.
5. N. Tombros, C. Josza, M. Popinciuc, H. Jonkman, and B. V. Wees, "Electronic spin transport and spin precision in single graphene layers at room temperature," *Nature*, vol. 448, 2007.
6. J. Su and A. MacDonald, "How to make a graphene bilayer excitons condensate flow," *Nature Physics*, vol. 4, August 2008.
7. F. Miao, S. Wijeratne, Y. Zhang, U. Coskun, W. Bao, and C. Lau, "Phase-coherent transport in graphene quantum billiards," *Science*, vol. 317, September 2007.
8. P. S. Jose, E. Prada, E. McCann, and H. Schomerus, "Pseudospin valve in bilayer graphene: Towards graphene-based pseudospintronics," arXiv: 0901.0889v2.
9. N. Magen, A. Kolondy, U. Weiser, and N. Shamir, "Interconnect-power dissipation in a microprocessor," SLIP, 2004.
10. ITRS 2008 Update on PIDS and Interconnects. Website: <http://www.itrs.net/Links/2008ITRS/Home2008.htm>.
11. J. Meindl, J. Davis, P. Zarkesh-Ha, C. Patel, K. Martin, and P. Kohl, "Interconnect opportunities for gigascale integration," *IBM Journal of Research and Development*, vol. 46, no. 2/3, March/May 2002.
12. P. Andricacos, "Copper-on-chip-interconnections, a breakthrough in electrodeposition to make better chips," *The Electrochemical Society Interface*, pp. 32–37, 1999.

13. P. Andricacos, C. Uzoh, J. Dukovic, J. Horkans, and H. Deligianni, "Damascene copper electro- plating for chip interconnections," IBM Journal of Research and Development, vol. 42, no. 5, pp. 567–574, Sept. 1998.
14. K. Saraswat, "Interconnections: Copper and low k dielectrics," Stanford University. online: www.stanford.edu/class/ee311/NOTES/.
15. G. Lopez, "The impact of interconnect process variations and size effects for gigascale integration," 2009.
16. J. A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect limits on gigascale integration (gsi) in the 21st century," Proceedings of the IEEE, vol. 89, no. 3, March 2001.
17. A. Mayadas, M. Shatzkes, and J. Janak, "Electrical resistivity model for polycrystalline films: the case of specular reflection at external surfaces," Applied Physics Letters, vol. 14, no. 11, 1969.
18. E. Sondheimer, "Mean free path of electrons in metals," Advances In Physics (Quarterly Supplement of Philosophical Magazine), vol. 1, no. 1, pp. 1–42, 1952.
19. S. Rakheja and A. Naemi, "Interconnects for Novel State Variables: Performance Modeling and Device and Circuit Implications," IEEE Trans. Electron Devices, vol. 57, no. 10, pp. 2711–2718, Oct. 2010.
20. J. Hu, X. Ruan, and Y. Chen, "Thermal conductivity and thermal rectification in graphene nanoribbons: A molecular dynamics study," NanoLetters, vol. 9, no. 7, 2009.
21. R. Dillenschneider and J.E.Moore, "Exciton formation in graphene bilayer," Physical Review B, vol. 78, 2008.
22. D. E. Nikonov, G. I. Bourianoff, and T. Ghani, "Proposal of a spin torque majority gate logic." online: <http://arxiv.org/abs/1006.4663>.
23. B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an all-spin logic device with built-in memory," Nature Nanotechnology, vol. 5, February 2010.
24. H. B. Bakoglu, Circuits, Interconnections and Packaging for VLSI, 1st ed. Springer, 1990.
25. R. Skeel and M. Berzins, "A method for the spatial discretization of parabolic equations in one space variable," SIAM Journal of Scientific and Statistical Computing, vol. 11, pp. 1–32, 1990.
26. L. Wang and L. Baowen, "Thermal logic gates: Computation with phonons," Physics Review Letters, vol. 9, 2007.
27. D. Widder, The Heat Equation (Pure and Applied Mathematics), Academic Press, 1975.
28. L. Baowen, L. Wang, and G. Casati, "Negative differential thermal resistance and thermal transistor," Applied Physics Letters, vol. 88, 2006.
29. D. Nika, E. P. Pokatilov, A. Askerov, and A. Balandin, "Phonon thermal conduction in graphene: Role of umklapp and edge roughness scattering," Physical Review B, vol. 79, 2009.
30. J. Hone, M. Whitney, C. Piskoti, and A. Zettl, "Thermal conductivity of single-walled carbon nanotubes," Physical Review B, vol. 59, no. 4, pp. 2514–2516, 1999.
31. S. Hepplestone, A. Ciavarella, C. Janke, and G. Srivastava, "Size and temperature dependence of the specific heat capacity of carbon nanotubes," in Proceedings of the 23 rd European Conference on Surface Science, vol. 600, no. 18, September 2006, pp. 3633–3636.
32. A. Naemi and J. Meindl, "Performance benchmarking for graphene nanoribbons, carbon nanotubes and Cu interconnects," International Interconnect Technology Conference, 2008.
33. A. Naemi and J. D. Meindl, "Design and performance modeling for single-wall carbon nanotubes as local, semi-global, and global interconnects in gigascale integrated systems," IEEE Transactions on Electron Devices, vol. 54, pp. 26–37, 2007.
34. S. Rakheja and A. Naemi, "Modeling Interconnects for Post-CMOS Devices and Comparison With Copper Interconnects," IEEE Trans. Electron Devices, vol. 58, no. 5, pp. 1319–1328, May 2011.
35. S. Datta, Quantum Transport: Atom to Transistor, 1st ed., Cambridge University Press, 2005.
36. A. Khitun, M. Bao, Y. Wu, J. Y. Kim, A. Hong, A. Jacob, K. Galatsis, and K. Wang, "Logic devices with spin wave buses - an approach to scalable magneto-electric circuitry," Material Research Society Symposium, vol. 1067, 2008.

37. A. Khitun, D. E. Nikonov, B. Mingqiang, K. Galatsis, and L. K. Wang, "Feasibility study of logic circuits with a spin wave bus," *Nanotechnology*, vol. 18, no. 46, 2007.
38. M. Cottam, *Linear and non-linear spin waves in magnetic films and superlattices*. World Scientific, 1994.
39. R. de Sousa and J. E. Moore, "Multiferroic materials for spin-based logic devices," arXiv: 0804.1539v1.
40. R. DeSousa and J.E.Moore, "Multiferroic materials for spin-based logic devices," *Journal of Nano-electronics and Optoelectronics*, vol. 3, no. 77, 2008.
41. N. Pyka, L. Pintschovious, and A. Rumiantsev, "High energy spin dynamics of La_2CuO_4 and $\text{La}_{1.9}\text{Sr}_{0.1}\text{CuO}_4$," *Z.Phys. B-Condensed Matter*, vol. 82, 1991.
42. D. B. Miller, "Device requirements for optical interconnects to silicon chips," *Proceedings of the IEEE*, vol. 97, no. 9, pp. 1166–1185, July 2009.
43. L. Pavesi and G. Guillot, *Optical Interconnects: The Silicon Approach*, 1st ed., Springer, 2006.
44. S. A. Maeir, M. L. Brongersma, P. Kik, S. Meltzer, A. Requicha, and H. A. Atwater, "Plasmonics: A route to nanoscale optical devices," *Advanced Materials*, vol. 13, 2001.
45. J. Conway, S. Sahni, and T. Szkopek, "Plasmonic interconnects versus conventional interconnects: A comparison of latency, cross-talk and energy costs," *Optics Express*, vol. 15, 2007.
46. W. Barnes, A. Dereux, and T. Ebbesen, "Surface plasmon subwavelength optics," *Nature*, vol. 424, August 2003.
47. A. Khitun, M. Bao, and K. L. Wang, "Spin wave magnetic nanofabric: A new approach to spin-based logic circuitry," *IEEE Transactions on Magnetics*, vol. 44, no. 9, September 2008.

Chapter 6

Formation of Epitaxial Graphene

D. Kurt Gaskill and Luke O. Nyakiti

Epitaxial Graphene (EG) has exceptional electronic properties that make it suitable for use in the fabrication of scalable, high frequency graphene field effect transistors, with cut-off frequencies in the gigahertz range. This chapter discusses recent advances in the growth, structural and electronic properties of epitaxial graphene on 4H- or 6H-SiC substrates. The first two sections of the chapter discuss a historical perspective on the development of graphene growth by Si-sublimation and provide basic information about the SiC substrate. The last section highlights comparative surface morphological variations as well as electronic properties of graphene grown under ultra high vacuum, intermediate vacuum and in Ar or controlled environment for the two polar surfaces of SiC. This chapter concludes by discussing potential obstacles to graphene growth and device development, such as the creation of a band gap, controlling doping, and uniformity of layers and suggest potential research areas for future investigations.

6.1 History

The first deliberate (yet, unidentified) formation of graphene due to the sublimation of Si from SiC most likely took place in the 1890s in experiments by Edward Acheson. In a search for durable industrial abrasives, Acheson had developed a process for making SiC—the material he first named carborundum [1]. Later, his experiments on heated SiC implied that the Si would sublime at high temperatures and leave behind graphitic carbon [2]; this process most likely began with the formation of graphene. Interest in semiconductors grew in the second half of the twentieth century, leading to a study of SiC surfaces using low energy electron

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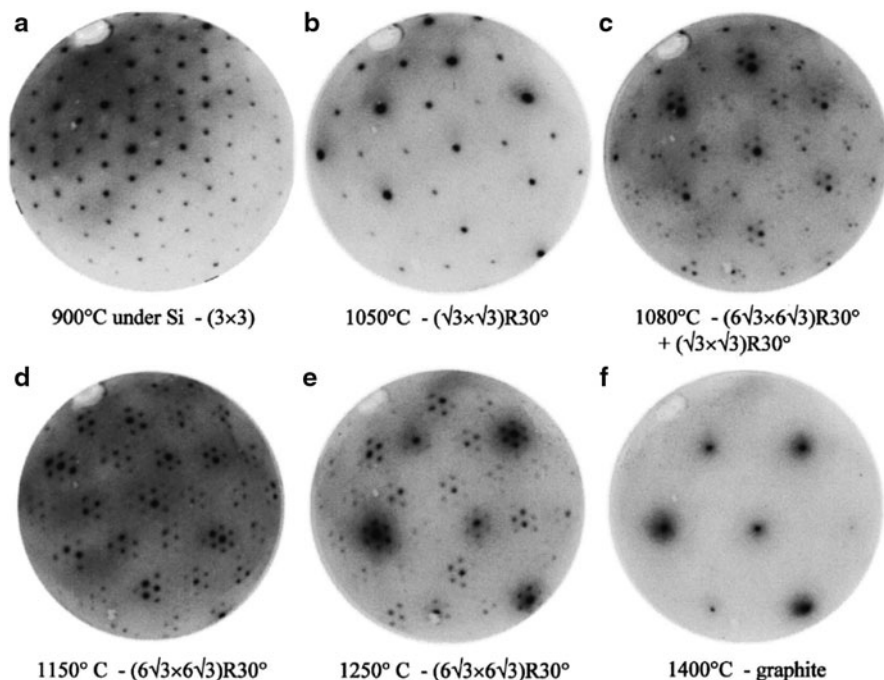


Fig. 6.1 LEED patterns from 6H-SiC (0001) with a primary energy of 130 eV obtained on (a) (1×1) , (b) $(\sqrt{3} \times \sqrt{3})$ R30°, (c) $(\sqrt{3} \times \sqrt{3})$ R30° and $(6\sqrt{3} \times 6\sqrt{3})$ R30°, (d) and (e) $(6\sqrt{3} \times 6\sqrt{3})$ R30°, and (f) graphite (1×1) (Reproduced with permission from [4]. © 1998 American Physical Society)

diffraction (LEED) and Auger electron spectroscopy by van Bommel et al. [3] Van Bommel, aware of the Si sublimation process, controllably heated the SiC surface and found that the rate of carbon formation was greater on the $(000\bar{1})$ polar face than on the (0001) face. In addition, the lattice constant was found to be similar to that of graphite and had a distinct crystallographic relation to the SiC crystal; the $(6\sqrt{3} \times 6\sqrt{3})$ R30° (for brevity, $6\sqrt{3}$) reconstruction of the (0001) surface was noted. Forbeaux et al. heated (0001) surfaces to successively higher temperatures showing the evolution of the surface as it became more graphite-like, as shown in Fig. 6.1 [4]. In addition, Forbeaux also identified Si vacancies in C-rich subsurface layers as a precursor to graphite formation by layer collapse, i.e., Si sublimation. In 2002, Charrier and co-workers controlled the Si sublimation rate from an electronic grade 6H-SiC wafer such that a single layer or few layers of graphene were formed on (0001) n^+ SiC and having the bulk graphite lattice parameter [5].

Just 2 years later the field of graphene research began its rapid rise to prominence beginning with three publications. Novoselov et al. demonstrated the electric field effect on exfoliated graphene [6], and Berger and colleagues demonstrated that few layers of graphene, formed by Si sublimation (“grown”) from SiC under ultrahigh vacuum (UHV) conditions (named epitaxial graphene) had very

interesting magnetoconductance properties [7]; both groups demonstrated that graphene could be patterned using conventional lithographic approaches. Shortly after, Zhang and co-workers described the relatively unique quantum Hall effect (QHE) and Berry's phase for exfoliated graphene. By 2006, the first description of an intermediate vacuum process, i.e., $\sim 10^{-5}$ mbar, for graphene on (0001) was provided [9]; then the application of this process for (0001) was described in late 2007 [10]. Soon afterward there was report of graphene growth using the UHV approach on a 75 mm 4H SiC wafer [11]. The Ar growth process was developed in 2008 [12]. In late 2008, growth of graphene on a 50 mm (0001) 6H SiC wafer using an intermediate vacuum process in a commercial chemical vapor deposition (CVD) reactor was reported [13, 14]. Wafer-scale epitaxial graphene grown under an argon atmosphere was noted in late 2008 on 50 mm 6H [15] and in late 2009 on 75 mm 6H [16]. With the ready availability of 100 mm SiC wafers in both 4H and 6H polytypes and in n^+ and semi-insulating conductivity types, plus the recently announced experimental development of 150 mm 4H SiC wafers [17], it is expected that larger area epitaxial graphene wafers will soon be synthesized.

Due to the relative youth of research in epitaxial graphene, there are few reviews that cover advancements in its growth and associated properties. The article by Haas and co-workers covers a great amount of information on the growth, structure and properties of epitaxial graphene that was current when written [18]. Seyller and co-workers review the photoemission, structural and electrical properties of graphene formed mainly by a UHV process [19] and de Heer et al. discusses the electronic structure and transport properties [20]. In this chapter, various approaches to grow epitaxial graphene on polar SiC surfaces are described; some of the properties of these ultra thin films are also discussed.

6.2 Background on SiC and Substrate Preparation for Graphene Synthesis

SiC is known to have at least 200 crystallographic variants called polytypes. These polytypes all have equal numbers of Si and C that are predominantly covalently bonded and are distinguished by different C–Si bilayer stacking sequences. The most common polytypes that are considered for electronic applications are cubic (zincblend): 3C; hexagonal (wurtzite): 4H and 6H; and rhombohedral: 15R. Table 6.1 compares the bandgaps and lattice constants of the polytypes along with the in-plane lattice constant and interplanar spacing for graphite. Many of the polytypes of SiC have been extensively investigated and a compendium of their properties can be found in, for example, Harris [26].

Commercially available, high quality, high purity 4H and 6H SiC wafers are sawn and polished from boules that are typically grown by the physical vapor transport process. This process takes place at high temperatures, $>2,000^\circ\text{C}$ [27]. Wafers can be doped n-type (resistivity, ρ , is typically $0.02\ \Omega\ \text{cm}$) or

Table 6.1 The room temperature band gaps and lattice constants for the common polytypes of SiC. The band gap of 3C is direct (D) whereas the others are indirect (I). For comparison, the in-plane lattice constant and interplanar distance for graphite is included. The Si-C layer spacing in the stacked layers for 4H, 6H, and 15 R are all approximately 2.52 Å

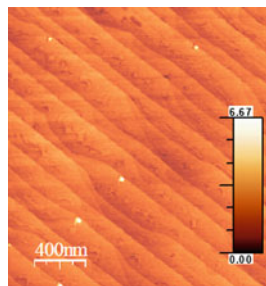
SiC Polytype	Band gap 300 K (eV)	a (Å)	c (Å)
3C [22]	2.36 (D)	4.3596	–
4H [23]	3.23 (I)	3.08051	10.08480
6H [23]	3.00 (I)	3.08129	15.11976
15R [24]	2.99 (I)	3.0813	37.7882
Graphite [25]	–	2.4589	3.354

semi-insulating ($\rho > 10^8 \Omega \text{ cm}$) and are available in different orientations; typical orientations are basal plane (also known as vicinal) or slightly misoriented from the basal plane by an offset towards either the $(11\bar{2}0)$ or (1100) directions for various angles, e.g., 8° . The (0001) polar face is often referred to as Si-face, and the $(000\bar{1})$ polar face as C-face. Both faces can be specified from substrate vendors.

SiC wafers contain various defects in a range of densities and the impact of defects on SiC-based devices have been extensively investigated, for example see [28]. The main defects are mixed polytypes, open core screw dislocations known as micropipes (because the defect typically has a diameter of order a micrometer or more), low angle grain boundaries, and conventional dislocations such as threading screw and threading edge dislocations and basal plane dislocations [22]. There has been considerable recent progress in SiC wafer technology which has lead to economically competitive commercial devices for low voltage power electronic and GaN light-emitting diode applications [29].

Significant progress has been made in preparing SiC wafers for epitaxy. However, since SiC is a very hard material, as such it is difficult to polish without leaving defects, i.e., polishing scratches. Removing these defects is desirable, so as to prepare a smooth surface with uniform orientation before graphene growth. A typical approach to prepare the surface is as follows: the wafer is cleaned in solvents, usually ending with an HF dip [30]. Following this, etching of the SiC surface is performed using flowing hydrogen at temperatures above $1,500^\circ\text{C}$ to remove the damaged surface layer from the substrate [31]. After etching in 100 mbar of hydrogen for about 5 min. at $1,600^\circ\text{C}$, substrates with nominally 0° misorientation for the Si-face show a terrace and step morphology, with the step heights being 0.25–0.50 nm (1–2 Si-C planar distances); Fig. 6.2 shows an atomic force microscopy (AFM) image of this morphology. For the C-face, morphology similar to that of (0001) is observed but with steps about 1.0 (1.5) nm in height corresponding to 4 (6) planar distances for 4H (6H)–SiC [32]. In each case, an estimated 300 nm of substrate material was removed. In addition to the removal of polishing defects, hydrogen etching has further value as was demonstrated in an x-ray scattering investigation of graphene grown on etched and unetched C-face. The etched surface exhibited significant reduction in background scattering intensity associated with point defects or local disorder at the graphene-substrate interface [18].

Fig. 6.2 Atomic force microscopy image of (0001) 6H-SiC morphology after hydrogen etching in 100 mbar at 1,600°C for 5 min. The scale is in nm (Adapted from [32])



6.3 Epitaxial Graphene: Theoretical Basis and Synthesis

6.3.1 Theoretical Basis

The band structure and electronic transport properties of sp^2 bonded carbon sheets, i.e., graphene, are affected by the interfaces between the active material and its surroundings; *ab initio* calculations show that carbon sheets on SiC behave with the same chiral properties as exfoliated graphene. The first band structure descriptions were given by Mattausch [33] and by Varchon [34]. In each case, the SiC surface was assumed to be reconstructed into the $6\sqrt{3}$ configuration but, since this was computationally expensive, the reconstruction used in the calculations was the simpler $(\sqrt{3} \times \sqrt{3}) R30^\circ$; the lattice was also stretched to accommodate the mismatch with the graphene unit cell. The density functional theory approach was used to calculate the band structure and Fig. 6.3 shows the results for both polar faces of SiC with 1, 2 and 3 carbon sheets assuming Bernal stacking. In each case, the first carbon layer is found to be covalently bonded to the reconstructed interface with distances less than those between graphene layers ($3.35 \text{ \AA}$ —see Table 6.1); thus, the first layer becomes an interface layer (IFL) between the SiC and the graphene, Fig. 6.3a and b. The second sheet of carbon gives rise to the linear dispersion characteristic of graphene. For the Si-face, the IFL is metallic and graphene is n-type (the Fermi energy (E_F) is 0.4 eV above the Dirac point) due to charge transfer from the dangling bond of the lonely Si atom at the interface, Fig. 6.3c. For the C-face, no doping is anticipated and the dangling bond state makes the IFL semimetallic, Fig. 6.3d. With the addition of a third carbon sheet, a bilayer graphene configuration is obtained and a potential band gap can be formed for both faces, Fig. 6.3e and f.

As will be seen in Sects. 6.3.3.2 and 6.3.3.4, the interface details for C-face assumed above are not correct; Magaud and co-workers used an *ab initio* approach with no interface layer and still found the linear dispersion in the band structure characteristic of graphene [35]. Later, Jayasekera accounted for the van der Waals force between adjacent graphene layers and found no evidence for an interface layer for graphene growth on C-face. In addition, they found the first graphene layer on the Si-face is expected to be n-type due to the charge transfer from the dangling

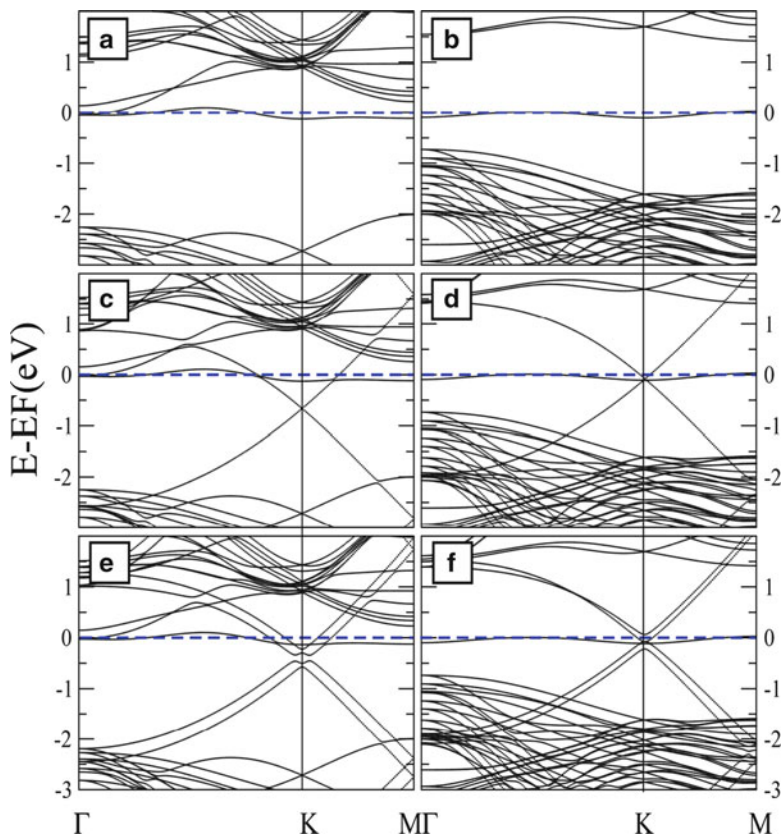


Fig. 6.3 Dispersion curves for one (a), (b), two (c), (d), and three (e), (f) carbon layers on bulk truncated SiC. Curves (a), (c), and (e) [(b), (d), and (f)] correspond to the Si- (C-) terminated face. The first C layer forms an IFL layer with no graphene-like dispersion (a), (b). The second C layer—on top of the IFL—shows a linear dispersion (c), (d) characteristic of a single graphene sheet. Two C layers on top of the IFL show a splitting of the Dirac bands (e), (f) as expected for a free graphene bilayer (Reproduced with permission from [34]. © 2007 American Physical Society)

bond states at the SiC surface [36]. The second graphene layer was assumed to be Bernal stacked and the typical bilayer graphene band structure was found.

6.3.1.1 Preliminaries on Growth: Is It Really Graphene?

The first report of epitaxial graphene were for samples formed in UHV, 10^{-10} Torr [7], using conditions similar to those reported in previous SiC surface studies [4, 5, 37]. Later, epitaxial graphene was formed in an intermediate vacuum, $\sim 10^{-6}$ – 10^{-4} mbar [9, 10]. Soon after, graphene growth in a relatively high pressure Ar ambient, 1 to several hundred mbar, was demonstrated [12]. Recently, graphene

Table 6.2 Comparison of properties of carbon films synthesized by various processes. The properties compared are: lattice constant, linear dispersion of the band structure, Landau level energies linearly dependent on $B^{1/2}$, the anomalous Berry’s phase of π for graphene, presence of an interface layer (IFL, symmetry given), observation of the quantum Hall effect (QHE), magnitude of the Fermi velocity (V_F), presence of Shubnikov-de Haas oscillations, and demonstration of field effect transistor (FET)

Process	Lattice constant	Linear dispersion of E_G	Landau level energy $f(B^{1/2})$	Anomalous Berry’s phase	IFL	QHE	V_F ($m\ s^{-1}$)	SdH	FET
UHV Si-face	2.4 Å	Yes		Yes	6√3		7.2×10^5	Yes	Yes
UHV C-face	2.465 Å	Yes			No				
Intermediate Vacuum Si-face	2.49 Å			Yes	6√3	Yes		Yes	Yes
Intermediate Vacuum C-face	2.3 Å	Yes	Yes	Yes	No	Yes	1.03×10^6	weak	Yes
Ar Si-face	2.5 Å	Yes			6√3	Yes			Yes
Ar C-face			Yes		No				
Confined process C-face				Yes		Yes	1.14×10^6		

has been formed in a confined volume to control the Si vapor pressure [38]. In all cases, *graphene* was claimed to have formed on Si and C-faces of SiC. Yet, each of these approaches (potentially) form carbon sheets with different interfaces and stacking sequences. So, is graphene really formed in each case? Table 6.2 summarizes information presented in the remainder of this chapter for each graphene formation approach. The correct lattice constant is a necessary but not sufficient condition to demonstrate graphene—ideally, the linear dispersion of the band structure is the necessary evidence. A linear dependence of Landau level energy spacing on the square root of magnetic field is consistent with graphene [39]. Also, possessing the anomalous Berry’s phase of π demonstrates the chiral nature of graphene [8]. The presence of an IFL at the SiC surface (and its symmetry) is of interest from a theory perspective when comparing different graphene formation approaches. Finally, other interesting properties are listed such as the Fermi velocity (V_F) and the QHE as well as noting whether field effect transistors (FETs) have been made.

The data in Table 6.2 supports the argument that graphene has been synthesized by all the SiC process approaches, although the evidence for the last entries are weaker.

6.3.1.2 Why Does It Work?

It is not surprising that graphene can be formed over a wide range of process conditions after considering the pressure-temperature diagram of volatile Si and

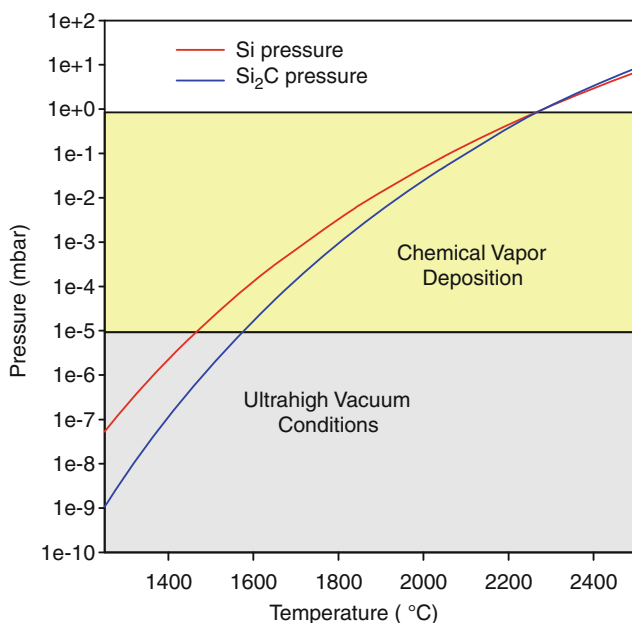


Fig. 6.4 The pressure–temperature phase diagram is shown for volatile Si and Si_2C over SiC. For a given temperature, the necessary vacuum conditions can be determined to remove the sublimated Si from the sample, thus enabling graphene growth

Si_2C over a SiC substrate, Fig. 6.4, calculated by Jernigan [40] [14], using the parameters found in Lilov [41]; note that partial pressure of carbon is much lower for temperatures less than 2,000°C. The diagram shows that under UHV conditions, graphene growth can be accomplished at temperatures below about 1,450°C since the sublimated Si can be swept away by the vacuum system. At higher temperatures, intermediate vacuum conditions will suffice. Inert blanket gases such as Ar can be added as long as the process gas control system mitigates Si condensation on the surface. Implicit in the pressure–temperature relationship is that the growth rate also increases as the temperature increases—this is because more Si is sublimated which implies more C is liberated for graphene growth. This means that the graphene growth rate can be controlled through temperature—the rate of Si generation—and the speed of Si moiety removal. This simple model makes use of the assumption that the surface reconstruction of SiC before graphene growth is relatively constant over a wide temperature range and so graphene nucleation processes are unchanged; UHV studies show that for Si-face the $6\sqrt{3}$ reconstruction is energetically favorable for temperatures above $\sim 1,150^\circ\text{C}$ [12], whereas for the C-face the reconstruction combinations $(3 \times 3)_\text{C}$ and $(2 \times 2)_\text{C}$ are favorable above $\sim 800^\circ\text{C}$; both cases persist to at least 1,500°C, the highest temperature probed. [4] This simple pressure–temperature model becomes less predictive when comparing growth on polar faces, since the surface properties of the faces impact graphene formation.

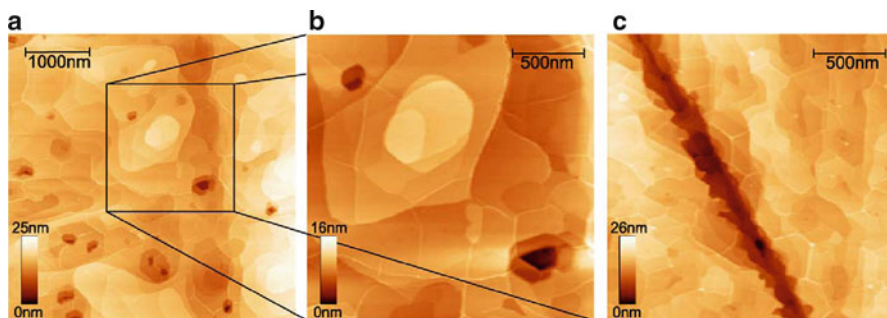


Fig. 6.5 Typical AFM images of graphite layers grown on a high-quality on-axis oriented (0001) 6H-SiC. Panel (c) is recorded at a polishing scratch in the substrate. Pitting can be seen in panels (a) and (b) (Reproduced with permission from [42]. © 2006 Elsevier)

The next sections will describe the three main growth approaches, which are differentiated by process pressure: UHV (10^{-10} Torr), intermediate vacuum (10^{-6} – 10^{-4} Torr), and blanket gas (usually Ar, >1 Torr). As will become clear, the properties of graphene grown on the two SiC polar surfaces are very different, and so are described separately; in addition, it will be seen that some properties are sensitive to the process pressure. Since the properties of graphene, such as band structure, are intimately connected to the surface on which it resides, the interface with the underlying SiC will be discussed in some detail. Some gaps in current understanding will be noted.

6.3.1.3 UHV Synthesis of Epitaxial Graphene, Si-Face

The process for forming graphene in UHV differs little from the early (e.g., before 2004) descriptions used in various surface science investigations. Seyller's 2006 description for Si-face samples is repeated *verbatim* here [42].

"After load-locking the samples into the UHV system they were annealed at 950°C in a flux of Si. This procedure results in the formation of a Si-rich (3×3) reconstruction. The excess Si was then removed from the surface by further annealing steps at $1,050^{\circ}\text{C}$, $1,150^{\circ}\text{C}$ and $1,400^{\circ}\text{C}$ leading to the Si-rich ($\sqrt{3} \times \sqrt{3}$)R 30° structure, the carbon rich ($6\sqrt{3} \times 6\sqrt{3}$)R 30° structure and finally the graphitized surface, respectively."

Except for very early reports, all work employed some form of surface preparation to mitigate polishing damage. For graphene growth under UHV conditions on Si-face, the typical graphitization temperature range is $1,250$ – $1,350^{\circ}\text{C}$ [43–45] yet temperatures up to $1,600^{\circ}\text{C}$ have been investigated [46]. The morphology of graphene shows vestiges of the original (often hydrogen etched) substrate step and terrace structure (this is variable with reports); the terrace widths are up to several hundred nm in extent and the step heights reported ranged from 0.25 to 0.75 nm, although Seyller [42] notes step bunching heights of 2 nm; Fig. 6.5 shows AFM examples of this morphology. Note that pits and low profile ridge structures can be observed; in

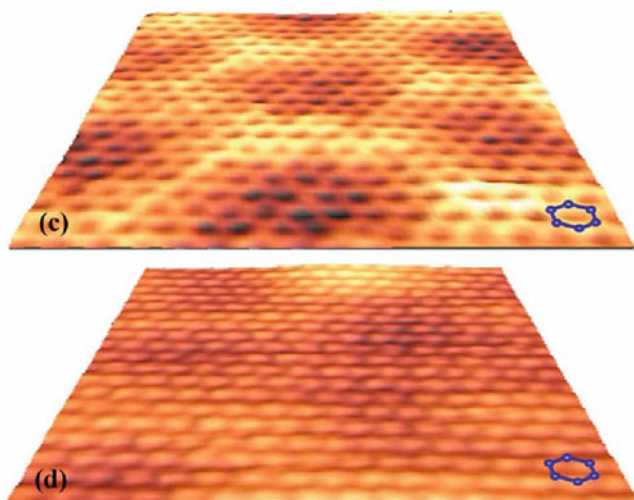


Fig. 6.6 STM 3D images ($4 \times 4 \text{ nm}^2$) for monolayer (c) and bilayer graphene (d) grown on (0001)6H-SiC. A hexagonal graphene unit cell is depicted in both images (Reproduced with permission from [48]. © 2007 American Physical Society)

general, the morphology is rough and irregular. Yet, small area scanning tunneling spectroscopy (STM) scans ($200 \times 200 \text{ Å}^2$) reveal rms roughness is 0.2 Å (0.1 Å) for monolayer (bilayer) graphene [47]. In addition, it has been noted from STM images that graphene “covers the step like a carpet” [42] and the graphene lattice constant of $2.4 \pm 0.2 \text{ Å}$ is confirmed [48]. STM image examples of monolayer and bilayer graphene hexagonal lattices are shown in Fig. 6.6 [48]. Multilayer growth is relatively easily obtained as thicknesses from one to five or more layers have been reported.

The UHV approach yielded opportunities to employ surface analytical tools. As mentioned earlier, the Si-face samples were found to have the $6\sqrt{3}$ reconstruction beginning at about $1,150^\circ\text{C}$ and this continued until graphene formation. Using STM methods, Reidl shows the $6\sqrt{3}$ reconstruction persists beneath the graphene [44] and he provides a schematic of the atom and atom cluster positions; it was noted that subtle changes in elements of the reconstruction appear to be preparation dependent. LEED demonstrates that the overlying graphene is epitaxial with respect to the underlying SiC substrate [7] showing that the graphene layers are aligned with respect to substrate so that the primitive translation vectors enclose an angle of 30° [3, 49]. Graphene growths for various coverages were investigated by Emtsev using x-ray photoelectron spectroscopy (XPS) [49]; initially the C 1s core spectra contained three peaks for the reconstructed surface: S1, S2 and a SiC derived peak; Fig 6.7a illustrates these peaks. Experiments using variations in the inelastic electron mean free path did not change the ratio of S1 to S2 and hence these demonstrated that the carbon source atoms for S1 and S2 were contained in the same plane. Furthermore, with additional graphene layers, the ratio of S2 to the SiC peaks stayed constant, shown in Fig 6.7b (inset), indicating that the associated

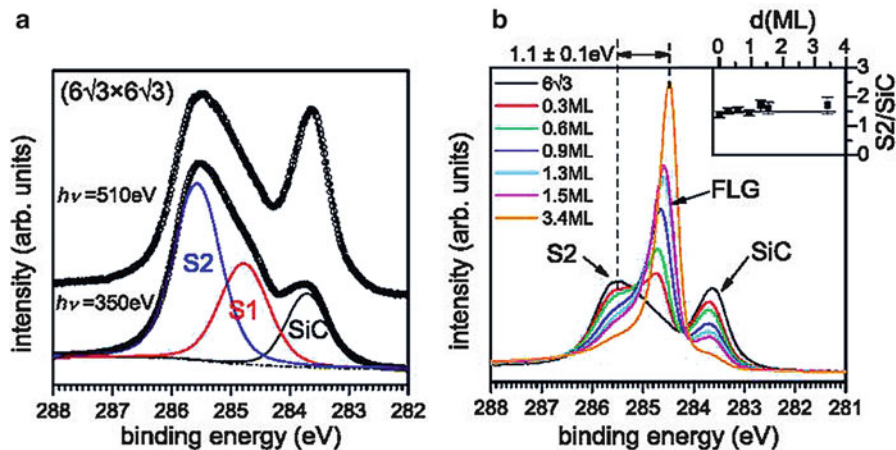


Fig. 6.7 (a) XPS C 1s core-level spectrum of the $6\sqrt{3}$ reconstruction on (0001)6H-SiC showing the S1, S2 and SiC derived peaks from fits. (b) Shows the evolution of the C 1s core-level spectrum upon the growth of up to 3.4 ML of graphene. The inset shows the intensity ratio of component S2 to bulk component SiC for measurements at $h\nu = 510$ eV as a function of thickness (Reproduced with permission from [49]. © 2008 American Physical Society)

bonding configuration remained unchanged during the growth process. Further analysis of the XPS data showed that approximately 1/3 of the density of carbon atoms—those associated with S2—strongly interact with the underlying SiC (peak S2 has an sp^3 character) and the remaining 2/3 of the density of carbon atoms—those associated with S1—do not strongly interact with the substrate (S1 is buried under the graphene peak as both have sp^2 character). Hence, the $6\sqrt{3}$ reconstruction is between the SiC substrate and the graphene and thus it represents an IFL that has a strong interaction with the SiC substrate; assuming the reconstructed layer has the same C-C bond lengths and C atom density, Emtsev notes that it must have an effective thickness of 2.4 ± 0.3 Å.

Charrier used LEED to show that two graphitic layers formed by annealing (0001) above $1,200^\circ\text{C}$ have the Bernal stacked structure [5]—similar to what is observed in graphite [50]. Ohta and co-workers calculated the expected band structure for bilayer, trilayer and quadlayer epitaxial graphene for both Bernal and rhombohedral stacked epitaxial graphene; comparing the band structure predictions to band structure measurements, obtained by angle-resolved photoemission spectroscopy (ARPES) on samples prepared using the UHV approach, showed that multilayer graphene grown on Si-face is Bernal stacked [51]. In addition, a rhombohedral stacking component was also noted for the trilayer case, but adding a fourth graphene layer stabilizes the structure to Bernal stacking [52]. Hass used x-ray scattering experiments to probe the IFL [53]. The data was fit to a model that used the Bernal stacked sequence for graphene and three different IFL models that consisted of a dense carbon layer with a partial layer of Si atoms in different configurations. Fits of the x-ray scattering data with each IFL model were all about

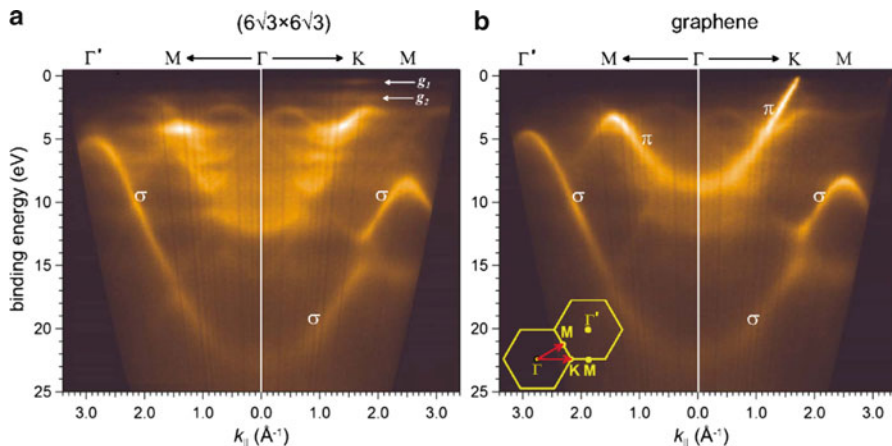


Fig. 6.8 Photoelectron intensity map vs binding energy and parallel electron momentum of (a) SiC(0001) – $6\sqrt{3}$ and (b) 1 ML graphene on top of SiC(0001) – $6\sqrt{3}$ ($h\nu = 50$ eV). The inset shows the direction of $k_{\parallel}$ within the hexagonal Brillouin zone of graphene. Note that there are no states near E_F in panel (a) other than the localized states, g_1 and g_2 , which have binding energies of 0.5 and 1.6 eV, respectively (Reproduced with permission from [49]. © 2008 American Physical Society)

the same, and so the true construction of this layer could not be conclusively identified, yet it does imply a complex interface and decidedly not a simple layer of graphene placed over a reconstructed Si-face surface. A long range order of ~ 290 Å was found for both 1 and 2 ML of graphene. The IFL—graphene spacing was found to be 2.32 ± 0.08 Å. This spacing was confirmed by an STM value of 2.6 ± 0.4 Å [54]. The x-ray fits also yielded a first to second graphene layer spacing of 3.50 ± 0.05 Å and subsequent spacings were 3.35 ± 0.01 Å; the latter spacing is similar to what is expected from graphite values (see Table 6.1) whereas the reason for the wider first spacing is not known at this time.

Emtsev and co-workers used ARPES to explore changes in the band structure as the first layer of carbon formed on the reconstructed layer (thus becoming the IFL). The IFL interacts with the underlying surface by covalent bonds and hence lacks a well-defined π -band, see Fig. 6.8a, instead only the σ -band, due to localized bonding in the $6\sqrt{3}$ reconstructed layer, is present [49]. As there are no states near E_F then the IFL is semiconducting (and apparently insulating below 300 K); it also possesses two surface states, g_1 and g_2 , located 0.5 and 1.6 eV below E_F , respectively. As the graphene forms, the π -band becomes prominent, see Fig. 6.8b, and graphene electronic transport is manifested and is accessible since the IFL electrically isolates the graphene layer from the substrate.

The electrical properties of UHV Si-face graphene were first probed by Berger et al. where it was noted that a 3 ML film was n-doped about $3.6 \times 10^{12} \text{ cm}^{-2}$ with mobility of $1,100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 4 K [7]. It was later noted that the film thickness was more likely 1 ML [20]. Others also noted the natural occurrence of n-type

doping in monolayer graphene with E_F above the Dirac point, by 260 meV [55], 400 meV [19], and 450 meV [52] often suggesting it was due to charge transfer from the doped substrate or due to a built-in electric field near the IFL [43]. *Ab initio* calculations point to the dangling bond associated with the lonely Si atom in the IFL as giving rise to the observed n-type charge transfer; this would occur even for semi-insulating SiC substrates [33, 34]. From ARPES measurements, Ohta also noted n-type behavior and extracted tight binding parameters including E_F for 1, 2, 3 and 4 ML obtaining 440, 300, 210, and 150 meV, respectively [51]. Since the total sheet charge density did not change much, it was concluded that screening results in a charge redistribution, with an effective screening length of 1.4 and 1.9 Å for 3 and 4 ML, respectively. Samples grown this way showed Shubnikov-de Haas oscillations, anomalous Berry's phase characteristic of graphene, yielded a V_F of $7.2 \times 10^5 \text{ cm s}^{-1}$ and showed gated conductance changes [7, 43]. Small samples patterned into field effect transistors have been reported [56].

6.3.1.4 UHV Synthesis of Graphene, C-Face

Similar to UHV graphene growth on Si-face, C-face growths used previously described surface preparation recipes. Earlier, van Bommel had noted that the growth rate of carbon on the C-face was over an order of magnitude faster than on the Si-face for temperatures near 1,300°C [3]. Reports on the morphology of UHV graphene on C-face are limited, mainly because the resulting films were of poor quality both morphologically and electrically. Kusunoki noted the formation of nanocaps on the substrate surface leading to a rough morphology [57]. Jernigan used growth temperatures from 1,200°C to 1,600°C and noted the films were granular in nature resulting from an islanding growth mode [46]. Film thicknesses, measured by attenuation of the Si 2p XPS signal from the SiC substrate, were reported to be up to 2.8 nm (8 ML). Recently, Creeth et al. explored growth conditions from 1,250°C to 1,450°C and found granular morphology for low temperatures (size scale 20 nm) and increased grain sizes at 1,450°C (up to 1 µm); AFM images of this morphology can be seen in Fig. 6.9 [58]—up to 4 ML were formed.

The C-face surface reconstruction of (3×3) and $(2 \times 2)_{\text{Si}}$ begins at 800°C and persists above 1,400°C [3, 59]. Upon graphitization, the $(2 \times 2)_{\text{C}}$ reconstruction coexists with the $(3 \times 3)_{\text{C}}$ and $(1 \times 1)_{\text{graphite}}$ structures. At 1,500°C, surface carbon is noted and the unit mesh dimension was found to be 2.465 Å (corrected for the updated 6H lattice constant) in agreement with graphite (see Table 6.1) [3]. Surface analysis shows that the graphene layers are rotationally disordered as the diffraction pattern was smeared out azimuthally, yet a strong intensity modulation in the streaks indicates that there are preferential rotational angles [19]; this disordered graphene is sometimes referred to as turbostratic graphene. In contrast to the Si-face case, there is a lack of strong coupling between the graphene and the substrate, as evidenced by XPS C 1s core levels showing only two peaks for the film and substrate and thus lacking an interface peak (see Fig. 6.7 for the Si-face case) [49]. Both σ and π bands are noted by ARPES measurements for 0.3 ML coverage

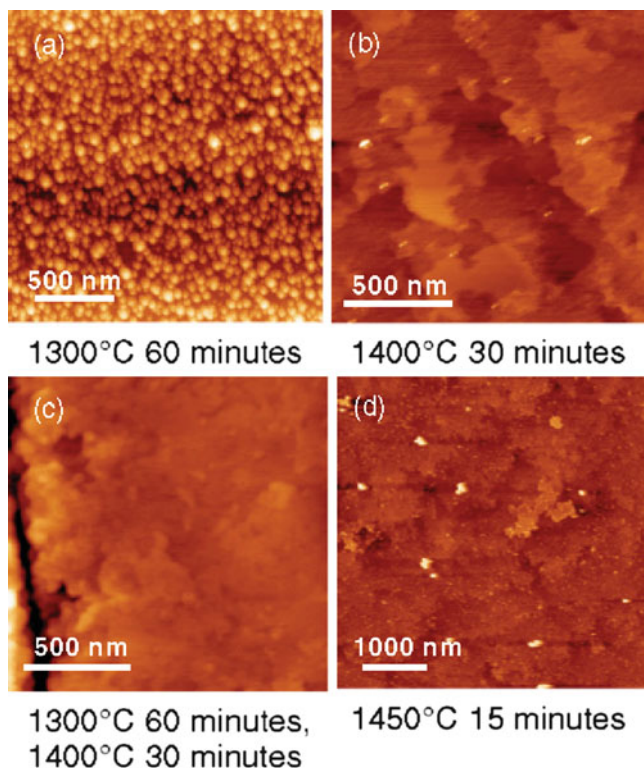
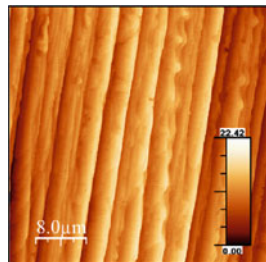


Fig. 6.9 AFM images of graphene formed from (000 $\bar{1}$)6H-SiC in UHV for (a) 60 min. at 1,300°C, (b) 30 min. at 1,400°C, (c) 60 min. at 1,300°C followed by 30 min. at 1,400°C and (d) 15 min. at 1,450°C. Note the variation in lateral scale between the images. The full range of the height scale in panel (a) is 20 nm, in panels (b) and (c) is 6 nm, and in (d) is 4 nm. The white spots in panel (d) are debris on the surface (Reproduced with permission from [58]. © 2011 American Physical Society)

and SiC bulk bands are almost completely attenuated with nearly a monolayer of coverage. No perturbations to the patterns are evident, unlike the Si-face case; this, when coupled with no evidence for an interfacial layer, implies weak coupling between the graphene and the substrate; Even at 0.3 ML coverage signatures of rotated domains are noted which persists with additional growth; this means that rotated domains exist at the very beginning of graphene growth.

The electrical properties of UHV graphene on C-face are relatively poor. Jernigan noted high resistances and 300 K Hall measurements yielded p-type carrier densities of $1.4\text{--}6.4 \times 10^{13} \text{ cm}^{-2}$ with associated mobilities ranging from 29 to $4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$; the higher mobility was obtained for a 1,600°C growth [46]. Creeth noted conductive films for a growth temperature of 1,450°C; they ascribed the temperature dependence of the resistance as due to variable range hopping [58].

Fig. 6.10 AFM image of graphene morphology grown on (0001)6H-SiC. Step bunching is evident and the terrace widths are up to 3–4 μm . The height scale is in nm (Adapted from [32])



6.3.1.5 Intermediate Vacuum Synthesis of Epitaxial Graphene, Si-Face

Wu first described EG growth on the Si-face using an intermediate vacuum process in 2007; the samples were formed by combining a hydrogen etch step with the graphene formation step in a commercial SiC CVD reactor [10]. Incomplete synthesis is noted at 1,300°C with growth occurring only next to substrate steps [60]. Complete graphitization takes place from 1,350 to 1,650°C in a pressure of about 10^{-7} mbar [10, 32] to as high as 2×10^{-4} mbar [32]. Morphology is considerably improved compared to the case of Si-face grown in UHV, as can be seen in comparing AFM images in Fig. 6.10 (intermediate vacuum) with Fig. 6.5 (UHV). Enhancement of step heights was noticed at 1,400°C [61] and steps with heights of 1.2–1.4 nm [10] and 1–15 nm [32] are noted for temperatures above 1,500°C; step bunching of the underlying substrate was thought to be the cause [32]. In addition, pitting was noted and graphene was found on the pit floor [10]. Terraces are wider than the UHV case and widths of up to 3–4 μm were found [32] with STM measured roughness of about 0.2 nm [10]. The graphene lattice spacing was confirmed by STM as 0.245 nm [62] and 0.249 ± 0.01 nm [61]. Bolen studied the growth rate as a function of temperature and time; the results are summarized in Fig. 6.11: panel (a) shows surface coverage vs growth temperature for 10 min of growth and panel (b) shows surface coverage vs growth time at a growth temperature of 1,475°C [61]. Thicknesses from 1 ML to ~25 ML (8 nm) have been reported [32] and 4° off-cut orientation increases the graphene thickness compared to vicinal orientation [60]; presumably, this is because of additional carbon diffusing from the many closely spaced SiC surface steps.

Jernigan and co-workers showed that the XPS C 1s core level spectra possessed the same structure and nearly the same energies as found for the UHV case (see Fig. 6.5b) [46]; this implies the presence of an IFL similar to what has been described for the UHV case. This is further reinforced by the $\sqrt{3}$ moiré pattern observed in STM [62]. The distance of the IFL to the first graphene layer was measured by transmission electron microscopy (TEM) to be 2.0 ± 0.2 Å and the next and subsequent layers were 3.3 ± 0.2 Å [63]; the latter value is the expected value found in graphite and shows that the IFL-first layer distance for this case is slightly smaller than that of UHV grown Si-face samples [53]. These distances were mostly confirmed by Norimatsu, who reported the IFL-first layer distance to be 2.3 Å and the next two distances to be 3.1 and 3.5 Å [64].

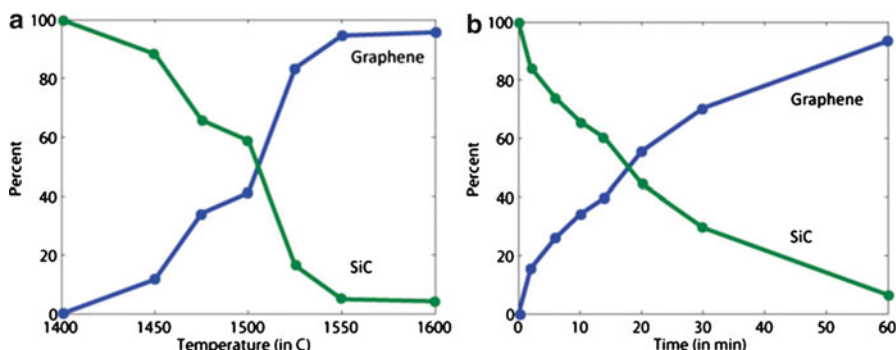


Fig. 6.11 Graphene and exposed (0001)SiC substrate coverages as a function of (a) growth temperature for a growth time of 10 min. and (b) growth time for a growth temperature of 1,475 °C (Reproduced with permission from [61]. © 2009 American Physical Society)

The electrical measurements of graphene grown in moderate vacuum have similarity to those of the UHV case. It is reported that a growth temperature range of 1,500–1,550 °C yields 1 ML with sheet resistance of 10^3 – $10^4 \Omega/\square$ [10]. Films are typically n-type; VanMil noted the highest mobilities were obtained for growth temperatures between 1,500 and 1,600 °C for growth times of 90 min and results were independent of 4H or 6H polytype; for a $16 \times 16 \text{ mm}^2$ sample the best 77 K mobility was $1,560 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for an electron concentration of $4.7 \times 10^{12} \text{ cm}^{-2}$ [32]. Shen and co-workers find n-type carriers with 300 K Hall mobilities of 1,300–1,600 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [65]. The dependence of Hall mobilities vs sheet density can be found in Tedesco [66]. For a gated structure using 30 nm Al_2O_3 as the dielectric, Shen reports the QHE as well as Shubnikov-de Haas oscillations and the anomalous Berry's phase appropriate to graphene. Graphene having 1–2 layers on 50.8 mm diameter 6H-SiC wafers were grown using this intermediate vacuum approach and processed into FETs having a $f_T \cdot L_g$ product of $8.2 \text{ GHz} \cdot \mu\text{m}$ [67]. Yakes and co-workers performed conductance measurements parallel and perpendicular to a small number of steps and report decreased conductance due to steps [68]; this means that placement of FETs to avoid steps may be preferred.

6.3.1.6 Intermediate Vacuum Synthesis of Epitaxial Graphene, C-Face

The intermediate vacuum approach was first described by Hass for C-face where graphene synthesis took place at 1,430 °C at 3×10^{-5} Torr for 5–8 min [9]. In most previous work, pressures used range from 10^{-7} to 10^{-4} Torr [32, 60, 65, 69]. Growth temperatures range from 1,300 °C to 1,650 °C and growth times are typically short, about 10 min although up to 90 min. has also been reported [32]. Incomplete growth is noted from 1,300 °C to 1,400 °C [60] or to 1,450 °C [70], and in these cases, graphene formation is only noted on edges of SiC steps. After graphene growth, the step and terrace morphology of a hydrogen etched substrate surface is distorted as steps get

Fig. 6.12 AFM image of graphene grown on (000 $\bar{1}$) 6H-SiC showing vestiges of steps and terraces and a network of ridges. Scale is in nm (Adapted from [32])

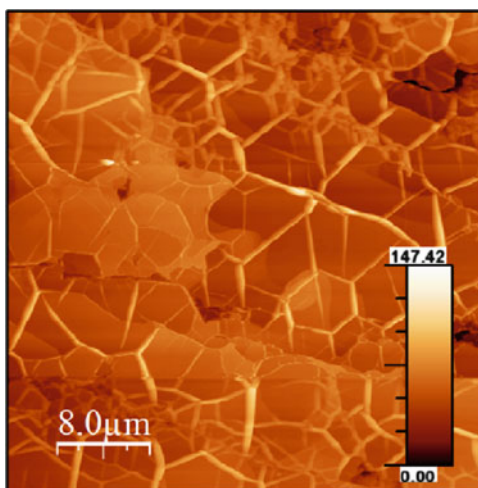
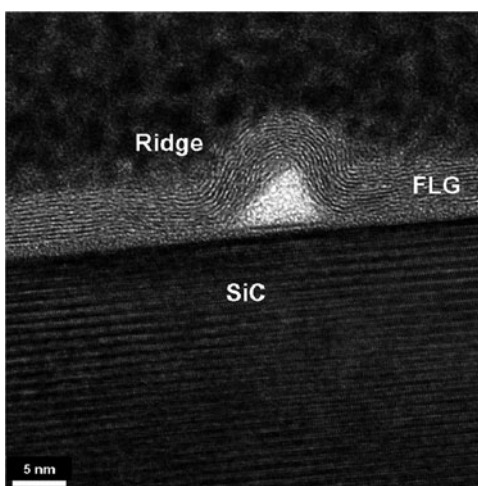


Fig. 6.13 TEM cross-sectional view of a ridge formed after graphene growth at 1,600°C for 10 min. on (000 $\bar{1}$)4H-SiC. Note the delamination of the sheet causes the ridge; this is thought to be due to stress release during cool down after growth (Reproduced with permission from [72]. © 2010 Institute of Physics Publishing)



more rounded with increasing growth temperature [71]; step bunching of 1–15 nm is found and is dominated by ridges that extend from the surface up to as high as 50 nm; Fig. 6.12 shows an example [32]. The graphene lattice parameter of 0.23 ± 0.09 nm was confirmed by STM [70]. Ridge height is reported to increase with temperature: formation begins near 1,475°C, is 6 nm high at 1,500°C and 20 nm high for higher temperatures [71]. The ridges and the graphene were removed by the “scotch tape” method and reveal that the graphene mimics the underlying morphology [32]. TEM images (Fig. 6.13) show the ridges are “buckled” regions of graphene that are

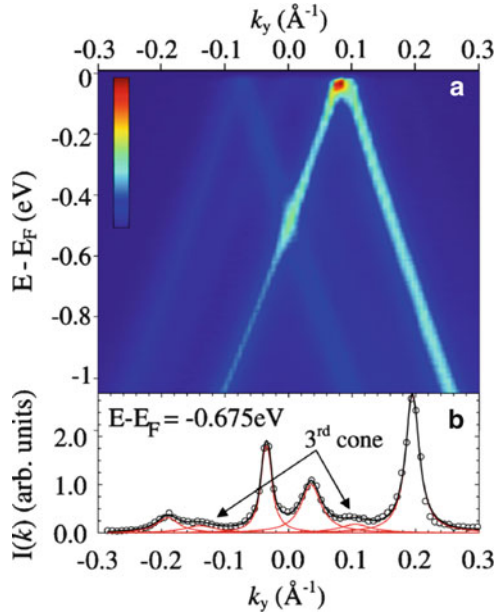
thought to be created during cooling from growth temperature due to the thermal coefficient of expansion differences between the graphene and the SiC substrate [72]. The graphene thickness rapidly increases with temperature: for 10 min growths 1,475°C yields 1.8 nm, 1,500°C yields 2.4 nm and 1,550°C yields 3.3 nm [70, 71]. Higher temperatures and longer times have resulted in films up to 30 nm thick [32]. There is only one report on film uniformity—Kedzierski notes thickness variations of 3–15 nm for a $3.5 \times 4.5 \text{ mm}^2$ sample grown at 1,400°C [56]. Pits have also been observed [70]. No differences in morphology for growth on 4H and 6H substrates have been noted [32, 60].

Since graphene formation on C-face is rapid and results in thick films, there are few reports probing the interface between the substrate and graphene. Biedermann utilized a thin film grown at 1,475°C for XPS analysis and found only sp^2 peaks in the spectra—no interface peak, as observed for growth on Si-face, was found [70]. Azimuthal streaking in LEED patterns was noted for samples 7–13 ML thick implying rotational disorder; some modulation of the intensity could be observed [9]. Additional work showed LEED intensity modulations were preferred at 30° and $\pm 2.2^\circ$ with respect to the SiC $[10\bar{1}0]$ direction [73]. A wide range of rotational disorder has been observed as other investigations have found preferred angles ranging from 6 to 13° with a locus near 7° [74]; $28.4 \pm 0.2^\circ$ [70], 7.42° , and 4.13° [75] have been found in STM investigations. Using *ab initio* calculations, it was shown that adjacent graphene sheets that are rotated by 2.2° resulted in Dirac dispersion at the K point, implying that the planes were electronically decoupled [73]. The linear dispersion in the band structure of the films grown on C-face was experimentally determined by Sprinkle using ARPES [76] and is shown in Fig. 6.14; contributions from three individual sheets can be seen. Although not completely understood in terms of growth and physical mechanism, the rotational disorder promotes decoupling of graphene sheets in multilayer epitaxial graphene.

The structure of multilayer graphene samples were probed in x-ray scattering experiments by Hass and co-workers [77]. Samples ranging from 4 to 12 ML were investigated and the data was fit to a model that uses a SiC reconstructed interface layer with different relaxations at the interface and different thicknesses in the probed area. The first layer was found to be only $1.62 \pm 0.08 \text{ \AA}$ from the bulk SiC implying a strong covalent bond with the substrate. The distance from the first layer to the next is $3.41 \pm 0.04 \text{ \AA}$ and the distance between subsequent layers is $3.368 \pm 0.005 \text{ \AA}$ —these latter distances were relatively insensitive to model details. Since the distances are larger than expected for graphene (3.354 nm, see Table 6.1), the results imply stacking faults are present in the samples; STM results were consistent with the high stacking fault density and suggests that different parts of the surface are in different stages of graphitization [73].

The electrical properties are significantly better than those of graphene on Si-face, with the initial report from Berger and co-workers describing Hall bars having mobility up to $27,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for p-type carriers with density of about 10^{12} cm^{-2} [78] (at 4 K). VanMil reports that the best 300 K results were for a

Fig. 6.14 (a) ARPES measured band structure of an 11-layer graphene film grown on (0001)6H-SiC. The ARPES resolution was set at 7 meV at $h\nu = 30$ eV. The sample temperature is 6 K. The scan in k_y is perpendicular to the SiC $[10 - 10]$ direction at the K point. Two linear Dirac cones are easily visible. (b) A momentum dispersion curve at $BD = E_F - 0.675$ eV shows a third faint cone. Heavy solid line is a fit to the sum of six Lorentzians (thin solid lines) (Reproduced with permission from [76].
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10 min growth at $1,500^\circ\text{C}$ yielding $2,160 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $+1.24 \times 10^{13} \text{ cm}^{-2}$ for a $16 \times 16 \text{ mm}^2$ sample and $18,100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $10 \mu\text{m}$ Hall bar sample having a sheet density of $+2.1 \times 10^{12} \text{ cm}^{-2}$ [32]. Tedesco shows the dependence of mobility with sheet density [66]. In addition, Tedesco notes that extrapolation of mobility to intrinsic carrier concentration would result in 300 K mobilities of about $150,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, comparable to the reported intrinsic mobility of exfoliated graphene at 300 K due only to electron–phonon scattering [79] as well as mobilities reported for suspended exfoliated graphene [80].

Far infrared transmission measurements in a magnetic field gave Sadowski and co-workers an opportunity to measure the graphene Landau levels, finding that the level spacing depended linearly with the square root of the magnetic field, implying Dirac charge carrier behavior [81]; the results also imply that no Bernal components are contributing to the presented data. The V_F was found to be $1.03 \pm 0.01 \times 10^6 \text{ m s}^{-1}$ and at least one of the Landau levels behaved as if it were nearly empty of carriers [39]. This latter result suggests that the interface layer dominates the electronic transport and the upper layers are mostly intrinsic in concentration. Transport measurements by Berger show that n-type carriers with density $3.7 \times 10^{12} \text{ cm}^{-2}$ dominate the transport (at 180 mK) [82]. Since at 300 K, samples act heavily p-type doped, the result implies that the p-type doping probably reflects the influence of the ambient on the topmost layers in the sample whereas the layer(s) nearest the substrate are n-type. The charge screening length in these multilayer epitaxial graphene samples is about 1 ML [83]. Orlita used the

dependence of the Landau level absorption as a function of magnetic field to extract out a lower bound to the mobility, obtaining $250,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ which was ascribed to relatively undoped layers [84]. This same lower bound was confirmed by Jernigan using a sample having large area ($16 \times 16 \text{ mm}^2$) Hall mobility $475 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [46] demonstrating the decoupling of the intrinsic-like layers from those that dominate electronic transport.

Graphene grown in the intermediate vacuum process exhibits the anomalous Berry's phase, and weak Shubnikov deHaas oscillations [43] yet quantum Hall oscillations have not been observed [65]. FETs have also been fabricated from graphene grown in an intermediate vacuum [56].

6.3.1.7 Ar Blanket Gas Synthesis of Epitaxial Graphene, Si-Face

The Ar blanket gas synthesis approach to forming graphene, first described by Emtsev [12], makes use of the phenomena explained by Langmuir that collisions between the desorbed Si atoms and Ar atoms will reflect the Si atoms back to the surface, thus effectively decreasing the growth rate compared to the intermediate vacuum and UHV cases [85]. This enables reconstruction of the surface to be completed before graphene growth and increased carbon surface diffusion distances; hence, the effects of chaotic Si sublimation, such as the poor morphology found for UHV growth (see Fig. 6.5), are diminished. Emtsev used 10–900 mbar Ar pressures and 1,500–2,000°C and found improved morphology over UHV results except for the lowest pressures used; step bunches of 8–15 nm were noted yet terraces up to 50 μm were also observed and nucleation started at step edges. Below 1,500°C no growth was found. Tedesco [86] used 100 mbar of Ar and notes that 1,500°C SiC morphology began showing signs of step bunching with heights 6–9 nm and for growth temperatures at or above 1,550°C similar morphologies as the graphene grown at intermediate vacuum are obtained; results are independent of 4H or 6H polytype. Virojanadara uses 1 atm of Ar at 2,000°C and notes step heights of 1–1.5 nm for 0.03° orientations and 4–5 nm for 0.25° misoriented 6H substrates; STM measurements yield the 0.25 nm graphene lattice constant [87, 88].

The structure of graphene grown under Ar is similar to that of the samples prepared in intermediate vacuum. Emtsev reports the XPS spectra for films that have 1 ML on terraces contains the same interface peak as reported for UHV and intermediate vacuum approaches [12]. In addition, LEED shows the diffraction spots consistent with the $6\sqrt{3}$ reconstruction and the film is epitaxial and rotated 30° with respect to the SiC lattice. Virojanadara confirms the XPS interface peak for films grown at 2,000°C and reports thicknesses of 1–4 ML [87]. Raman spectra demonstrate the films are compressively strained [12]. ARPES measurements reveal the linear band dispersion and $E_F = 0.45 \text{ eV}$ above the Dirac point is noted [12, 87].

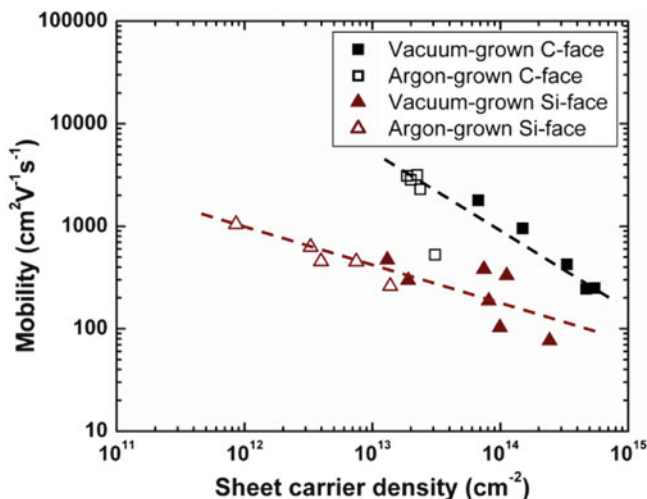


Fig. 6.15 Hall effect mobilities and sheet carrier densities measured at 300 K for $16 \times 16 \text{ mm}^2$ epitaxial graphene films grown on the C-face and Si-face grown under vacuum and under argon. The dashed lines are linear fits to the data for C- and Si-face samples (Reproduced with permission from [86]. © 2009 Electrochemical Society)

Tedesco notes that, in general, the mobility for 100 mbar Ar grown samples was increased and the (electron) sheet charge density decreased as compared to samples grown by the intermediate vacuum approach; mobility vs sheet density is plotted in Fig. 6.15. A sample grown at $1,600^\circ\text{C}$ for 120 min in 100 mbar Ar showed the best 77 K mobility for a $16 \times 16 \text{ mm}^2$ sample, $2,647 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $-1 \times 10^{12} \text{ cm}^{-2}$ [86]. Jobst electrostatically gated a sample grown at $1,650^\circ\text{C}$ in 900 mbar Ar using tetrafluoro-tetracyanoquinodimethane (F4-TCNQ) which acted as a dopant and gate dielectric; the compound shifted E_F by $0.3 \pm 0.05 \text{ eV}$ rendering it closer to the Dirac point with a 300 K sheet density of $-7 \times 10^{11} \text{ cm}^{-2}$. This yielded a 25 K sheet density and mobility of $-5.4 \times 10^{10} \text{ cm}^{-2}$ and $29,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively, thus demonstrating values similar to the best exfoliated samples despite being in contact with the IFL and the F4-TCNQ [89].

For samples made in 1 atm Ar at $2,000^\circ\text{C}$ and having a $\mu(300 \text{ K})$ of $2,400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu(4.2 \text{ K})$ of $4,000\text{--}7,500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, Tzalenchuk and co-workers demonstrated the QHE using 1 ML material that stretched across many terraces; quantization accuracy was 0.4 ± 3 parts in a billion which is 4 orders of magnitude improvement over the previous best results using exfoliated graphene [90]. Samples statically gated by F4-TCNQ showed Shubnikov-de Haas oscillations for a material from a single terrace as well as Berry's phase appropriate to graphene [89]. Pan also reports QHE for a sample with 4 K density and mobility

of $-6.1 \times 10^{11} \text{ cm}^{-2}$ and $14,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [91]. Graphene grown this way was used for Kelvin microprobe studies of IFL, 1 ML and 2 ML layers on the same sample [92]. In addition, state-of-the-art FET performance was obtained for devices grown on a 50.8 mm wafer [93] and recently, a graphene FET with a de-embedded cutoff frequency of 200 GHz for a 210 nm gate has been reported [94]. Also, FET noise performance equal to or exceeding that of exfoliated graphene and frequency multiplication in the GHz range was demonstrated [95].

6.3.1.8 Argon Blanket Gas and Confined Synthesis of Epitaxial Graphene, C-Face

Similar to the Si-face case above, the blanket gas approach was used to better control the graphene formation on the C-face yet the results are mixed. Two different approaches are noted—the first approach uses Ar and the second approach controls the Si overpressure over the substrate by using geometry. For the Ar approach, Tedesco reports improved morphology for growths in 100 mbar when compared to samples grown at intermediate vacuum conditions: there was a reduction in the high density of irregular pits and an improvement in roughness; otherwise the morphology was similar to samples grown under intermediate vacuum [86]. In addition, incomplete growth was found for range of pressures and temperatures as depicted in Fig. 6.16 [96]. Yet, film thicknesses for growth temperatures and times were roughly the same as for graphene formed in intermediate vacuum conditions.

Hite and co-workers showed that threading screw dislocations play a role in the nucleation of the graphene [97]. That work further implies graphene nucleation occurs stochastically across the sample and film uniformity will be difficult to control for the growth conditions employed. TEM investigations for graphene formed at $1,425^\circ\text{C}$ in 100 mbar Ar (30–40 min) reveal the first layer is $3.2 \pm 0.2 \text{ \AA}$ from the bulk SiC and the next layer is $3.6 \pm 0.2 \text{ \AA}$. At $1,600^\circ\text{C}$ the spacing of subsequent carbon layers range from 3.35 to $3.7 \text{ \AA}$ [98]. These results are similar to the intermediate vacuum case and imply rotational faulting and no IFL. In a recent report, for the $1,600^\circ\text{C}$ growth, the first layer distance was noted as $3.0 \pm 0.2 \text{ \AA}$ and high resolution TEM images showed three types of carbon layer stacking: Bernal, Rhombohedral and AAAA(rotationally faulted) [99]. This raises the question as to whether the Bernal and Rhombohedral stacking types are present in graphene grown by the UHV and intermediate vacuum processes.

Tedesco finds a general improvement in electronic transport showing decreased sheet charge density and increased mobility for samples grown in Ar vs intermediate vacuum and that the sheet charge density is dominated by holes. The best mobility reported for $1,600^\circ\text{C}$ growth in 100 mbar of Ar for a $16 \times 16 \text{ mm}^2$ sample was $3,168 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $+1.9 \times 10^{13} \text{ cm}^{-2}$ at 300 K and $7,197 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $+1.1 \times 10^{13} \text{ cm}^{-2}$ at 77 K [86, 96]. Lin and colleagues showed that samples of this

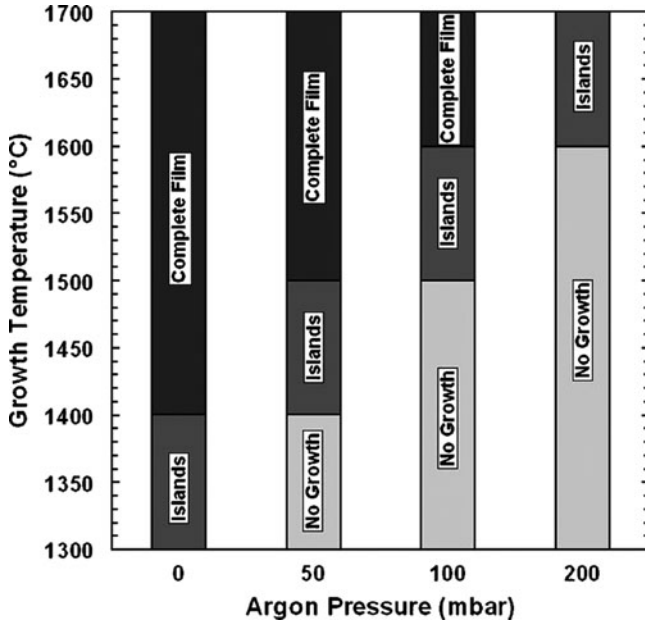


Fig. 6.16 General descriptions of the morphology of the graphene formed on the C-face as a function of growth temperature and Ar growth pressure. Zero Ar pressure corresponds to the intermediate vacuum growth at 10^{-5} mbar

type have at least 3 parallel conductivity channels—an n-type channel probably near the substrate interface, a nearly intrinsic channel, and a p-type channel probably near the sample surface [100]; the number of layers involved in each conductivity channel is not known. As discussed earlier in Sect. 6.3.3.4, the ambient is thought to be the source of the p-type dopant. Orlita used samples formed at 1,600°C in 100 mbar Ar and showed from infrared transmission experiments in a magnetic field that the cyclotron resonance has components that act like rotationally faulted graphene (since the Landau level energies depend linearly on $B^{1/2}$) and bilayer (Bernal) graphene inclusions (since these Landau level energies depend linearly on B); the latter made up no more than 10% of the volume [101]. This is consistent with the high resolution TEM investigation noted above.

The confined approach was reported by Wu and co-workers. Here the SiC C-face sample is placed into an enclosed chamber designed to control the pressure of Si over the substrate surface. An inert gas may have been added. The graphene was continuous over steps and the morphology has ridges. At 300 K, the best mobility reported was $15,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with an n-type sheet density of $1.27 \times 10^{12} \text{ cm}^{-2}$; these values were independent of temperature down to 4.2 K. The QHE was noted along with Berry's phase appropriate for graphene and the V_F was $1.14 \times 10^6 \text{ m s}^{-1}$ [38].

6.4 Outlook

In less than a decade, there has been considerable progress in developing epitaxial graphene from little more than a concept to a potential device technology. But, considerably more work needs to be done. Potential obstacles to device development are forming a band gap and controlling doping and uniformity of layers—issues that have been barely addressed to-date. Investigations into growth mechanisms may yield clues to controlling uniformity and doping. First principles understanding of the graphene—SiC interface still require development to match experimental results. The impact of substrate orientation is an open question – especially if it affects the graphene growth rate. Initial investigations on forming graphene on other SiC polytypes (not covered here) have only just begun and offer potentially new avenues to exploit. The basic physics of electronic transport and the impact of an interface layer require significant effort which will go hand-in-hand with the development of dielectric deposition approaches (see Chap. 9).

Yet, there is room for considerable optimism. Nature has been very generous—graphene is relatively easy to form on SiC. And large area substrates (essential for future device technologies) are becoming readily available. Recent investigations indicate that controlling the doping either chemically and/or electrostatically should result in excellent electronic transport properties. Also, transistor development for high frequency applications has shown considerable promise. Thus, continued progress in the epitaxial graphene field is expected in the foreseeable future.

Acknowledgements The authors thank Glenn Jernigan and Charles Eddy for a critical reading of the manuscript. We thank Rachael Myers-Ward, Ginger Wheeler, Jennifer Hite and Nelson Garces for useful discussions. LON is grateful for postdoctoral support from the ASEE. This work was supported by the Office of Naval Research.

References

1. Production of artificial crystalline carbonaceous E. Acheson and United States Patent No. 492.767 (28.02.1893).
2. Edward Acheson – Carborundum The Lemelson – MIT Program, electronic source (<http://web.mit.edu/invent/and/iow/acheson.html>).
3. A. J. Vanbommel, J. E. Crombeen, and A. Vantooren, “LEED and Auger-electron observations of SiC (0001) surface,” *Surface Science* **48** (2), 463–472 (1975).
4. I. Forbeaux, J. M. Themlin, and J. M. Debever, “Heteroepitaxial graphite on 6H-SiC(0001): Interface formation through conduction-band electronic structure,” *Physical Review B* **58** (24), 16396–16406 (1998).
5. A. Charrier, A. Coati, T. Argunova et al., “Solid-state decomposition of silicon carbide for growing ultra-thin heteroepitaxial graphite films,” *Journal of Applied Physics* **92** (5), 2479–2484 (2002).
6. K. S. Novoselov, A. K. Geim, S. V. Morozov et al., “Electric field effect in atomically thin carbon films,” *Science* **306** (5696), 666–669 (2004).

7. C. Berger, Z. M. Song, T. B. Li et al., "Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics," *Journal of Physical Chemistry B* **108** (52), 19912–19916 (2004).
8. Y. B. Zhang, Y. W. Tan, H. L. Stormer et al., "Experimental observation of the quantum Hall effect and Berry's phase in graphene," *Nature* **438** (7065), 201–204 (2005).
9. J. Hass, R. Feng, T. Li et al., "Highly ordered graphene for two dimensional electronics," *Applied Physics Letters* **89** (14), 143106 (2006).
10. Y. Q. Wu, P. D. Ye, M. A. Capano et al., "Top-gated graphene field-effect-transistors formed by decomposition of SiC," *Applied Physics Letters* **92** (9), 092102 (2008).
11. private communication G. Jernigan and P. Campbell, Nov 30, 2007.
12. K. V. Emtsev, A. Bostwick, K. Horn et al., "Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide," *Nature Materials* **8** (3), 203–207 (2009).
13. private communication D. K. Gaskill and J. L. Tedesco, Sept, 2008.
14. D. K. Gaskill, G. G. Jernigan, P. M. Campbell et al., in *Graphene and Emerging Materials for Post-Cmos Applications*, edited by Y. Obeng, S. DeGendt, P. Srinivasan et al. (2009), Vol. 19, pp. 117–124.
15. private communication D. K. Gaskill and J. L. Tedesco, Dec 4, 2008.
16. private communication D. K. Gaskill and J. L. Tedesco, Dec 17, 2009.
17. Cree press release, Aug. 30, 2010, www.cree.com.
18. J. Hass, W. A. de Heer, and E. H. Conrad, "The growth and morphology of epitaxial multilayer graphene," *Journal of Physics-Condensed Matter* **20** (32), 323202 (2008).
19. T. Seyller, A. Bostwick, K. V. Emtsev et al., "Epitaxial graphene: a new material," *Physica Status Solidi B-Basic Solid State Physics* **245** (7), 1436–1446 (2008).
20. W. A. de Heer, C. Berger, X. S. Wu et al., "Epitaxial graphene electronic structure and transport," *Journal of Physics D-Applied Physics* **43** (37), 374007 (2010).
21. R. F. Davis, "Proceedings of the international conference in SiC and related materials – 93," *Institute of Physics Conference Series* 137, 1 (1994).
22. A. Taylor, Jones, R. M. in *Silicon Carbide - A High Temperature Semiconductor*, Eds. O'Connor, J. R., Smiltens, J., Pergamon Press, Oxford, London, New York, Paris 1960, 14.
23. A. Bauer, J. Krausslich, L. Dressler et al., "High-precision determination of atomic positions in crystals: The case of 6H- and 4H-SiC," *Physical Review B* **57** (5), 2647–2650 (1998).
24. F. R. Chien, S. R. Nutt, and W. S. Yoo, "Lattice mismatch measurement of epitaxial beta-SiC on alpha-SiC substrates," *Journal of Applied Physics* **77** (7), 3138–3145 (1995).
25. Y. Baskin and L. Meyer, "Lattice constants of graphite at low temperatures," *Physical Review* **100** (2), 544–544 (1955).
26. ed. Gary L. Harris "Properties of Silicon Carbide", INSPEC, the Institution of Electrical Engineers, London 1995.
27. A. Powell "Growth of SiC Substrates", J. Jenny, S. Muller, H. Mcd. Hobgood, V. Tsvetkov, R. Lenoard, and C. Carter, Jr., in "SiC Materials and Devices, vol. 2", ed. Michael Shur, Sergey Rumyantsev, and Michael Levinshstein, World Scientific, Singapore (2007).
28. P. G. Neudeck, W. Huang, and M. Dudley, "Breakdown degradation associated with elementary screw dislocations in 4H-SiC p(+)/n junction rectifiers," *Solid-State Electronics* **42** (12), 2157–2164 (1998).
29. C. R. Eddy and D. K. Gaskill, "Silicon Carbide as a Platform for Power Electronics," *Science* **324** (5933), 1398–1400 (2009).
30. K. K. Lew, B. L. VanMil, R. L. Myers-Ward et al., in *Silicon Carbide and Related Materials 2006*, edited by N. Wright, C. M. Johnson, K. Vassilevski et al. Materials Science Forum (2007), Vol. 556–557, pp. 513–516.
31. B. L. VanMil, K. K. Lew, R. L. Myers-Ward et al., "Etch rates near hot-wall CVD growth temperature for Si-face 4H-SiC using H-2 and C3H8," *Journal of Crystal Growth* **311** (2), 238–243 (2009).

32. B. L. VanMil, R. L. Myers-Ward, J. L. Tedesco et al., in *Silicon Carbide and Related Materials 2008*, edited by A. PerezTomas, P. Godignon, M. Vellvehi et al. Materials Science Forum (2009), Vol. 615–617, pp. 211–214.
33. A. Mattausch and O. Pankratov, “Ab initio study of graphene on SiC,” *Physical Review Letters* **99** (7), 076802 (2007).
34. F. Varchon, R. Feng, J. Hass et al., “Electronic structure of epitaxial graphene layers on SiC: Effect of the substrate,” *Physical Review Letters* **99** (12), 126805 (2007).
35. L. Magaud, F. Hiebel, F. Varchon et al., “Graphene on the C-terminated SiC (0001) surface: An ab initio study,” *Physical Review B* **79** (16) (2009).
36. Shu Xu Thushari Jayasekera, K.W. Kim, and M.Buongiorno Nardelli, “Electronic properties of the Graphene/6H-SiC(000–1) interface: a first principles study,” *Physical Review B* **84**, 035442 (2011).
37. A. J. Van Bommel, J. E. Crombeen, and A. Van Tooren, “LEED and Auger-Electron Observations of SiC (0001) Surface,” *Surface Science* **48**, 463–472 (1975).
38. X. S. Wu, Y. K. Hu, M. Ruan et al., “Half integer quantum Hall effect in high mobility single layer epitaxial graphene,” *Applied Physics Letters* **95** (22), 223108 (2009).
39. M. L. Sadowski, G. Martinez, M. Potemski et al., “Landau level spectroscopy of ultrathin graphite layers,” *Physical Review Letters* **97** (26), 266405 (2006).
40. private communication G. G. Jernigan, 2009.
41. S. K. Lilov, “Thermodynamic analysis of the gas-phase at the dissociative evaporation of silicon-carbide,” *Crystal Research and Technology* **28** (4), 503–510 (1993).
42. T. Seyller, K. V. Emtsev, K. Gao et al., “Structural and electronic properties of graphite layers grown on SiC(0001),” *Surface Science* **600** (18), 3906–3911 (2006).
43. W. A. de Heer, C. Berger, X. S. Wu et al., “Epitaxial graphene,” *Solid State Communications* **143** (1–2), 92–100 (2007).
44. C. Riedl, U. Starke, J. Bernhardt et al., “Structural properties of the graphene-SiC(0001) interface as a key for the preparation of homogeneous large-terrace graphene surfaces,” *Physical Review B* **76** (24), 245406 (2007).
45. G. Gu, S. Nie, R. M. Feenstra et al., “Field effect in epitaxial graphene on a silicon carbide substrate,” *Applied Physics Letters* **90** (25), 253507 (2007).
46. G. G. Jernigan, B. L. VanMil, J. L. Tedesco et al., “Comparison of Epitaxial Graphene on Si-face and C-face 4H SiC Formed by Ultrahigh Vacuum and RF Furnace Production,” *Nano Letters* **9** (7), 2605–2609 (2009).
47. V. W. Brar, Y. Zhang, Y. Yayon et al., “Scanning tunneling spectroscopy of inhomogeneous electronic structure in monolayer and bilayer graphene on SiC,” *Applied Physics Letters* **91** (12), 122102 (2007).
48. P. Mallet, F. Varchon, C. Naud et al., “Electron states of mono- and bilayer graphene on SiC probed by scanning-tunneling microscopy,” *Physical Review B* **76** (4), 041403 (2007).
49. K. V. Emtsev, F. Speck, T. Seyller et al., “Interaction, growth, and ordering of epitaxial graphene on SiC{0001} surfaces: A comparative photoelectron spectroscopy study,” *Physical Review B* **77** (15), 155303 (2008).
50. D. Graf, F. Molitor, K. Ensslin et al., “Raman imaging of graphene,” *Solid State Communications* **143** (1–2), 44–46 (2007).
51. T. Ohta, A. Bostwick, J. L. McChesney et al., “Interlayer interaction and electronic screening in multilayer graphene investigated with angle-resolved photoemission spectroscopy,” *Physical Review Letters* **98** (20), 206802 (2007).
52. A. Bostwick, T. Ohta, J. L. McChesney et al., “Symmetry breaking in few layer graphene films,” *New Journal of Physics* **9**, 385 (2007).
53. J. Hass, J. E. Millan-Otoya, P. N. First et al., “Interface structure of epitaxial graphene grown on 4H-SiC(0001),” *Physical Review B* **78** (20), 205424 (2008).
54. G. M. Rutter, N. P. Guisinger, J. N. Crain et al., “Imaging the interface of epitaxial graphene with silicon carbide via scanning tunneling microscopy,” *Physical Review B* **76** (23), 235416 (2007).

55. E. Rollings, G. H. Gweon, S. Y. Zhou et al., "Synthesis and characterization of atomically thin graphite films on a silicon carbide substrate," *Journal of Physics and Chemistry of Solids* **67** (9–10), 2172–2177 (2006).
56. J. Kedzierski, P. L. Hsu, P. Healey et al., "Epitaxial graphene transistors on SiC substrates," *IEEE Transactions on Electron Devices* **55** (8), 2078–2085 (2008).
57. M. Kusunoki, T. Suzuki, T. Hirayama et al., "A formation mechanism of carbon nanotube films on SiC(0001)," *Applied Physics Letters* **77** (4), 531–533 (2000).
58. A. J. Strudwick G. L. Creeth, J. T. Sadowski, and C. H. Marrows, "Surface morphology and transport studies of epitaxial graphene on SiC(000 $\bar{1}$)," *Physical Review B* **43**, 195440 (2010).
59. U. Starke, in *Recent Major Advances in SiC*, edited by H. Matsunami W. Choyke, and G. Pensl (Springer Scientific, 2003), p. 281.
60. W. Strupinski, R. Bozek, J. Borysiuk et al., in *Silicon Carbide and Related Materials 2008*, edited by A. PerezTomas, P. Godignon, M. Vellvehi et al. (2009), Vol. 615–617, pp. 199–202.
61. M. L. Bolen, S. E. Harrison, L. B. Biedermann et al., "Graphene formation mechanisms on 4H-SiC(0001)," *Physical Review B* **80** (11), 115433 (2009).
62. J. Borysiuk, R. Bozek, W. Strupinski et al., "Transmission electron microscopy and scanning tunneling microscopy investigations of graphene on 4H-SiC(0001)," *Journal of Applied Physics* **105** (2), 023503 (2009).
63. J. Borysiuk, W. Strupinski, R. Bozek et al., in *Silicon Carbide and Related Materials 2008*, edited by A. PerezTomas, P. Godignon, M. Vellvehi et al. (2009), Vol. 615–617, pp. 207–210.
64. W. Norimatsu and M. Kusunoki, "Transitional structures of the interface between graphene and 6H-SiC (0001)," *Chemical Physics Letters* **468** (1–3), 52–56 (2009).
65. T. Shen, J. J. Gu, M. Xu et al., "Observation of quantum-Hall effect in gated epitaxial graphene grown on SiC (0001)," *Applied Physics Letters* **95** (17), 172105 (2009).
66. J. L. Tedesco, B. L. VanMil, R. L. Myers-Ward et al., "Hall effect mobility of epitaxial graphene grown on silicon carbide," *Applied Physics Letters* **95** (12), 122102 (2009).
67. J. S. Moon, D. Curtis, M. Hu et al., "Epitaxial-Graphene RF Field-Effect Transistors on Si-Face 6H-SiC Substrates," *IEEE Electron Device Letters* **30** (6), 650–652 (2009).
68. M. K. Yakes, D. Gunlycke, J. L. Tedesco et al., "Conductance Anisotropy in Epitaxial Graphene Sheets Generated by Substrate Interactions," *Nano Letters* **10** (5), 1559–1562 (2010).
69. S. Shivaraman, M. V. S. Chandrashekhar, J. J. Boeckl et al., "Thickness Estimation of Epitaxial Graphene on SiC Using Attenuation of Substrate Raman Intensity," *Journal of Electronic Materials* **38** (6), 725–730 (2009).
70. L. B. Biedermann, M. L. Bolen, M. A. Capano et al., "Insights into few-layer epitaxial graphene growth on 4H-SiC(0001)over-bar substrates from STM studies," *Physical Review B* **79** (12), 125411 (2009).
71. G. Prakash, M. A. Capano, M. L. Bolen et al., "AFM study of ridges in few-layer epitaxial graphene grown on the carbon-face of 4 H-SiC(000 $\bar{1}$)," *Carbon* **48** (9), 2383–2393 (2010).
72. G. Prakash, M. L. Bolen, R. Colby et al., "Nanomanipulation of ridges in few-layer epitaxial graphene grown on the carbon face of 4H-SiC," *New Journal of Physics* **12**, 125009 (2010).
73. J. Hass, F. Varchon, J. E. Millan-Otoya et al., "Why multilayer graphene on 4H-SiC (000 $\bar{1}$) behaves like a single sheet of graphene," *Physical Review Letters* **100** (12), 125504 (2010).
74. Luxmi, N. Srivastava, G. He et al., "Comparison of graphene formation on C-face and Si-face SiC {0001} surfaces," *Physical Review B* **82** (23), 235406 (2010).
75. D. L. Miller, K. D. Kubista, G. M. Rutter et al., "Observing the Quantization of Zero Mass Carriers in Graphene," *Science* **324** (5929), 924–927 (2009).
76. M. Sprinkle, D. Siegel, Y. Hu et al., "First Direct Observation of a Nearly Ideal Graphene Band Structure," *Physical Review Letters* **103** (22), 226803 (2009).

77. J. Hass, R. Feng, J. E. Millan-Otoya et al., "Structural properties of the multilayer graphene/4H-SiC(000 $\bar{1}$) system as determined by surface x-ray diffraction," *Physical Review B* **75** (21), 214109 (2010).
78. C. Berger, Z. M. Song, X. B. Li et al., "Electronic confinement and coherence in patterned epitaxial graphene," *Science* **312** (5777), 1191–1196 (2006).
79. J. H. Chen, C. Jang, S. D. Xiao et al., "Intrinsic and extrinsic performance limits of graphene devices on SiO₂," *Nature Nanotechnology* **3** (4), 206–209 (2008).
80. K. I. Bolotin, K. J. Sikes, Z. Jiang et al., "Ultrahigh electron mobility in suspended graphene," *Solid State Communications* **146** (9–10), 351–355 (2008).
81. M. L. Sadowski, G. Martinez, M. Potemski et al., "Magnetospectroscopy of epitaxial few-layer graphene," *Solid State Communications* **143** (1–2), 123–125 (2007).
82. C. Berger, Z. M. Song, X. B. Li et al., "Magnetotransport in high mobility epitaxial graphene," *Physica Status Solidi a-Applications and Materials Science* **204** (6), 1746–1750 (2007).
83. D. Sun, C. Divin, C. Berger et al., "Spectroscopic Measurement of Interlayer Screening in Multilayer Epitaxial Graphene," *Physical Review Letters* **104** (13), 136802 (2010).
84. M. Orlita, C. Faugeras, P. Plochocka et al., "Approaching the Dirac Point in High-Mobility Multilayer Epitaxial Graphene," *Physical Review Letters* **101** (26), 267101 (2008).
85. I. Langmuir, "Convection and conduction of heat in gases," *Physical Review* **34** (6) (1912); G. R. Fonda, "Evaporation of tungsten under various pressures of argon," *Physical Review* **31** (2), 260–266 (1928).
86. J. L. Tedesco, B. L. VanMil, R. L. Myers-Ward et al., in *Graphene and Emerging Materials for Post-Cmos Applications*, edited by Y. Obeng, S. DeGendt, P. Srinivasan et al. (2009), Vol. 19, pp. 137–150.
87. C. Virojanadara, M. Syvajarvi, R. Yakimova et al., "Homogeneous large-area graphene layer growth on 6H-SiC(0001)," *Physical Review B* **78** (24), 245403 (2008).
88. C. Virojanadara, R. Yakimova, J. R. Osiecki et al., "Substrate orientation: A way towards higher quality monolayer graphene growth on 6H-SiC(0001)," *Surface Science* **603** (15), L87–L90 (2009).
89. J. Jobst, D. Waldmann, F. Speck et al., "Quantum oscillations and quantum Hall effect in epitaxial graphene," *Physical Review B* **81** (19), 195434 (2010).
90. A. Tzalenchuk, S. Lara-Avila, A. Kalaboukhov et al., "Towards a quantum resistance standard based on epitaxial graphene," *Nature Nanotechnology* **5** (3), 186–189 (2010).
91. W. Pan, S. W. Howell, A. J. Ross et al., "Observation of the integer quantum Hall effect in high quality, uniform wafer-scale epitaxial graphene films," *Applied Physics Letters* **97** (25), 252101 (2010).
92. T. Filletter, K. V. Emtsev, T. Seyller et al., "Local work function measurements of epitaxial graphene," *Applied Physics Letters* **13**, 133117 (2008).
93. J. S. Moon, D. Curtis, S. Bui et al., "Top-Gated Epitaxial Graphene FETs on Si-Face SiC Wafers With a Peak Transconductance of 600 mS/mm," *IEEE Electron Device Letters* **31** (4), 260–262 (2010).
94. Damon B. Farmer Yu-Ming Lin, Keith A. Jenkins, Joseph L. Tedesco, Rachael L. Myers-Ward, Charles R. Eddy, Jr., D. Kurt Gaskill, Yanqing Wu, Phaendon Avouris, and Christos Dimitrakopoulos, "Enhanced Performance in Epitaxial Graphene FETs with Optimized Channel Morphology," *Applied Physics Letters* **submitted** (2011).
95. J. S. Moon, D. Curtis, D. Zehnder et al., "Low-Phase-Noise Graphene FETs in Ambipolar RF Applications," *IEEE Electron Device Letters* **32** (3), 270–272 (2011).
96. J. L. Tedesco, G. G. Jernigan, J. C. Culbertson et al., "Morphology characterization of argon-mediated epitaxial graphene on C-face SiC," *Applied Physics Letters* **96** (22), 222103 (2010).
97. J. K. Hite, M. E. Twigg, J. L. Tedesco et al., "Epitaxial Graphene Nucleation on C-Face Silicon Carbide," *Nano Letters* **11** (3), 1190–1194 (2011).

98. J. Borysiuk, R. Bozek, K. Grodecki et al., "Transmission electron microscopy investigations of epitaxial graphene on C-terminated 4H-SiC," *Journal of Applied Physics* **108** (1), 013518 (2010).
99. J. Borysiuk, J. Soltys, and J. Piechota, "Stacking sequence dependence of graphene layers on SiC (0001)-Experimental and theoretical investigation," *Journal of Applied Physics* **109** (9), 093523 (2011).
100. Y. M. Lin, C. Dimitrakopoulos, D. B. Farmer et al., "Multicarrier transport in epitaxial multilayer graphene," *Applied Physics Letters* **97** (11), 112107 (2010).
101. M. Orlita, C. Faugeras, J. Borysiuk et al., "Magneto-optics of bilayer inclusions in multilayered epitaxial graphene on the carbon face of SiC," *Physical Review B* **83** (12), 125302 (2011).

Chapter 7

Graphene Growth by CVD Methods

Alfonso Reina and Jing Kong

In this chapter, the production of graphene by chemical vapor deposition (CVD) is discussed. CVD is widely used in the microelectronics industry in processes involving the deposition of thin films of various materials. The deposition is made from precursors in the gas phase which adsorb on the target surface producing a condensed phase of a specific material. The attractiveness of the generation of graphene by CVD is based on the fact that this technique allows for scalability as well as low cost.

7.1 Introduction

CVD of carbon materials is based on the pyrolysis of hydrocarbons over various surfaces [1–3]. Graphite is grown using the pyrolysis of hydrocarbons such as methane, ethylene and acetylene. Transition metals are extensively used in this process because of their ability to catalyze the dehydrogenation of these hydrocarbons and produce high quality graphite crystals over their surface [1]. Carbon nanotubes are also grown mostly from transition metal nanoparticles. The growth of a single layer graphene (SLG) over transition metals by CVD methods has been known since the 1950s [1]. Since much of this work has involved transition metals, this chapter will focus on the growth of graphene over these types of substrates.

Graphene growth on a transition metal substrate can be broadly classified into two mechanisms.

- *Graphene growth by surface segregation of carbon:* Here, graphene grows from carbon atoms diffusing to free surfaces of transition metals. Such

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carbon atoms are introduced to the bulk of these metals by various methods including CVD (Sect. 7.2).

- *Graphene growth by surface decomposition of hydrocarbons:* In this mechanism, graphene grows from carbon atoms that are produced by the decomposition of a hydrocarbon directly on the surface of the metal (Sect. 7.3).

It must be emphasized that monolayers of graphitic carbon by these methods were synthesized as early as the second half of the last century. The recent interest in using graphene for various applications triggered more research on CVD approaches for graphene production. Recent research has led to simplification of the processes by using readily available substrates such as thin films of metals deposited by e-beam evaporation or sputtering and polycrystalline metallic foils; also, graphene growth by CVD can be carried out in ambient pressures, thereby simplifying the process further. It is also now possible to isolate graphene (grown by CVD) from metals and transfer it to other substrates (discussed in Sect. 7.4).

Experiments to date have provided some information on growth mechanisms and have pointed to key parameters that affect graphene quality. These parameters include substrate properties such as the type of metal, carbon solubility, and structural quality. CVD process parameters such as temperature, hydrocarbon concentration, pressure, and cooling rate can also play a role. These parameters will be discussed in Sect. 7.5. Growth of graphene directly on a non-catalytic substrate will be discussed in Sect. 7.6. Generation of graphene-based materials from substrate-free CVD approaches will be explored in Sect. 7.7.

7.2 Graphene by Segregation of Carbon

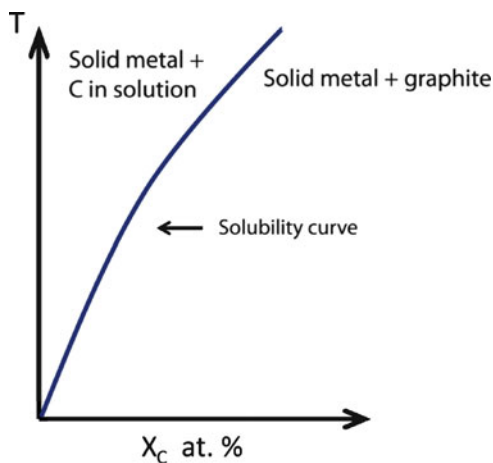
Segregation of carbon impurities to interfaces or free surfaces of a metal in the solid phase was observed in the 1960s. This segregation is driven by supersaturation of carbon impurities in the material. Assuming an ideal solution, the carbon solubility in a transition metal can be expressed as:

$$\ln X_C = \frac{\Delta G}{kT} \quad (7.1)$$

where X_C is the carbon concentration, T is the system temperature, k is the Boltzmann constant and ΔG is the difference in chemical potential between a pure solvent and the solvent with diluted carbon impurities. This relation defines the maximum carbon content at a given temperature beyond which a second phase is developed under thermodynamic equilibrium (Fig. 7.1). In the case of carbon diluted in a transition metal, supersaturation leads to carbon segregation and the nucleation of a graphitic phase.

A popular way to obtain single crystals of graphite in the first half of the twentieth century was purification of flakes of natural graphite [4]. It was later discovered that graphite was also produced in steel-making (kish graphite) during

Fig. 7.1 Typical solubility curve for carbon in a transition metal. The solubility of carbon X_C follows the expression in (7.1)



the cooling of steel. This was explained by the steel's high solubility of carbon impurities which precipitated as highly crystalline graphite upon cooling. Further developments in the production of graphite crystals came along during the 1960s [4–6]. Such processes relied on the formation of a melt of transition metals (solvent) containing carbon impurities (solute). The carbon solute was introduced from the graphite crucible on which the melt was formed at high temperatures. Supersaturation by cooling [4] or the creation of a temperature gradient across the body of the melt [6] induced the segregation of carbon to the surface of the melt and finally the formation of graphite.

The segregation of carbon is currently employed as a means to fabricate graphene on various substrates. The temperature dependent solubility of carbon in Ruthenium was used by Sutter [7] to grow SLG and bi-layer graphene (BLG). Growth occurred epitaxially on a Ru(0001) surface under UHV conditions. In this process, carbon is evaporated over Ru(0001). At 1,150°C, carbon is absorbed by the Ru bulk. After this, the samples are cooled slowly to 850°C to promote the formation of single-layer (SLG) and bilayer (BLG) graphene. The growth of SLG and BLG islands, as large as 200 μm , was observed by in-situ electron microscopy and low energy electron diffraction (LEED) after carbon segregation. Remarkably, such islands grow continuously across the steps of the Ru surface suggesting that every island is a single crystal. The growing graphene glides across the surface by stepping down on each of the surface steps. The growth of the islands can only proceed in this direction (Fig. 7.2). Sutter et al. also concluded that the first graphene layer growing on such a substrate is strongly bound to the Ru surface and therefore loses its electrical conductivity. Electrical conduction is only observed for the second layer growing on the Ru surface.

Polycrystalline metallic thin films can also be used to fabricate graphene films in ambient pressure CVD (APCVD) via a carbon segregation mechanism [8–13]. The use of metallic thin films (200–500 nm) is advantageous since they are readily

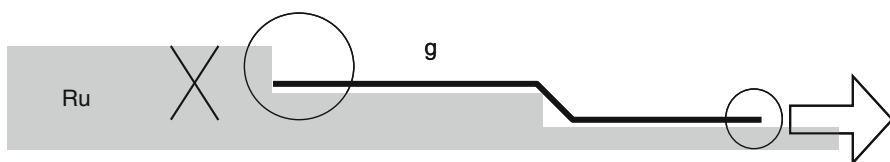


Fig. 7.2 Graphene grown on crystalline Ru. Mechanism of graphene growth. Graphene extends across the crystal's steps in a downhill manner (Adapted from [7])



Fig. 7.3 Cross-sectional view of deposited metallic films on SiO_2 -Si substrates

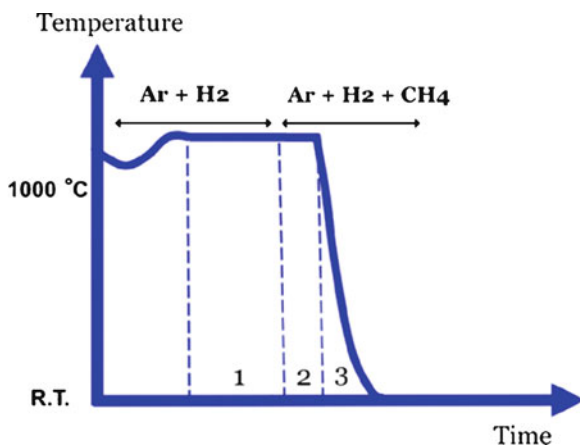


Fig. 7.4 Temperature–time diagram for the ambient pressure CVD (APCVD) process used to grow few-layer graphene (FLG) films. (1) annealing of Ni thin films, (2) exposure to methane. Carbon is produced on the surface of the metal and/or diffuses to the bulk to form a metal-C solid solution. (3) sample cooling

obtained and they are of lower cost than single-crystalline substrates. The use of thin films also facilitates the transfer of the graphene to non-specific substrates.

The thin films are deposited by e-beam evaporation or by sputtering on oxidized silicon substrates with 100 nm of silicon dioxide (Fig. 7.3). Typically, CVD processes for graphene growth by carbon segregation involve three stages (Fig. 7.4):

1. *Annealing of the metal film:* Here, the catalyst film is annealed at temperatures between 900°C and $1,000^\circ\text{C}$ in order to induce its recrystallization. Increased grain size can help in avoiding excess nucleation sites for amorphous carbon or multilayer graphene. Furthermore, by annealing the thin film, it is possible to

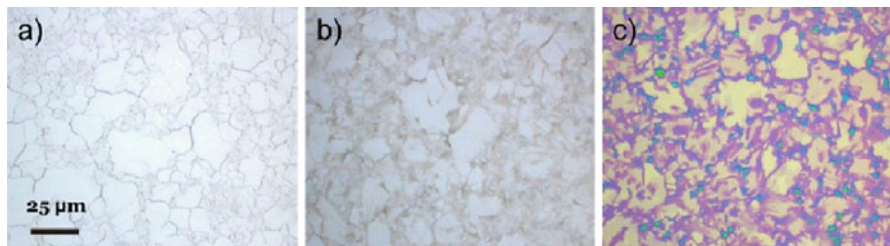


Fig. 7.5 FLG on Ni. (a) Optical image of a clean Ni film which was annealed. (b) Optical image of a Ni film after graphene growth. (c) FLG film transferred to a SiO₂-Si substrate

induce a preferential texture of the film in the case of some metals (e.g. towards the (111) orientation for fcc metals). This is desired, for example, in the case of Ni(111) due to its lattice matching with graphene. The annealing treatment is typically done under gas mixtures of Ar and H₂.

2. *Exposure to CH₄*: After the annealing treatment, the surface is exposed to diluted methane gas. The hydrocarbon gas can also be introduced with a mixture of Ar and H₂. The temperature during this part of the process can be the same or different from the annealing temperature. It is expected that methane is decomposed catalytically on the surface of the metal to produce carbon atoms on its surface. The decomposition of methane by transition metals has been studied extensively [14]. The following reaction is used to describe the decomposition:



However, it is also thought that such a decomposition may involve intermediate steps involving other hydrocarbons such as ethylene (C₂H₄) and acetylene (C₂H₂) [2].

Since this process occurs at temperatures around 900–1,000°C, it is expected that diffusion of carbon to the bulk of the film occurs for metals with high carbon solubility at that temperature, e.g. Ni (1% at.).

3. *Cooling of the metallic film*: Segregation of carbon stored inside the film is promoted by cooling the sample. The carbon segregated to the surface initiates the growth of SLG and few-layer graphene (FLG). The cooling rates typically used are between 4 and 100°C min⁻¹ [9, 15].

Figure 7.5 compares a clean Ni film which was annealed, a Ni film after the three process steps described above and the graphene film transferred onto a SiO₂/Si substrate. The dark features in Fig. 7.5b suggest the precipitation of FLG and graphite. Their nucleation distribution depends on the grain size of the initial Ni film [16]. The clear regions contain SLG or BLG and these tend to be away from the grain boundaries of the Ni film. They can only be detected optically once the graphene film has been isolated from the Ni and transferred to a SiO₂-Si substrate. Later in this chapter, a discussion on this effect is included and it will be shown that by manipulating the Ni grain size, it is possible to change the morphology and optical properties of the grown graphene films.

In this section, growth of graphene is done via the segregation of carbon atoms from the bulk of a metal substrate to its surface. The introduction of carbon atoms to the bulk of the metal is done by the decomposition of hydrocarbons on the surface of the metal using CVD processes. In the next section, the discussion focuses on a different mechanism in which graphene grows directly on the surface of the metals without the need to segregate carbon impurities from the bulk of a metal.

7.3 Graphene by Surface Decomposition of Hydro-Carbons

In the early 1960s, the exploration of carbon segregation from melts was paralleled by the use of pyrolysis of carbon containing gases [3, 17, 18]. Initially, pyrolysis was done over non-metallic substrates such as porcelain. Banerjee et al. [17] realized that the rate of carbon formation and the structure of the graphite film formed were different depending on the substrates used. Later, the use of nickel and other transition metals was pursued because of their dehydrogenation ability rather than their high carbon solubility like in the case of carbon segregation. Indeed, during early experiments it was not clear whether the graphite grown on nickel was formed directly from the carbon produced during the hydrocarbon decomposition or if it involved the dissolution of carbon into the bulk followed by precipitation of graphite [2]. Presland et al. initially theorized that the former was the more likely, on the basis that the cooling of their foils would only take place in a few seconds, making the formation of highly crystalline graphite during cooling unlikely. Later in the 1970s it was realized that the pyrolysis processes could also involve the dissolution–precipitation mechanism [19, 20]. This took place while carbon segregation studies on nickel were better understood by Derbyshire et al. [19, 20].

Direct deposition of graphite with CVD without dissolution-precipitation can be accomplished either by: (1) use of lower CVD operating temperatures or (2) use of metallic substrates that have negligible carbon solubility at the operating temperature. Lowering the process temperature inhibits carbon diffusion to the bulk of the metal and it also lowers carbon solubility of the metal used. Most of the reports on graphite growth by CVD are unclear about whether the growth occurs by direct deposition or by dissolution–precipitation mechanisms [21–23]. Differentiation between both mechanisms emerged as more work was done aimed towards lowering the CVD temperatures [24] and growing thinner graphite films [22].

The growth of SLG on Ni(111) by CVD was possible using relatively lower temperatures (500–600°C), UHV conditions, and hydrocarbons such as ethylene and propylene [25–27]. Coverage of the Ni(111) surface with one monolayer was accomplished by exposure to a few langmuirs (1 La = 10^6 Torr-s) of the hydrocarbon used [25–27]. The growth of SLG was reported to be self limiting. This observation was explained by the fact that catalytic activity of the Ni(111) surface was negligible once covered with one monolayer of graphite. At the hydrocarbon partial pressure in operation, the reduced catalytic activity would not generate enough carbon species to sustain further graphite growth.

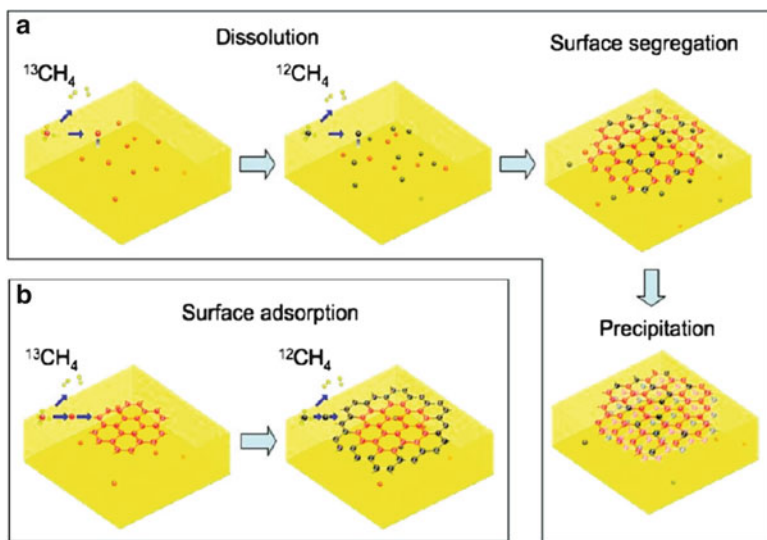


Fig. 7.6 Graphene growth mechanisms. Differentiation of graphene growth on Cu and Ni. Graphene grows on Cu by direct deposition from CVD. In Ni, graphene grows by precipitation after dissolution of carbon in the bulk (Reproduced with permission from [30]. © 2009 American Chemical Society)

Following the increased interest in graphene during the last few years, research on CVD growth of graphene became more specific about whether growth occurred via direct deposition or carbon segregation. Loginova et al. [28] intentionally used low temperatures (500–700°C) to avoid diffusion to the substrate bulk during the evaporation of C atoms over Ru(0001). In contrast, Sutter et al. [7] used higher temperature (850–1,150°C) to promote carbon dissolution and segregation for the growth of SLG and BLG. These two examples represent the ability to use different temperature ranges to select the mechanism by which graphene grows. Lowering the temperature of the CVD can lead to lower carbon solubility (7.1), therefore promoting the growth of graphene by direct deposition on the surface of the metal. The same result is obtained by using metals with low carbon solubility at the CVD processing temperature.

Growth of graphene without carbon dissolution can be done by using Cu since it has negligible carbon solubility at high temperatures [29]. At these temperatures, other metals such as Ni and Ru show significant carbon diffusion and solubility in the bulk of the films (1% at.). It was suggested that the growth of graphene on Cu is also self-limiting due to reduced hydrocarbon decomposition after the surface is covered with graphene. Li et al. [30] investigated differences between the graphene growth mechanisms on Ni and Cu. It was found that at elevated temperatures close to 1,000°C, graphene films on Ni grew by carbon segregation from the bulk whereas those over Cu grew from carbon atoms adsorbed on the Cu surface (Fig. 7.6). This was shown by switching the hydrocarbon source during CVD between ^{12}C and ^{13}C labeled methane. Spatial distributions of carbon isotopes forming the graphene could be identified by mapping the Raman G-band frequency of the graphene surface.

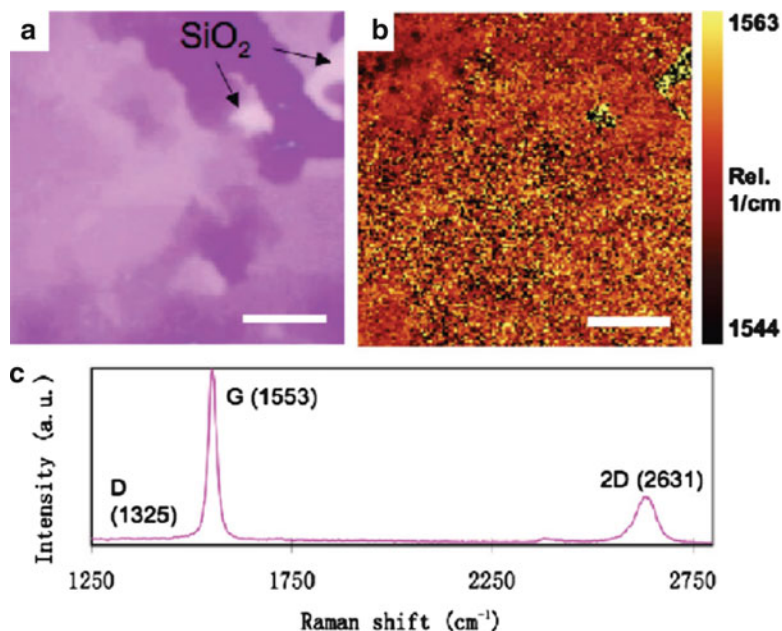


Fig. 7.7 ^{12}C and ^{13}C distribution on graphene from Ni. (a) Optical image of the surface of a graphene film grown on Ni. (b) Map of the G band frequency of the surface region in (a). The G band frequency is homogeneous across the area mapped. This suggests a homogeneous distribution of carbon isotopes across the graphene film. (c) Raman spectra obtained from (a) (Reproduced with permission from [30]. © 2009 American Chemical Society)

G-band frequencies between the isotopes are distinguishable due to their mass difference [30]. If growth of graphene occurred according to the dissolution-precipitation model, it was expected that mixing of the carbon isotopes occurred in the bulk and the resulting graphene film would be formed of randomly distributed carbon isotopes. However, if the graphene film grew without dissolution of the carbon isotopes, it was expected that the switching between the two types of methane gases would be reflected in the spatial distribution of the carbon isotopes on the grown graphene film. Dissolution of carbon was observed in Ni (Fig. 7.7) whereas no dissolution was observed in Cu during graphene growth (Fig. 7.8).

7.4 Transferring of Graphene

For most applications, it is necessary to transfer the grown graphene, usually on a metallic substrate, to dielectric ones. In this section, processes that allow this transfer will be explained with emphasis on electronic devices that use graphene as a functional material.

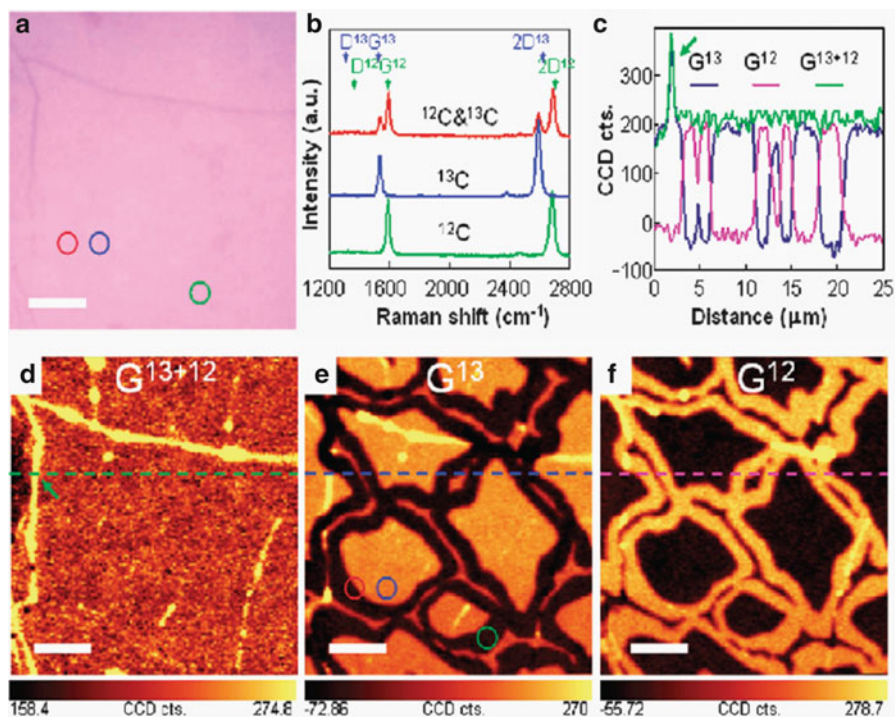


Fig. 7.8 ^{12}C and ^{13}C distribution on graphene from Cu. (a) Optical image of the surface of a graphene film grown on Cu. (b) Raman spectra from graphene composed of ^{13}C (middle curve), ^{12}C (bottom curve) and from the junction between ^{12}C and ^{13}C graphene (top curve). (c) Raman intensities from the G band signal corresponding to ^{13}C ($\text{G}^{13} = 1,500\text{--}1,560\text{ cm}^{-1}$) ^{12}C ($\text{G}^{12} = 1,560\text{--}1,620\text{ cm}^{-1}$) and both cases ($\text{G}^{13+12} = 1,500\text{--}1,620\text{ cm}^{-1}$) across the line shown in (d, e and f). Integrated intensity maps of (d) G^{13+12} , (e) G^{13} , and (f) G^{12} from the surface region shown in (a) (Reproduced with permission from [30]. © 2009 American Chemical Society)

The isolation of graphene films from the growth substrate relies on chemical etching of metallic films or substrates. This is mostly done by using a wet-etch process and there are different variations of how this can be done. One example is shown in Fig. 7.9 for thin metallic films deposited on SiO_2/Si . Before etching of the thin film, a support layer is adhered to the graphene. The purpose of this layer is to give mechanical support to the graphene layer and allow for handling after etching the metallic film. A requirement for this layer is that it can be removed after the graphene film is transferred to another substrate. Usually, this layer is poly (methyl methacrylate) (PMMA) and it has been used for similar purposes in the transfer of carbon nanotubes between different substrates [31]. PMMA is widely used as a positive e-beam resist in lithography and it can be easily dissolved in acetone. A PMMA layer is deposited on the graphene surface by spin-coating a solution of this polymer. The solution forms a thin film on the graphene surface with a thickness estimated to be around $1.5\text{ }\mu\text{m}$. The sample with the PMMA film is

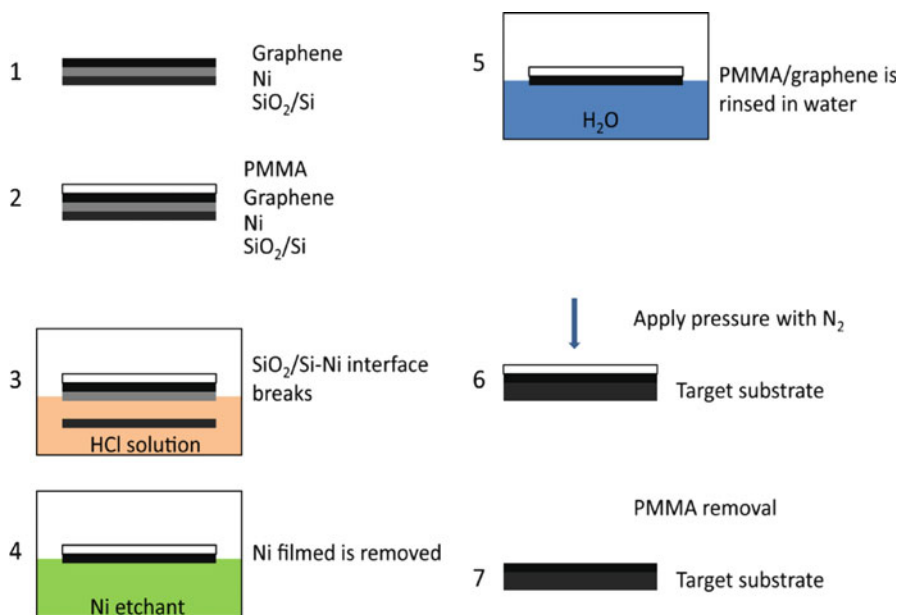


Fig. 7.9 Steps involved in the isolation of FLG films from Ni and their transfer to other substrates

baked to evaporate the solvent contained in the PMMA film. This step helps in the hardening of the PMMA layer, thereby giving it mechanical stability.

After deposition of the support layer, the metallic thin film is detached from the SiO₂-Si substrate at the metal-SiO₂ interface. This can be done by laying the substrate on an aqueous hydrochloric acid (HCl) solution. While the sample is suspended over the acid-air interface, the acid etches some of the metal in contact with the SiO₂, releasing the metal-graphene-PMMA assembly from the SiO₂/Si substrate. This typically occurs within 5 min after the sample is laid on the surface of the acid solution. After this, the released stack is transferred to water to rinse away any HCl residue. In the next step, the metal-graphene-PMMA film is laid on top of a commercial metal etchant which contains nitric acid (HNO₃). Here, the metal side of the stack is put in direct contact with the etchant to maximize the etching rate. After etching the metal film, the graphene-PMMA membrane is suspended over deionized water to rinse any residue. The membrane can be handled with conventional tweezers and laid on top of the target substrate (graphene side contacting the surface). Conformation and adhesion of graphene to the new surface is induced by applying N₂ air pressure perpendicular to the membrane surface (PMMA side). Water from the previous step is trapped between the graphene side and the substrate, and is driven towards the edges of the membrane and finally to the outside where it is dried. After 1 min of this procedure, graphene adheres to the target substrate, fixing the position of the graphene-PMMA membrane on the substrate. Lastly, the PMMA is removed by exposing it to acetone vapor or to an Ar and H₂ gas mixture at elevated temperatures (450°C).

Direct transfer of the graphene film is also possible by replacing the support layer with a target substrate of interest. It is possible to use cured PDMS stamps and place them in contact with the graphene-covered metal surface [8]. The PDMS, graphene and metal stay together due to the stickiness of PDMS. This stack is then placed on the surface of an etchant to etch away the metal and leave the graphene on the PDMS. Subsequently, graphene devices can be used directly. Alternatively, PDMS can be used as a stamp to place the graphene on another substrate. The ability of placing graphene on a flexible substrate such as PDMS allows the testing of graphene conductivity under bending and stress. Bending experiments of graphene on these substrates show that there is little change in resistance for a 2.5 mm bending radius (6.5% tensile strain) which is reversible upon releasing the bending. For a 0.8 mm bending radius (18.6% tensile strain), the original resistance can be recovered. Uniaxial strain on the PDMS shows changes of resistance of around one order of magnitude which are reversible; however, mechanical failure sets in at around 6% of uniaxial strain. It is possible to enhance the mechanical performance of graphene electrodes by transferring them to pre-stretched PDMS. This creates wrinkles on the graphene film that help stabilize the film upon stretching. When this is done, the resistance is stable up to 11% of uniaxial strain and a change of one order of magnitude in resistance is obtained at 25% uniaxial strain.

These electromechanical properties show that graphene films are not only the strongest but also the most flexible and stretchable conducting transparent materials so far measured [8]. The scalability of graphene transfer processes could permit the integration of CVD graphene in several applications. Scalability for transferring graphene has been demonstrated with the transfer of 30 in. graphene films for transparent electrode applications by a roll-to-roll process [32]. Graphene is produced by a low pressure CVD process on a copper foil. A thermal adhesive is coated on the graphene covered foil by passing the adhesive and foil together between two rollers while applying a small pressure of 0.2 MPa. After this, the copper foil is etched by exposing it to a 0.1 M ammonium persulphate aqueous solution. This is also done using rollers. Lastly, graphene is transferred to a target substrate by passing the target substrate and the graphene/adhesive film together between two rollers. This is done with the application of mild heating (90–120°C) in order to release the adhesive film from graphene while leaving graphene attached to the target surface. This process achieves a rate of transfer of 150–200 mm min⁻¹ and was used for the fabrication of touch screen panels with graphene as a transparent electrode.

These transfer processes can be modified to suit various applications. A transfer free process can be applied for the fabrication of large arrays of graphene-based FETs on SiO₂/Si substrates. This can be done by growing graphene on thin metallic films deposited on SiO₂/Si and using the metal film to fabricate electrodes, with the SiO₂/Si substrate as the support (Fig. 7.10). The fabrication involves spin-coating a photoresist over the graphene surface and patterning the device geometry consisting of two electrodes joined by a device channel (which is a graphene strip). The unprotected graphene is removed by oxygen plasma. At this point, the unprotected metal is etched by a wet process. The metal below the channel region is also etched

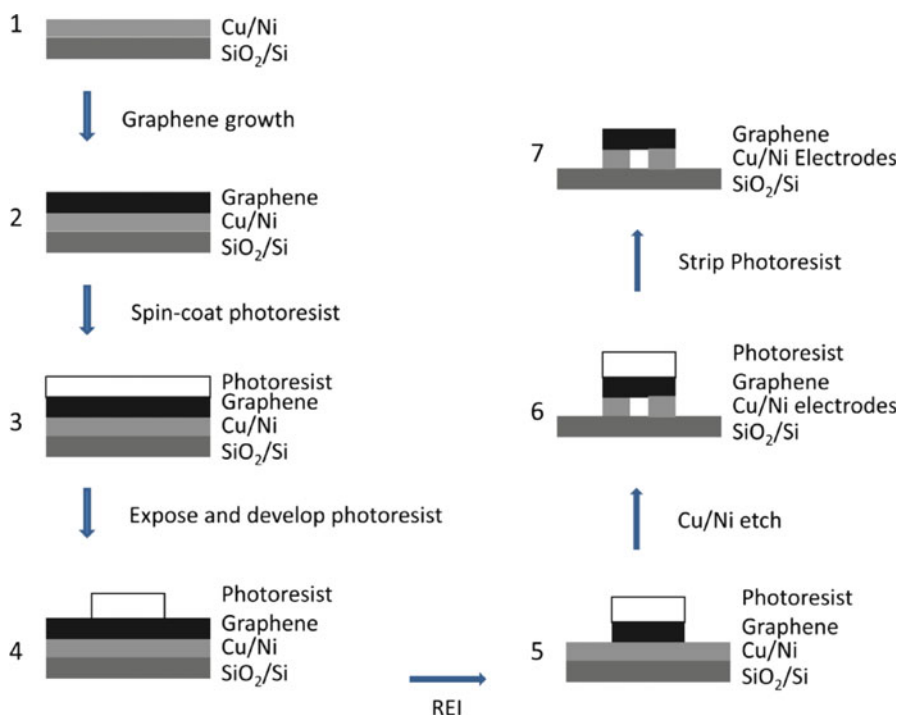


Fig. 7.10 A transfer free process for the fabrication of graphene FET arrays. First, the graphene covered metal thin film is covered with a photoresist by spin-coating. The device geometry is then patterned over the photoresist. The unprotected graphene is etched with oxygen plasma. Then, the sample is wet-etched by which the unprotected metal as well as the metal below the device channel are etched away. Finally, the photoresist is removed, leaving behind two electrode pads joined by a graphene strip (device channel) (Adapted from [33])

due to lateral etching, thereby producing a graphene channel resting on the SiO_2/Si surface. After removing the remaining photoresist, the process results in a complete FET device consisting of two metal electrodes joined by a graphene strip. This process was demonstrated using a thin film of a Cu/Ni alloy [33]. With this process a failure rate of less than 5% was obtained using a channel device dimension of up to 0.5 mm. The devices also show a good carrier mobility of $\sim 700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and transconductances of $8 \mu\text{S } \mu\text{m}^{-1}$.

7.5 Control of Graphene Film Quality

The quality of graphene films is important for electronic properties and influence the resistivity and carrier mobility. So far, exfoliated graphene has shown the highest mobility amongst the various graphene types. CVD growth methods are

starting to produce graphene with properties close to that of exfoliated graphene. In this section, the quality of these films will be quantified by domain size, defect density, and thickness uniformity. Recent work has shown that several parameters affect graphene quality including the type of substrate material, structure of the substrate (polycrystalline vs. single-crystalline), and CVD process parameters. Furthermore, it has also been shown that grain boundaries within graphene films can significantly degrade electronic properties, therefore justifying efforts for finding better ways to produce larger domain size graphene films.

7.5.1 CVD Parameters

There are numerous parameters in the CVD processes that affect the attributes of the graphene film; these include: temperature, hydrocarbon pressure, hydrocarbon concentration, and cooling rate. In addition, the growth mechanism of graphene may be different depending on the type of metal used. While a discussion of current understanding is given in this section, more research is necessary to elucidate the complete mechanism of graphene growth for different metals.

7.5.1.1 CVD Parameters and Graphene Domain Size

CVD parameters can be used to control the grain size of graphene [34]. An example of this is shown by graphene grown over polycrystalline Cu foils. Parameters such as temperature, methane flow rate and partial pressures seem to affect the number of graphene nucleation islands. These islands continue to grow after nucleation and they eventually join each other. Therefore, the number of nucleation sites at the beginning of the process determines the average graphene domain size.

Figure 7.11 shows SEM images of a Cu surface partially covered with graphene islands under different conditions. Panels (a) and (b) show surfaces under the same conditions except with different processing temperatures (985°C and 1,035°C, respectively). Panel (c) shows the case for the same conditions as (b) but with lower methane flux (7 sccm vs. 35 sccm). Panel (d) shows the case for the same conditions as in (c) but with lower methane partial pressure (160 mTorr vs. 460 mTorr). The graphene island density and their sizes decrease and increase, respectively, with higher temperatures and lower methane flux and partial pressures. These three parameters control the amount of C-species supersaturation on the Cu surface, therefore, changing the density of nucleating graphene domains. However, conditions that yield low nucleation densities also yield an incomplete coverage of the Cu surface. This is explained by the fact that the C-species supersaturation required for a continuous graphene growth is halted due to the combination of the coverage of the Cu surface and low methane flux and partial pressures.

Based on these observations, the CVD process can be modified into a two step process to give a continuous graphene layer with an optimized graphene grain size.

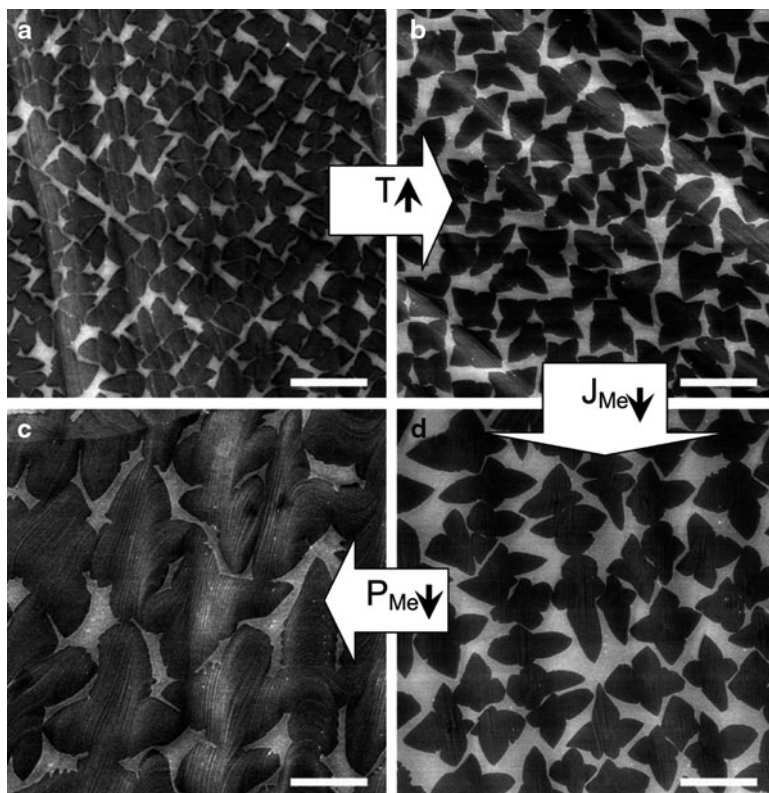


Fig. 7.11 SEM images of partially grown graphene under different growth conditions to elucidate the effect of temperature (T), methane concentration (J_{Me}) and methane partial pressure (P_{Me}) on the graphene domain size. $T(^{\circ}\text{C})/J_{Me}(\text{sccm})/P_{Me}(\text{mTorr})$: (a) 985/35/460, (b) 1035/35/460, (c) 1035/7/460, and (d) 1035/7/160 (Reproduced with permission from [34]. © 2010 American Chemical Society)

The first step includes low methane flux and partial pressures in order to generate a low graphene island density. The second step includes high methane flux and partial pressures to complete the growth of such islands and cover the Cu surface completely. A schematic of this process is shown in Fig. 7.12. For a given temperature and partial pressure, once the nucleation density is fixed, no new graphene nuclei are formed and the changes in conditions from step 1 to step 2 only affects the growth rate. The result of this process can be tested by isotope-labeled methane. The first step is done with ^{13}C labeled methane and the second one with ^{12}C methane. The distribution of carbon isotopes can be mapped by Raman spectroscopy in order to locate regions grown in each step of the process. Figure 7.13 shows optical images and Raman maps of the G and D band for graphene films grown with two different two step processes. The two processes are done at the same temperature. The film shown in Fig. 7.13a–c was grown with 7 sccm of methane and 160 mTorr for the first

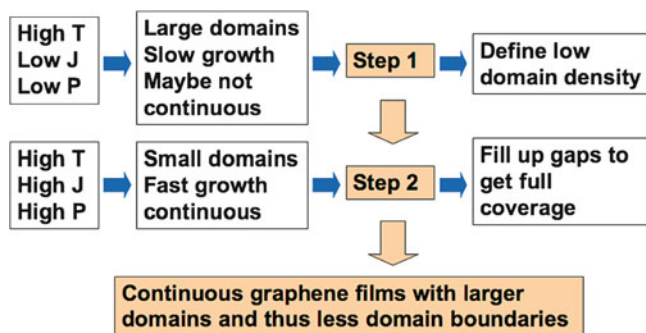


Fig. 7.12 Conditions involved in order to obtain a continuous graphene film with a maximized domain size (Reproduced with permission from [34]. © 2010 American Chemical Society)

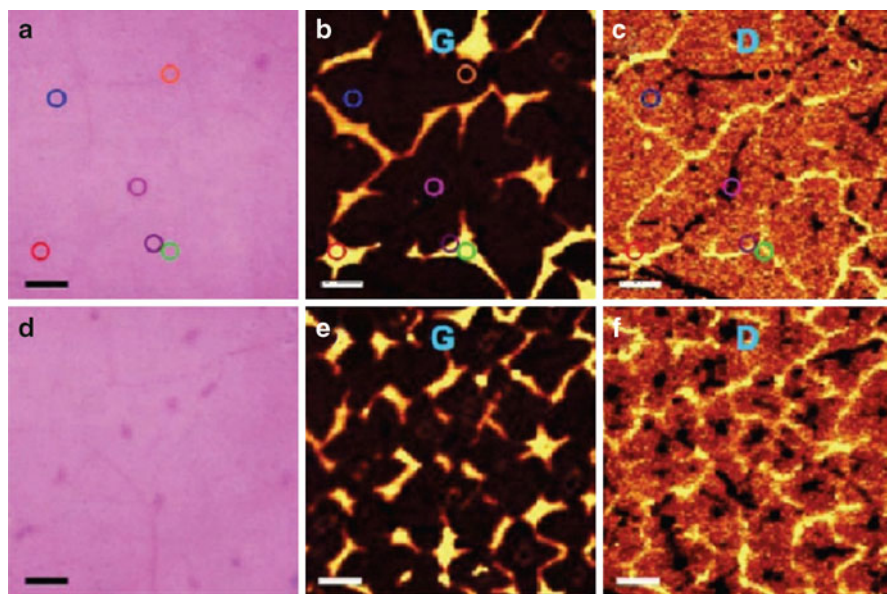


Fig. 7.13 Optical images and Raman mapping of graphene films transferred to SiO₂/Si substrates. Optical images (a, d), Raman G¹² maps (b, e) and Raman D¹² mapping (c, f) of films A (a) and B (b), respectively. The G¹² signal corresponds to the second step in the process in Fig. 7.17 confirming that the completion of the film takes place at this step of the process. Film A is grown with the following conditions ($T(^{\circ}\text{C})/J_{Me}(\text{sccm})/P_{Me}(\text{mTorr})$): step 1: 1035/7/160 and step 2: 1035/7/2000. For film B: step 1: 1035/35/460 and step 2: 1035/35/2000 (Reproduced with permission from [34]. © 2010 American Chemical Society)

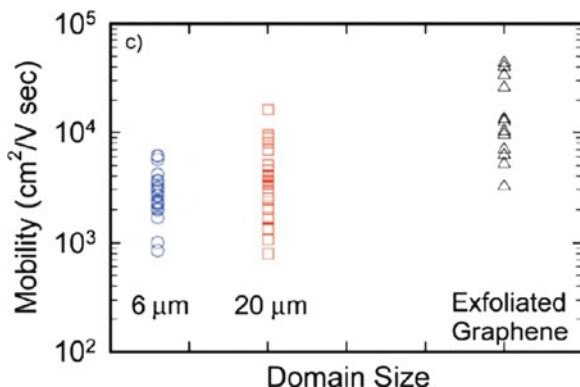


Fig. 7.14 Carrier mobility as a function of graphene domain size in comparison to exfoliated graphene (Reproduced with permission from [34]. © 2010 American Chemical Society)

step. The film shown in Fig. 7.13d–f was grown with 35 sccm of methane and 460 mTorr for the first step. For both cases, in the second step, the pressure was 2,000 mTorr. The first and second films result in an average graphene domain area 142 and 332 μm^2 , respectively.

The optimization of the graphene domain size is reflected in the carrier mobility measured in graphene-based field effect transistors (FET). Figure 7.14 shows the mobility measured for graphene films with average grain sizes of 6 and 20 μm and exfoliated graphene. For the film with 6 μm domains, the range of mobility is from 800 to 7,000 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. The mobility measured for the film with 20 μm domains lie between 800 and 16,000 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ whereas mobility for exfoliated graphene ranges from 2,500 to 40,000 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$.

Optimizing the domain size affects the resistivity of the graphene film. Resistivity measurements on a graphene flake consisting of two single crystal domains show that a significant change in resistivity is associated by a grain boundary [35]. Differences between resistivities within a grain and across a grain boundary are found for many other devices.

7.5.1.2 CVD Parameters and Thickness Uniformity

Film thickness uniformity can be changed by different process parameters depending on the growth mechanism involved. In the case of direct deposition of graphene over surfaces such as Cu, optimization of thickness uniformity can be performed through parameters such as pressure and hydrocarbon concentration. Otherwise, for graphene growth based on the dissolution and segregation of carbon, the thickness uniformity has to be optimized predominantly by the cooling rate of the film.

Figure 7.15a shows a schematic of a simple CVD model. Here, no dissolution of carbon is considered and therefore it can only be applied for metals with

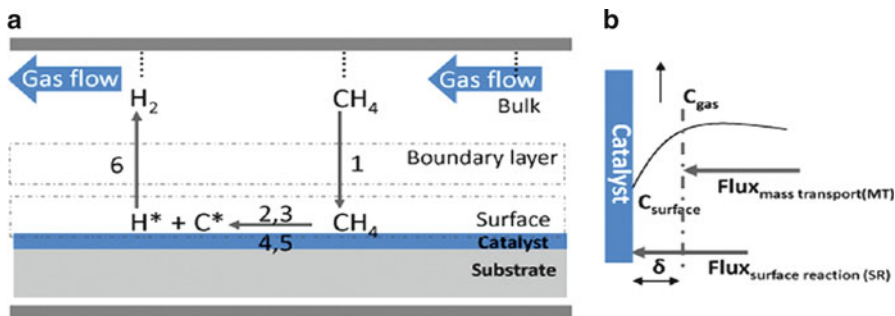


Fig. 7.15 (a) Steps involved in a CVD process for graphene growth on a low solubility metal substrate like Cu. (b) Mass transport and surface reaction fluxes at steady state conditions (Reproduced with permission from [36]. © 2010 American Chemical Society)

low carbon solubility such as Cu or for low temperature CVD processes in which the carbon solubility is also negligible. This CVD model can be used to provide an understanding of the effect of kinetic factors such as pressure and methane concentration on the thickness uniformity of graphene films. This model considers the following process as part of the CVD process: (1) diffusion of hydrocarbon species from the gas phase to the region near the metal surface, (2) adsorption of hydrocarbon species on the metal substrate, (3) decomposition of the hydrocarbon to active species, (4) diffusion of active species and formation of graphene on the metal surface, (5) desorption of inactive species such as atomic hydrogen (H^*) and formation of molecular hydrogen (H_2) and (6) diffusion of inactive species to the gas phase.

The processes can be divided into two groups, those that take place near the surface (2–4) and those taking place at the boundary layer formed by the flow of the gas over the surface (1,6). Therefore, it is possible to model this process with two fluxes in series—one corresponding to the diffusion of species through the boundary layer (mass transport) and the second corresponding to the consumption of carbon species at the surface (surface reaction). These fluxes are:

$$F_{transport} = h_g(C_g - C_s) \quad (7.3)$$

$$F_{reaction} = K_s C_s \quad (7.4)$$

where h_g is the mass transport coefficient, C_g and C_s are the hydrocarbon concentration in the gas phase and the surface of the metal, respectively, and K_s is the surface reaction constant. Both of these fluxes are assumed to have first order kinetics. At steady state, both fluxes should equal each other:

$$F_{reaction} = F_{transport} = \frac{K_s h_g}{K_s + h_g} C_s \quad (7.5)$$

The total flux of active species and therefore the growth of the graphene film can be limited either by the surface reaction constant ($K_s \gg h_g$), the mass transport constant ($K_s \ll h_g$) or both ($K_s \approx h_g$). At high temperature and ambient pressure, mass transport through the boundary layer is rate-limiting ($K_s \gg h_g$); under low pressure/UHV conditions, the surface reaction is the rate limiting step ($K_s \ll h_g$). At high temperatures (900°C) and atmospheric conditions, growth is limited by mass transport since at these temperatures decompositions occur much faster due to their exponential dependence on temperature. Also, diffusion of species is lower due to atomic collisions:

$$h_g = \frac{D_g}{\delta} \quad ; \quad D_g \propto \frac{1}{P} \quad (7.6)$$

Where δ is the boundary layer thickness, D_g is the diffusivity of the gas species and P is the overall pressure. When working under the mass transport regime, the supply of species is affected by local variations of the flow profile of gases in the CVD chamber. Therefore, some thickness nonuniformity across the sample is expected [36]. In order to minimize flow effects on the thickness uniformity of samples, it is better to work in the surface rate limiting step. This can be done by decreasing the working pressure enough so that $K_s \ll h_g$. These trends are consistent with observations of the thickness uniformity accomplished with ambient pressure and low pressure conditions [36]. Results show that low pressure conditions are more favorable for accomplishing uniform SLG [36]. Ambient pressure conditions demonstrate that graphene growth on copper is not self-limiting [36]. The growth of multilayer graphene islands is evident in multiple conditions. Such islands are minimized and uniform SLG can be achieved under ambient pressure by decreasing the methane concentration significantly to about 100 ppm.

The cooling rate during the CVD process can be used to improve the thickness uniformity of the FLG films in the case of graphene grown by the segregation mechanism [9, 15]. The morphology of films obtained with fast cooling rates ($>100^\circ\text{C min}^{-1}$) can be very different when compared with that obtained with cooling rates below $25^\circ\text{C min}^{-1}$. The most important effect of lower cooling rates is an improvement of the area covered by SLG and BLG. When fast cooling rates ($>100^\circ\text{C min}^{-1}$) are used, the film consists mostly of graphene with more than two graphene layers, Fig. 7.16a, b. Multilayer graphene with more than two graphene layers grows around the grain boundaries of the polycrystalline Ni film. Graphene films consisting mostly of SLG and BLG (Fig. 7.16c, d) are obtained by using low cooling rates ($<25^\circ\text{C min}^{-1}$). It is observed that not all grain boundaries on the polycrystalline Ni show the nucleation of multilayers, resulting in an increase of the area fraction covered by SLG and BLG.

The area covered by SLG and BLG (θ_{I-2LG}) is dependent on the cooling rate in the regime of $<25^\circ\text{C min}^{-1}$. Figure 7.17 shows that decreasing the cooling rate below $25^\circ\text{C min}^{-1}$ during the segregation step further increases the area fraction of S/BLG

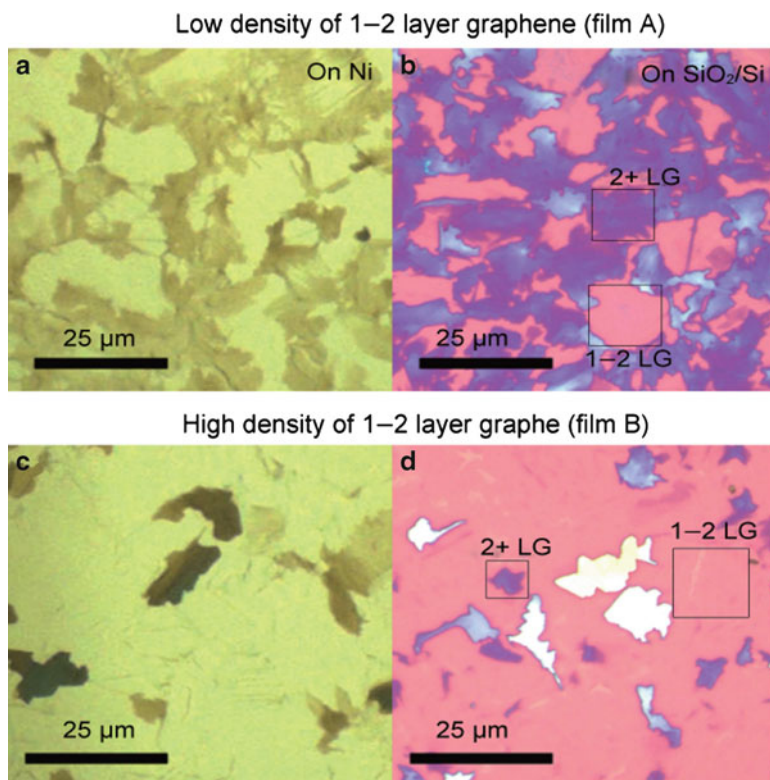


Fig. 7.16 The effect of cooling rate. Optical images of FLG films grown with fast ($>100^{\circ}\text{C min}^{-1}$) (a, b), and slow ($<25^{\circ}\text{C min}^{-1}$) (c, d) cooling rates before (a, c) and after transferring (b, d) to $\text{SiO}_2\text{-Si}$. With fast cooling rates, multilayer graphene with more than two layers forms around the grain boundaries of the Ni film. With slow cooling rates, multilayer graphene precipitates on isolated islands randomly distributed across the Ni film. Regions between the islands are formed by SLG or BLG (Reproduced with permission from [15]. © 2009 Springer)

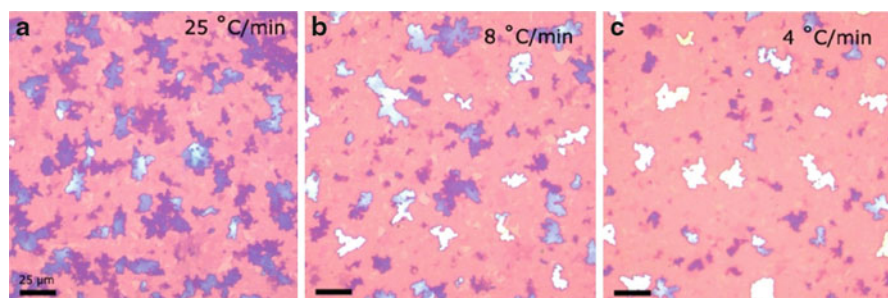


Fig. 7.17 FLG films transferred to $\text{SiO}_2\text{-Si}$ and grown with three cooling rates. Decreasing cooling rates are shown from left to right. The density of multilayer islands decreases with decreasing cooling rates. Regions between the islands consisting of SLG and BLG increase in area fraction with decreasing cooling rates (Reproduced with permission from [15]. © 2009 Springer)

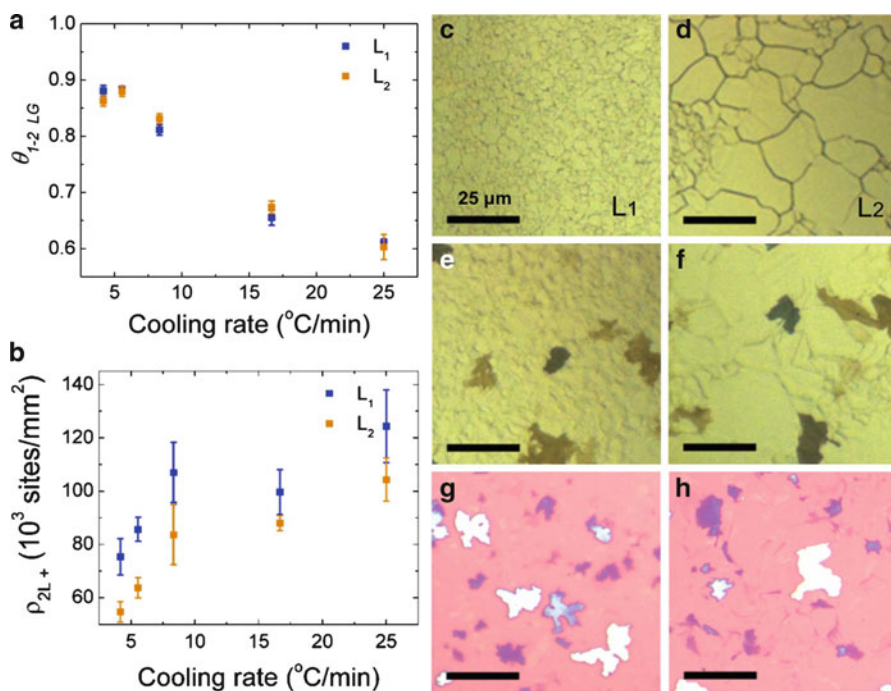


Fig. 7.18 Area fraction of regions with SLG and BLG. (a) Area fraction occupied by SLG and BLG as a function of cooling rate. (b) Density of multilayer islands (three layers or more) as a function of cooling rate. (a) and (b) includes data for two Ni grain sizes (L_1 and L_2 in black and grey, respectively). (c, d) Optical images of pristine Ni films with grain sizes L_1 and L_2 , respectively. (e, f) Optical images of Ni films with the same grain sizes after the CVD process. (g, h) FLG transferred to SiO_2 -Si and grown on Ni films with L_1 and L_2 , respectively (Reproduced with permission from [15]. © 2009 Springer)

(light background). The area fraction with no more than two layers (θ_{1-2LG}) increases as the cooling rate is decreased and it can be tuned from 0.6 to 0.87, Fig. 7.18a. In addition, the slower the cooling rate, the fewer are the nucleation sites of multilayer graphene, Fig. 7.18b. The area covered by SLG and BLG is plotted together since this is the area fraction changing noticeably with the cooling rate. The area fraction with SLG is estimated to remain constant close to 0.1–0.15. Optical images of graphene films grown with $4^{\circ}\text{C min}^{-1}$ on two Ni grain sizes before and after transferring to SiO_2 -Si are shown in Fig. 7.18e–h, respectively.

The cooling rate can also determine whether a graphene film forms at all [9] and influences the structural nature of the graphene film [9] (Fig. 7.19). With cooling rates as low as $0.1^{\circ}\text{C min}^{-1}$, no graphitic carbon is detected on the Ni surface by Raman spectroscopy, indicating that carbon segregation was not sufficient to form a graphene film. The film, if formed, was at least not thick enough to be detected by Raman spectroscopy. It is reported that Raman signal suppression of a monolayer

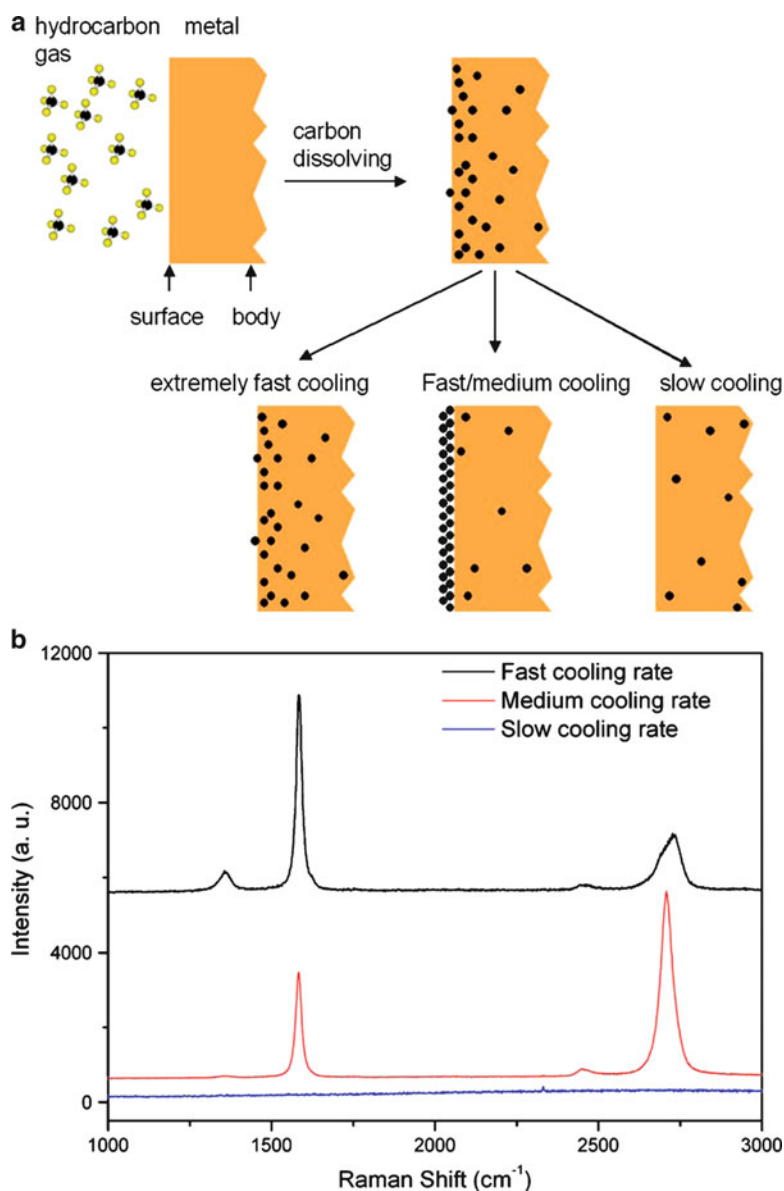


Fig. 7.19 (a) Schematic of the carbon segregation for graphene growth for different cooling rates. At low cooling rates ($0.1^\circ\text{C min}^{-1}$) no graphene film is grown due to diffusion of carbon species into the bulk of the metal film. Graphene growth is obtained at high and intermediate cooling rates ($10\text{--}20^\circ\text{C min}^{-1}$). (b) Raman spectroscopy of the metal surface for the three cooling rate regimes confirming that no graphene spectrum is observed at slow cooling rates. For intermediate cooling rates, the graphene film has a lower density of defects compared to that obtained with fast cooling rates (Reproduced with permission from [9]. © 2008 American Institute of Physics)

of graphene over transition metals is possible. With a medium cooling rate of around $10^{\circ}\text{C min}^{-1}$, the G and the G' bands are observed (without a defect-related D band). TEM analysis shows a graphene film of three to four layers. With faster cooling rates (up to $20^{\circ}\text{C min}^{-1}$), a D band is now observed which suggests a higher density of defects. A higher cooling rate may give less time to carbon atoms to form a good graphitic structure before the temperature is too low, thus resulting in a higher density of defects.

7.5.1.3 Uniform Bilayer Graphene by CVD

Most research on CVD of graphene has focused on growing SLG over large areas. However, SLG graphene is a semimetal and therefore, it lacks an intrinsic band gap which this limits the number of applications possible. Several ways to induce a band gap in single-layer graphene have been explored, which include, patterning nanometer width graphene ribbons [37, 38] or using special substrates [39]. Bilayer graphene (BLG) can develop a band gap of up to 250 meV by the application of a vertical electric field across the two layers [40].

The production of uniform BLG using CVD on copper foils was demonstrated over areas of at least $2'' \times 2''$ [41]. The process is similar to that for uniform SLG, however, the key changes in CVD conditions which permit the growth of BLG graphene include the depletion of hydrogen, high vacuum, and a slower cooling rate compared to SLG growth. The optimal growth conditions for BLG graphene on copper foils occur at $1,000^{\circ}\text{C}$ for 15 min with a pressure of 0.5 Torr, a methane flow rate of 70 sccm, and a cooling rate of $18^{\circ}\text{C min}^{-1}$. Evidence for the existence of uniform BLG after this process includes AFM height measurements, electron diffraction, Raman spectroscopy and transport measurements. An important characteristic of the bilayer grown on copper foils is that the layers are stacked in an AB manner which allows for the induction of a band gap with electric fields. This can be demonstrated by constructing BLG field effect transistors with two independent gates. The independent operation of these two gates (top and bottom) allows a decoupled control of both the induced band gap and the carrier density in the transistor [40, 41].

Although research on the growth of uniform BLG graphene is very recent, results suggest that the most important parameter is the lowering of cooling rates during the CVD process [41]. Doubling the methane flow rate leads to the growth of SLG graphene with no other noticeable effects except for an increase in the defect density. Increasing the chamber pressure so far has resulted in the increase of the trilayer content of these films. The most uniform BLG samples (estimated coverage of 99% by Raman spectroscopy) are produced when the cooling rate is decreased significantly to $18^{\circ}\text{C min}^{-1}$. More detailed studies in the growth mechanism of BLG on copper and other metals are therefore expected to develop in the near future.

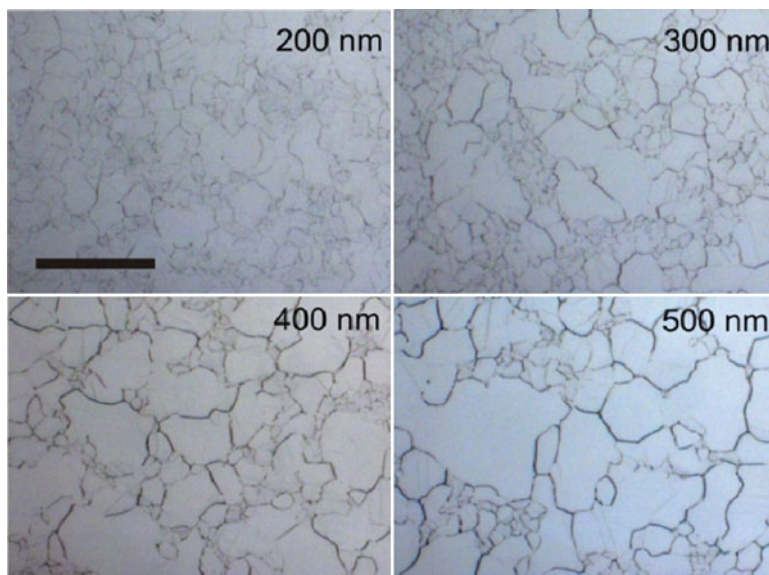


Fig. 7.20 Optical images of Ni thin films after being annealed in H_2 and Ar at $1,000^\circ\text{C}$ for 20 min. Scale bar is $20\ \mu\text{m}$

7.5.2 Crystallinity of Metal Substrates

7.5.2.1 Polycrystalline Substrates

Polycrystallinity of substrates seems to affect thickness uniformity of the grown graphene film. In Ni, the dissolution of carbon in the bulk limits the control of the amount of carbon participating in the formation of the graphene film. Extra carbon species tend to form multilayer graphene islands and multilayer graphene seems to form on grain boundaries of the polycrystalline metal substrate.

Figure 7.20 shows SEM images of Ni films with various grain sizes. The thickness of the Ni film has a strong influence on grain size. Figure 7.21 shows graphene films obtained from the same Ni films in Fig. 7.20. The distribution of multilayer graphene (dark regions) resembles the boundaries seen in Fig. 7.20. The thickness of the substrate also seems to have an effect on graphene thickness (Fig. 7.22) as measured by film transparency. This may be due to larger number of graphene layers nucleating at grain boundaries.

The polycrystallinity of some metal films like Ru and Cu surprisingly seem not to influence graphene domain orientation. Moreover, better thickness uniformity can be accomplished with Ru and Cu polycrystalline films and foils [12, 42] with a coverage of SLG up to 95% using Cu foils [42]. On Ru polycrystalline thin films deposited on SiO_2/Si , graphene grows continuously over the Ru grains as suggested by the moiré patterns observed over two Ru grains with graphene [12]. Figure 7.23 shows

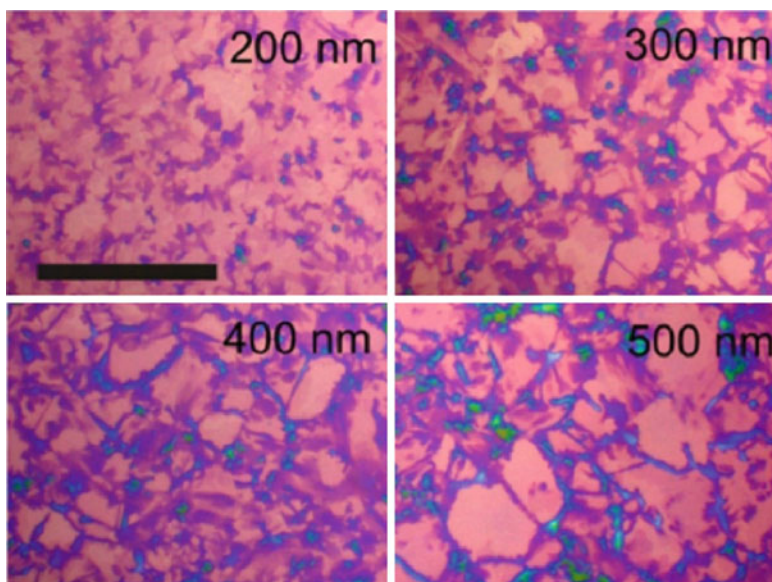


Fig. 7.21 Effect of Ni film thickness. FLG films transferred to a SiO_2 substrate after grown from Ni films of various thicknesses. Scale bar: $25\ \mu\text{m}$

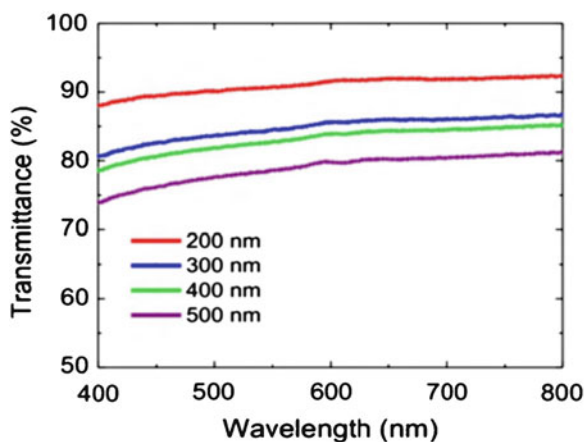


Fig. 7.22 Transparency across the visible range of FLG films

two cases of Ru grains with contrasting moiré patterns. All grains in the film have a (0001) texture but the grains have different in-plane rotations. For a single graphene domain over two of these Ru grains, it should be expected that different moiré patterns arise from each grain. It is possible to show that the relation between the change in pattern orientation (θ) and the change of the relative scaling of the pattern

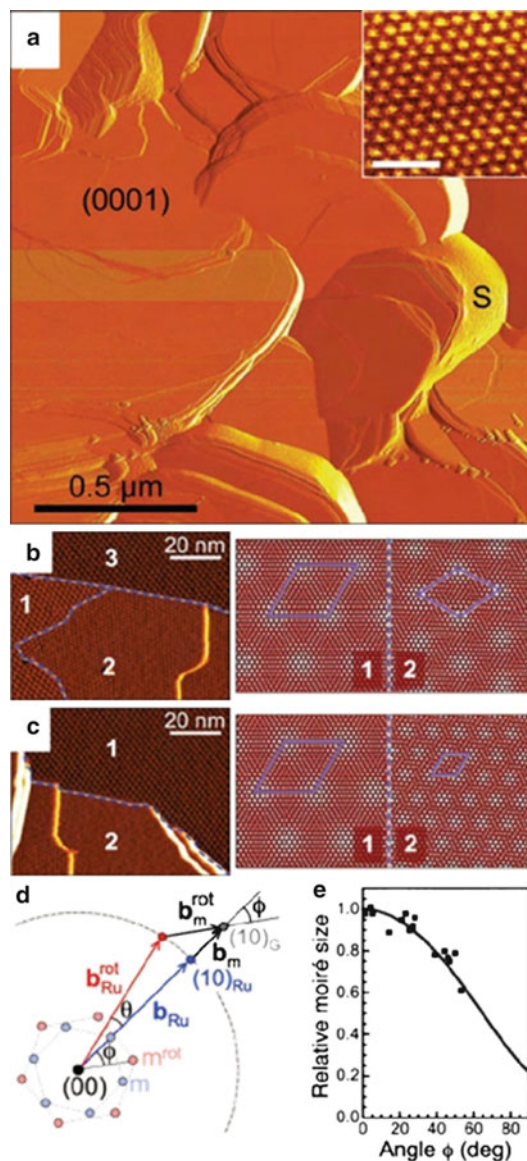


Fig. 7.23 (a) STM image showing the topography of the polycrystalline Ru film grown on SiO₂ ($V = +0.4$ V, $I = 0.2$ nA). The inset shows a high magnification view of the graphene/Ru moiré structure (scale bar: 10 nm). (b, c) STM images of the moiré patterns over different Ru grains and the grain boundaries that separate them. (d) Reciprocal representation of the moiré patterns resulting by the rotation of the Ru lattice with a fixed graphene rotation. (e) Relative moiré size as a function of the rotation of the Ru lattice with a fixed graphene rotation. The panels on the right show models of the abrupt change in the moiré resulting from an in-plane rotation of the Ru lattice due to different in-plane orientations in each grain. The curve represents the theoretical relationship between moiré orientations and scalings assuming a continuous graphene sheet connecting contiguous Ru grains with different orientations. (Reproduced with permission from [12]. © 2009 American Institute of Physics)

unit cell (**b**) can be reproduced by in-plane rotations of the underlying Ru with a fixed graphene domain orientation (Fig. 7.23). Graphene moiré patterns can be observed without defective boundaries over areas of several μm^2 whereas the Ru grain size is around 0.5–0.6 μm . Similar observations were found for Cu polycrystalline thin films [36]. The continuous growth of graphene over grain boundaries is relevant since they open the possibility of growing graphene with single-crystal domains larger than the polycrystalline metal film. Therefore, it could be possible to obtain higher quality graphene films without the use of single-crystal substrate. The advantages of using polycrystalline films are ease of fabrication and lower cost as compared to.

7.5.2.2 Single-Crystal Metal Substrate

Single-crystal substrates offer the possibility of avoiding multilayer graphene nucleation. Furthermore, it also provides a possible improvement of single-crystal domain size in the graphene film. Graphene growth on bulk single-crystal metals is well known [1]. Graphene typically grows on the (0001) surface of metals with hexagonal structures such as Ru and on (111) surfaces of metals with face centered cubic structures such as Ni and Cu [7, 42]. It is also possible to use single-crystal metallic thin films. Such films are advantageous since etching them is faster, simpler and less expensive than bulk crystals. Graphene growth over single-crystal metal thin-films is possible with Ru [13], Ni [43] and Cu [44]. These thin films are usually grown by sputtering and epitaxially over substrates with the same surface orientation needed for the metal film. The support substrate should also have a similar lattice constant as the metal used. For Ru (0001) and Cu (111) films, Al_2O_3 (0001) can be used as support. For Ni (111), $\text{MgO}(111)$ can be used. Graphene regions with the same moiré pattern, without defects and grain boundaries, are observed over a few μm^2 areas [13] on Ru single crystal thin films. LEED suggests the epitaxial growth of graphene single crystals of at least 1 mm^2 over a single-crystalline Ni thin film (Fig. 7.24) [43]. Graphene growth is also possible on Cu thin films grown over sapphire (0001) [44]. However, more detailed graphene structure characterization has been reported on bulk single-crystalline Cu [45]; here, multiple graphene nucleation islands are observed (Fig. 7.25). These islands have two predominant moiré patterns despite the single-crystal nature of the Cu surface and can be explained by a low energy interaction between graphene and Cu [45]. These two moiré patterns correspond to two different graphene crystal orientations which generate multiple grain boundaries when the islands join each other during growth (Fig. 7.25).

7.5.2.3 Growth on Ni(111)

Blakely et al. [46] studied the segregation of carbon on a Ni(111) surface; such studies are primarily aimed towards understanding the segregation of impurities in

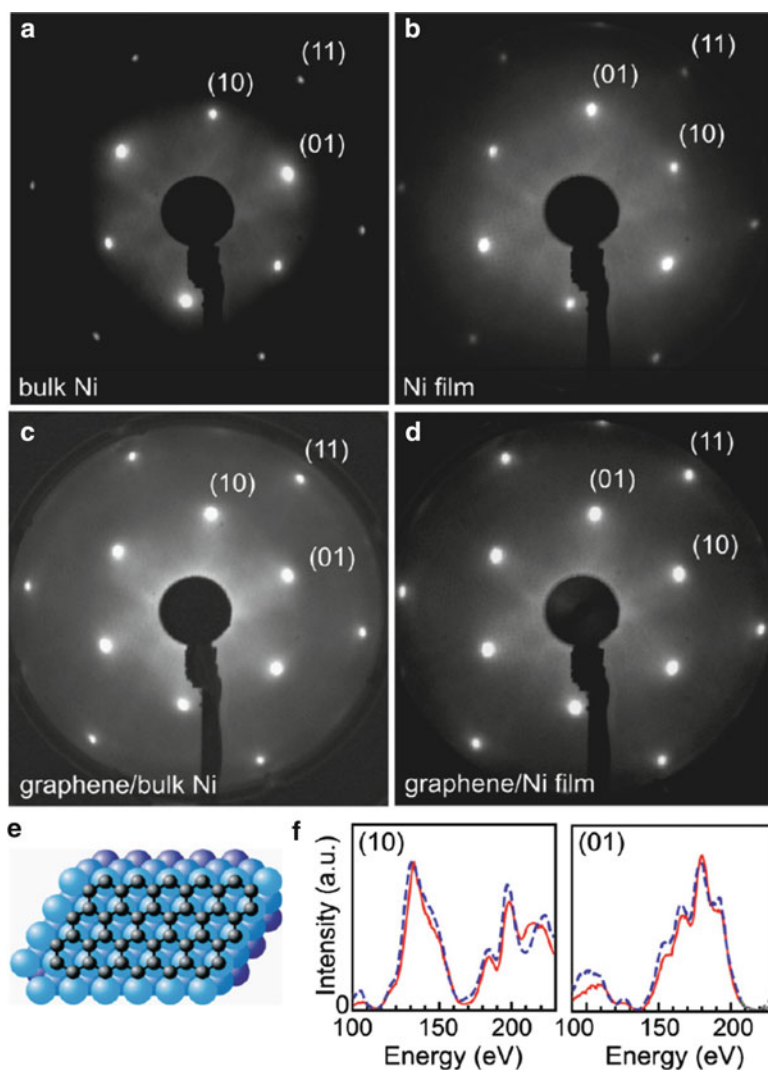


Fig. 7.24 LEED patterns of a clean Ni(111) bulk crystal (a), a clean Ni(111) thin film on MgO(111) (b), graphene synthesized on a Ni(111) bulk crystal (c), and graphene synthesized on a Ni(111) thin film on MgO(111) (d). Patterns were recorded for a primary electron energy of 185 eV. The spot size is 1 mm². The LEED patterns in (c) and (d) lack a moiré pattern due to the small lattice mismatch of 1.2% between Ni and graphene. (e) Atomic configuration of graphene on Ni(111) based on the LEED patterns obtained. (f) I–V curves of the (10) and (01) spots extracted from the Ni(111) film (solid line) and the Ni(111) bulk crystal (dashed line). At the electron energy at which the (01) spot intensity reaches a minimum, the (10) spot has a high intensity and vice versa. This serves as an unambiguous proof that boundary formation is absent (Reproduced with permission from [43]. © 2011 American Chemical Society)

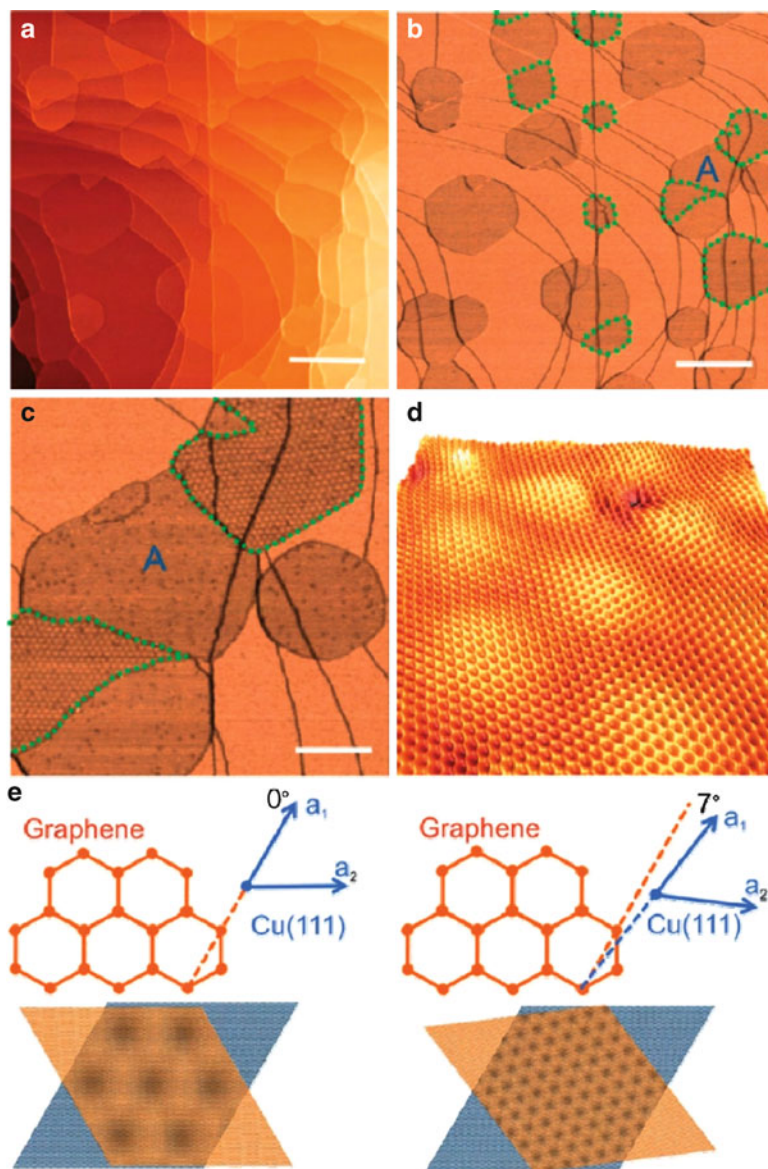


Fig. 7.25 (a) STM topography of graphene partially covering a Cu(111) substrate (scale bar: 200 nm). (b) Differential conductance dI/dV image ($U = -200$ mV) of the same region as (a) which increases the contrast between graphene domains and the Cu(111) substrate. *Dotted lines highlight the boundaries defining graphene domains.* The graphene domains show a moiré pattern together with the underlying Cu(111) surface. (c) A higher magnification dI/dV image of a graphene island—spot “A” in (b). Scale bar: 60 nm. (d) Atomic resolution STM image of graphene showing a moiré pattern and a *honeycomb structure* corresponding to the graphene lattice. (e) and (f) show the two graphene orientations observed with respect to the Cu(111) lattice (Reproduced with permission from [45]. © 2010 American Chemical Society)

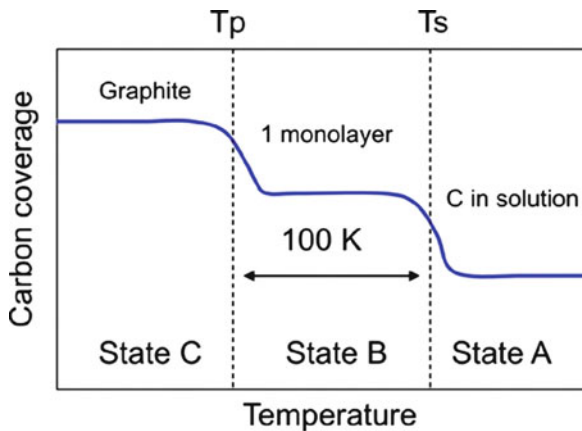


Fig. 7.26 Schematic view of the surface segregation phases on the Ni(111)–C system. The *vertical axis* represents the amount of carbon segregated on the surface and the *horizontal axis* represents temperature

metals since such segregation contributed to the hardening of metal structures. Instead, the study showed that SLG could be grown on a Ni(111) surface. In the study, carbon was introduced into a Ni substrate by contacting the top Ni(111) surface of the sample with a graphite piece at an elevated temperature. After equilibrium is reached, the concentration of carbon in the metal is known. Following this, the Ni(111) substrates are heated in UHV. During cooling of the samples, it was observed that carbon segregated on the Ni surface and formed only a monolayer of graphite. It was found that segregating carbon atoms formed three distinct stable phases on a Ni(111) surface at different temperature ranges and at bulk carbon concentrations of 1% at. The three observed phases are the following (Fig. 7.26): (1) a high temperature phase ($T > T_s$) consisting of diluted carbon atoms on the surface, (2) an intermediate phase ($T_p < T < T_s$) where the segregating carbon atoms form a monolayer of graphite on the Ni(111) surface, (3) a low temperature phase ($T < T_p$) in which precipitation of graphite occurs. These observations were the first reports of distinct transitions between phases of segregations [45]. The intermediate phase exists for a range of 100 K before the graphite precipitate appears. Blakely et al. differentiate between equilibrium segregation and precipitation. The former refers to an accumulation of impurities at a surface during compositional homogeneity in thermal equilibrium, i.e. while the system is at the one-phase field of the phase diagram (metal + diluted impurities). This description is assigned to the first transition (T_s). Equilibrium precipitation refers to inhomogeneities which arise due to equilibrium phase separation. This is assigned to the second transition (T_p) and is thought of as the precipitation of graphite that occurs from saturated transition metals.

The existence of an intermediate phase between slowly segregating carbon atoms (state A) and the graphite precipitate (state C) is explained by a higher

binding energy of a monolayer of carbon atoms on the Ni(111) surface with respect to that of the graphite precipitate (0.06 eV). This higher binding energy also explains why the formation of the monolayer occurs at a temperature above the precipitation temperature (100 K).

The heat of segregation can be estimated by equating the chemical potential of carbon atoms in solution to the chemical potential of the monolayer at T_s :

$$\mu_{sol}(T_s) = \bar{G}(T_s) + kT_s \ln \chi = \mu_{mono} \quad (7.7)$$

and to the chemical potential of graphite at T_p :

$$\mu_{sol}(T_p) = \bar{G}(T_p) + kT_p \ln \chi = \mu_{graphite} \quad (7.8)$$

where G is the partial atomic free energy of solution and χ is the fraction of available interstitial sites occupied by carbon atoms in the bulk. The chemical potential of graphite is the reference point and set to zero. The free energy of solution can be expanded to its enthalpy and entropy terms as found in reference [47]:

$$G(T) = H_{sol} + TS_{sol} = 0.49\text{eV} + 0.2kT \quad (7.9)$$

With this and (7.8), the carbon solubility is obtained:

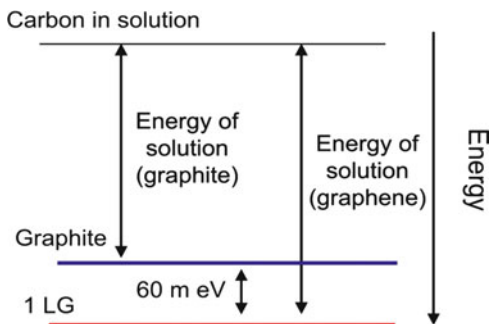
$$\ln \chi = -0.2 - \frac{0.49}{kT_p} \quad (7.10)$$

To obtain the relationship between T_s and carbon concentration, (7.7) and (7.9) are used:

$$\ln \chi = \frac{(\bar{H}_{mono} - \bar{H}_{sol})}{kT_s} - \frac{(\bar{S}_{mono} - \bar{S}_{sol})}{k} = \frac{\Delta \bar{H}_{seg}}{kT_s} - \frac{\Delta \bar{S}_{seg}}{k} \quad (7.11)$$

where H_{seg} and S_{seg} are the enthalpy and entropy of segregation, respectively. By fitting the experimental values of T_s , Blakely et al. obtained a value of 0.55 eV for $\Delta \bar{H}_{seg}$. The binding energy per carbon atom for the monolayer on the Ni(111) surface is 0.55 eV. For the graphite phase it was found to be 0.49 eV. Figure 7.27 shows an energy diagram describing the observations. The observation that a monolayer of graphene can exist at thermodynamic equilibrium independently from the graphitic (multilayer) phase opens the possibility of growing uniform SLG graphene over Ni(111) by segregation of carbon. However, this would require the elimination of multilayer phase nucleation by methods such as rapid cooling.

Fig. 7.27 Single atom energy diagram for carbon in Ni(111). The diagram shows binding energies for the monolayer and graphite phase during carbon segregation to a Ni(111) surface



7.5.3 Summary of the Effects of Process Parameters on the Growth of Graphene

There are numerous parameters that affect the quality of graphene grown by CVD methods. These include the type of metal used, its structure and CVD process parameters. The critical parameters in a CVD process may depend on the mechanism by which graphene grows which in turns depends on the type of metal used and its carbon solubility at the operating temperature. For example, for the direct surface deposition mechanism, parameters such as hydrocarbon concentration and pressure could have a larger effect than cooling rate (vice versa for the carbon dissolution-segregation mechanism). Table 7.1 gives a summary of key process parameters and their effect on graphene quality. A better understanding of the growth mechanism will improve graphene quality and allow greater control on the type of graphene films grown.

7.6 Catalyst-Free and Low Temperature Growth of Graphene

CVD of graphene on metallic substrates requires post-fabrication transfer and is usually carried out at temperatures which are incompatible with silicon technology. The direct growth of graphene without a catalyst is advantageous for graphene device fabrication. Low temperature growth of graphene permits deposition of graphene over surfaces that cannot withstand temperatures as high as 900–1,000°C.

Graphene can be grown directly on the surface of various substrates such as insulators, semiconductors and metals without the need for a catalytic substrate [50–53]. Plasma-enhanced CVD (PECVD) is used to grow nanographene films at temperatures as low as 550°C, using methane as a precursor [50]. The plasma produces radical species such as CH_x , C_2H_y and C_3H_z that play an important role in the formation of graphene islands. The islands produced have a size of around 10 nm in lateral size. The surface is covered by isolated graphene islands, for short

Table 7.1 Process parameters and their effect on graphene quality

Parameter	Domain size	Thickness uniformity	Defect density
Temperature	Larger domain size with increased temperature [34, 48]	–	Lower defect density with increased temperature [49]
Hydrocarbon pressure	Smaller domain size with pressure [34]	Decreased uniformity with pressure [35]	Higher defect density with pressure [35]
Hydrocarbon flow rate	Smaller domain size with flow rate [34]	Decreased uniformity with flow rate [35]	Higher defect density with flow rate [35]
Cooling rate	–	Improved thickness uniformity with lower cooling rates [15]	Lower defect density with lower cooling rates [9]
Metal carbon solubility	–	Improved thickness uniformity with lower carbon solubility [42]	–
Metal crystallinity	Graphene domains can grow continuously over grain boundaries [12]. The role of the substrate crystallinity is still unclear	Improved thickness uniformity with single crystal substrates [43]	–
Type of metal	Ru and Cu have shown the largest graphene domains (100–200 μm and ~ 400 μm , respectively) [7, 42]	Ru and Cu show better thickness uniformity over others [12, 13, 42] at more CVD conditions	–

exposure times; however, for longer plasma exposure, graphene islands populate the entire surface until they form a continuous graphene film [50]. Graphene grows directly on MgO substrates without the need for plasma enhancement [51]. The temperature required for graphene growth can be modified by the hydrocarbon precursor used. Whereas cyclohexane requires a temperature of 875°C, acetylene requires only 325°C to grow graphene [51].

Catalyst free processes with microwave-assisted plasma and radio-frequency assisted plasma produce graphene films that consist of “petal-like” graphene sheets standing vertically with respect to the surface [52, 53]. These films are produced in a variety of substrates such as Si, W, Mo, Zr, Ti, Hf, Nb, Ta, Cr, SiO₂, Al₂O₃ and stainless steel [53]. Applications of these films include electrodes for biosensing and field emitters. The use of these films as field emitters is attractive because of their low turn-on field (4.7 V/ μm) and the fact that the edge of a free standing graphene sheet may be more stable compared to the tip of free standing nanotubes.

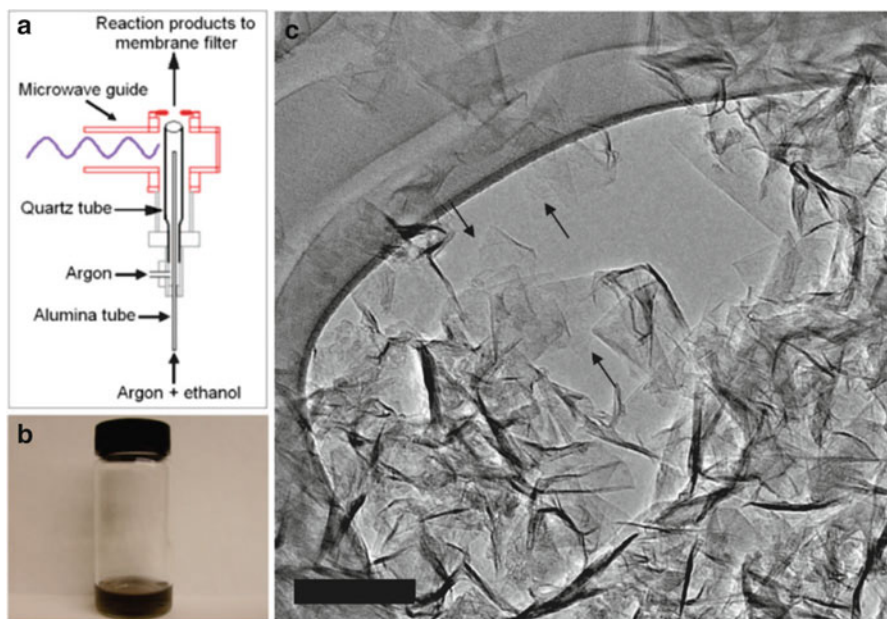


Fig. 7.28 (a) The plasma-assisted set up used to produce graphene in the gas phase. (b) A TEM image of the resulting material. (c) A methanol-based dispersion of the graphene flakes (Reproduced with permission from [54]. © 2008 American Chemical Society)

7.7 Substrate Free Gas-Phase Approaches

The CVD methods so far involved the planar deposition of graphene over a substrate. There are other CVD methods that do not need a substrate and the final product is a conglomeration of graphene sheets which can be processed to obtain a liquid suspension of graphene sheets. These forms of graphene find use in applications in which room temperature deposition is required. The deposition processes include spraying or drop casting of a graphene liquid suspension.

An example of a substrate-free fabrication process involves the use of an atmospheric microwave (2.45 GHz) Ar plasma, such as that shown in Fig. 7.28a [54]. A quartz tube (21 mm internal diameter) situated inside the reactor is used to flow Ar. A smaller alumina tube (3 mm internal diameter) is placed concentrically within the quartz tube and it is used to deliver an aerosol consisting of Ar and ethanol droplets directly into the plasma. During their time inside the plasma, these droplets rapidly evaporate and dissociate to form solid matter. After going through the plasma chamber, these products cool down and are collected downstream on nylon membrane filters. The rate of material collection on the filters is about 2 mg min^{-1} for a mass input of carbon in the ethanol of 164 mg min^{-1} . These graphene sheets collected on the filters can be sonicated in methanol for 5 min. The sheets were found to form a homogeneous black suspension of the material

(Fig. 7.28b). Figure 7.28c shows a TEM image of the material after depositing a drop of the methanol suspension on a TEM lacey carbon grid.

A second example consists of the decomposition of hydrocarbons over supported catalysts such as Co particles on magnesium oxide [55]. In this method, the catalyst is prepared by immersing powdered MgO (5 g) in a solution of cobalt nitrate hexahydrate ($\text{Co}(\text{NO}_3)_2 \cdot 6\text{H}_2\text{O}$, 98%, 0.36 g) dissolved in 100 mL of ethanol, under sonication for 1 h. After being dried, the solid is heated at 130°C for 12 h and ground into a fine powder. This powder is placed inside a CVD reactor in a ceramic boat and a mixture of CH_4 and Ar gas is passed over it at 1,000°C for 30 min. The support and catalyst are etched away in a solution of HCl and then the final product is rinsed with water and dried at 70°C. For this method, 50 mg of FLG material is obtained from 500 mg of the Co/MgO catalyst. HRTEM images of the final material show that most of the graphene sheets are sutured together to form a large crumpled paper.

These gas-phase, substrate free methods are another way to pursue the large scale, low cost synthesis of graphitic materials. These methods are especially suitable when graphene needs to be incorporated into a material in a non-planar way, such as polymer composites.

7.8 Concluding Remarks

The growth of graphene films over large areas on transition metals (such as Ru, Cu and Ni) is possible with CVD processes. Graphene films can grow over these metals by two possible mechanisms. One involves the dissolution of carbon inside the bulk of the metal substrate and the growth of graphene is initiated by the cooling and supersaturation of the metal substrate. The second mechanism involves direct deposition of graphene over the metal substrate. Here, carbon produced by the catalytic decomposition of hydrocarbons on the metal surface diffuses only on the surface until graphene growth occurs.

Transfer processes allow the fabrication of graphene based devices on other substrates such as SiO_2 , PDMS and PET. Applications enabled by these transfer processes include graphene FETs and touch screens with graphene as the transparent electrode. Key parameters affecting graphene properties depend on the type of growth mechanism involved as well as growth conditions.

References

1. J. Wintterlin and M. L. Bocquet. Graphene on metal surfaces. *Surface Science*, 603 (10–12):1841–1852, 2009.
2. A. E. B. Presland and P. L. Walker. Growth of single-crystal graphite by pyrolysis of acetylene over metals. *Carbon*, 7(1):1–4, 1969.
3. Alexander E. Karu and Michael Beer. Pyrolytic formation of highly crystalline graphite films. *Journal of Applied Physics*, 37(5):2179–2181, 1966.

4. P. E. I. Ching Li. Preparation of single-crystal graphite from melts. *Nature*, 192 (4805):864–865, 1961.
5. I. Minko and I. Einbinder. Dendritic growth of graphite from melts. *Nature*, 194 (4830):765–766, 1962.
6. S. B. Austerman, S. M. Myron, and J. W. Wagner. Growth and characterization of graphite single crystals. *Carbon*, 5(6), 1967.
7. Peter W. Sutter, Jan-Ingo Flege, and Eli A. Sutter. Epitaxial Graphene on Ruthenium. *Nat Mater*, 7(5):406–411, 2008.
8. Keun Soo Kim, Yue Zhao, Houk Jang, Sang Yoon Lee, Jong Min Kim, KS Kim, Jong Ahn, Philip Kim, Jae Choi, Byung Hee Hong. Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature*, 457(7230):706–710, 2009.
9. Qingkai Yu, Jie Lian, Sujitra Siriponglert, Hao Li, Yong P. Chen, and Shin-Shem Pei. Graphene segregated on Ni surfaces and transferred to insulators. *Applied Physics Letters*, 93(11):113103–3, 2008.
10. L. G. De Arco, Zhang Yi, A. Kumar, and Zhou Chongwu. Synthesis, transfer, and devices of single- and few-layer graphene by chemical vapor deposition. *Nanotechnology*, IEEE Transactions on, 8(2):135–138, 2009.
11. Alfonso Reina, Xiaoting Jia, John Ho, Daniel Nezich, Hyungbin Son, Vladimir Bulovic, Mildred S. Dresselhaus, and Jing Kong. Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition. *Nano Letters*, 9(1):30–35, 2009.
12. E. Sutter, P. Albrecht, and P. Sutter. Graphene growth on polycrystalline Ru thin films. *Applied Physics Letters*, 95(13):133109, 2009.
13. P. W. Sutter, P. M. Albrecht, and E. A. Sutter. Graphene growth on epitaxial Ru thin films on sapphire. *Applied Physics Letters*, 97(21):213101, 2010.
14. S. D. Robertson. Carbon Formation from Methane Pyrolysis over some Transition Metal surfaces-II. Manner of carbon and graphite formation. *Carbon*, 10(2):221–229, 1972.
15. Alfonso Reina, Stefan Thiele, Xiaoting Jia, Sreekar Bhaviripudi, Mildred Dresselhaus, Juergen Schaefer, and Jing Kong. Growth of large-area single- and bi-layer graphene by controlled carbon precipitation on polycrystalline Ni surfaces. *Nano Research*, 2(6): 509–516, 2009.
16. Stefan Thiele, Alfonso Reina, Paul Healey, Jakub Kedzierski, Peter Wyatt, Pei-Lan Hsu, Craig Keast, Juergen Schaefer, and Jing Kong. Engineering polycrystalline Ni films to improve thickness uniformity of the chemical-vapor-deposition-grown graphene films. *Nanotechnology*, 21(1):015601, 2009.
17. B. C. Banerjee, T. J. Hirt, and P. L. Walker. Pyrolytic carbon formation from carbon suboxide. *Nature*, 192(4801):450–451, 1961.
18. A. R. Ubbelohde, D. A. Young, and A. W. Moore. Annealing of pyrolytic graphite under pressure. *Nature*, 198(4886):1192–1193, 1963.
19. F. J. Derbyshire, A. E. B. Presland, and D. L. Trimm. The formation of graphite films by precipitation of carbon from nickel foils. *Carbon*, 10(1):114, 1972.
20. F. J. Derbyshire, A. E. B. Presland, and D. L. Trimm. Graphite formation by the dissolution-precipitation of carbon in cobalt, nickel and iron. *Carbon*, 13(2):111–113, 1975.
21. Masako Yudasaka, Rie Kikuchi, Takeo Matsui, Yoshimasa Ohki, Mark Baxendale, Susumu Yoshimura, and Etsuro Ota. Graphite formation on Ni film by chemical vapor deposition. *Thin Solid Films*, 280(1–2):117–123, 1996.
22. Yudasaka Masako, Kikuchi Rie, Ohki Yoshimasa, and Yoshimura Susumu. Graphite growth influenced by crystallographic faces of Ni films. *Journal of Vacuum Science and Technology A: Vacuum, Surfaces, and Films*, 16(4):2463–2465, 1998.
23. A. N. Obraztsov, E. A. Obraztsova, A. V. Tyurmina, and A. A. Zolotukhin. Chemical vapor deposition of thin graphite films of nanometer thickness. *Carbon*, 45(10):2017–2021, 2007.
24. M. Yudasaka, R. Kikuchi, T. Matsui, H. Kamo, Y. Ohki, S. Yoshimura, and E. Ota. Graphite thin film formation by chemical vapor deposition. *Applied Physics Letters*, 64(7):842–844, 1994.
25. A. Nagashima, N. Tejima, and C. Oshima. Electronic states of the pristine and alkali-metal-intercalated monolayer graphite/Ni(111) systems. *Physical Review B*, 50(23):17487, 1994.

26. Y. Gamo, A. Nagashima, M. Wakabayashi, M. Terai, and C. Oshima. Atomic structure of monolayer graphite formed on Ni(111). *Surface Science*, 374(1–3):61–64, 1997.
27. D. Farias, A. M. Shikin, K. H. Rieder, and S. Dedkov Yu. Synthesis of a weakly bonded graphite monolayer on Ni(111) by intercalation of silver. *Journal of Physics: Condensed Matter*, (43):8453, 1999.
28. Elena Loginova, Norman C. Bartelt, Peter J. Feibelman, and Kevin F. McCarty. Evidence for graphene growth by c cluster attachment. *New Journal of Physics*, 10(9):093026, 2008.
29. Xuesong Li, Weiwei Cai, Jinho An, Seyoung Kom, Junghyo Na, Dongxing Yang, Richard Piner, Aruna Velamakanni, Inhwa Jung, Emanuel Tutuc, Sanjay K. Banerjee, Luigi Colombo, and Rodney S. Ruoff. Large-Area synthesis of high-quality and uniform graphene films on Copper foils. *Science* 324 (5932): 1312–1314, 2009.
30. Xuesong Li, Weiwei Cai, Luigi Colombo, and Rodney S. Ruoff. Evolution of graphene growth on Ni and Cu by carbon isotope labeling. *Nano Letters*, 9(12):4268–4272, 2009.
31. Liying Jiao, Ben Fan, Xiaojun Xian, Zhongyun Wu, Jin Zhang, and Zhongfan Liu. Creation of nanostructures with poly(methyl methacrylate)-mediated nano-otransfer printing. *Journal of the American Chemical Society*, 130(38):12612–12613, 2008.
32. Sukang Bae, Hyeongkeun Kim, Youngbin Lee, Xiangfan Xu, Jae-Sung Park, Yi Zheng, Jayakumar Balakrishnan, Tian Lei, Hye Ri Kim, Young Il Song, Young-Jin Kim, Kwang S. Kim, Barbaros Ozyilmaz, Jong-Hyun Ahn, Byung Hee Hong, and Sumio Iijima. Roll-to-roll production of 30-inch graphene films for transparent electrodes. *Nat Nano*, 5(8):574–578, 2010.
33. Mark P. Levendof, Carlos S. Ruiz-Vargas, Shivank Garg, and Jiwoong Park. Transfer-free batch fabrication of single layer graphene transistors. *Nano Letters*, 9(12):4479–4483, 2009.
34. Xuesong Li, Carl W. Magnuson, Archana Venugopal, Jinho An, Ji Won Suk, Boyang Han, Mark Borysiak, Weiwei Cai, Aruna Velamakanni, Yanwu Zhu, Lianfeng Fu, Eric M. Vogel, Edgar Voelkl, Luigi Colombo, and Rodney S. Ruoff. Graphene films with large domain size by a two-step chemical vapor deposition process. *Nano Letters*, 10(11):4328–4334, 2010.
35. Qingkai Yu, Luis A. Jauregui, Wei Wu, Robert Colby, Jifa Tian, Zhihua Su, Helin Cao, Zhihong Liu, Deepak Pandey, Dongguang Wei, Ting Fung Chung, Peng Peng, Nathan P. Guisinger, Eric A. Stach, Jiming Bao, Shin-Shem Pei & Yong P. Chen. Control and characterization of individual grains and grain boundaries in graphene grown by chemical vapour deposition. *Nature Materials*, 10: 443–449. 2011.
36. Sreekar Bhaviripudi, Xiaoting Jia, Mildred S. Dresselhaus, and Jing Kong. Role of kinetic factors in chemical vapor deposition synthesis of uniform large area graphene using copper catalyst. *Nano Letters*, 10(10):4128–4133, 2010.
37. Melinda Y. Han, Barbaros Ozyilmaz, Yuanbo Zhang, and Philip Kim. Energy band-gap engineering of graphene nanoribbons. *Physical Review Letters*, 98(20):206805, 2007.
38. Yu-Ming Lin, Vasili Perebeinos, Zhihong Chen, and Phaedon Avouris. Electrical observation of subband formation in graphene nanoribbons. *Physical Review B*, 78(16):161409, 2008.
39. S. Y. Zhou, G. H. Gweon, A. V. Fedorov, P. N. First, W. A. de Heer, D. H. Lee, F. Guinea, A. H. Castro Neto, and A. Lanzara. Substrate-induced bandgap opening in epitaxial graphene. *Nat Mater*, 6(10):770–775, 2007.
40. Yuanbo Zhang, Tsung-Ta Tang, Caglar Girit, Zhao Hao, Michael C. Martin, Alex Zettl, Michael F. Crommie, Y. Ron Shen, and Feng Wang. Direct observation of a widely tunable bandgap in bilayer graphene. *Nature*, 459(7248):820–823, 2009.
41. Seunghyun Lee, Kyunghoon Lee, and Zhaohui Zhong. Wafer scale homogeneous bilayer graphene films by chemical vapor deposition. *Nano Letters*, 10(11):4702–4707, 2010.
42. Xuesong Li, Weiwei Cai, Jinho An, Seyoung Kim, Junghyo Nah, Dongxing Yang, Richard Piner, Aruna Velamakanni, Inhwa Jung, Emanuel Tutuc, Sanjay K. Banerjee, Luigi Colombo, and Rodney S. Ruoff. Large-area synthesis of high-quality and uniform graphene films on copper foils. *Science*, 324(5932):1312–1314, 2009.
43. Takayuki Iwasaki, Hye Jin Park, Mitsuharu Konuma, Dong Su Lee, Jurgen H. Smet, and Ulrich Starke. Long-range ordered single-crystal graphene on high-quality heteroepitaxial Ni thin films grown on MgO(111). *Nano Letters* 11 (1): 79–84, 2011.

44. Kongara M. Reddy, Andrew D. Gledhill, Chun-Hu Chen, Julie M. Drexler, and Nitin P. Padture. High quality, transferable graphene grown on single crystal Cu(111) thin films on basal-plane sapphire. *Applied Physics Letters* 98: 113117, 2011.
45. Li Gao, Je rey R. Guest, and Nathan P. Guisinger. Epitaxial graphene on Cu(111). *Nano Letters*, 10(9):3512–3516, 2010.
46. M. Eizenberg and J. M. Blakely. Carbon monolayer phase condensation on Ni (111). *Surface Science*, 82: 228–236, 1979.
47. W.W. Dunn, R.B. McLellan, and W.A. Oates. Segregation isosteres for carbon at the (100) surface of nickel. *Trans. AIME*, 242:2129, 1968.
48. Archana Venugopal-Eric M. Vogel Rodney S. Ruo Luigi Colombo Xuesong Li, Carl W. Magnuson. Large domain graphene. *arXiv:1010.3903v1*, 2010.
49. Chae Seung Jin, Gne Fethullah, scedil, Kim Ki Kang, Kim Eun Sung, Han Gang Hee, Kim Soo Min, Shin Hyeon-Jin, Yoon Seon-Mi, Choi Jae-Young, Park Min Ho, Yang Cheol Woong, Pribat Didier, and Lee Young Hee. Synthesis of large-area graphene layers on poly-Nickel substrate by chemical vapor deposition: Wrinkle formation. *Advanced Materials*, 21 (22):2328–2333, 2009.
50. Lianchang Zhang, Zhiwen Shi, Yi Wang, Rong Yang, Dongxia Shi, and Guangyu Zhang. Catalyst-free growth of nanographene films on various substrates. *Nano Research* 4(3): 315–321, 2011.
51. Mark H. Rummeli, Alicja Bachmatiuk, Andrew Scott, Felix Bornert, Jamie H. Warner, Volker Ho man, Jarrn-Hornng Lin, Gianauelio Cuniberti, and Bernd Buchner. Direct low-temperature nanographene CVD synthesis over a dielectric insulator. *ACS Nano*, 4(7): 4206–4210, 2010.
52. Nai Gui Shang, Pagona Papakonstantinou, Martin McMullan, Ming Chu, Artemis Stamboulis, Alessandro Potenza, Sarnjeet S. Dhesi, and Helder Marchetto. Catalyst-free efficient growth, orientation and biosensing proper-ties of multilayer graphene nano flake films with sharp edge planes. *Advanced Functional Materials*, 18(21):3506–3514, 2008.
53. J. J. Wang, M. Y. Zhu, R. A. Outlaw, X. Zhao, D. M. Manos, B. C. Holloway, and V. P. Mammana. Free-standing subnanometer graphite sheets. *Applied Physics Letters*, 85(7):1265–1267, 2004.
54. Albert Dato, Velimir Radmilovic, Zonghoon Lee, Jonathan Phillips, and Michael Frenklach. Substrate-free gas-phase synthesis of graphene sheets. *Nano Letters*, 8(7):2012–2016, 2008.
55. Xianbao Wang, Haijun You, Fangming Liu, Mingjian Li, Li Wan, Shaoqing Li, Qin Li, Yang Xu, Rong Tian, Ziyong Yu, Dong Xiang, and Jing Cheng. Large-scale synthesis of few-layered graphene using CVD. *Chemical Vapor Deposition*, 15(1–3):53–56, 2009.

Chapter 8

Chemical Approaches to Produce Graphene Oxide and Related Materials

Alexander Sinitskii and James M. Tour

The “physical” separation of graphite layers with adhesive tape was a novel approach that spawned a flurry of activity [1–8] but the chemical separation of graphite layers has been known for decades. The chapter starts off with a historical perspective of chemical exfoliation. The following topics are then discussed in detail: the morphology of chemically converted graphene (CCG) and graphene oxide (GO); models and supporting experiments that provide insight into the structural properties of GO; electrical characterization of CCG and GO; improvements made in CCG formation and functionalization of CCG; and, obtaining graphene ribbons from carbon nanotubes (CNTs).

8.1 Introduction

The first known example of chemical exfoliation of graphite dates back to 1859 when B.C. Brodie treated flakes of natural graphite with potassium chlorate (KClO_3) and fuming nitric acid (HNO_3) [9]. The reaction was typically performed at 60°C for 3–4 days, the product was washed by water to remove acid and salts, and then the entire procedure was repeated several times until no further change was observed. Brodie managed to isolate crystals of the material that were “extremely thin and perfectly transparent”. As for the chemical composition, Brodie found that the resulting material consisted of carbon, oxygen and hydrogen, which explained the increase in the total mass from the starting flakes of graphite. For decades this

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material was known as “*graphic acid*” (Brodie’s term) or “*graphitic acid*”, since it was dispersible in neutral and basic media, but not in acids; although now it is typically named “*graphite oxide*”. Graphite oxide (GO) preserves the layered structure of the starting graphite, but the layers are heavily oxidized, bearing numerous oxygen-containing functional groups. As was demonstrated later, these layers can be relatively easily separated in water or other polar solvents by mild sonication or stirring, resulting in a solution of *graphene oxide* (GO), where the majority of the flakes are either monolayers or few-layer stacks.

Graphite/graphene oxide has rather strong oxidizing properties and can be reduced by treatment with hydrazine [10], hydroxylamine [11], sodium borohydride [12], sodium hydride [13] and other reducing agents. Alternatively, GO can be reduced by high temperature annealing in vacuum or a reducing atmosphere (Ar/H_2) [14], at room temperature by photothermal heating induced by a flash light [15] or by a solvothermal approach [16]. Recent studies suggest that some bacteria could also reduce GO under certain conditions [17]. These reduction approaches remove the majority of the oxygen-containing functional groups from the flakes of graphite/graphene oxide, and the resulting product is often termed “*chemically converted graphene*” (CCG).

Later researchers attempted to modify Brodie’s approach or develop other procedures to oxidize graphite. In the late 1890s, Staudenmaier modified Brodie’s method by using sulfuric acid in addition to KClO_3 and HNO_3 , and adding potassium chlorate to the reaction mixture in multiple aliquots rather than in a single addition [18]. An alternative approach to produce graphite oxide was proposed by Hummers and Offeman in 1958 [19]. They pointed out that Brodie’s and Staudenmaier’s approaches are time consuming and hazardous, since the reaction takes several days and chlorine dioxide, which is toxic and explosive, evolves during the process. They suggested that the synthesis of graphite oxide can be accomplished by treating graphite with a mixture of concentrated sulfuric acid, sodium nitrate (NaNO_3) and potassium permanganate (KMnO_4). This reaction is much faster, since it takes only a few hours for completion, and no explosive gases evolve (although nitrogen oxides are toxic). Thus, a significant degree of caution should be taken when using any of three approaches (Brodie’s, Staudenmaier’s or Hummers’) that to date remain the most common preparation techniques (although with some modifications) for making graphite and graphene oxides.

8.2 Morphology of CCG and GO

The first attempts to observe the individual flakes of graphite/graphene oxide were made using optical microscopy [9]. However, with the development of microscopy techniques it became clear that the flakes of graphene oxide and CCG are indeed extremely thin, with a thickness as small as one atomic layer. The first transmission electron microscopy (TEM) images were reported in the work by Boehm et al. in 1962 [20], where graphite oxide produced by Hummers’ method and its reduction product (CCG) were analyzed (Fig. 8.1). Some flakes are so thin that they are barely visible in contrast to the substrate (thin polymer film). By processing the data,

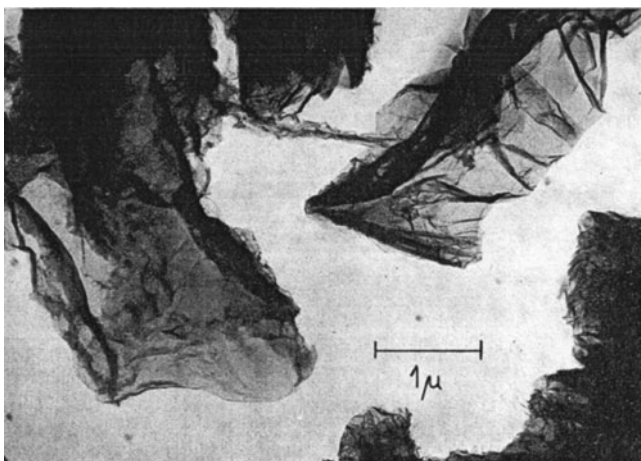


Fig. 8.1 TEM image of CCG flakes obtained by hydrazine reduction of GO produced by Hummers' method (Adapted from [20])

Boehm et al. found that for the thinnest parts the average thickness was ~ 4.6 Å, suggesting that these parts were monolayers.

Mono- and few-layer thick flakes of graphene oxide can be imaged by not only TEM but other techniques such as scanning electron microscopy (SEM) and atomic force microscopy (AFM). Figure 8.2a shows a large GO flake on a Si/SiO₂ substrate. Although it is hard to determine the thickness of GO flakes by looking at such images, the SEM contrast usually serves as a fairly good indication whether it is a thin (mono- or few-layer) or thick flake. In Fig. 8.2a, the difference between the areas where the numbers of layers are doubled and tripled due to the folds is obvious. This brightness contrast is especially useful when it is necessary to compare the thickness of different flakes. Figure 8.2b shows numerous GO flakes on a Si/SiO₂ substrate, and it is clear that some flakes are thicker than the others. AFM is a characterization technique that is used to determine the precise thicknesses of GO flakes and thus confirm the complete exfoliation of sheets, as the heights of monolayer GO flakes are reported in the range of 0.6–1.1 nm [22–26]. Figure 8.2c shows a typical AFM image of a small monolayer GO flake on Si/SiO₂ substrate; the thickness of this flake is about 1 nm (Figure 8.2d).

When GO flakes are deposited on a substrate, they exhibit nanoscopic corrugation that is mostly caused by the roughness of the substrate [27]. Extremely flat flakes of GO can be achieved if placed on top of an atomically flat substrate because intrinsic ripples and the corrugation induced by different functional groups can be strongly suppressed by the interfacial van der Waals interactions of graphene with the substrate. To demonstrate this effect, GO flakes were deposited on substrates with different roughnesses [27]: “rough” Si/SiO₂ (chemically etched substrate; root mean square (rms) roughness ~ 0.5 nm), smoother Si/SiO₂ (rms roughness ~ 0.3 nm) and freshly cleaved mica. The thickness of the flakes was about 1 nm, indicating that they are monolayers. AFM imaging clearly shows that the corrugation of GO flakes strongly correlates to the roughness of the substrate. The average roughness of the

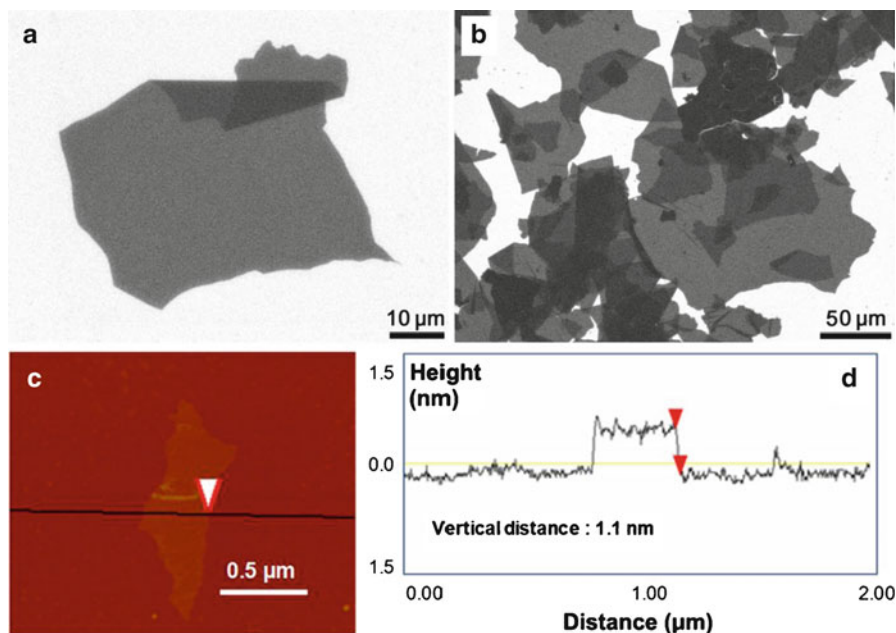


Fig. 8.2 (a, b) SEM and (c) AFM images of graphene oxide flakes on Si/SiO₂ substrates. Panel (d) shows a height profile along the line in (c) (Reproduced with permission from [21]. © 2010 American Chemical Society)

flakes on the “rough” Si/SiO₂ had an rms of ~ 0.38 nm, on the smoother Si/SiO₂ the rms was ~ 0.3 nm and for the flakes on mica an extremely low rms of ~ 0.07 nm was measured. This indicates that substrate roughness is a key factor in the corrugation of graphene materials, whereas other factors have smaller impact.

Graphite oxide is a layered structure that consists of stacked sheets of GO. These layers are heavily functionalized with oxygen-containing functional groups and therefore strongly hydrophilic, enabling intercalation of water molecules between the layers [28]. As a result, the interlayer distance between sheets of GO increases from 6 to 12 Å with increasing humidity [28].

8.2.1 Structure of GO

To date, the exact structure of GO remains unknown despite more than a century of thorough investigation. The complexity of GO and the strong dependence of its composition and properties on the starting material, preparation technique and experimental conditions make understanding of the structure of GO quite complicated. Furthermore, only recent progress in TEM analysis made possible the direct visualization of the GO structure [29, 30], whereas all previous conclusions were largely drawn from indirect analytical techniques.

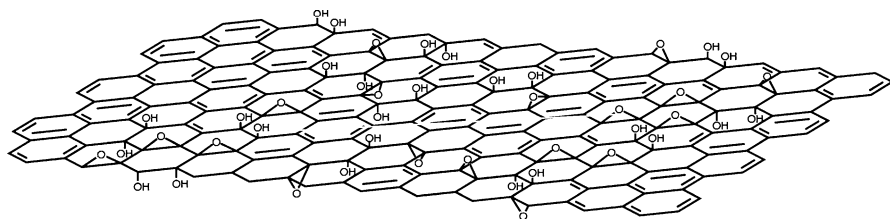


Fig. 8.3 Chemical structure of graphite oxide. For clarity, minor functional groups, carboxylic groups and carbonyl groups have been omitted at the edges (Reproduced with permission from [32]. © 1998 Elsevier)

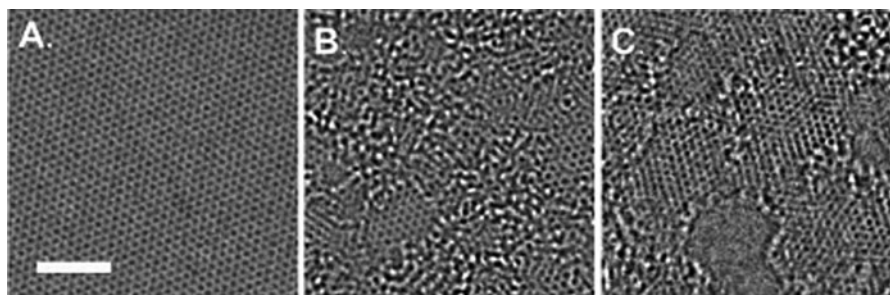


Fig. 8.4 Aberration corrected TEM images of the following suspended monolayer materials: (a) Graphene, (b) GO, and (c) CCG. The scale bar is 2 nm; all panels in this figure have the same magnification (Adapted from [30])

One of the most widely recognized models is the one by Lerf and Klinowski, based on the results of solid-state ^{13}C NMR spectroscopy [31–33]. In this model, GO has an irregular structure with different oxygen-containing functionalities: hydroxyl and epoxy groups bonded to the basal plane and carboxylic or carbonyl groups attached to the edges of the GO (Fig. 8.3). A comprehensive review of other proposed models of GO has been published [34].

Arguably, the most direct way of identifying the structure of GO is a high-resolution TEM, and the results of such experiments largely support the structural model of GO proposed by Lerf and Klinowski. Figure 8.4 shows high resolution TEM images of suspended monolayer sheets of graphene, GO, and CCG, respectively, reported by Erickson et al. [30]; it illustrates the structural differences between graphene, GO produced by Hummers' method [19], and CCG, which was produced by reducing GO with hydrazine vapor followed by slow heating to 550°C under flowing N_2 .

In contrast to a nearly defect-free graphene sheet with long-range order (Fig. 8.4a), GO has a highly inhomogeneous structure (Fig. 8.4b). Three major features can be seen in GO sheets: holes, graphitic regions, and disordered regions, indicating areas of high oxidation, with approximate area percentages of 2%, 16%, and 82%, respectively. Holes, usually less than 5 nm^2 , were observed in several TEM studies of GO [29, 30]; they form because of the CO and CO_2 release during the aggressive oxidation and sheet exfoliation [35]. The presence of graphitic

regions (usually 1–6 nm²) indicates incomplete oxidation of the starting graphite material. The disordered oxidized regions of the basal plane form a continuous network throughout the GO sheet. Monolayer CCG (Fig. 8.4c) contains more holes (approximately 5% of the area) compared to GO, which is expected as CO and CO₂ form during annealing [36]. The significant increase in graphitic area, up to approximately 70% of the area, indicates that the reduction of oxygen functionalities results in a substantial restoration of the original *sp*² carbon network lost during the oxidation, although extensive disordered regions are still observed, likely caused by nitrogen and oxygen functionalities which persist even after reduction and annealing [14, 22, 37].

These TEM observations are in a good agreement with the results of theoretical simulations by Boukhvalov and Katsnelson [38]. Based on density functional calculations, it was predicted that incomplete functionalization of GO (75%) is more energetically favorable than complete functionalization (100%). It was also postulated that complete reduction of GO back to graphene is very difficult to achieve, although reduction of GO from 75% to 6.25% (C:O ratio 16:1) coverage is relatively easy. The TEM data (Fig. 8.4) confirms incomplete oxidation in GO and incomplete reduction achieved in CCG.

TEM observations and deductions about the structure of GO were summarized by Erickson et al. as follows: [30] (1) even oxidized GO contains graphitic regions up to 8 nm² in size, (2) Oxidized regions appear in TEM images as being amorphous with no order with regards to oxidation, have minimal *sp*² bonding character, and form a continuous network across the GO sheet, (3) GO sheets contain numerous holes that are usually less than 5 nm² in size, (4) TEM data and simulations suggest that hydroxyls and 1,2-epoxies are the dominant functionalities; carbonyls likely populate the edges of the holes, (5) The *sp*² bonds between carbon atoms within the core of graphitic regions are largely unstrained, (6) No lines of graphitic or oxidized regions or other superstructures within GO sheets were observed.

Given all these considerations, TEM experiments [29, 30] mostly support the structural model of GO proposed by Lerf and Klinowski [31], i.e. GO is amorphous in nature with densely oxidized regions with hydroxyls and 1,2-epoxies as the primary functionalities and carbonyls along the edges [31, 32, 35, 39–41]. However, the sizes of graphitic and oxidized regions are much larger than those proposed by Lerf et al., and this structural model does not take into consideration the presence of a significant number of holes in GO sheets.

The high degree of oxidation of GO is clearly visible in X-ray photoelectron spectroscopy (XPS) data. A typical C1s XPS spectrum of GO (Fig. 8.5a) exhibits four components that correspond to carbon atoms in different functional groups: the C in C–C bonds in aromatic rings, the C in C–O bonds, the C in C=O bonds, and the carboxylate carbon (O–C=O) [22, 42]. The C1s XPS spectrum of the CCG (Fig. 8.5b) exhibits these same oxygen-containing functional groups, but their peak intensities are significantly smaller than those in GO, indicating considerable de-oxygenation by the reduction process. Noteworthy, the CCG obtained by reduction of GO using hydrazine contains a noticeable amount of nitrogen, as the XPS spectrum of this material exhibits an additional component at 285.9 eV corresponding to C bound to nitrogen [22, 42].

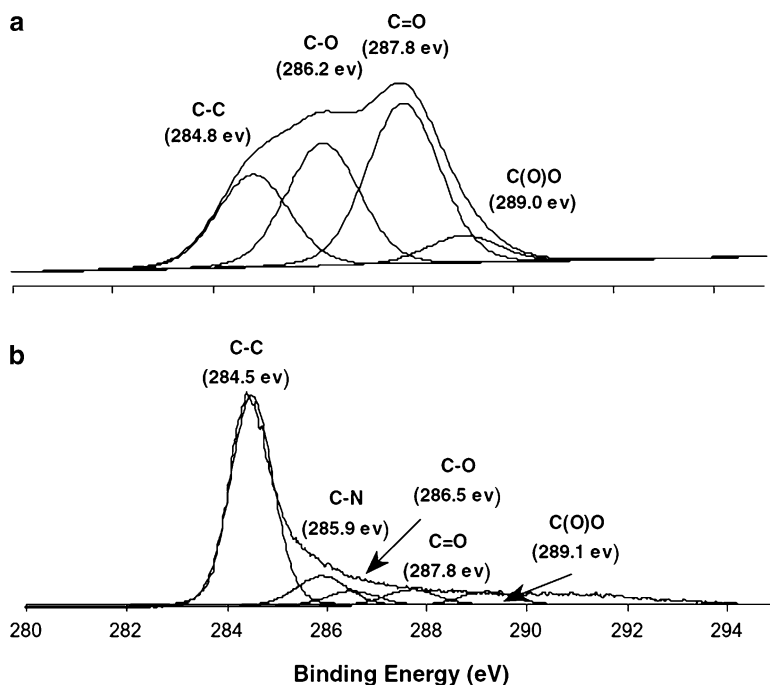


Fig. 8.5 The C1s XPS spectra of: (a) GO, and (b) CCG (Reproduced with permission from [22]. © 2007 Elsevier)

8.3 Electrical Properties of GO and CCG

Since GO is heavily oxidized, it is not electrically conductive. Reduction of GO results in the removal of the majority of the functional groups, increases the size of graphitic regions and as a result, partially restores the conductivity of the material. According to the theoretical study by Boukhvalov and Katsnelson, GO sheets become conducting if their coverage with functional groups does not exceed 25%, otherwise they are insulators [38].

Figure 8.6 shows the electrical properties of a typical electronic device based on CCG that was obtained by reduction of GO using hydrazine [21]. All flakes used in the study exhibited qualitatively the same electrical properties; they behaved as p-type semiconductors in air, but exhibited ambipolar electric field effect in vacuum after desorption of the atmospheric adsorbates that are known to cause doping effects in graphene [43]. This effect is completely reversible; after exposure to air the CCG flakes again behaved as p-type semiconductors [44–46]. Conductivity of hydrazine-reduced CCG flakes was reported to be in the range of 0.05–2 S/cm [24].

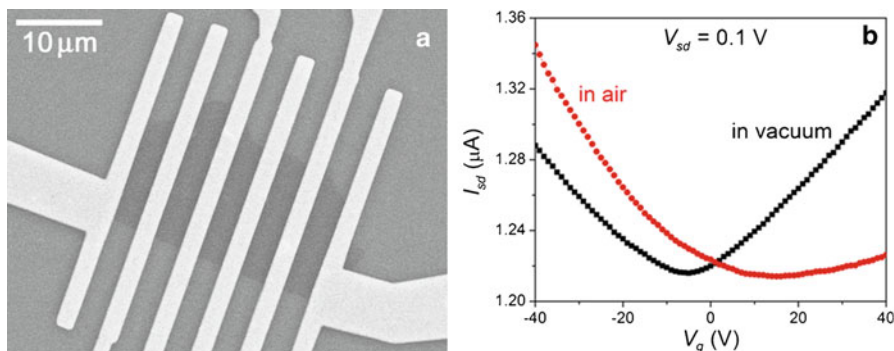


Fig. 8.6 (a) SEM image of a multiterminal electronic device based on a hydrazine-reduced CCG flake. (b) Source-drain current (I_{sd})—gate voltage (V_g) characteristics of the same electronic device based on a few-layer CCG flake measured in air and in vacuum (Reproduced with permission from [21]. © 2010 American Chemical Society)

Figure 8.7a shows a typical temperature dependence of resistance of a CCG flake [24]. Reduced CCG exhibits semiconductor-type behavior, so its resistance increases with decreasing temperature; the resistance increases by more than three orders of magnitude upon cooling from 298 to 4 K, which is different from the behavior of mechanically exfoliated graphene that exhibits little temperature dependence [47–49]. The temperature-dependent data for CCG can be linearized in $\ln(I/A)$ versus $T^{-1/3}$ coordinates, pointing to variable range hopping (VRH) as a relevant charge-transport mechanism [24, 50, 51]. VRH obeys the following general temperature dependence: $I = I_0 \cdot \exp((T_0/T)^{1/n})$, where $(n - 1)$ is the dimensionality of the sample [52]. The two-dimensional (2D) character reflected by the $T^{-1/3}$ -dependence is consistent with the 2D nature of CCG sheets. This behavior has been correlated [24] with results from scanning tunneling microscopy (STM) under ambient conditions. STM images of the GO sheets look quite different from those reported for pristine graphene [53] due to the appearance of bright regions lacking ordered lattice features. Most likely, these regions correspond to the parts of GO sheet with remaining oxygen-containing functional groups, which are also observed in the TEM images that were discussed previously. The “patchy” structure of CCG, where graphitic islands are separated by heavily oxidized regions and holes, is thus responsible for the VRH transport mechanism. In view of the described CCG structure, hopping presumably occurs between the intact graphene regions.

It is interesting to point out that GO/CCG flakes strongly interact with Si/SiO₂ substrates. In the same work [24], electronic devices were fabricated based on selected partially folded sheets that allow simultaneous contacting of a mono- and bilayer configuration, Fig. 8.7c. It was found that the conductivity of bilayer regions reproducibly exceeded those of the first layers by more than a factor of 2, suggesting that the second layer is more conducting than the first one. Statistical analysis over a range of CCG sheets with different number of layers revealed that no further increase in conductivity could be detected for sheets containing between

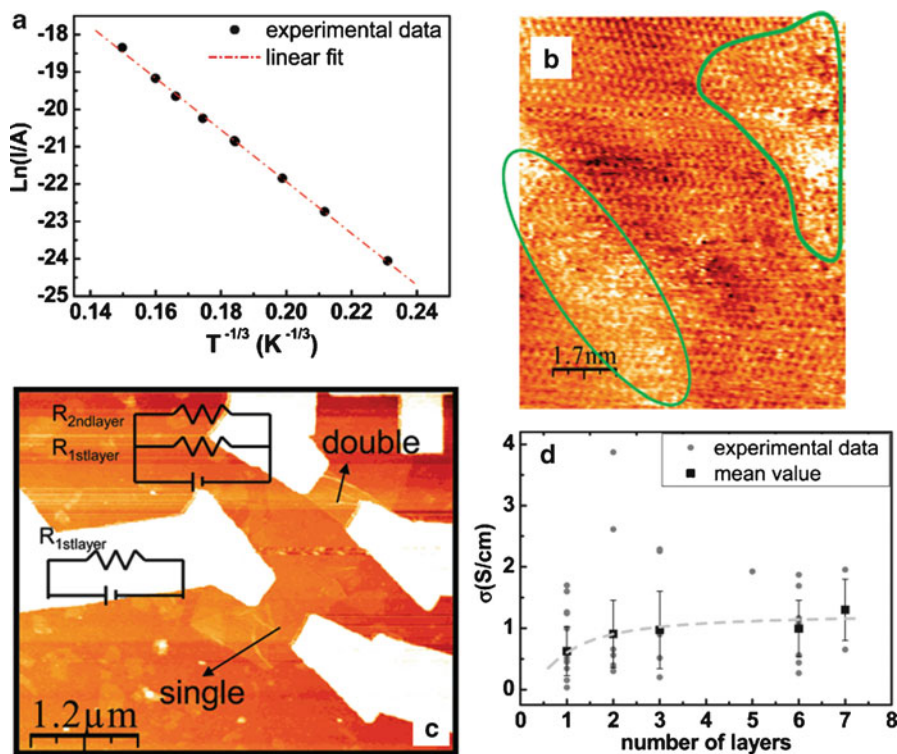


Fig. 8.7 Electronic properties of CCG. (a) Temperature dependence of conductivity of CCG linearized in $\ln(I/A)$ versus $T^{-1/3}$ coordinates ($V_{\text{bias}} = 0.2$ V). (b) STM image of a GO monolayer on a HOPG substrate; contours denote oxidized regions. (c) AFM image of a folded CCG flake where electrical contacts are attached to mono- and bilayer regions. The insets show the simple electronic circuits used for data evaluation. (d) Statistical plot of the mean volume conductivity (measured under ambient conditions) as a function of the number of layers within CCG sheets. The gray dashed line has been drawn as a guide to the eye (Reproduced with permission from [24]. © 2010 American Chemical Society)

three and seven layers, suggesting that only the conductivity of the very bottom layer is suppressed due to interaction with the Si/SiO₂ substrate. There is a similar effect of the SiO₂ substrate on mechanically exfoliated [5–8] graphene and so replacing the substrate with an atomically flat highly crystalline substrate, like hexagonal boron nitride, [54] or suspending graphene [55, 56] dramatically increase the mobility of charge carriers in graphene.

8.3.1 Dispersions of GO

Because of the presence of numerous functional groups, GO sheets are hydrophilic. Therefore, stable colloidal suspensions of GO in water and some organic solvents

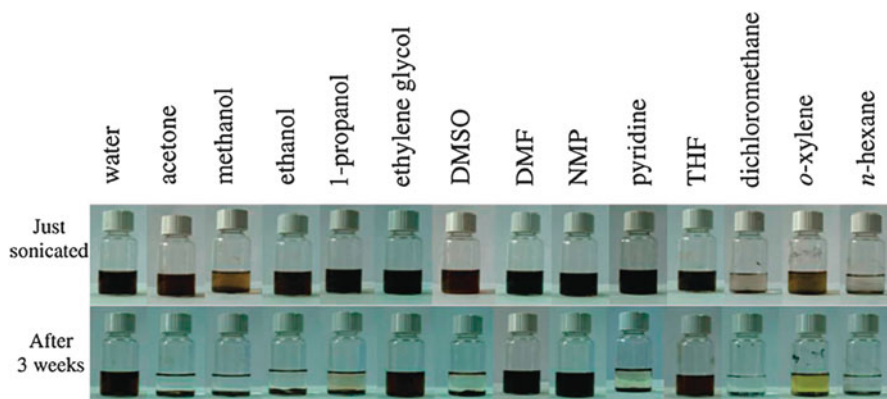


Fig. 8.8 Photographs of dispersions of GO in different solvents captured immediately after 1 h sonication (*top row*) and 3 weeks later (*bottom row*). The color of the o-xylene sample is due to the solvent itself (Reproduced with permission from [58]. © 2008 American Chemical Society)

can be achieved simply by sonication [22, 57, 58]. For instance, GO can be dispersed in water, resulting in brown suspensions. However, sonication has a disadvantage, as it causes substantial damage to GO flakes. Usually, the typical size of GO flakes in stable suspensions is about several 100 nm [22]. Flakes of GO as large as several hundreds of μm (lateral size) are also possible to obtain (see Fig. 8.2a, b) if gentle mechanical stirring is used during the synthesis, although solutions of such large flakes are not stable.

Studies have been performed to identify solvents suitable for forming stable dispersions of GO. One necessary requirement is that the solvent should be considerably polar, since GO sheets are heavily functionalized with polar oxygen-containing functional groups. Correspondingly, the degree of functionalization of GO is another important factor to form stable dispersions. Paredes et al. reported an experiment where GO was dispersed in water and 13 different organic solvents at the same nominal concentration of 0.5 mg/mL by ultrasonication [58]. After allowing to settle down for several weeks, stable dispersions of GO were observed in water and several organic solvents, including N,N-dimethylformamide (DMF), N-methyl-2-pyrrolidone (NMP), tetrahydrofuran (THF), and ethylene glycol (Fig. 8.8). From AFM data, in all of these solvents GO was exfoliated into individual, single-layer flakes, that were from a few 100 nm to a few micrometers in size.

Different stabilizers can also be used to achieve stable dispersions of GO in different solvents. For instance, 1-pyrenebutyrate, a water-soluble pyrene derivative, is efficient for preparing stable aqueous dispersions, since the pyrene moiety is known to have strong affinity with the basal plane of graphite via π -stacking [59].

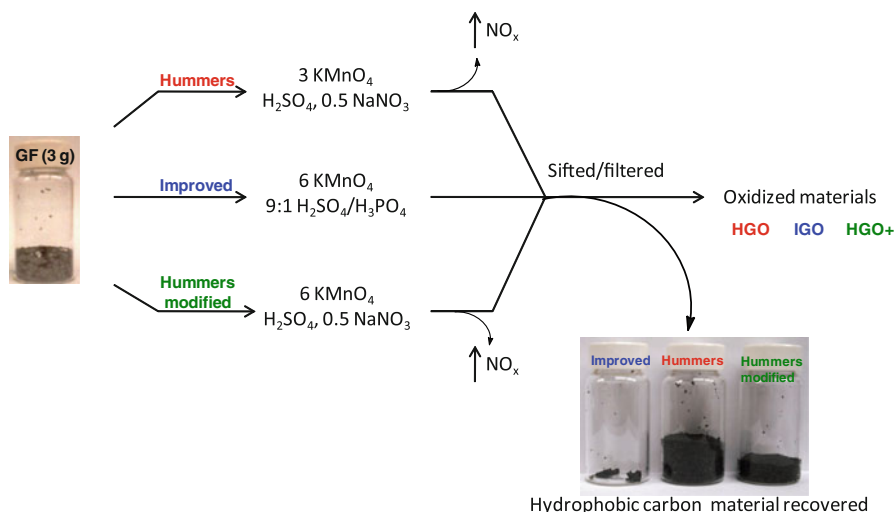


Fig. 8.9 Methods to oxidize graphite flakes (GF) to GO [21]. Under-oxidized hydrophobic carbon materials were recovered during the purification of IGO, HGO, and HGO+. The increased efficiency of the IGO method is indicated by the very small amount of under-oxidized material produced (Reproduced with permission from [21]. © 2010 American Chemical Society)

8.3.2 Improved Methods of Forming GO and soluble graphene

There were several attempts to modify the conventional preparation techniques for GO (Brodie's, Staudenmaier's and Hummers') to yield better properties. Currently, Hummers' method (KMnO₄, NaNO₃, H₂SO₄) is the most common method used for the GO preparation. Luo et al. have reported that large GO flakes with fewer defects can be synthesized by Hummers' method from graphite that was pre-exfoliated by microwave heating [60]. Marcano et al. have demonstrated that excluding the NaNO₃ from the original Hummers' protocol, increasing the amount of KMnO₄ and performing the reaction in a 9:1 mixture of H₂SO₄:H₃PO₄ improves the efficiency of the oxidation process [21]. The role of a second acid, such as H₃PO₄, in the oxidation process is discussed later in this chapter. This improved method (IGO) provides a greater amount of hydrophilic oxidized graphene material as compared to Hummers' method (HGO) or Hummers' method with additional KMnO₄ (HGO+, "modified Hummers' method"), Fig. 8.9. Although IGO is more oxidized than HGO, the IGO can be reduced to a conductive CCG by hydrazine treatment. In contrast to Hummers' method, the improved method does not generate toxic gas and the temperature is easily controlled. The improved synthesis of GO [21] is important for large-scale production of GO and CCG.

Since conventional approaches for making soluble graphenes involve harsh oxidative conditions that result in materials with disrupted *sp*² network and poor conductivity, there were numerous attempts to disperse graphite in different solvents

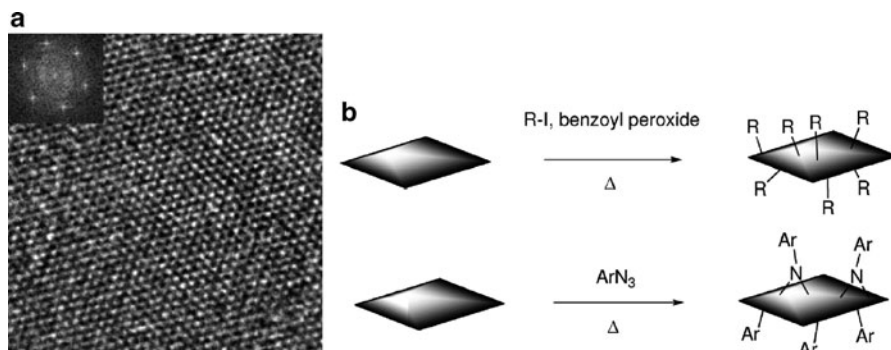


Fig. 8.10 Graphene dispersed in ODCB. (a) TEM image of single layer graphene. (b) Schematics of possible reactions to produce functionalized graphene; R = dodecyl and Ar = phenyl (Reproduced with permission from [63]. © 2009 American Chemical Society)

without oxidation. For instance, the dispersion of graphene has been reported using some polar solvents such as DMF [61] and NMP [62], although the concentrations attainable are low (~ 0.01 mg/mL). Hamilton et al. have demonstrated a method of producing homogeneous dispersions of graphene nanosheets in a non-polar solvent, *ortho*-dichlorobenzene (ODCB), from various graphite materials at concentrations of 0.02–0.03 mg/mL [63]; ODCB was previously known as a common reaction solvent for fullerenes and single-walled carbon nanotubes (SWCNTs), presumably as a result of efficient π – π interaction [64]. TEM studies (Fig. 8.10a) confirm that the graphene flakes in the dispersions are mostly few-layer graphene with the number of layers usually less than five. The advantage of this method lies in its high yield, simplicity, and its avoidance of harsh oxidation chemistry. These ODCB dispersions were also used to covalently functionalize graphene (Fig. 8.10b). Thermal decomposition of benzoyl peroxide was used to initiate the radical addition of alkyl iodides to graphene in ODCB dispersions. Alternatively, ODCB-dispersed graphene may be readily functionalized with nitrenes generated by thermal decomposition of aryl azides (Fig. 8.10b).

Dispersions of graphene flakes in different polar solvents, such as alkaline water solutions, DMF and DMSO, can be prepared from thermally expanded graphite (TEG) using 7,7,8,8-tetracyanoquinodimethane (TCNQ) anions as a stabilizer [65]. TCNQ exhibits a strong π – π stacking interaction with aromatic systems, so that TCNQ anions adsorbed on the surface of graphene effectively repel individual graphene sheets from each other, forming a homogenous suspension.

Another promising solvent for non-oxidized graphene flakes is chlorosulfonic acid (HSO_3Cl), which was previously demonstrated to be a good solvent for SWCNTs as well [66]. Behabtu et al. have demonstrated that graphite spontaneously exfoliates into single-layer graphene in chlorosulfonic acid, and dissolves at isotropic concentrations as high as ~ 2 mg/mL [67]. This occurs without the need for

covalent functionalization, surfactant stabilization, or sonication, which can compromise the properties of graphene or reduce flake size. Furthermore, these isotropic solutions of graphene in chlorosulfonic acid are ten to a hundred times more concentrated than those that are attained by sonicating graphite in organic solvents [61, 62] or in water in the presence of surfactants [68]. Transparent, conducting films produced from these dispersions have a sheet resistance of $1,000 \Omega/\square$ at ~80% transparency.

It was found that acid strength affects dispersion quality, so that if chlorosulfonic acid is diluted with concentrated (98%) sulfuric acid, graphite solubility decreases. Interestingly, for the same acid solutions graphene is less soluble than SWCNTs; SWCNTs are soluble not only in chlorosulfonic acid but in weaker superacids, such as 102% sulfuric acid, as well. The monolayer exfoliation of graphite in HSO_3Cl was confirmed by TEM and AFM; it was found that 70% of the dispersed graphene flakes were monolayer. The average size of the flakes strongly depends on graphite source; for instance, microcrystalline graphite and grafoil[®] (flexible graphite foil) yield an average flake size of 300 and 900 nm, respectively.

Cryo-TEM experiments have revealed that graphene flakes in chlorosulfonic acid are approximately flat, so they act roughly as rigid platelets [67]. It is known that rigid anisotropic molecules undergo an isotropic/liquid-crystalline transition as their concentration is raised [69]. Thus, concentrated dispersions of graphene in a good solvent, such as HSO_3Cl should yield isotropic/liquid-crystalline phase separation. At high concentrations of graphene in chlorosulfonic acid (~20–30 mg/mL), Behabtu et al. have observed a spontaneous formation of liquid-crystalline phases [67]. Under a cross-polarizer, such dispersion shows birefringence typical of a liquid crystal. While various liquid-crystalline phases (nematic, chiral, columnar) have been reported for disc-like platelets (called discotics), it has been suggested that nematic phase is the only probable phase for polydisperse, unfunctionalized systems such as graphene/superacid [67]. In addition, Behabtu et al. have observed the liquid-crystalline Schlieren texture that is very similar to typical discotic nematic samples [70]. This liquid-crystalline phase is promising for processing of neat graphitic macroscopic articles such as fibers and films.

Several approaches to synthesize non-oxidized graphene use graphite intercalation compounds (GICs) as precursors. GICs have been studied for decades [71, 72], and they have been shown to serve as precursors for exfoliated graphite nanoplatelets with thicknesses of 2–10 nm [73]. To produce monolayer graphene flakes from graphite, several groups reported on a two-step approach, where graphite was first expanded by an acid-temperature treatment to form TEG, and then different intercalating species could be introduced between the layers in the resulting product to further expand the interlayer distance. This approach was employed by Li et al., who inserted tetrabutylammonium hydroxide (TBA) into oleum-intercalated TEG, and then sonicated the product in a solution of a surfactant in DMF to form a homogeneous suspension [74]. After removing large pieces of non-exfoliated TEG platelets from the supernatant, it was found that

the latter contained ~90% of monolayer flakes. Intercalation of TBA to expand the layers in TEG is a crucial step, and it facilitates exfoliation of monolayer flakes in a surfactant solution. In a control experiment without the TBA treatment step, the yield of monolayer graphene flakes was very low. Another approach employing GIC as a precursor for graphene was demonstrated by Lee et al. [75], where thermal decomposition of $C_2F_{10}ClF_3$ (a fluorinated GIC containing the inorganic volatile intercalating agent ClF_3) was performed at 600–700°C followed by dispersion of the resulting product in water with 0.1% sodium dodecylbenzene sulfonate (SDBS). If the product of the thermal shock of fluorinated GIC is treated with a mixture of concentrated nitric and sulfuric acids, the resulting product resembles GO, i.e. it forms stable dispersions in polar solvents, such as water or alcohol, without any surfactants [76]. Graphene can also be obtained by spontaneous exfoliation of a potassium-containing GIC $(K(THF)_x)C_{24}$, where THF—tetrahydrofuran, and $x = 1-3$ in NMP [77] and by microwave induced rapid decomposition of nitromethane in a GIC co-intercalated with $FeCl_3$ and CH_3NO_2 [78].

8.4 Functionalized Graphene and GO

Several studies have been performed to achieve solutions of functionalized graphene and GO; three examples are shown in Fig. 8.11. In the work by Lomeda et al. surfactant-wrapped CCG sheets were functionalized by treatment with aryl diazonium salts [79], Fig. 8.11a. Individual sheets of soluble functionalized graphene can also be prepared via a mechanically assisted exfoliation and functionalization process that involves grinding of thermally expanded graphite oxide (TEGO) with an aryl diazonium salt and potassium carbonate in the presence of an ionic liquid (IL) [80], Fig. 8.11b. The starting TEGO (with less than ten layer graphene) can be obtained by rapidly heating GO (synthesized by the Staudenmaier method) to above 1000°C in a H_2/Ar gas atmosphere to remove most of the oxygen content; the IL used in the work [80] was 1-octyl-3-methylimidazolium tetrafluoroborate (OMIBF₄). By employing different aryl diazonium salts (Fig. 8.11b), the addends of the functionalized materials can be conveniently customized. Previously, ILs have been extensively studied [82], and were found to be attractive for functionalizing SWCNTs due to their ability to exfoliate SWCNT bundles [83, 84], so that the use of ILs in the above process facilitates exfoliation and functionalization of graphene sheets. Recently, ILs were also used to exfoliate graphene flakes from graphite electrodes by electrochemical action [85].

Another approach to synthesize soluble functionalized graphene is shown in Fig. 8.11c [81]. Chemical functionalization of TEG with 4-bromophenyl groups facilitates exfoliation of graphene sheets during sonication of TEG in DMF. The resulting graphene sheets were predominantly edge-functionalized, as confirmed by energy filtered transmission electron microscopy (EFTEM). Because the 4-bromophenyl diazonium salt is a relatively bulky molecule, it does not penetrate

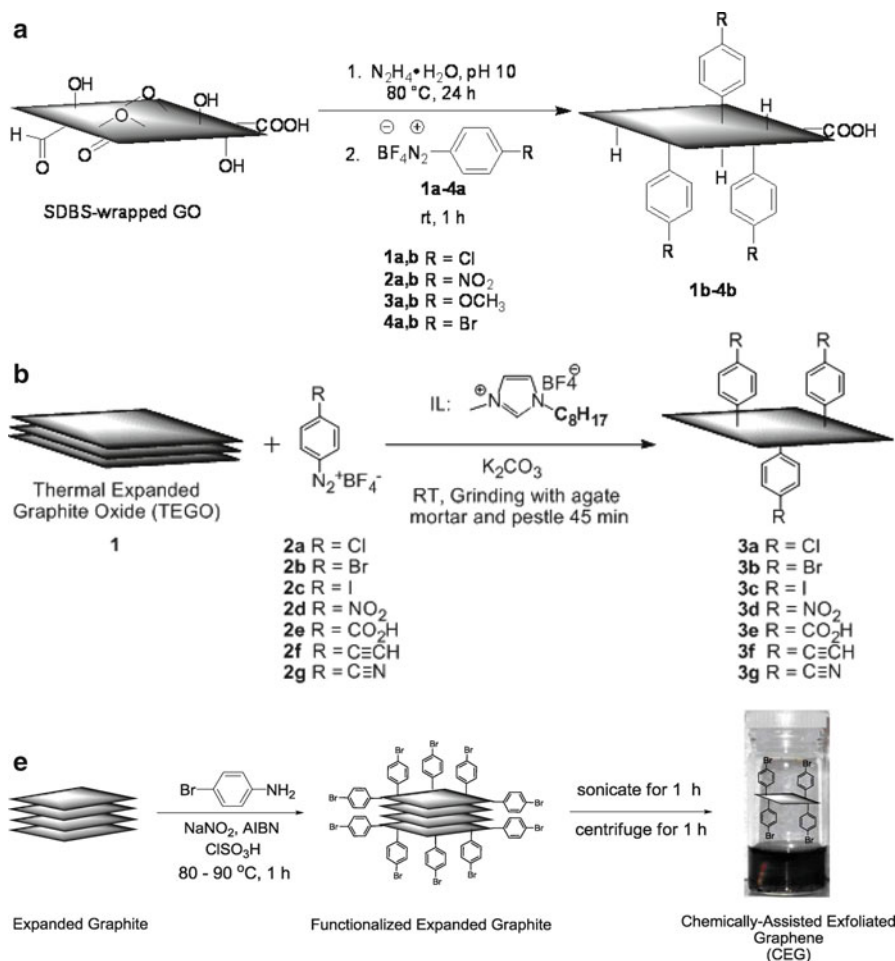


Fig. 8.11 Different approaches for making solutions of graphene functionalized using diazonium chemistry. **(a)** Functionalization of GO Adapted from [79]. **(b)** Exfoliation and functionalization of graphene sheets by grinding thermally expanded graphite in ionic liquid Adapted from [80]. **(c)** Functionalization of TEG to facilitate the exfoliation of graphene (Reproduced with permission from [81]. © 2010 Springer)

and react to the same degree with all of the graphene layers in TEG. In other words, except for the edges, functionalization of the faces of the inner sheets of TEG material is retarded since the reagents cannot readily gain access to the spaces between the sheets. The 4-bromophenyl functional groups are, in large part, bonded within ~ 70 nm of the edges of the functionalized graphene sheets. The TEM data suggest that $>70\%$ of graphene flakes obtained by this method have <5 layers and about 10% are single-layer.

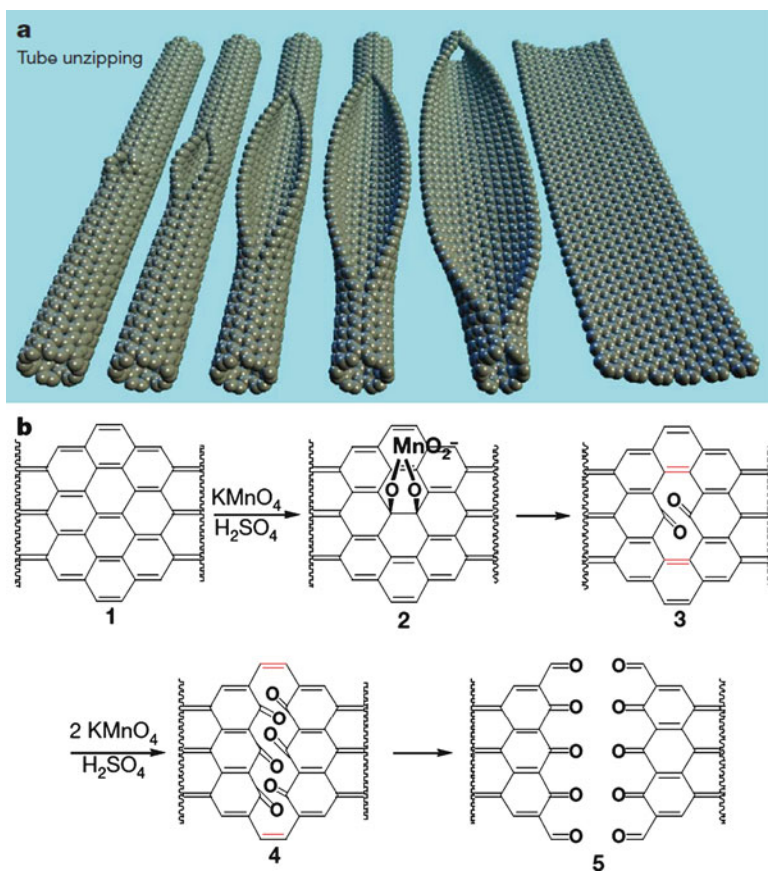


Fig. 8.12 Mechanism of the GONR formation. (a) Schematic representation of the gradual unzipping of one wall of a carbon nanotube to form a nanoribbon. Oxygenated sites are not shown. (b) Scheme of the mechanism of nanotube unzipping as proposed in [86], see text for details (Adapted from [86])

8.5 Graphene from Unzipping CNTs

Recent experiments suggest that Hummers' reagents (H_2SO_4 and KMnO_4) can be successfully used to make graphene oxide not only from flaked graphite but also from carbon nanotubes, another carbon allotrope [86]. In this case, the oxidation of the shells of carbon nanotubes results in their longitudinal “unzipping” and formation of the flakes of graphene oxide with high aspect ratio, so-called “*graphene oxide nanoribbons*” (GONRs). Such GONRs are highly soluble in water (12 mg/mL), ethanol, and other polar organic solvents. The opening of the nanotubes appears to occur along a line, affording straight-edge ribbons (Fig. 8.12a). Kosynkin et al. proposed a mechanism for the nanotube opening, which is based

upon literature precedent for the oxidation of alkenes by permanganate in acid. The first step in this process is manganate ester formation (**2** in Fig. 8.12b) as the rate-determining step, and further oxidation is possible to afford the dione (**3**) in the dehydrating medium [87]. Juxtaposition of the buttressing ketones distorts the β,γ -alkenes making them more prone to the next attack by permanganate. As the process continues, the buttressing-induced strain on the β,γ -alkenes lessens since there is more space for carbonyl projection; however, the bond-angle strain induced by the enlarging hole (or tear if originating from the end of the nanotube) would make the β,γ -alkenes (**4** in Fig. 8.12b) increasingly reactive. Hence, once an opening is initiated, its further opening is enhanced relative to an unopened tube or to an uninitiated site on the same tube. The ketones can be further converted, through their O-protonated forms, to the carboxylic acids [88] that will line the edges of the nanoribbons. Finally, relief of the bond-angle strain when the nanotube opens to the graphene ribbon (**5** in Fig. 8.12b) slows further dione formation and cutting [89]. Thus, the preference for sequential bond cleavage over random opening and subsequent cutting, as occurs with nitric acid oxidation, can be explained by concerted attachment to neighboring carbon atoms by permanganate while the nitronium species from nitric acid does not concertedly attack neighboring carbons. The surface of the now less strained nanoribbon remains prone to 1,2-diol formation which leads to the overall highly oxidized ribbon, but this is less likely to result in further oxidative cutting to the dione due to relief of the tubular strain on the double bonds. Rangel et al. reported *ab initio* density functional theory calculations of the unzipping process [90], confirming the mechanism that was originally proposed in [86]. The important conclusion of the above experimental and theoretical studies is that these nanoribbons have dominant zigzag edges.

Figure 8.13a, b shows representative TEM images of the precursor MWCNTs and the resulting GONR material. While MWCNTs have a starting diameter of 40–80 nm and approximately 15–20 inner nanotube layers, after reaction, the width of the carbon nanostructures increases to >100 nm. The structure of nanoribbons formed from the oxidative unzipping of MWCNTs resembles that of GO, which was confirmed by XPS, XRD and IR-spectroscopy [86]. While hydrazine (N_2H_4) reduction of GO is known to provide a means for restoring conjugation and thus some of the conductivity to form CCG [10, 22, 44, 92], it can also be successfully used to reduce the nanoribbons. Figure 8.13c–l shows SEM images of the reduced graphene nanoribbons (GNRs) that were deposited from aqueous solutions onto Si/SiO₂ substrates [91].

The difference in the appearance of mono-, bi- and multi-layer GNRs is clearly demonstrated in Fig. 8.13. Monolayer GNRs can be distinguished by SEM since their brightness is very close to that of a substrate and they have their long edges parallel to each other. The difference in appearance of mono- and bi-layer GNRs is demonstrated in Figs. 8.13h and i, which show the GNRs with coexisting mono- and bi-layer fragments. After 40 min of hydrazine reduction, monolayer nanoribbons typically had a thickness of 0.7–1.1 nm, whereas bi- and trilayer GNRs were proportionally thicker [91].

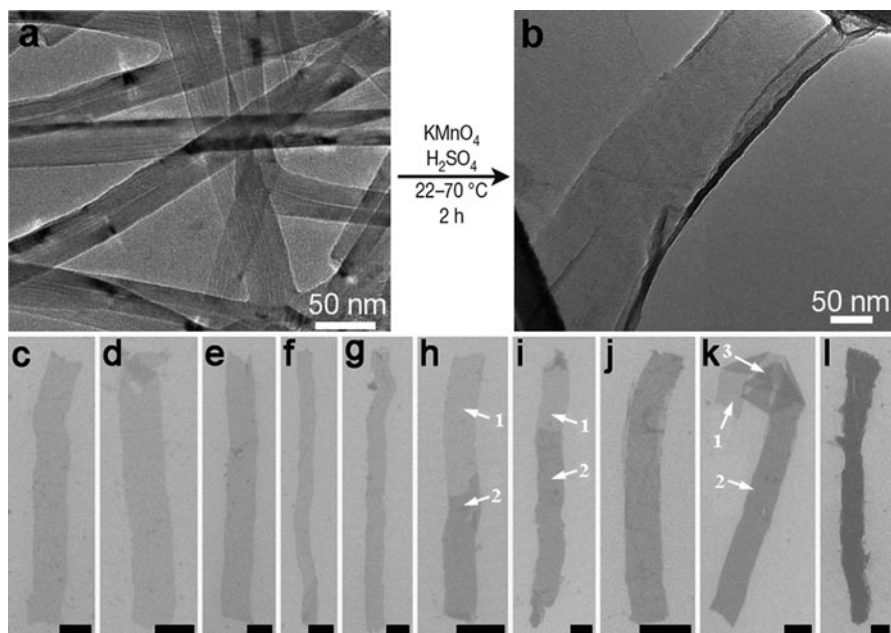


Fig. 8.13 Images of the GONRs and GNRs. (a, b) TEM images depicting the transformation of MWCNTs (a) into GONRs (b). The right side of the ribbon is partially folded onto itself. The dark structures are part of the carbon imaging grid. Images of the hydrazine-reduced GNRs deposited on a Si/SiO₂ substrate. (c–l) SEM images of GNRs: monolayers (c–g), GNRs with coexisting mono- and bi-layer fragments (h,i), bilayers (j,k), and a multilayer stack of GNRs (l). Arrows in (h), (i) and (k) show the number of layers in the corresponding areas of the GNRs; the region in (k) with effective trilayers arises due to the folding of the upper layer in a bilayer GNR. All scale-bars in (c–l) are 250 nm, except for (f) at 500 nm. All GNRs in (c–k) have a width of 180–320 nm, they can be up to several μm long, as shown in (f) at 6.1 μm and (g) at 3.2 μm . Panels (a) and (b) are reproduced from [86], the others are reproduced from [91]

Figure 8.14 demonstrates that GONRs and their reduction products have properties that are very similar to those of GO and CCG. Different approaches can be used to reduce GONRs to GNRs, including hydrazine treatment and annealing in Ar/H₂ atmosphere at different temperatures. The C1s XPS spectra show the decrease in the amount of oxygen-containing functionalities in the GONRs upon reduction (Fig. 8.14a), similarly to the case of GO (Fig. 8.5). The inset in Fig. 8.14a shows the evolution of the Raman spectra of the GONRs upon reduction. Oxidized nanoribbons exhibit a D band at 1363 cm^{-1} and G band at 1594 cm^{-1} with comparable intensities. After reduction the I(D)/I(G) ratio slightly increases, a tendency that was also reported for the reduced product of GO [22]. The reduction results in increased conductivity of the GNRs; Fig. 8.14c illustrates the electronic properties of devices based on GNRs reduced by annealing in Ar/H₂ atmosphere at 900°C [93]. Such reduced GNRs exhibit an ambipolar field effect typical for graphene [5–8]. The conductivity of thus reduced monolayer GNRs on a

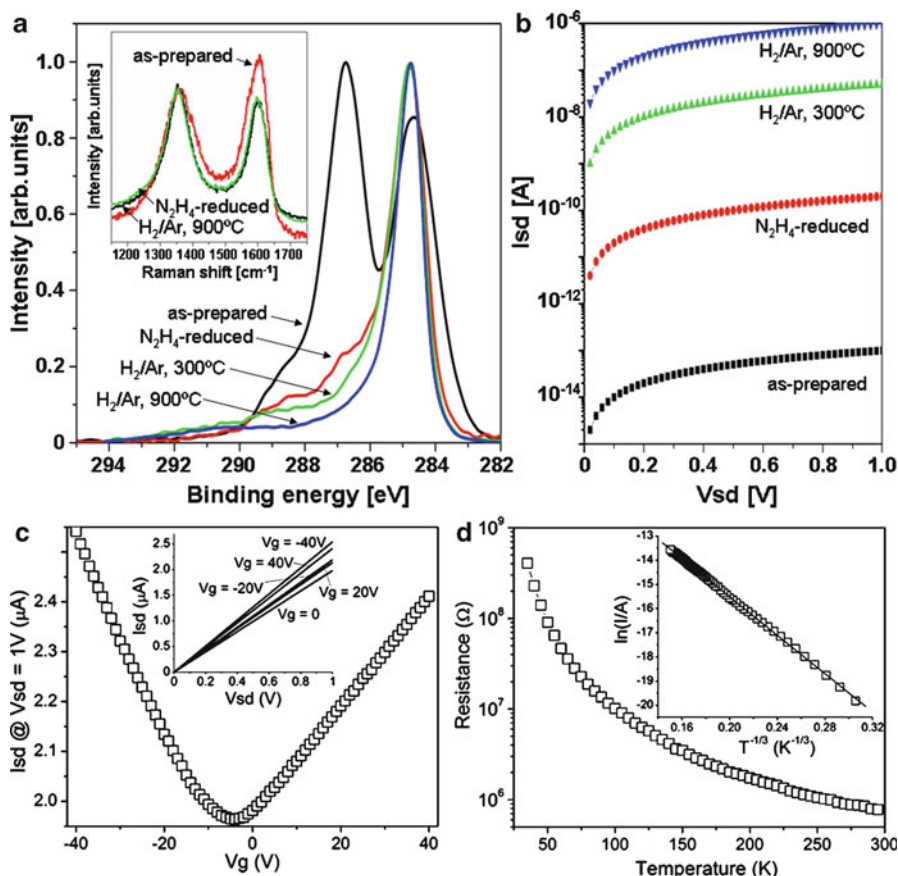


Fig. 8.14 Reduction of GONRs and electrical testing. (a) C1s XPS and Raman (inset) spectra and (b) logarithmic IV curves for the nanoribbons with different degree of reduction. (c, d) Electronic properties of monolayer GNRs reduced in H_2/Ar at 900°C: (c) ambipolar electric field effect and (d) typical temperature dependence of resistance of a GNR. Room temperature source-drain current (I_{sd}) dependence on the gate potential (V_g) shown in (c) was recorded at $V_{sd} = 1$ V for the electronic device based on a 257-nm-wide GNR with the source-drain length of 610 nm. The inset shows $I_{sd} - V_{sd}$ curves recorded at different gate voltages for the same electronic device. Temperature dependence in (d) was recorded for a GNR with $w = 347$ nm and $l = 520$ nm. The inset shows the same data plotted as a logarithm of current (I_{sd}) at $V_{sd} = 1$ V versus $T^{-1/3}$; squares correspond to experimental data and the line is a linear fit. Panels (a) and (b) are reproduced from [91]; panels (c) and (d) are reproduced from [93]

SiO_2 surface at zero gate bias is 35 S/cm; room temperature field-effect mobilities were 0.5–3 $cm^2/V\cdot s$ for both holes and electrons; these measured values of conductivity and mobility of charge carriers are comparable to the numbers reported for CCG produced by reduction of GO [24]. To extend the analogy between GNRs and CCG, a typical temperature dependence of a GNR device in the 20–300 K temperature range is shown (Fig. 8.14d) [93]. Similarly to the case of CCG (Fig. 8.7a),

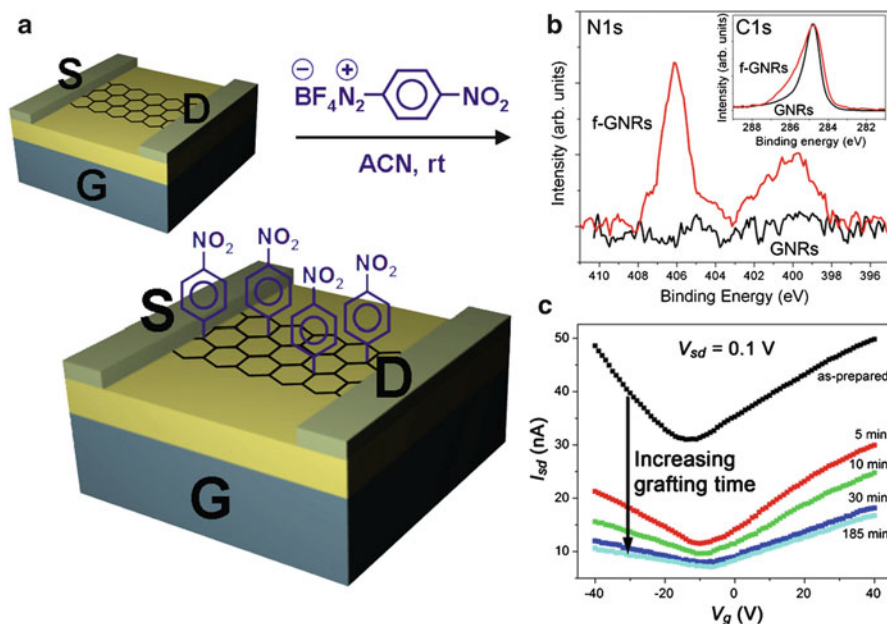


Fig. 8.15 Functionalization of GNRs via diazonium chemistry. (a) Schematic of the chemical functionalization of GNR devices with 4-nitrophenyl groups. Electronic devices with Pt source (S) and drain (D) electrodes were fabricated on a Si/SiO₂ substrate; heavily doped p-type Si was used as a back gate (G). (b) N1s and C1s XPS spectra of the functionalized (f-) and as-prepared GNRs. (c) $I_{sd} - V_g$ curves recorded at $V_{sd} = 0.1$ V for the same GNR device after several consecutive grafting experiments; the captions show the total grafting time (Adapted from [94])

the reduced GNRs exhibit semiconductor-type temperature dependence of conductivity, that is best fit by VRH mechanism, again suggesting similarities between CCG and GNRs.

GNRs prepared by the above approach can be functionalized using diazonium chemistry, similarly to graphene and GO materials. Functionalization with 4-nitrophenyl groups was performed on GNRs serving as channels of nanoscale electronic devices [94], as schematically shown in Fig. 8.15a. This approach enables direct probing of the effect of chemical functionalization on the electronic properties of GNRs. XPS spectroscopy confirms that 4-nitrophenyl groups are strongly attached to GNRs (Fig. 8.15b). After the diazonium treatment, the conductivity of GNR devices gradually decreases with grafting time over the entire V_g -range (Fig. 8.15c), which can be explained by the covalent attachment of 4-nitrophenyl groups to the GNRs, resulting in a transition of graphene carbon atoms from sp^2 to sp^3 hybridization.

Although the original procedure for making GONRs from MWCNTs involved only the use of KMnO₄ and H₂SO₄ [86], further studies suggest that an addition of a second acid may result in GONRs with fewer defects and/or holes on the basal plane. Changes in the reaction conditions such as acid content, time, and temperature were

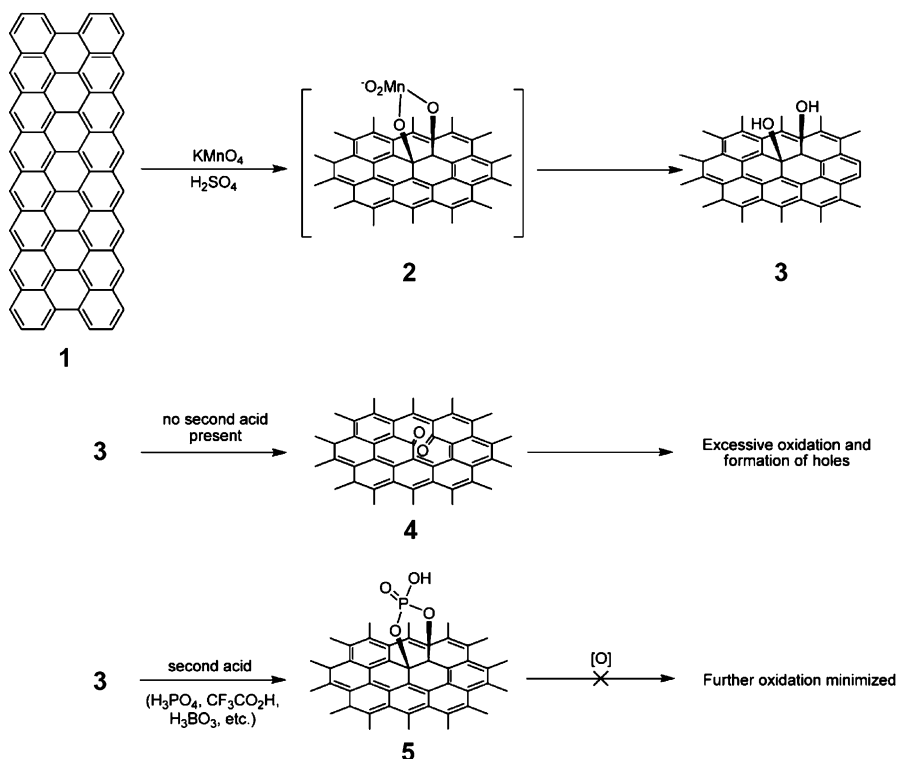


Fig. 8.16 Proposed mechanism for the effect of the second acid in preventing over-oxidation of the GONRs. The manganate ester in **2** could also be protonated. The key step is formation of the cyclic intermediate **5**, resulting in protection of the vicinal diols (**3**) formed during the oxidation (Adapted from [95])

investigated in [95]. A new, optimized method was proposed which introduces a second, weaker acid into the system, improves the selectivity of the oxidative unzipping presumably by in situ protection of the vicinal diols formed on the basal plane of graphene during the oxidation, and thereby prevents their over-oxidation and subsequent hole generation (Fig. 8.16). Examples of such weaker acids include H_3PO_4 , H_3BO_3 , and $\text{CF}_3\text{CO}_2\text{H}$. It is also important to note that the presence of a second acid does not change the overall process through which unzipping of the MWCNT occurs. A proposed mechanism for the participation of the second acid in the oxidation of MWCNTs that results in XGONRs is given in Fig. 8.16. After initial manganate ester formation (**2** in Fig. 8.16), the vicinal diols that are formed will eventually cleave at the carbon-carbon bond between them, giving dione **4** and a new hole in the nanoribbon. Destructive oxidation throughout the structure then occurs and leads to defects and irreversible changes in the basal planes that cannot be repaired with chemical reduction. However, when an acid such as H_3PO_4 is present,

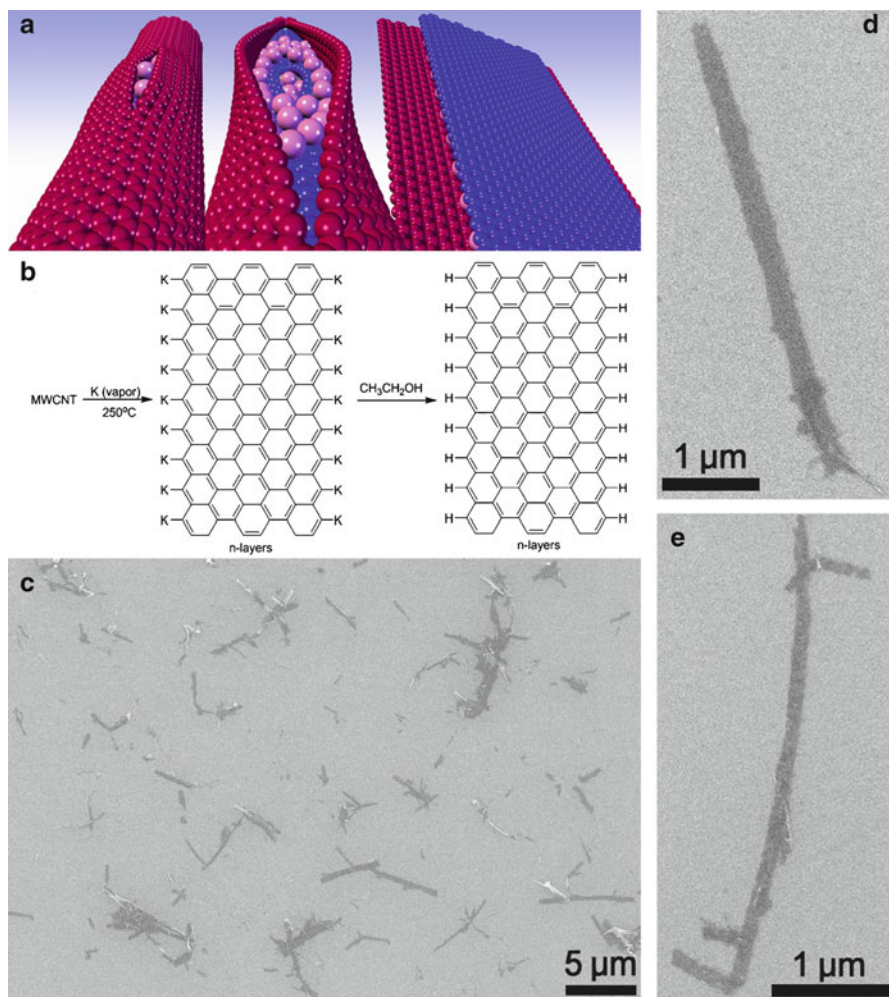


Fig. 8.17 GNRs prepared by splitting MWCNTs with potassium vapor. (a) A schematic of potassium intercalation between the nanotube walls and sequential longitudinal splitting of the walls. (b) A chemical schematic of the splitting processes where ethanol is used to quench the aryl potassium edges; only a single layer is shown for clarity while the actual number of GNR layers correlates with the number of concentric tubes in the MWCNT. (c) SEM image of the nanoribbon material deposited on a Si/SiO₂ substrate, showing complete conversion of MWCNTs to GNRs. (d, e), SEM images of isolated GNR stacks demonstrating characteristic high aspect ratios and predominantly parallel edges (Reproduced from [99])

it will protect the vicinal diols by forming cyclic structure **5**, thus preventing or retarding over-oxidation to the diones.

Several techniques have been reported to unzip MWCNTs without the use of oxidative agents. GNRs can be obtained by the cutting action of catalytic metal

nanoparticles to give low yields of GNRs consisting of 50–100 layers [89], or by treatment of MWCNTs with a solution of lithium in liquid ammonia [96]. While oxidative defects are not introduced by the lithium/liquid ammonia intercalation-driven opening [96], the process fails with pristine nanotubes; a preliminary treatment of the MWCNTs with a strong oxidant is required to induce defects that permit intercalation of the ammonia-solvated lithium rendering defective ribbons that only partially unwrap from the tubular state. Other recently reported techniques to unzip MWCNTs include plasma etching of polymer masked nanotubes [97] and sonication of mildly oxidized MWCNTs in an organic solvent [98]; these two approaches result in GNRs that were demonstrated to be highly conductive. Recently, Kosynkin et al. have demonstrated that GNRs free of oxidized surfaces can be prepared at high yields by splitting MWCNTs with potassium vapor (Fig. 8.17) [99]. If desired, exfoliation is attainable in a subsequent step using chlorosulfonic acid. The low defect density of these GNRs is indicated by their electrical conductivity, comparable to that of graphene derived from mechanically exfoliated graphite. If compared to the GNRs obtained from MWCNTs using the $\text{KMnO}_4/\text{H}_2\text{SO}_4$ protocol, these ribbons are more difficult to exfoliate from multilayer stacks down to monolayers, because they are not chemically functionalized. Also, these new ribbons are not expected to have atomically straight edges, because the MWCNTs are split from the inside by K atoms and not precisely cut by the $\text{KMnO}_4/\text{H}_2\text{SO}_4$ reaction to leave straight zigzag edges. However, the high conductivity of these new ribbons makes them advantageous for applications in composites [100] and conductive thin films [101]. It is interesting to point out that some of the techniques originally developed to unzip carbon nanotubes, were recently shown to also work on boron nitride nanotubes (BNNTs) that share many similarities with CNTs. Boron nitride nanoribbons can also be obtained by plasma etching of BNNTs embedded in the polymer [102], as well as by splitting BNNTs with potassium vapor [103]. It is possible, that these unzipping techniques will also be suitable for nanotubes made of other materials.

8.6 Summary

Many different methods to synthesize GO and related materials have been reported, and many more are anticipated in coming years. Significant progress in preparing stable dispersions of oxidized and nearly pristine graphene, developing new chemistries to functionalize graphene, as well as understanding the structure and properties of these materials has been made. Although most of these materials are inferior to mechanically exfoliated graphene [5–8], as well as graphene grown by chemical vapor deposition [104–106] in terms of electrical conductivity, they enjoy simple bulk fabrication techniques from inexpensive source (graphite) and therefore are suitable for many large-scale applications. Some of these applications, such as polymer composites [100, 107] and supercapacitors [108–114], are already being

commercialized [115]. Other applications, including coatings and paper-like materials [116], flexible transparent electrodes [10, 117–121], chemical sensors [122–126], drug-delivery vectors [127], highly transparent supports for TEM [128], and flame retardant materials [129] may find their way to the market. In addition, there is developing interest in a solution-phase exfoliation of other layered materials, such as BN, MoS₂ and WS₂ [130]. These and other materials will likely spark a new wave of research activity, as well as novel applications.

References

1. Castro Neto, A. H.; Guinea, F.; Peres, N. M. R.; Novoselov, K. S.; Geim, A. K. The Electronic Properties of Graphene. *Rev. Mod. Phys.* **2009**, *81*, 109–162.
2. Geim, A. K.; Novoselov, K. S. The Rise of Graphene. *Nature Mater.* **2007**, *6*, 183–191.
3. Geim, A. K. Graphene: Status and Prospects. *Science* **2009**, *324*, 1530–1534.
4. Allen, M. J.; Tung, V. C.; Kaner, R. B. Honeycomb Carbon: A Review of Graphene. *Chem. Rev.* **2010**, *110*, 132–145.
5. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
6. Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K. Two-Dimensional Atomic Crystals. *Proc. Natl. Acad. Sci. USA* **2005**, *102*, 10451–10453.
7. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Katsnelson, M. I.; Grigorieva, I. V.; Dubonos, S. V.; Firsov, A. A. Two-Dimensional Gas of Massless Dirac Fermions in Graphene. *Nature* **2005**, *438*, 197–200.
8. Zhang, Y.; Tan, Y. W.; Stormer, H. L.; Kim, P. Experimental Observation of the Quantum Hall Effect and Berry's Phase in Graphene. *Nature* **2005**, *438*, 201–204.
9. Brodie, B. C. On the Atomic Weight of Graphite. *Philosophical Transactions of the Royal Society of London* **1859**, *149*, 249–259.
10. Li, D.; Mueller, M. B.; Gilje, S.; Kaner, R. B.; Wallace, G. G. Processable aqueous dispersions of graphene nanosheets. *Nature Nanotech.* **2008**, *3*, 101–105.
11. Zhou, X.; Zhang, J.; Wu, H.; Yang, H.; Zhang, J.; Guo, S. Reducing Graphene Oxide via Hydroxylamine: A Simple and Efficient Route to Graphene. *J. Phys. Chem. C* **2011**, *115*, 11957–11961.
12. Gao, W.; Alemany, L. B.; Ci, L.; Ajayan, P. M. New Insights into the Structure and Reduction of Graphite Oxide. *Nature Chem.* **2009**, *1*, 403–408.
13. Mohanty, N.; Nagaraja, A.; Armesto, J.; Berry, V. High-Throughput, Ultrafast Synthesis of Solution-Dispersed Graphene via a Facile Hydride Chemistry. *Small* **2010**, *6*, 226–231.
14. Yang, D.; Velamakanni, A.; Bozoklu, G.; Park, S.; Stoller, M.; Piner, R. D.; Stankovich, S.; Jung, I.; Field, D. A.; Ventrone Jr., C. A.; Ruoff, R. S. Chemical Analysis of Graphene Oxide Films after Heat and Chemical Treatments by X-Ray Photoelectron and Micro-Raman Spectroscopy. *Carbon* **2009**, *47*, 145–152.
15. Cote, L. J.; Cruz-Silva, R.; Huang, J. Flash Reduction and Patterning of Graphite Oxide and Its Polymer Composite. *J. Am. Chem. Soc.* **2009**, *131*, 11027–11032.
16. Dubin, S.; Gilje, S.; Wang, K.; Tung, V. C.; Cha, K.; Hall, A. S.; Farrar, J.; Varshneya, R.; Yang, Y.; Kaner, R. B. A One-Step, Solvothermal Reduction Method for Producing Reduced Graphene Oxide Dispersions in Organic Solvents. *ACS Nano* **2010**, *4*, 3845–3852.
17. Salas, E. C.; Sun, Z.; Lüttge, A.; Tour, J. M. Reduction of Graphene Oxide via Bacterial Respiration. *ACS Nano* **2010**, *4*, 4852–4856.

18. Staudenmaier, L. Verfahren zur Darstellung der Graphitsäure *Ber. Dtsch. Chem. Ges.* **1898**, *31*, 1481–1487.
19. Hummers, W. S.; Offeman, R. E. Preparation of Graphitic Oxide. *J. Am. Chem. Soc.* **1958**, *80*, 1339.
20. Boehm, H. P.; Clauss, A.; Fischer, G. O.; Hofmann, U. Dünnsche Kohlenstoff-Folien. *Z. Naturforsch.* **1962**, *17 b*, 150–153.
21. Marcano, D. C.; Kosynkin, D. V.; Berlin, J. M.; Sinitskii, A.; Sun, Z.; Slesarev, A.; Alemany, L. B.; Lu, W.; Tour, J. M. Improved Synthesis of Graphene Oxide. *ACS Nano* **2010**, *4*, 4806–4814.
22. Stankovich, S.; Dikin, D. A.; Piner, R. D.; Kohlhaas, K. A.; Kleinhammes, A.; Jia, Y.; Wu, Y.; Nguyen, S. T.; Ruoff, R. S. Synthesis of Graphene-Based Nanosheets via Chemical Reduction of Exfoliated Graphite Oxide. *Carbon* **2007**, *45*, 1558–1565.
23. Gilje, S.; Han, S.; Wang, M.; Wang, K. L.; Kaner, R. B. A Chemical Route to Graphene for Device Applications. *Nano Lett.* **2007**, *7*, 3394–3398.
24. Gómez-Navarro, C.; Weitz, R. T.; Bittner, A. M.; Scolari, M.; Mews, A.; Burghard, M.; Kern, K. Electronic Transport Properties of Individual Chemically Reduced Graphene Oxide Sheets. *Nano Lett.* **2007**, *7*, 3499–3503.
25. Tung, V. C.; Allen, M. J.; Yang, Y.; Kaner, R. B. High-Throughput Solution Processing of Large-Scale Graphene. *Nature Nanotech.* **2009**, *4*, 25–29.
26. Schniepp, H. C.; Li, J. L.; McAllister, M. J.; Sai, H.; Herrera-Alonso, M.; Adamson, D. H.; Prud'homme, R. K.; Car, R.; Saville, D. A.; Aksay, I. A. Functionalized Single Graphene Sheets Derived from Splitting Graphite Oxide. *J. Phys. Chem. B* **2006**, *110*, 8535–8539.
27. Sinitskii, A.; Kosynkin, D. V.; Dimiev, A.; Tour, J. M. Corrugation of Chemically Converted Graphene Monolayers on SiO₂. *ACS Nano* **2010**, *4*, 3095–3102.
28. Buchsteiner, A.; Lerf, A.; Pieper, J. Water Dynamics in Graphite Oxide Investigated with Neutron Scattering. *J. Phys. Chem. B*, **2006**, *110*, 22328–22338.
29. Gómez-Navarro, C.; Meyer, J. C.; Sundaram, R. S.; Chuvilin, A.; Kurasch, S.; Burghard, M.; Kern, K.; Kaiser, U. Atomic Structure of Reduced Graphene Oxide. *Nano Lett.* **2010**, *10*, 1144–1148.
30. Erickson, K.; Erni, R.; Lee, Z.; Alem, N.; Gannett, W.; Zettl, A. Determination of the Local Chemical Structure of Graphene Oxide and Reduced Graphene Oxide. *Adv. Mater.* **2010**, *22*, 4467–4472.
31. Lerf, A.; He, H.; Forster, M.; Klinowski, J. Structure of Graphite Oxide Revisited. *J. Phys. Chem. B* **1998**, *102*, 4477–4482.
32. He, H.; Klinowski, J.; Forster, M.; Lerf, A. A New Structural Model for Graphite Oxide. *Chem. Phys. Lett.* **1998**, *287*, 53–56.
33. He, H.; Riedl, T.; Lerf, A.; Klinowski, J. Solid-State NMR Studies of the Structure of Graphite Oxide. *J. Phys. Chem.* **1996**, *100*, 19954–19958.
34. Dreyer, D. R.; Park, S.; Bielawski, C. W.; Ruoff, R. S. The Chemistry of Graphene Oxide. *Chem. Soc. Rev.* **2010**, *39*, 228–240.
35. Paci, J. T.; Belytschko, T.; Schatz, G. C. Computational Studies of the Structure, Behavior upon Heating, and Mechanical Properties of Graphite Oxide. *J. Phys. Chem. C* **2007**, *111*, 18099–18111.
36. Jung, I.; Dikin, D.; Park, S.; Cai, W.; Mielke, S. L.; Ruoff, R. S. Effect of Water Vapor on Electrical Properties of Individual Reduced Graphene Oxide Sheets. *J. Phys. Chem. C* **2008**, *112*, 20264–20268.
37. Becerril, H. A.; Mao, J.; Liu, Z.; Stoltenberg, R. M.; Bao, Z.; Chen, Y. Evaluation of Solution-Processed Reduced Graphene Oxide Films as Transparent Conductors. *ACS Nano*, **2008**, *2*, 463–470.
38. Boukhvalov, D. W.; Katsnelson, M. I. Modeling of Graphite Oxide. *J. Am. Chem. Soc.* **2008**, *130*, 10697–10701.
39. Kim, M. C.; Hwang, G. S.; Ruoff, R. S. Epoxide Reduction with Hydrazine on Graphene: A First Principles Study. *J. Chem. Phys.* **2009**, *131*, 064704.

40. Cai, W.; Piner, R. D.; Stadermann, F. J.; Park, S.; Shaibat, M. A.; Ishii, Y.; Yang, D.; Velamakanni, A.; An, S. J.; Stoller, M.; An, J.; Chen, D.; Ruoff, R. S. Synthesis and Solid-State NMR Structural Characterization of ^{13}C -Labeled Graphite Oxide. *Science* **2008**, *321*, 1815–1817.
41. Jeong, H. K.; Lee, Y. P.; Lahaye, R. J. W. E.; Park, M. H.; An, K. H.; Kim, I. J.; Yang, C. W.; Park, C. Y.; Ruoff, R. S.; Lee, Y. H. Evidence of Graphitic AB Stacking Order of Graphite Oxides. *J. Am. Chem. Soc.* **2008**, *130*, 1362–1366.
42. Stankovich, S.; Piner, R. D.; Chen, X.; Wu, N.; Nguyen, S. T.; Ruoff, R. S. Stable Aqueous Dispersions of Graphitic Nanoplatelets via the Reduction of Exfoliated Graphite Oxide in the Presence of Poly(sodium 4-styrenesulfonate). *J. Mater. Chem.* **2006**, *16*, 155–158.
43. Schedin, F.; Geim, A. K.; Morozov, S. V.; Hill, E. W.; Blake, P.; Katsnelson, M. I.; Novoselov, K. S. Detection of Individual Gas Molecules Adsorbed on Graphene. *Nat. Mater.* **2007**, *6*, 652–655.
44. Eda, G.; Fanchini, G.; Chhowalla, M. Large-Area Ultrathin Films of Reduced Graphene Oxide as a Transparent and Flexible Electronic Material. *Nat. Nanotech.* **2009**, *3*, 270–274.
45. Jung, I.; Dikin, D. A.; Piner, R. D.; Ruoff, R. S. Tunable Electrical Conductivity of Individual Graphene Oxide Sheets Reduced at “Low” Temperatures. *Nano Lett.* **2008**, *8*, 4283–4287.
46. Wang, H.; Robinson, J. T.; Li, X.; Dai, H. Solvothermal Reduction of Chemically Exfoliated Graphene Sheets. *J. Am. Chem. Soc.* **2009**, *131*, 9910–9911.
47. Morozov, S. V.; Novoselov, K. S.; Katsnelson, M. I.; Schedin, F.; Ponomarenko, L. A.; Jiang, D.; Geim, A. K. Strong Suppression of Weak Localization in Graphene. *Phys. Rev. Lett.* **2006**, *97*, 016801.
48. Tan, Y. W.; Zhang, Y.; Stormer, H. L.; Kim, P. Temperature Dependent Electron Transport in Graphene. *Eur. Phys. J. Special Topics* **2007**, *148*, 15–18.
49. Bolotin, K. I.; Sikes, K. J.; Hone, J.; Stormer, H. L.; Kim, P. Temperature-Dependent Transport in Suspended Graphene. *Phys. Rev. Lett.* **2008**, *101*, 096802.
50. Kaiser, A. B.; Gómez-Navarro, C.; Sundaram, R. S.; Burghard, M.; Kern, K. Electrical Conduction Mechanism in Chemically Derived Graphene Monolayers. *Nano Lett.* **2009**, *9*, 1787–1792.
51. Eda, G.; Mattevi, C.; Yamaguchi, H.; Kim, H. K.; Chhowalla, M. Insulator to Semimetal Transition in Graphene Oxide. *J. Phys. Chem. C*, **2009**, *113*, 15768–15771.
52. N.F. Mott, E.A. Davis, *Electronic Processes in Non-Crystalline Materials*; Oxford University Press: Oxford, England, 1971.
53. Stolyarova, E.; Rim, K. T.; Ryu, S.; Maultzsch, J.; Kim, P.; Brus, L. E.; Heinz, T. F.; Hybertsen, M. S.; Flynn, G. W. High-Resolution Scanning Tunneling Microscopy Imaging of Mesoscopic Graphene Sheets on an Insulating Surface. *Proc. Natl Acad. Sci. USA* **2007**, *104*, 9209–9212.
54. Dean, C. R.; Young, A. F.; Meric, I.; Lee, C.; Wang, L.; Sorgenfrei, S.; Watanabe, K.; Taniguchi, T.; Kim, P.; Shepard, K. L.; Hone, J. Boron Nitride Substrates for High-Quality Graphene Electronics. *Nature Nanotech.* **2010**, *5*, 722–726.
55. Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Klima, M.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. Ultrahigh Electron Mobility in Suspended Graphene. *Solid State Comm.* **2008**, *146*, 351–355.
56. Du, X.; Skachko, I.; Barker, A.; Andrei, E. Y. Approaching Ballistic Transport in Suspended Graphene. *Nature Nanotech.* **2008**, *3*, 491–496.
57. Si, Y.; Samulski, E. T. Synthesis of Water Soluble Graphene. *Nano Lett.* **2008**, *8*, 1679–1682.
58. Paredes, J. I.; Villar-Rodil, S.; Martínez-Alonso, A.; Tascón, J. M. D. Graphene Oxide Dispersions in Organic Solvents. *Langmuir* **2008**, *24*, 10560–10564.
59. Xu, Y.; Bai, H.; Lu, G.; Li, C.; Shi, G. Flexible Graphene Films via the Filtration of Water-Soluble Noncovalent Functionalized Graphene Sheets. *J. Am. Chem. Soc.* **2008**, *130*, 5856–5857.
60. Luo, Z.; Lu, Y.; Somers, L. A.; Johnson, A. T. C. High Yield Preparation of Macroscopic Graphene Oxide Membranes. *J. Am. Chem. Soc.* **2009**, *131*, 898–899.

61. Blake, P.; Brimicombe, P. D.; Nair, R. R.; Booth, T. J.; Jiang, D.; Schedin, F.; Ponomarenko, L. A.; Morozov, S. V.; Gleeson, H. F.; Hill, E. W.; Geim, A. K.; Novoselov, K. S. Graphene-Based Liquid Crystal Device. *Nano Lett.* **2008**, *8*, 1704–1708.
62. Hernandez, Y.; Nicolosi, V.; Lotya, M.; Blighe, F. M.; Sun, Z.; De, S.; McGovern, I. T.; Holland, B.; Byrne, M.; Gun'Ko, Y. K.; Boland, J. J.; Niraj, P.; Duesberg, G.; Krishnamurthy, S.; Goodhue, R.; Hutchinson, J.; Scardaci, V.; Ferrari, A. C.; Coleman, J. N. High-Yield Production of Graphene by Liquid-Phase Exfoliation of Graphite. *Nature Nanotech.* **2008**, *3*, 563–568.
63. Hamilton, C. E.; Lomeda, J. R.; Sun, Z.; Tour, J. M.; Barron, A. R. High-Yield Organic Dispersions of Unfunctionalized Graphene. *Nano Lett.* **2009**, *9*, 3460–3462.
64. Bahr, J. L.; Mickelson, E. T.; Bronikowski, M. J.; Smalley, R. E.; Tour, J. M. Dissolution of small diameter single-wall carbon nanotubes in organic solvents? *Chem. Commun.* **2001**, 193–194.
65. Hao, R.; Qian, W.; Zhang, L.; Hou, Y. Aqueous Dispersions of TCNQ-Anion-Stabilized Graphene Sheets. *Chem. Commun.* **2008**, 6576–6578.
66. Davis, V. A.; Parra-Vasquez, A. N. G.; Green, M. J.; Rai, P. K.; Behabtu, N.; Prieto, V.; Booker, R. D.; Schmidt, J.; Kesselman, E.; Zhou, W.; Fan, H.; Adams, W. W.; Hauge, R. H.; Fischer, J. E.; Cohen, Y.; Talmon, Y.; Smalley, R. E.; Pasquali, M. True Solutions of Single-Walled Carbon Nanotubes for Assembly into Macroscopic Materials. *Nature Nanotech.* **2009**, *4*, 830–834.
67. Behabtu, N.; Lomeda, J. R.; Green, M. J.; Higginbotham, A. L.; Sinitiskii, A.; Kosynkin, D. V.; Tsentalovich, D.; Parra-Vasquez, A. N. G.; A; Schmidt, J.; Kesselman, E.; Cohen, Y.; Talmon, Y.; Tour, J. M.; Pasquali, M. Spontaneous High-Concentration Dispersions and Liquid Crystals of Graphene. *Nature Nanotech.* **2010**, *5*, 406–411.
68. Lotya, M.; Hernandez, Y.; King, P. J.; Smith, R. J.; Nicolosi, V.; Karlsson, L. S.; Blighe, F. M.; De, S.; Wang, Z.; McGovern, I. T.; Duesberg, G. S.; Coleman, J. N. Liquid Phase Production of Graphene by Exfoliation of Graphite in Surfactant/Water Solutions. *J. Am. Chem. Soc.* **2009**, *131*, 3611–3620.
69. Onsager, L. The Effects of Shape on the Interaction of Colloidal Particles. *Ann. NY Acad. Sci.* **1949**, *51*, 627–659.
70. Chandrasekhar, S. Liquid Crystals. *Cambridge Univ. Press.* **1992**.
71. Dresselhaus, M. S.; Dresselhaus, G. Intercalation Compounds of Graphite. *Adv. Phys.* **1981**, *30*, 139–326.
72. Enoki, T.; Suzuki, M.; Endo, M. Graphite Intercalation Compounds and Applications. *Oxford Univ. Press.* **2003**.
73. Viculis, L. M.; Mack, J. J.; Mayer, O. M.; Hahn, H. T.; Kaner, R. B. Intercalation and Exfoliation Routes to Graphite Nanoplatelets. *J. Mater. Chem.* **2005**, *15*, 974–978.
74. Li, X.; Zhang, G.; Bai, X.; Sun, X.; Wang, X.; Wang, E.; Dai, H. Highly Conducting Graphene Sheets and Langmuir–Blodgett Films. *Nature Nanotech.* **2008**, *3*, 538–542.
75. Lee, J. H.; Shin, D. W.; Makotchenko, V. G.; Nazarov, A. S.; Fedorov, V. E.; Kim, Y. H.; Choi, J. Y.; Kim, J. M.; Yoo, J. B. One-Step Exfoliation Synthesis of Easily Soluble Graphite and Transparent Conducting Graphene Sheets. *Adv. Mater.* **2009**, *21*, 4383–4387.
76. Vallés, C.; Drummond, C.; Saadaoui, H.; Furtado, C. A.; He, M.; Roubeau, O.; Ortolani, L.; Monthieux, M.; Pénicaud, A. Solutions of Negatively Charged Graphene Sheets and Ribbons. *J. Am. Chem. Soc.* **2008**, *130*, 15802–15804.
77. Grayfer, E. D.; Nazarov, A. S.; Makotchenko, V. G.; Kim, S. J.; Fedorov, V. E. Chemically Modified Graphene Sheets by Functionalization of Highly Exfoliated Graphite. *J. Mater. Chem.* **2011**, *21*, 3410–3414.
78. Fu, W.; Kiggans, J.; Overbury, S. H.; Schwartz, V.; Liang, C. Low-Temperature Exfoliation of Multilayer-Graphene Material from FeCl_3 and CH_3NO_2 Co-Intercalated Graphite Compound. *Chem. Commun.* **2011**, *47*, 5265–5267.

79. Lomeda, J. R.; Doyle, C. D.; Kosynkin, D. V.; Hwang, W. F.; Tour, J. M. Diazonium Functionalization of Surfactant-Wrapped Chemically Converted Graphene Sheets. *J. Am. Chem. Soc.* **2008**, *130*, 16201–16206.
80. Jin, Z.; Lomeda, J. R.; Price, B. P.; Lu, W.; Zhu, Y.; Tour, J. M. Mechanically Assisted Exfoliation and Functionalization of Thermally Converted Graphene Sheets. *Chem. Mater.* **2009**, *21*, 3045–3047.
81. Sun, Z.; Kohama, S.; Zhang, Z.; Lomeda, J. R.; Tour, J. M. Soluble Graphene Through Edge-Selective Functionalization. *Nano Res.* **2010**, *3*, 117–125.
82. Greaves, T. L.; Drummond, C. J. Protic Ionic Liquids: Properties and Applications. *Chem. Rev.* **2008**, *108*, 206–237.
83. Fukushima, T.; Kosaka, A.; Ishimura, Y.; Yamamoto, T.; Takigawa, T.; Ishii, N.; Aida, T. Molecular Ordering of Organic Molten Salts Triggered by Single-Walled Carbon Nanotubes. *Science* **2003**, *300*, 2072–2074.
84. Price, B. K.; Hudson, J. L.; Tour, J. M. Green Chemical Functionalization of Single-Walled Carbon Nanotubes in Ionic Liquids. *J. Am. Chem. Soc.* **2005**, *127*, 14867–14870.
85. Liu, N.; Luol, F.; Wu, H.; Liu, Y.; Zhang, C.; Chen, J. One-Step Ionic-Liquid-Assisted Electrochemical Synthesis of Ionic-Liquid-Functionalized Graphene Sheets Directly from Graphite. *Adv. Funct. Mater.* **2008**, *18*, 1518–1525.
86. Kosynkin, D. V.; Higginbotham, A. L.; Sinitskii, A.; Lomeda, J. R.; Dimiev, A.; Price, B. K.; Tour, J. M. Longitudinal Unzipping of Carbon Nanotubes to Form Graphene Nanoribbons. *Nature* **2009**, *458*, 872–876.
87. Wolfe, S.; Ingold, C. F.; Lemieux, R. U. Oxidation of olefins by potassium permanganate. Mechanism of α -ketol formation. *J. Am. Chem. Soc.* **1981**, *103*, 938–939.
88. Banoo, F.; Stewart, R. Mechanisms of permanganate oxidation. IX. Permanganate oxidation of aromatic alcohols in acid solution. *Can. J. Chem.* **1969**, *47*, 3199–3205.
89. Elías, A. L.; Botello-Méndez, A. R.; Meneses-Rodríguez, D.; González, V. J.; Ramírez-González, D.; Ci, L.; Muñoz-Sandoval, E.; Ajayan, P. M.; Terrones, H.; Terrones, M. Longitudinal Cutting of Pure and Doped Carbon Nanotubes to Form Graphitic Nanoribbons Using Metal Clusters as Nanoscalpels. *Nano Lett.* **2010**, *10*, 366–372.
90. Rangel, N. L.; Sotelo, J. C.; Seminario, J. M. Mechanism of Carbon Nanotubes Unzipping into Graphene Ribbons. *J. Chem. Phys.* **2009**, *131*, 031105.
91. Sinitskii, A.; Dimiev, A.; Kosynkin, D. V.; Tour, J. Graphene Nanoribbon Devices Produced by Oxidative Unzipping of Carbon Nanotubes. *ACS Nano* **2010**, *4*, 5405–5413.
92. Bourlino, A. B.; Gournis, D.; Petridis, D.; Szabó, T.; Szeri, A.; Dékány, I. Graphite Oxide: Chemical Reduction to Graphite and Surface Modification with Primary Aliphatic Amines and Amino Acids. *Langmuir* **2003**, *19*, 6050–6055.
93. Sinitskii, A.; Fursina, A. A.; Kosynkin, D. V.; Higginbotham, A. L.; Natelson, D.; Tour, J. M. Electronic Transport in Monolayer Graphene Nanoribbons Produced by Chemical Unzipping of Carbon Nanotubes. *Appl. Phys. Lett.* **2009**, *95*, 253108.
94. Sinitskii, A.; Dimiev, A.; Corley, D. A.; Fursina, A. A.; Kosynkin, D. V.; Tour, J. M. Kinetics of Diazonium Functionalization of Chemically Converted Graphene Nanoribbons. *ACS Nano* **2010**, *4*, 1949–1954.
95. Higginbotham, A. L.; Kosynkin, D. V.; Sinitskii, A.; Sun, Z.; Tour, J. M. Lower-Defect Graphene Oxide Nanoribbons from Multiwalled Carbon Nanotubes. *ACS Nano* **2010**, *4*, 2059–2069.
96. Cano-Márquez, A. G.; Rodríguez-Macías, F. J.; Campos-Delgado, J.; Espinosa-González, C. G.; Tristán-López, F.; Ramírez-González, D.; Cullen, D. A.; Smith, D. J.; Terrones, M.; Vega-Cantú, Y. I. Ex-MWNTs: Graphene Sheets and Ribbons Produced by Lithium Intercalation and Exfoliation of Carbon Nanotubes. *Nano Lett.*, **2009**, *9*, 1527–1533.
97. Jiao, L.; Zhang, L.; Wang, X.; Diankov, G.; Dai, H. Narrow Graphene Nanoribbons from Carbon Nanotubes. *Nature* **2009**, *458*, 877–880.
98. Jiao, L.; Wang, X.; Diankov, G.; Wang, H.; Dai, H. Facile Synthesis of High-Quality Graphene Nanoribbons. *Nature Nanotech.* **2010**, *5*, 321–325.

99. Kosynkin, D. V.; Lu, W.; Sinitskii, A.; Pera, G.; Sun, Z.; Tour, J. M. Highly Conductive Graphene Nanoribbons by Longitudinal Splitting of Carbon Nanotubes Using Potassium Vapor. *ACS Nano*, **2011**, 5, 968–974.
100. Rafiee, M. A.; Lu, W.; Thomas, A. V.; Zandiatashbar, A.; Rafiee, J.; Tour, J. M.; Koratkar, N. A. Graphene Nanoribbon Composites. *ACS Nano*, **2010**, 4, 7415–7420.
101. Zhu, Y.; Lu, W.; Sun, Z.; Kosynkin, D. V.; Yao, J. Tour, J. M. High Throughput Preparation of Large Area Transparent Electrodes Using Non-Functionalized Graphene Nanoribbons. *Chem. Mater.* **2011**, 23, 935–939.
102. Zeng, H.; Zhi, C.; Zhang, Z.; Wei, X.; Wang, X.; Guo, W.; Bando, Y.; Golberg, D. “White Graphenes”: Boron Nitride Nanoribbons via Boron Nitride Nanotube Unwrapping. *Nano Lett.* **2010**, 10, 5049–5055.
103. Erickson, K. J.; Gibb, A. L.; Sinitskii, A.; Rousseas, M.; Alem, N.; Tour, J. M.; Zettl, A. K. Longitudinal Splitting of Boron Nitride Nanotubes for the Facile Synthesis of High Quality Boron Nitride Nanoribbons. *Nano Lett.* **2011**, 11, 3221–3226.
104. Reina, A.; Jia, X.; Ho, J.; Nezich, D.; Son, H.; Bulovic, V.; Dresselhaus, M. S.; Kong, J. Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition. *Nano Lett.* **2009**, 9, 30–35.
105. Kim, K. S.; Zhao, Y.; Jang, H.; Lee, S. Y.; Kim, J. M.; Kim, K. S.; Ahn, J. H.; Kim, P.; Choi, J. Y.; Hong, B. H. Large-Scale Pattern Growth of Graphene Films for Stretchable Transparent Electrodes. *Nature* **2009**, 457, 706–710.
106. Li, X.; Cai, W.; An, J.; Kim, S.; Nah, J.; Yang, D.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; Banerjee, S. K.; Colombo, L.; Ruoff, R. S. Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils. *Science* **2009**, 324, 1312–1314.
107. Potts, J. R.; Dreyer, D. R.; Bielawski, C. W.; Ruoff, R. S. Graphene-Based Polymer Nanocomposites. *Polymer* **2011**, 52, 5–25.
108. Stoller, M. D.; Park, S.; Zhu, Y.; An, J.; Ruoff, R. S. Graphene-Based Supercapacitors. *Nano Lett.* **2008**, 8, 3498–3502.
109. Liu, C.; Yu, Z.; Neff, D.; Zhamu, A.; Jang, B. Z. Graphene-Based Supercapacitor with an Ultrahigh Energy Density. *Nano Lett.* **2010**, 10, 4863–4868.
110. Kim, T. Y.; Lee, H. W.; Stoller, M.; Dreyer, D. R.; Bielawski, C.; Ruoff, R. S.; Suh, K. S. High-Performance Supercapacitors Based on Poly(ionic liquid)-Modified Graphene Electrodes. *ACS Nano* **2010**, 5, 436–442.
111. Chen, S.; Zhu, J.; Wu, X.; Han, Q.; Wang, X. Graphene Oxide-MnO₂ Nanocomposites for Supercapacitors. *ACS Nano* **2010**, 4, 2822–2830.
112. Wu, Q.; Xu, Y.; Yao, Z.; Liu, A.; Shi, G. Supercapacitors Based on Flexible Graphene/Polyaniline Nanofiber Composite Films. *ACS Nano* **2010**, 4, 1963–1970.
113. Yoo, J. J.; Balakrishnan, K.; Huang, J.; Meunier, V.; Sumpter, B. G.; Srivastava, A.; Conway, M.; Reddy, A. L. M.; Yu, J.; Vajtai, R.; Ajayan, P. M. Ultrathin Planar Graphene Supercapacitors. *Nano Lett.* **2011**, 11, 1423–1427.
114. Zhu, Y.; Murali, S.; Stoller, M. D.; Ganesh, K. J.; Cai, W.; Ferreira, P. J.; Pirkle, A.; Wallace, R. M.; Cychosz, K. A.; Thommes, M.; Su, D.; Stach, E. A.; Ruoff, R. S. Carbon-Based Supercapacitors Produced by Activation of Graphene. *Science* **2011**, 332, 1537–1541.
115. Segal, M. Selling Graphene by the Ton. *Nature Nanotech.* **2009**, 4, 612–614.
116. Dikin, D. A.; Stankovich, S.; Zimney, E. J.; Piner, R. D.; Dommett, G. H. B.; Evmenenko, G.; Nguyen, S. T.; Ruoff, R. S. Preparation and Characterization of Graphene Oxide Paper. *Nature* **2007**, 448, 457–460.
117. Wang, X.; Zhi, L.; Müllen, K. Transparent, Conductive Graphene Electrodes for Dye-Sensitized Solar Cells. *Nano Lett.* **2008**, 8, 323–327.
118. Eda, G.; Lin, Y. Y.; Miller, S.; Chen, C. W.; Su, W. F.; Chhowalla, M. Transparent and Conducting Electrodes for Organic Electronics from Reduced Graphene Oxide. *Appl. Phys. Lett.* **2008**, 92, 233305.
119. Wu, J.; Becerril, H. A.; Bao, Z.; Liu, Z.; Chen, Y.; Peumans, P. Organic Solar Cells with Solution-Processed Graphene Transparent Electrodes. *Appl. Phys. Lett.* **2008**, 92, 263302.

120. Tung, V. C.; Chen, L. M.; Allen, M. J.; Wassei, J. K.; Nelson, K.; Kaner, R. B.; Yang, Y. Low-Temperature Solution Processing of Graphene-Carbon Nanotube Hybrid Materials for High-Performance Transparent Conductors. *Nano Lett.* **2009**, *9*, 1949–1955.
121. Yin, Z.; Sun, S.; Salim, T.; Wu, S.; Huang, X.; He, Q.; Lam, Y. M.; Zhang, H. Organic Photovoltaic Devices Using Highly Flexible Reduced Graphene Oxide Films as Transparent Electrodes. *ACS Nano* **2010**, *4*, 5263–5268.
122. Robinson, J. T.; Perkins, F. K.; Snow, E. S.; Wei, Z.; Sheehan, P. E. Reduced Graphene Oxide Molecular Sensors. *Nano Lett.* **2008**, *8*, 3137–3140.
123. Fowler, J. D.; Allen, M. J.; Tung, V. C.; Yang, Y.; Kaner, R. B.; Weiller, B. H. Practical Chemical Sensors from Chemically Derived Graphene. *ACS Nano* **2009**, *3*, 301–306.
124. Lu, G.; Ocola, L. E.; Chen, J. Gas Detection Using Low-Temperature Reduced Graphene Oxide Sheets. *Appl. Phys. Lett.* **2009**, *94*, 083111.
125. Lu, G.; Park, S.; Yu, K.; Ruoff, R. S.; Ocola, L. E.; Rosenmann, D.; Chen, J. Toward Practical Gas Sensing with Highly Reduced Graphene Oxide: A New Signal Processing Method To Circumvent Run-to-Run and Device-to-Device Variations. *ACS Nano* **2011**, *5*, 1154–1164.
126. Sudibya, H. G.; He, Q.; Zhang, H.; Chen, P. Electrical Detection of Metal Ions Using Field-Effect Transistors Based on Micropatterned Reduced Graphene Oxide Films. *ACS Nano* **2011**, *5*, 1990–1994.
127. Liu, Z.; Robinson, J. T.; Sun, X.; Dai, H. PEGylated Nanographene Oxide for Delivery of Water-Insoluble Cancer Drugs. *J. Am. Chem. Soc.* **2008**, *130*, 10876–10877.
128. Wilson, N. R.; Pandey, P. A.; Beanland, R.; Young, R. J.; Kinloch, I. A.; Gong, L.; Liu, Z.; Suenaga, K.; Rourke, J. P.; York, S. J.; Sloan, J. Graphene Oxide: Structural Analysis and Application as a Highly Transparent Support for Electron Microscopy. *ACS Nano*, **2009**, *3*, 2547–2556.
129. Higginbotham, A. L.; Lomeda, J. R.; Morgan, A. B.; Tour, J. M. Graphite Oxide Flame-Retardant Polymer Nanocomposites. *App. Mater. Interfac.* **2009**, *1*, 2256–2261.
130. Coleman, J. N.; Lotya, M.; O'Neill, A.; Bergin, S. D.; King, P. J.; Khan, U.; Young, K.; Gaucher, A.; De, S.; Smith, R. J.; Shvets, I. V.; Arora, S. K.; Stanton, G.; Kim, H. Y.; Lee, K.; Kim, G. T.; Duesberg, G. S.; Hallam, T.; Boland, J. J.; Wang, J. J.; Donegan, J. F.; Grunlan, J. C.; Moriarty, G.; Shmeliov, A.; Nicholls, R. J.; Perkins, J. M.; Grievson, E. M.; Theuwissen, K.; McComb, D. W.; Nellist, P. D.; Nicolosi, V. Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials. *Science* **2011**, *331*, 568–571.

Chapter 9

Atomic Layer Deposition of Dielectrics on Graphene

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Graphene, a monolayer of sp^2 bonded carbon atoms, has recently attracted widespread attention because of its unique transport and physical properties that are appealing for a wide range of electronic applications. Integration with scalable high- κ dielectrics is important for the realization of graphene-based top-gated electronic devices including field effect transistors (FETs) and new logic device concepts. These gate dielectrics are expected to be thin (2–30 nm), with minimal trapped and mobile charges that otherwise would negatively affect device performance. In addition, the dielectrics are expected to enable operation at very high frequencies (including the THz range) needed for next generation radiofrequency applications, improve the channel mobility by screening charged impurities, and reduce the high leakage currents observed in traditional silicon dioxide (SiO_2) gated devices.

This chapter will describe the status and challenges of atomic layer deposition (ALD) of high- κ dielectrics such as Al_2O_3 , HfO_2 , Ta_2O_5 , and TiO_2 . ALD, a method based on two separate self-limiting surface reactions, is the preferred technique to achieve high-quality, conformal, ultrathin dielectric films with precise thickness control at low deposition temperatures. However, the chemical inertness and hydrophobic nature of the graphene surface inhibits direct deposition of uniform thermal ALD dielectrics. Several different methods have recently been developed to render the graphene more susceptible to the ALD process including: deposition of a e-beam metal seed layer, an ozone pretreatment, a low- κ polymer seed layer, and a wet chemical pretreatment. The advantages and disadvantages of each approach are discussed. In addition other factors are discussed that play a role in high-quality deposited oxides attaining a conformal interface with graphene, such as deposition temperature and ALD cycle characteristics.

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9.1 Introduction

Graphene, a monolayer of sp^2 bonded carbon atoms is an outstanding material for electronic device applications because of its exceptional electronic and physical properties, including high intrinsic carrier (electron and hole) mobility, excellent thermal conductivity, and remarkable mechanical properties [1–4] that are appealing for a wide range of applications [5–8]. High carrier mobility combined with the integration of highly insulating films, acting as gate dielectrics in field-effect transistors (FETs), potentially enable device operation at low power and high frequencies needed for terahertz applications and analog communications. Also, it is envisioned that highly insulating films including Al_2O_3 , HfO_2 , Ta_2O_5 , TiO_2 , etc., will help overcome the limitations of current Si-based complementary metal oxide semiconductor (CMOS) technology. Successful implementation of dielectric deposition on graphene is expected to improve channel mobility by screening charged impurities and help meet scaled device designs—which require an equivalent oxide thickness of 1.0 nm and below. In addition to oxide candidates, AlN is also a suitable dielectric for epitaxial graphene (EG) due to the predicted reduced phonon scattering at the EG layer [9]. These high- κ gate dielectrics are expected to be thin (2–30 nm layers) with minimal trapped and mobile charges that would otherwise deleteriously affect device performance. Thus, high- κ dielectrics are essential for graphene-based top-gated electronics [10].

A major driving force for recent interest in atomic layer deposition (ALD) is the role it can play in scaling microelectronic devices. Following Dennard's scaling laws for MOSFETs, oxide thickness needs to be scaled at the same rate as lateral dimensions of a device; this is so that gate electrostatics are maintained even in a scaled device. But continued scaling of traditional silicon dioxide (SiO_2) led to increased gate leakage current. High- κ gate dielectrics can be thicker than SiO_2 , which results in reduced tunneling currents for the same equivalent oxide thickness [11].

ALD, a low temperature deposition method based on two separate self-limiting surface reactions, is a preferred technique to achieve high-quality, conformal, ultra-thin dielectric films with precise control of thickness and chemical composition at the atomic level [12–14]. However, the chemical inertness and hydrophobic nature of the graphene surface inhibits direct deposition of uniform ALD dielectrics. Several different methods have recently been developed to render the graphene more susceptible to the ALD process including: ozone pretreatments, wet chemical pretreatment, deposition of a low- κ polymer seed layer, deposition of e-beam metal seed layers, etc. This chapter will describe the status and challenges of various graphene functionalization methods used for uniform ALD of high- κ dielectrics including: Al_2O_3 , HfO_2 , Ta_2O_5 , and TiO_2 . The advantages and disadvantages of each approach will be discussed. In addition, other factors play a role in high-quality deposited oxides attaining a conformal interface with graphene including deposition temperature, and ALD cycle characteristics. The results will be qualified using morphological data and electrical characterization results where available.

9.2 Basic Principles of Atomic Layer Deposition

Atomic layer deposition (ALD), is a thin film deposition method with origins in the 1960s and pioneered by T. Suntola and co-workers in the 1970s [15, 16]. It is a modified chemical vapor deposition (CVD) process based on the sequential use of two separate self-limiting gas–solid surface reactions. The self-limiting reactions guarantee a surface controlled process where the amount of material deposited in each reaction cycle is constant. Thus, extremely conformal and uniform films with precise thicknesses are obtained [12, 13]. A key feature of the ALD process is that both precursors are never pulsed simultaneously, so effectively they do not see each other, which results in only surface reactions and prevents vapor phase reactions leading to parasitic CVD deposition on the substrate.

A typical ALD process uses two different reactants (commonly referred to as precursors), one for each half reaction. These precursors are selected so they are volatile at room temperature or at elevated temperatures, they do not decompose thermally in the ALD temperature window, and their reactions are self terminating [14]. The ALD temperature window refers to the temperature interval where true layer-by-layer ALD processes take place, i.e., where the deposition rate per ALD cycle is constant [16, 17]. It is essential that the deposition rate is constant in this regime in order to minimize gas phase reactions and accurately control ultrathin film thicknesses. Atomic layer deposition is, typically, a low temperature process where most saturating reactions take place at temperatures below about 400°C. For given precursors however, regions of constant deposition (Å/cycle) can be quite narrow, ~50–100°C.

An ALD cycle uses two precursors and consists of four basic sequential steps: an exposure of the first precursor, a purging step, an exposure of the second precursor and another purging step. A schematic representation of one ALD cycle using trimethylaluminum ($\text{Al}(\text{CH}_3)_3$, TMA) and H_2O precursors is shown in Fig. 9.1a. Details about each step are as follows:

1. Initially, a metal precursor (TMA) is exposed so that it reacts with a pre-existing species (O–H-terminated bonds adsorbed on the surface) on the solid surface. During this first reaction, Al atoms (which will form part of the ALD film) are adsorbed on the surface until all O–H-active sites have reacted with TMA, thus, achieving saturation. At this point, the surface has a CH_3 termination and no further reactions with TMA can take place.
2. The first purging step (using N_2 , Ar) removes un-reacted TMA and methane gas (CH_4) which is a reaction by-product, and retains the CH_3 -terminated surface.
3. The CH_3 -terminated surface is exposed to the second precursor H_2O . This reaction will convert methyl groups (CH_3) to methane (CH_4), and will leave an O–H-terminated surface. After H_2O has reacted with all the available CH_3 , the reaction achieves saturation and the O–H-terminated surface prevents any further reactions with H_2O .
4. The second purging step removes un-reacted H_2O precursor and methane by-products, and the newly O–H-terminated surface is ready for the next TMA pulse.

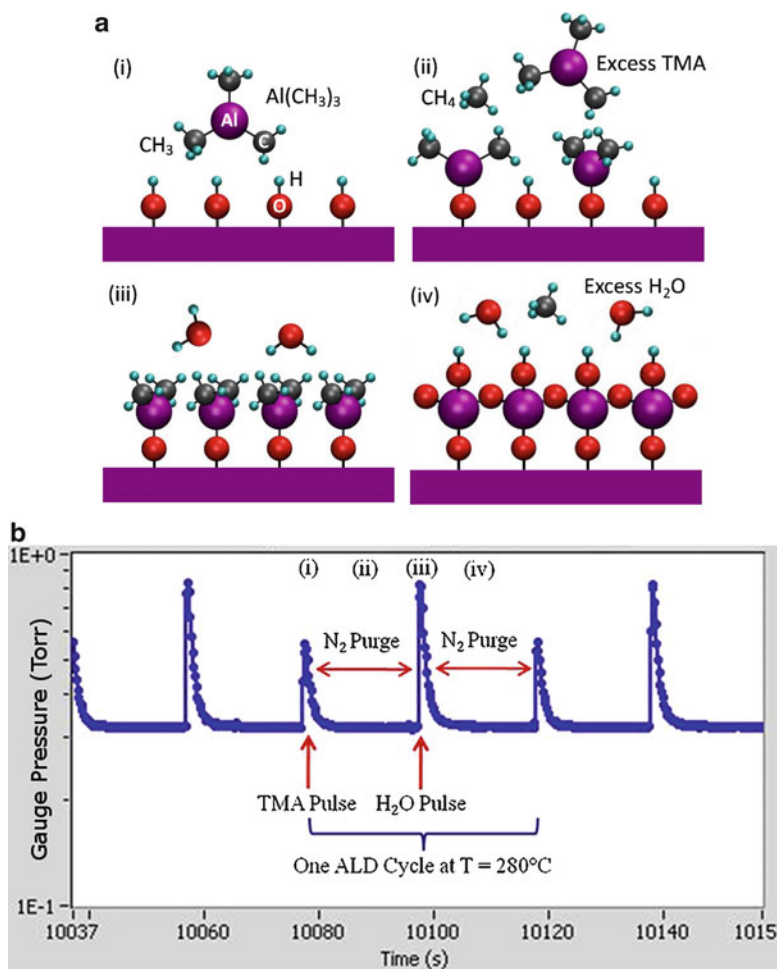
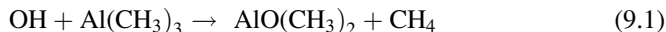


Fig. 9.1 (a) Cartoon rendition of an ALD cycle using TMA/ H_2O precursors. (b) Schematic representation of an ALD cycle

The half-reactions can be presented as follows:



Ideally, each ALD reaction cycle adds a given amount of material to the surface, referred to as the growth per cycle, and the surface will return to its pre-cycle state, albeit slightly thicker. Therefore, to grow a film of desired thickness, one only needs to repeat the sequence as many times as necessary.

Deposition rate generally averages between 0.1 and several Å per ALD cycle, and is dependent on deposition temperature and precursor chemistries. Depending on the precursors used, exposure times are usually in the millisecond range whereas purging times can take up to several seconds. During purging, removal of unreacted precursors and gaseous by-products takes place, along with removal of unwanted impurities such as carbon. In many ALD processes, the purging gas is constantly flowing and used as a precursor carrier gas as well.

Currently many ALD reactor configurations exist, including commercial as well as homemade. Each reactor is unique and deposition conditions for one system do not necessarily produce identical films in other. It is thus up to the end user to optimize appropriate ALD deposition parameters including temperature, pulse duration, and purging times.

An example is shown by the schematic in Fig. 9.1b. It represents Al_2O_3 ALD using TMA/ H_2O , obtained from a commercially available Cambridge Nanotech Savannah 200 thermal ALD system. The numerals indicate the reaction steps described by the chemistry in Fig. 9.1a. This example shows a complete ALD cycle with the following pulse and purge sequences: TMA pulse 15 ms, TMA purge 20 s, H_2O pulse 15 ms, H_2O purge 20 s. Note that the base pressure is ~ 0.3 Torr at a N_2 flow of 20 standard cubic centimeters per minute (sccm), and it peaks to ~ 1.0 Torr during pulsing. These are typical conditions for thermal ALD where the change in pressure during pulsing is determined by the partial pressures of the reactive precursors.

In summary, ALD offers the advantages of atomic level precision of film growth, excellent conformality and large area coverage. Film thicknesses are easily controlled by the number of reaction cycles and deposition temperatures $< 400^\circ\text{C}$ are generally used. A wide range of precursor materials is available for ALD with very low impurity content. One drawback of ALD is its slow deposition rate, generally limited to a fraction of a monolayer per cycle. However, for microelectronic applications where high- κ gate oxides are needed, the required thicknesses are expected to scale down to 10 nm or less, and the slow deposition rate of ALD is not a decisive factor.

The preceding section is only intended to motivate and introduce the reader to the general principles of ALD and by no means is an exhaustive account of the technique. For in-depth reviews of ALD and the chemistry of ALD processes, the reader is referred to the excellent reviews by Suntola [12], George [13], Ritala and Leskelä [18], Ritala [19], Puurunen [14], and Seidel [17], to mention just a few. In particular the review article by Puurunen presents a detailed case study of the classical thermal ALD of Al_2O_3 via TMA/ H_2O precursors.

9.3 Graphene Functionalization for Uniform ALD

Direct deposition of dielectric oxides on pristine or non-functionalized graphene sheets, using H_2O -based precursors, is hindered by the highly hydrophobic and chemically inert nature of graphene. Efforts in ALD on exfoliated graphene

has not yielded direct deposition on defect-free pristine exfoliated graphene [20]. On highly-oriented pyrolytic graphite (HOPG), as well as EG, ALD resulted in non-uniform coverage [21–23]. On exfoliated graphene and HOPG, ALD results in selective growth at step edges and defects, where broken dangling bonds are believed to serve as nucleation sites for deposition [24]. For ALD on EG, preferential nucleation on terraces has been reported yet enhanced nucleation along step edges is problematic [22, 23].

To render the graphene surface more suitable to oxide precursor bonding and/or to create a functionalized layer that will promote uniform deposition, several different surface preparation approaches have been investigated. Some of these approaches include: wet chemical treatments [23, 25]; ozone (O_3) or nitrous oxide (NO_2) surface treatments of EG or HOPG [22, 26, 27]; initial ALD pulse sequencing of NO_2 -TMA [28]; oxidation of electron beam (e-beam) evaporated metallic seed layers [29, 30]; and spin-coating of a buffered low- κ dielectric-seeding polymer [7, 31]. Additional functionalization methods for uniform dielectric deposition were also described by Liao et al. [10]. Not all these functionalization strategies resulted in complete dielectric coverage and in some instances degradation of electronic properties of the underlying graphene was observed. For the covalent functionalization of the graphene basal plane, it is necessary to alter the surface by breaking sp^2 bonds to form sp^3 bonds [32]; however, these broken lattice sites can lead to significant degradation in carrier mobility. Therefore, there remains a need to develop viable, reproducible methods to deposit high-quality, high- κ dielectrics on large area graphene while maintaining large intrinsic carrier mobilities and low interface trap densities.

9.3.1 Direct Deposition of Dielectrics Via ALD on Graphene

Uniform oxide deposition on graphene by ALD is quite challenging due to the chemical inertness and lack of dangling bonds normal to the basal plane of graphene [33]. To this end, direct ALD of high- κ oxide layers on graphene surfaces using H_2O -based precursors results in either no coverage or non-uniform coverage [20–24]. Xinran et al. [20] have shown that ALD of metal oxides gives no direct deposition on the basal plane of defect-free pristine exfoliated graphene due to absence of surface functional groups, necessary for reaction with the ALD precursors. In contrast, a partial Al_2O_3 coverage of graphene sheets near the step edges was observed; dangling bonds or OH-terminated edges are believed to exist at step edges. This situation is illustrated in the atomic force microscopy (AFM) images of Fig. 9.2, where Al_2O_3 preferentially grows on graphene edges and around defect sites.

Xuan et al. [24], were able to deposit 1–35 nm Al_2O_3 and HfO_2 on HOPG using TMA, $HfCl_4$ and H_2O precursors at a range of temperatures from 200°C to 300°C. Although uniform gate dielectrics were not achieved, highly conformal and uniform oxide nanoribbons several nanometre (5–200) wide, ~1.5 nm high, and with lengths in excess of >50 μm were formed. Again, these nanostructures grew

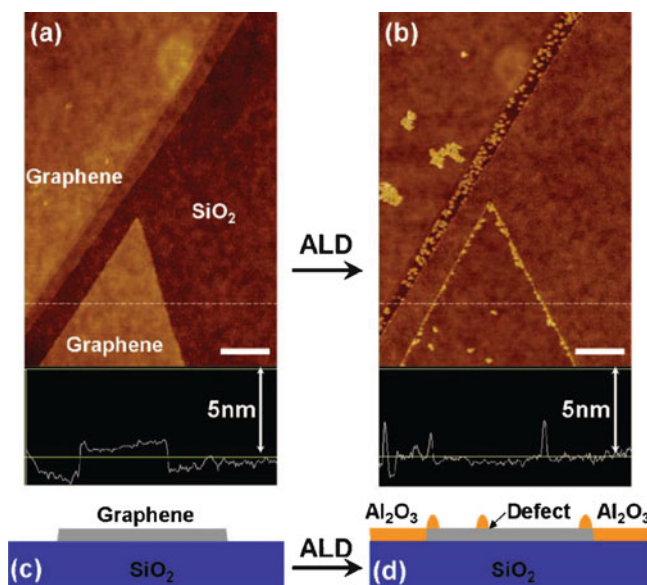


Fig. 9.2 ALD of Al₂O₃ on pristine graphene. (a) AFM image of graphene on SiO₂ before ALD. The height of the triangular shaped graphene is ~1.7 nm as shown in the height profile along the dashed line cut. Scale bar is 200 nm. (b) AFM image of the same area as (a) after ~2 nm Al₂O₃ ALD deposition. The height of the triangular shaped graphene becomes ~0.3 nm as shown in the height profile along the dashed line cut. Scale bar is 200 nm. (c and d) Schematics of graphene on SiO₂ before and after ALD. The Al₂O₃ grows preferentially on graphene edge and defect sites (Reproduced with permission from [20]. © 2008 American Chemical Society)

exclusively along the atomically sharp step edges between broken graphene layers. Figure 9.3 is an SEM micrograph illustrating the results of various ALD depositions under different conditions. Only within the correct ALD window were dielectric nanoribbons deposited (see plots (a), (b), and (d)), whereas very rough and discontinuous films were obtained otherwise. These experiments provide evidence that direct ALD using H₂O-based processes on atomically flat HOPG, are not suitable for producing continuous and uniform two-dimensional oxide films. On the other hand, the atomically sharp edges on graphene serve as one-dimensional (1D) nucleation sites for ALD processes [24].

In a separate deposition study of Al₂O₃ by ALD on HOPG, Speck et al. [22] found randomly distributed wire-like formations having very dense coverage. Their vertical growth rate was about 1 Å/cycle, but laterally, the wires did not coalesce to form continuous 2D films as observed in [24]. This discrepancy was not further investigated as it could be merely related to the quality and number of layers of the starting HOPG and not the ALD process. Their deposition results are presented in the AFM images of Fig. 9.4.

Also, on mechanically exfoliated graphene, Zou et al. [34] demonstrated ~30 nm thick HfO₂ deposited by ALD at 110°C. Their films are continuous and smooth across the graphene/SiO₂ step. On single layer graphene, pinhole-free films with

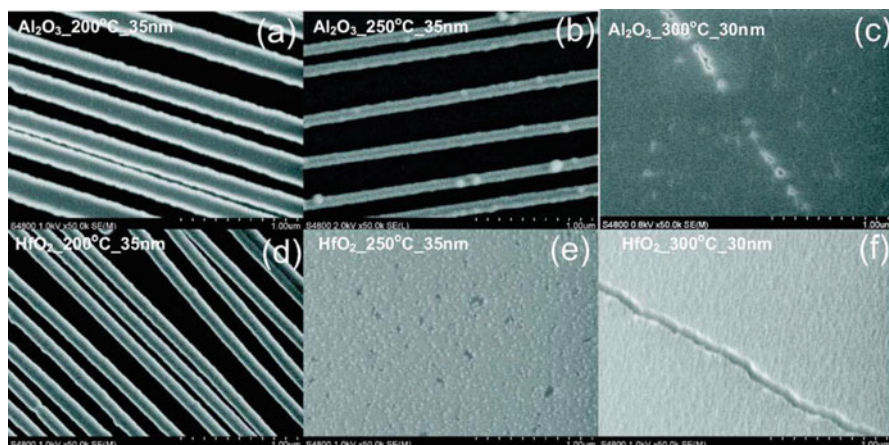


Fig. 9.3 SEM images of high-quality nanoribbons are shown in (a), (b), and (d) on HOPG surface, while very rough and discontinuous films are formed out of ALD process window, as shown in (c), (e), and (f); process conditions are contained in each image (Reproduced with permission from [24]. © 2008 American Institute of Physics)

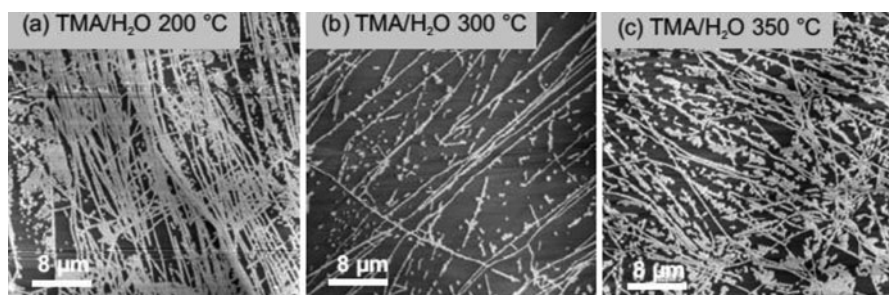


Fig. 9.4 AFM images of ALD Al_2O_3 films on HOPG. (a)–(c) 500 cycles TMA/water at different temperatures (Reproduced with permission from [22]. © 2010 Wiley)

good morphology were obtained for thicknesses >10 nm. On multilayer (5–6 layers) graphene however, the coverage and uniformity are less ideal. The authors speculate that the curvature induced by the SiO_2 in single layer graphene facilitates adsorption and reaction of the ALD precursors. The dielectric constant of the HfO_2 films on graphene field effect transistors was ~ 17 , substantially lower than ideal ($\kappa = 25$) [35], and the Dirac voltage (V_{Dirac}) was within ± 20 V. Transistor field effect mobilities in excess of $6000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were also observed.

In stark contrast to ALD on exfoliated graphene and HOPG, thermal ALD of Al_2O_3 on graphene grown by Si sublimation of SiC, EG [36–38], shows preferential nucleation on terraces and occasional nucleation along step edges [22, 23]. Figure 9.5 shows AFM results of various TMA/ H_2O ALD cycles, where (a) corresponds to 100 ALD cycles on Si-face EG at 225°C , and (b) corresponds to a

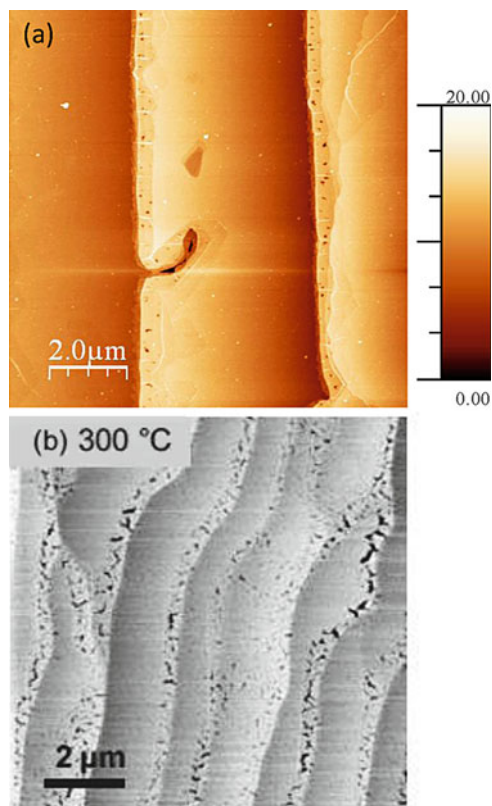


Fig. 9.5 AFM images of EG surfaces after (a) 250 cycles ALD at 225°C and (b) 500 cycles ALD at 300°C. Both samples were deposited with TMA/water based processes (Reproduced with permission from [22]. © 2010 Wiley)

much thicker film at 500 ALD cycles. Clearly, the EG films follow the morphology of the underlying SiC substrate, with large terraces delineated by step edges in between the terraces. Regardless of the oxide thickness, nucleation takes place preferentially on the terraces, whereas near step edges, extensive areas of missing oxide are evident. We have observed this deposition behavior quite often on various Si-face and C-face EG samples, independently of the ALD deposition temperature, as was also indicated by Speck et al. [22]. Areas of hindered oxide nucleation are believed to be related to bilayer graphene originating at the step edges of SiC [22].

A very interesting experiment was performed by Jernigan et al. [39], where a Si-face EG was subjected to a 1300°C H₂ anneal in ultra high vacuum (UHV) for 30 min, after which, thermal ALD of Al₂O₃ was deposited. The AFM image before H₂ anneal, displayed in Fig. 9.6a, shows an EG surface with many ridges and steps across terraces as well as macro steps. Figure 9.6b shows an SEM image of the

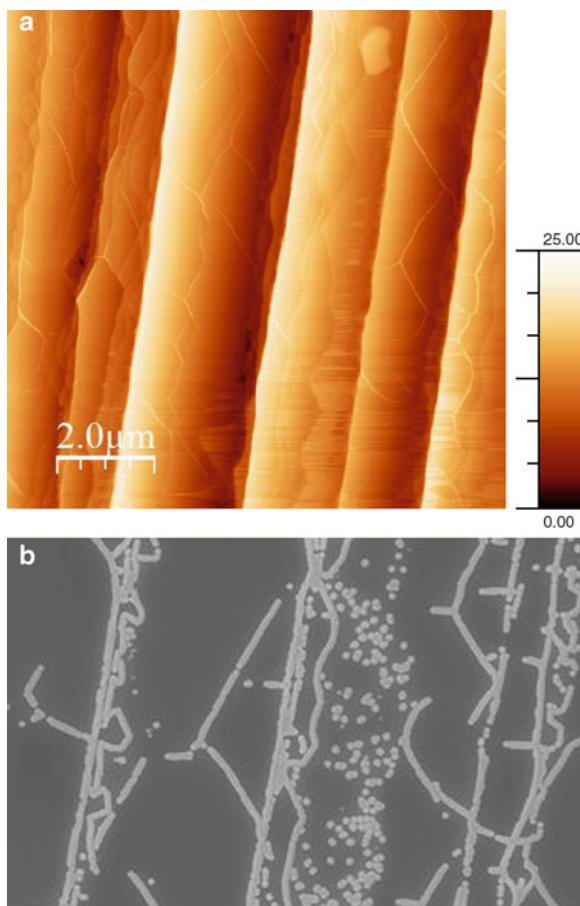


Fig. 9.6 (a) AFM image of EG before H_2 anneal and ALD. Many ridges and steps across terraces as well as step bunches are visible. (b) SEM image of the $\text{Al}_2\text{O}_3/\text{EG}/\text{SiC}$ after H_2 anneal and 260 cycles Al_2O_3 deposition (~ 300 Å) at 225°C . Deposition only occurs on step bunched edges and ridges

$\text{Al}_2\text{O}_3/\text{EG}/\text{SiC}$ after H_2 anneal and 260 cycles Al_2O_3 deposition (~ 300 Å) at 225°C . Contrary to expectations from previous experience of ALD on as-grown EG, the resulting oxide is primarily deposited along the step edges and on ridges (point defects), but not on the clean terraces. These deposition results are in agreement with those of thermal Al_2O_3 ALD on pristine exfoliated graphene [20]. From X-ray photoelectron spectroscopy (XPS) analysis of the EG after annealing (before ALD), there was a complete removal of oxide adsorbed species, and a significant reduction of excess carbon. Therefore, it is likely that the observed ALD nucleation on EG after the UHV anneal treatment takes place at the more reactive step edges, and at

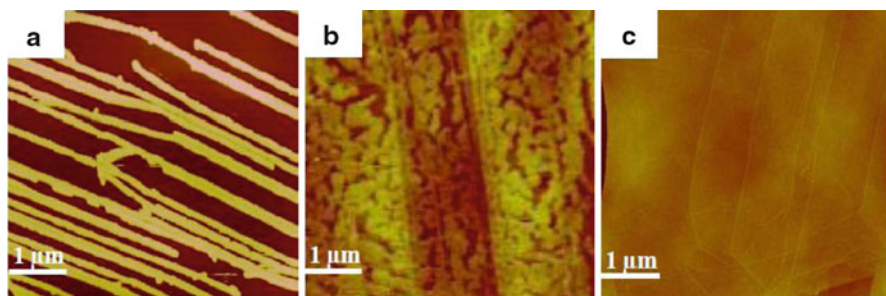


Fig. 9.7 (a) AFM image of the sample with Al_2O_3 layer deposited from TMA/ H_2O process (200 cycles) at 200°C . (b) Al_2O_3 layer from TMA/ O_3 process (50 cycles) on the fresh HOPG surface at 200°C . (c) Al_2O_3 layer from TMA/ O_3 process (50 cycles) on the ozone-treated HOPG surface at 200°C (Reproduced with permission from [26]. © 2009 Electrochemical Society)

defects and impurities not removed by the H_2 anneal. These results demonstrate that EG has a similar thermal ALD behavior to that of exfoliated graphene when elaborate cleaning is performed on the as-grown EG surface.

In summary, because of dangling carbon bonds, graphene edges have much higher chemical reactivity than the inert basal planes, and therefore H_2O precursors are preferentially adsorbed at the edges, creating a nucleation site for ALD films. However, on the terraces, nucleation happens only at defect sites and impurities, making it very difficult to nucleate on pristine graphene and to achieve uniform, 2D coalesced oxide films. Such irregularities in oxide surface coverage from deposition to deposition have prompted researchers to develop suitable, reproducible surface functionalization treatments before oxide depositions.

9.3.2 Ozone or NO_2 Treatments

A functionalization approach using ozone (O_3) pretreatment of HOPG followed by an ALD process with TMA/ O_3 was studied by Lee et al. [21]. It was found that an O_3 pretreatment could act as an initiator for uniform deposition of the high- κ dielectric on graphene. A starting experiment consisted of direct deposition of 50 cycles Al_2O_3 on HOPG from TMA/ O_3 . Compared to similar depositions using TMA/ H_2O processes, the obtained films nucleated not only at step edges but also on terraces. The total thickness was 4–5 nm, indicating a vertical growth rate well within the expected ALD deposition rates (~ 0.1 nm/cycle). Though enhanced nucleation was clearly observed with the TMA/ O_3 process, completely coalesced films were not achieved, see for instance Fig. 9.1c of [21].

Successful attempts to increase the number of nucleation sites on the basal plane were achieved by exposing the HOPG surface to an ozone treatment prior to Al_2O_3 deposition. A 10 s ozone (22 wt%) pretreatment of HOPG followed by <10 nm of Al_2O_3 via TMA/ O_3 resulted in a conformal and uniform oxide film as seen in the AFM image of Fig. 9.7c [26]. The figure shows the evolution of (a) direct

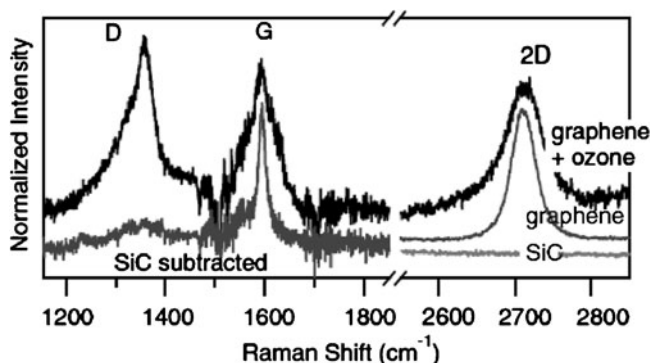


Fig. 9.8 Raman spectra of pristine EG before and after exposure to 20 ozone pulses at 350°C. Spectra are after the SiC substrate contribution was subtracted, and normalized to the G peak maximum and offset for clarity (Reproduced with permission from [22]. © 2010 Wiley)

deposition by a TMA/H₂O process, (b) direct deposition by TMA/O₃ process, and (c) deposition by TMA/O₃ process on an ozone-treated HOPG, respectively. Figure 9.7c clearly shows an almost ideal 2D growth mode with very little surface roughness, rms ~0.2 nm. These results suggest that an O₃ pretreatment followed by an ALD process would modify the HOPG surface rendering it more susceptible to oxide deposition and lead to conformal layer-by-layer growth. It has been argued in [21] that this functionalization occurs mainly through an increase in the concentration of epoxide functional groups after the ALD Al₂O₃. Moreover, XPS and Raman spectroscopy results show little or no defect population, supporting the claim that the O₃ pretreatment does not seem to significantly disturb the *sp*² arrangement or have any etching effects on graphene [21]. The thickness, shown to be conformal, was <10 nm suggesting it is possible to deposit thinner dielectrics on graphene for realistic top gate applications. *C*–*V* measurements performed on a metal/10 nm Al₂O₃/HOPG stack yielded an effective dielectric constant of ~9, which is ideal [35]. However, there are still significant amounts of leakage current ($\sim 3.4 \times 10^{-8}$ A cm⁻² at -1 V) in these devices suggesting that there is a non-uniform oxide film or imperfections at the graphene/oxide interface.

On HOPG, Speck et al. [22], demonstrated a homogeneous and conformal, albeit rather thick (~50 nm) Al₂O₃ film deposited with TMA/ozone at 350°C, see Fig. 9.1d of [22]. Their results differ somewhat with those of Lee's on HOPG in that they did not use an ozone pretreatment of the graphene prior to ALD but still were able to obtain a pinhole-free oxide as shown by AFM. Additional XPS and Raman spectroscopy experiments were performed on EG treated with ozone before and after ALD. These results showed that a number of defects are created by the ozone, as well as some etching of the EG. Degradation of the structural integrity of the EG is confirmed by the Raman results presented in Fig. 9.8, where an increase in the D peak along with a severe broadening of the G peak due to ozone exposure are evident. The EG damage introduced by the ozone pretreatment can be reduced by

lowering the exposure temperature and by reducing the number of ozone pulses prior to oxide deposition, while still providing enough nucleation sites for ALD growth. However, a substantial increase in graphene electrical resistance is still observed under all conditions.

Lin et al. [40] opted for a different graphene functionalization approach involving deposition of 50 cycles of NO_2 -TMA prior to growth of the gate oxide by ALD [27, 41]. In their approach, exfoliated graphene on a highly resistive Si substrate on a 300 nm SiO_2 layer is fabricated into a top-gated graphene field effect transistor. A functionalization layer consisting of 50 ALD cycles of NO_2 -TMA was initially deposited to promote a gate dielectric without pinholes. The top gate insulator consisted of ~ 12 nm Al_2O_3 deposited at 250°C and its dielectric constant determined from C - V measurements was ~ 7.5 . These devices showed ideal $1/f$ frequency dependence, characteristic of FET-like behavior, but both device conductance and field-effect mobility were significantly reduced after ALD deposition. It was suggested that the conductance and mobility degradation could be associated with the NO_2 functionalization and interface phonon scattering in the oxide [42]; a maximum cut off frequency of 26 GHz was achieved for a 150 nm gate length.

Gas phase functionalization allows for uniform deposition of thermal ALD on graphene. However, electrical results are limited and should be investigated further to determine the viability of such processes in top-gated graphene technologies.

9.3.3 Wet Chemistry Approaches

Pirkle et al. [25] used a wet chemistry functionalization approach consisting of immersing exfoliated HOPG samples in DI water (DIW) at room temperature for 1 h to facilitate ALD nucleation. Instead of water-based ALD Al_2O_3 , ozone was used as the oxygen precursor, but deposition was carried out at a lower temperature (30°C) to prevent etching of graphene and degradation of device properties. The oxides produced at lower temperature are known to be of lower quality, but they may very well serve as seeding layers for subsequent high-quality high- κ dielectric deposition under different conditions. This study also investigated samples exposed to the DI water treatment with ALD done at 200°C . XPS results show various C 1s states at 285, 287, and 290 eV, after ALD at 30°C and 200°C , associated with amorphous carbon [43], methoxy groups [44], and carbonate [45] or formate groups [46], respectively. All these impurities can degrade the quality of the oxide, resulting in poorer performing devices; however no electrical data was provided. AFM results confirm the oxide deposition coverage for samples deposited at 30°C and 200°C to be 75% and 55%, respectively. Better deposition was achieved at the lower temperature for DIW-treated samples, however, the coverage was not uniform and had lots of holes (see Fig. 9.3 of [25] for a comparison of AFM results of the various surface preparations). As discussed by Pirkle, deposition at the

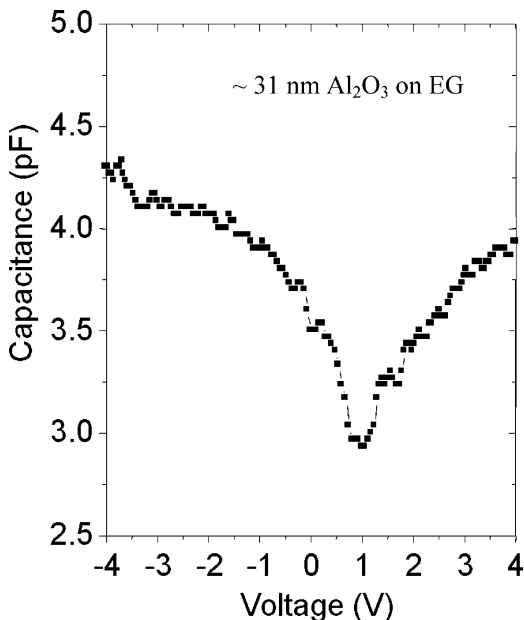
lower temperature is accompanied by incomplete reactions of methoxy and carbonate groups leading to incorporation of impurities in the dielectric; but even at higher deposition temperatures, adsorbed species are observed within the Al_2O_3 .

The authors of this chapter also developed a wet chemistry treatment to modify the EG surface prior to thermal ALD of Al_2O_3 [23]. This surface modification approach offers a simple, yet reliable way to alter the graphene bonding without compromising the electrical or structural properties. EG was first exposed to a diluted hydrofluoric acid (HF, 1:1) for 1–2 min., and then rinsed with DI water. This preparation step is expected to remove impurities and any oxides from the graphene surface. Next, the samples were exposed to an SC1 solution consisting of 1 part NH_4O_4 , 1 part H_2O_2 , and 5 parts 18.2 M Ω cm DI water at 80°C for 5–10 min. Exposure to SC1 promoted an O-H terminated surface with many available hydroxyl groups necessary for nucleating thermal ALD. The samples were rinsed with DIW and blown dry with N_2 before being placed in the reaction chamber for ALD growth of 250 cycles of Al_2O_3 (~31 nm). This sample shows morphology similar to that before ALD deposition. The rms roughness of the sample before and after the oxide deposition was 1.16 and 1.13 nm, respectively, implying the ALD did not impact this parameter. Since XPS verified the presence of Al_2O_3 , the AFM image indicates conformal oxide coverage on both terraces and step edges without the presence of significant pinholes. SEM imaging confirms the AFM results on a larger scale (~80 μm^2). It indicates a uniform, continuous film across step edges and terraces, without interruptions. These results were reproducible in subsequent experiments under identical conditions.

Chemical analysis of the oxide was obtained from XPS peak positions and peak areas for the O 1s, Al 2p, and C 1s photoelectrons. Analysis of the data indicates a nearly stoichiometric Al_2O_3 with an O/Al ratio of 1.57, comparable to XPS spectra taken of a single crystal sapphire standard. The O 1s has a slight asymmetry and deconvolution of the peak reveals two distinct components, one centered about 532.2 eV participating in Al–O bonding and one shifted toward higher energy at 533.9 eV associated with Al–O–H hydroxyl groups resulting from the ALD process with TMA/ H_2O [47, 48]. The Al 2p is a single symmetric line centered about 75.38 eV. The C 1s spectrum is a very small peak near 283.2 eV and is most likely residual carbon from incomplete precursor reactions within or near the surface of the dielectric. Although the O/Al ratio and presence of hydroxyl groups indicate a slight O enrichment in the oxide, the narrow full-width at half maximum of the O 1s (1.93 eV) and Al 2p (1.6 eV) peaks as well as the small amount of residual carbon in the film are indicative of a high quality oxide.

More importantly from a device stand point, the Hall mobility of the Al_2O_3 /EG sample was not significantly affected by either the pre-deposition treatment or the Al_2O_3 deposition, and only a small change was observed from ~550 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ before ALD to ~600 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ after ALD. It has been argued that electrical measurements are a highly sensitive indicator of minute changes in the quality of the EG, whereas techniques such as Raman spectroscopy are used to evaluate larger scale variations [49]. Since carrier mobility of the sample was maintained, this implies that the graphene structure is not significantly deteriorated by the surface

Fig. 9.9 C - V measurement at 1 MHz from a 50- μm -diameter Ti/Au circular capacitor patterned on top of the Al_2O_3 /EG/SiC. From the measured dielectric thickness a ~ 7.6 dielectric constant was extracted. The Dirac voltage shift is ~ 1 V



treatment and the oxide deposition. The C - V measurement shown in Fig. 9.9 resulted in a $V_{\text{Dirac}} \sim 1.0$ V. Using the measured 31 nm dielectric thickness, a dielectric constant of ~ 7.6 was extracted. The lower dielectric constant could be the result of hydroxides and carbon trapped within the oxide. Also, fixed charge in the substrate, in the oxide, or at the graphene-substrate/graphene-oxide interface can result in a shifted V_{Dirac} .

Wet chemical treatments are a simple viable alternative for graphene surface modification without major disruptions of the structural and electrical properties. The deposited oxides show excellent uniformity over large areas and minimal impurity incorporation. More studies exploring device characteristics are necessary to assess the quality of the dielectrics.

9.3.4 Polymer Buffer Layer

Another method explored to obtain uniform high- κ dielectric films on graphene involves the use of a low- κ polymer buffer layer. Two different polymer studies have been conducted on exfoliated graphene sheets transferred to SiO_2/Si substrates. Each one will be examined in depth below.

Since ALD of high- κ dielectrics cannot achieve uniformity on pristine graphene, Wang et al. [20] explored the use of 3,4,9,10-perylene tetracarboxylic acid (PTCA) as a seed layer for conformal Al_2O_3 films. PTCA is an ideal candidate since it is a planar, conjugate ring system with negatively charged terminal carboxylates that

provide suitable reaction sites for ALD. Exfoliated graphene on SiO_2 was annealed at 600°C in a 1 Torr argon environment to clean the surface prior to soaking the sample in PTCA for ~ 30 min. and immediately loading into the ALD chamber. Al_2O_3 films deposited at 100°C were ~ 2 nm thick. It was determined that the PTCA film was $0.5\text{--}0.8$ nm thick, yielding an overall stack thickness $\sim 2.8 \pm 0.2$ nm.

AFM was used to determine the morphology of the $\text{Al}_2\text{O}_3/\text{PTCA}$ stack (~ 2 nm Al_2O_3 ALD). These films were found to be extremely smooth, resulting in a mean roughness of only ~ 0.33 nm over a $5\text{ }\mu\text{m}^2$ region. The highly favorable separation of PTCA from methanol creates a dense uniform coating across the graphene surface, which in turn is responsible for the uniform Al_2O_3 films deposited. It is expected that the electrical properties will not be degraded by this process but no electrical characterization was performed on these films.

Farmer et al. [7], attained good graphene transistor performance using NFC 1400-3CP (JSR Micro, Inc.), a low- κ polymer buffer prior to ALD of HfO_2 . This particular polymer contains methyl and hydroxyl groups which act as ideal reaction sites for subsequent ALD. By diluting NFC in propylene glycol monomethyl ether acetate (PGMEA), it can be easily spin-coated onto the graphene surface. The thickness and uniformity of the polymer buffer layer can be controlled by adjusting the dilution and spin speed. It was found that a 24:1 dilution of PGMEA/NFC, spun at 4000 rpm for 60 s, results in a continuous 10 nm buffer layer. A curing step was performed at 175°C for 5 min. to remove any residual solvent and then, 10 nm of HfO_2 was deposited to complete the dielectric stack.

Although the specific morphology of the dielectric stack was not discussed, it is assumed that the HfO_2/NFC must coat the entire gated area of the graphene channel to obtain the transistor characteristics presented. From capacitance measurements the NFC buffer layer and the HfO_2 film were determined to have dielectric constants of $\kappa = 2.4$ and 13, respectively. Though the dielectric constant of the HfO_2 film is significantly less than the ideal, it is still sufficiently high for the applications being explored.

The graphene V_{Dirac} was found to greatly shift with each part of the dielectric stack as can be seen in Fig. 9.10. Exfoliated flakes on 300 nm of SiO_2/Si exhibited a slight n-type doping with the $V_{\text{Dirac}} = -3.5$ V. After the low- κ polymer was spun on, V_{Dirac} is 42.5 V indicating a significant shift due to high p-type doping of the graphene by the polymer. The deposition of HfO_2 compensated for some of this p-type doping resulting in a $V_{\text{Dirac}} = 13.25$ V. This large shift creates a problem in modulating the devices and V_{Dirac} should be as close to 0 V as possible. Only by exposing the dielectric/graphene stack to an O_2 plasma, known to etch graphene, Farmer and co-workers were able to obtain a reasonable low Dirac voltage ($V_{\text{Dirac}} = 5.75$ V) sufficient for operation of these graphene transistors. In addition, the graphene mobility was only reduced by $\sim 15\%$ from before to after processing. It is interesting to note that Farmer found a linear dependence of field-effect mobility on temperature. This indicates phonon scattering is the dominant scattering process in these devices, which is in contrast to alternative dielectrics and surface preparations where charge impurities dominate the scattering process.

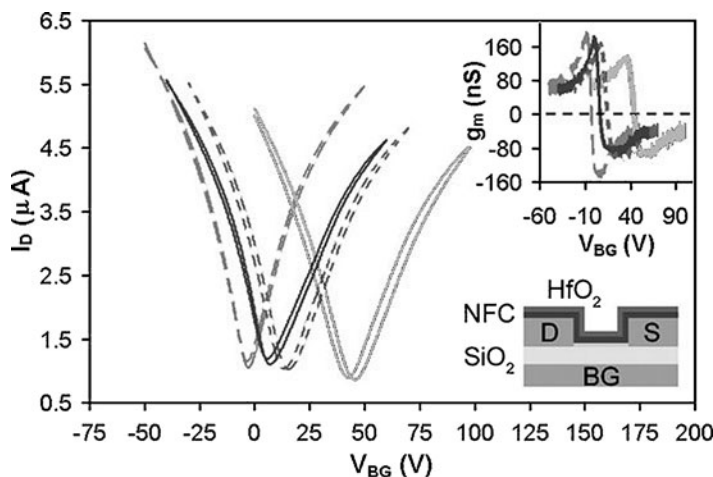


Fig. 9.10 Two-point back-gated measurements of graphene flakes. (a) Transfer characteristics and corresponding transconductances (*inset*) after the different stages of buffered dielectric processing: before processing (*long-dashed*), after NFC polymer deposition (*gray*), after HfO_2 deposition (*dashed*), and after 50 W O_2 plasma treatment for 30 s (*dark*). The schematic shows the completed device configuration (Reproduced with permission from [7]. © 2009 American Chemical Society)

The studies above show that a low- κ polymer buffer layer can successfully be used to obtain uniform, conformal high- κ dielectric films on graphene. Electrically, these polymers have a tendency to highly dope the graphene film, creating large shifts in the Dirac voltage and limiting the usefulness of these layers in devices. Only through annealing in an O_2 plasma was V_{Dirac} reduced. In addition, mobility is still slightly degraded by these films and leaves room for improvement in overall device performance.

9.3.5 Metal Seed Layers

Fully oxidized metal seed layers have been used as a method to nucleate ALD on graphene and to address the degradation in mobility that accompanied other methods.

In 2009, Kim et al. [50] was the first to introduce a thin nucleation layer of fully oxidized metal between the exfoliated graphene and dielectric film. This initial investigation deposited 15 nm ALD Al_2O_3 films on a fully oxidized Al metal seed layer. Since metal contacts were defined before depositing the top gate dielectric, the graphene was annealed in a hydrogen atmosphere at 200°C to remove any excess resist or residue prior to depositing a metal seed for ALD. A thin 1–2 nm Al metal seed layer was deposited using electron beam (e-beam) evaporation. The Al/graphene stack was then exposed to air during transfer to the ALD chamber.

XPS confirmed the air transfer resulted in a fully oxidized metal seed layer, but an additional H₂O oxidizing cycle at elevated temperatures was carried out in the ALD chamber to ensure complete oxidation.

Electrical characterization of these devices back-gated with SiO₂ and top-gated with Al₂O₃ yielded a V_{Dirac} of 0.08 V. This shows there is little unintentional doping of the graphene layer by the top-gate dielectric stack. In addition, the leakage current through the Al₂O₃ top-gate was $<0.75 \text{ pA } \mu\text{m}^{-2}$, and implies a high quality dielectric film. However, the relative dielectric constant of the Al₂O₃ layer was only 6.0, which is significantly lower than the ideal value. By fitting the transport data to a model the authors developed, an effective mobility $\mu = 8600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was extracted, at a carrier concentration of $n_0 = 2.3 \times 10^{11} \text{ cm}^{-2}$. Although no comparison was made with exfoliated graphene devices without the Al₂O₃ films, this high mobility value obtained after processing does validate the use of metal seeds for ALD on graphene. Finally, carrier mobility was insensitive to temperature, suggesting that charge impurities are the dominant scattering process in these devices.

An *in situ* XPS study, by Pirkle et al. [29], was conducted on high- κ Al₂O₃ and HfO₂ films prepared using metal seed layers. The metal seeds used were Al for the Al₂O₃ films and Hf for the HfO₂ films. The effects of a pre-deposition vacuum anneal (500°C for 30 min in UHV) on the evolution of the dielectric/metal seed/graphene stack was also investigated. In this experiment, $\sim 1 \text{ nm}$ of metal was deposited by e-beam evaporation and oxidized in a cluster chamber with high-purity dry O₂ at 200°C.

The Al layer deposited on an annealed surface still had some metallic Al after oxidization, while deposition on non-annealed surfaces resulted in fully oxidized Al layers. In addition, AFM images showed non-uniform Al clusters for both surface types with heights as large as 10 nm. XPS spectra verify that there were no changes in bonding states of the C1s peak, thus indicating no detectable covalent bonding with the graphene substrate. The lack of Al–C bonds also implies that the graphene lattice remains undisturbed by the seeding method, and therefore a significant degradation in mobility is not expected (though not explored in this study).

The Hf seed layers were found to form a carbide (HfC) when a predeposition anneal was not performed. This carbide is formed at the expense of sp^2 bonding in the graphene lattice and should result in substantial reductions in mobility. However, by annealing the sample in H₂ prior to metal deposition this carbide can be prevented and a fully oxidized Hf seed layer can be produced. Unlike the Al₂O₃ films, the HfO₂ films were much smoother and exhibited no clustering, which may imply that this is a better dielectric for graphene.

A more exhaustive study of this seeding method was done by Robinson et al. [30], and included high- κ Al₂O₃, HfO₂, Ta₂O₅, and TiO₂ films on epitaxial graphene. This work also explored the effect of dielectric deposition temperature on obtaining uniform films with and without the nucleation layer. Without the metal seed, non-uniform coverage was found for all of the oxides examined at all temperatures up to 300°C. However, as seen in Fig. 9.11, although film uniformity and coverage improved for Al₂O₃ as deposition temperatures increased from 150°C

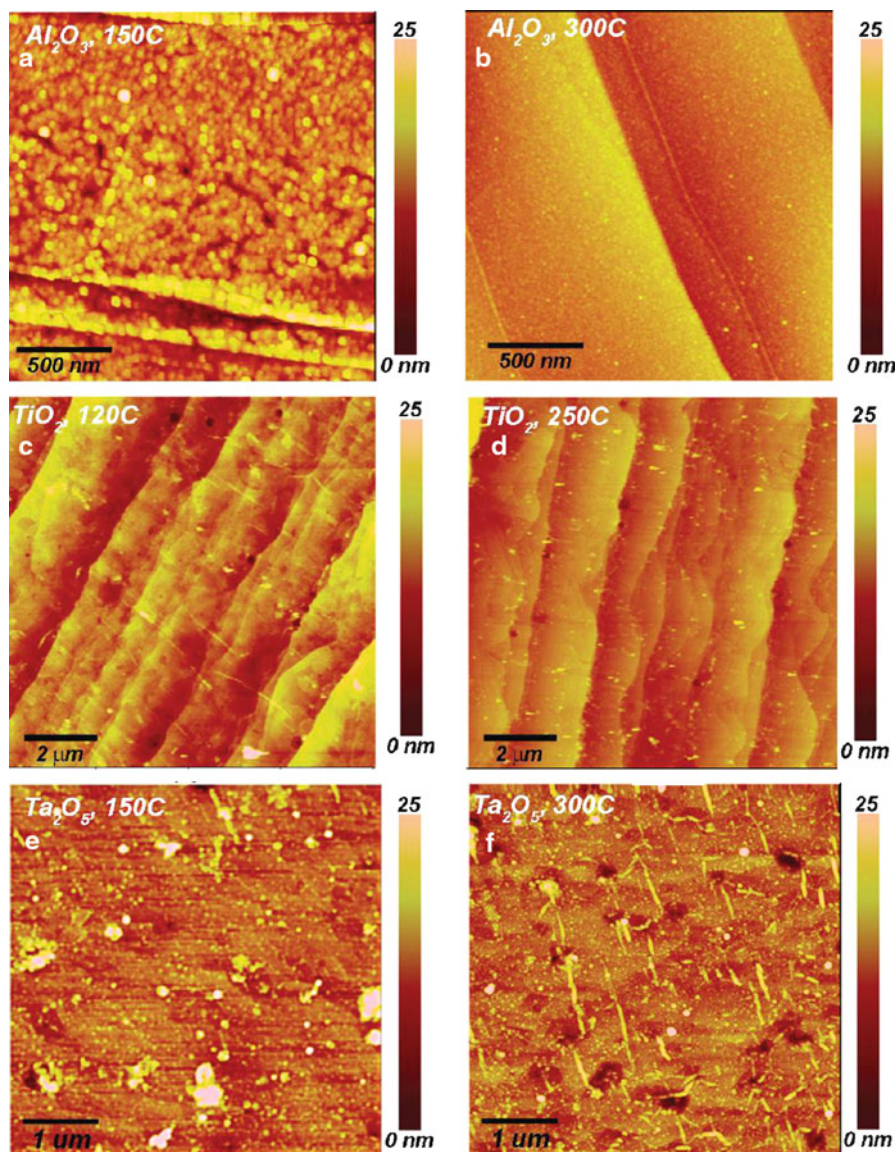


Fig. 9.11 Film uniformity and coverage on seeded graphene is dependent on deposition temperature. Atomic force microscopy images of seeded Al_2O_3 , TiO_2 , Ta_2O_5 films. Films deposited on graphene via ALD indicates that Al_2O_3 requires temperatures $>150^\circ\text{C}$ while complete coverage of TiO_2 and Ta_2O_5 occurs at $\leq 150^\circ\text{C}$. The use of Ta_2O_5 as a dielectric material, however, may result in an unacceptable surface roughness for subsequent device fabrication (Reproduced with permission from [30]. © 2010 American Chemical Society)

to 300°C, morphology was still nonconformal and rough. In addition, TiO₂ films had good uniformity and showed no dependence on ALD temperature, while Ta₂O₅ had poor film morphologies under all temperatures investigated. ALD of Ta₂O₅, even with a continuous metal seed layer, resulted in large particulates and buckling that left peak-to-valley heights of greater than 50 nm. These morphology results imply that Ta₂O₅ may not be a viable gate dielectric for graphene transistors unless significant improvement in deposition technology occurs.

Raman measurements performed before and after depositing the metal seed/oxide stack show an increase in the D/G ratio from 0.04 to 0.10 before to >0.1 after deposition. This suggests that the process introduces a slight increase in defects within the graphene lattice. Transmission electron microscopy (TEM) images also show that the top layer of all the graphene films have higher defect densities than the underlying layers, although it is unclear whether this is a true effect of the metal seed layer or simply a result of TEM sample preparation.

Non-destructive, contactless Leighton mobility measurements were taken on both as-grown graphene films and films after having undergone metal seed deposition, oxidation and ALD of each oxide. Both Al and Ta metal nucleation layers resulted in a decrease in mobility by as much as 25%, while the use of a Ti seed resulted in an increase in mobility of 10–22%. Additionally, HfO₂ films, which could be successfully deposited without a metal seed, showed no considerable change in mobility after deposition. Films deposited using the Ti metal seed layer also resulted in a reduction of the carrier concentration ($\sim 2\times$), most likely due to compensation doping by the metal seed. These results suggest that integration of TiO₂ could improve transistor gate performance, but it should be noted that previous integration into silicon- and silicon carbide-based transistors often resulted in high gate leakage during device operation [35, 51, 52].

This section has shown that fully oxidized, e-beam metal seed layers are a viable method for obtaining uniform high- κ dielectric films on graphene. The choice of seeding layer, as well as preparation of the graphene prior to seeding, is critical to reduce interaction with the graphene lattice which subsequently results in additional defects and degrades the electrical properties of the underlying graphene.

9.4 Summary and Future Directions

Since the application of gated graphene electronic devices are envisioned to manifest dimensions less than 100 nm, high- κ dielectrics are an essential component in the domain of future graphene applications. The implementation of these high- κ dielectrics is expected to improve the channel mobility by screening charged impurities and to reduce the high leakage currents in traditional SiO₂ gated oxides. Deposition of these dielectric oxides on graphene however, has proven to be a formidable challenge due to the highly hydrophobic and chemically inert nature of graphene. When direct deposition has been used, this has resulted in selective growth at the step edges and occasionally on the basal planes. Such irregularities in surface

coverage prompted researchers to develop suitable surface preparation approaches before oxide depositions. Moreover, any functionalization of the graphene surface, which is needed to nucleate the oxide layer, should not degrade the performance of device operation. Functionalization methods explored to date often deteriorate the graphene lattice and enhance electronic scattering in the graphene layer, leading to significant reductions in carrier mobility. As a result of impurity incorporation and structural damage to the graphene during functionalization and subsequent ALD, mobility values in top-gated devices are still below those observed in back-gated devices, and large fixed charges result in significant shifts of the Dirac voltage. Correlation between oxide morphology, electronic properties of the graphene, and device performance is still scarce and requires further studies. Each method has some advantages, limitations, and unknowns impacting the ALD on graphene, making it difficult to choose a leading functionalization technique. There is still much room for improvement in the ALD of oxides on graphene in order to fully realize the potential of graphene-based technologies.

Acknowledgements The authors thank L.O. Nyakiti, N. Nepal, R.L. Myers-Ward, J.K. Hite, G.G. Jernigan, and C.R. Eddy, Jr, for helpful discussions, and Dr. Eva Darian for providing Fig. 9.1(a). This work was supported by the Office of Naval Research. VDW is grateful for a postdoctoral fellowship from ASEE.

References

1. Novoselov, K.S., et al., *Electric field effect in atomically thin carbon films*. Science, 2004. **306**(5296): p. 666–669.
2. Novoselov, K.S., et al., *Two-dimensional gas of massless Dirac fermions in graphene*. Nature, 2005. **438**(7065): p. 197–200.
3. Geim, A.K. and K.S. Novoselov, *The rise of graphene*. Nature Materials, 2007. **6**(3): p. 183–191.
4. Lee, C., et al., *Measurement of the elastic properties and intrinsic strength of monolayer graphene*. Science, 2008. **321**(5887): p. 385–388.
5. Jenkins, K.A., et al. *Graphene RF transistor performance*. in ECS Transactions. Vancouver, BC.
6. Lin, Y.M., et al., *100-GHz transistors from wafer-scale epitaxial graphene*. Science. **327** (5966): p. 662.
7. Farmer, D.B., et al., *Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors*. Nano Letters, 2009. **9**(12): p. 4474–4478.
8. Moon, J.S., et al., *Epitaxial-graphene RF field-effect transistors on Si-face 6 H-SiC substrates*. IEEE Electron Device Letters, 2009. **30**(6): p. 650–652.
9. Konar, A., T.A. Fang, and D. Jena, *Effect of high-kappa gate dielectrics on charge transport in graphene-based field effect transistors*. Physical Review B, 2010. **82**(11): p. 115452.
10. Liao, L. and X. Duan, *Graphene-dielectric integration for graphene transistors*. Materials Science and Engineering R: Reports. **70**(3–6): p. 354–370.
11. Lu, Q., et al., *Leakage current comparison between ultra-thin Ta2O5 films and conventional gate dielectrics*. Ieee Electron Device Letters, 1998. **19**(9): p. 341–342.
12. Suntola, T., *Atomic layer epitaxy*. Material Science Reports/Material Science Reports, 1989. **4**(7): p. 261–312.

13. George, S.M., A.W. Ott, and J.W. Klaus, *Surface chemistry for atomic layer growth*. Journal of Physical Chemistry, 1996. **100**(31): p. 13121–13131.
14. Puurunen, R.L., *Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process*. Journal of Applied Physics, 2005. **97**(12): p. 1–52.
15. Suntola, T. and J. Anston. 1977.
16. Suntola, T., *Atomic Layer Epitaxy*, in *Handbook of Crystal Growth*, D.T.J. Huerle, Editor. 1994, Elsevier: Amsterdam.
17. Seidel, T.E., *Atomic Layer Deposition*, in *Handbook of Semiconductor Manufacturing Technology*, R.D.a.Y. Nishi, Editor. 2008, CRC Press
18. Leskelä, M.R.a.M., in *Handbook of Thin Film Materials*, H.S. Nalwa, Editor. 2002, Academic Press: San Diego. p. 103–159.
19. Ritala, M., *Atomic layer deposition*. High-K Gate Dielectrics, 2004: p. 17–64.
20. Wang, X.R., S.M. Tabakman, and H.J. Dai, *Atomic layer deposition of metal oxides on pristine and functionalized graphene*. Journal of the American Chemical Society, 2008. **130**(26): p. 8152–8153.
21. Bongki, L., et al., *Conformal Al/sub 2/O/sub 3/dielectric layer deposited by atomic layer deposition for graphene-based nanoelectronics*. Applied Physics Letters, 2008: p. 203102–1-3.
22. Speck, F., et al., *Atomic layer deposited aluminum oxide films on graphite and graphene studied by XPS and AFM*. Physica Status Solidi C: Current Topics in Solid State Physics, Vol 7, No 2, 2010. **7**(2): p. 398–401.
23. Garces, N.Y., et al., *Epitaxial Graphene Surface Preparation for Atomic Layer Deposition of Al₂O₃*. Journal of Applied Physics, 2011. **109**(12).
24. Xuan, Y., et al., *Atomic-layer-deposited nanostructures for graphene-based nanoelectronics*. Applied Physics Letters, 2008: p. 013101–1-3.
25. Pirkle, A., et al., *The effect of graphite surface condition on the composition of Al₂O₃ by atomic layer deposition*. Applied Physics Letters. **97**(8).
26. Lee, B., et al., *Atomic-Layer-Deposited Al₂O₃ as Gate Dielectrics for Graphene-Based Devices*. ECS Transactions, 2009. **19**(5): p. 225–230.
27. Farmer, D.B. and R.G. Gordon, *Atomic layer deposition on suspended single-walled carbon nanotubes via gas-phase noncovalent functionalization*. Nano Letters, 2006. **6**(4): p. 699–703.
28. Lin, Y.M., et al., *Operation of Graphene Transistors at Gigahertz Frequencies*. Nano Letters, 2009. **9**(1): p. 422–426.
29. Pirkle, A., R.M. Wallace, and L. Colombo, *In situ studies of Al₂O₃ and HfO₂ dielectrics on graphite*. Applied Physics Letters, 2009. **95**(13).
30. Robinson, J.A., et al., *Epitaxial Graphene Materials Integration: Effects of Dielectric Overlayers on Structural and Electronic Properties*. Acs Nano, 2010. **4**(5): p. 2667–2672.
31. Dimitrakopoulos, C., et al., *Wafer-scale epitaxial graphene growth on the Si-face of hexagonal SiC (0001) for high frequency transistors*. Journal of Vacuum Science & Technology B, 2010. **28**(5): p. 985–992.
32. Koehler, F.M., et al., *Permanent pattern-resolved adjustment of the surface potential of graphene-like carbon through chemical functionalization*. Angewandte Chemie - International Edition, 2009. **48**(1): p. 224–227.
33. Yang, F.H. and R.T. Yang, *Ab initio molecular orbital study of adsorption of atomic hydrogen on graphite: Insight into hydrogen storage in carbon nanotubes*. Carbon, 2002. **40**(3): p. 437–444.
34. Zou, K., et al., *Deposition of High-Quality HfO₂ on Graphene and the Effect of Remote Oxide Phonon Scattering*. Physical Review Letters, 2010. **105**(12): p. -.
35. Robertson, J., *High dielectric constant gate oxides for metal oxide Si transistors*. Reports on Progress in Physics, 2006. **69**(2): p. 327–396.
36. Berger, C., et al., *Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics*. Journal of Physical Chemistry B, 2004. **108**(52): p. 19912–19916.

37. Emtsev, K.V., et al., *Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide*. Nature Materials, 2009. **8**(3): p. 203–207.
38. VanMil, B.L., et al., *Graphene Formation on SiC Substrates*. Silicon Carbide and Related Materials 2008, 2009. **615–617**: p. 211–214.
39. Jernigan, G.G., V.D. Wheeler, and N.Y. Garces, *Presented at the 58th AVS Meeting*. Nashville, TN, Oct 30–Nov 4, 2011.
40. Lin, Y.M., et al., *Operation of graphene transistors at gigahertz frequencies*. Nano Letters, 2009. **9**(1): p. 422–426.
41. Williams, J.R., L. DiCarlo, and C.M. Marcus, *Quantum hall effect in a gate-controlled p-n junction of graphene*. Science, 2007. **317**(5838): p. 638–641.
42. Chen, J.H., et al., *Intrinsic and extrinsic performance limits of graphene devices on SiO₂*. Nature Nanotechnology, 2008. **3**(4): p. 206–209.
43. Jackson, S.T. and R.G. Nuzzo, *Determining Hybridization Differences for Amorphous-Carbon from the Xps C-1s Envelope*. Applied Surface Science, 1995. **90**(2): p. 195–203.
44. Beamson, G., D.T. Clark, and D.S.L. Law, *Electrical conductivity during XPS of heated PMMA: Detection of core line and valence band tacticity effects*. Surface and Interface Analysis, 1999. **27**(2): p. 76–86.
45. Briggs, D. and G. Beamson, *Primary and Secondary Oxygen-Induced C1s Binding-Energy Shifts in X-Ray Photoelectron-Spectroscopy of Polymers*. Analytical Chemistry, 1992. **64**(15): p. 1729–1736.
46. Stone, P., et al., *An STM, TPD and XPS investigation of formic acid adsorption on the oxygen-precovered c(6*2) surface of Cu(110)*. Surface Science, 1998. **418**(1): p. 71–83.
47. Renault, O., et al., *Angle-resolved x-ray photoelectron spectroscopy of ultrathin Al₂O₃ films grown by atomic layer deposition*. Journal of Vacuum Science & Technology a-Vacuum Surfaces and Films, 2002. **20**(6): p. 1867–1876.
48. Alexander, M.R., G.E. Thompson, and G. Beamson, *Characterization of the oxide/hydroxide surface of aluminium using x-ray photoelectron spectroscopy: a procedure for curve fitting the O 1s core level*. Surface and Interface Analysis, 2000. **29**(7): p. 468–477.
49. Nair, R.R., et al., *Fluorographene: A two-dimensional counterpart of Teflon*. Small. **6**(24): p. 2877–2884.
50. Kim, S., et al., *Realization of a high mobility dual-gated graphene field-effect transistor with Al₂O₃ dielectric*. Applied Physics Letters, 2009. **94**(6).
51. Wilk, G.D., R.M. Wallace, and J.M. Anthony, *High-kappa gate dielectrics: Current status and materials properties considerations*. Journal of Applied Physics, 2001. **89**(10): p. 5243–5275.
52. Mahapatra, R., et al., *Leakage current and charge trapping behavior in TiO₂/SiO₂ high-kappa gate dielectric stack on 4 H-SiC substrate*. Journal of Vacuum Science & Technology B, 2007. **25**(1): p. 217–223.

List of Abbreviations

Chapter 1

CMOS	Complimentary metal oxide semiconductor
DIBL	Drain-induced barrier lowering
FDSOI	Fully-depleted silicon-on-insulator
HEMT	High electron mobility transistor
MOSFET	Metal-oxide-semiconductor field effect transistor
SRAM	Static random-access memory

Chapter 2

2D	Two dimension
2DEG	Two-dimensional electron gas
AFM	Atomic force microscope
ARPES	Angle resolved photoemission spectroscopy
CVD	Chemical vapor deposition
DFT	Density functional theory
EG	Epitaxial graphene
FET	Field effect transistor
GNR	Graphene nanoribbon
HOMO	Highest occupied molecular orbital
LA	Longitudinal acoustic
LUMO	Lowest unoccupied molecular orbital
MBE	Molecular beam epitaxy
PMMA	Poly (methyl methacrylate)
ROP	Remote oxide phonon
STM	Scanned tunneling microscopy
TEM	Transmission electron microscope

Chapter 3

AES	Auger electron spectroscopy
AFM	Atomic force microscopy
ARPES	Angle resolved photoelectron spectroscopy
BG, TG	Bottom- and top- gated
CDG	Chemically derived graphene
CMOS	Complementary metal oxide semiconductor
CNT	Carbon nanotube
CVD	Chemically derived graphene
DIBL	Drain induced barrier lowering
DOS	Density of states
GFET	Graphene FET
GNR	Graphene nanoribbon
HSQ	Hydrogen silsesquioxane
MLG	Multi-layered graphene
MOSFET	Metal oxide semiconductor field effect transistor
NSOM	Near-field scanning optical microscopy
PEI	Poly (ethylene imine)
RF	Radio frequency
SCE	Short channel effects
SCPM	Scanning photocurrent microscopy
SLG, BLG, TLG	Single-, bi-, tri- layer graphene
TMAH	Tetramethyl ammonium hydroxide

Chapter 4

BiSFET	Bilayer pseudospin field effect transistor
MOSFET	Metal oxide semiconductor field effect transistor
GNR	Graphene nanoribbon
CMOS	Complementary metal oxide semiconductor
RF	Radio frequency
THz	Tera hertz
SO	Spin orbit
STTRAM	Spin torque transfer random access memory

Chapter 5

FET	Field effect transistor
MOS	Metal oxide semiconductor
DIBL	Drain induced barrier lowering
ITRS	International technology roadmap for semiconductors
SWB	Spin wave bus

Chapter 6

AES	Auger electron spectroscopy
AFM	Atomic force microscope
ARPES	Angle resolved photoemission spectroscopy
FET	Field effect transistor
IFL	Interfacial layer
LEED	Low energy electron diffraction
QHE	Quantum hall effect
STM	Scanning tunneling microscopy
TEM	Transmission electron microscopy
UHV	Ultra high vacuum
XPS	X-ray photoemission spectroscopy

Chapter 7

APCVD	Atmospheric pressure CVD
CVD	Chemical vapor deposition
FET	Field effect transistor
LEED	Low energy electron diffraction
LEEM	Low energy electron microscopy
PDMS	Poly dimethoxy silane
PECVD	Plasma enhanced CVD
PET	Polyethylene terephthalate
PMMA	Poly methyl methacrylate
SLG, BLG, FLG	Single/bi/tri layer graphene
STEM	Scanning transmission electron microscopy
STM	Scanning tunneling microscopy
TEM	Transmission electron microscopy

Chapter 8

AFM	Atomic force microscopy
CCG	Chemically converted graphene
DMF	N,N-dimethylformamide
EFTEM	Energy filtered transmission electron microscopy
GIC	Graphite intercalation compounds
GO	Graphene oxide
GONR	Graphene oxide nanoribbon
NMP	N-methyl, 2-pyrrolidone
NMR	Nuclear magnetic resonance
ODCB	Ortho-dichlorobenzene
SDBS	Sodium dodecylbenzene sulfonate
STM	Scanning tunneling microscopy
SW/MW-CNT	Single-wall/multi-wall carbon nanotube
TBA	Tetrabutylammonium hydroxide
TEG	Thermally expanded graphite

TEM	Transmission electron microscopy
THF	Tetrahydrofuran
VRH	Variable range hopping
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

Chapter 9

AFM	Atomic force microscopy
Al ₂ O ₃	Aluminum oxide
ALD	Atomic layer deposition
AlN	Aluminum nitride
CH ₃	Methyl
CH ₄	Methane
CMOS	Complementary metal oxide semiconductor
C–V	Capacitance–voltage
CVD	Chemical vapor deposition
DI	Deionized
EG	Epitaxial graphene
FETs	Field effect transistors
GHz	Gigahertz
H ₂ O ₂	Hydrogen peroxide
HF	Hydrofluoric acid
HfC	Hafnium carbide
HfCl ₄	Hafnium tetrachloride
HfO ₂	Hafnium oxide
High- κ	High dielectric constant
HOPG	Highly-oriented pyrolytic graphite
NH ₄ O ₄	Ammonium hydroxide
NO ₂	Nitrous oxide
O ₃	Ozone
O–H	Hydroxyl
PGMEA	Propylene glycol monomethyl ether acetate
PTCA	Perylene tetracarboxylic acid
SC1	Standard clean 1
SEM	Scanning electron microscopy
SiC	Silicon carbide
SiO ₂	Silicon dioxide
Ta ₂ O ₅	Tantalum oxide
TEM	Transmission electron microscopy
TiO ₂	Titanium dioxide
TMA	Trimethylaluminum
UHV	Ultra high vacuum
V _{Dirac}	Dirac voltage
wt%	Weight percentage
XPS	X-ray photoelectron spectroscopy

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